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Investigation of properties of thin silicon pixel detectors before and after particle irradiation

Untersuchung von Eigenschaften dünner Silizium Pixeldetektoren vor und nach Teilchenbestrahlung

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Betreut von Priv.-Doz. Dr. Richard Nisius



To my grandfather Shri A.M. Banerjee and my parents.

॥ শ্রীজগন্নাথস্তোত্র ১ ॥

॥ জগন্নাথপ্রণামঃ ॥

নীলাচলনিবাসায় নিত্যায় পরমাত্মনে ।
বলভদ্রসুভদ্রাভ্যাং জগন্নাথায় তে নমঃ ॥ ১॥
জগদানন্দকন্দায় প্রণতর্ভরায় চ ।
নীলাচলনিবাসায় জগন্নাথায় তে নমঃ ॥ ২॥

॥ শ্রী জগন্নাথ প্রার্থনা ॥

রত্নাকরস্তব গৃহং গৃহিণী চ পদ্মা
কিং দেয়মস্তি ভবতে পুরুষোত্তমায় ।
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দত্তং মনো যদুপতে ত্বরিতং গৃহাণ ॥ ১॥
ভক্তানামভয়প্রদো যদি ভবেত্ কিস্তদ্বিচিত্রং প্রভো
কীটোহপি স্বজনস্য রক্ষণবিধাবেকান্তমুদ্বিজিতঃ ।
যে যুগ্মচ্চরণাবিন্দবিমুখা স্বপ্নেহপি নালোচকা-
স্তেষামুদ্ধরণ-ক্ষমো যদি ভবেত্ কারুণ্যসিকুস্তদা ॥ ২॥
অনাথস্য জগন্নাথ নাথস্ত্বং মে ন সংশয়ঃ ।
যস্য নাথো জগন্নাথস্তস্য দুঃখং কথং প্রভো ॥ ৩॥
যা ত্বরা দ্রৌপদীত্রাণে যা ত্বরা গজমোক্ষণে ।
ময়্যার্ভে করুণামূর্তে সা ত্বরা ক্ব গতা হরে ॥ ৪॥
মত্সমো পাতকী নাস্তি ত্বত্সমো নাস্তি পাপহা ।
ইতি বিজায় দেবেশ যথাযোগ্যং তথা কুরু ॥ ৫॥

Abstract

ATLAS is one of the two general purpose experiments at the Large Hadron Collider (LHC) at CERN and it addresses the most fundamental questions of particle physics. In two long shut down periods the LHC and all its experiments will be upgraded for the High Luminosity LHC. This will extend the present discovery potential of the LHC. However, the present LHC detectors will not be able to withstand the higher particle track density and the corresponding high levels of radiation. To meet the experimental challenges of the increased peak luminosity of $7 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ (i.e. almost 3 times the luminosity achieved in LHC Run II) the entire ATLAS inner detector will be replaced by the new all silicon inner tracker (ITk).

The pixel detector, being the innermost part of the ITk, is expected to be exposed to a radiation fluence of up to $1.4 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$. A new read-out chip prototype, called the RD53A read-out chip, was designed by the RD53 Collaboration with a read-out cell size of $50 \times 50 \mu\text{m}^2$ which results in a higher granularity with respect to the present minimum read-out cell size of $50 \times 250 \mu\text{m}^2$. Sensors with pixel cell sizes of $50 \times 50 \mu\text{m}^2$ and $25 \times 100 \mu\text{m}^2$, compatible with the RD53A read-out chip were also designed.

In course of this thesis, two aspects were studied. The first, is the characterisation of thin n^+ -in-p planar pixel sensors. In this part, the breakdown voltages are identified for the different sensor designs with and without punch through dots to select the design resulting in the best performance. To allow for a measurement of IV characteristics, a TiW barrier layer was used to short the pixel cells without biasing structures at an intermediate step of the production. The charge collection and threshold properties were also investigated. It was demonstrated that modules with sensors interconnected with the RD53A read-out chip, deplete at low voltages, due to the high bulk resistivity of the sensors investigated here. Furthermore, the threshold of the RD53A readout chip was independently measured and found compatible with the value determined from the internal calibration mechanism. The second part of this thesis was the extraction of the effective band gap energy E_{eff} for irradiated sensors. It was observed that in the temperature range from -20°C to -45°C for sensors irradiated to fluences in the range from $2 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ to $1 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$, the E_{eff} ranges from $1.22 \pm 0.01 \text{ eV}$ to $1.33 \pm 0.05 \text{ eV}$.

Contents

1	Introduction	1
1.1	The LHC and the ATLAS experiment	2
1.2	The LHC and ATLAS upgrades	6
1.3	The ATLAS inner tracker upgrade	7
2	Theory of silicon detectors	9
2.1	Basics of semiconductors	9
2.2	The pn-junction	11
2.3	Depletion voltage and leakage current	11
2.4	Charge generation and collection	13
2.5	Effects of radiation damage	16
3	The ATLAS pixel sensors	18
3.1	Pixel sensor concepts	18
3.2	Processing of pixel sensors	18
3.3	Pixel sensor structures	20
3.4	Sensor production at the Max-Planck-Society Halbleiter Labor	22
3.5	The RD53A ATLAS read-out chip	24
3.6	Hybrid pixel detectors	26
4	Experimental set-up	28
4.1	Sensor characterisation	28
4.1.1	Measurement of leakage current as a function of bias voltage	28
4.1.2	Measurement using radioactive sources	31
4.2	The BDAQ53 read-out system	31
4.2.1	Hardware components	31
4.2.2	Read-out Software	33
5	Sensor characteristics	38
5.1	Characterisation of IV	38
5.2	Charge collection	49
5.2.1	Laboratory measurements	49
5.2.2	Test beam results	49
5.3	Properties of the target threshold	54
6	The effective band gap energy of irradiated sensors	58
6.1	Effect of uncertainties in temperature in the effective band gap energy measurements	59

6.2	Calibration of the probe station	61
6.3	Extraction of effective band gap energy	62
Conclusions		69
Acknowledgements		71
List of Figures		72
List of Tables		75
Abbreviations and acronyms		76
Bibliography		78

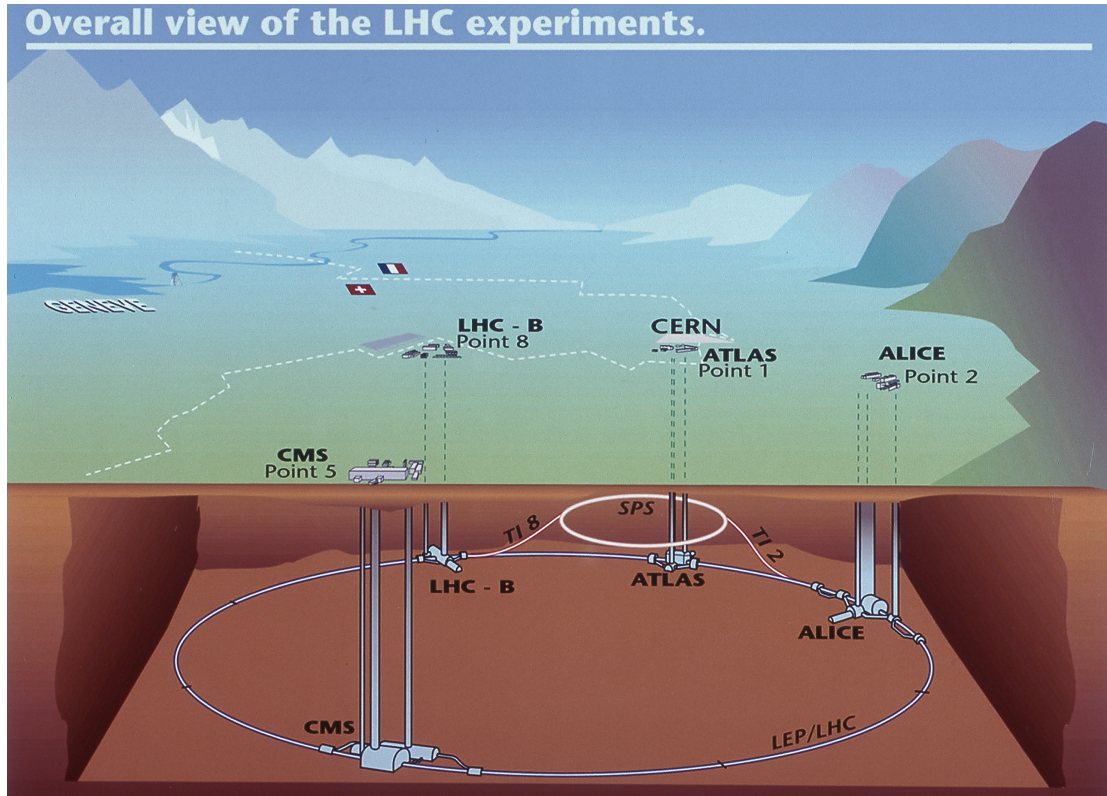


Figure 1.1: This diagram shows the locations of the four main experiments (ALICE, ATLAS, CMS and LHCb) that are installed at the LHC. Located between 50 m and 150 m underground, huge caverns had been excavated to house the giant detectors. The SPS, the last pre-accelerator in the chain, and its connection tunnels to the LHC are also shown. This image has been taken from [1].

1 Introduction

There are many fundamental and open questions in particle physics as, for example, the nature of dark matter, fermion mass hierarchy, matter-antimatter asymmetry and the existence of a graviton. Over the last decades, the Standard Model (SM) of particle physics was able to describe the elementary matter constituents and their interactions [2], [3,4] and was tested to very high precision. To answer all this and specifically to search for the boson predicted by the electroweak symmetry breaking [5–7] that provides mass to particles, the Large Hadron Collider (LHC) was built. The latest step in its successful history was marked by the observation of the Higgs boson with a mass around 125 GeV [8,9].

This chapter describes and motivates the LHC and the ATLAS detector and their upgrades. Chapter 2 provides the basic concepts of semiconductor detectors. Chapter 3 describes the fabrication process and the production steps of thin n^+ -in-p planar sensors as the baseline sensors for the ATLAS pixel detector that have been studied in this thesis. Chapter 4 describes the experimental setup for sensor characterisation. Chapter 5 presents the obtained results for sensor characterisation from the laboratory and test beam measurement. And lastly, Chapter 6 presents the obtained results from the band gap energy measurements.

1.1 The LHC and the ATLAS experiment

The LHC was constructed in the already existing 27 km long Large Electron-Positron Collider (LEP) tunnel [10], [11]. It is located at the Conseil Européen pour la Recherche Nucléaire (CERN) in Geneva. The accelerator is designed for proton-proton collisions up to a centre of mass energy of $\sqrt{s} = 14$ TeV and lead ion collisions up to $\sqrt{s} = 1.15$ PeV [12]. Two proton beams circulating in opposite directions in separate beam pipes are brought to collision at four interaction points (IPs). The same is also done using heavy ions. The injection chain for the LHC, shown in Figure 1.2 is a chain of accelerators with the LHC being the final accelerator ring [13]. Protons extracted from ionised H_2 are accelerated in bunches in the LINear ACcelerator (LINAC) 2 up to an energy of 50 MeV before they are injected to the Booster to be accelerated to an energy of 1.4 GeV. Further accelerating steps within the Proton Synchrotron (PS) and the Super proton Synchrotron (SpS) increase the energy further to 25 GeV and 450 GeV respectively. From the SpS, the proton bunches are injected in two opposing directions into the LHC to finally collide at the experiments. In case of heavy ion collisions, lead ions are accelerated first in the LINAC 3 and then in the Low Energy Ion Ring (LEIR) before being injected into the PS. From there, they follow the same course of acceleration as the protons to enter the LHC for eventual collision. Both operation modes can also be combined to collide protons with lead ions [14]. The detectors of the four main experiments LHC-based are located at these IPs as listed below:

1. A Toroidal LHC Apparatus (ATLAS) [15]: It is one of the two general multi-purpose experiments and performs high precision measurements on SM parameters and the Higgs boson and searches for several new physics processes that may be expected at the TeV scale. ATLAS is the largest LHC detector. It employs two magnets, a solenoid for the inner detector and a toroid for the muon spectrometer.
2. Compact Muon Solenoid (CMS) [16]: It is the other general multi-purpose experiment with a scope of discovery the same as ATLAS though the experimental design i.e. the hardware and software is different. It is designed such that it can generate a unique non-linear magnetic field up to 4 T using a solenoidal magnet.
3. Large Hadron Collider beauty (LHCb) [17]: This experiment has been designed to measure the parameters of CP violation in the interactions of b-hadrons. The detector is designed as a 20 m long single arm spectrometer, with its sub-detectors stacked behind each other like books on a shelf.

4. A Large Ion Collider Experiment (ALICE) [18]: This experiment investigates quark-gluon plasma properties with a luminosity of $10^{27} \text{ cm}^{-2} \text{ s}^{-1}$ mainly for lead-lead ion nuclei (Pb-Pb) operation.

The ATLAS detector is 46 m long, has a diameter of 25 m, and weighs 7000 t. The parts of the detector are arranged in layers. Figure 1.3 shows a cross-section of the detector while Figure 1.4a depicts how the ATLAS detector identifies the particles from the collision. The main detector has the following sub-parts:

1. The Inner Detector (ID) is the sub-detector closest to the IP and is made of three different detectors: the pixel detector, the SemiConductor Tracker (SCT) made of silicon strip detectors and the Transition Radiation Tracker (TRT) made of thin drift tubes filled with gas. Figure 1.4b shows all the parts of the ID. It is designed for momentum and vertex measurements along with identification of electric charge of electrically charged particles. It is also used to reconstruct short-lived particles from their decay products. A 2 T magnetic field along the direction of the beam from a superconducting solenoid surrounds and therefore influences the ID. The pixel detector within the ID, hosts the Insertable B-Layer (IBL) that was inserted in 2014 along with the original three barrel layers and their respective end-caps. The main motivation behind the insertion of the IBL from Ref.

citeReemThesis10, ReemThesis11, was to compensate for the inefficiencies of the original pixel layers due to prolonged exposure to high levels of radiation. Moreover, with the reduced radial distance of the IBL from the beam line 3.3 cm, the tracking resolution is enhanced. It covers a wider range with pseudorapidity $0 < |\eta| < 2.5$, where η is the spatial coordinate describing the angle of a particle relative to the beam axis. The following equation is used to calculate the pseudorapidity,

$$\eta \equiv -\ln\left[\tan\left(\frac{\theta}{2}\right)\right] \quad (1.1)$$

where θ the angle between the particle three-momentum and the direction of the beam axis. Around the pixel detector, is the SCT detector. It is made of silicon micro-strips instead of pixels. It also has four barrel layers like the present pixel detector. The micro-strips have larger readout structures and therefore reduced spatial resolution and cost with respect to pixel detectors. This part of the ID is suitable to cover areas at the outer radii. After the pixel and SCT detectors, the TRT is located. It is composed of straw tubes with 4 mm of diameter filled with a mixture of ionising gas (mostly xenon) [12]. To distinguish between pions and electrons i.e. transition radiation hits and track hits, radiation foils and fibres are placed between the tubes.

2. The next layer is the calorimeter system consisting of the Electromagnetic CALorimeter (ECAL) and the Hadronic CALorimeter (HCAL). The main purpose of these calorimeters is to measure the energy of the particles, jets and missing transverse energy. The ECAL is a sampling calorimeter composed of Liquid Argon (LAr) as active material and lead plates as absorbers. It is designed to stop and measure the

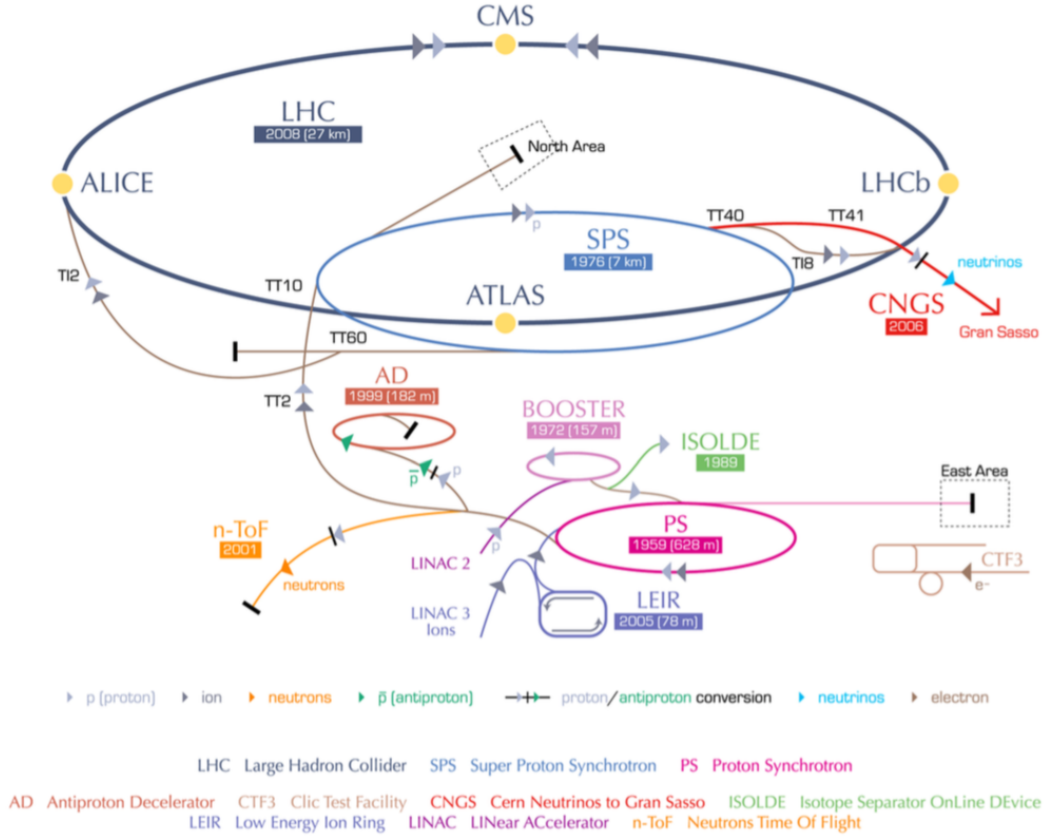


Figure 1.2: The LHC accelerator complex is composed of the LHC shown in black and the injection complex, which help to boost the particles to their final energies. This image has been taken from [19].

energy of electrons and photons. The HCAL, on the other hand is a scintillator-steel sampling detector designed to measure the energy of hadronic particles. These calorimeters absorb most particles with the exception of muons and neutrinos. The HCAL the end-caps employ copper absorbers for electromagnetic showers and tungsten absorbers for hadronic showers with LAr filled in between the absorber plates.

3. Lastly, the outermost part of the detector is the muon spectrometer (MS) immersed in an inhomogeneous magnetic field of 4 T generated by a system of toroidal magnets. It is made of Monitored Drift Tubes (MDTs), Cathode Strip Chambers (CSCs), Resistive Plate Chambers (RPCs) and Thin Gap Chambers (TGCs). The MS as its name suggests, measures muon properties by employing the toroidal magnetic field to bend the muon tracks accordingly. The MDTs and CSCs implemented in the barrel region measure the tracks with high-precision and the RPCs and the TGCs implemented in the end-caps provide bunch-crossing and trigger information.

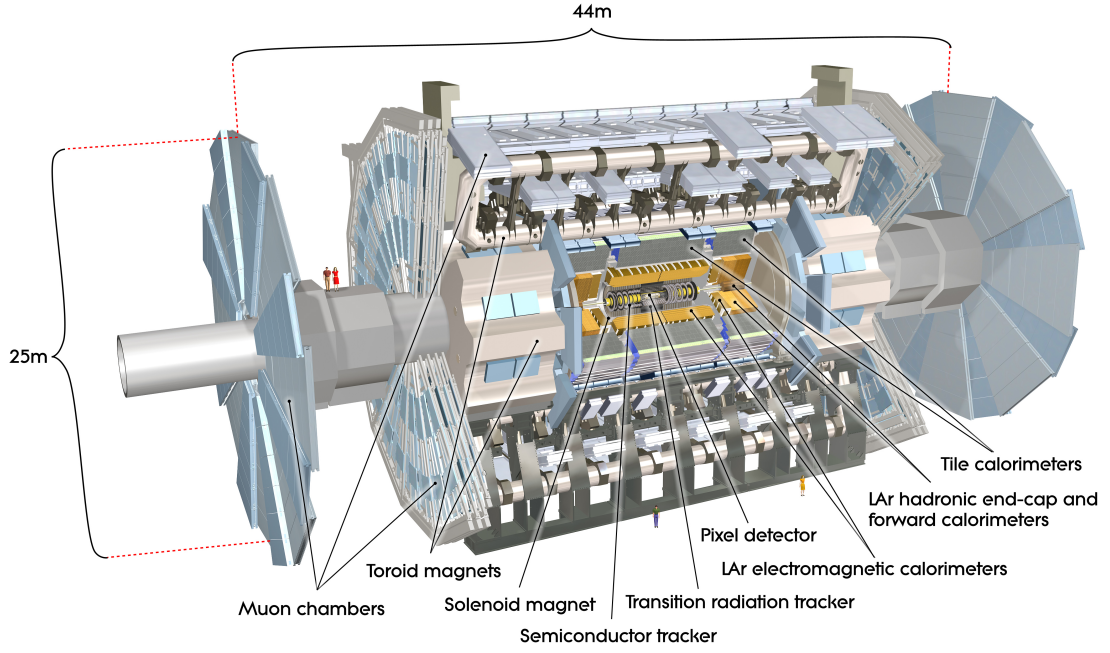


Figure 1.3: The cross-section of the ATLAS experiment showing the inner detector, calorimeters and the muon spectrometer for increasing radius. This image has been taken from [1].

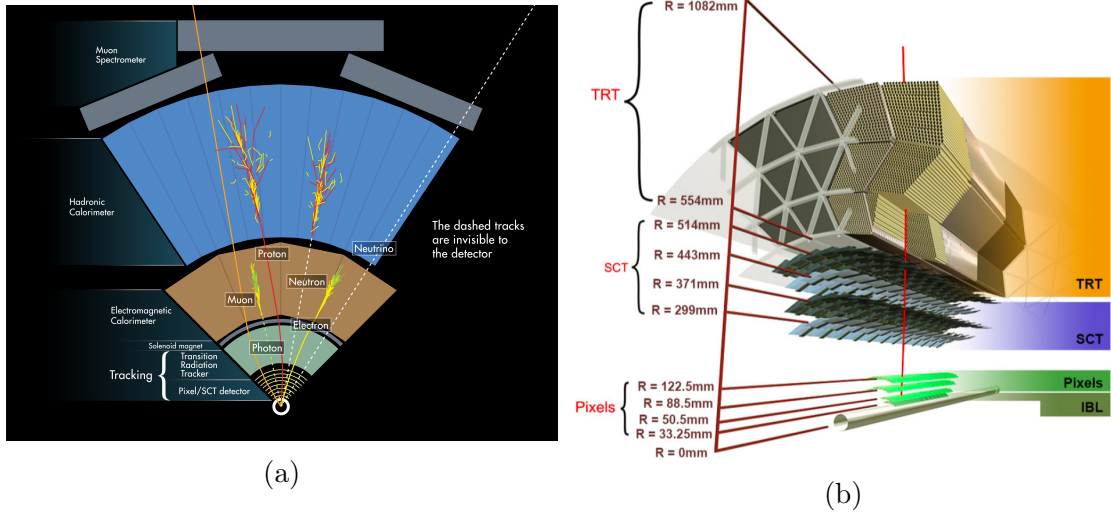


Figure 1.4: In (a) a computer generated image representing how ATLAS detects particles taken from [1] is shown and in (b) a schematic representation of the cross-section of the present inner detector taken from [20] is shown.

1.2 The LHC and ATLAS upgrades

The present centre of mass energy for pp collisions is $\sqrt{s} = 13$ TeV with a peak instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ in the current running in 2018. The quantity that measures the ability of a particle accelerator to produce the required number of interactions is called the luminosity and is the proportionality factor between the number of events per second and the cross section. The number of interactions per second is the instantaneous luminosity. However the final figure of merit is the so-called integrated luminosity as it directly relates to the number of observed events. For a given physics process with a cross-section σ_{process} , the number of events N_{event} occurring is given by [14],

$$N_{\text{event}} = L\sigma_{\text{process}} \quad (1.2)$$

where L is the integrated luminosity.

One pp collision may lead to several individual events on top of the hard interaction event known as pile-up events. The total cross-section is the probability of occurrence of a physical process and smaller the cross-section the rarer it is. From Equation 1.2, we know the number of events is proportional to the luminosity and total cross-section. Therefore, the higher the luminosity, greater the number of events. To see these rare processes, a greater number of events is required, consequently, a higher luminosity must be achieved. To find answers to the open questions by studying the rare events, the LHC and all the main experiments will undergo upgrades.

The LHC first started taking data in 2011 at $\sqrt{s} = 7$ TeV. The centre of mass energy was then increased to 8 TeV the following year. And on 4th July 2012, it was announced by CERN that the ATLAS and CMS experiments had observed the Higgs boson which had a mass of 125 GeV. The journey from LHC to High Luminosity LHC (HL-LHC) is divided into periods of running time and in between each of these runs there are long periods of shut down (LS) for accelerator and detector maintenance and upgrade. The runs are listed as follows:

1. Run-I (2011-2013) followed by LS1
2. Run-II (2015-2018) followed by LS2. Presently, the LHC is in its Run-II phase with $\sqrt{s} = 13$ TeV and bunch-crossing time of 25 ns. During LS2, it has been planned to replace the present LINAC 2 pre-accelerator which accelerates protons to 50 MeV with the LINAC 4 which will be able to accelerate protons to 160 MeV [20].
3. Run-III (2021-2023) followed by LS3. During the LS3 period, the LHC will be finally upgraded to HL-LHC. The accelerator and detector parts such as the quadrupole focusing magnets will be replaced such that a peak luminosity of $7 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ can be achieved.
4. Run-IV (from 2026 onwards)

The upgrade plans for the LHC is shown in Figure 1.5.

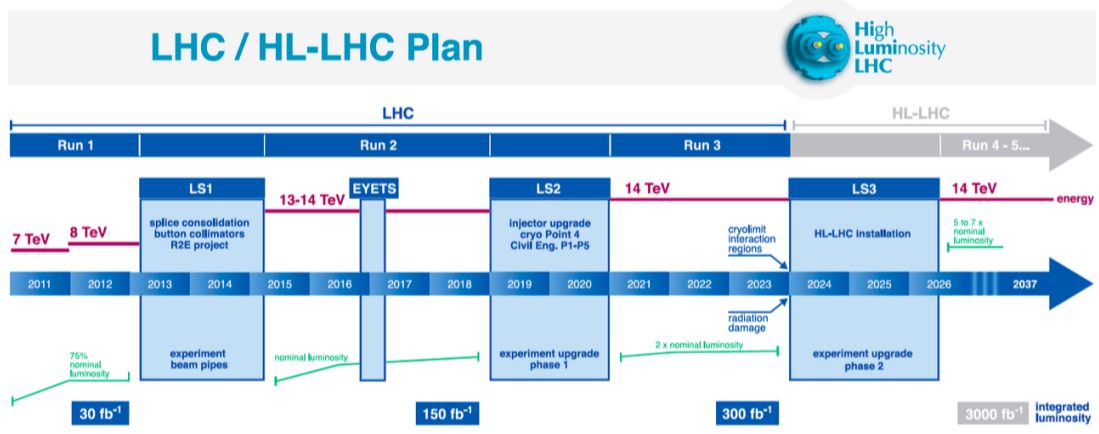


Figure 1.5: The LHC schedule toward HL-LHC. This image has been taken from [21].

Likewise, the ATLAS detector is being upgraded in three phases described as follows:

1. Phase 0 (LS1): During this time the IBL was inserted in the ID. The upgraded pixel modules, implemented in the IBL, are designed to be more radiation hard and have a higher granularity for readout chip and sensor to withstand the development of the fluence and the larger number of pile-up events as the LHC was proceeding to Run-II. Insertion of the IBL also increases the amount of material therefore multiple scattering. The sensor and the electronics were cooled with an improved new CO₂ system of reduced mass. In the MS a new neutron shielding was inserted which reduces the background. As background increases with luminosity, the steel beam pipes in the forward regions was replaced with aluminium ones. This helps in reducing the additional background from slow neutrons and photons [21].
2. Phase-I (LS2): The outer parts of the ATLAS detector will be upgraded in this time. Introduction of New Small Wheels (NSW) to improve the trigger system which reduces the rate of data acquisition is one such improvement.
3. Phase-II (LS3): From 2024 onwards, major parts of the ATLAS detector will be replaced for the HL-LHC. Additionally the readout electronics and trigger systems will also be upgraded.

1.3 The ATLAS inner tracker upgrade

For the HL-LHC, ID will be fully replaced by an all-silicon new ITk system. It needs to have a finer granularity for high precision tracking, reduced material budget, lower cost and higher radiation hardness to withstand the high fluence being closest to the IP. The new ITk will have 5 layers of pixel detectors and four layers of strip detectors. New modules with pixel cell geometries of $50 \times 50 \mu\text{m}^2$ and/or $25 \times 100 \mu\text{m}^2$ will be implemented. Due to the harsher environment of the HL-LHC, the two innermost layers are designed to

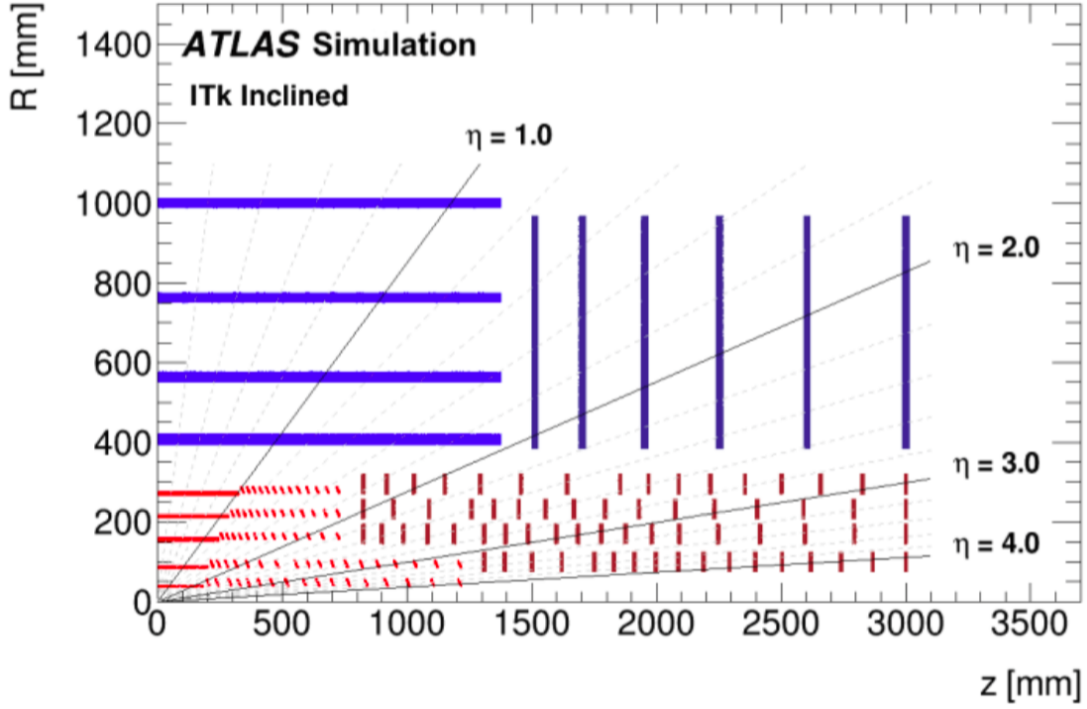


Figure 1.6: A schematic representation of one quadrant of the ITk system to be used at the HL- LHC. The image has been taken from [22].

be replaceable. Two different sensor technologies will also be implemented. The innermost layer of the pixel detector is to be made of 3D sensors designed to withstand irradiation up to a fluence of $1.4 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$ and the outer layers are to be made of thin planar sensors designed to withstand irradiation up to a fluence of $4 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$. The new ITk will additionally ensure a complete $|\eta|$ coverage up to 4.0 [22] as shown in Figure 1.6.

2 Theory of silicon detectors

Since the 1950s the field of semiconductor detectors have been constantly advancing. These solid-state detectors use crystalline semiconductor materials, mostly silicon and germanium and behave like solid-state ionisation chambers.

In their simplest form, these detectors are an absorbing medium coupled by a pair of electrodes connected to an external voltage source that creates an electric field in the semiconductor bulk in between. Any traversing particle creates electron-hole (e-h) pairs inside this bulk via ionisation. Under the influence of an applied field, these e-h pairs move towards their respective electrodes, thus generating a current flow. The average number of e-h pairs generated is proportional to the absorbed energy divided by the mean ionisation energy. The traversing particle is stopped inside the detector so that the signal is proportional to its energy in case of energy spectroscopy measurements.

In case of high energy tracking experiments instead, the particle deposits only a very small fraction of its energy thus yielding a high resolution position information. Multiple layers of such detectors make a track reconstruction possible and can be used for momentum and charge measurements.

2.1 Basics of semiconductors

The extraordinary properties of semiconductors reside in their energy-band structure. The band gap energy of any material is the energy difference between the conduction and the valence band. Conductors have a very small band gap or overlapping bands while insulators have a very large band gap. Semiconductors do not have either very small or non-existent band gap energies like the conductors or very large band gap energies like in insulators. They have a band gap energy around 1 eV. The difference between their band levels can be seen in Figure 2.1. Silicon (Si) has a band gap of 1.12 eV at 300 K and it changes with absolute temperature (T) in accordance to the Varshni equation [23]. This equation for Si is given by

$$E_g(T)[eV] = 1.17[eV] - \frac{(4.9 \cdot 10^{-4}[eV/K])T^2[K]^2}{T[K] + 655[K]} \quad (2.1)$$

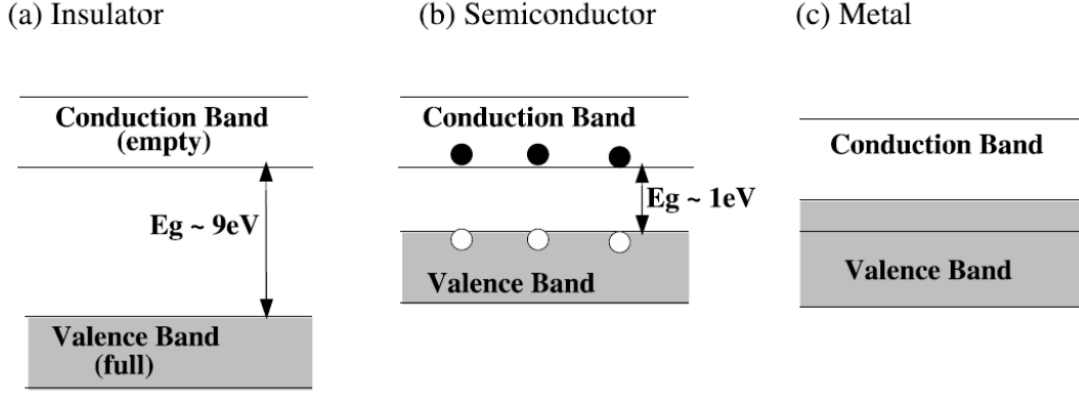


Figure 2.1: Schematic representations of band structures of (a) an insulator, (b) a semiconductor and (c) a conductor.

where $E_g(T)$ is expressed in eV, 1.17 eV is the band gap energy at 0 K, T is the temperature in K and 4.9×10^{-4} eV/K and 655 K are the α and β parameters. The E_g decreases with increase in temperature.

The probability of the occupancy of a specific energy state E in the band levels can be expressed by the Fermi-Dirac distribution:

$$f_e(E) = \frac{1}{\exp\left(\frac{E-E_F}{k_B T}\right) + 1} \quad (2.2)$$

where k_B is the Boltzmann constant and E_F the Fermi energy. The Fermi level is the highest occupied electron energy level at $T = 0$ K and lies between the valence and conduction band and its position is determined by the density of the charge carriers.

Semiconductors can be of two types: intrinsic or the pure semiconductor and extrinsic. An extrinsic semiconductor is an intrinsic semiconductor whose electrical properties and conductivity are enhanced and is controlled, with the introduction of a certain amount of impurities. This controlled addition of impurities is known as doping.

Two types of semiconductors are obtained using the doping process: the n-type donor semiconductor with negatively charged free majority carriers and the p-type acceptor semiconductors with positively charged free majority carriers. Silicon is a group IV element with four valence electrons. The addition of pentavalent impurities (group V material with 5 valence electrons) such as antimony (Sb), arsenic (As) or phosphorous (P), introduces an extra electron into the Si structure which is loosely bound such that it is easily excited into the conduction band at room temperature. The doping with these elements results in n-type silicon. While, the addition of trivalent impurities (group III material with 3 valence electrons) such as boron (B), aluminium (Al) or gallium (Ga) creates vacancies

in the valence band, producing free positive charge carriers known as ‘holes’ resulting in p-type silicon.

2.2 The pn-junction

The fundamental basis for a semiconductor detector is a pn-junction. A pn-junction is formed by joining together n-type and p-type silicon. This device has an excess of acceptor impurities in the p-region and donor impurities in the n-region. As soon as the p-n junction is formed there is an instant diffusion of the majority charge carriers across the junction caused by different concentration levels of holes and electrons in each side of the junction. Electrons of the n-region diffuse into the p-region and a holes of the p-region diffuse into the n-region. These diffused charge carriers interact with their respective complement counterparts around the junction region and neutralise each other. Therefore, in the vicinity of the junction there is a build up of positive charge on the n-side and negative charge on the p-region. This creates a potential difference across the junction and an internal electric field E is directed from the positive n-side to the negative p-side.

The remaining non-mobile positive ions on the n-side and the negative ions on the p-side generates a Space Charge Region (SCR) also known as depletion zone as this region is depleted of its free charge carriers in the vicinity of the junction. The electric field created in the SCR forms a barrier for further diffusion known as the potential barrier. The device reaches a state of equilibrium when the net current flow is zero i.e. drift current equals diffusion current. The potential difference which corresponds to the difference in the Fermi levels between the n and p-sides is known as the built-in voltage V_{bi} .

Assuming charge neutrality and a homogeneous SCR density ρ , the electric potential V can be obtained from solving the Poisson’s equation which takes the following form:

$$\nabla^2 V = -\frac{\rho}{\epsilon} = \frac{q_0 N_{eff}}{\epsilon_{Si} \epsilon_0} \quad (2.3)$$

where ∇^2 is the laplace operator i.e. the the divergence of the gradient of V , $N_{eff} = N_D - N_A$ in units of cm^{-3} is the effective doping concentration, i.e. the difference between the donor and acceptor concentration in the SCR, ϵ the dielectric constant and q_0 is the elementary charge. Integrating Equation 2.3 with a specific boundary condition gives an expression for electric field E which develops linearly inside the SCR.

2.3 Depletion voltage and leakage current

The pn-junction is reverse biased for sensor operations. A pn-junction is said to be reverse biased, when the positive terminal of the external power supply is connected to the n-side

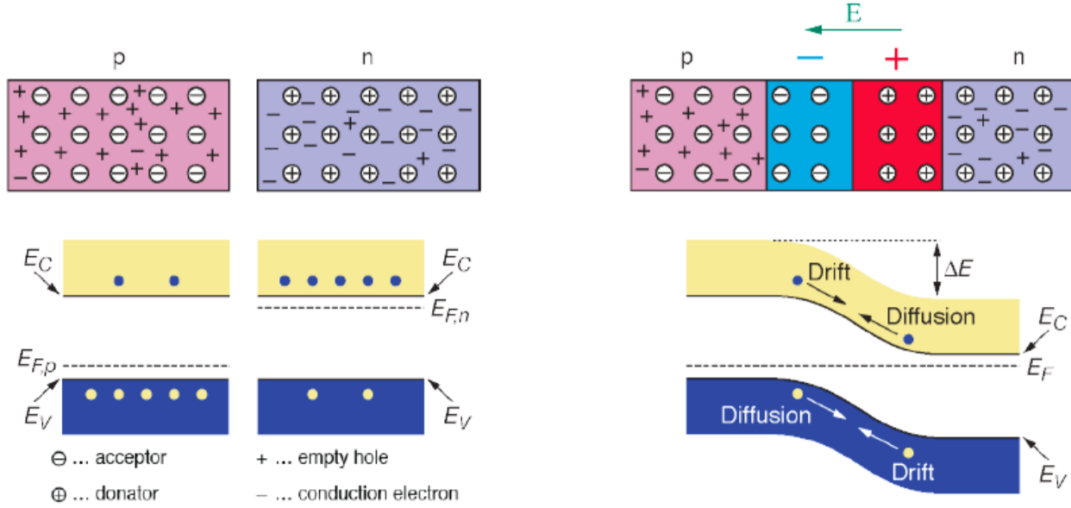


Figure 2.2: Schematic representation of p-n junction formation under conditions of thermal equilibrium and no applied bias voltage. Left: Separate n and p-type semiconductors with their respective energy bands. Right: The p-n junction with the depletion region around the junction denoted in blue and red colours [24].

while the negative terminal is connected to the p-side. When a pn-junction device is reverse biased the applied electric field increases the built-in potential barrier. Therefore the majority carriers are forced further away from the junction. Under reverse bias conditions, the depletion zone widens and the electric field increases. Thus the drift current becomes larger than the diffusion component. The reverse bias current is carried by some minority carriers produced due to thermal excitation. The density of the minority carriers is therefore temperature dependent. The bias voltage at which the sensor becomes fully depleted of its free charge carriers is called the depletion voltage V_{depl} .

The V_{depl} is directly proportional to the bulk resistivity and the squared thickness d of the sensor as given by the following equation:

$$V_{\text{depl}} = \frac{|N_{\text{eff}}|d^2}{2\epsilon_{\text{Si}}\epsilon_0} \quad (2.4)$$

If the applied bias voltage is more than the V_{depl} , the sensor becomes over-depleted, with a higher electric field across its bulk.

The leakage current is a very important parameter as it directly influences noise and power consumption of a detector and is composed of bulk generation current and the surface generation current. Surface generation current arises due to defects in the Si – SiO₂ interface introduced by ionising radiation, i.e. photons or charged particles and is usually negligible, after irradiation. On the other hand, bulk generation current arises from e-h pair generation caused by defects in the silicon bulk. The width of the depleted area depends on the applied voltage. The resulting leakage current therefore also scales with the applied

bias voltage. As this current is dominated by thermally generated e-h pairs, it is strongly temperature dependent.

The expected leakage current I_{leak} for a given T can which can be approximated for both non-irradiated and irradiated sensors by the following formula:

$$I_{\text{leak}}(T) \propto T^2 \exp\left(\frac{-E_g}{2k_B T}\right) \quad (2.5)$$

where k_B is the Boltzmann constant.

The leakage current approximately doubles every 7 K and can lead to thermal runaway especially in case of irradiated sensors, due to self-heating effects. This can be avoided by operating the sensors at very low temperatures. As such, the Si detectors to be used at the HL-LHC will be operated around -20°C to avoid the thermal runaway, power consumption and noise.

An important parameter of silicon sensors is the breakdown voltage. Carriers that gain high energies while traveling through high field regions can undergo scattering events with bonded electrons in the valence band. The excess energy is transferred to this electron which is lifted into the conduction band creating a new electron-hole pair. This secondary electron-hole pair can also have a rather high energy. In this case the avalanche effect is triggered and the carrier density increases heavily. This is known as impact ionisation [23]. An avalanche breakdown occurs as a result of an exponential increase in current and will lead to an electrical breakdown at the junction which is the region of maximum electric field. The voltage at which the electrical breakdown occurs is called the breakdown voltage, V_{bd} . Therefore the V_{bd} defines the operational bias limit of a sensor.

2.4 Charge generation and collection

Moderately relativistic charged particles, other than electrons, lose energy in matter primarily by ionisation and atomic excitation. The mean rate of energy loss, also known as the stopping power of the traversing charged particle, is described by the Bethe-Bloch process from Ref. [26] as illustrated in Figure 2.3 and represented by the following equation:

$$-\frac{dE}{dz} = K z^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{\text{max}}}{I^2} - \beta^2 - \frac{\delta}{2} \right] \quad (2.6)$$

where,

1. $\frac{dE}{dz}$ is the mean energy loss of the traversing particle per unit traversed distance of the detector in units of MeV cm^2 ,

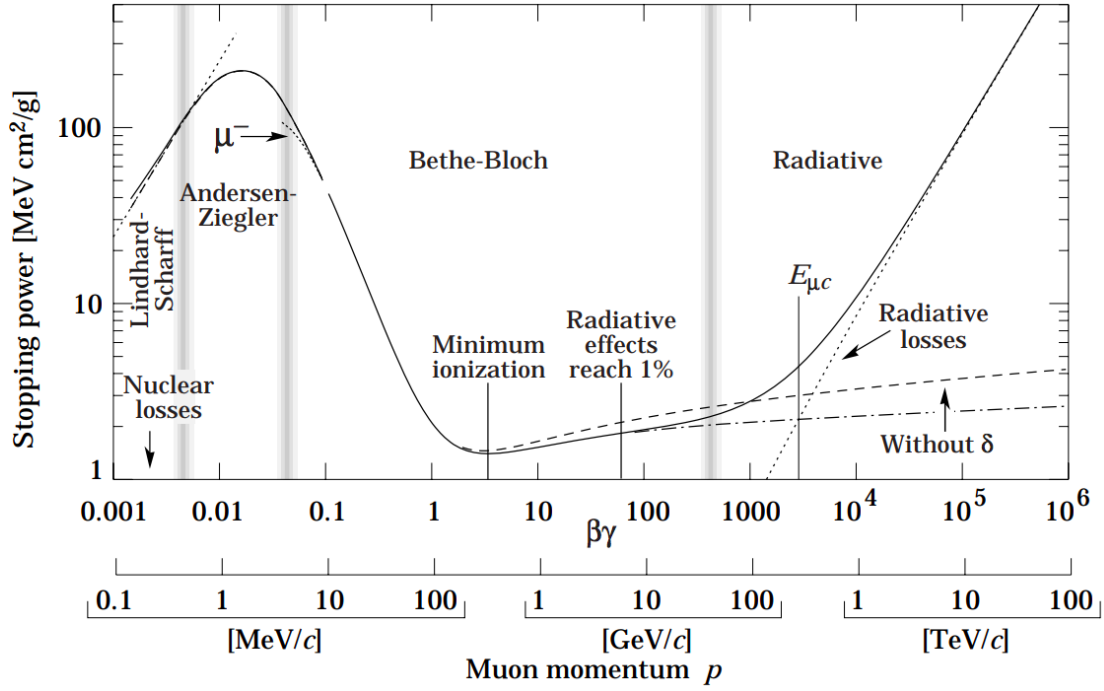


Figure 2.3: Stopping power ($-\frac{dE}{dx}$) for positive muons in copper as a function of momentum ($p = M\beta c\gamma$). Solid curves indicate the total stopping power. This image has been taken from [25].

2. K is a constant
3. z is the charge of the traversing particles in units of e
4. Z is the atomic number of the absorption medium which is 14 for silicon
5. A is the atomic mass of the absorption medium which is 28 for silicon
6. m_e is the electron rest mass
7. c is the speed of light
8. β is the ratio of the velocity of the traversing particle in units of c
9. I is the mean excitation potential in eV
10. $T_{\max}$ is the maximum kinetic energy and
11. $\gamma = 1/\sqrt{1 - \beta^2}$ is the Lorentz factor

In practical cases, most relativistic particles have mean energy loss rates close to the minimum, and are said to be Minimally Ionising Particle, or MIPs. When a MIP passes through the Silicon lattice with almost the speed of light, it liberates valence electrons. These electrons get ionised into higher energy states and reach thermal equilibrium by entering the conduction band as free electrons due to collisions.

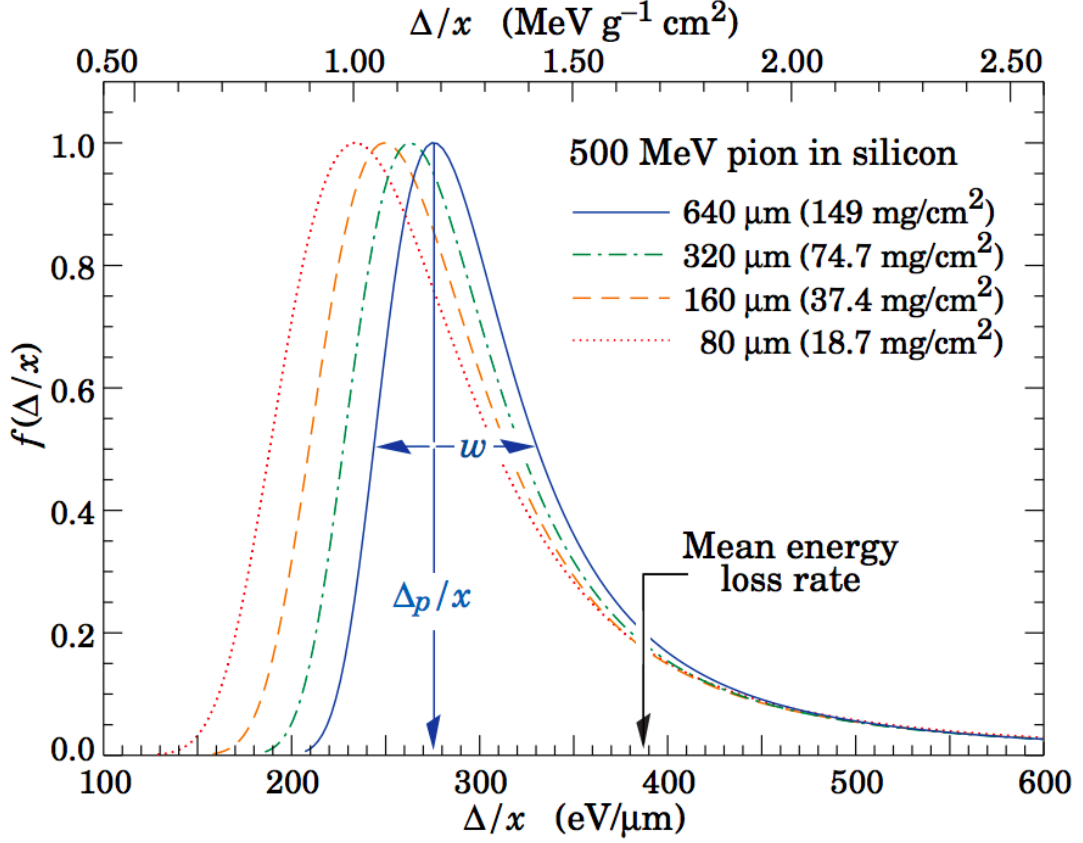


Figure 2.4: The most probable energy loss in silicon for 500 MeV pions, normalised to unity at the most probable value Δ_p/x . The width w is the full width at half maximum. This image has been taken from [28].

Sometimes, the MIP releases a core electron that is more tightly bound and possesses more kinetic energy. This leads to secondary ionisation of the Silicon. Thus energy deposited by these core electrons also known as delta electrons are significantly higher than that of the valence electrons. The energy spectrum of these rare high energy events generate an asymmetric distribution. These events are therefore described using gaussian corrections over a Landau curve also known as Landau-Vavilov distribution from Ref. [27] as shown in Figure 2.4.

The number of e-h pairs produced in the depleted zone is calculated by dividing the energy deposited by the MIP by the ionisation energy required to generate an e-h pair in Si at a temperature of 300 K [29]. For Si, the ionisation energy is thrice the band gap energy 1.12 eV i.e. 3.36 eV. The number of e-h pairs corresponds to the most probable value of the deposited charge per μm . For sensors of thicknesses 100 μm and 150 μm , an incident MIP creates around 70 – 80 electrons per μm .

Under the influence of an external electric field induced by the applied bias voltage, the

signal inside the Si bulk is composed of the electrons and holes drifting to their respective electrodes. This induced charge can be calculated using the Shockley-Ramo theorem from Ref. [30] as described in Equation 2.7.

$$I = e\vec{v} \cdot \vec{E}_W \quad (2.7)$$

where $\vec{E}_W$ is the the weighting field which is defined as the negative gradient of the weighting potential ϕ_W . The potential is calculated solving the Laplace equation $\Delta^2\phi_W = 0$ with the condition that the voltage applied to the collecting electrode is 1 and 0 for all the other electrodes. The signal obtained from the total integrated current over the charge collection time corresponds to the total collected charge.

While drifting to their respective electrodes, some loss of charge can occur such that the collected charge is reduced. The ratio between collected charge Q and deposited charge Q_0 is known as the Charge Collection Efficiency (CCE):

$$CCE = \frac{Q}{Q_0} \quad (2.8)$$

2.5 Effects of radiation damage

Silicon detectors are severely affected by the harsh radiation environments of high luminosity particle accelerators, like the LHC. Properties of the sensor such as leakage current, depletion voltage and charge collection efficiency are affected by radiation. The leakage current is mainly affected by the bulk damage, caused by Non-Ionising Energy Loss (NIEL) processes leading to lattice defects. In this case one or more of the Si atoms get displaced and changes the effective doping concentration and therefore alters the electrical properties of the crystal. Moreover, the vacancies left by the displaced electrons leads to charge trapping. The NIEL hypothesis scales the radiation damage in silicon bulk of particles of different types and energies assuming that the damage caused by displacement of the lattice atoms is linearly proportional to the energy transferred in these displacements [12].

Radiation damage in high energy physics is measured in units of 'neutron equivalent fluence' that is calculated using the following formula:

$$\phi_{eq} = \kappa\phi_{irr} = \kappa \int \phi(E)dE \quad (2.9)$$

where ϕ_{eq} is the equivalent irradiation fluence, ϕ_{irr} is the actual fluence received during irradiation and κ is the hardness factor which scales the damage caused by displacement integrated over the energy spectrum $\phi(E)$, to the equivalent one for 1 MeV neutrons. Different types of radiation defects cause various changes in the operational parameters such as:

- Depletion voltage: The V_{depl} is directly proportional to the effective doping concentration N_{eff} as shown in Equation 2.4. Current ATLAS pixel detectors employs n-type bulk material. The bulk damage results an increase of the acceptors and hence the N_{eff} with an impact on the V_{depl} . For p-type material there is no type inversion as for the n-type silicon and the V_{depl} always increases with fluence.
- Leakage current: The I_{leak} proportionally increases with the fluence as shown in Equation 2.10. This is generally caused by generation and Poole-Frenkel effect.

$$\Delta I_{\text{leak}} = \alpha \phi V \quad (2.10)$$

where α is the proportionality constant, V is the volume of the sensor and ΔI_{leak} is the difference between the leakage current before and after irradiation to a fluence ϕ .

- Charge Collection Efficiency: Electron and hole trapping is caused by localised energy states that capture the carriers ,for some time before being released. This leads to loss in charge collection efficiency.

Not all defects generated by NIEL are stationary and permanent. Some are mobile even at room temperature and interact with other defects in the silicon material. These interactions are in generally referred to as annealing. They can be classified into beneficial and reverse annealing as they result in a decrease or increase of the N_{eff} . The annealing effect on N_{eff} can be described as a function of the equivalent fluence ϕ_{eq} , for a time after irradiation t , and annealing temperature T using the following relation [31]:

$$\Delta N_{\text{eff}}(\phi_{\text{eq}}, T, t) = N_A(\phi_{\text{eq}}, T, t) + N_\gamma(\phi_{\text{eq}}, T, t) + N_C(\phi_{\text{eq}}) \quad (2.11)$$

where N_A denotes the short term annealing also known as beneficial annealing, N_γ denotes the long time annealing also known as reverse annealing and N_C denotes the damage constant that is proportional to the fluence and the annealing time. In case of n^+ -in-p sensors, beneficial annealing reduces the number of acceptors due to irradiation. This type of annealing takes approximately 7 – 10 days at room temperature. On the other side, reverse annealing occurs over a longer time period of several weeks. If the irradiated sensors are not kept in sufficiently cold temperatures, the number of acceptors increase. This increases the N_{eff} and consequently the V_{depl} also increases.

3 The ATLAS pixel sensors

3.1 Pixel sensor concepts

Pixel sensors provide an explicit two dimensional information of the particle impact point. The implants of these sensors can be produced with either heavily doped n^+ or p^+ in a lightly doped silicon bulk material of either n or p type. As such the following four possibilities are available - p^+ -in-n p^+ -in-p n^+ -in-n and n^+ -in-p. The performance of p^+ -in-n and p^+ -in-p sensors are more affected by charge trapping after irradiation (see 2.5) as they collect holes which have a lower mobility than electrons in comparison to the performance of irradiated n^+ -in-n and n^+ -in-p sensors. Therefore the present silicon sensors used or planned for the LHC experiments are the sensors employing n^+ -in-n and n^+ -in-p concepts.

The two sensor concepts of interest are described as follows:

1. n^+ -in-n concept: In this kind of sensor the detector bulk is n-type with n^+ pixel implants. Prior to irradiation, the pn-junction is on the backside and the depletion starts from the homogenous p^+ backside and increases with increasing bias voltage. For the e-h pairs to reach the electrodes, sensors employing this concept need to be completely depleted. After type inversion with irradiation the depletion region extends from the n^+ electrodes enabling these type of sensors to operate at partial depletion. These sensors undergo double-side processing given the fact that the guard ring structure must be implemented on the backside, around the main junction, making it more expensive and complicated than the n^+ -in-p type.
2. n^+ -in-p concept: In this kind of sensor the detector bulk is p-type with n^+ strip implants. The depletion region grows from the implants to the backplane enabling the sensor to operate partially depleted. These sensors can be produced with a single-sided processing as the the guard ring structure can be implemented on the frontside.

In this thesis, all the sensors studied employ the n^+ -in-p concept.

3.2 Processing of pixel sensors

The processing of n^+ -in-p pixel sensors is shown schematically in Figure 3.1a. The steps performed are described as follows:

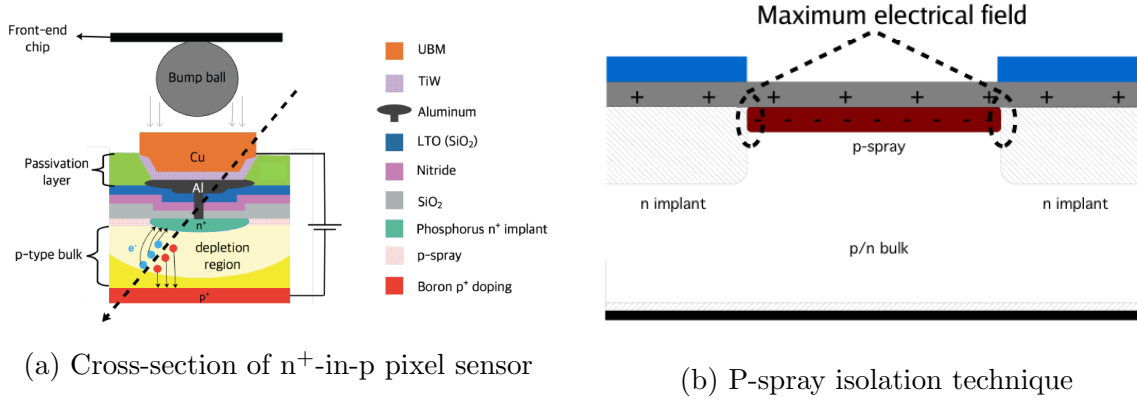


Figure 3.1: Schematic representation of (a) the cross-section of n⁺-in-p pixel sensor. This image has been taken from [20] and (b) p-spray isolation technique for adjacent n⁺ implants using a low dose of boron. This image has been taken from [32]. In both the images the dimensions are not to scale.

- Step I: The p-type silicon bulk is thermally oxidised at high temperature.
- Step II: Photolithography is used to partially etch the SiO₂ layer from thermal oxidation, to define the n⁺ segmentation.
- Step III: Doping is done by implanting phosphorous ions through the thin oxide layer to form the n⁺ implants. The doping concentration of the n⁺ implant depends on the intensity of ion exposure and its energy. Boron ions are implanted on the backside to form a p⁺ layer.
- Step IV: Annealing of the ions of the n⁺ implants is required for electrical activation.
- Step V: An additional isolation (p-spray) is added at the surface in between the n⁺ implants as shown in Figure 3.1b. This is necessary as the trapped positive charge in the SiO₂ layer attracts electrons, that could short the n⁺ electrodes.
- Step VI: Silicon Nitride and Low Temperature Oxide (LTO) are deposited through dedicated openings on top of these structures. Afterwards biasing structures are created in these layers to allow for a contact between n⁺ implant and metal layer.
- Step VII: The metal layer is made of aluminium. The Aluminium layer is sputtered on top of the wafer and then patterned in correspondence with the pixel implants and guard ring structures with an additional lithographic process.
- Step VIII: A passivation layer (BCB) is added over the full sensor-surface for high voltage stability and to protect it from the environment, such as dust and humidity. This layer is opened on top of the aluminium layer to establish electrical contact to the copper pad of the Under Bump Metallisation (UBM) which serves as landing pad for the bump ball on the chip side.

For two special wafers (6 and 7) of the SOI4 production studied in this thesis, the layer of a Titanium-Tungsten layer (TiW) that is routinely used as barrier layer to protect the

silicon from the copper atoms of the UBM, was patterned to serve as temporary layer to measure the IV characteristics of the sensors without biasing structures.

3.3 Pixel sensor structures

Two main structures of pixel sensors that have undergone re-design and optimisation are guard rings and biasing structures.

Guard rings

The edge of the sensor becomes conductive due to the damage caused by the mechanical cutting procedure. When the depleted region stretches up to the cutting edge, the high electric field leads to an instantaneous increase of the leakage current which could cause a breakdown. To protect the sensor-edges, guard rings are implemented around the active area on the sensor-surface. This ensures a smooth drop of the slope of the potential from the pn-junction to the cutting edge. The breakdown characteristics of a sensor is influenced by the number and structure of the guard rings. In n^+ -in-n sensors the guard rings are implemented on the backside and the entire edge is therefore kept at ground potential. While in the case of n^+ -in-p sensors, the guard rings are implemented on the frontside and therefore the edge is at the backside potential. Therefore n^+ -in-p sensors are affected by the risk of sparks between the sensor edge and read-out chip which would destroy the detector. This risk can be avoided by implementing additional insulation layers between the sensor and the read-out chip.

Biasing structures

Biasing structures are implemented which allow to measure the electrical properties of the sensor prior to interconnection. This structure is composed of a metal bias rail starting from the bias ring (BR) which is the innermost guard ring and a implant dot (known as bias/punch-through dot) to which it is connected. In general cases, the nearest pixel cells are at a potential induced by the ground potential of the bias dot as the implant follows the potential of the grounded one. This effect is known as punch-through. The punch-through mechanism allows the characterisation of the full sensor before interconnection. The bias dot can be of two types described as follows:

1. Standard bias dot: This type of structure is implemented inside an opening of the pixel implant as shown in Figure 3.2a. The standard bias dot employs the punch-through mechanism to apply ground potential to only one pixel implant.
2. Common bias dot: This type of structure is implemented externally to the pixel implant at the corner of four neighbouring pixel cells as shown in Figures 3.2b and 3.2c.

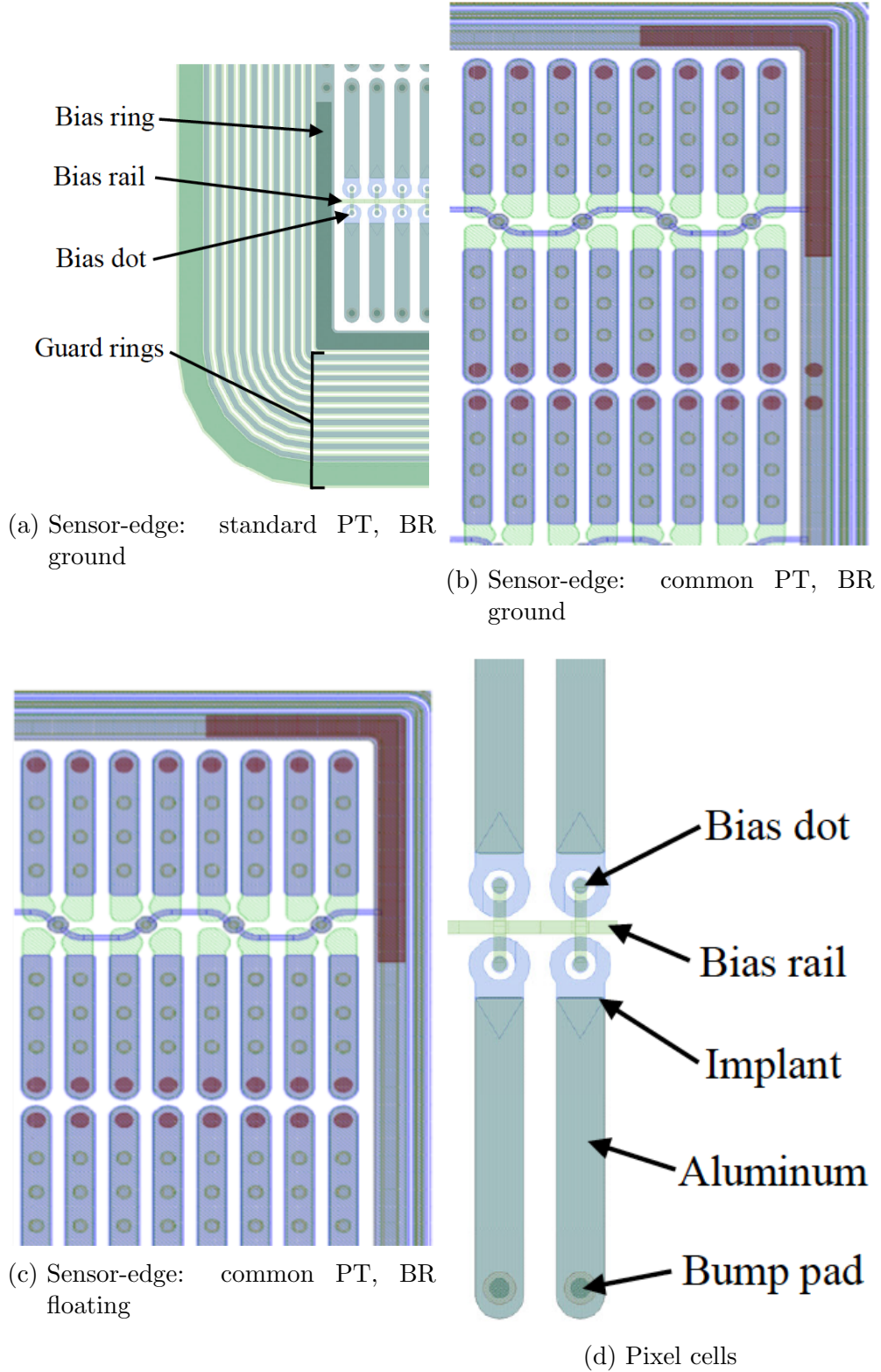


Figure 3.2: Schematic representation of the edge of: (a) a sensor with standard punch-through and grounded bias ring. This image has been taken from [12]. (b) a sensor with common punch-through and grounded bias ring. This image has been taken from [20]. (c) a sensor with common punch-through and floating bias ring. This image has been taken from [20]. (d) The structure of the pixel cells presently implemented in the ATLAS pixel detector. This image has been taken from [12].

To investigate the effectiveness of the biasing structures, three designs are investigated:

- grounded BR: the bias ring is grounded by the read-out chips through the UBM that are on top of the ring, such that the BR is also at ground potential,
- floating BR: the bias ring does not have UBM pads to be connected to bump balls and is grounded using the needle of the probe station while taking IV measurements and
- split BR: the aluminium contact in the BR is separated into two parts such that the implant is grounded by the chips through the ad-hoc bumps while the section where the biasing metal lines are connected is a metal line floating over the ring implant, without a direct contact. This section of the metal ring can be grounded with a needle during IV characterisation but it is floating after flip-chipping to the read-out chip.

3.4 Sensor production at the Max-Planck-Society Halbleiter Labor

The ATLAS Inner Detector group at the MPP designed new n^+ -in-p pixel sensor prototypes as a baseline for the new ITk system. The new designs are based on the previously achieved results (see [33–35]). An overview of the sensor designs relevant for this thesis is presented in Table 3.1.

The Semiconductor Laboratory of the Max-Planck-Society (MPG HLL) has produced several productions of 6-inch wafers of standard p-type Float Zone (FZ) silicon. The sensors studied in this thesis are from Silicon on Insulator (SOI) wafer production, in which a handle wafer is attached to the active pixel wafer, serving as a mechanical support to ensure the rigidity of the structure for the subsequent processing steps described in 3.2. At the end of the front-side processing, the handle wafer is etched away using an additional carrier wafer attached to the front side to give mechanical stability during this process. The second carrier wafer is also implemented for deposition of the aluminium layer on the backside of the active wafer. The sensors embedded in their wafers are then diced and the diced sensors are used in modules after interconnection to the read-out chips. The SOI4 production was completed in 2017 and it includes several single chip sensors compatible with the new read-out chip with a reduced pixel cell size of $50 \times 50 \mu\text{m}^2$ developed by the RD53 Collaboration to address the issue of high track density foreseen during the HL-LHC. The sensors designed to be compatible with the RD53 read-out chip are implemented with pixel cell sizes of $25 \times 100 \mu\text{m}^2$ and $50 \times 50 \mu\text{m}^2$. There are 8 wafers of this production which are of either $100 \mu\text{m}$ or $150 \mu\text{m}$ thickness. The sensors have either a standard edge region $d_e = 450 \mu\text{m}$ which is structured to have ten guard rings and one bias ring or a smaller edge region $d_e = 250 \mu\text{m}$ which is structured to have seven guard rings and one

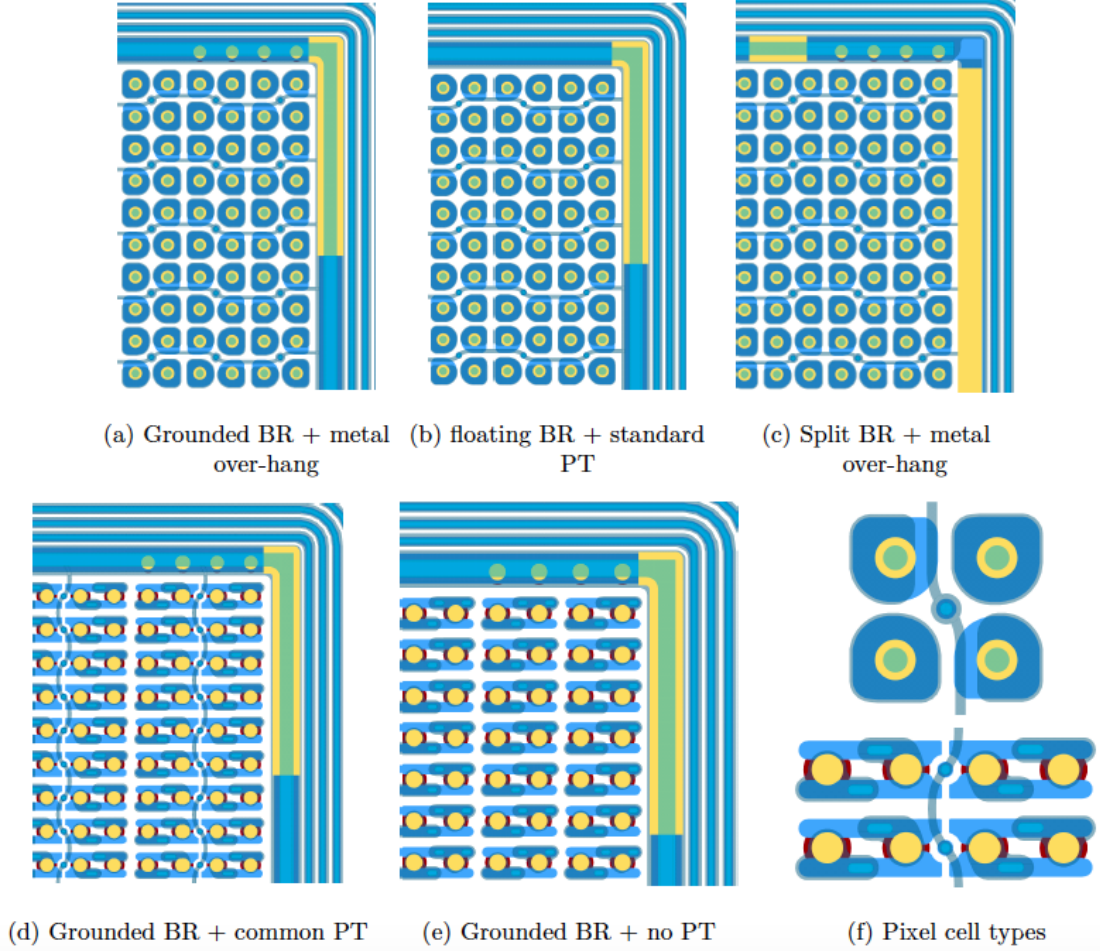


Figure 3.3: Schematic representation of sensor structures of the SOI4 production for sensors with $25 \times 100 \mu\text{m}^2$ and $50 \times 50 \mu\text{m}^2$ pixel cells and (a) with grounded bias ring implementing punch-through dots and metal over-hang, (b) floating bias ring and standard punch-through, (c) split bias ring and common punch-through with a metal over-hang, (d) grounded BR with common punch-through and (e) grounded BR with no punch-through. (f) Shows the two types of pixel cells. This image has been taken from [20].

bias ring. One of the three different biasing structures - grounded, floating or split is implemented in each of the sensors embedded in wafers of the SOI4 production. Except for wafer 8, which has a lower p-spray dose of 1.0×10^{12} Boron ions per cm^2 , the other wafers have a p-spray dose of 1.4×10^{12} Boron ions per cm^2 . Also, two wafers 6 and 7 of $150 \mu\text{m}$ thickness were processed with a special photolithographic step. The applied barrier layer composed of titanium-tungsten (TiW) prevents the atoms of the copper contained in the UBM to diffuse into the silicon. This layer has undergone an additional lithographic step with respect to the standard processing, where it was patterned to cover the full area contained within the bias ring. In this way all the pixels of one sensors were shorted, through the contacts in the passivation layer, thus allowing for the measurement of the IV characteristic. Afterwards the TiW has been etched from the surface, leaving it only below the UBM pad, as in the standard processing.

Figure 3.3 shows schematically the sensor designs of this production. In (a) a sensor with $50 \times 50 \mu\text{m}^2$ pixel cells, grounded BR, common punch-through dot and metal over-hang structure over the dot implant, is shown. The bias ring is kept at ground potential by the chip thanks to the presence of the UBM pads to which the bumps on the chip side can electrically connect. Therefore after the flip-chipping, also the bias grid will be directly at ground potential. The size of the metal over-hang is larger than that of the bias dot implant over which is placed, thus improving the breakdown characteristics due to the fact that the high electric field region shifts to the SiO_2 layer. In (b) a sensor with $50 \times 50 \mu\text{m}^2$ pixel cells, floating BR and standard punch-through dot is shown. The floating BR reduces the effect of punch-through on the hit efficiency after irradiation. A consequence of the floating BR is that it allows the leakage current from the edges of the sensor to directly flow into the edge columns. This bears the risk of increasing the noise level of the edge pixels. The drawback of the floating BR can be overcome by the split BR design shown in (c). The metal over-hang design and split BR has only been used for some sensors with $50 \times 50 \mu\text{m}^2$ pixel cells in this production. In (d) a sensor with $25 \times 100 \mu\text{m}^2$ pixel cells, grounded BR and common punch-through dot is shown. In (e) a sensor with the same size of pixel cells and grounded BR, but without biasing structure is shown. And finally in (f) the two different pixel cells are shown with the $50 \times 50 \mu\text{m}^2$ pixel cells positioned on top of the $25 \times 100 \mu\text{m}^2$ geometry.

In the initial measurements to investigate the band gap energy of irradiated sensors, only one sensor of the CiS wafer production was used. Details of this production can be found in Ref. [21].

3.5 The RD53A ATLAS read-out chip

The main purpose of the RD53 collaboration is to design the next generation of hybrid pixel read-out chips for the ATLAS and CMS Phase II upgrade of the pixel detectors. The integrated circuit of the RD53A demonstrates in a large format IC the suitability of the chosen 65 nm CMOS^1 technology (including radiation tolerance), the stable low threshold operation, and the high hit and trigger rate capabilities, required for HL-LHC upgrades

¹Complementary Metal–Oxide–Semiconductor

Table 3.1: The types of SOI4 sensors studied in this thesis.

Sensor type	Pixel cell [μm^2]	Biasing structure	Edge distance [μm]	Biasing structure
14gn	25×100	no	450	grounded
14gp	25×100	yes	450	grounded
14fp	25×100	yes	450	floating
52sp	50×50	yes	250	split
54gp	50×50	yes	450	grounded
54fp	50×50	yes	450	floating
54sp	50×50	yes	450	split
54gn	50×50	no	450	grounded
24gn	50×250	no	450	grounded
24gp	50×250	yes	450	grounded
24fp	50×250	yes	450	floating

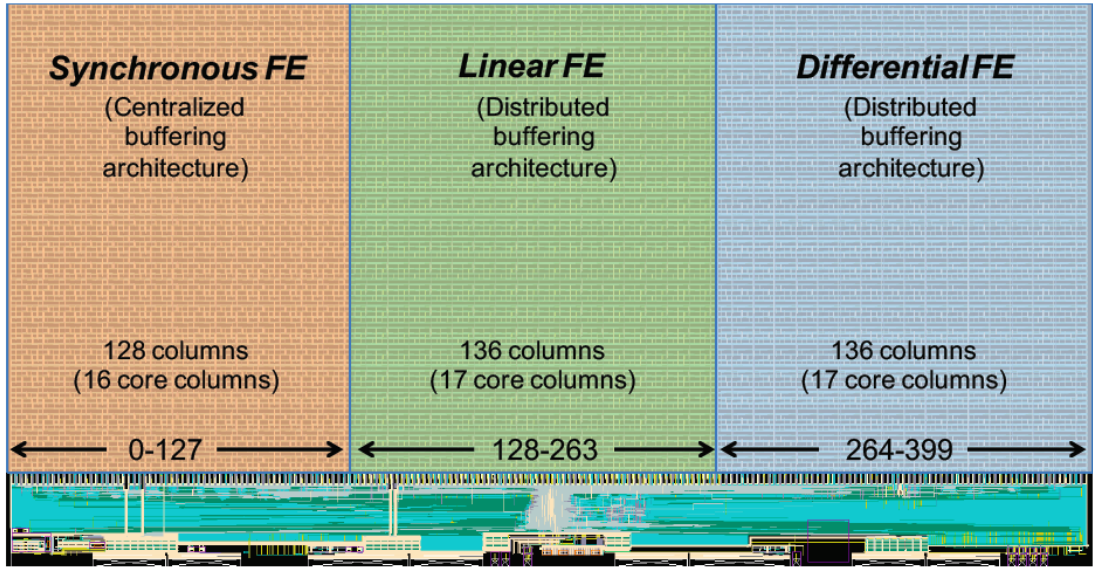


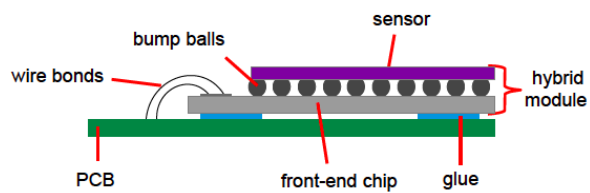
Figure 3.4: Schematic representation of the three different analogue circuitry implemented in RD53A front-end - Synchronous, Linear and Differential. The range of pixel columns of each flavour is shown along the bottom. This image has been taken from [36].

of ATLAS and CMS. This read-out chip is a prototype for the experiments and therefore contains front-end variations for testing purposes and detailed performance comparisons. The chip itself consists of two main parts: the active area of a matrix made of 76800 pixels with a pixel size of $50 \times 50 \mu\text{m}^2$ and the chip periphery, located at the bottom of the chip. The three different analogue circuitry in a RD53A Front-End (FE) are known as: Synchronous FE, Linear FE and Differential FE as shown in Figure 3.4. The layout area for a 4-pixel analog island, the bump bond pads, the calibration injection circuit, used to test the FEs via the injection of a defined amount of charge in pixels based on the configuration, and the organisation of the bias distribution is the same for the three FEs. The distinguishing features of each of the three FEs are as follows:

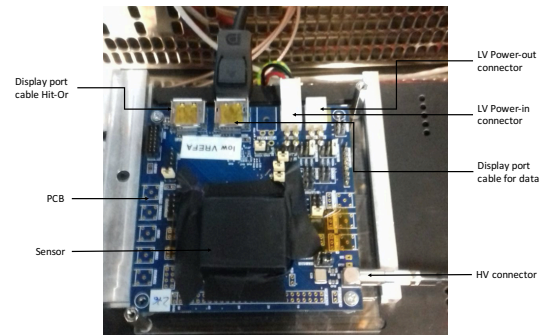
- **Synchronous FE:** Consists of a synchronous discriminator made of a differential amplifier and a positive feedback latch that can be converted to a local oscillator (till 800 MHz) implementing an asynchronous logic feedback loop which aids in performing a fast Time-over Threshold (ToT) counting. The SFE also uses a unique method of an auto-zeroing scheme that requires periodic acquisition of a baseline for tuning the threshold .
- **Linear FE:** Consists of a complete analogue circuit employing a linear pulse amplification in front of the discriminator that compares the pulse to the set threshold voltage of the discriminator. The LFE uses a pixel-by-pixel threshold trimming with local threshold adjustments using 4-bit resistor ladders.
- **Differential FE:** Also consists of a complete analogue circuit employing a differential gain stage in front of the discriminator and implements a threshold by unbalancing the two branches. The DFE uses a pixel-by-pixel threshold trimming with local threshold adjustments using 4-bit binary weighted Digital-to-Analogue-Converters (DAC).

3.6 Hybrid pixel detectors

The sensor and the chip are produced separately. The combination of a sensor bump bonded to the read-out chip, front-to-front, in a process known as flip-chipping is called the hybrid module. The module is then connected to a polyimide Printed Circuit Board (PCB) via wire-bonding as schematically shown in Figure 3.5a. The combination of the module wire-bonded to the PCB is called a dressed module. The PCBs used in the measurements for this thesis are compatible with the RD53A readout system implementing DisplayPort sockets for transferring data and for the Hit-Or, low voltage connectors and a high voltage power supply connector as shown in Figure 3.5b.



(a) Cross-section of a module wire bonded to a PCB



(b) Module

Figure 3.5: (a) Schematic representation of a cross-section of a hybrid wire bonded to a PCB. Dimensions are not to scale. This image has been taken from [20]. (b) A RD53A module with certain dedicated structures indicated.

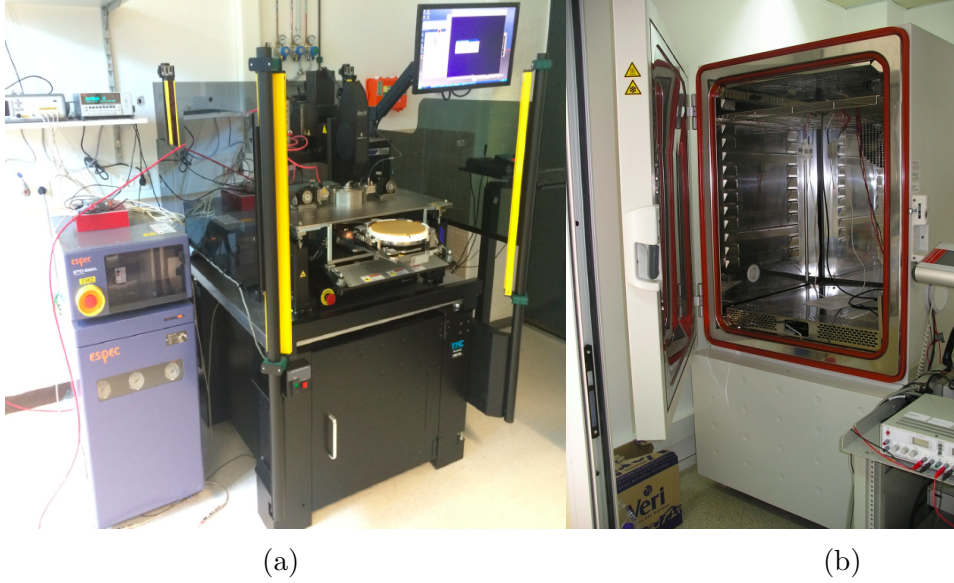


Figure 4.1: Photographs of the MPP ATLAS laboratory equipment, where (a) shows the probe station for sensor characterisation and (b) the climate chamber for module characterisation.

4 Experimental set-up

This chapter describes the laboratory set-up used to characterise the sensors and the data acquisition system employed to tune and perform measurements on the investigated modules.

4.1 Sensor characterisation

4.1.1 Measurement of leakage current as a function of bias voltage

The first test of the functionality of a pixel sensor is measuring its leakage current as a function of the applied bias voltage (IV measurements) to determine the breakdown voltage and leakage current. The IV measurements are done for sensors at wafer level, diced level, module level and before and after irradiation. At wafer and diced levels, it is done directly using the biasing structures of the sensors and after flip-chipping at module level using the readout chip. The breakdown voltages observed from the IV curves of sensors of different structures and wafer productions are used to select the best candidates for interconnection.

A high breakdown voltage and low leakage current with the breakdown voltage at least higher than the depletion voltage is expected for an ideal sensor.

For IV characterisation at wafer and diced levels, measurements are done using a probe station by Cascade Microtech shown in Figure 4.1a which is a semi-automatic measuring device with a thermal chuck that is able to apply high voltage (HV) up to 3000 V. This thermal chuck is used to apply the high bias voltage and to regulate the temperature with the help of a chiller of ESPEC company that can set the required temperatures down to -65°C . This is especially necessary while measuring the IV characteristics of irradiated sensors. The chuck is also equipped with a vacuum system to ensure proper positioning and mechanical stability of the wafer and diced sensors. A flow of nitrogen is used to prevent the formation of ice crystals on the sensors while conducting measurements at temperatures below 0°C . The HV is applied to the sensor backside via the thermal chuck, while the bias ring on the frontside of the sensor is kept at ground potential by contacting it with a needle through dedicated openings in the passivation layer. In case of sensors without biasing structures investigated in this thesis, the IV characterisation at wafer level is normally not possible, unless it implements a temporary TiW layer as described in 3.2. Unirradiated sensors are measured at a temperature of $+20^{\circ}\text{C}$, while the IV characteristics of irradiated sensors are tested in a range between -45°C and -20°C .

For IV characterisation at module level, the measurements are done using the voltage connection of the PCB and the modules are kept at stable temperature inside a Vötsch climate chamber (Model VT7011) as shown in Figure 4.1b. These measurements are done to recheck the quality after flip-chipping the sensors and then wire bonding them to their respective PCBs. All the modules investigated for this thesis are unirradiated. Therefore the temperature inside the climate chamber is maintained at 20°C .

The high bias voltage is supplied by either a high resolution picoamperemeter Keithley of Tectronix company (Model 6517) with ± 1000 V DC voltage source or a ISEG of SHQ series with switchable polarity. The ISEG can supply HV up to 3000 V and higher power than the Keithley, therefore it is used for the characterisation of the irradiated sensors. The ISEG is therefore mostly used for IV characterisation of irradiated sensors. For both these devices, the voltage ramp is programmable. At each voltage step, ten subsequent measurements are executed and the resulting mean and standard deviation of the corresponding leakage currents are calculated.

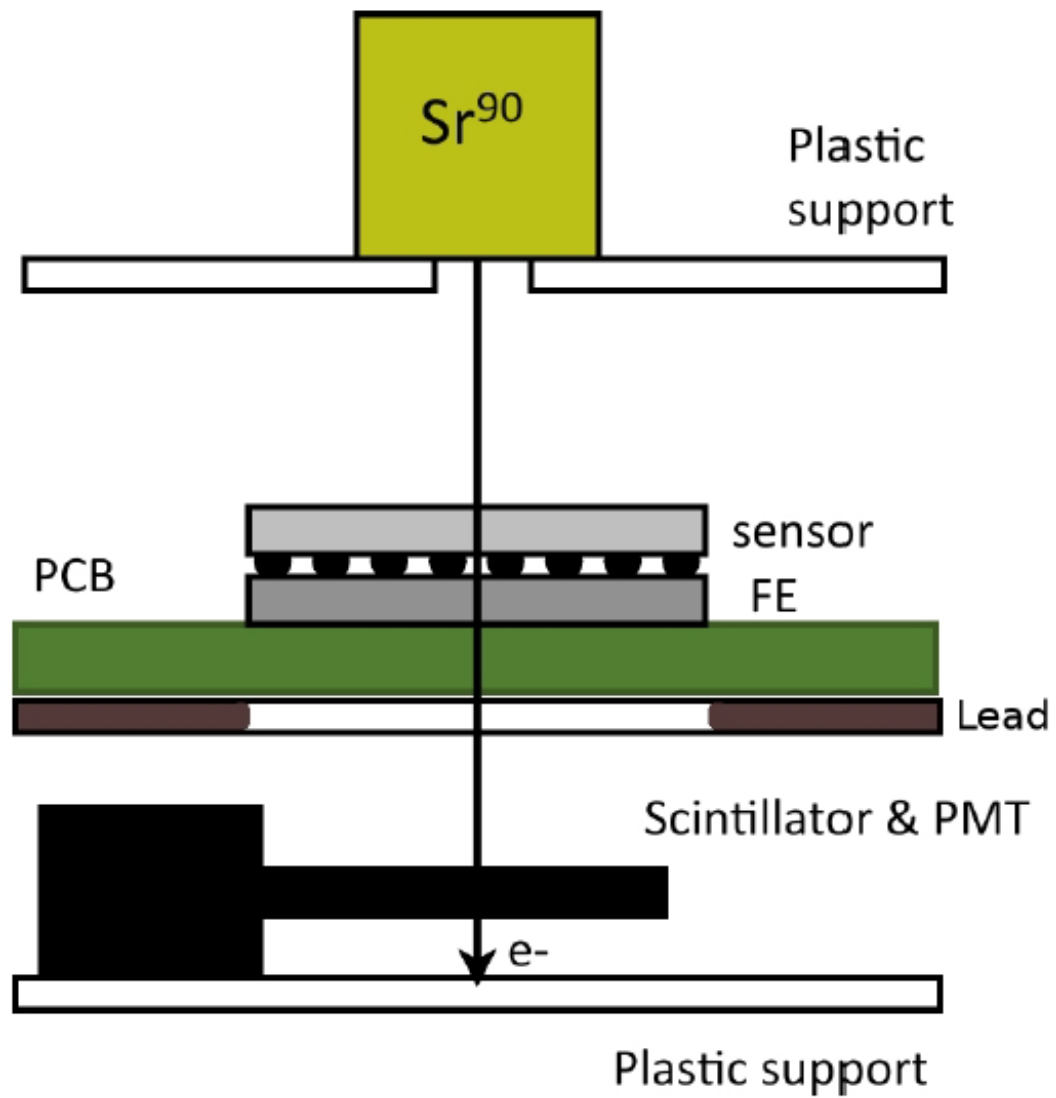


Figure 4.2: A schematic representation of the experimental set-up inside the climate chamber for charge collection measurements. This image has been taken from [12].

4.1.2 Measurement using radioactive sources

An important test of the functionality of a pixel sensor is measuring its charge collection properties, after it has been flip-chipped to a read-out chip. The characterisation of charge collection is performed using the β -electrons emitted from an ^{90}Sr source using the set up as shown in Figure 4.2. The decay chain of ^{90}Sr consists of two β emissions to Yttrium and Zirconium with a characteristic continuous three-body spectrum [12, 37]:

$$\begin{aligned} ^{90}\text{Sr} &\rightarrow e^- + \bar{\nu}_e + ^{90}\text{Yt} \text{ with half-life } 28.8 \text{ y and } E_{max} = 0.546 \text{ MeV} \\ ^{90}\text{Yt} &\rightarrow e^- + \bar{\nu}_e + ^{90}\text{Zr} \text{ with half-life } 2.67 \text{ d and } E_{max} = 2.280 \text{ MeV} \end{aligned} \quad (4.1)$$

Measurements are carried out after tuning the front-end and masking the noisy pixels. The module to be investigated is then placed inside the climate chamber with the ^{90}Sr source placed on a plastic support positioned on top of the sensor and the scintillator directly underneath. The β electrons from the source traverse the entire thickness of the sensor to reach the scintillator to register these hits and enable external triggering.

Source scans using the BDAQ53 hardware and software as described in 4.2 are executed. The cluster ToT obtained from each source scan at a certain set bias voltage is fitted with a Landau function convoluted with a Gaussian function to describe the effect of electronic noise, and from this resulting function the most probable value of the ToT is extracted. This value and its corresponding bias voltage is displayed for each sensor to determine the the bias voltage at which the charge collection saturates. The charge deposited by a MIP in a sensor depends on its thickness as mentioned in 2.4.

Measurements performed with γ sources use the same set-up. However, instead of the external trigger, internal self-trigger of the read-out chip is enabled. This is because the low energy photons when interacting with silicon atoms, mainly through photoelectric effect release all their energy at once and do not reach the scintillator. The internal self-trigger registers signals above the set threshold and therefore is very sensitive to noise. So, tuning and masking noisy pixels after irradiation is very important to avoid accepting hits generated by noise which ultimately hinders the measurement.

All the modules tested were kept at a stable temperature of $+20^\circ\text{C}$ as none of them was irradiated. The whole set-up is shown schematically in Figure 4.3.

4.2 The BDAQ53 read-out system

The purpose of the BDAQ53 read-out system is to investigate modules with RD53A read-out chips in laboratory and testbeam set-ups. It is also used to tune the modules to reach a uniform response from the front-end chip used for all the pixel cells.

4.2.1 Hardware components

The BDAQ53 read-out board is custom designed and can be powered in either USB or VCC mode. However for the laboratory measurements the USB mode was implemented.

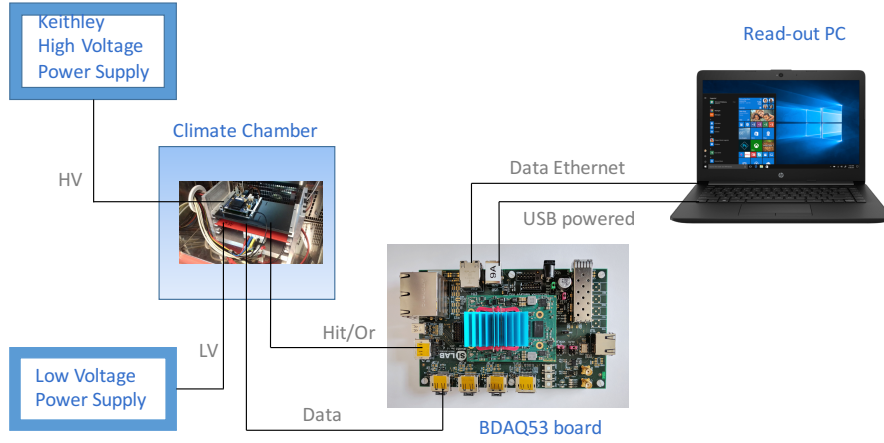


Figure 4.3: Schematic representation of the laboratory set-up for RD53A module characterisation.

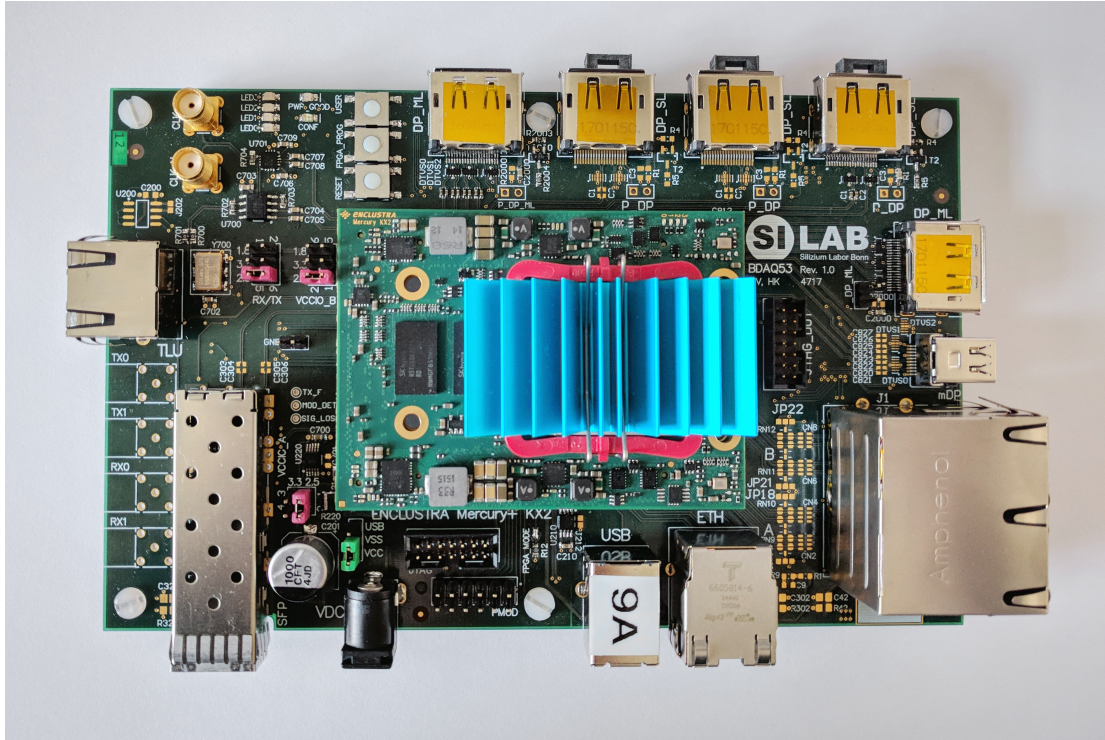


Figure 4.4: The BDAQ53 board with its FPGA module, DisplayPort sockets, ethernet and power supply connectors. This image has been taken from [38].

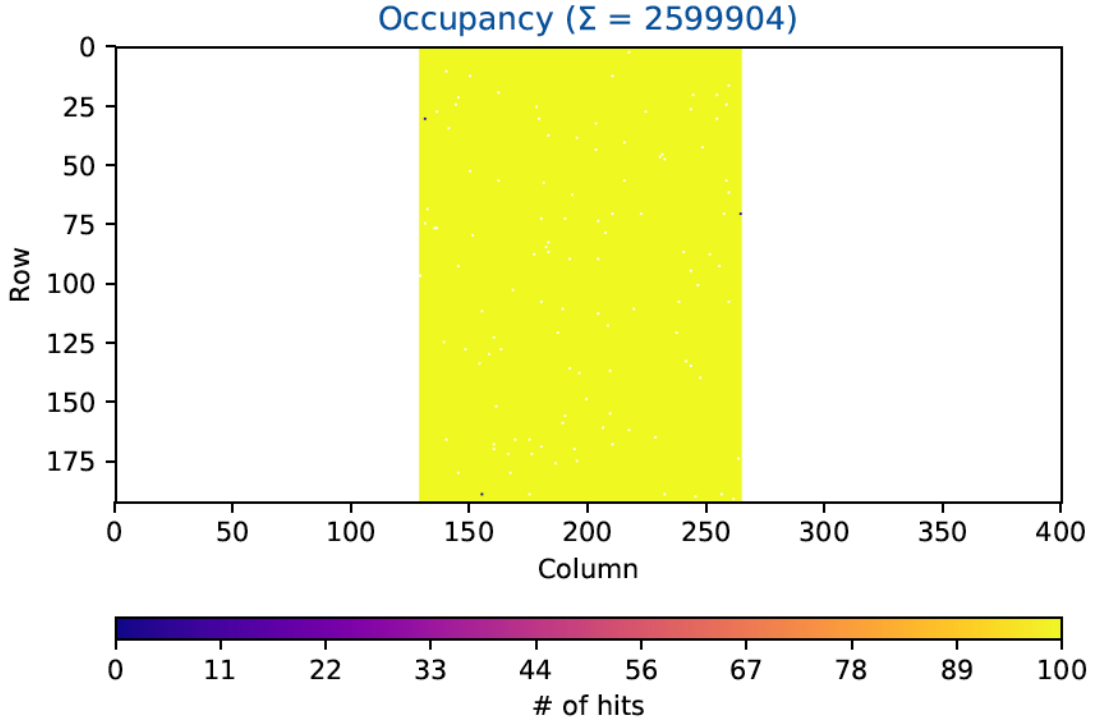


Figure 4.5: Analogue test results of an unirradiated module using the linear front-end (columns from 128 to 264) of the RD53A read-out chip. This is a good example of an analogue scan of a module with no noise. All the pixels see uniform number of hits.

The board has a Mercury+KX2 FPGA module configured according to the RD53A read-out chip requirements. For more information regarding the chip requirement of RD53A refer to Ref. [39]. It is designed to support four RD53A read-out chips using DisplayPort cables connecting the modules to the board to enable data taking. There is one additional DisplayPort connector that is used to receive detector response (Hit-Or signals) from the RD53A. The board has an ethernet connector to receive the triggers in the test-beam setup. Finally to communicate with the PC, an additional ethernet connection is used.

4.2.2 Read-out Software

The software steering of the readout system is written in Python and is easily adaptable. Each scan within BDAQ53 read-out software loads a chip configuration file in "yaml" format which contains settings for each of the three analogue front-ends of the chip, for example, the global threshold parameter and some chip-specific information, for example, the chip ID and the disabled pixels. To tune a specific front-end, the respective front-end columns are set in all the scans executed.

A digital scan "scan_digital.py" maybe executed where a digital signal is injected into each enabled pixel. At one time only a few pixels are injected via the injection circuitry with an

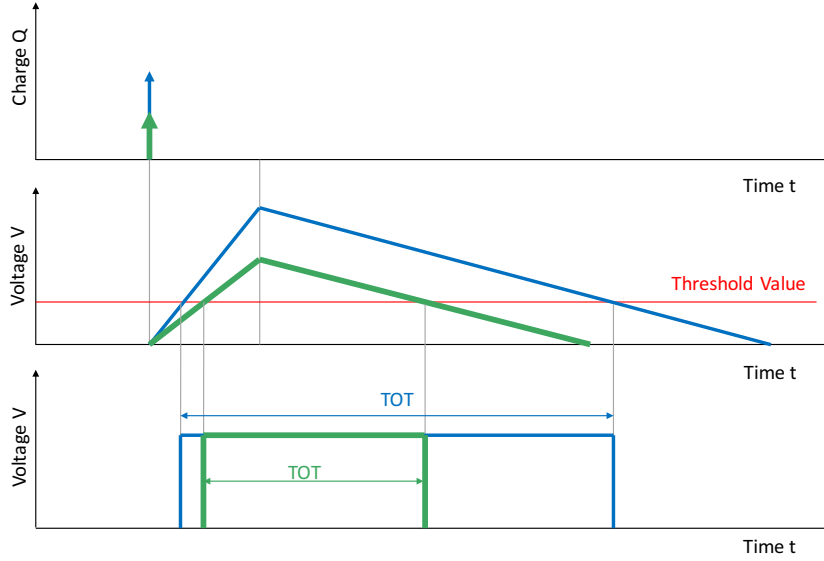


Figure 4.6: Schematic representation of relation between threshold and time over threshold (ToT). Two charge signals are registered - denoted by blue and green in the first graph. The next graph displays the corresponding voltage after being preamplified, the falling slope corresponding to the feedback current. The voltage that is above the threshold is registered as a signal. And in the final graph the inter-relation between ToT and threshold is displayed.

injection mask and then this mask is shifted until all enabled pixels have been injected to check the response of the front-end for each pixel cell. Next an analogue scan is executed in the same method to check the occupancy and pixel response using "scan_analog.py". In this scan, an analogue pulse is injected into each enabled pixel whose height is defined by the two differential DAC (Digital-to-Analogue-Converter) settings VCAL_MED and VCAL_HIGH. The VCAL_MED is always set to 500 DACs and if the VCAL_HIGH is set to 1700 DACs, the difference is 1200 DACs. Therefore the corresponding injected charge is 12ke (1200×10), to mimic the charge collection for 150 μm thickness (150×80 e-h pairs = 12ke). For sensors of 100 μm thickness (100×60 e-h pairs = 6ke), the VCAL_MED is as usual set to 500 DACs and VCAL_HIGH = 1100. The released charge by a MIP in Silicon is in the range of 60 – 80 e per distance depending on the sensor thickness. So VCAL_HIGH is set depending on the thickness of the sensor.

To equalise the pixel response, two parameters that need to be tuned: the threshold and the ToT. The threshold is determined by the discriminator after the amplification stage in the injection circuitry. Signals below this threshold value are not registered. The ToT depends on the feedback current of the circuit, which affects the fall time of the signal. As shown in Figure 4.6, ToT and threshold are interrelated and a change in one of these parameters affects the other.

A range of charge is injected via the injection circuitry to determine the threshold for each pixel. For each pixel, the charge is injected multiple times and the response of the pixel is recorded. If the collected charge crosses the threshold value set in the discriminator,

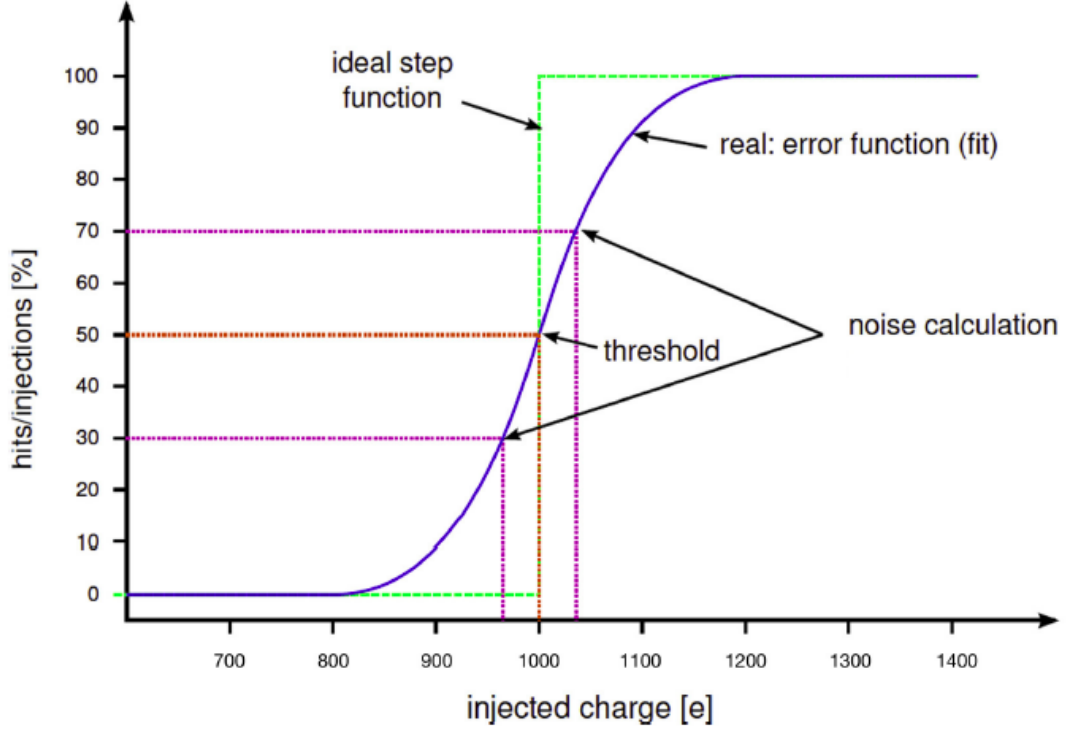


Figure 4.7: An example of a typical outcome of a threshold measurement of a single pixel cell known as the S-Curve. This image has been taken from [40].

a hit is registered. When the number of registered hits correspond to an occupancy of 50%, the equivalent amount of collected charge is defined to be the threshold value. In an ideal case, no hits would be recorded as soon as the signal is below the threshold, resulting into a step function. However, taking into consideration the noise contribution, the step function is convoluted with a gaussian distribution. Figure 4.7 represents a typical outcome of a threshold measurement of a single pixel cell also known as the S-curve. This S-curve describes the probability to detect a hit corresponding to a certain amount of charge Q and can be described by the following equation:

$$P(Q) = \frac{1}{2} \operatorname{erfc} \left(\frac{Q_{thr} - Q}{\sqrt{2}\sigma_{noise}} \right) \quad (4.2)$$

where Q_{thr} is the charge set as threshold value of the discriminator and σ_{noise} is the voltage fluctuation at the input of the discriminator and represents the electronic noise of the pixel cell. The $\operatorname{erfc}(x)$ function is the complementary error function and is calculated using the following equation:

$$\operatorname{erfc}(x) = 1 - \operatorname{erf}(x) = 1 - \frac{2}{\sqrt{\pi}} \int_{-x}^x e^{-t^2} dt \quad (4.3)$$

where $\operatorname{erf}(x)$ describes the probability of a random variable x with a mean value $x/2$ within the range of 0 and x .

The threshold scan "scan.threshold.py" is used to check what the threshold value is, or to

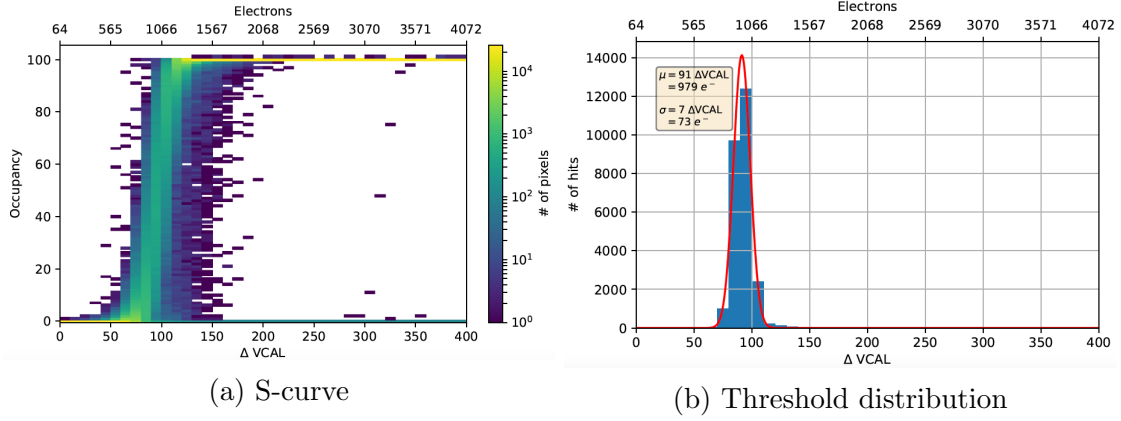


Figure 4.8: (a) S-curve and (b) the fitted threshold distribution for an unirradiated module tuned to 1000 e threshold.

test if the desired threshold value has been acquired after a tuning. This scan executes several analog scans with varying injection charge for each pixel to find the actual threshold value. In a threshold scan, the lower value of the differential injection DAC (VCAL_MED) is set to a fixed value while the higher value (VCAL_HIGH) is scanned over a defined injection range (VCAL_HIGH.start to VCAL_HIGH.stop) with a set step size (VCAL_HIGH.step). The VCAL_HIGH.stop can be set to a higher or lower value and likewise the step size can be changed depending on the requirements. This scan yields the S-curve for each enabled pixel and shows the amount of hits in a pixel at a given injection value. Fitting this curve returns the threshold and the corresponding noise. Figure 4.8 shows the S-curve and the fitted threshold distribution for an unirradiated module obtained from executing a threshold scan.

The main purpose of threshold tuning is to achieve the same value of the threshold for each pixel such that a uniform response is obtained in the entire module. This can be achieved by adjusting two registers in the chip which control the global and local discriminator (TDAC) stages of the chip respectively. The global discriminator sets a common threshold for the entire chip while the TDAC is used to fine tune the threshold of each pixel separately. Threshold tuning is done using the following scans:

1. "meta_tune_threshold_noise.py": This script tunes the chip to the lowest possible threshold by running a noise occupancy scan in a loop. It increases the local threshold of noisy pixels until they are either no longer noisy or disabled. The tuning is completed in two cases: (i) a specified amount of pixels is disabled, (ii) the TDAC distribution is centered.
2. "tune_local_threshold.py": This script scans over the local threshold (TDAC) with fixed global threshold to find the optimal TDAC value for each pixel.
3. "scan_noise_occupancy.py": This script sends triggers without injection into enabled pixels to identify and mask noisy pixels.

From the first two scans listed above a mask file is generated, containing the TDAC value for each pixel. A threshold scan is repeated to determine if the desired threshold has been

achieved. If the module is still noisy, the noise occupancy scan is executed which overwrites the the mask file, adding the information of which pixels are disabled. During the time of this thesis, ToT tuning and ToT-to-Charge calibration tuning is still under development. The final mask file along with the settings for the tuned front-end is used to carry out the charge collection measurements by executing source scans which are equivalent to an external trigger scan with Hit-Or.

5 Sensor characteristics

5.1 Characterisation of IV

The first step in sensor characterisation is measuring the leakage current as a function of the bias voltage. Using these IV measurements, the breakdown voltages of the sensors are identified thus defining their operational limit. These measurements are done at each step - after the sensor structures are embedded into the wafer (at wafer level), after they are singularised (at diced-sensor level) and finally after flip-chipping and wire-bonding to the PCB (at module level). The characterisation of IV are also done for irradiated sensors and modules as this allows the investigation of the detector performance in the operational conditions at HL-LHC.

The sensor structures studied within this thesis:

1. SOI4 sensors at wafer level, diced-sensor level and module level
 - a) comparison of IV curves between different sensor structures
 - b) characterisation of IV of standard wafers of 100 μm and 150 μm thickness
 - c) investigating the effect of TiW layer and the change in IV characteristics after removal of this layer
 - d) comparison of IV curves at different stages - from wafer level to module level
2. Irradiated sensors of the SOI3 and CiS production at diced sensor level
 - a) comparison of IV curves for different fluences

For the SOI4 production, the characterisation of the leakage current as a function of the bias voltage has been performed starting from wafer level to module level. This production consists of wafers of two different thicknesses and exploits three different designs of the biasing structures. The sensor designs used in this production have been discussed in 3.4. The three different pixel cell sizes: $50 \times 50 \mu\text{m}^2$, $25 \times 100 \mu\text{m}^2$ and $50 \times 250 \mu\text{m}^2$ exhibit different characteristics driven by the distance between two implants and have been schematically represented in Figure 5.1.

The $50 \times 50 \mu\text{m}^2$ pixel cells have implants of dimension $36 \times 36 \mu\text{m}^2$ and the maximum distance between two neighbouring implants is about 27 μm . The $25 \times 100 \mu\text{m}^2$ pixel cells have implants of dimension $19 \times 90 \mu\text{m}^2$ with 15 μm inter-implant distance. The

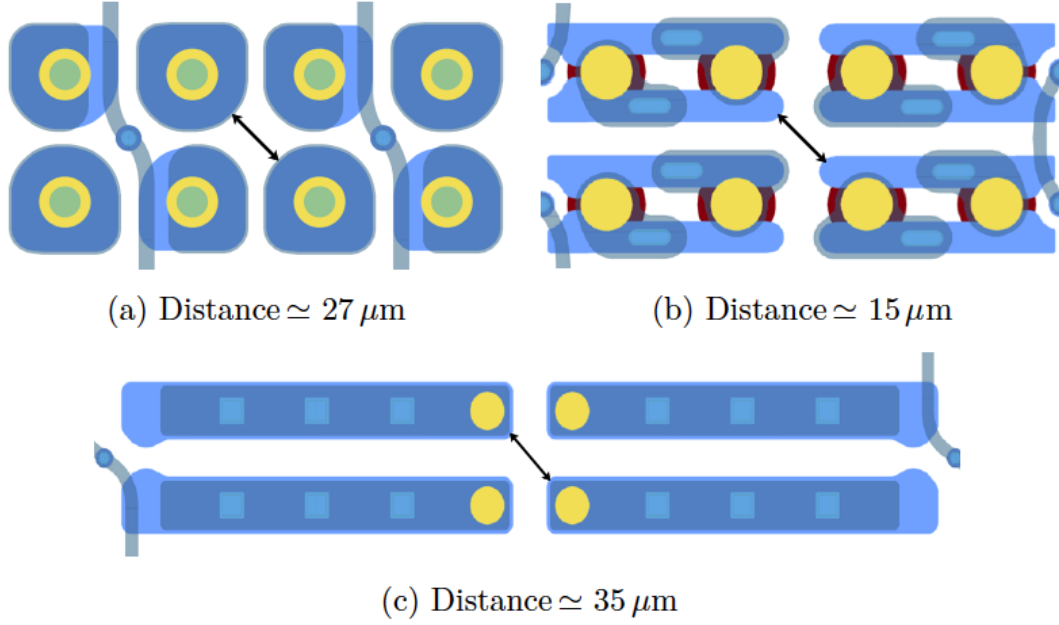


Figure 5.1: Schematic representation of the dimensions of the pixel cell implant showing the inter-implant distances for the different pixel cell sizes where (a) is $50 \times 50 \mu\text{m}^2$, (b) $25 \times 100 \mu\text{m}^2$ and (c) $50 \times 250 \mu\text{m}^2$. This image has been taken from [20].

$50 \times 250 \mu\text{m}^2$ pixel cells have implants of dimension $30 \times 230 \mu\text{m}^2$ with an inter-implant distance of $35 \mu\text{m}$. Smaller distances between two implants result in a lower electrical field at the interface between the pixel implant and p-spray and consequently larger breakdown voltages. Comparing structures "25 × 100 – 450 – BRground", "50 × 50 – 250 – BRsplit" and "50 × 250 – 450 – BRground" in Figure 5.2a, it is observed that the $25 \times 100 \mu\text{m}^2$ pixel cell sensor has the highest breakdown voltage of 230 V followed by the $50 \times 50 \mu\text{m}^2$ pixel cell sensor which breaks down at 140 V and finally the $50 \times 250 \mu\text{m}^2$ pixel cell sensor which has the lowest breakdown voltage of 90 V. From Figure 5.2, it is observed for the $50 \times 50 \mu\text{m}^2$ pixel cells with the metal over-hang design on top of the punch-through structure have a very high operational limit with breakdown voltage around 350 V – 500 V. The very high breakdown voltages in the sensors with this design is due to the shift of the electrical field to the silicon oxide layer which possesses a higher electrical strength than silicon.

For most pixel cell types and biasing structures, thicker sensors have higher breakdown voltages as shown in figure Figures 5.2 and 5.3 for sensors embedded in a wafer and after dicing, respectively. One exception observed is the "50 × 50 – 250 – BRsplit-PTovrhng" sensor at wafer level, probably due to a local defect of the 150 μm thick sensor.

The depleted region of a sensor can be approximated by a capacitor, with the undepleted p and n⁺ regions as electrodes. Upon application of a reverse bias voltage, the width of the depletion region increases, which increases the distance between the electrodes. For a larger thickness of the sensor, a higher depletion depth is achieved, with a lower electric field for the same applied bias voltage. The lower electric field then results in a higher

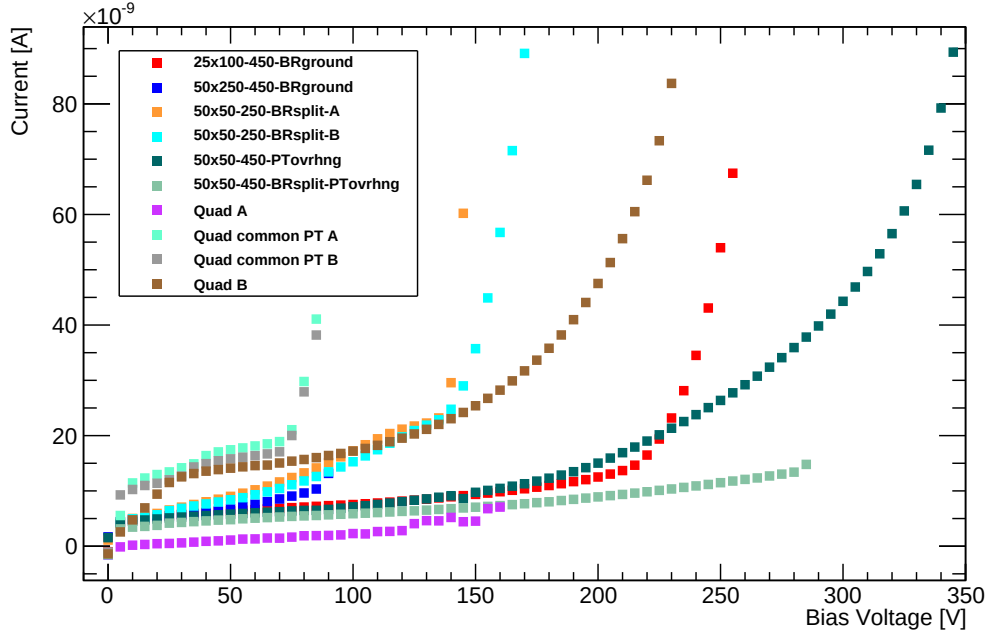
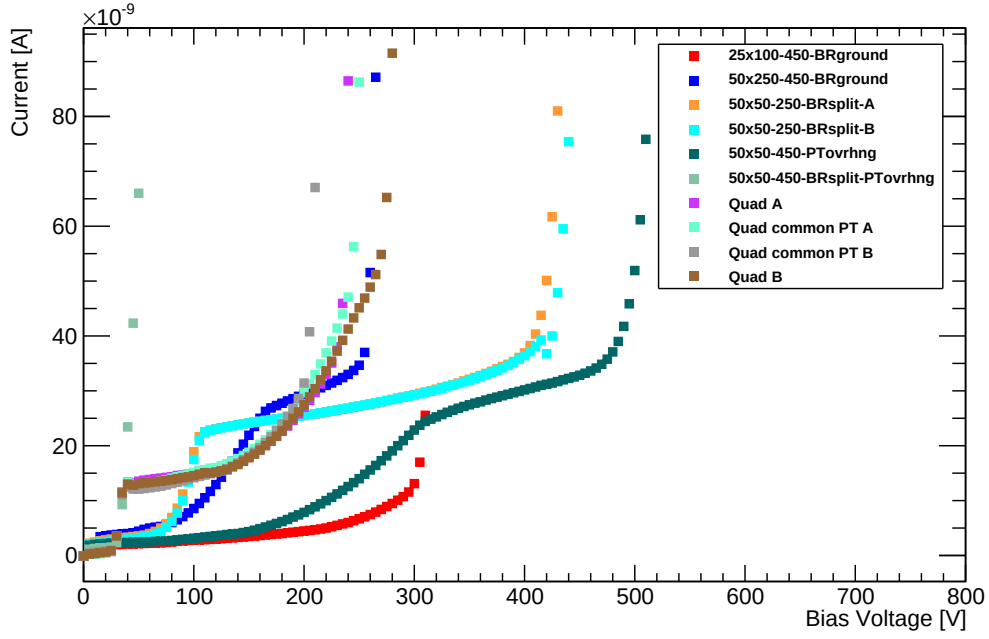

(a) Wafer 3 of $100 \mu\text{m}$ thickness

(b) Wafer 6 of $150 \mu\text{m}$ thickness

Figure 5.2: Measured leakage current as a function of bias voltage for some selected sensors embedded into two exemplary wafers of (a) $100 \mu\text{m}$ and (b) $150 \mu\text{m}$ thickness.

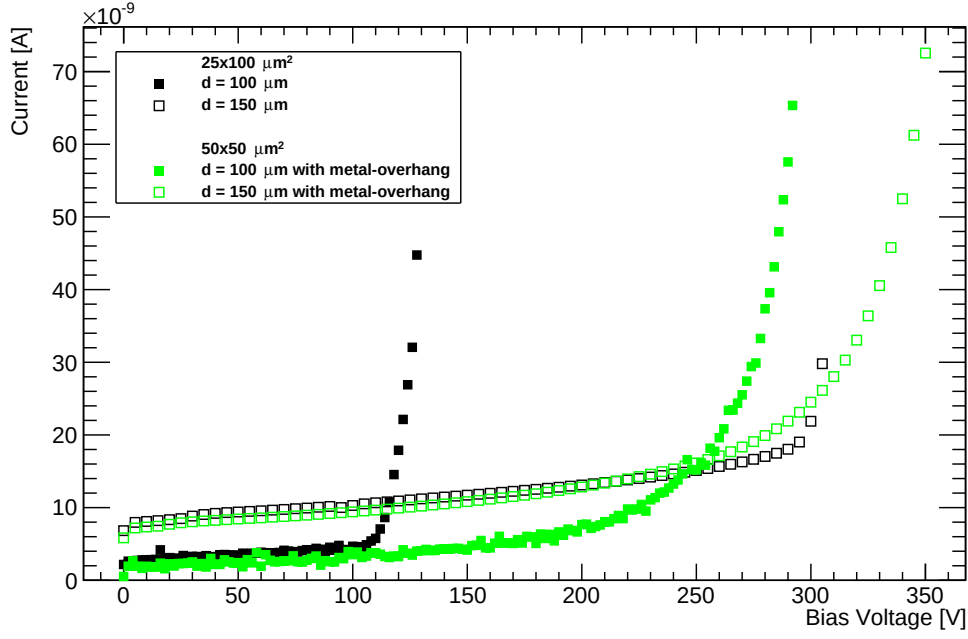


Figure 5.3: Comparison of the IV curves at diced-sensor level of sensors of 100 μm and 150 μm thicknesses for $25 \times 100 \mu\text{m}^2$ and $50 \times 50 \mu\text{m}^2$ pixel cells with a grounded bias ring.

breakdown voltage. Pixel cells of $25 \times 100 \mu\text{m}^2$ geometry exhibit breakdown voltages around 300 V for sensors of thickness 150 μm thickness, while sensors of 100 μm thickness break down around 210 V – 230 V as observed from Figure 5.2 at wafer level. Pixel cells of $50 \times 50 \mu\text{m}^2$ geometry, with a grounded bias ring, exhibit breakdown voltage around 250 V for sensors of 150 μm thickness, while sensors of 100 μm thickness break down around 150 V as observed from Figure 5.2 at wafer level. After dicing, as the $25 \times 100 \mu\text{m}^2$ geometry show a breakdown around 260 V for sensors of 150 μm thickness, while sensors of 100 μm thickness break down at around 110 V as observed from Figure 5.3. Also comparing the sensors with metal overhang for the two thicknesses, the thicker sensor breaks down at 300 V while the other breaks down at 250 V.

The influence of dicing on the breakdown voltage for some of the sensor structures is displayed in Figure 5.4. The electrical field at the sensor edges increases because of the dicing process, that introduces damages to the silicon lattice, thus lowering the breakdown voltage. For almost all the pixel cell types, and the different biasing structures, the breakdown voltage is seen to decrease after dicing.

The $50 \times 50 \mu\text{m}^2$ pixel cell design is implemented with two different edge distances in the

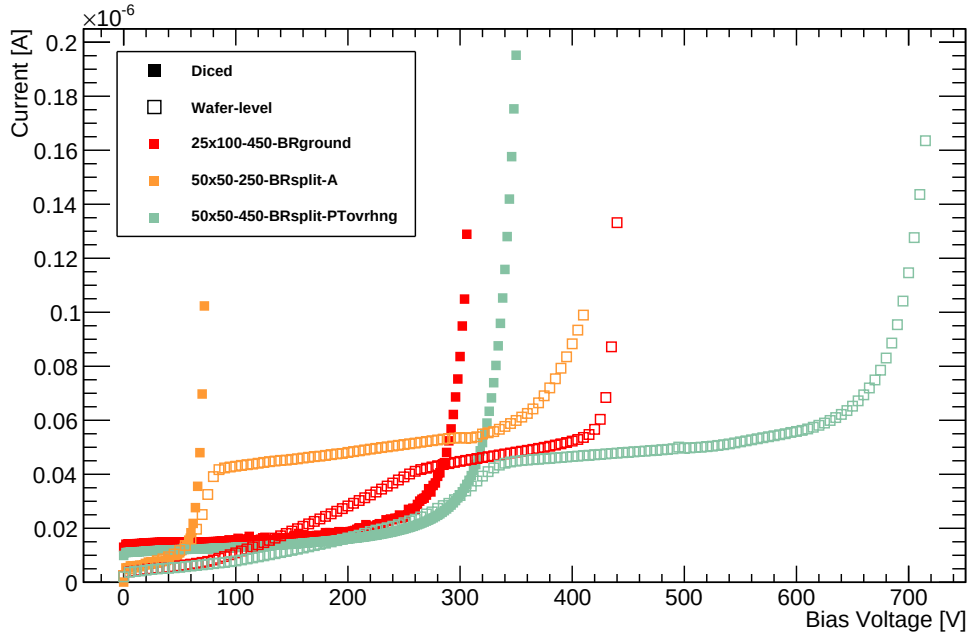


Figure 5.4: Comparison of measured leakage current as a function of bias voltage between selected sensors at wafer level and after dicing for wafer 8 of $150\ \mu\text{m}$ thickness.

”BRSplit” design, as explained in 3.4. Comparison of the IV curves for singularised sensors with different edge distances, in Figure 5.5, reveals that sensors with the standard edge region $d_e = 450\ \mu\text{m}$ have a higher breakdown voltage in comparison to sensors with smaller edge region $d_e = 250\ \mu\text{m}$. The standard edge region is structured to have ten guard rings and one bias ring while the smaller edge region is structured to have seven guard rings and one bias ring. The slope of the potential drop between the ground potential at the bias ring and the high voltage at the sensor edge is affected by this width. The wider the edge region with a higher number of guard rings, the smoother and lower the electric field. Therefore, the breakdown voltage is higher. In the case of the $100\ \mu\text{m}$ thick sensors of wafer 3 shown in Figure 5.5, sensors with $50 \times 50\ \mu\text{m}^2$ pixel cells, with standard edge region exhibit a breakdown voltage of $120\ \text{V}$, while for the smaller edge region, the breakdown voltage is $100\ \text{V}$. In the case of the $150\ \mu\text{m}$ thick sensors of wafer 6 with the standard edge region, the breakdown voltage is $290\ \text{V}$ while with the smaller edge region the breakdown voltage is $50\ \text{V}$.

In the SOI4 production, two wafers of $150\ \mu\text{m}$ thickness were processed with a special photolithographic step. The applied titanium-tungsten (TiW) layer forms a barrier layer preventing the atoms of the copper contained in the UBM to diffuse into the silicon as discussed in 3.4. The dedicated lithographic step shapes the TiW in such a way that this temporary metal shorts all implants within the bias ring of the sensors. In this way it is

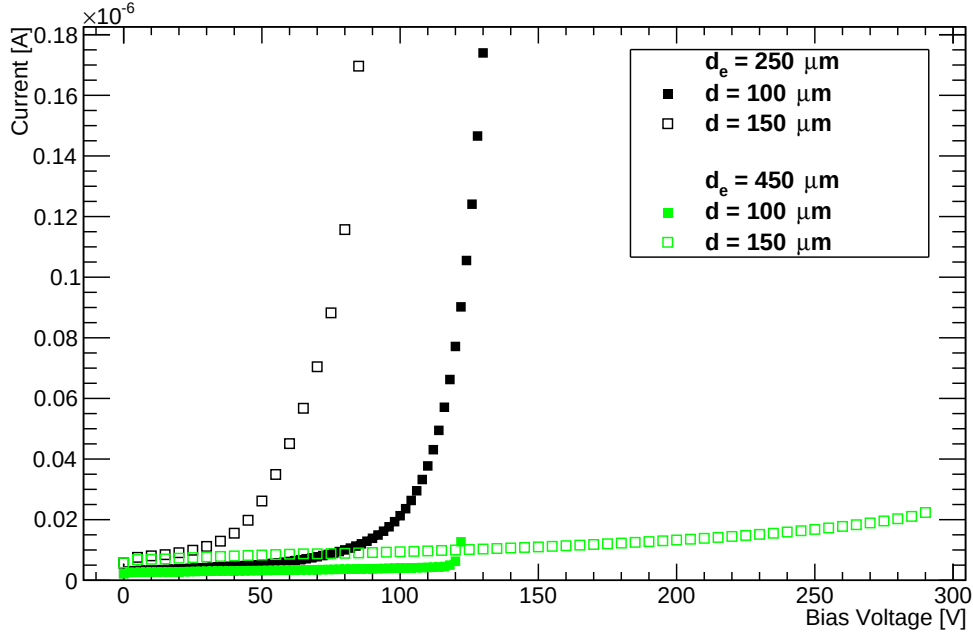
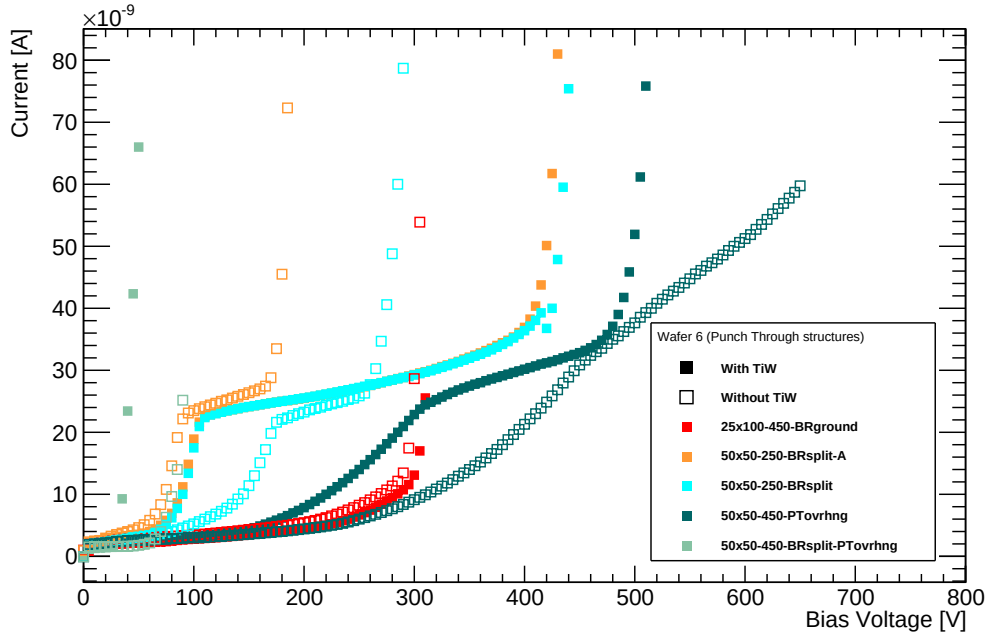
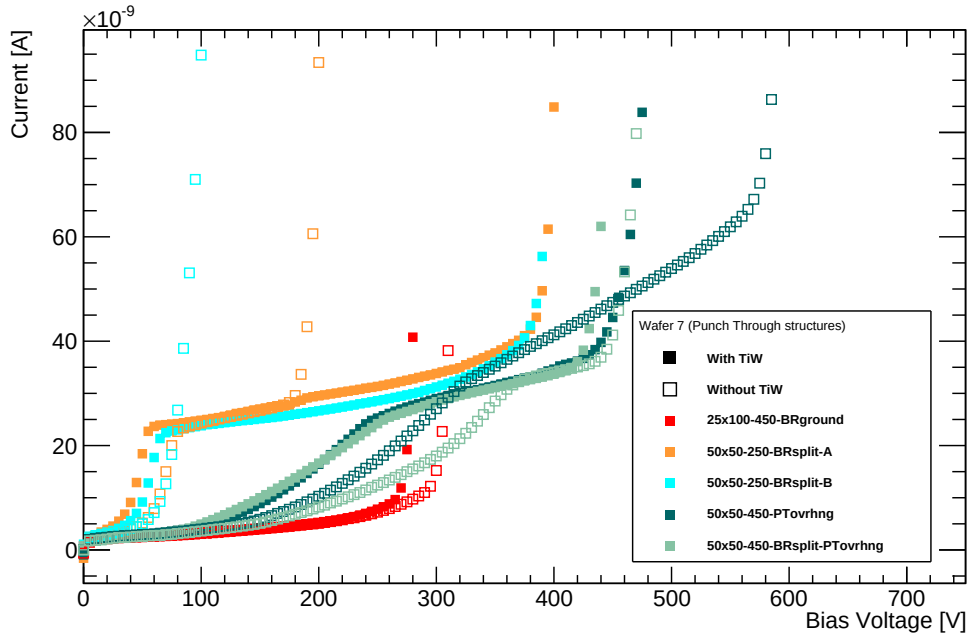


Figure 5.5: Comparison of IV curves between different edge distances for sensors with $50 \times 50 \mu\text{m}^2$ pixel cells for wafers with thicknesses of $100 \mu\text{m}$ (wafer 3) and $150 \mu\text{m}$ (wafer 6).

possible to apply the ground potential to all the implants for the IV characterisation, also in the case where a permanent biasing structure is not implemented. The IV characterisation was done for all sensors at wafer level for structures with and without punch through structures, before the removal of the TiW layer that is routinely done to leave this barrier only below the copper UBM pads. The measurements with the TiW layer were compared with those performed, after the removal of the TiW layer, in both cases at wafer level. After the TiW etching, this is only possible for those structures with punch through. The IV characterisation before and after TiW layer removal for sensors with punch through structures is displayed in Figure 5.6 and without punch through structures in Figure 5.7a, only with TiW. Most of the structures have a good IV characteristic after TiW removal as shown in Figure 5.6. Therefore performing the intermediate measurement does not represent a risk for the sensor performance. In general, the breakdown measured with the TiW layer is higher than in the case of the IV performed through the punch-through mechanism. This is expected since the TiW layer results in a diode-like configuration with a lower electric field than what is created through the punch-through implants. The sensors with metal overhang are exceptions with larger breakdown voltages after the TiW removal. Figure 5.7b is a comparison of the IV curves between sensors with and without punch through structures. It is observed that the breakdown voltages of sensors with punch through structures is equivalent to that of sensors without punch through structures hinting to a good performance of this second type of structure. Lastly, Figure 5.8 is a comparison of the IV curves at wafer level and after dicing for the sensors with punch through structures. As observed in Figure 5.4 for wafer 8, the breakdown voltage is lower after dicing for the



(a) wafer 6



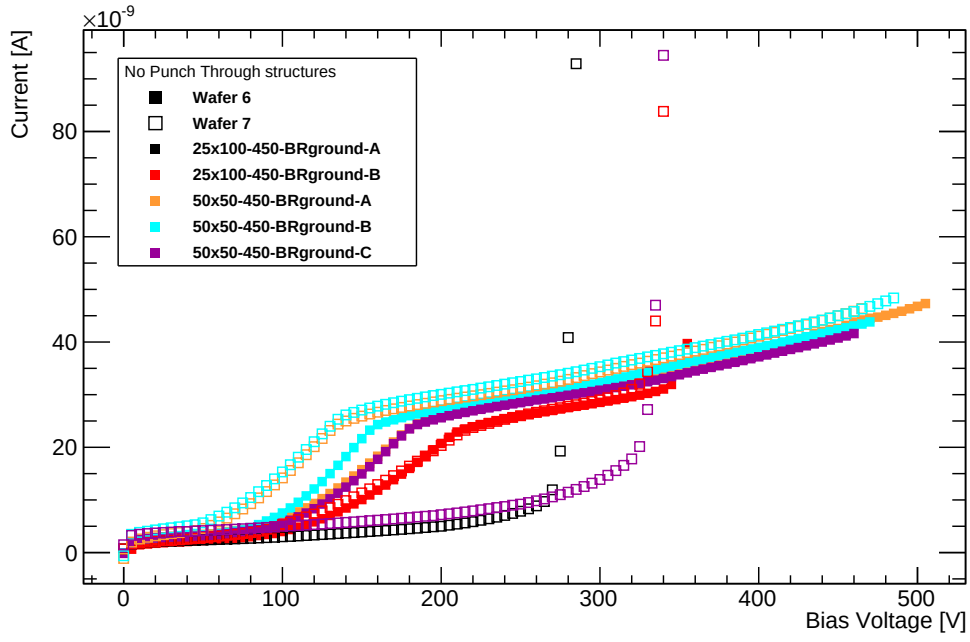
(b) wafer 7

Figure 5.6: Measured leakage current as a function of bias voltage for sensors embedded into two different wafers of $150\ \mu\text{m}$ thickness, before and after removing the coating with a TiW layer for the sensors with punch through structures.

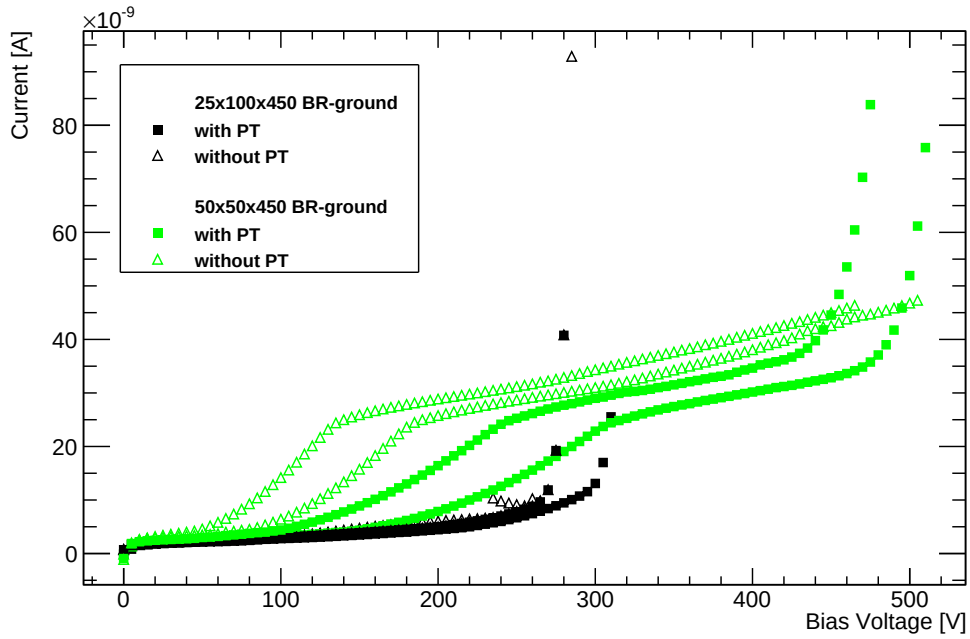
sensors of wafers 6 and 7.

The characterisation of the leakage current as a function of the bias voltage has been performed also for some irradiated sensors designed to be flip-chipped with RD53A read-out chips of the SOI3 wafer production. One of the sensors was irradiated to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ and the other to a fluence of $1 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$. These irradiated sensors show higher leakage current in comparison to unirradiated ones as explained in 2.3 and 2.5. The increase of the leakage current is proportional to the received fluence as shown in Figure 5.9.

The final stage of IV characterisation are the measurements done at module level. In comparison to diced-sensor level, the breakdown voltage is generally further reduced. Therefore, only sensors with breakdown voltages higher than 100 V were selected to be interconnected to the read-out chips. The RD53A modules as seen in Figure 5.10 have an operational voltage limit ranging from 70 V for most sensors to 200 V in exceptional cases like the $25 \times 100 \mu\text{m}^2$ sensor. This is probably because this sensor has a standard edge region while the others shown in the figure have a smaller edge region.

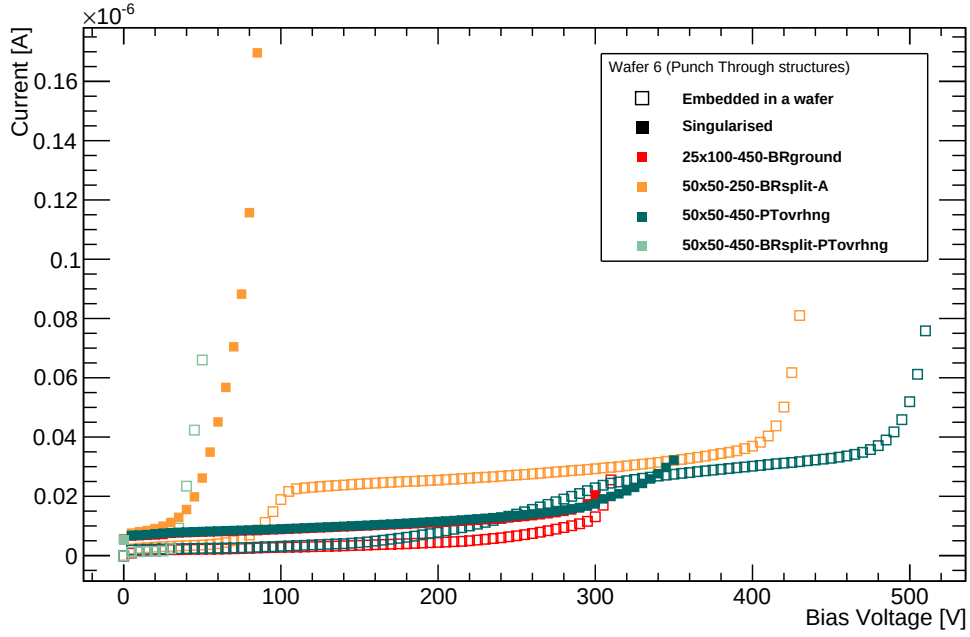


(a) No Punch Through structures for both the wafers

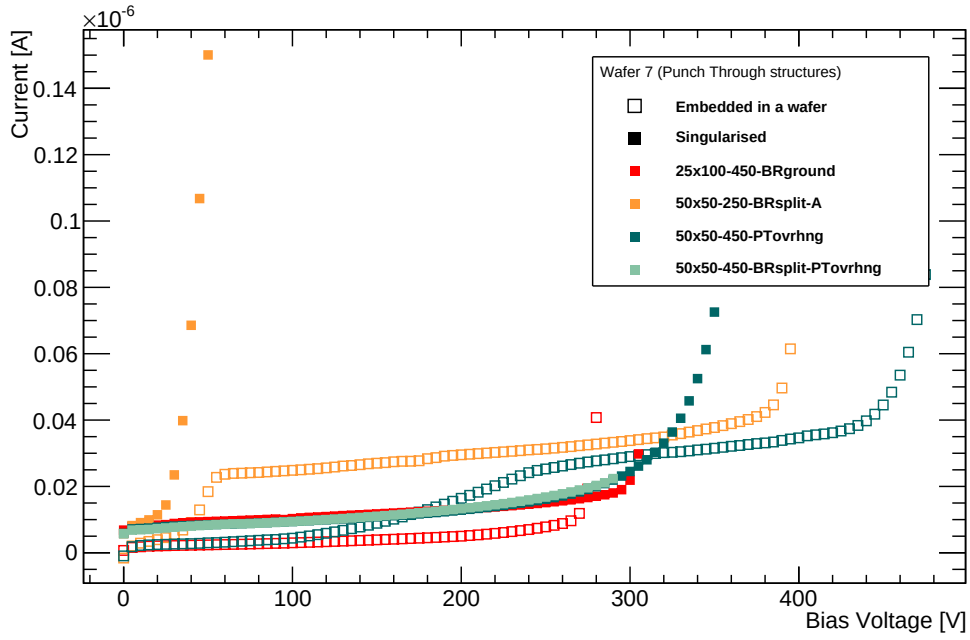


(b) Comparing punch through with no punch through structures

Figure 5.7: (a) Measured leakage current as a function of bias voltage for sensors embedded into two different wafers of $150\ \mu\text{m}$ thickness, before and after removing the TiW layer for the sensors without punch through structures and (b) comparison of the IV curves between structures of same geometry for sensors with punch through and without punch through structures before the removal of TiW layer.



(a) wafer level vs. singularised for wafer 6



(b) wafer level vs. singularised for wafer 7

Figure 5.8: Comparison of measured leakage current as a function of bias voltage for sensors embedded into two different wafers of $150\text{ }\mu\text{m}$ thickness after singularisation for the sensors after TiW removal.

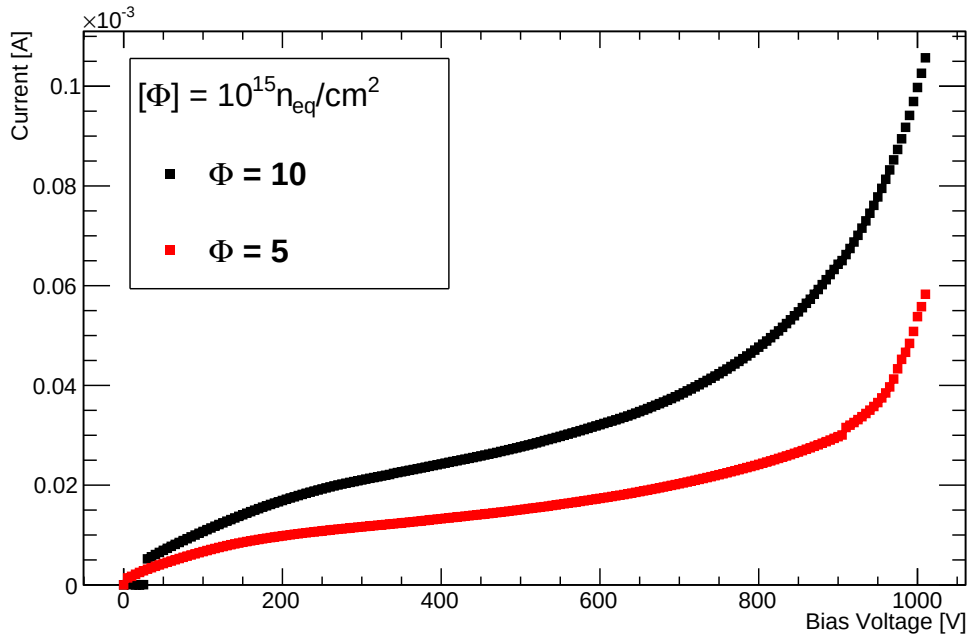


Figure 5.9: Comparison of IV curves at a set temperature of -25°C irradiated at different fluences of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ and $1 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$.

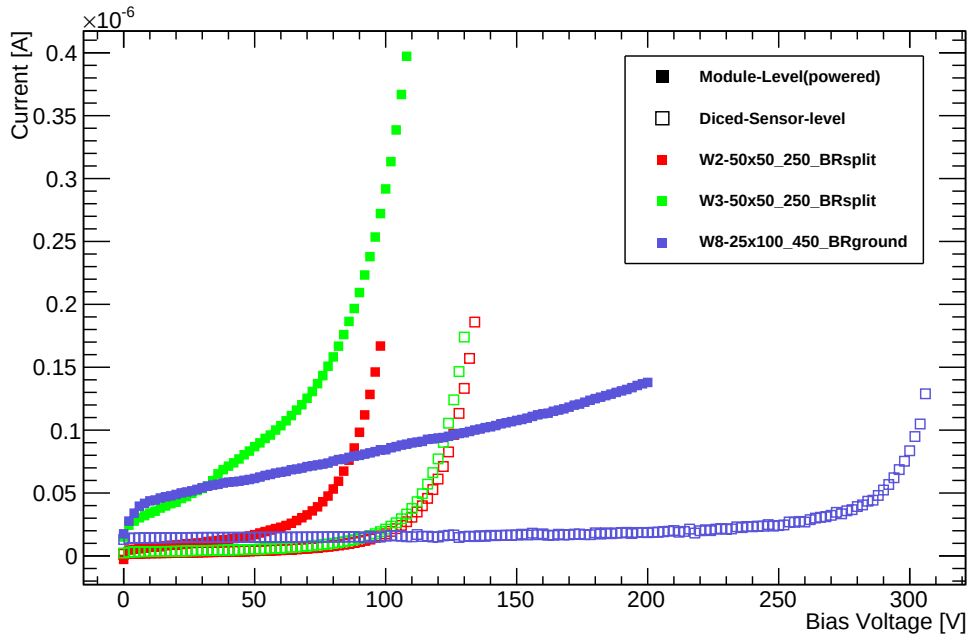


Figure 5.10: Measured leakage current as a function of bias voltage for sensors at diced-sensor level and at module level of $100 \mu\text{m}$ and $150 \mu\text{m}$ thickness. Here, W2, W3 and W8 denotes the wafer number of the SOI4 production.

5.2 Charge collection

The charge collection properties of a module is investigated with radioactive sources or a particle beam. The measured ToT is proportional to the charge released by the particles passing through the sensor [12]. The ToT distribution in case of charged particles is described by a Landau function convoluted with a Gaussian function as shown in Figure 5.11. The Landau curve represents the collected charge expected theoretically in case of a MIP, while the Gaussian function represents the experimental resolution. Using the most probable ToT value obtained as a function of the bias voltage, the deposited charge and the depletion voltage of the sensor is estimated.

5.2.1 Laboratory measurements

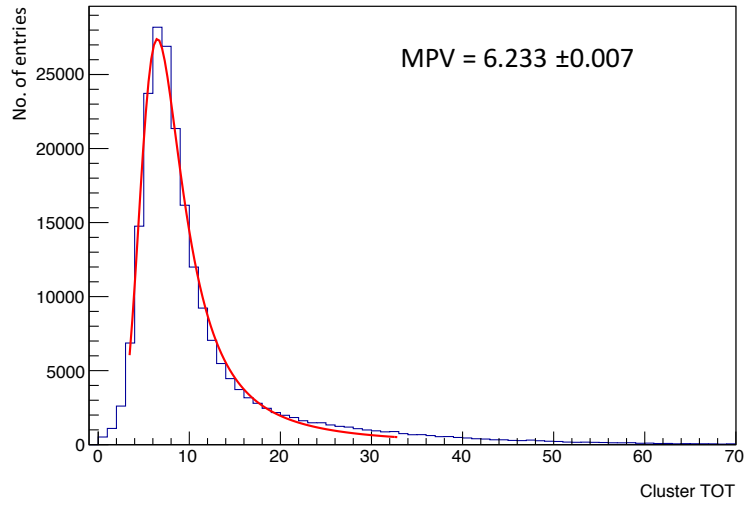
To investigate the charge collection in the laboratory, the experimental set-up discussed in 4.1.2 is employed. The modules of 100 μm and 150 μm sensor-thicknesses used are unirradiated. Both the linear and differential front-ends of a RD53A read-out chip were investigated (see 3.5). Source scans were performed using a ^{90}Sr source that decays via β^- decay. These scans were done at different voltages from 1 V to 50 V or 60 V. The cluster ToT distribution was extracted and the number of entries as a function of the cluster ToT was fitted to the convolution of Landau and Gaussian functions to obtain the most probable cluster ToT value at each voltage. Figure 5.11a shows the number of entries as a function of the cluster ToT for a module of 100 μm thickness biased at 60 V for the differential FE and tuned to a threshold of 1560 e.

The most probable cluster ToT is shown as a function of the voltage for the modules and their respective FEs in Figure 5.12. It is observed that thicker the sensor, higher the depletion voltage. The sensor with $50 \times 50 \mu\text{m}^2$ pixel cells and has a thickness of 100 μm saturates at 5 V, while the sensor with $25 \times 100 \mu\text{m}^2$ pixel cells and a thickness of 150 μm saturates at 11 V. Also a comparison between the linear and differential FE in terms of ToT is shown. For the same sensor, for the analogue circuitry of the different FEs, the charge saturation voltage is observed to be similar, around 5 V.

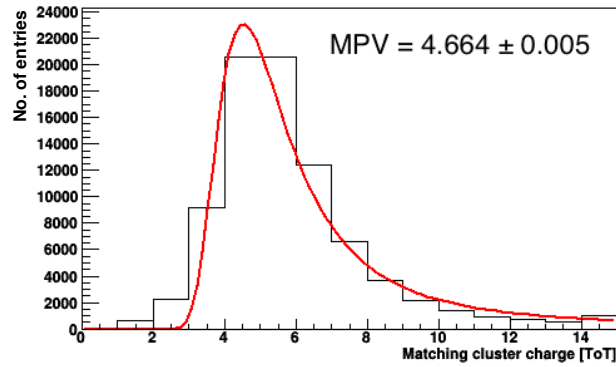
5.2.2 Test beam results

To investigate the charge collection properties of modules, a test beam set-up discussed in detail in [21, 41], is employed. High energy pion beams of 120 GeV were used for the modules shown in Figures 5.13 and 5.14. The measurement was done in two ways:

1. from the raw data files that were reconstructed using EUDET and TBMON software as described in [21, 41]. From the analysed data file, the cluster ToT distribution was fitted to a Gaussian function convoluted Landau function and the obtained most probable ToT value is displayed as a function of the bias voltage in Figure 5.13. Some fluctuations of the ToT after saturation are also observed. However, the depletion voltage of the module with a sensor of 100 μm thickness and $50 \times 50 \mu\text{m}^2$ pixel cells



(a) An example of fitting the cluster ToT histogram using a langaus fit function.



(b) An example of fitting the cluster ToT histogram from a track file from the data collected in a test-beam.

Figure 5.11: (a) ToT distribution together with a fit to a convolution of a Landau and a Gaussian function for a module of 100 μm thickness biased at 60 V for the differential front-end which is tuned to a threshold of 1560 e. The figure shows the number of entries as a function of the cluster ToT. The most probable cluster ToT value obtained from the fit is 6.233 ± 0.007 , where the quoted uncertainty is statistical only. (b) Example of fitting the cluster ToT histogram from a track file analysed from the test-beam data, for a module of 100 μm thickness biased at 15 V for the linear FE which is tuned to a threshold of 1700 e. The x axis displays the cluster ToT and the y axis displays the number entries.

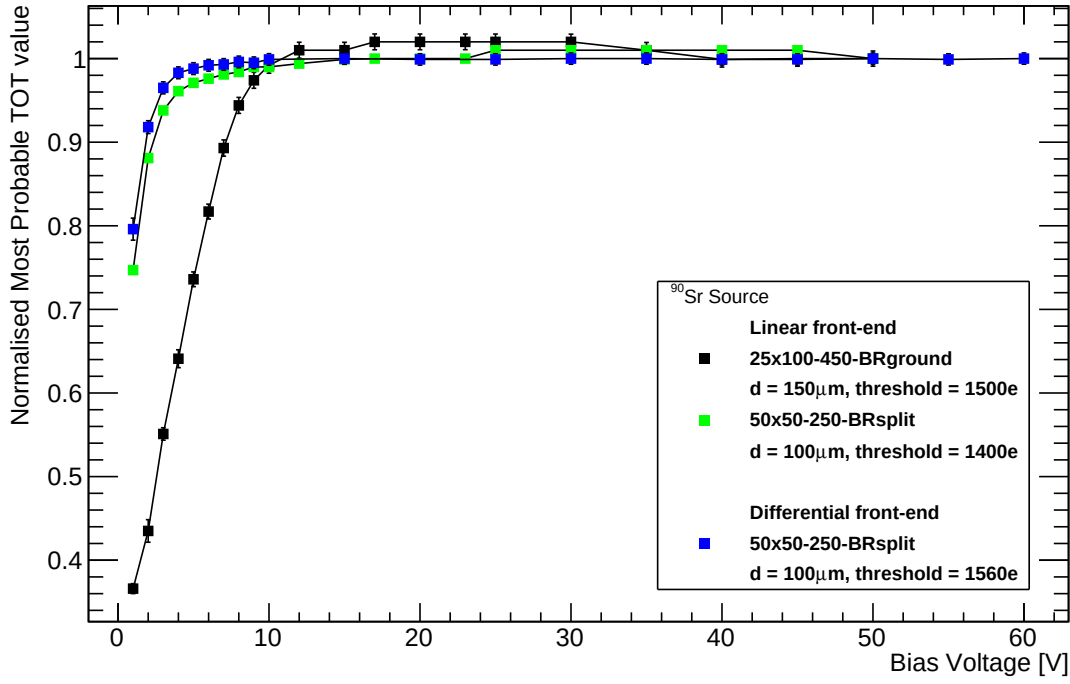


Figure 5.12: Comparing the collected charge of two modules as a function of the Bias Voltage: the first module with a sensor of $100\mu\text{m}$ thickness, using both the linear and the differential FE and the second module with a sensor of $150\mu\text{m}$ thickness, using the linear FE. The most probable ToT values have been normalised to 1. The uncertainty on the most probable ToT value comes from the fit. In this figure no ToT to charge calibration was done.

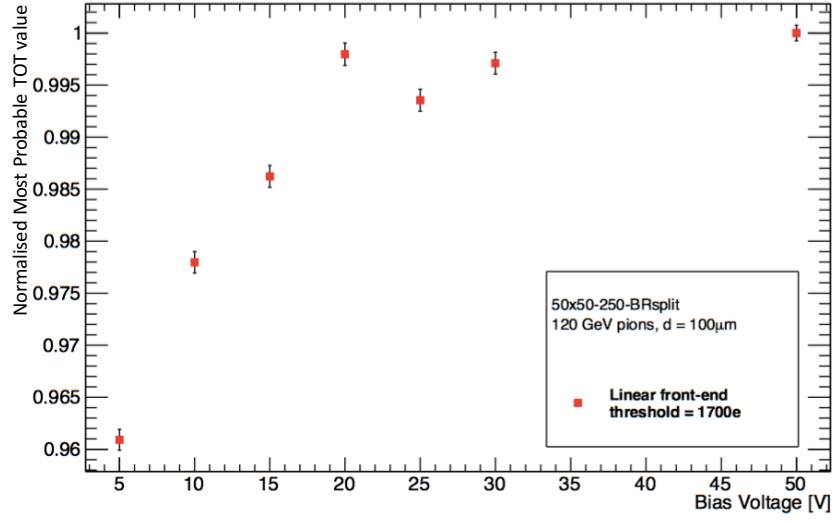


Figure 5.13: For a module of $100\ \mu\text{m}$ thickness using the linear front-end the most probable value of the ToT as a function of bias voltage is shown. The most probable ToT values have been normalised.

for the linear front-end tuned to a threshold of $1700\ \text{e}$ is in the range from $20\ \text{V}$ to $30\ \text{V}$.

2. from the source scans executed using the pion beam instead of the ^{90}Sr source used in the laboratory set-up, to obtain the collected charge and depletion voltage as shown in Figure 5.14 for a module with a sensor of $100\ \mu\text{m}$ thickness and $50 \times 50\ \mu\text{m}^2$ pixel cells for the linear front-end tuned to thresholds of $1700\ \text{e}$ or $1500\ \text{e}$. For the lower threshold the saturation voltage is around $10\ \text{V}$ while for the higher threshold the saturation voltage is around $20\ \text{V}$.

For this set-up the ToT to charge calibration is not yet optimised. The software used to tune the new RD53A modules is still under development and scans to tune the ToT were not yet available at the time of this thesis.

However, it is concluded that, before irradiation, all the sensors of the SOI4 production characterised in this thesis at module level show a very early saturation of the charge collection, namely between $5\ \text{V}$ and $20\ \text{V}$.

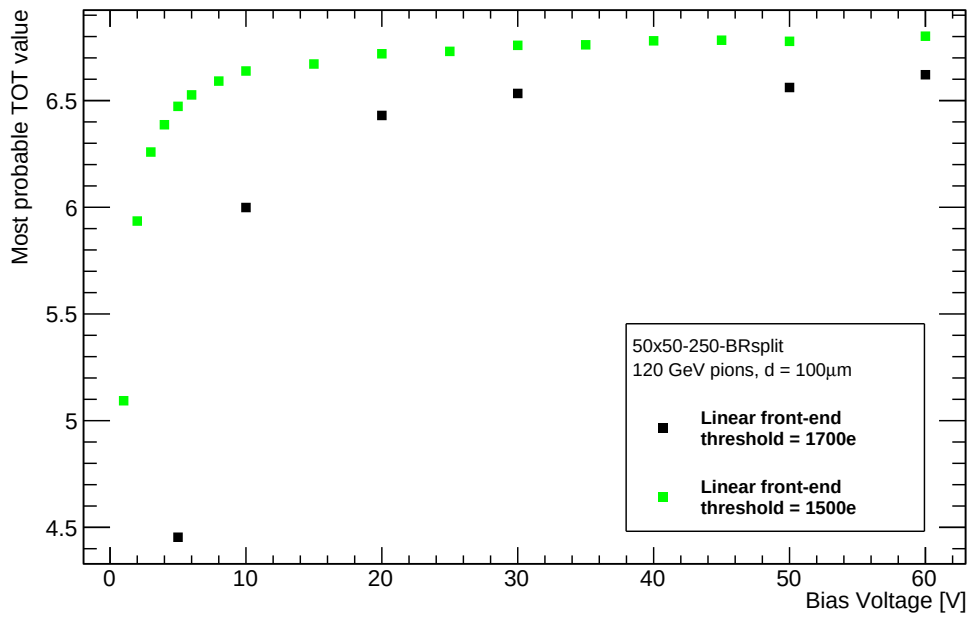


Figure 5.14: The most probable ToT as a function of the bias voltage of a module with a sensor of 100 μ m thickness using the linear front-end tuned to a threshold of 1700 e or 1500 e respectively.

5.3 Properties of the target threshold

An investigation of properties of the target threshold is performed using the laboratory set-up. Modules with an RD53A read-out chip, with sensors of 100 μm and 150 μm thickness, were used. In a general threshold scan, the threshold is measured for each pixel by injecting increasing amounts of charge through the chip injection circuitry, as discussed in 4.2.2. At each scan point, the charge is injected multiple times and the fraction of injections, for which a signal is recorded, is obtained. By definition, the threshold corresponds to a fraction of 50%. The wanted threshold is steered using the BDAQ53 software by setting the global threshold parameter and is referred in this section as the target or tuned threshold. A calibration of the threshold is performed by executing several source scans, increasing the target threshold with each scan for a constant bias voltage. The global threshold parameter setting for the linear front-end is a value that determines the height of the discriminator, while for the differential front-end, employing a differential gain stage in front of the discriminator, the difference between the set values of these two branches is used (see 3.5). Measuring the number of hits from ^{55}Fe and ^{109}Cd sources as a function of the global threshold parameter setting and the equivalent target threshold, determines the real threshold of the module from the global threshold parameter (and tuned threshold) by selecting the measured point which is closest to a fraction of 50% of the total number of hits.

The RD53A read-out chip is designed to be tuned to low thresholds, and therefore for this investigation the ^{55}Fe source, yielding a low energy peak, was initially selected. All source scans were executed for 300 s and the bias voltage was set to 25 V. The ^{55}Fe source decays via electron capture to ^{55}Mn . The capture of the electron by a proton in the nucleus is accompanied by the emission of a neutrino. The process creates a vacancy which is mainly occupied by the dropping down of an electron from a higher energy shell with the emission of a photon or by the ejection of an electron in a process called the Auger effect. These photons release all their energy at once upon interaction with the silicon atoms providing an average signal of approximately 1600 e. The ^{109}Cd source on the other hand releases an average signal of approximately 6100 e. Therefore, the global parameter corresponding to the target threshold of 1600 e or 6100 e, depending on the source used, in principle should result in 50% of the total hits. From Figure 5.15, the following is observed:

1. The global threshold parameter resulting in 50% of the largest measured number of hits does correspond approximately to a target threshold 1600 e. A consistent scale for the threshold was further corroborated using a ^{109}Cd source which also decays via electron capture and provides an average signal of approximately 6100 e from the photons obtained from this process,
2. At very low global threshold parameters which correspond to low thresholds, the S-curve, does not saturate after a certain point as expected.

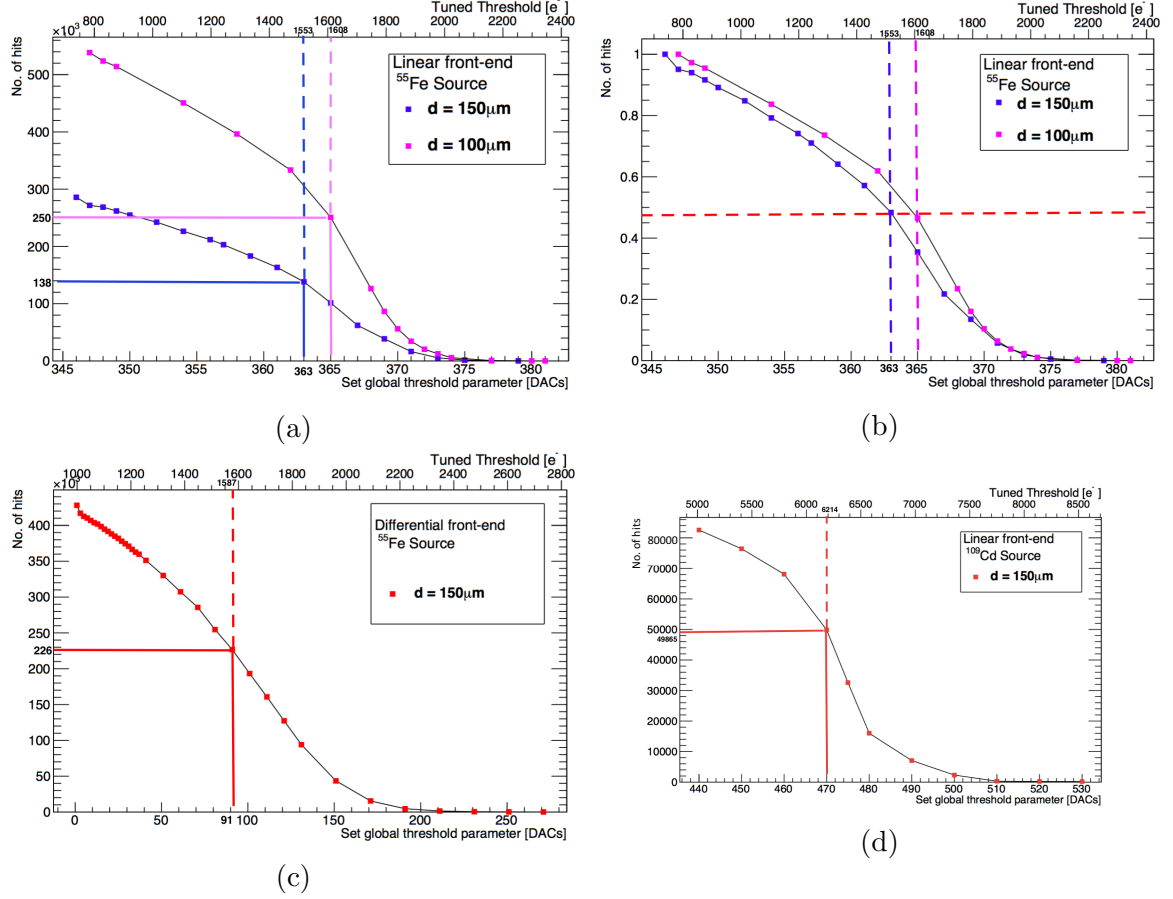


Figure 5.15: Calibration of the threshold for two $50 \times 50 \mu\text{m}^2$ modules of $100 \mu\text{m}$ and $150 \mu\text{m}$ thicknesses without punch through structures. Investigations were done using both ^{55}Fe and ^{109}Cd sources. The number of hits as a function of the set global threshold parameter setting and tuned threshold is shown. In (a) comparison is done for the linear front-end for the two modules of different thicknesses, in (b) the number of hits is normalised to 1, in (c) for the differential front-end of the module of $150 \mu\text{m}$ thickness and in (d) for the linear front-end for the module of $150 \mu\text{m}$ thickness using the ^{109}Cd source.

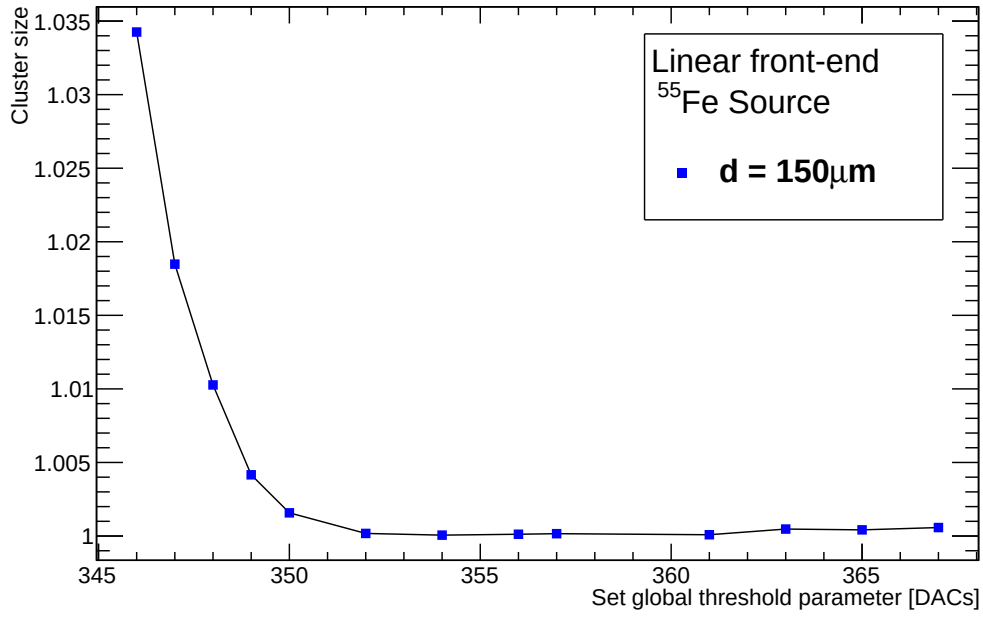


Figure 5.16: The cluster size as a function of the set global threshold parameter for a module with a sensor of $150\ \mu\text{m}$ thickness, $50 \times 50\ \mu\text{m}^2$ pixel cells and without punch through structures for source scans with the ^{55}Fe source.

Charge sharing and multiple scattering at low threshold could result in higher cluster sizes. For a charged particle passing through a sensor, if the generated carriers are collected by a single pixel, the cluster size is 1. If instead the charge is shared between two neighbouring pixels, both above threshold, the cluster size is 2. Measurements to this end were performed using the module with $150\ \mu\text{m}$ thick sensor and the linear front-end. For this module, the number of hits as a function of global threshold parameter setting and equivalent target threshold is shown in Figure 5.15a. From Figure 5.16, for the same module, it is observed that the average cluster size is 1.034. Therefore it is concluded that the maximum contribution to the increase of hits at low threshold for charge sharing is below 4%. From the investigation of the amount of charge-sharing at low thresholds, it is excluded that this is the only cause of the non-saturation.

The following table summarises the observed results from Figure 5.15.

Table 5.1: Summary of the observed threshold for the two modules using the different radioactive sources and front-ends.

Sensor thickness [μm]	Front-end	Source	50% hits	Global parameter [DAC]	Tuned threshold [e]
100	linear	^{55}Fe	250758	365	1608
150	linear	^{55}Fe	138210	363	1553
150	differential	^{55}Fe	226543	91	1587
150	linear	^{109}Cd	49865	470	6214

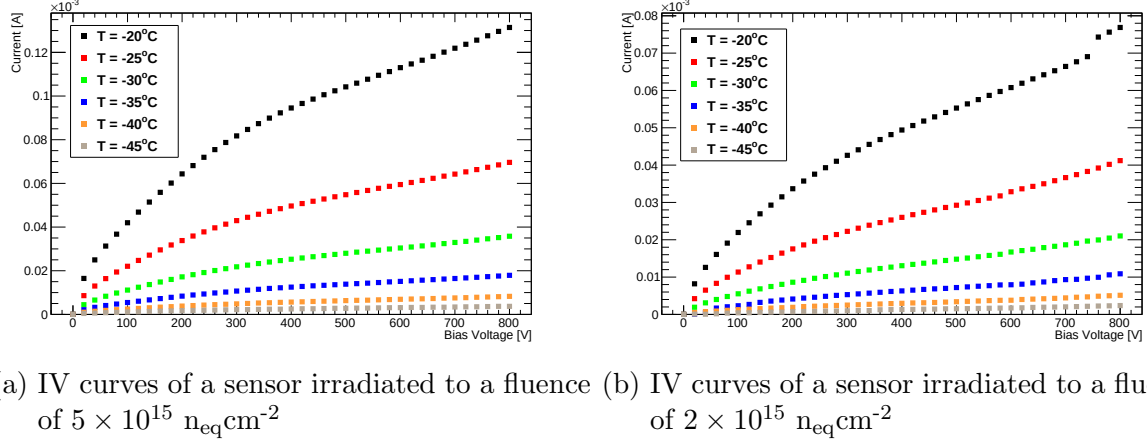


Figure 6.1: Measured leakage current as a function of bias voltage for sensors with $25 \times 100 \mu\text{m}^2$ pixel cells, $150 \mu\text{m}$ thickness and irradiated to a fluence of (a) $2 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ and (b) $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ for different temperatures.

6 The effective band gap energy of irradiated sensors

The innermost tracking detectors of present experiments at the LHC are operated around or below 0°C . The present IBL at the ATLAS experiment is operated at -15°C . The temperature of these detector elements influences its operational parameters such as the leakage current. The temperature scaling of this current is dependent on the effective band gap energy E_{eff} . It is particularly important to measure E_{eff} for irradiated sensors operated in cold temperatures, to reproduce the conditions for the detectors at HL-LHC. The first step is to determine the operational limit of each sensor. This is done by measuring the leakage current, at different bias voltages, over the temperature range of interest. Figure 6.1 shows that the measured leakage current is higher for the sensor irradiated to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ (Figure 6.1a) in comparison to the sensor irradiated to a fluence of $2 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ (Figure 6.1b).

The probe station with the thermal chuck connected to the chiller is used for the measurements as described in 4.1.1. For the final measurements four sensors, irradiated with neutrons at the Jozef Stefan Institute (JSI) in Ljubljana were used. They are tabularised as follows:

Table 6.1: Summary of the types of sensors measured along with their irradiation fluence.

Wafer	Thickness [μm]	Pixel cell size [μm^2]	Fluence [$10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$]
6	150	25×100	2
6	150	50×50	10
7	150	25×100	5
7	150	50×50	5

6.1 Effect of uncertainties in temperature in the effective band gap energy measurements

The dependence of temperature scaling of leakage current $I(T)$ on E_{eff} is described by Equation 2.5. The $I(T)$ dependence is measured either from repeating the IV scans at different temperature values or keeping the bias voltage constant and changing the temperature (IT curve). In case of the irradiated sensors used for the measurements, the bulk generation current $I(T)$ dominates (see 2.5). A problem in measuring the $I(T)$ is the self-heating of the sensors under measurement. Therefore, the actual operating temperature is warmer than the temperature set on the chiller.

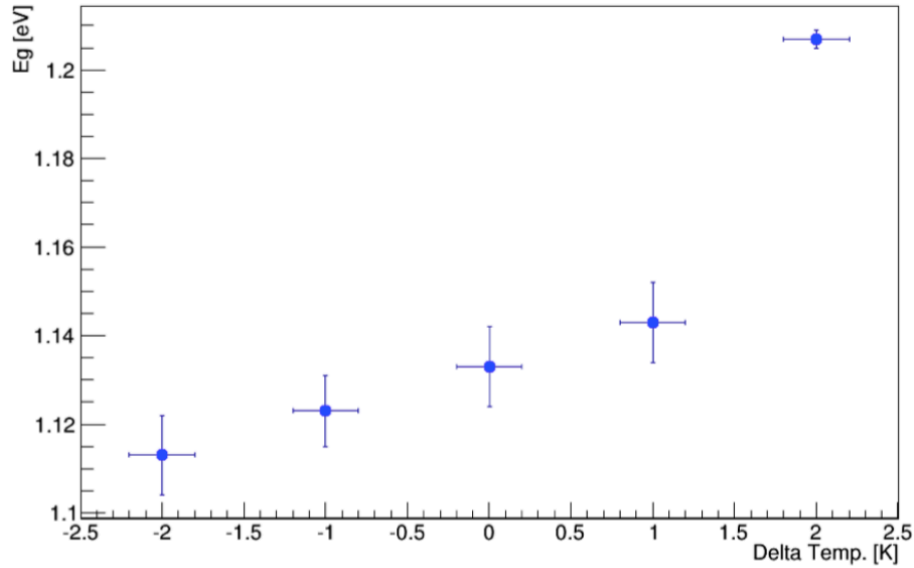


Figure 6.2: Effect of systematic shifts in temperature on effective band gap energy in the initial round of measurements using a sensor from the CiS wafer production, irradiated to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ at a constant bias voltage 800 V, over a temperature range from -25°C to -50°C .

In the initial set of measurements, the effect of systematic shifts in temperature on E_{eff} was studied using a sensor from the CiS wafer production irradiated to a fluence of

Table 6.2: Table displaying the effect of systematic shifts in temperature on E_{eff} studied using a sensor from the CiS wafer production irradiated to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ at a constant bias voltage 800 V over a temperature range from -25°C to -50°C and corresponds with Figure 6.2

With -2° shift [eV]	With -1° shift [eV]	Original E_{eff} value [eV]	With $+1^\circ$ shift [eV]	With $+2^\circ$ shift [eV]
1.113 ± 0.009	1.123 ± 0.008	1.133 ± 0.009	1.143 ± 0.009	1.207 ± 0.002

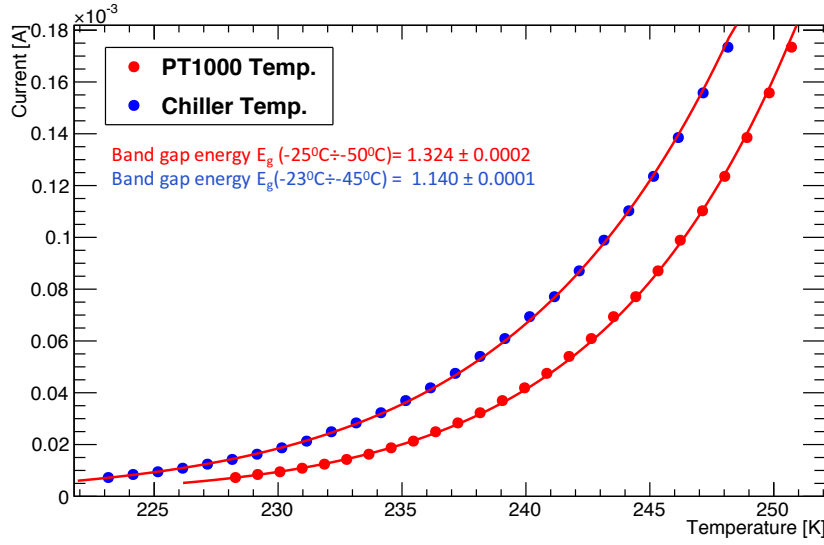


Figure 6.3: Measured leakage current as a function of the temperature measured by a PT1000 sensor (red) and the nominal temperature set in the chiller (blue), at a constant bias voltage of 400 V. E_{eff} is extracted from IT measurements for a sensor from a CiS wafer production which is irradiated to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$.

$5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ at a constant bias voltage 800 V over a temperature range from -25°C to -50°C as shown in Figure 6.2 and included in Table 6.2. For this purpose, the E_{eff} was extracted from the IT curve over the temperature range set using the chiller and constant bias voltage. Then, the value of E_{eff} was extracted from the same measured current values as a function of the set temperature points, shifted by $+$ and -1° and 2° . It was seen that that E_{eff} shows a strong dependence on systematic shifts in temperature with respect to the values assumed in the calculations.

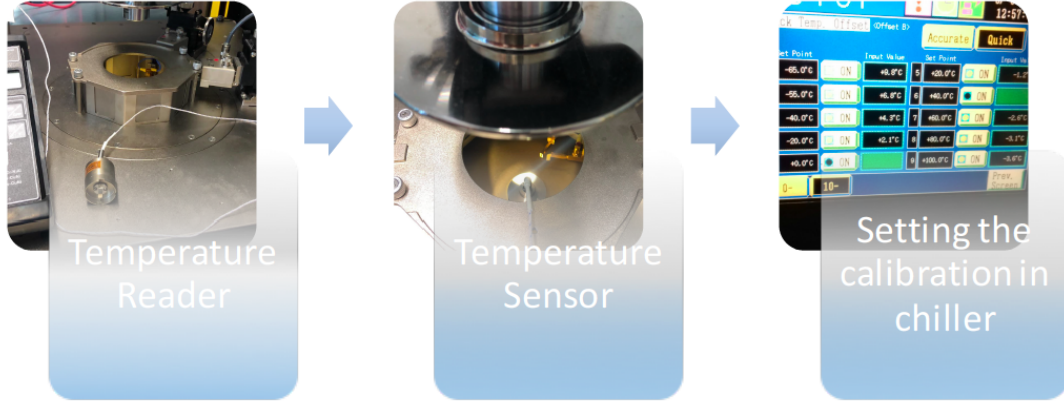


Figure 6.4: Process of calibrating the temperature of the thermal chuck of probe station. The thermocouple was connected to the temperature reader and then placed inside the chuck. Then the pre-installed programme in the chiller controller was run, the offset between the measured data and the set point was calculated and inserted in the chiller steering software.

6.2 Calibration of the probe station

The next step was to check if the temperature set on the chiller was the same as the temperature of the thermal chuck on which the sensor is placed. To this end, three PT1000 sensors were placed, one at a time, on the chuck and from the measured resistance recorded, the actual temperature reading was obtained. A clear offset was observed between the temperature set on the chiller and the average temperature measured using the PT1000 sensors. The observed offset reduces with increasing set temperature value and also the E_{eff} obtained using the average temperature measured by PT1000 is higher as shown in Figure 6.3. This offset in set point and measured temperature is assumed to be caused by environmental losses in the coolant from the chiller to the chuck.

Therefore, a calibration of the operating temperature of the thermal chuck was performed. The process is schematically represented in Figure 6.4. The calibration range was from -65°C to $+200^{\circ}\text{C}$. The thermocouple was placed on the centre of the chuck as shown in Figure 6.4 and was connected to the monitoring equipment. The pre-installed programme in the chiller controller, which included the temperature operation profile i.e. the calibration range with the operation time at each temperature point, was started. Then the offset was calculated (measured data – set point) and the offset at each temperature was inserted into the chiller controller. After calibration, verification of the set point was done for the temperatures used for measurements presented in this thesis and the uncertainty on each set point was observed to be within $\pm 0.5^{\circ}\text{C}$.

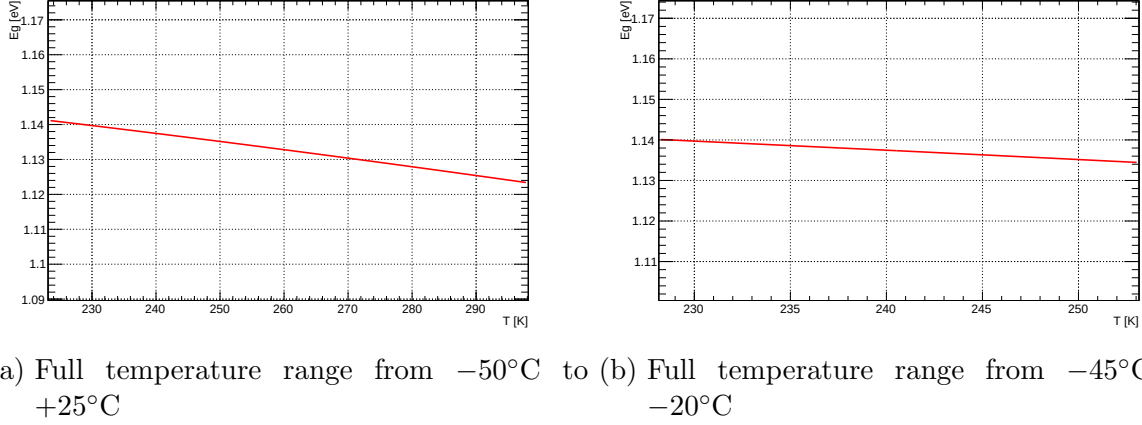


Figure 6.5: Dependence of band gap energy on temperature using Varshni equation over the (a) whole range from -50°C to $+25^\circ\text{C}$ and (b) measured range from -45°C to -20°C .

6.3 Extraction of effective band gap energy

The temperature dependence of E_{eff} according to the Varshni equation is described by Equation 2.1. The difference in ΔE_g shown in Figure Figure 6.5, is approximately 0.017 eV across the whole temperature range from -50°C to $+25^\circ\text{C}$, while it is 0.006 eV in the temperature range investigated in this study (-45°C to -20°C). Therefore, the temperature dependence of E_{eff} is not negligible. This is corroborated from the comparison between the E_{eff} calculated from the fitted $E_{\text{eff}}(0)$ (band gap energy at 0 K) using its temperature dependence according to the Varshni equation and the E_{eff} directly obtained from the fit, shown in Figures 6.6 and 6.7, corresponding to the average value of -32.5°C in the temperature range of -45°C to -20°C .

Two types of data set were used as follows:

- Type—I: several IV scans made at different temperatures. At each bias voltage for a constant temperature, the corresponding current was an average of 10 measured values.
- Type—II: several IT scans made at different bias voltages. At each temperature for a constant bias voltage, the corresponding current was an average of 5 measured values.

A fixed relative uncertainty of 1 K was assigned to the temperature points and the uncertainty assigned to the average current value was the corresponding standard deviation. For the final measurements a one parameter fit was done i.e. only E_{eff} was fitted from the IT curves instead of fitting both the proportionality constant and E_{eff} from 2.5.

At a constant bias voltage, the current dependence on temperature was therefore fit by the following equation thereby eliminating the proportionality constant:

$$\frac{I(T)}{I(T_0)} = \left(\frac{T}{T_0}\right)^2 \exp\left(\frac{-E_{eff}}{2k_B} \times \left(\frac{1}{T} - \frac{1}{T_0}\right)\right) \quad (6.1)$$

The normalisation point T_0 was excluded from the fit. For the fits done using data set I, the normalisation temperature was -25°C and for the fits done using data set II, the normalisation temperature was -20°C .

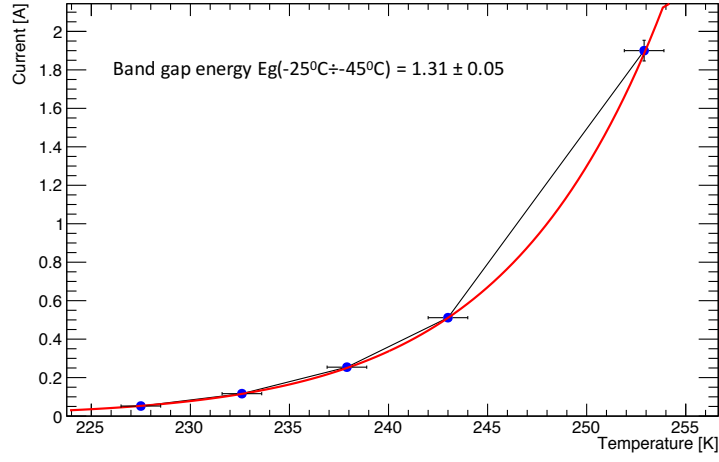
The fits using both types of data set, for the same sensor with $25 \times 100 \mu\text{m}^2$ pixel cells, $150 \mu\text{m}$ thickness and irradiated to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ at a bias voltage of 600 V is shown in Figures 6.6 and 6.7. Figure 6.6 shows the fits done using data set I and Figure 6.7 shows the fits done using data set II. In both cases, the E_{eff} was either fitted directly from the IT curve or was calculated from the fitted $E_{\text{eff}}(0)$ in accordance with the Varshni equation. The value of E_{eff} obtained from fitting the IV curve from data set I is higher than the E_{eff} obtained from fitting the IT curve from data set II. A possible explanation is that with the IT method, the leakage current has a very long time to set at a particular voltage with respect to the IV where the time interval between measurements is set to 300 s. This can result in a lower evolution of the current with the temperature and therefore a lower value of E_{eff} .

The value of $E_{\text{eff}}(0)$ calculated from both data sets is higher the E_{eff} , as expected from the Varshni equation. Also, rescaling $E_{\text{eff}}(0)$ according to this equation, the corresponding value of E_{eff} obtained for the average temperature of -32.5°C in the temperature range of interest gives a good agreement between the two methods (see Figures 6.6a and 6.7). The same fitting procedure was followed for all the four sensors. The results obtained have been included in Table 6.3.

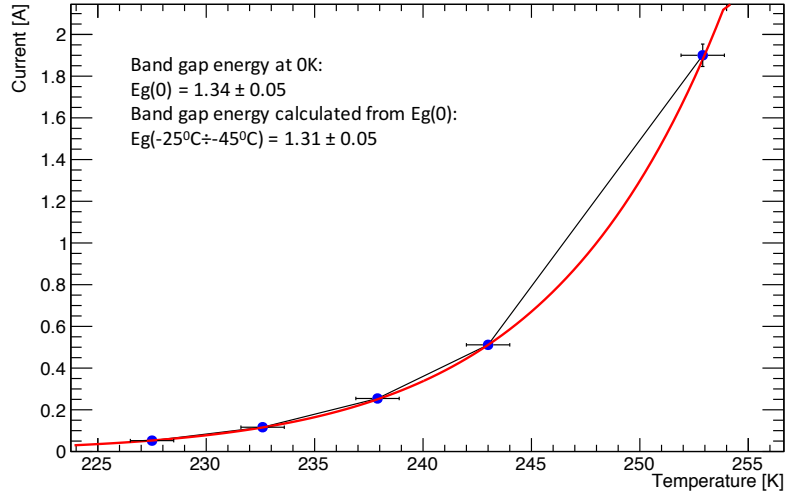
The value of E_{eff} as a function of the bias voltage is shown in Figure 6.8a. With increasing bias voltage the E_{eff} is observed to decrease except in case of the sensor with $50 \times 50 \mu\text{m}^2$ pixel cells, $150 \mu\text{m}$ thickness and irradiated to a fluence of $1 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$. The decrease of E_{eff} with increasing bias voltage is probably due to impact ionisation. The higher the bias voltage, the higher the electric field and higher the impact ionisation coefficient. Also, for the same electric field, higher the temperature, lower the impact ionisation coefficient. Therefore at high voltages for a set temperature, the E_{eff} estimation is biased to a lower value as a higher fraction of $I(T)$ is generated due to impact ionisation. The observed exception is probably caused by power dissipation during measurements for this sensor irradiated to a very high fluence of $1 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$.

The E_{eff} as a function of the fluence is shown in Figure 6.8b and no particular trend is observed.

The measured leakage current at -45°C is rescaled to that of -20°C using the E_{eff} obtained from fitting the IV curves of data set I taken at a bias voltages of 400 V and 800 V. The

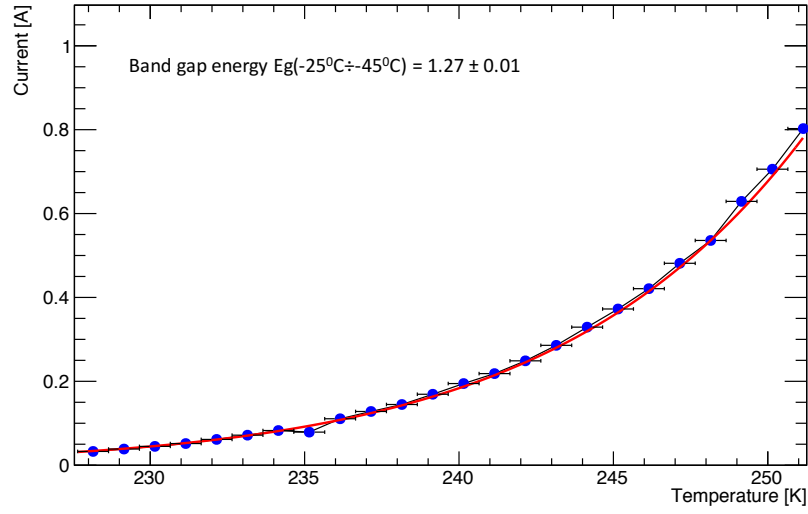


(a)

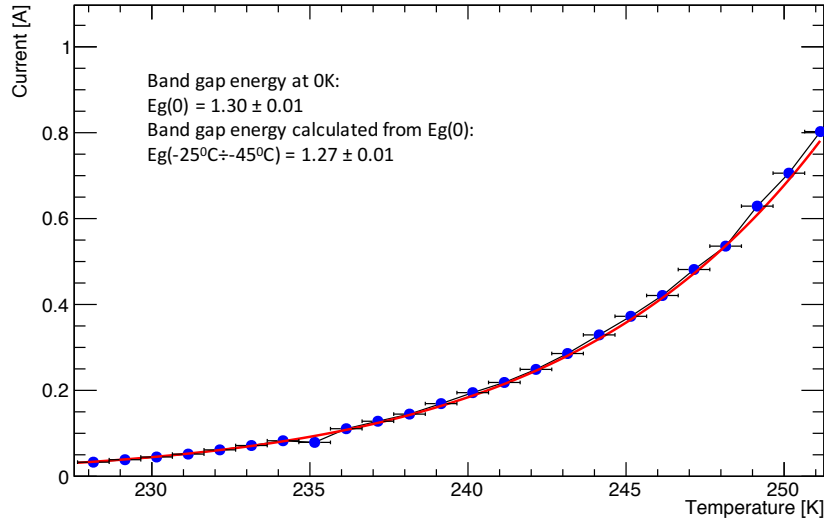


(b)

Figure 6.6: Measured leakage current as a function of the temperature at a bias voltage of 600 V to obtain E_{eff} for a sensor with $25 \times 100 \mu\text{m}^2$ pixel cells, $150 \mu\text{m}$ thickness and irradiated to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$. In (a) the $E_{\text{eff}}(T)$ at the average temperature of -32.5°C and (b) the $E_{\text{eff}}(0)$ is shown, as extracted by fitting the data obtained from IV measurements at different temperatures in the temperature range investigated. The rescaled value of $E_{\text{eff}}(T)$ is obtained with the Varshni equation starting from $E_{\text{eff}}(0)$ in the temperature range investigated.

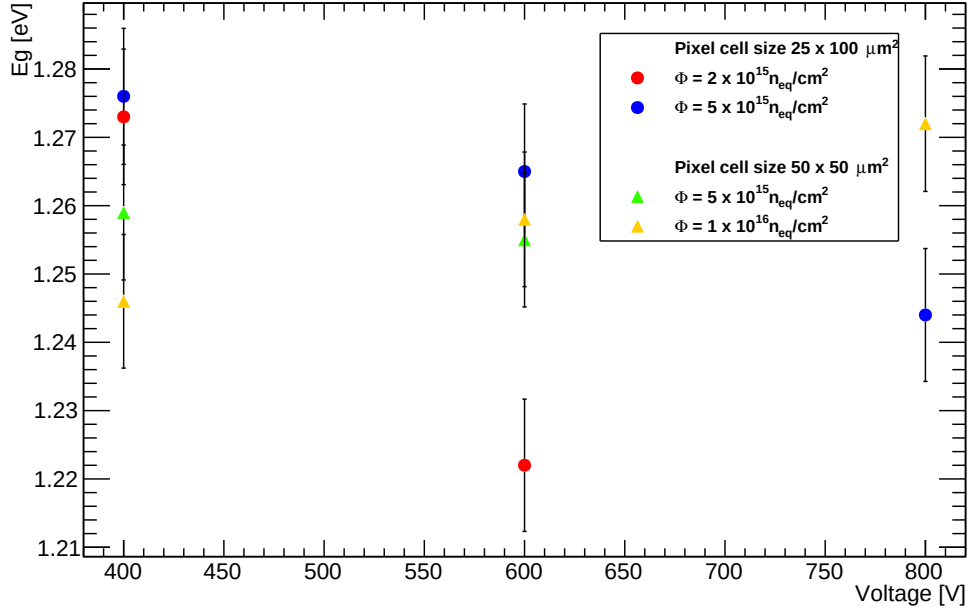


(a)

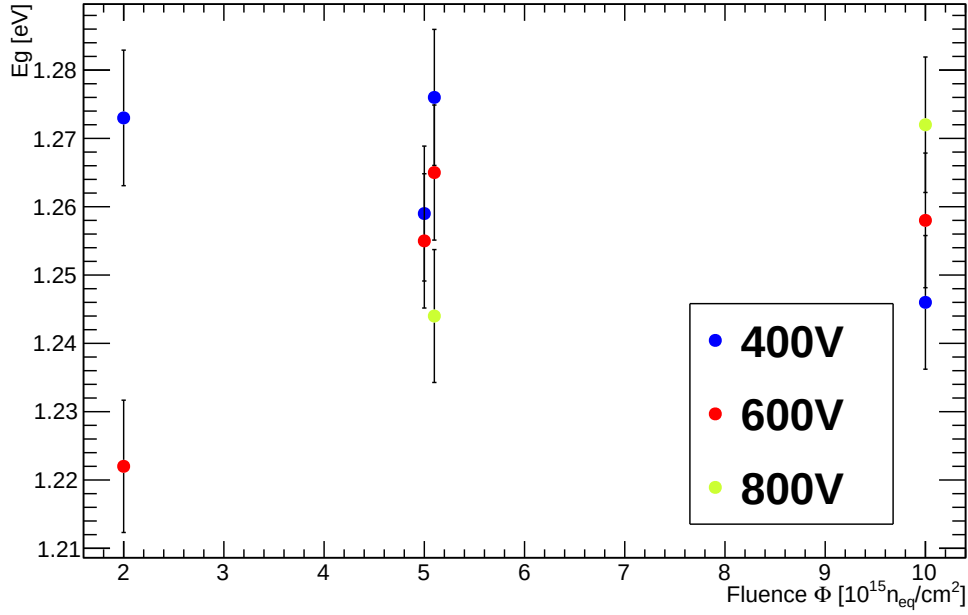


(b)

Figure 6.7: Measured leakage current as a function of the temperature at a constant bias voltage of 600 V to obtain E_{eff} directly from IT measurements for a sensor with $25 \times 100 \mu\text{m}^2$ pixel cells, $150 \mu\text{m}$ thickness and irradiated to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$. In (a) the $E_{\text{eff}}(T)$ at the average temperature of -32.5°C and (b) the $E_{\text{eff}}(0)$ is shown, as extracted by fitting the data obtained from measuring the leakage current for different temperatures. The rescaled value of $E_{\text{eff}}(T)$ is obtained with the Varshni equation starting from $E_{\text{eff}}(0)$ in the temperature range investigated.



(a) E_{eff} as a function of the bias voltage



(b) E_{eff} as a function of the fluence

Figure 6.8: Band gap energy from IT measurements (a) as a function of the bias voltage and (b) taken at constant voltages of 400 V, 600 V and 800 V as a function of the fluence (one of the sensors with $25 \times 100 \mu\text{m}^2$ pixel cells, $150 \mu\text{m}$ thickness and irradiated to a fluence of $5 \times 10^{15} n_{\text{eq}}/\text{cm}^2$ has been shifted by 0.1 on the x-axis for improved visibility).

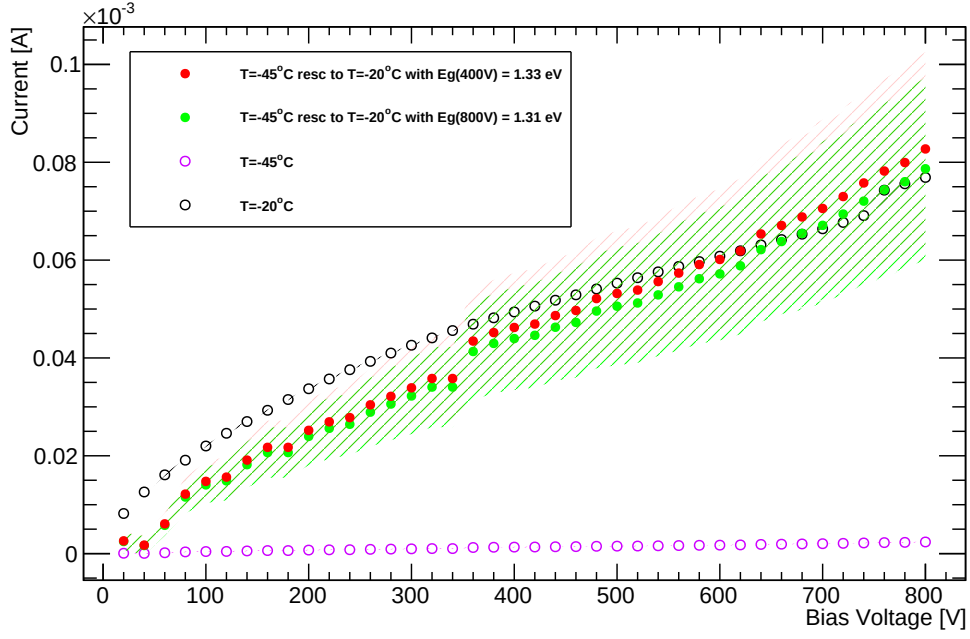
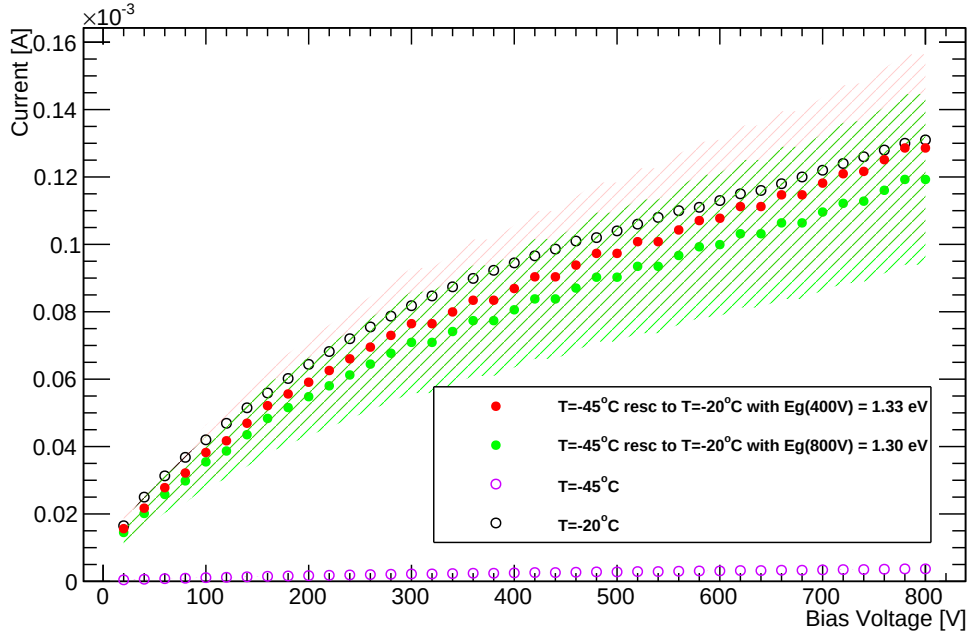
(a) Irradiated to a fluence of $2 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ (b) Irradiated to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$

Figure 6.9: Measured leakage current as a function of bias voltage for two different sensors with $25 \times 100 \mu\text{m}^2$ pixel cells, $150 \mu\text{m}$ thickness and irradiated to a fluence of (a) $2 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ and (b) $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ respectively. The measured leakage current at -45°C is rescaled to that of -20°C using the E_{eff} obtained from fitting the measurements belonging to data set I at voltages of 400 V and 800 V respectively.

results are shown in Figure 6.9. Both the sensors shown are with $25 \times 100 \mu\text{m}^2$ pixel cells, $150 \mu\text{m}$ thickness and irradiated to fluences of $2 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ and $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$. The rescaled IV curves provide a good approximation of the original IV curve within their uncertainties.

Table 6.3: Summary of the E_{eff} obtained from fitting the data from IV measurements at different temperatures and IT measurements for the four sensors at different bias voltages in the temperature range of interest from -45°C to -20°C .

Sensor type	Fluence [$10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$]	Band gap energy [eV]					
		Directly from IT			From IV at different T		
		E_g (400V)	E_g (600V)	E_g (800V)	E_g (400V)	E_g (600V)	E_g (800V)
W6_25 $\times$ 100	2	1.27 ± 0.01	1.22 ± 0.01		1.33 ± 0.05	1.32 ± 0.05	1.31 ± 0.05
W6_50 $\times$ 50	10	1.25 ± 0.01	1.26 ± 0.01	1.27 ± 0.01			
W7_25 $\times$ 100	5	1.28 ± 0.01	1.27 ± 0.01	1.24 ± 0.01	1.33 ± 0.05	1.31 ± 0.05	1.30 ± 0.05
W7_50 $\times$ 50	5	1.27 ± 0.01	1.26 ± 0.01				

The E_{eff} values obtained with both methods are higher than those reported in literature [42]. It has to be noted that these values are relative to an average temperature of -32°C , which is lower than temperature range of the measurements discussed in [42]. Other important differences are the values of the fluence, which is higher in the measurements described here, and the fact that in this thesis pixel sensors are investigated rather than diodes and strip sensors as in [42]. Furthermore in Ref. [42], high bias voltages were routinely excluded when the resulting E_{eff} was too high with respect to the lower bias range, to exclude the case of self-heating. On the other hand, a study of E_{eff} at high fluence and high bias voltages as reported in this thesis can be useful to determine the real effect of temperature scaling in a realistic scenario.

Conclusions

As discussed in Chapter 1, the inner detector (ITk) of the ATLAS experiment plays a fundamental role in the identification of charged particle and the reconstruction of their tracks. The pixel detector is the innermost part of the ITk. Due to the increase in peak luminosity from the LHC to the HL-LHC, the number of tracks per collision will also significantly increase. A novel module prototype with thin sensors and small pixel cell sizes, crucial to ensure low occupancy was designed. The pixel detector will be exposed to a maximum expected fluence of $1.4 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$ in its innermost layer. The characterisation of planar pixel sensors, compatible with the new read-out chip developed for ITk, is the focus of this thesis.

To avoid thermal runaway at high irradiation levels, the detector will be operated at temperatures well below 0°C . An accurate rescaling of the leakage current is essential to derive estimates of power dissipation and thermal performance. In this thesis an investigation of the effective band gap energy (E_{eff}), driving the temperature scaling, has been carried out.

Characterisation of the sensors with $50 \times 50 \mu\text{m}^2$ and $25 \times 100 \mu\text{m}^2$ pixel cells, compatible with the novel RD53A read-out chip, was performed by measuring the leakage current and the charge collection properties. Furthermore the threshold of the RD53A read-out chip has been calibrated using radioactive sources. The operational limit of the sensors is determined by the breakdown voltage. From the IV characterisation, it was shown that most of the sensors with thickness of $150 \mu\text{m}$ have a higher breakdown voltage than sensors with thickness of $100 \mu\text{m}$. The sensors implementing the metal over-hang design also shows a higher breakdown voltage in comparison to those, where the metal layer is not larger than the implant. Two designs with different edge regions were also compared and it was observed that the sensors with the standard edge region of $d_e = 450 \mu\text{m}$ have a higher breakdown voltage in comparison with those with smaller edge region of $d_e = 250 \mu\text{m}$. In general, the sensors with the smaller edge region displayed breakdown voltages that met with requirements for interconnection.

Sensors with and without biasing structures were also compared. For sensors without the biasing structure, a TiW metal layer was used to short the pixel cells at an intermediate step of the SOI4 wafer production. In this thesis, the IV characterisation was done for both types of sensors before removing the TiW layer, whereas, after the removal, it was again performed for the sensors with biasing structures. It was observed that the breakdown voltages of sensors with these structures is equivalent to that of sensors without these structures, thus implying that these latter sensors also display a good performance. It was

also observed that most of the sensors have a good IV characteristic after TiW removal, a fact indicating that performing the intermediate measurement does not represent a risk for the sensor performance. In general, the breakdown voltage obtained for sensors with the biasing structures during the intermediated step with TiW was higher than in those measured after its removal. This effect is attributed to the TiW layer resulting in a diode-like configuration with a lower electric field.

The leakage current as a function of the bias voltage was also measured at diced-sensor and module levels. The breakdown voltage is reduced after dicing as the electrical field at the sensor edges increases because of the dicing process. At module level, the breakdown voltage is even lower. Therefore it is important that the sensor display a very high breakdown voltage at wafer level, so that a high enough breakdown voltage is ensured at module level.

The charge collection measurements were performed using unirradiated modules implementing the RD53A read-out chip by exposition with a ^{90}Sr source. It was observed that the charge collection saturates at low voltages ranging from 5 V to 20 V, due to the high bulk resistivity of the sensors.

In the last part of sensor characterisation, an independent threshold study of the RD53A read-out chip was conducted for unirradiated modules using ^{55}Fe and ^{109}Cd sources. It was shown that the calibrated threshold of the RD53A read-out chip coincides well with the nominal tuned threshold, determined by the global threshold parameter.

The extraction of E_{eff} for irradiated sensors has been performed. Two types of measurements were conducted using four sensors irradiated to various fluences. One set of measurements utilises IV curves taken at different temperatures. The other set of measurements is based on measurements of the leakage current at a fixed bias voltage, while varying the temperature. The measured temperature range is from -20°C to -45°C . One sensor was irradiated to $2 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$, two were irradiated to $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ and one was irradiated to $1 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$. These experimental conditions are closer to the real operational conditions at the end of the lifetime of the HL-LHC pixel detectors. The observed E_{eff} ranges from $1.22 \pm 0.01 \text{ eV}$ to $1.33 \pm 0.05 \text{ eV}$. While the E_{eff} reported in the literature (see Ref. [42]) for irradiated silicon microstrip sensors is $1.211 \pm 0.008 \text{ eV}$ and the measurements described to obtain the reported E_{eff} value were not aimed at the investigation of $I(T)$ dependence and consequently were not optimised for this purpose. Therefore, the results of these two studies cannot be directly compared as, in this thesis, the temperature range, irradiation fluences and bias voltages differ from those described in [42].

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“For all that has been – thanks. For all that shall be – yes.”

-Dag Hammarskjöld

List of Figures

1.1	This diagram shows the locations of the four main experiments (ALICE, ATLAS, CMS and LHCb) that are installed at the LHC.	1
1.2	The LHC accelerator and injection complex	4
1.3	Cross-section of the ATLAS experiment	5
1.4	Schematic representation of the ATLAS detector detecting particles and a cross-section of the present ID	5
1.5	The LHC schedule toward HL-LHC	7
1.6	Schematic representation of one quadrant of the ITk system at the HL- LHC	8
2.1	Band structures.	10
2.2	Band structures.	12
2.3	Stopping power for positive muons in copper as a function of momentum. .	14
2.4	Most probable energy loss in silicon for 500 MeV pions.	15
3.1	Schematic representation of processing of pixel sensors	19
3.2	Schematic representation of the guard rings and biasing structures	21
3.3	Schematic representation of the different sensor structures of the SOI4 wafer production	23
3.4	Schematic representation of the three different analogue circuitry implemented in a RD53A read-out chip.	25
3.5	Schematic representation of a cross-section of a module wire bonded to a PCB and a module with certain dedicated structures indicated.	27
4.1	Experimental set-up of IV characterisation	28
4.2	Schematics of the experimental set-up for charge collection measurements .	30
4.3	Schematics of the laboratory set-up for RD53A module characterisation. .	32
4.4	BDAQ53 board	32
4.5	Analogue test results of an unirradiated module.	33
4.6	Relation between threshold and time over threshold (ToT)	34
4.7	Typical threshold measurement	35
4.8	S-curve and the fitted threshold distribution	36
5.1	Schematic representation of the dimensions of the pixel cell implant showing the inter-implant distances for the different pixel cell sizes where (a) is $50 \times 50 \mu\text{m}^2$, (b) $25 \times 100 \mu\text{m}^2$ and (c) $50 \times 250 \mu\text{m}^2$	39

5.2	Measured leakage current as a function of bias voltage for some selected sensors embedded into two exemplary wafers of (a) 100 μm and (b) 150 μm thickness.	40
5.3	Comparison of the IV curves at diced-sensor level of sensors of 100 μm and 150 μm thicknesses for $25 \times 100 \mu\text{m}^2$ and $50 \times 50 \mu\text{m}^2$ pixel cells with a grounded bias ring.	41
5.4	Comparison of measured leakage current as a function of bias voltage between selected sensors at wafer level and after dicing for wafer 8 of 150 μm thickness.	42
5.5	Comparison of IV curves between different edge distances for sensors with $50 \times 50 \mu\text{m}^2$ pixel cells for wafers with thicknesses of 100 μm (wafer 3) and 150 μm (wafer 6).	43
5.6	Measured leakage current as a function of bias voltage for sensors embedded into two different wafers of 150 μm thickness, before and after removing the coating with a TiW layer for the sensors with punch through structures.	44
5.7	IV curves of sensors without punch through structures and comparison of the IV curves between structures of same geometry for sensors with punch through and without punch through structures before the removal of TiW layer.	46
5.8	Comparison of measured leakage current as a function of bias voltage for sensors embedded into two different wafers of 150 μm thickness after singularisation for the sensors after TiW removal.	47
5.9	Comparison of IV curves at a set temperature of -25°C irradiated at different fluences of $5 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ and $1 \times 10^{16} \text{ n}_{\text{eq}}\text{cm}^{-2}$	48
5.10	Measured leakage current as a function of bias voltage for sensors at diced-sensor level and at module level of 100 μm and 150 μm thickness. Here, W2, W3 and W8 denotes the wafer number of the SOI4 production.	48
5.11	ToT distribution together with a fit to a convolution of a Landau and a Gaussian function.	50
5.12	Comparing the collected charge of two modules as a function of the Bias Voltage.	51
5.13	For a module of 100 μm thickness using the linear front-end the most probable value of the ToT as a function of bias voltage.	52
5.14	The most probable ToT as a function of the bias voltage of a module with a sensor of 100 μm thickness using the linear front-end tuned to a threshold of 1700 e or 1500 e respectively.	53
5.15	Calibration of the threshold for two $50 \times 50 \mu\text{m}^2$ modules of 100 μm and 150 μm thicknesses without punch through structures.	55
5.16	The cluster size as a function of the set global threshold parameter for a module with a sensor of 150 μm thickness, $50 \times 50 \mu\text{m}^2$ pixel cells and without punch through structures for source scans with the ^{55}Fe source.	56
6.1	Measured leakage current as a function of bias voltage for irradiated sensors for different temperatures.	58

6.2	Effect of systematic shifts in temperature on effective band gap energy in the initial round of measurement.	59
6.3	Process of calibrating the temperature of the thermal chuck of probe station.	60
6.4	Process of calibrating the temperature of the thermal chuck of probe station.	61
6.5	Dependence of band gap energy on temperature using Varshni equation over the (a) whole range and (b) measured range of temperature.	62
6.6	Measured leakage current as a function of the temperature at a bias voltage of 600 V to obtain E_g from IV measurements at different temperatures.	64
6.7	Measured leakage current as a function of the temperature at a constant bias voltage of 600 V to obtain E_{eff} directly from IT measurements.	65
6.8	Band gap energy from IT measurements as a function of (a) the bias voltage and (b) the fluence.	66
6.9	The measured leakage current at -45°C is rescaled to that of -20°C using the band gap energy obtained from fitting the IT measurements at constant voltages of 400 V and 800 V respectively.	67

List of Tables

3.1	The types of SOI4 sensors studied in this thesis.	25
5.1	Summary of the observed threshold for the two modules using the different radioactive sources and front-ends.	57
6.1	Summary of the types of sensors measured along with their irradiation fluence.	59
6.2	Table displaying the effect of systematic shifts in temperature on E_{eff}	60
6.3	Summary of the E_{eff} obtained from fitting the data from IV measurements at different temperatures and IT measurements.	68

Abbreviations and acronyms

ATLAS	A Toroidal LHC Apparatus
ALICE	A Large Ion Collider Experiment
BCB	Benzocyclobutene
BR	Bias ring
CERN	European Organization for Nuclear Research
CMOS	Complementary Metal–Oxide–Semiconductor
CMP	Chemical mechanical polishing
CMS	Compact Muon Solenoid
CSC	Cathode Strip Chamber
DAC	Digital to analog converter
DFE	Differential Front-end
DESY	Deutsches Elektronen-Synchrotron
DUT	Device under test
ECAL	Electromagnetic Calorimeter
EoC	End of chip
FE	Front-end
FZ	Float zone
FPGA	Field programmable gate array
GR	Guard ring
HCAL	Hadronic Calorimeter
HLL	Halbleiter Labor
IC	Integrated circuit
ID	Inner Detector
ILC	International linear collider
JSI	Jozef Stefan Institute
KIT	Karlsruher Institut für Technologie
LFE	Linear Front-end
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LS	Long Shutdown

MDT	Monitored Drift Tube
MPP	Max-Planck-Institut für Physik
MPV	Most probable value
MPW	Multi-project wafer
MS	Muon Spectrometer
PCB	Printed-circuit board
PDR	Pixel digital region
PPS	Planar pixel sensor
RMS	Root mean square
RoI	Region of interest
RPC	Resistive Plate Chamber
SCC	Single chip card
SCR	Space charge region
SFE	Synchronous Front-end
SOI	Silicon on Insulator
SPS	Super Proton Synchrotron
TGC	Thin Gap Chambers
TLU	Trigger logic unit
ToT	Time over threshold
UBM	Under bump metallization
USB	Universal serial bus

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Erklärung:

Hiermit erkläre ich, die vorliegende Arbeit selbständig verfasst zu haben und keine anderen als die in der Arbeit angegebenen Quellen und Hilfsmittel benutzt zu haben.

München, 10.12.2018