

MASTER THESIS

Quality control for service hybrid test cards and thermal long term tests of electronics components for the CMS Phase-2 tracker upgrade

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I. Motivation

One of the most successful achievements of modern physics is the development of the Standard Model (SM) of particle physics. This comprehensive theory describes the fundamental particles of the universe and their interactions. The model has been experimentally confirmed with high precision. Most of the fundamental particles were discovered with particle accelerators during the last 70 years. These experiments can generate heavy standard-model particles through high-energy collisions, necessitating the use of sophisticated particle detectors for the measurement of these particles and their properties.

The largest and most powerful particle accelerator today is the Large Hadron Collider (LHC) [1] based at the European Organization for Nuclear Research (CERN) near Geneva, Switzerland. It accelerates protons and collides them with a center-of-mass energy, $\sqrt{s}$, of 13.6 TeV. Positioned at the four interaction points within the LHC are large particle detectors, each composed of various sub-detectors designed to fulfill distinct functions. One of these detectors is the multi-purpose CMS (Compact Muon Solenoid) detector [2]. The greatest success of CMS was the discovery of the Higgs boson in 2012 [3].

Even if the Standard Model is a very precise theory, there remain some unanswered questions in modern physics. Theoretical models beyond the Standard Model (BSM) endeavor to address these questions, often predicting effects in particle interactions, including the possible existence of undiscovered particles. To study high-energy physics with increased statistical power, the LHC is going to be upgraded to the so-called High Luminosity LHC (HL-LHC) [4]. This also affects the CMS experiment, and different sub-detectors will be enhanced during the so-called Phase-2 upgrade [5]. It includes a full replacement of the old tracker system [6], and this thesis deals with components of the new Outer Tracker (OT). The OT comprises two distinct silicon detection modules, the so-called 2S and PS modules. The 2S modules are constructed with two silicon strip sensors, enabling the measurement of particle momentum as the particles traverse the tracker. A detailed summary of the LHC, the CMS experiment, the 2S module, and the HL-LHC upgrade is given in Chapter II.

The modules feature various printed circuit boards (PCBs) for data readout, known as hybrids. The service hybrid (SEH) is crucial for the power supply on the module and the distribution of collected data to the trigger system of the detector. In the CMS detector, the OT is not easily accessible, necessitating comprehensive quality control for all its components. To assess the SEH's functionality, a specialized test card PCB has been developed at the Physics Institute IB of RWTH Aachen University (Aachen-1B), designed to measure and verify all critical SEH properties. Chapter III provides a detailed description of the test card. Ninety test cards were manufactured and delivered. The primary focus of this thesis centers on the quality control (QC) procedure for these test cards. A two-stage quality control process is conducted. First, the functionality of all the test cards is tested at room temperature, as detailed in Chapter IV. To ensure the comparability of test card results, a single SEH is employed as a reference. During the second stage, the test cards undergo thermal cycles within a climatic chamber, and tests at different ambient temperatures are conducted, as outlined in Chapter V. Various issues concerning the test routine were observed, and the procedure was improved. In addition, the power distribution from the SEH to the other module components is analyzed. Voltage drops on the hybrids are measured and presented in Chapter VI. In Chapter VII the climatic chamber setup is used to test the performance of a module at different temperature conditions. The main focus is on the performance of the SEH within a module.

In the framework of this thesis, the development of a quality control procedure for the service hybrid test cards is undertaken, and high-quality test cards are identified for subsequent SEH testing. Additionally, various other aspects of hybrids within 2S modules in different environmental and temperature conditions are examined, and a deeper understanding is gained.

II. Introduction

II.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is the world's largest particle accelerator, providing particles with the highest center-of-mass energies [1]. It is located near Geneva on the French-Swiss border and is operated by the European Organization for Nuclear Research, CERN [7]. The Compact Muon Solenoid (CMS) experiment is one of the four large experiments at the LHC. The concept behind these particle accelerators is to propel particles in two opposing beams to speeds approaching the velocity of light, and then collide them at precisely defined interaction points. The center-of-mass energy at these interaction points is then used to create many new high-energetic particles. The LHC collides protons (p) with a center-of-mass energy of $\sqrt{s} = 13.6$ TeV. This energy corresponds to the particle energies of the universe approximately 10^{-10} s after the big bang, which gives physicists the possibility to gain a better understanding of the creation and development of the early universe. In addition to protons, it is also possible to accelerate heavy ions at the LHC like lead ions (Pb). Therefore, pp-, PbPb- and pPb-collisions are possible [1]. Proton-proton collisions are the most important mode for the CMS experiment, and therefore the following description will focus on this mode.

To accelerate particles to high energies, multiple preaccelerators are necessary. In each step of the preaccelerator chain, the beam energy is successively increased. A sketch of the accelerator complex is shown in Figure II.1. It was possible to modify and reuse some of the existing accelerator infrastructure at CERN, consisting of accelerators for older experiments. The whole preaccelerator system was upgraded at the last shutdown of the LHC, the so-called Long Shutdown 2 from 2019 to 2022. At the beginning of the whole accelerator chain, there is a bottle of liquid hydrogen. By ionization, negative hydrogen ions can be accelerated by Linac4. Linac4 is a linear accelerator, bringing the ions to energies of 160 MeV [8]. Before injecting the ions into the next preaccelerator, the electrons are removed from the H^- ions to get protons. After that, they are injected into the Proton Synchrotron Booster (PSB) and then into the Proton Synchrotron (PS) with proton energies of 2 GeV and 25 GeV, respectively. The last preaccelerator is the Super Proton Synchrotron (SPS). After that, protons are injected into the LHC ring with an energy of 450 GeV. These accelerators were upgraded to meet the special needs of the LHC. In particular, the high number of proton bunches (2808 per LHC ring) with a time spacing of 25 ns between the bunches was challenging. The LHC itself is located in the old tunnel of the Large Electron-Positron Collider (LEP), built to accelerate and collide electrons and positrons. The tunnel has a total length of 26.7 km and has eight straight sections and eight arcs [1]. It lies approximately 100 m below the surface on a plane inclined at 1.4% sloping. The limitation factor of the reachable beam energy is the magnetic field strength of 8 T, used to bend and focus the particles into the designated trajectory. For this, superconducting magnets are used. To reach superconductivity, these magnets are cooled to their operation temperature of 1.9 K. At the four interaction points of the LHC, the large experiments ALICE [9], LHCb [10], ATLAS [11] and CMS [2] are located. The operation of the LHC is divided into different phases. In the different runs, the LHC is under operation, and data are collected. The runs are interspersed by Long Shutdowns (LS). They are used to upgrade the accelerator and the experiments for better performance during the runs. At the moment, LHC is in operation of Run 3 until the end of 2025 [12]. The next shutdown (LS3) will be used to increase the instantaneous luminosity of the accelerator to increase the data rate by getting more collisions at the interaction points. This has major consequences for the accelerator and the experiments, which will be discussed in Section II.3. This thesis deals with new parts for the CMS detector for the upgrades in LS3, planned to be completed in January 2029.

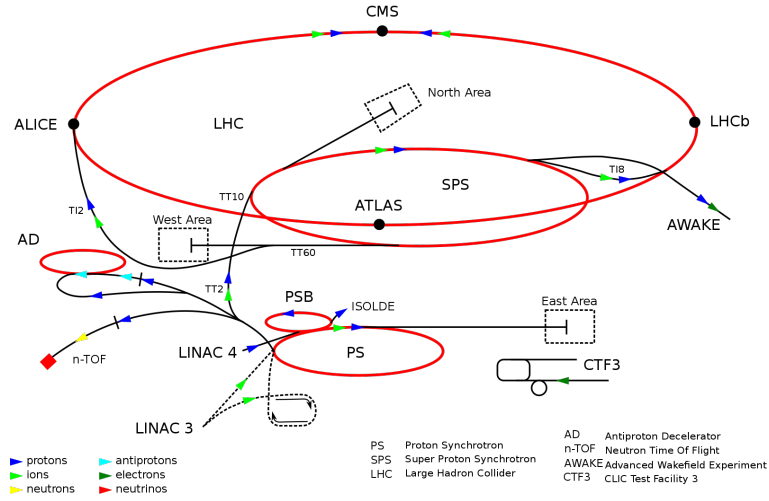


Figure II.1: Sketch of the preaccelerator complex of the LHC. Green and blue arrows represent the direction of flight for protons and ions. Also the four large experiments ALICE, ATLAS, LHCb and CMS are shown in the figure [13].

II.2 The CMS Detector

A schematic drawing of the CMS detector is shown in Figure II.2. It is installed at LHC point 5, close to the French village of Cessy [2]. CMS is a multi-purpose detector built to detect many kinds of different particles. The main properties of the detector are already given in its name:

- **Compact:** with a cylindrical shape with a diameter of 15 m and a length of 28.7 m it is with a weight of 14 000 t very compact.
- **Muon:** the CMS detector offers the possibility of detection of muon tracks with excellent efficiency and P_T -resolution.
- **Solenoid:** one of the most important parts of the detector is a solenoid magnet that generates a magnetic field of 3.8 T which bends charged particles on a curved path.

The purpose of this kind of detector is to give the possibility to analyze initially created heavy particles and their interactions by measuring all the decay particles produced. This implies a measurement of the energy and momentum of around 1000 charged particles emerging from the interaction region every 25 ns for an instantaneous luminosity of $2 \times 10^{-34} \text{ cm}^{-2} \text{ s}^{-1}$ [14]. The total integrated luminosity recorded by CMS until today is 245.54 fb^{-1} [14]. To detect most of the produced particles, a geometry near a 4π coverage is necessary. To understand the geometry of the detector, the right-handed coordinate system used by CMS will be introduced. The center of the coordinate system is the interaction point. The z -axis points counterclockwise along the beam pipe, the x -axis points in the direction of the center of the LHC, and the y -axis points upwards. In spherical coordinates, the azimuthal angle ϕ is measured from the x -axis in the x - y plane. Instead of the polar angle θ , the so-called pseudo-rapidity η is used. Here, θ is the angle between the beam axis and a particle track. The pseudo-rapidity is then defined as

$$\eta = -\ln \left(\tan \frac{\theta}{2} \right). \quad (\text{II.1})$$

The whole detector has a cylindrical shape consisting of barrel parts in the middle and endcap discs at its ends. Different sub-detectors are mounted in layers around the beam pipe. Each sub-detector fulfills a certain task in detecting and characterizing the produced particles. In the following, each sub-detector will be explained going from the inside to the outside.

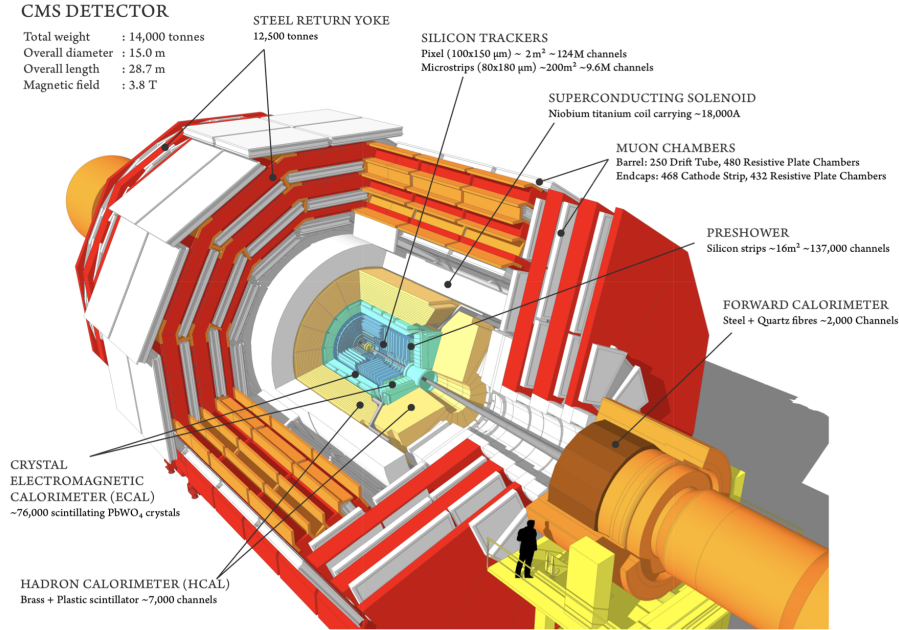


Figure II.2: Schematic drawing of the CMS detector [15].

Silicon Pixel Detector The pixel detector is the innermost part of the detector. It is used to measure the trajectories of charged particles. Its first layer is placed as close as possible to the beam pipe, so radiation hardness is one of the key challenges for this detector part. Additionally, the readout bandwidth must be sufficiently high for the bunch crossing frequency, and the pixel detector has a small material budget to reduce secondary interactions of particles in the inner part of the detector. The pixel detector is used to localize the interaction point by interpolating the reconstructed trajectories towards the interaction region. This is necessary to sort the produced particles to the point they originate from. Also, it is interesting to detect tracks of particles decaying within a few centimeters and their secondary vertices with high precision. Therefore, excellent spatial resolution is necessary, which is fulfilled with a silicon pixel detector. At the Phase-1 Upgrade, the whole pixel detector was replaced by a four-layer detector to have four-hit coverage over the pseudorapidity range $|\eta| < 2.5$ [16]. The innermost layer has a distance of 29 mm to the beam pipe while the outermost layer has a distance of 160 mm. The pixel detector is built from 1856 segmented silicon sensor modules. The main part of each module is a silicon sensor with pixels bump-bonded to the readout chips (ROCs). The pixel size is $100 \times 150 \mu\text{m}^2$.

Silicon Strip Detector The current strip detector occupies the radial region between 20 cm and 116 cm. It is composed of four different subsystems, the Tracker Inner Barrel (TIB), the Tracker Inner Disc (TID), the Tracker Outer Barrel (TOB), and the Tracker EndCaps (TEC). Each subsystem is mounted at a different location in the tracker and contains various module types with different geometries and strip sizes. In total, 15148 silicon sensors with 9.3 million strips are used in the strip tracker, making up a total active area of 198 m^2 [2]. The strips in the barrel are oriented parallel to the beam pipe to make a measurement of the transversal momentum possible.

Electromagnetic calorimeter (ECAL) In the calorimeters, the energy of incoming particles is measured. The main requirements of the electromagnetic calorimeter at CMS are excellent energy resolution, high granularity, radiation hardness and a high readout speed. In the ECAL mainly electrons and photons deposit their whole energy, so they are absorbed completely. To fulfill the requirements, a homogeneous calorimeter made of lead tungstate (PbWO_4) crystals is used. They generate scintillation light when particles pass through them, and the number of produced photons is proportional to the deposited energy. A total of 61200 crystals are mounted

in the central barrel part and 7324 in each of the two endcaps [2]. The crystals have a high density (8.28 g/cm^3) and a short radiation length (0.89 cm). About 80% of the scintillation light is emitted within 25 ns, so the scintillation decay time is the same order of magnitude as the LHC bunch crossing time. Photodetectors mounted on the crystals detect the emitted light. Avalanche photodiodes (APDs) are used as photodetectors in the barrel. In the endcaps vacuum phototriodes (VPTs) are used. The energy resolution of the ECAL was found to be

$$\left(\frac{\sigma}{E}\right)^2 = \left(\frac{2.8\%}{\sqrt{E}}\right)^2 + \left(\frac{0.12}{E}\right)^2 + (0.30\%)^2. \quad (\text{II.2})$$

With the good energy resolution [2], it was possible to detect the decay of a Higgs boson into two photons, which was a great success of CMS.

Hadronic calorimeter (HCAL) Most of the hadrons are able to pass the electromagnetic calorimeter and are stopped in the hadronic calorimeter. Hadrons collide inelastically with the nuclei, producing showers of secondary particles. The interaction length λ is 16.42 cm [2]. In CMS, in radial direction, the HCAL begins at the outer extent of the ECAL ($R = 1.77 \text{ m}$) and reaches out to the beginning of the magnetic coil ($R = 2.95 \text{ m}$). Additionally, an outer hadron calorimeter, or *tail catcher*, is placed outside the solenoid. The combined energy resolution of ECAL and HCAL is

$$\left(\frac{\sigma}{E}\right)^2 = \left(\frac{84.7\%}{\sqrt{E}}\right)^2 + (4.4\%)^2, \quad (\text{II.3})$$

and therefore it is worse compared to the energy resolution of the ECAL alone [17].

Solenoid A large solenoid is used to provide a strong magnetic field inside the detector. In this field, charged particles are bent into curved trajectories. The curvature of the trajectories depends on the strength of the magnetic field and the particle momentum. Therefore, the measurement of the curvature provides a method to measure the particle momentum. Depending on the direction in which the particle is bent, its charge can be inferred. The magnetic field in the inner part of the detector has a strength of 3.8 T and the solenoid has a 6 m diameter and a 12.5 m total length [2]. The heavy weight of more than $10\,000 \text{ t}$ is caused by the iron yoke used to return the magnetic flux. This yoke is composed of three layers in the barrel and the endcaps with varying thickness and is enclosing the muon chambers. The winding of the solenoid is made of a stabilized NbTi superconductor to enable the required currents. In total, there is an energy of 2.6 GJ stored in the solenoid at full current [2].

Muon chambers In many models, muons provide a clean signature for new physics, making their identification and momentum measurement with great precision indispensable for the CMS detector's functionality. Muons are not stopped in the calorimeters, so the muon system is the outermost part of the detector. The different sub-detectors of the muon system are alternating with the iron return yoke for the magnetic field. This has the consequence that remaining hadrons are filtered in the iron parts before reaching muon detectors, and the magnetic field points in the opposite direction compared to the detector part inside the solenoid. That is why the muon tracks are bent in the opposite direction. The muon system itself consists of four different types of subdetectors. Drift tubes are used in the barrel part; in the endcaps cathode strip chambers are used, while resistive plate chambers are used as trigger detectors in both parts. Gas electron multipliers (GEMs) are used in the forward regions close to the beampipe. Because of the large surface area of $25\,000 \text{ m}^2$ the muon system has to cover, inexpensive gaseous detectors are used [2]. The muon system plays a crucial role in the trigger of the CMS detector readout.

Trigger system As described in Section II.1 the collision rate and also the readout rate of the detector measurement is 40 MHz . Even with modern computing technologies, the readout of the whole detector at this rate is not possible. Therefore, a trigger is necessary to filter interesting events already at the back-end of the detector. The CMS trigger system consists of

two stages. The Level-1 trigger combines signals from the calorimeters and the muon system. The combined total trigger rate is 100 kHz [2]. It consists of custom-designed electronics to make it fast enough. From these trigger events, the high-level trigger (HLT) selects events also based on tracker information. The HLT is a software-based system using a large filter farm. It features an output rate of about 1 kHz. The selected events are then stored for offline analysis all around the world.

II.3 The HL-LHC upgrade

The goal of the next long shutdown (LS3) of the LHC, beginning at the end of 2025 [12], is to further increase the instantaneous luminosity. It describes the number of particle interactions per time and cross-section and is measured in units of $\text{cm}^{-2}\text{s}^{-1}$. The actual luminosity in Run 3 is more than $2 \times 10^{-34} \text{ cm}^{-2}\text{s}^{-1}$ [14], which is already twice as high as originally planned [6]. For the HL-LHC, the instantaneous luminosity should be increased to $5 - 7.5 \times 10^{-34} \text{ cm}^{-2}\text{s}^{-1}$. This will be achieved by a variety of methods. Most importantly, the focusing magnets will be replaced to lower the beam beta function in the collision region. Also, a number of new corrector magnets and separation dipoles will need to be installed. The higher luminosity has an impact on the CMS experiment in two different ways. Especially the inner parts of the detector, like the pixel detector or the tracker, are exposed to higher levels of radiation. The expected ionizing dose for the innermost parts of the detector is up to 12 MGy for an integrated luminosity of 3000 fb^{-1} [6]. This places special demands on the radiation hardness of the detector elements, such as the Outer Tracker silicon modules. The second impact to the CMS experiment is the higher particle rate to deal with. To profit from the higher luminosity interesting events shall be selected from all the detected hits. This is done primarily by improving the trigger system due to the use of data from the tracker. The trigger rate is enhanced to 750 kHz [6]. From the outside to the inside of the detector, the following upgrades are planned:

In the muon system, some parts of the front-end electronics for the Drift Tubes will be replaced to improve radiation tolerance, and the trigger latency of other electronics components will be adapted [5]. For the HCAL in the barrel region, the front-end electronics will also be upgraded. The endcaps of the HCAL and ECAL will be replaced by a new high granularity calorimeter (HGCAL) [4], based on silicon sensors and scintillating tiles. During the LS3, the whole tracker will be replaced by the so-called Phase-2 tracker upgrade. The new tracker design is separated into the Inner Tracker (IT) and the Outer Tracker (OT). The layout is shown in Figure II.3. The Inner Tracker is equipped with different types of pixel modules. The Outer Tracker consists of PS modules, combining macro-pixel and strip sensors, and 2S modules. The 2S modules are made of two silicon strip sensors and are described in more detail in Section II.4. The design with two parallel sensors provides the possibility to gain information about the particle momentum on each module and therefore can provide data for the Level-1 trigger (see Section II.4.2). The components of the tracker are mounted in cylindrical barrels in the middle part of the detector. The inner part of the barrel is the Tracker Barrel with PS modules (TBPS), the outer part is composed of 2S modules, the Tracker Barrel with 2S modules (TB2S). Some of the PS modules in the barrel are mounted on tilted rings to reduce the material budget traversed by particle tracks. Towards the outer parts of the detector along the beampipe the modules are mounted on discs named Tracker Endcap Double-Discs (TEDD). They consist of PS and 2S modules. The modules are overlapping in the detector, so the particles must pass through the sensor of at least one module per layer. The Outer Tracker consists of six layers surrounding the beam pipe to provide a good measurement of the particle momentum. In total, 7680 2S modules are needed for the OT [6] and around 1000 of them will be built by the physics institutes at RWTH Aachen University. Therefore, the whole infrastructure necessary for a module production center is installed there. The serial production of modules will start in 2024. The upgrade of the detector hardware is planned to take place during LS3, therefore, during the production period, everything has to run smoothly so that there are no major delays. All the modules built by the institutes in Aachen will be integrated into endcap discs at DESY in Hamburg.

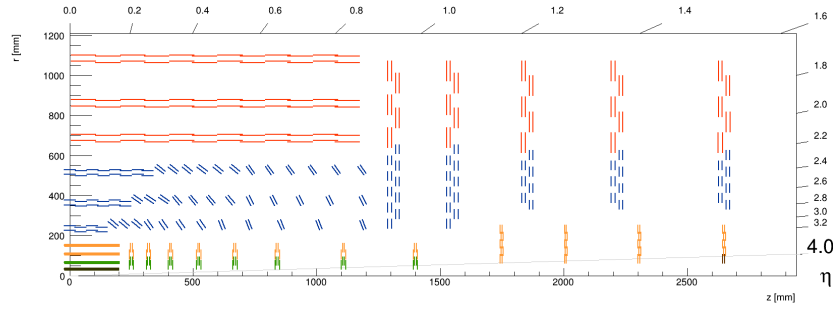


Figure II.3: Layout of one quarter of the CMS tracker in r - z view. In yellow and green the different types of pixel modules are shown. Blue are the PS modules and the outer part in red are the 2S modules. The interaction point is at $r = z = 0$ [18].

II.4 The 2S Module

II.4.1 The silicon strip sensors

The main parts of the 2S module are the two silicon strip sensors. They are both separated into two rows of strips with the size $5\text{ cm} \times 10\text{ cm}$. Therefore, one sensor has the dimension of $10\text{ cm} \times 10\text{ cm}$ with a thickness of $320\text{ }\mu\text{m}$. The sensors are made of p-doped silicon. On this bulk of silicon are n-doped strips with a width of $22.5\text{ }\mu\text{m}$. Each sensor has 2032 strips. The distance between two strips (pitch) is $90\text{ }\mu\text{m}$ [6]. The last layer of each strip is made of aluminium for electrical connections.

Between the raw silicon and the n-doped strips, a depletion zone without free charge carriers is formed. The principle works like a semiconductor diode operated in reverse-biased mode. A sketch of a strip sensor is shown in Figure II.4. The individual strips are electrically isolated by a layer of silicon dioxide (SiO_2). By applying voltage, the depletion zone increases. In the CMS detector, the applied voltage will be between 300 V and 800 V, depending on the accumulated dose. If a particle goes through the depletion zone or a photon is absorbed in this region, it creates electron-hole pairs. The produced electrons are drifting to the strips and generating a signal. So it is possible to localize the strip near which a particle passes the sensor.

II.4.2 The p_T module concept

Interesting events are often characterized by tracks with a high transverse momentum (p_T), so a basic momentum measurement technique is included in a special module design. The so-called p_T -module concept provides the opportunity for the Outer Tracker to contribute to the Level-1 trigger. To reduce the amount of data sent from the module to the trigger at a rate of 40 MHz, a first filter mechanism is already included at module level. As explained in Section II.2 charged particle tracks are bent by the magnetic field inside the detector. To measure the particle momentum with the module, two stacked silicon strip sensors are mounted in parallel above each other with a distance of 1.8 mm or 4 mm. If a particle hits the first sensor, it creates a signal in one or a few neighboring strips. Then, the front-end chips on the module calculate an acceptance window on the second sensor where the particle is expected (Figure II.5). Low-momentum particles are bent so much by the magnetic field that they miss the acceptance window on the second sensor. Only particle tracks that are also detected in the acceptance window are used for the Level-1 trigger. This kind of recorded signal is called a "stub". The size of the acceptance window is programmable to a certain p_T threshold of the particle. A threshold of 2 GeV corresponds to a reduction of the transmitted data volume of roughly one order of magnitude [6]. A total of five out of the six electrical links (E-links) to send data to the back-end of the detector are used for trigger information. Only one E-link is required to send full readout data when requested by the back-end [6]. This happens with a latency of about $12.5\text{ }\mu\text{s}$, so the data is buffered by the front-end chips.

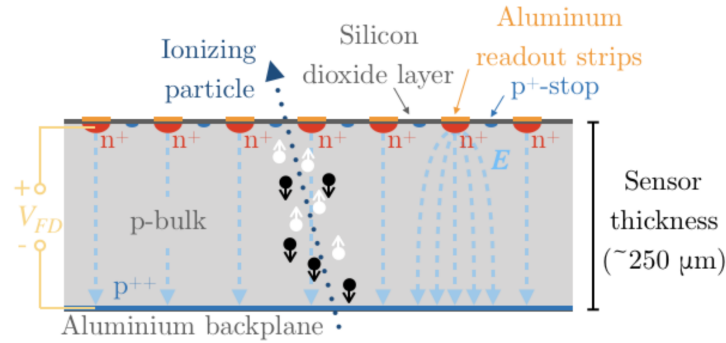


Figure II.4: Basic principle of a silicon strip sensor. Electrons are shown in white, and the produced holes are presented in black [19].

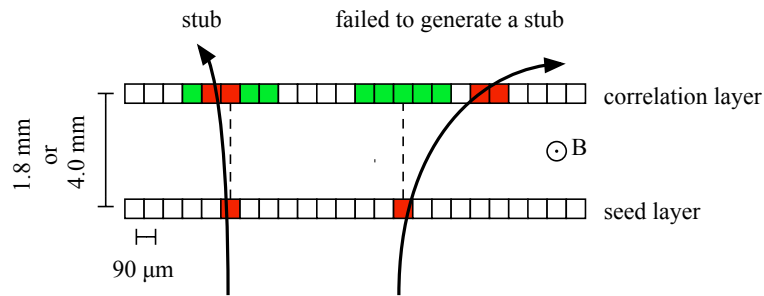


Figure II.5: Illustration of the p_T concept. Particles hitting the green acceptance window pass the momentum filter and create a stub [20].

II.4.3 2S module design

As described in Section II.4.2 the main parts of the module are two $10\text{ cm} \times 10\text{ cm}$ silicon strip sensors. A sketch of the module is presented in Figure II.6. The two sensors are glued to Aluminium Carbon Fibre (AlCF) spacers called bridges to ensure the correct gap between the sensors. Mechanically and electrically connected to the sensors are the front-end hybrids (FEH), which host the readout chips. They are printed circuit boards (PCBs) with a fold-over design in such a way that the upper surface of the FEH is on one level with the top sensor. The fold-over surface on the bottom side of the FEH is on one level with the bottom sensor. This makes it possible to connect the strips of the sensor with pads on the FEH via small wirebonds. It allows the electrical readout of both sensors on one readout chip. A total of 127 strips of the top and 127 strips of the bottom sensor are read out by one CBC (CMS Binary Chip) [21]. These chips can convert the voltage pulses from the strips of a sensor into a binary signal, meaning that no information about the actual pulse height is read out. Voltage signals from the sensor are shaped and amplified by the CBCs. Then the signal height is compared with a threshold. Only signals above the threshold are detected as hits. On each FEH eight CBCs are mounted. This results in a total of 2032 readout channels. The data from eight CBCs per FEH are processed, buffered, and forwarded to the service hybrid (SEH) by another chip, the CIC (Concentrator Integrated Circuit) [22]. Both chips were developed for the CMS experiment and fulfill the requirements on radiation tolerance and readout speed. The FEHs are connected to the service hybrid. This is another PCB hosting important components for further data processing, data transmission to the back-end of the detector, and the power supply. A significant part of this thesis deals with the testing system of the SEHs. Therefore, they will be described in more detail in Section II.4.4. On the opposite side of the SEH the FEHs are connected by an electrical ground tail PCB which also connects the electrical ground levels of both FEHs on the opposite side to reduce the electrical noise.

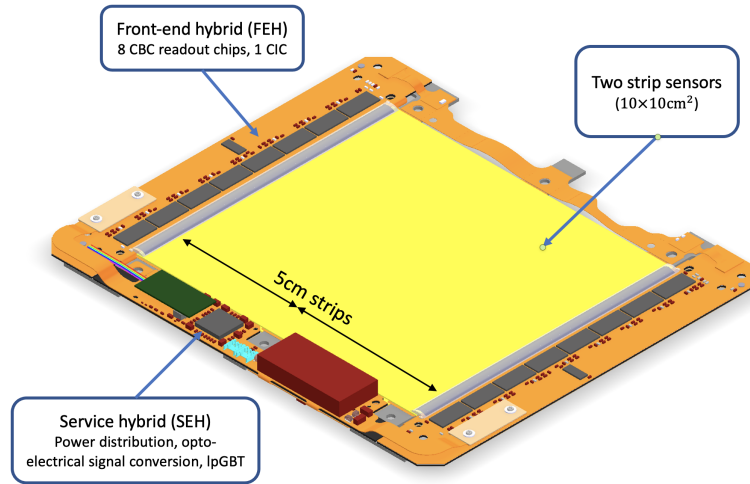


Figure II.6: Schematic drawing of the 2S module. Shown in yellow are the two silicon strip sensors. The two front-end hybrids (FEH) and the service hybrid (SEH) are shown in orange [23].

II.4.4 Service hybrids

The new 2S module for the HL-LHC upgrade has a standalone module design. This means that no common service boards are needed, and the number of connections to the back-end of the detector is reduced to a minimum by generating the necessary voltages directly on the SEH. Only three wires, one for low voltage (LV), one for high voltage (HV), and one for electrical ground, as well as two optical fibers, are connected to the module [6]. A picture of the SEH is shown in Figure II.7. The SEH is connected to both FEHs via AXE850124 connectors. The electrical schematics are presented in Appendix A.1.

To reduce the material budget in the detector, thinner wires with higher voltages should be used to power the module. The power losses in the wires are proportional to I^2 , where I is the current. Therefore, a higher voltage with smaller currents is advantageous. The input low voltage of the SEH is 10.5 V. This voltage is reduced to the necessary voltages for the ASICs and the optoelectronics in a two-stage powering scheme. A first DC-DC converter, using a bPOL12V chip [24], provides a 2.55 V voltage necessary for the VTRx⁺ [6]. The other DC-DC converter (with a bPOL2V5 chip) [24] reduces this 2.55 V voltage further to 1.25 V, necessary for the other components on the module like CBCs, CICs, VTRx⁺, or lpGBT. Each DC-DC converter is a step-down buck converter operating with switching frequencies between 3 MHz and 4.5 MHz. They convert higher voltages with smaller currents to lower voltages with higher currents. A DC-DC converter consists of the bPOL chip and passive filter components. An air-core inductor coil is used as an energy storage element. The magnetic coils produce high-frequency electromagnetic fields. These fields cause electrical noise at the nearby sensors. To reduce this effect, both converters are covered by one shield made from a tin-coated aluminium case, which is soldered on the service hybrid PCB. Disadvantages of the use of DC-DC converters on the module are power losses because the voltage conversion is not 100 % efficient.

The high voltage for the sensors is also connected to the SEH. It is then filtered and distributed to the sensors. The filter and the connection traces for the HV are located on the bottom side of the SEH. The part of the flexible PCB that contains the HV components is folded around a stiffener. Via flexible Kapton cables, the HV is connected to the sensors, and the cables are wirebonded there.

The collected data from the CICs are serialized by the Low-Power Gigabit Transceiver (lpGBT) ASIC [25]. It sends and receives data to and from the VTRx⁺ (Versatile Transceiver plus) [26]. Also, it configures the front-end ASICs via a modified I^2C protocol [27]. Additionally, it features an analog-digital-converter (ADC) that makes it possible to measure different voltages and temperatures on the module. For example, an NTC (Negative Temperature Coefficient) thermistor is glued on the backplane of the top sensor and is connected via a flexible Kapton

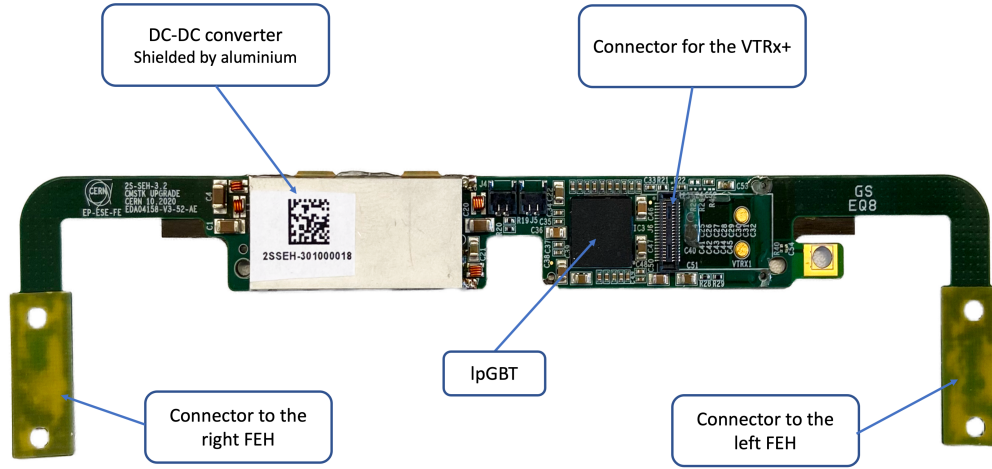


Figure II.7: Picture of the 2S module service hybrid (SEH). The $VTRx^+$ is not mounted on the SEH.

cable to the SEH. This allows for a measurement of the sensor temperature with the lpGBT. An overview of the measured ADC values and a short explanation are given in Table II.1. A more detailed description is given in Section III.4. Additionally, the lpGBT monitors and controls different components on the SEH like the proper functionality of the DC-DC converters and the $VTRx^+$. The final version of service hybrids uses lpGBT version 1.

Table II.1: ADC measurements conducted on the SEH by the lpGBT.

Measured parameter	Explanation
AMUX_L	Multiplexed line for different signals from the left front-end ASICs.
VMON_P1V25_L	Monitoring of the 1.25 V voltage received of the left FEH.
VMIN	Measurement of the input voltage on the SEH.
AMUX_R	Multiplexed line for different signals from the right front-end ASICs.
TEMP_P	Voltage proportional to the sensor temperature.
VTRX+_RSSI_ADC	Voltage corresponding to the optical signal strength received by the $VTRx^+$.
PTAT_BPOL2V5	Output voltage of the BPOL2V5 proportional to its internal temperature.
PTAT_BPOL1V25	Output voltage of the BPOL1V25 proportional to its internal temperature.

The $VTRx^+$ serves as an opto-electrical transceiver, converting the electrical signals from the module to optical signals and vice versa. It is connected with two optical fibers to the back-end of the detector. Via one fiber, trigger stub data and full readout data are sent from the module to the back-end. Via the other fiber, trigger signals and control signals are received. The full readout data is only sent if a trigger-accept signal is received from the back-end. The laser driver in the $VTRx^+$ can measure the optical signal strength and sends it, converted to an RSSI voltage (Received Signal Strength Indication) signal, to the lpGBT. The clock for the correct readout timing is also received by the $VTRx^+$ and distributed by the lpGBT to the FEHs. The design of the SEH was developed at CERN. Important parts of its quality control procedure are developed at Aachen-1B as described in Section III.1.

III. SEH quality control

III.1 Quality control for SEHs

The Phase-2 Outer Tracker upgrade is a project with high demands for quality control (QC) of its components. Several factors emphasize the importance of stringent QC measures in this endeavor. The tracker is the innermost subdetector and especially the Outer Tracker is hard to access after installation which makes repairs difficult. The components have to withstand 15 years of operation in a difficult environment with high radiation level. Additionally, the tracker is operated with a CO₂ cooling temperature of -35°C and has to endure many temperature changes. Furthermore, even minor failures involving just a few modules have a negative impact on the data quality and should be avoided, because every module that fails reduces the number of hits used for track reconstruction and worsens the track resolution.

Therefore, it is necessary to develop robust quality control. This procedure must ensure that all components installed in the experiment meet stringent quality standards and perform as expected. The quality control (QC) for the 2S module begins with the individual components, like the service hybrids or the sensors. All the hybrids for 2S- and PS-modules will undergo sophisticated testing procedures. The quality control procedure for the service hybrids is designed and implemented by Aachen-1B. After successfully testing the individual components, full modules can be built. These assembled modules undergo another round of testing then. This secondary evaluation includes assessments of alignment, module noise, and IV-scans, among other critical parameters.

The first stage of quality control for service hybrids is performed at the contractor [28]. The QC contains a visual inspection as well as functional tests. Given that the Outer Tracker (OT) operates at cold temperature in the final detector, the electrical components need to endure numerous temperature changes from room temperature to the cold operation temperature of -35°C and vice versa. This means a high mechanical stress, especially for the soldering connections, and therefore the temperature ramps are also included in the quality control procedure. During the QC, different failure modes like bad soldering connections, shorts, open lines, or problems with the chip performance can be found. At the contractor, hybrids undergo 20 passive thermal cycles as well as active functional tests at warm and cold temperatures. Only hybrids that pass the testing procedure at the contractor's side will be delivered to CERN, and the quality control procedure will be repeated there and in several other institutes. In essence, every hybrid destined for inclusion in the detector will experience at least two thermal cycle procedures paired with comprehensive functional testing to guarantee optimal performance and reliability.

III.2 The test system

To facilitate electrical testing and test data integrity, tailored PCBs are developed. These PCBs are called test cards. An individual type of test card was developed for each hybrid used in the 2S or PS modules. The test card for the service hybrid was developed by Aachen-1B, and a detailed description can be found in Section III.3. The most important tests performed with the test card are described in Section III.4.

A standard 3U-Eurocrate with twelve slots is used and all the different test cards have to fit in this crate. This specifies the requirements concerning size and electrical connections for all types of test cards. It is important that the thickness of the test card is small enough to place two test cards next to each other into the crate. Figure III.1 shows a picture of twelve test cards within the crate. The customized backplane of the crate, developed by the CERN electronics department, allows electrical connection to one card in a selected slot. During the QC, different test card types for different hybrids can be operated in the same crate. Via USB communication, the PC of the test system receives the ID of each test card and can choose the correct settings for the card.

To evaluate the data lines of the SEH, an FC7 FPGA, the standard tracker readout board for test systems [29], is connected to the backplane of the crate. Because it is connected electrically to the test cards, this FC7 is named electrical FC7. It allows to transmit specific signal patterns through the crate and the test card into the SEH. These patterns effectively emulating signals originating from the FEHs and arriving at the SEH. For data transmission, buffers, level translators, and multiplexers are used on the test card. On the SEH, the signals are detected and converted to an optical signal, sent to a second FC7 (optical FC7) via an optical fiber pair. It is possible to compare the sent and received signal pattern to check for errors in the data transfer and for problems in the lpGBT or the VTRx⁺. Also, the reverse direction can be tested to check if fast command signals or clock signals would reach the CIC in the module.

III.3 Service hybrid test card

The test card effectively emulates the behavior of other module components, such as FEHs and sensors, and is capable to measure currents, voltages, and temperatures. To test the SEH, active transistor loads are able to draw a load current from the SEH, via the data lines data pattern can be sent from the test card to the hybrid to test the data integrity, and a high voltage test PCB measures the HV input and output to the service hybrid. Figure III.2 shows a picture of the SEH test card; detailed schematics for the essential electrical components are shown in Appendix A.2. This section gives a description of the test card hardware and functionality, while a summary of the used tests in the testing procedure is given in Section III.4.

A standardized FPGA Mezzanine Card (FMC) is used, to connect the test card with the specialized backplane of the crate and to provide a connection for all power and data lines. The test cards are multiplexed and can start one after the other. The front panel of the test card is equipped with connections for high-voltage lines and the optical fibre and allows direct assessment of basic functionalities through status LEDs. All the other components, especially the connector cables and fibres are flat on the PCB to be able to push it into the crate without damaging any components.

For controlling the test card and measuring different voltages, a micro-controller (μC) is employed [30]. Three temperature sensors on the test card are connected to the μC . These sensors enable temperature measurements at three distinct locations on the test card, positioned near the two active transistor loads and the milled aluminium block with the hybrid on top. To facilitate communication with a PC via USB, a USB-to-SPI bridge is utilized, specifically the CP2130-F01-GMR [31]. With a certain software solution of the company SiliconLabs it is possible to flash an individual identification number to the USB-to-SPI bridge of each test card. This allows for digital authentication of each card in a multi-card test system. Additionally to USB data signals, the 5 V power supply is conducted via the USB cable. Furthermore, 3.3 V and 10.5 V are provided to the test card by an external power supply connected to the crate. The whole test setup is described in IV.1. For any other required voltages, an auxiliary power supply PCB is connected to the test card. This PCB serves to convert the 3.3 V input voltage into 2.5 V and 1.25 V, needed to externally fuse the lpGBT and for the data communication.

The SEH is connected via the front-end connectors to the test card. To allow more mating cycles with the connectors, small adapter PCBs are inserted, enabling easy replacement if the specified number of mating cycles is reached. To connect the HV output and the thermistor input of the SEH with the test card, flat flexible cables are used [32]. Within a module, the SEH connects to both the top and bottom sensors via two cables, providing high voltage, and to a thermistor on the top sensor for temperature measurement [6]. On the test card, the thermistor is emulated using a resistor. The 10.5 V LV and the input HV connectors are designed for a limited number of mating cycles. Therefore, a small adapter PCB is employed to extend the connector lifespan. The hybrid is connected to the optical FC7 via an optical fibre pair. In total, all the connections possible with the SEH in a module are connected and tested on the test card. Attaching the SEH to the test card involves the use of two mechanical retaining springs, that place the hybrid on a milled aluminium block that functions as a passive heat sink.

The test card hardware enables the measurement of both input and output voltages, along with the corresponding currents of the SEH. The input voltage is 10.5 V, fed to the SEH. The SEH

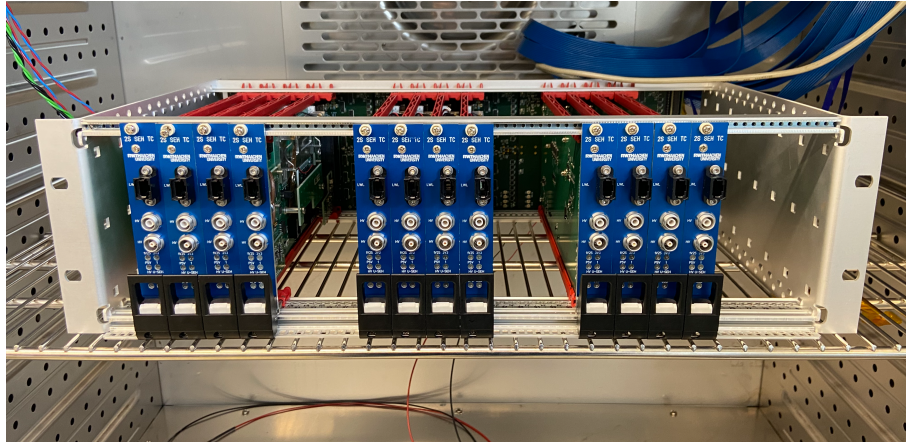


Figure III.1: Picture of a crate filled with 12 service hybrid test cards in a climatic chamber.

output voltage is 1.25 V, which is usually distributed to the FEHs in the module. To simulate the load current drawn by the front-end hybrids, active transistor loads are integrated into the test card. For each side individual, a load current can be drawn. Therefore, the components on the test card for the load test are identical on both sides. The voltage of 1.25 V is supplied from the SEH to the test card. There, the voltage drop over the known resistor is measured. This voltage drop is proportional to the current drawn from the SEH. The voltage is amplified and compared with the voltage reference U_{ref_Load} . The difference between the two voltages is calculated by a chip and regulates a transistor. This transistor operates like a small switch, opening and closing at a high frequency to precisely control the average current. After setting the transistor frequency, the current is measured again, and the frequency is adapted to hit the desired current. This constitutes a regulation circuit that sets the current based on a voltage reference provided by the micro-controller. Next to the regulation circuit, on an additional circuit, the current and the corresponding P1V2 voltage are measured on the test card.

To measure the current of the high voltage, a custom current measurement board is used. This is an additional PCB connected to the test card. Given that the measured leakage current is approximately 50 nA, necessitating amplification of the voltage drop over a known resistor, an operational amplifier on the board increases the voltage drop by a factor of 201. An analogue to digital converter (ADC) measures the voltage drop. The high voltage itself is measured directly on the test card with a voltage divider. However, due to a relatively high leakage current during voltage measurement compared to the SEH leakage current, simultaneous voltage and current measurements cannot occur. A description of the performed tests and measurements is given in the next section.

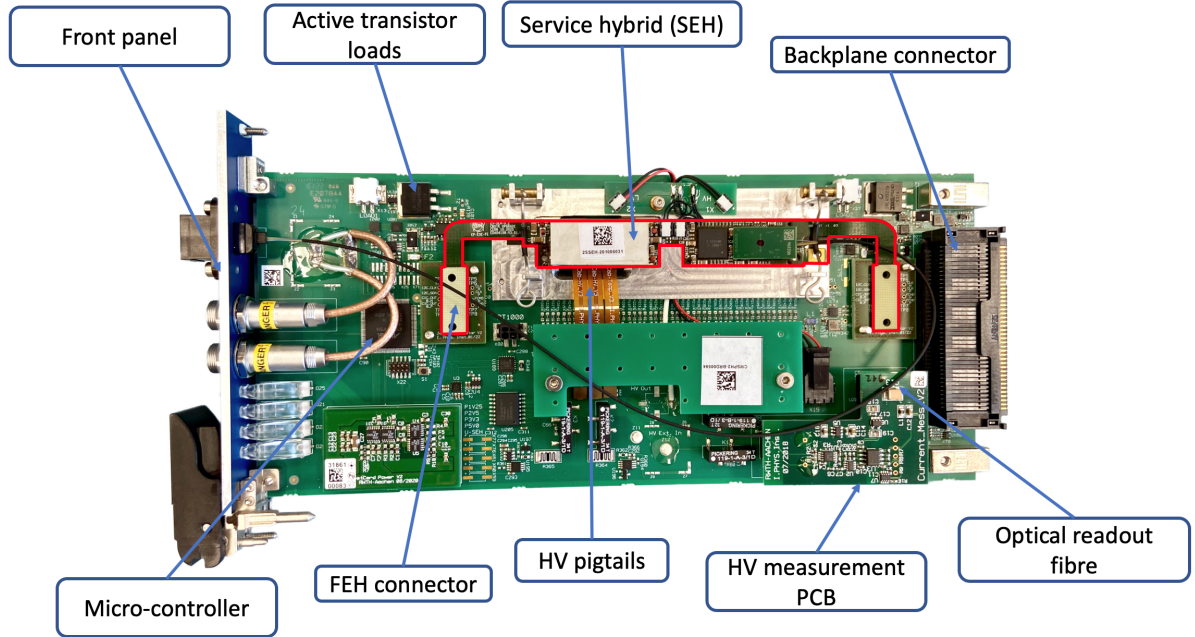


Figure III.2: Picture of the service hybrid test card. The service hybrid on the test card is marked in red. Important components are inscribed.

III.4 SEH DAQ test

To test the functionalities of the service hybrids on a test card, a test routine is developed that uses the described hardware components of the test card. Three different types of values are acquired. The first category encompasses binary values, such as pass or fail results for various tests that are executed. The second category comprises voltage measurements obtained from the micro-controller on the test card or the lpGBT on the SEH. The third category are calculated values gained from the data analysis, e.g., the turn-on voltage of the SEH. The most important tests and measurements are described in the following sections.

For a better overview of the test result, the open-source tool Grafana [33] is employed for visualizing the acquired data. The raw data are analyzed and graded by a C++ script, and the results are stored in an SQL database. The database entries are displayed with Grafana. The analysis script and the visualization of the database were developed by Martin Lipinski. The visualization method enables the direct identification of any issues by representing all the important results on one webpage. An exemplary test result in Grafana is shown in Figure III.3. Green fields represent passed tests, red fields would indicate problems. Fields with a gray color indicate measured but not graded values. Yellow fields correspond to tests that were not conducted. This can be caused by a problem during the test or, like in the figure, because some tests are not performed when a load current is drawn. Additionally, plots for the different subtests are produced. Some of them are shown in the next sections. In the plots, the criteria for a good test result are shown. Often, green error-bands correspond to the expectation regions for the data points. They are determined empirically from previous measurements. Only if all the points lie within these bands, the test pass.

III.4.1 Efficiency measurement

One important quantity of the SEH is the efficiency of the DC-DC converters. It is not possible to measure the isolated efficiency of the DC-DC converters, but the test card allows a measurement of the efficiency (η) of the hybrid. Efficiency, in this context, is defined as the ratio of the output

Load drawn right [A]	Load drawn left [A]	SEH input voltage	TC temperature	Vout Test	Efficiency Test	HV connectivity test	HV leakage current test	Stub 0 on hybrid 0 match	Stub 1 on hybrid 0 match	Stub 2 on hybrid 0 match	Stub 3 on hybrid 0 match	Stub 4 on hybrid 0 match	LA1 on hybrid 0 match	Stub 0 on hybrid 1 match	Stub 1 on hybrid 1 match
0.00	0.00	10.5	-35.1	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED
Stub 2 on hybrid 1 match	Stub 3 on hybrid 1 match	Stub 4 on hybrid 1 match	LA1 on hybrid 1 match	Reset CBC left high	Reset CBC right high	Reset CIC left high	Reset CIC right high	Reset CBC left low	Reset CBC right low	Reset CIC left low	Reset CIC right low	PG1V25	PG2V5	VTRx+ Slow Control	PC master 0
PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED
PC master 2	PTAT bPOL12V	PTAT bPOL2V5	TEMP	VMIN	Vmon 1.25V left	VTRx+ RSSI ADC	VREFCNTR	ADC gain	ADC offset	320 MHz Clk test left	320 MHz Clk test right	FCMD CIC left match	FCMD CIC right match		
PASSED	1.03	0.553	0.856	0.519	0.816	0.828	155	1.87	514	PASSED	PASSED	PASSED	PASSED		
~ Detailed Tests Results															
Subtest Results															
Load drawn right [A]	Load drawn left [A]	SEH input voltage	TC temperature	Vout Test	Efficiency Test	HV connectivity test	HV leakage current test	Stub 0 on hybrid 0 match	Stub 1 on hybrid 0 match	Stub 2 on hybrid 0 match	Stub 3 on hybrid 0 match	Stub 4 on hybrid 0 match	LA1 on hybrid 0 match	Stub 0 on hybrid 1 match	Stub 1 on hybrid 1 match
1.19	1.19	10.4	-31.7	Untested	Untested	Untested	Untested	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED
Stub 2 on hybrid 1 match	Stub 3 on hybrid 1 match	Stub 4 on hybrid 1 match	LA1 on hybrid 1 match	Reset CBC left high	Reset CBC right high	Reset CIC left high	Reset CIC right high	Reset CBC left low	Reset CBC right low	Reset CIC left low	Reset CIC right low	PG1V25	PG2V5	VTRx+ Slow Control	PC master 0
PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED	PASSED
PC master 2	PTAT bPOL12V	PTAT bPOL2V5	TEMP	VMIN	Vmon 1.25V left	VTRx+ RSSI ADC	VREFCNTR	ADC gain	ADC offset	320 MHz Clk test left	320 MHz Clk test right	FCMD CIC left match	FCMD CIC right match		
PASSED	1.03	0.540	0.842	0.504	0.810	0.818	167	1.88	514	PASSED	PASSED	PASSED	PASSED		

Figure III.3: Example of the Grafana overview for one test with hybrid 2SSEH-201000030. Each field represents the result of one subtest. The two blocks represent the test results with and without a drawn load current.

power delivered to the FEHs by the SEH to the input power supplied by the power source, expressed by the equation:

$$\eta = \frac{P_{\text{Out}}}{P_{\text{In}}} = \frac{I_{\text{Out}} U_{\text{Out}}}{I_{\text{In}} U_{\text{In}}}. \quad (\text{III.1})$$

It is dominated by the efficiency of the DC-DC converters, but it is also lowered by consumers on the SEH like the lpGBT or the VTRx⁺. The power consumed by these components is not measurable individually. To obtain the efficiency (η), the test card employs the active transistor loads, which draw current from the SEH. By multiplying this current with the output voltage, the total output power is calculated for each side of the SEH individually. Furthermore, a third test evaluates the efficiency when considering the total output current on both sides together. When increasing the output current in steps of 0.5 A, the efficiency can be calculated at each step. The resulting efficiency curve is shown in Figure III.4. The data points for three different efficiency measurements are shown in the figure. Two curves for the load current drawn individually on each side are shown and named "Load left" or "Load right". The third curve is the efficiency of the total load current as a sum of currents on both sides. The corresponding test is graded "passed" if all the calculated red points for the total load fall within the empirically determined green band. The efficiency depends on the temperature, so the curve of the green band is adapted for different temperatures. This is explained in Section V.5.1.

III.4.2 Turn-on and turn-off point

To characterize the turn-on behavior, the input voltage provided via the test card to the SEH is incrementally ramped up from 4.6 V to 10.5 V and is then subsequently ramped back down to 4.6 V. The size of the voltage steps is non-uniform to ensure a finer resolution at the interesting turn-on points. For each voltage step, the drawn current is measured by the power supply. Thereby, a whole IV scan of the turn-on process is measured. It is shown in Figure III.5. During the voltage increase, the current remains at a constant level of around 10 mA. At 10.2 V the current increases significantly to more than 100 mA. This is the turn-on point, when the DC-DC converter sees enough voltage to enable and starts to draw more current. A regulator routine on the BPOL chip already starts at lower voltages of around 4 V. After that point, the BPOL chip is able to monitor the input voltage with a voltage divider and enables the DC-DC conversion when a specific input voltage threshold is reached.

The first point with a current above 100 mA is the turn-on point. Its voltage and current are stored and analyzed later as `turn_on_voltage` and `turn_on_current`. After increasing the voltage to 10.5 V, it is decreased again. One can see that with decreasing voltage, the current rises. This is different from resistors and is a property of DC-DC converters. If the voltage decreases, the output current increases to keep the total output power constant. When the

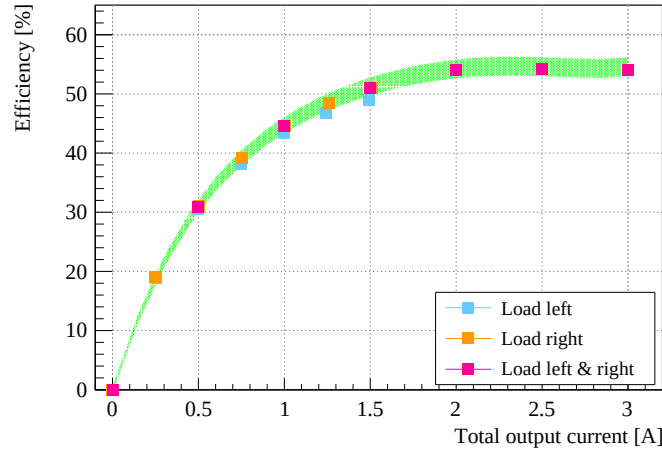


Figure III.4: Figure of the efficiency curve based on the Grafana visualization. The efficiency is calculated for different load currents drawn from the SEH. A measurement for a load current only drawn from the left side is plotted in blue, and for the right side it is plotted in orange. Red markers correspond to an efficiency measurement for the total load current drawn on both sides. These points have to lie within the green band for a good test result.

voltage falls below 6.7 V, the current drops to a level below 20 mA. This point corresponds to the `turn_off_voltage` and `turn_off_current`, when the DC-DC converter turns off.

The exact values of these two points depend on the specific SEH being measured and the ambient temperature. Knowing these values for the modules within the detector is crucial. The turn-on and turn-off voltages are separated by around 3.5 V. If this difference decreases, for example, at colder temperatures, it could happen that the DC-DC converter turns on, and because of the current-induced voltage drop, the input voltage might decrease. The voltage drops can be explained by the long cables in the detector between the power supplies and the modules of around 100 m and by the fact that twelve modules are supplied by one cable. No sensing method is used to measure the voltage directly at the modules. Therefore, the voltage supplied to the last module in the chain is significantly reduced compared to the supply voltage. If the voltage at the module drops below the turn-off voltage, the converter would switch off, creating an undesired situation in the detector. By measuring the turn-on and turn-off voltages for each hybrid at different temperatures, this problematic behavior in the detector can be excluded.

III.4.3 HV tests

The distribution of bias voltage (HV) to the sensor occurs through the SEH. For this, the high voltage connected to the HV connector is routed at the bottom side of the SEH to two Molex connectors [32]. On the module, they are connected to the backsides of the top and bottom sensors, respectively, with flexible Kapton cables. The test card provides the possibility of measuring both the voltage and current of the bias voltage.

For the HV leakage test, a voltage of 1000 V is applied to the SEH and the current is measured for a total time of 150 s. The leakage current is shown in Figure III.6. The plot shows the measured HV current, once measured on the test card and once with the HV power supply. During the first 20 s the leakage current is decreasing (in fact, the negative current is rising) towards zero. This initial decline can be attributed to two capacitors on the SEH, which connect the HV line to electrical ground. At the beginning of the test, they charge up, resulting in a current of around -60 nA. Once the capacitors are fully charged, the leakage current represents the current flowing through them, as they only have a finite internal resistance. Its value is measured to be around -30 nA. As long as the current remains above the threshold of -150 nA

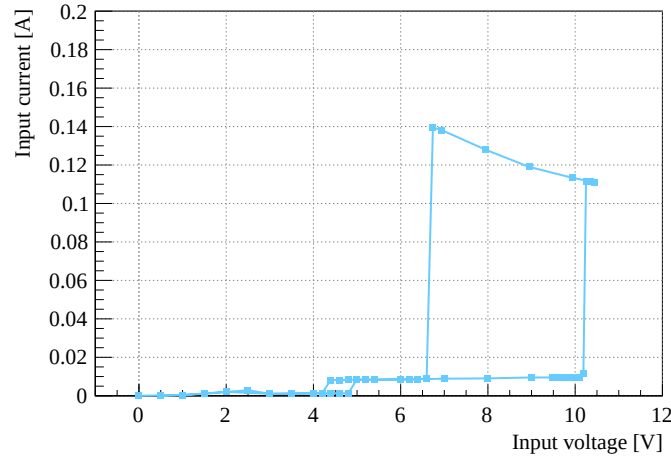


Figure III.5: Turn on characteristic of the service hybrid based on the Grafana visualisation. With the IV scan, the turn-on voltage can be determined. The data points in the plot are measured counterclockwise.

until a time of 80 s and above -120 nA after that, the hybrid passes the test. These threshold are indicated by a red dotted line.

The second test concerning high voltage is the measurement of the voltage. On the test card, the high voltage is connected to electrical ground via a voltage divider consisting of a $5\text{ M}\Omega$ and a $5\text{ G}\Omega$ resistor. When the voltage drop over the smaller resistor is measured, it is $\frac{1}{1001}$ of the total voltage between the high voltage and ground. Because of the high resistances, the measured currents are small and require amplification by amplifiers. Then it can be measured by the micro-controller. The voltage measurement is performed individually for the two connectors. The HV is gradually increased by the HV power supply and simultaneously monitored on the test card. This measurement is shown in Figure III.7. It shows the measured voltage over the applied voltage by the power supply. Two curves of data points are presented for the two HV connections between the SEH and the test card. Only if all the data points from both connectors fall within the narrow green band, the test pass. It is not possible to measure current and voltage simultaneously because the leakage current on the hybrid is of the same order of magnitude as the small current necessary for a voltage measurement. Therefore, a simultaneous measurement of the voltage would distort the current measurement.

III.4.4 Data integrity test

One important test on the test card is the data test, designed to ensure the data integrity of the SEH. Its primary objective is to verify that, within the module, signals originating from the FEHs are accurately distributed to the back-end by the SEH. This includes the data integration in the lpGBT as well as the electro-optical conversion in the VTRx⁺. In the test setup, the electrical FC7 simulates the FEHs. It transmits various patterns via the front-end connectors to the SEH. The optical signal from the VTRx⁺ is then received by the optical FC7. The software on the PC compares the sent and received signals. The test is deemed "passed" only when the received signal perfectly matches the sent signal for all the different patterns tested. Five different patterns are used, including examples like *0b00000000* (*0x00*), *0b11111111* (*0xFF*), or *0b01010101* (*0xAA*). The patterns are presented in binary values, indicated by the prefix *0b*. Additionally, the conversion to hexadecimal numbers is given in brackets. One pattern is an 8-bit binary sequence that is repeated periodically. Each pattern is sent 10,000 times. Five different patterns are necessary because some issues with the hybrids could produce signals that look identical to the sent patterns. For example, the signal received from an open connection can not be distinguished from a sent pattern with zeros. With the five different patterns, data integrity

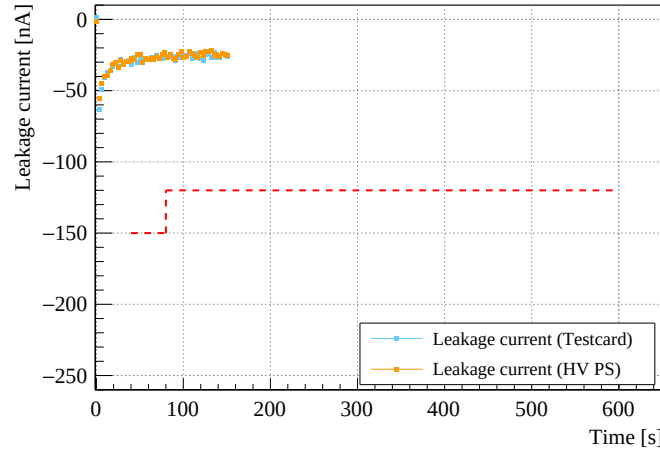


Figure III.6: Measurement of the HV leakage current for an applied voltage of 1000 V based on the Grafana visualisation. Blue data points correspond to currents measured by the test card, orange points are measured by the power supply. The test passes if the points after 20 s lay above the red dotted line.

can be ensured. The exact start of a pattern is not so important because the whole pattern is shifted to check if it fits the sent pattern. This means if *0b11001010* is sent, then the received pattern *0b01100101* would pass the test because it is essentially the same pattern shifted by one bit. The results of these tests are recorded as binary values, indicating either "passed" or "failed," and are stored in the database. The test is executed for the five stub lines and the trigger line of each hybrid. So, in total, twelve lines are tested.

III.4.5 FCMD test

Fast command (FCMD) communication is used by the lpGBT to distribute trigger signals to the front-end ASICs. The test for these communications works similarly to the data integrity tests. Various eight-bit patterns are transmitted by the lpGBT to the electrical FC7. In addition to the data test patterns, the idle frame pattern *0b11100000* is also transmitted periodically. Each FCMD signal consists of a three-bit sync code, set to *111* for the idle pattern, and a five-bit command code, which is set to 0 for this pattern. The test is successful only if the electrical FC7 correctly receives the expected patterns.

III.4.6 I²C test

The I²C communication protocol, short for Inter-Integrated Circuit, is a widely adopted standard for chip-to-chip communication [27]. In the module, the lpGBT acts as an I²C master, enabling it to configure the front-end ASICs [6]. Additionally, the VTRx⁺ can be controlled by the lpGBT via the I²C protocol. In total, two I²C masters are used to control the left and right FEH. Each master operates at a speed of 1 Mb/s. To evaluate the integrity of the I²C connection, the master dispatches a command through the test card to the electrical FC7, which is simulating a slave like a front-end ASIC. If the FC7 slave is addressed correctly, it sends a certain ACK signal back (9th bit of the data line low). Only if the lpGBT does not see any errors during the transmission, the test is passed. This testing procedure is repeated 10,000 times. The tests of the connection to the two front-ends are named "i2cmaster0" and "i2cmaster2".

III.4.7 Clock test

The timing synchronization is distributed to the module from the clock channel of the lpGBT. It is a 320 MHz E-port. This clock frequency is established by dividing the incoming 2.56 Gbit/s

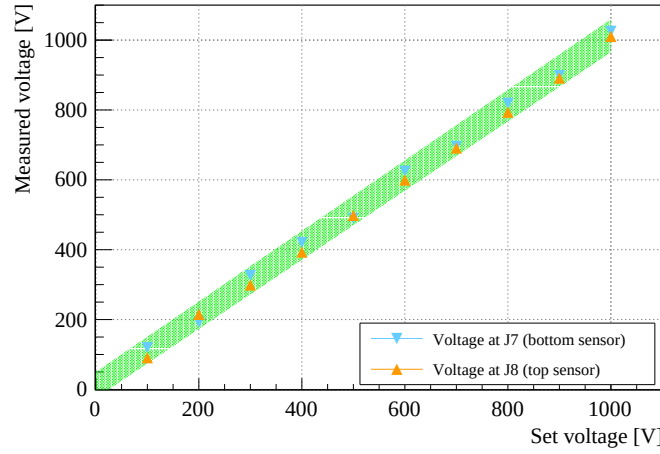


Figure III.7: Measurement of the output high voltage for different set high voltages based on the Grafana visualisation. The two different markers correspond to measurements with the two high voltage connections. Only if all the points are within the green band, the test passes.

data stream from the back-end by eight. The on-module clock is distributed to all front-end chips. The front-end ASICs convert the 320 MHz from the lpGBT to an internal 40 MHz clock signal for the readout. To assess the accuracy of the clock distribution using the test card, the electrical FC7 counts the incoming voltage edges per second on the clock line and compares them with the expected frequency.

III.4.8 Reset test

The lpGBT provides the possibility of resetting the front-end ASICs. For this, a dedicated reset signal is sent from an lpGBT GPIO (General Purpose Input/Output) pin to the front-end hybrids. This functionality is tested on the test card. The reset signal is sent from the hybrid to the test card. Only if the correct voltage signal is received there, the test pass.

III.4.9 ADC calibration

The lpGBT provides an internal Analog-to-Digital-Converter (ADC) that allows voltage measurements on the SEH [25]. The accurate calibration of this ADC is crucial because many other measurements, like temperatures or currents, are measured as voltages. The lpGBT has an internal reference voltage, V_{ref} and it measures voltages between $-V_{\text{ref}}$ and $+V_{\text{ref}}$. This internal reference voltage can be set by an external register value. External voltages (V_{pos}) between electrical ground (GND) and 1 V should be able to be measured as 10-bit ADC values. To allow this, the voltage range is shifted by internally setting the negative input to the fixed value of $\frac{V_{\text{ref}}}{2}$. When an external voltage is applied to the positive input, the difference between this voltage and the $\frac{V_{\text{ref}}}{2}$ on the negative input is measured. As an example, an applied voltage of 0 V results in a measurement of $-\frac{V_{\text{ref}}}{2}$ by the lpGBT, while 1 V corresponds to $+\frac{V_{\text{ref}}}{2}$. Therefore, a measurement range between $-\frac{V_{\text{ref}}}{2}$ and $+\frac{V_{\text{ref}}}{2}$ is used. To utilize the entire measurement range between $-V_{\text{ref}}$ and $+V_{\text{ref}}$, a gain (G) of approximately 2 is used and an offset (O) of the middle of the measurement range is applied. The master formula for the calculation of the ADC values is derived in the following lines:

$$ADC = \frac{V_{\text{pos}} - V_{\text{neg}}}{V_{\text{ref}}} \cdot G \cdot 512 + O \quad \left| \quad V_{\text{neg}} = \frac{V_{\text{ref}}}{2} \right. \quad (\text{III.2})$$

$$= \left(\frac{V_{\text{pos}}}{V_{\text{ref}}} - \frac{1}{2} \right) \cdot G \cdot 512 + O \quad \left| \quad O \approx 512 \text{ (half scale)} \right. \quad (\text{III.3})$$

$$\approx \frac{V_{\text{pos}}}{V_{\text{ref}}} \cdot G \cdot 512 + O \cdot \left(1 - \frac{G}{2} \right). \quad (\text{III.4})$$

With the derived formula, a measured input voltage can be converted to ADC values. The factor 512 represents half of the maximum scale for a 10-bit value. To calculate the correct ADC values, G , O , and V_{ref} must be determined. The exact value of V_{ref} is not important, it just has to be constant for each ADC measurement. To simplify calculations, it is tuned to 1 V. The tuning algorithm has several steps:

1. Write the register value $V_{\text{ref,tune}}$ to set the internal reference voltage V_{ref} to a fixed but unknown value.
2. A known voltage is supplied from the test card to the SEH.
3. The lpGBT measures it as an input voltage on its AMUX input as any ADC value.
4. When additionally using the values for G and O determined before, one can calculate V_{ref} with equation III.4. ADC , G , O , and V_{pos} are known values in the formula.
5. The value $V_{\text{ref,tune}}$ is adjusted bitwise to tune V_{ref} to 1 V.

This algorithm has the consequence that V_{ref} is set to 1 V and that the input voltage VMIN used for the calibration will always be measured to its reference value set by the test card.

For the calibration in the module, a known measured input voltage at the voltage divider R19/R20 on the SEH is needed. This voltage is measured before the calibration by hand with a multimeter, and the acquired voltage value is saved into a settings file. The same voltage is measured as VMIN on the ADC2 input of the lpGBT and by comparing both voltages, a similar algorithm as described for the test cards is performed.

G and O are independent of V_{ref} . To determine the offset (O), the difference between the internal $\frac{V_{\text{ref}}}{2}$ on the negative input and a measurement of the same external voltage $\frac{V_{\text{ref}}}{2}$ on the positive input is measured. In that case, by using the equation III.4, the resulting ADC value is exactly the offset. By measuring the difference between $\frac{V_{\text{ref}}}{2}$ and GND the gain (G) can be calculated. The gain is not exactly 2, but around 1.9, and the offset is expected to be around 512. Values for G , O , and V_{ref} are acquired and logged for each test.

III.4.10 VMIN

VMIN is the input voltage measured on the SEH. It is recorded as an ADC value from the lpGBT. The input voltage of 10.5 V is measured close to the LV connector with a voltage divider with two resistors of 90.9 k Ω and 4.7 k Ω . Therefore, the expected value for VMIN is

$$10.5 \text{ V} \cdot \frac{4.7 \text{ k}\Omega}{4.7 \text{ k}\Omega + 90.9 \text{ k}\Omega} = 0.516 \text{ V}. \quad (\text{III.5})$$

III.4.11 TEMPP measurement

On the module, it is possible to measure the sensor temperature. To achieve this, a small NTC thermistor is glued to the sensor and connected to the SEH via a flat connector cable. The resistance of the NTC thermistor is proportional to its temperature. So, by measuring the resistance, the temperature can be calculated. The exact resistance is measured by the lpGBT. It supplies a specific current to the NTC thermistor and measures the necessary voltage. The value of this voltage is stored as TEMPP. With Ohm's law, the resistance is calculated, and with

the known behavior of the NTC, the temperature can be determined. On the test card, the NTC thermistor is emulated by a $5.1\text{ k}\Omega$ resistor connected to the SEH. This does not provide actual temperature information, but the resistance measurement procedure can be tested. A current of approximately $95\text{ }\mu\text{A}$ is set, and the necessary voltage is measured as TEMPP.

III.4.12 PTAT BPOL2V5 measurement

The BPOL chips in the DC-DC converters provide information about their internal chip temperature. It is the voltage output of the chip named PTAT BPOL2V5 for the 2.5 V DC-DC converter. PTAT, for "Proportional To Absolute Temperature", already describes its functionality. The voltage is directly measured as an ADC input in the lpGBT. The relation between the PTAT voltage and the chip temperature is given in the BPOL2V5 manual [24]. The PTAT increases linearly with respect to the absolute temperature. The slope is approximately 4 mV/K [24]. The absolute voltage depends on whether the chip was irradiated or not. It is hard to get information about the actual chip temperature because it is mounted below an aluminium case to shield the produced magnetic field. The information in the manual regarding the slope will be verified for a module in Section VII.3.3. Unfortunately, on the used prototype hybrids it is not feasible to measure the PTAT BPOL12V from the first-stage DC-DC converter because a necessary voltage divider is missing on the SEHs. Therefore, the measured voltage always lies in the saturation range of the ADC.

III.4.13 Additional measurements

Different other measurements are performed by the lpGBT as summarized in Table II.1. An RSSI voltage is provided by the VTRx^+ . It is an output voltage that corresponds to the optical signal strength received by the VTRx^+ . Thereby, a large RSSI voltage corresponds to a small photo current, and vice versa [26]. Power-good signals from the two DC-DC converters are measured by the lpGBT. They are output signals from the BPOL chips and indicate the proper operation of the chips. It is asserted during normal operation, while it is negated when the output voltage is outside a regulation window, which is approximately $\pm 6.5\%$ around the selected output voltage. Additionally, AMUX values are measured by the lpGBT. These are voltage signals from the front-end ASICs on a multiplexed trace to provide information about different states of the chips.

IV. Test card quality control

The operation of the test system will primarily be handled by technicians who do not have experience troubleshooting issues related to the test card. Therefore, it is of great importance that all the test cards function well. A defective test card could potentially lead to failed SEH tests, resulting in the exclusion of otherwise viable hybrids. As the hybrids shall undergo thermal cycling, the test cards need to withstand hundreds of thermal cycles. This underlines the importance of implementing quality control (QC) measurements for the test cards. This chapter explains the quality control of the test cards conducted with functional tests and presents the results. The procedure tests the general functionality of test cards in a simplified setup at room temperature without a crate. In the next chapter, the test will be extended by thermal cycles at warm and cold temperatures.

IV.1 Test setup

To test the test cards, a small setup with a mini-backplane is used. It is a smaller version of the backplane used later for the thermal tests. It has only one FMC connector to connect a single test card. The whole setup lies flat on a table to have better access for debugging measurements. A sketch of the setup is shown in Figure IV.1. Different low voltages are supplied by a Hameg HMP 4040 power supply [34]. The power supply provides 3.3 V needed for the operation of the test card and -3.3 V necessary for the backplane, as well as 10.5 V for the operation of the SEH on the test card. All the voltages are connected to the mini backplane and distributed via the FMC connector to the test card. A high voltage of up to 1000 V for the HV test (Section III.4.3) is connected directly to the front panel of the test card and is provided by an ISEG SHR [35]. The SEH is connected to the optical FC7 [29] with the optical fiber, and the mini backplane is connected to the electrical FC7. With this configuration, it is possible to simulate data patterns with the electrical FC7 and send them via the test card and the SEH to the optical FC7 or vice versa. The clocks of both FC7 are synchronized by the μ TCA crate the FC7 are mounted in. A special module in the crate distributes the clock signal through the backplane to both FC7. Additionally, another configuration is possible when the first FC7 outputs the clock signal to the second FC7, which uses the clock signal as an input via two connector cables. This configuration is used later for the climatic chamber setup (Section V.1). Only with synchronized internal clocks can the data patterns sent or received by the FC7 be compared. The whole setup is controlled by a C++ routine on a Linux-based PC. The PC controls all the components, like the HV- and LV-supply as well as the FC7 in the crate.

IV.2 Test procedure

To test the different functionalities of the test card, a two-stage test procedure is used. First, a basic electrical test is performed to test the electronic properties of the test card. Second, an extended SEH DAQ test is conducted to judge the data lines and the 1000 V high voltage connection. This test procedure is performed with every test card. A shorter and faster version of this DAQ test with a graphical user interface (GUI) is going to be used for the quality control of SEHs at the manufacturer. A functional SEH is necessary to evaluate the full functionality of the test card. To make tests of different cards comparable, the identical SEH is used for each test. The used SEH has the ID 2SSEH-201000045.

IV.2.1 Basic electrical test

This routine is based on a LabVIEW [36] script and was mainly developed by Stefan Schmitz [37]. It allows communication with the CP2130 USB-SPI bridge on the test card. It offers a wide range of measurement capabilities made possible by the micro-controller. This includes the readout of

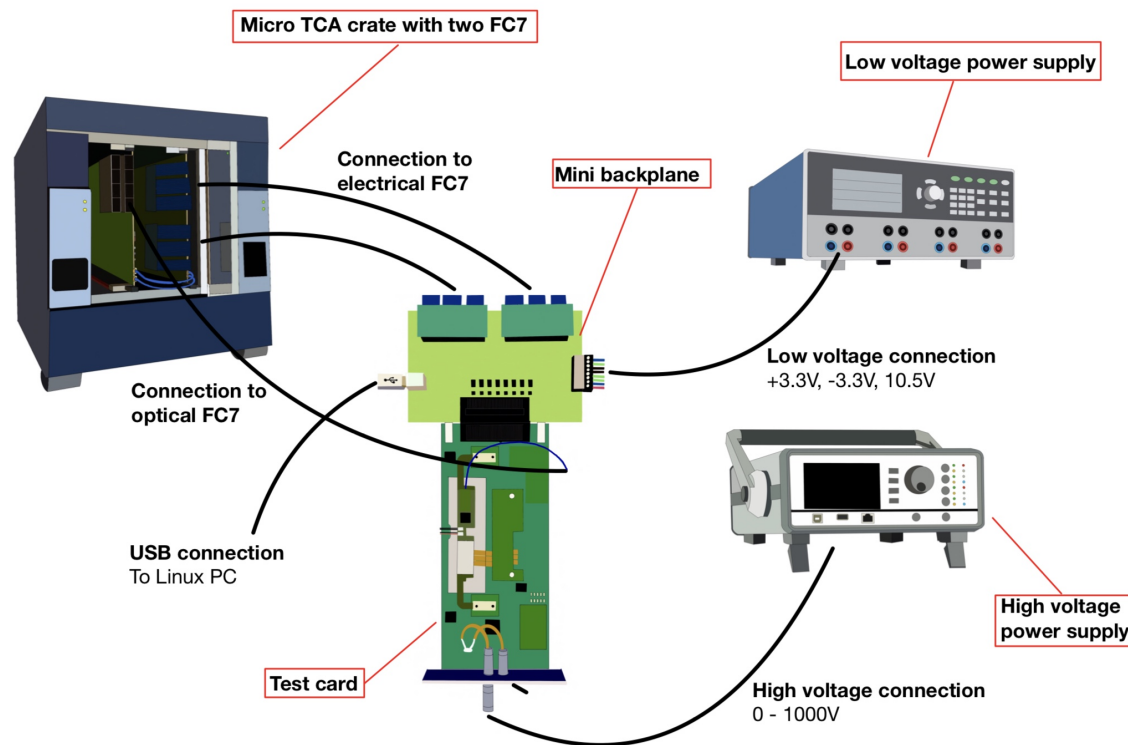


Figure IV.1: Sketch of the test setup. For better visualisation only the most important components are shown with their connections to the test card.

the three temperature sensors on the test card. Additionally, all the crucial voltage levels and their corresponding currents are measured. It shows the importance of a voltage measurement during quality control, as even a minor deviation in any voltage value could lead to a failure in the fundamental functionalities of the test card. To achieve this measurement, the voltage readings are obtained by utilizing current shunt and power monitor chips. The corresponding currents are measured by monitoring the voltage drop across known resistors using the same chips. The acquired measurements are transmitted through the I^2C protocol to the micro-controller and subsequently recorded via USB communication. In the following, the measured voltages and their functionalities are described, and the name of the voltage is given in brackets.

The supply voltage of 10.5 V for the SEH (U SEH) received from the backplane is distributed to the SEH. Meanwhile, the 5 V voltage (U P5V) is essential for powering components like the CP2130 USB-SPI bridge and the HV current-measurement PCB. It is supplied by the USB cable from the PC. The 3.3 V voltage (U P3V3) serves as the supply voltage for various test card components, such as chips, buffers, and comparators. A 2.5 V voltage originates from the SEH and is used as a supply voltage for the $VTRx^+$ there. On the test card, it could be measured as P2V5_VTRx_MON by the micro-controller, but this measurement is not included in the basic electrical test. Furthermore, there is a 2.5 V voltage generated by the test card power PCB (U P2V5), primarily used to fuse the lpGBT chip from the test card. This feature was required for lpGBT version 0 but is no longer in use for version 1. Nevertheless, the U P2V5 voltage is still measured. A voltage of 1.25 V is used on the test card for the pull-ups for data communication with I^2C (U P1V25). It is important to note that only the most important components, for which the voltages are essential, are described here.

Additionally to these more or less static voltage and current values, a dynamic load ramp test is performed. For this, the active transistor loads are controlled by the LabVIEW program, allowing them to draw current from the SEH. The load current on each side is increased from 0 A to 1.5 A in steps of 0.25 A. At each step, ten measurements were taken to be able to calculate the mean and standard deviation. This functionality provides the possibility of emulating the

power consumption of the FEHs. The static voltage and current values are measured while a load current of 1.5 A is drawn on each side.

The aim of the voltage measurements is to allow quality control tests and debugging possibilities on the test card. The acquired values are internal properties of the test card and have nothing to do with the tested service hybrids. Most of these measurements are not included in the extended DAQ test. For the quality control of the test cards, both tests are performed and analyzed.

IV.2.2 Extended DAQ test

For the quality control of test cards, an extended version of the DAQ test used to test the SEHs is performed. It is described in detail in Section III.4. Measurements with the known test hybrid are acquired, and bad test results can be traced back to an issue on the test card. The test is an extended version because, during the test procedure, two DAQ tests are performed. The whole test routine with the described subtests is conducted without load. The only exception is the efficiency measurement, described in Section III.4.1, which varies the load current. The voltages and currents for load currents of 0 A and 1 A are stored, for example, as `vout_1_0A`, representing the voltage on the left connector for a 0 A load current. The general load current for the other subtests is set to 0. A second DAQ test is repeated with a predefined load current. Many of the subtests, including the I^2C test, the stub test, or the FCMD test, are performed while a load of 1.2 A is drawn from the hybrid. Other subtests are not repeated with load because it would be too time-consuming. Therefore, the turn-on test or the HV test are only performed without a load current. The DAQ test with load current emulates the behavior of a full module with power consumption on the FEHs and tests how the measured values and parameters are behaving. Some of the measurements performed during these tests only involve the SEH. For example, for the measurement of the RSSI optical signal strength, the VTRx⁺ provides a signal to the lpGBT and the test card is not involved. But still, they are important tests for the SEH quality control and therefore are also conducted during the test card tests.

IV.3 Test results

IV.3.1 Basic electrical tests

As described in Section IV.2.1, a load ramp is performed with the test cards. The load ramp measured with test card CMSPH2-BRD00600 is displayed in Figure IV.2. The test is divided into three sections. The first ten data points, up to a time of 50 s, are measured with the test card while the hybrid remains switched off. The measured voltage is not 0 V because residual voltages applied by pull-up resistors on the test card are measured. After these points, the hybrid is switched on with a load current of 0 A and ten further measuring points are recorded. The turn-on can also be observed in the voltage, which rises to 1.25 V. Following these ten points, the load ramp begins with a drawn current of 0 A, which is increased in steps of 0.25 A to a maximum current of 1.5 A for each side of the hybrid. Ten data points are measured at each step.

The measurement clearly demonstrates that the load ramp functions as expected and that the test cards are capable of drawing load currents from the hybrid. The measured voltage does not stay constant but decreases by about 10 % over the full current range for the left connector. This can be attributed to Ohm's law, as higher currents lead to increased voltage drops in the lines to the measurement point on the test card. This is also the reason why the voltage for the right connector is higher. The connector is much closer to the generated output voltage of the BPOL2V5 and smaller voltage drops occur on the shorter connection to the front-end connector. Additionally, the BPOL provides an internal load regulation to adapt the output voltage, but this has an effect of around 0.1 % [24]. Also, the current differs slightly between the two sides. This difference of approximately 5 % is consistent with previous measurements on earlier prototypes. The current is set by a DAC (digital-to-analog converter) value for each side. Slightly different ground levels on both sides could result in different currents, even if the same DAC value is set.

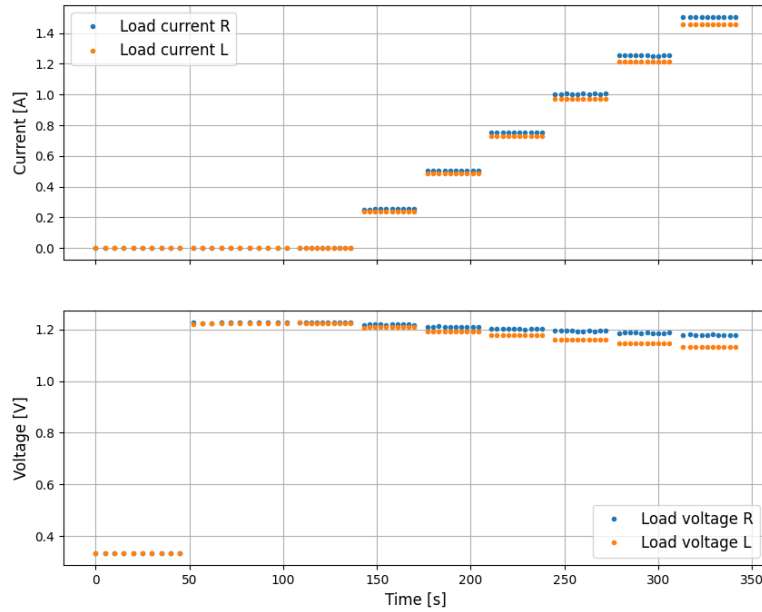


Figure IV.2: Load ramp performed on test card CMSPH2-BRD00600. The different load currents are shown in the top plot, and the corresponding voltage in the bottom one.

The measurement of static voltages and currents is performed twice, once without load and once with a drawn load current of 1.5 A per side. The produced test cards were sent in three batches, and accordingly, they were also tested in these batches. The voltage and current measurement results are obtained for all three batches. As an example of a current measurement, Figure IV.3 illustrates the distribution of the current corresponding to the P3V3 voltage. Significant outliers in the following plots, which indicate problems on the test cards, are ignored for the calculation of the mean. The P3V3 voltage is supplied to many parts of the test card, and its associated current is measured. All the presented results were obtained under realistic conditions, with a load current of 1.5 A drawn on each side. The left side of the plot displays a histogram for the results of all the test cards. The measurement results follow a narrow distribution, without any double peaks or other anomalies. The right side of the plot presents the results for the individual test cards. For each card, the current measurement is given as a mean value over ten measurements, with the standard deviation used for the uncertainty estimation. One can see the gap in the test card IDs provided by CERN between CMSPH2-BRD00603 and CMSPH2-BRD00752. The cards were tested in sequence, with test cards with smaller ID numbers being tested earlier in time. For the individual test card results, no outliers or systematics were observed. For better reading flow, the test card IDs are abbreviated, and only the three-digit number is given in the following sections.

Another interesting measurement is the temperature measured on the test cards. Equivalent to the voltage, the temperature is measured ten times, and the mean values are presented. The measurement is shown for temperature sensor T2 in Figure IV.4. The sensor is placed close to the transistor load at the front side of the test card. The results for individual test cards display some systematic behavior. The temperature of consecutive cards often exhibits a rising or falling slope. This is explained by the room temperature or other environmental effects. The room temperature heats up during the day, and this can be seen in the measured temperature, for example, for cards 777 to 781. Card 782 was measured the next day, when the ambient temperature was lower. Also, the fan used for cooling was placed by hand once for a day. This can explain slightly different temperature levels on different days. Additionally, one can see that

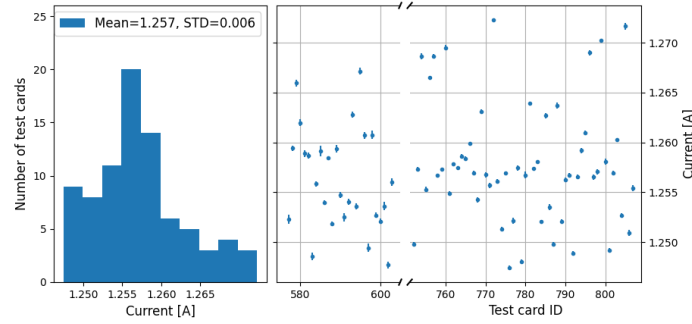


Figure IV.3: Histogram for the measurement results of the P3V3 current. The right plot shows the results for the individual test cards.

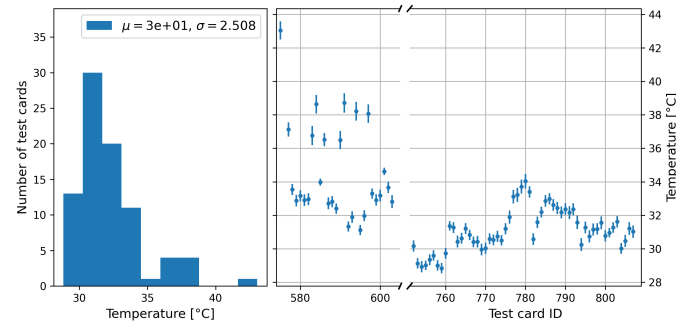


Figure IV.4: Temperature measured on the test card at point T2.

the first batch of cards up to ID 603 was tested in November 2022 and the other ones in March 2023 by Felix Boschke, which results in different test card temperature levels. Similar behavior is observed in the measurements for T1 and T3.

Most of the basic electrical measurements show a similarly narrow distribution without any outliers. Not all the measured and analyzed plots can be presented in this thesis. Observed outliers are hints of some irregularities or problems on the test card. They are discussed in Section IV.4.

All the measured results are summarized in Table IV.1. For a better overview, the internal names of the voltages are given in the table, which were already explained in Section IV.2.1. This means that U P3V3 is the name of the 3.3 V voltage on the test card and I P3V3 is the corresponding current. The table presents the mean values over all the measured test cards together with their standard deviations. The voltage U P2V5 is not required anymore, and the current I P1V25 is only used for the I^2C level translator. Therefore, the corresponding currents are very small compared to other currents on the test card. The measured temperatures vary by a few Kelvin, depending on the measurement position of the temperature sensor on the test card. In general, the test card is around 10 K warmer than the ambient temperature during the test procedure. The measured voltages are close to the expected values. For some voltages, e.g. for U SEH, voltage drops in the wires from the power supply explain small deviations. The observed standard deviation can be used to set loose limits on the measured values. If a measurement result for a single test card deviates by around three standard deviations from the mean, it may signal a problem, and the card will be subject to more detailed testing. This occurred on three test cards. All the presented values are well within the specifications and ensure the good functionality of the tested test cards.

Table IV.1: Summarized results for the test card measurements with the basic electrical test at room temperature, measured with a load current of 1.5 A. In total 88 test cards are tested.

Measured value	Mean	$\pm$	STD
Load voltage left [V]	1.1283	$\pm$	0.0015
Load voltage right [V]	1.1778	$\pm$	0.0019
U P1V25 [V]	1.2492	$\pm$	0.0019
I P1V25 [A]	0.0002	$\pm$	0.0014
U P2V5 [V]	2.498	$\pm$	0.005
I P2V5 [A]	0.00016	$\pm$	0.00009
U P3V3 [V]	3.284	$\pm$	0.008
I P3V3 [A]	1.257	$\pm$	0.006
U P5V [V]	4.991	$\pm$	0.020
I P5V [A]	0.0450	$\pm$	0.0013
U SEH [V]	10.22	$\pm$	0.10
I SEH [A]	0.607	$\pm$	0.006
Temperature at T1 [°C]	34.5	$\pm$	2.4
Temperature at T2 [°C]	32.3	$\pm$	2.5
Temperature at T3 [°C]	28.4	$\pm$	2.6

IV.3.2 Extended DAQ tests

In the same way as for the basic electrical test, the extended DAQ test results are displayed. The measured results are evaluated with a C++ routine and uploaded into an internal SQL database. From this database, they can be downloaded and presented in plots for all the test cards. One illustrative example is the service hybrid efficiency measured for different test cards. The results shown in Figure IV.5 are determined at a load current of 1 A per side. The histogram displays a narrow distribution with a mean value of 0.5408 ± 0.0019 . The measurements fluctuate about 0.35 % around the mean value. There are no significant outliers in the individual test card results. However, there is a noticeable decreasing trend towards higher test card IDs, which can be attributed to an increase in room temperature. It is shown in Section V.5 that with increasing ambient temperatures, the efficiency is decreasing. As explained in Section III.4.1 the efficiency is plotted against different load currents. Only if each measurement point lies within the empirically determined expectation band, the test pass. When the efficiency of the hybrid is measured with the test cards, the measurements always pass the test.

A second result to show is the measurement of the turn-off voltage, presented in Figure IV.6. The discrete step size of the applied voltages results in two larger bins in the histogram. Therefore, turn-off voltage falls in the bins of 6.3 V–6.5 V or 6.5 V–6.7 V. As evident in the right plot of the figure, the voltage varies within these bins, and the slight voltage fluctuations may occur due to the imperfect alignment of voltage steps by the power supply and the brief stabilization period at each step.

The last example presented is the VMIN measurement of the low voltage input, shown in Figure IV.7. In the figure, two different VMIN levels are apparent. The values measured for the first batch are around 0.57 V, for the other test cards the value is around 0.515 V. One outlier at the same voltage level can also be seen in the first batch. The two levels can be explained by the ADC calibration. The algorithm explained in Section III.4.9 was added to the DAQ test routine after the measurements of batch one. Only one test card from batch one is also tested with the ADC calibration algorithm. For the other cards, a fixed default ADC calibration is used, which is not adapted individually. The ADC calibration algorithm is performed at the chip level, and the test can not be reanalyzed. The VMIN voltage measurement clearly illustrates the significant influence of the ADC calibration on measurement results. The same effect is observed in all other ADC measurements, such as TEMPP or PTAT. The calculation of the mean and standard deviation is not very meaningful for distributions with two distinct levels.

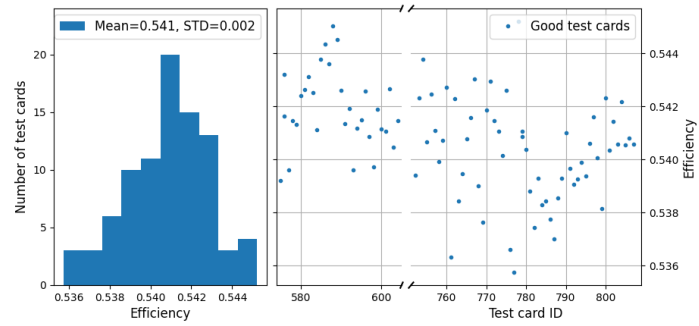


Figure IV.5: Efficiency for all the test cards.

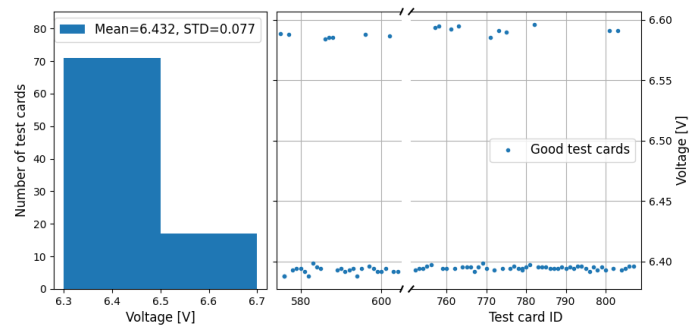


Figure IV.6: Histogram and distribution of the turn-off voltage measurement.

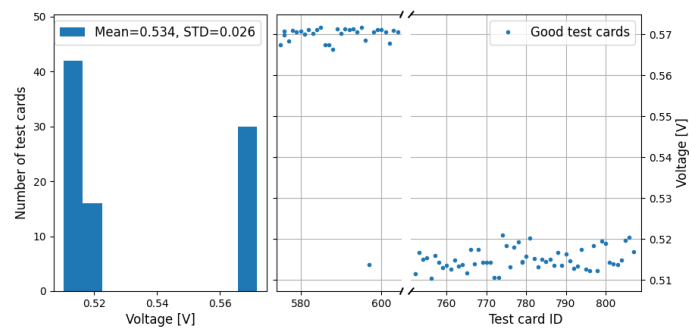


Figure IV.7: Histogram and distribution of the VMIN measurement of the input voltage.

All the other analyzed parameters exhibit a narrow distribution in the histograms. Again, outliers in the data points are an indicator of problems on the test card. These observed effects are described in the next section. The summarized measurement results are presented in Table IV.2. The mean values for all the tested cards are given with their standard deviations. For PTAT, TEMPP, and VMIN only the last two batches with 56 test cards are used to calculate the mean because of the added ADC calibration. PTAT and TEMPP voltages can not be converted to actual temperatures. The measurement for VMIN of 0.515 V corresponds to an actual input voltage of 10.48 V which is close to the applied 10.5 V. The turn-on voltage is larger than 10 V, but this is a property of the used prototype hybrid and changes for the produced kick-off hybrids. All the values are within expectations, and the uncertainties are on the order of a few percent. The presented results are acquired during the first DAQ test without a constant external load of 1.2 A drawn because, during the second test with load, only a reduced number of measurands are recorded. In the Grafana interface, both tests are analyzed and used to grade the test card.

Table IV.2: Summarized results for the test card measurements at room temperature with 88 cards.

Measured value	Mean	$\pm$	STD
SEH efficiency	0.541	$\pm$	0.002
PTAT BPOL2V5 [V]	0.557	$\pm$	0.003
TEMPP [V]	0.913	$\pm$	0.005
VMIN [V]	0.5150	$\pm$	0.0026
Turn-on voltage [V]	10.245	$\pm$	0.019
Turn-on current [A]	0.1122	$\pm$	0.0014
Turn-off voltage [V]	6.43	$\pm$	0.08
Turn-off current [A]	0.0087	$\pm$	0.0003
2.5 V output of DC-DC [V]	2.531	$\pm$	0.007
1.25 V output voltage at 0 A load [V] (left)	1.2200	$\pm$	0.0013
1.25 V output voltage at 1 A load [V] (left)	1.1566	$\pm$	0.0013
1.25 V output voltage at 0 A load [V] (right)	1.2263	$\pm$	0.0011
1.25 V output voltage at 1 A load [V] (right)	1.1918	$\pm$	0.0017

IV.4 Observed effects

IV.4.1 Rotated chip

One example of an issue identified with the electrical test can be observed in the plot of the current of the P3V3 supply voltage, presented in Figure IV.8. The plot for all the three batches was already shown in Figure IV.3, but the outlier was excluded there. For test card 575, the current is significantly higher than for the other measured cards.

To understand the reason for the outlier, a visual inspection was performed on card 575 under the microscope. One could see that the specific chip U130 was soldered incorrectly, with a rotation of 90°, as depicted in Figure IV.9. When comparing the two chips in the back row, the rotation of the right chip is evident. A white dot indicates the position of pin one of the chip, and this position is different for both chips in the back. The rotation means that all the pins of the chip are connected incorrectly, and the chip does not work as expected. It was an error made by the manufacturer of the test cards during the assembly process. The faulty connection explains the higher current measured for the P3V3 voltage. The effect of the rotated chip can also be seen in the functional test with full DAQ. The chip serves as a CIC fanout buffer, and the e-link for stub 3 is consistently broken for the left and right sides. The signal line is split up at chip U130 and connects to two chips in the front row for both sides. Therefore, by having a problem with U130, both sides are affected. The chip was resoldered correctly by the electronics team, and the test card is fully functional now. The same test is repeated, and the measurement result for the P3V3 current is perfectly aligned with the results from the other test cards.

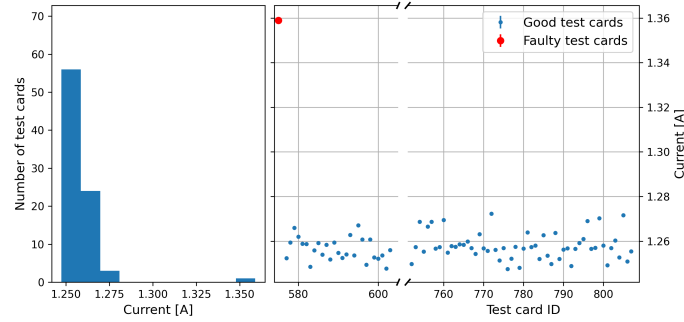


Figure IV.8: Distribution of the current corresponding to the P3V3 supply voltage. The outlier for test card 575 is a hint of a problem on the card.

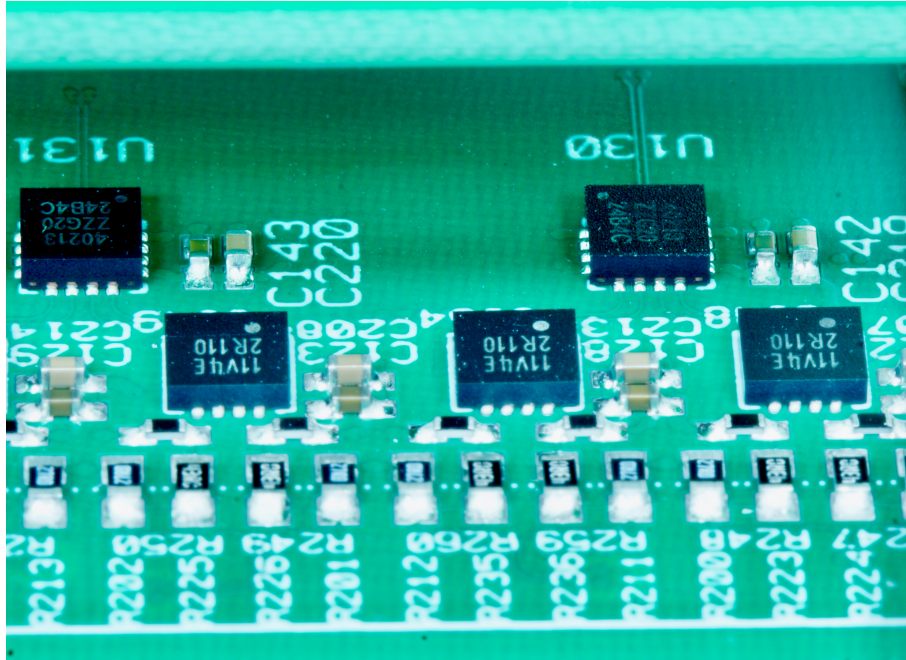


Figure IV.9: Picture of the rotated chip U130, made under the microscope.

IV.4.2 Soldering issues

Another issue arose during the tests of the I^2C communication protocol, which is part of the extended DAQ test and is described in more detail in Section III.4.6. For test cards 585 and 590 the test failed, as shown in Figure IV.10, where the grading of the test is set to zero. The reason for this failure was traced back to a soldering problem. A microscopic examination revealed that two resistors were not correctly soldered, resulting in an open connection. They influence the I^2C line and are leading to test failures. The problem was repaired in house by resoldering the resistors, and the functional test was repeated. That is the reason why the two problematic test cards have additional blue data points in the plot for the successfully conducted second tests.

Additionally, on another test card two improperly soldered resistors, R202 and R205, which serve as pull-down resistors connected to the CIC out level translate, are observed. The test card does not turn on at all for other reasons, as explained in the next section. The problem was spotted in the visual inspection, and no electrical effect could be measured.

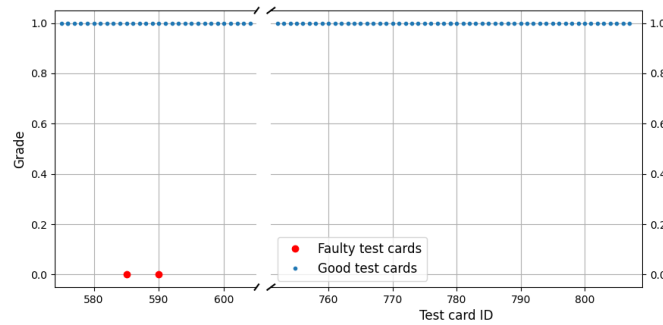


Figure IV.10: The test results for the tested I^2C protocol are bad for two test cards.

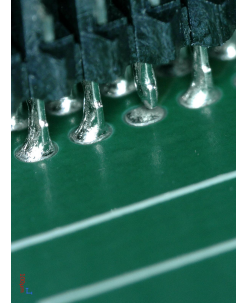
IV.4.3 Problems with the backplane connector

A significantly more severe issue has been identified in the case of the test card with internal ID 10, which is entirely non-operational. An irregularity found under the microscope are open pins in the backplane connector. A few pins are observed to not be soldered correctly, so they do not provide a good electrical connection. Pictures of not-connected pins below the backplane FMC connector are shown in Figure IV.11. The microscope only allows visibility of the first two rows of pins, with the pins in the middle obscured by the backplane connector. One example of an open pin in the first row that could be seen under the microscope is shown on the left side of the figure. This pin is a redundant pin and has no effect on the turn-on. Because it is not possible to observe open pins in the middle rows, all the test cards are scanned with X-rays by the manufacturer to check for any faulty connections. For the problematic card, one of these open pins, unfortunately not visible under the microscope, distributes the enable signal to the test card. This explains why the card does not turn on. On four test cards in total, open connections are observed, but most of these pins are redundant. Nevertheless, the corresponding test cards are being tested with great care and will not be delivered to CERN.

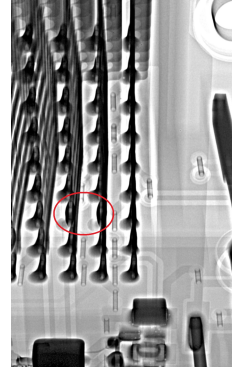
IV.5 Comparision to SEH tests

After analyzing the results for different test cards and calculating the variation between the cards, it is interesting to compare these variations with those for different hybrids. For this, the results from the first batch of 28 test cards are compared to measurements conducted on 20 distinct service hybrids of batch 2, performed by Alexander Pauls. The test cards were all tested with the identical hybrid, whereas the hybrids are all tested with an identical test card. This guarantees that variations are caused by the different cards or hybrids, but not both together. An exemplary measurement of the efficiency for different hybrids is shown in Figure IV.12. The two outliers, denoted by red dots and corresponding to ID 50 and 53, are attributed to the utilization of a distinct VTRx⁺ version in these tests. The used VTRx⁺ prototypes use four laser drivers instead of one. This leads to higher power consumption and a lower efficiency in the test.

Similarly, all the other measured results are analyzed, and the calculated mean and standard deviations can be compared. Outliers are ignored for the calculation of the mean. The summary of the most important results is shown in Table IV.3. Only the first batch of 28 test cards was used for the comparison. The setup and software version used are comparable for the first batch of measurements with different SEHs. The ADC calibration was not included in the tests for these test cards, which makes the results comparable to the SEH measurements. It is evident that the variations among hybrids are more pronounced in comparison to the test cards. This observation underscores that the outcome of a measurement is predominantly influenced by the specific SEH in use, with the test cards' variations being negligible in comparison.



(a) Microscope picture.



(b) X-ray picture.

Figure IV.11: Pictures of open pins of the backplane connector on different test cards made with the microscope at Aachen-1B and with X-rays by the manufacturer [38].

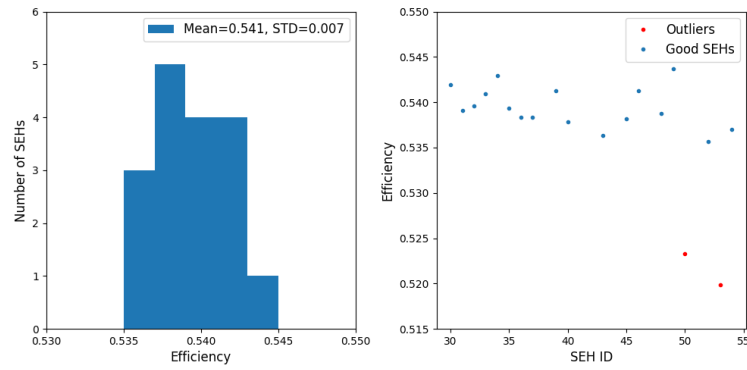


Figure IV.12: Efficiency result for different SEHs.

Table IV.3: Comparison of the mean and standard deviations for different measurands. They can be compared between test cards and service hybrids.

Measured test cards/SEHs	Test cards			SEHs		
	28			20		
	Mean	$\pm$	STD	Mean	$\pm$	STD
SEH efficiency	0.542	$\pm$	0.002 (0.28%)	0.540	$\pm$	0.003 (0.49%)
2.5 V output of DC-DC [V]	2.532	$\pm$	0.007 (0.27%)	2.50	$\pm$	0.03 (1.14%)
Output voltage at 0 A (left) [V]	1.2200	$\pm$	0.0013 (0.11%)	1.234	$\pm$	0.009 (0.73%)
Output voltage at 1 A (left) [V]	1.1566	$\pm$	0.0013 (0.11%)	1.169	$\pm$	0.009 (0.76%)
SEH turn-on current [A]	0.1121	$\pm$	0.0006 (0.50%)	0.111	$\pm$	0.002 (1.79%)
SEH turn-on voltage [V]	10.241	$\pm$	0.021 (0.20%)	10.15	$\pm$	0.11 (1.08%)
TEMP [V]	0.575	$\pm$	0.001 (0.21%)	0.567	$\pm$	0.011 (1.94%)
VMIN [V]	0.5716	$\pm$	0.0013 (0.23%)	0.563	$\pm$	0.009 (1.60%)

IV.6 Summary

Out of the 90 test cards received, 88 underwent evaluation in the described test setup. Two cards with more fundamental issues were already sorted out by the electronics team in their first inspection. From the 88 cards, 84 successfully passed the evaluation. One test card had a chip rotated by 90° , while two others had incorrectly soldered resistors, and one card had problems due to open pins in the backplane connector. Other open pins in the connector were found in the X-ray tests, but these were redundant pins, and they had no implications for the functional test. All the issues, except for the open pins in the backplane connector, have been solved by the electronics team so far. The cards concerned will stay at Aachen-1B and not be delivered to the manufacturer or to CERN. It is noteworthy that all the observed issues occurred on cards from the initial batch (batch 1). This shows that the communication with the manufacturer helped to improve the internal quality control procedure, and no problematic cards were delivered in batch 2 or batch 3.

To summarize, 84 out of 90 delivered test cards were tested successfully, and three additional cards could be repaired in house. This is a good result, but it also shows the importance of the testing procedure. The tests were only conducted at room temperature and not at the operation temperature of -35°C . These tests are also performed and reveal more issues, as presented in the next chapter.

V. Thermal quality control

After successfully conducting tests with test cards at room temperature, additional tests are carried out at different temperature levels closer to the operation temperature of the test cards. The manufacturer of the service hybrids is required to subject them to thermal cycling between temperatures of -35°C and 40°C , and consequently, the test cards must withstand these temperature extremes. Two main problems can be caused by thermal cycles. First, at colder or warmer temperatures, the electronic components, such as the microchips used in the system, exhibit different behaviors compared to those observed at room temperature. This could, for example, cause timing issues where some components operate faster than expected. The second type of problem is caused by mechanical stress.

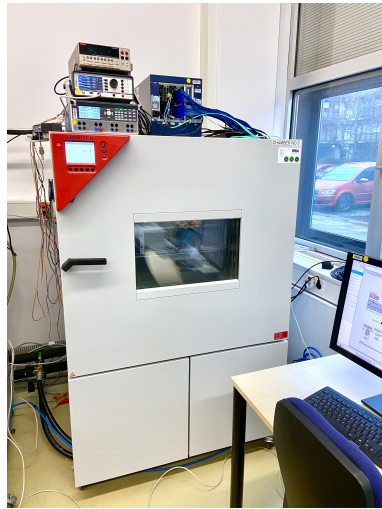
To exclude this kind of issues, a climatic chamber setup is used to test the test cards in different temperature environments. Every test card is subjected to at least eight thermal cycles. A measurement with the basic electrical and the extended DAQ test are performed at both temperature levels. For the tests, four hybrids can be used to test four test cards during one cycling. It would be possible to test up to twelve test cards in the crate, but unfortunately only four functional hybrids were available. Through previous functional testing, it has been ensured that the hybrids have a good quality, in the sense that all the tests requiring a test card are working as expected. Some cards are tested for more than 60 cycles to judge the long-term reliability of the components. Additionally to thermal cycles, a temperature ramp test is conducted on two test cards. This provides valuable insights into the temperature-dependent behavior of the measured parameters, offering a comprehensive understanding of how these parameters vary between the maximum and minimum temperature extremes for the test cards as well as for the hybrids.

It is possible to control the climatic chamber, the temperature measurement, and the DAQ test with the same program. This integration allows initiating the testing of the test cards precisely when the desired temperature level is reached. Additionally, an interlock mechanism for the measured relative humidity is included. High relative humidity with condensation on the electronic components could cause shorts and damages to the test cards or the hybrids. The next section provides a detailed description of the setup.

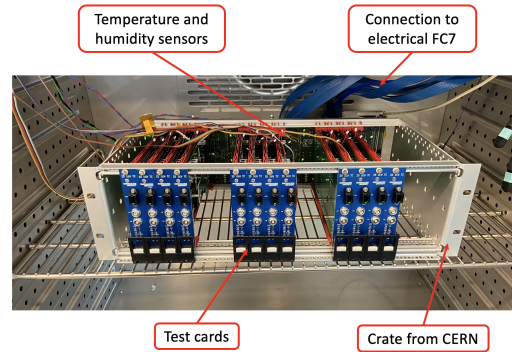
V.1 Climatic chamber setup

The central component of the setup is the climatic chamber, Binder MK240 [39]. Figure V.1 shows pictures of the full setup. The image on the left showcases the climate chamber within the laboratory. It allows for manual temperature adjustments via the display located in the top left corner of the chamber. However, to achieve integration of all subsystems within the setup, temperature settings are managed using a LabVIEW program. Section V.1.1 gives a detailed description of this. The Linux PC used for controlling the setup is visible on the right side of the picture. The climatic chamber itself allows temperatures from -40°C to 180°C with a maximal heating rate of $5 \frac{\text{K}}{\text{min}}$ [39]. These specifications are sufficient for the needs of the thermal cycles to test the test cards. The chosen temperature changes of $3 \frac{\text{K}}{\text{min}}$ avoid large damage to the electrical components due to a temperature shock but are fast enough to reduce the time needed for testing of the SEHs. Through the glass window in the door the crate can be seen, and problems indicated by the LEDs on the front panels of the test cards can be identified.

To eliminate moisture from the air, the air-dryer-unit DRYPOINT AC [40] is affixed to the rear of the climatic chamber. It is using the dry air provided by the in-house infrastructure. However, the initial dew point of this air remains too high to prevent condensation at lower temperatures, necessitating additional drying steps. The air with a pressure of 7 bar is flowing through a drying cartridge containing a specialized granulate material designed to absorb moisture from the air. This process significantly lowers the dew point of the dry air, making it suitable for use in the climatic chamber. Approximately every two minutes, as the granulate



(a) Climatic chamber setup.



(b) Crate with test cards.

Figure V.1: Figures of the climatic chamber setup and the crate inside the chamber.

material becomes saturated with water, a valve redirects the airflow to a second cartridge with the same moisture-absorbing function. In the meantime, a small fraction of the dry air is not flowing into the chamber but is used to dry the first cartridge again. This alternating procedure ensures a continuous supply of low-humidity air to the chamber.

On top of the climate chamber, all the electronic devices are positioned. The Hameg HMP 4040 power supply [34] provides the different low voltages like 3.3 V, -3.3 V, and 10.5 V. These voltages are connected to the crate and then distributed to the test cards via the FMC connectors. High voltage, reaching up to 1000 V for the HV tests, is directly connected to one front panel of the test cards. Each test card features an HV input and output, allowing for daisy-chained connections between cards and the power supply by interconnecting the output of one card with the input of the next. Short HV-protected Lemo cables facilitate this connection, with the high voltage sourced from an ISEG SHR power supply [35]. For data transmission, each test card is connected to the optical FC7 using optical fibers. The electrical FC7 is connected to the crate. A more detailed description of the electrical test setup is given in Section IV.1. The FC7s are housed inside a μ TCA crate, but the clock signal cannot be distributed via the crate's backplane. Therefore, two short cables are used to establish a connection between the clock output of one FC7 and the clock input of another. This configuration needs to be enabled in the settings of the FC7. All connection cables and optical fibers are carefully guided through openings into the climatic chamber. To prevent warm, humid air from entering the chamber, these openings are sealed with rubber plugs.

Additionally to the electronic components for the test card tests, a Keithley 2701 [41] device is used to measure temperature and humidity inside the chamber. The temperature measurement is explained in Section V.1.2.

V.1.1 Climatic chamber TCP control

The basic control of the chamber is possible with the provided software, APT-COM4 [42]. This tool is user-friendly but does not allow combined control of the chamber with the test card test system. Consequently, initiating tests at specific temperature points becomes a challenge.

To address this problem, a direct control mechanism of the climatic chamber via the TCP protocol is implemented. This involves connecting the chamber to a Linux-based PC via an Ethernet cable and addressing it using its IP address. Unfortunately, there are no common software tools for the control of the chamber available for LabVIEW or Python, so the raw Modbus [43] communication is implemented into the LabVIEW program. Modbus is a protocol for communication with different devices, and the necessary commands are given in the Binder

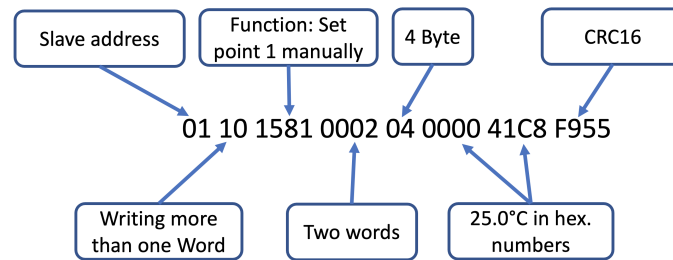


Figure V.2: Exemplary Modbus command to set the climatic chamber to 25 °C.

Interface Manual [44]. An example of a used Modbus command is shown in Figure V.2. With this command, the temperature of the chamber is set to 25 °C. To give a brief overview, the components of a Modbus command are presented. It is composed of different parts:

- One byte for the address of the receiver. The address of the climate chamber is 0x01.
- One byte to choose the function that is addressed. It is possible to read or write single inputs or whole registers.
- Two bytes to address the function. The possible functions and the translation to the hexadecimal numbers are given in the Interface Manual. Exemplary functions are "Set temperature", "Read temperature", or "Set humidity".
- Three bytes to specify the number of words and then the number of bytes used for the value sent to the climatic chamber. One word is a 16-bit sequence. These numbers have to be calculated individually for each value sent to the chamber.
- Different bytes to send a specific value to the chamber. The number of bytes is variable. To send a float number, for example, for the set temperature in the climatic chamber, the number has to be encoded in binary float notation.
- The last two bytes represent a checksum. It needs to be calculated for all the bytes sent before. Only if the checksum is correct can communication with the device work properly. The algorithm to calculate the checksum is implemented in the LabVIEW program.

The calculation is performed automatically by a developed LabVIEW script. The implemented algorithm allows for sending and receiving different temperature values to and from the device. Additionally, the humidity control of the chamber can be activated. In consequence, the control of the whole setup, including the climatic chamber, the temperature and humidity measurements, and the test card tests, can be arranged by a single LabVIEW script. This seamless integration permits comprehensive control using a single PC, and all subcomponents can be coordinated based on settings or measurements obtained from other components. Consequently, it is possible to start the test when the desired temperature is reached or to change the temperature when the DAQ test is completed.

V.1.2 Temperature and relative humidity measurement

The temperature measurement is performed with a Keithley 2700 multimeter [41]. With a specific plug-in module, it is possible to connect three temperature sensors and a HHH-4000 humidity sensor [45]. The temperature sensors are placed directly next to the test cards in the crate to measure the air temperature. The climatic chamber provides an additional temperature measurement, but the Keithley sensors are used to control the thermal cycling because they are measuring close to the test cards. The humidity sensor needs a 5 V supply voltage. The output voltage of the sensor is proportional to the measured relative humidity. A calibration is needed to convert the measured voltage to the relative humidity inside the chamber. It is explained in Section V.1.3.

During this fast increase in air temperature, the massive mechanical components like the crate respond with a temperature delay of up to 10 K and water could condense on the colder components. This was measured in a previous study with temperature sensors glued to an aluminium block with a large thermal mass. For studies with the test card, only the air temperature is measured, and a large margin in relative humidity is assumed. To maintain the dew point at least 10 K below the current air temperature, the relative humidity must be kept sufficiently low. In practice, during the cycles, the relative humidity is below 1 % and a safety interlock mechanism stops the measurement if it exceeds 10 %.

V.1.3 Calibration

To calibrate the used HIH-4000 humidity sensor, a calibrated Labkit HYGROCHIP temperature and humidity sensor is used [46]. Both sensors are positioned inside the chamber next to each other. The calibration process begins by initially heating the chamber to a temperature of 40 °C. When the temperature is reached, the Labkit sensor records a relative humidity level of 0 %. Then, the temperature is gradually reduced to −35 °C and therefore the relative humidity rises to a few percent. At intervals of 20 s, simultaneous measurements of the relative humidity with the Labkit sensor and the output voltage of the HIH-4000 sensor are conducted. The data is illustrated in Figure V.3, revealing a mostly linear relationship between the measured humidity and the HIH sensor's output voltage. For the calibration, only relative humidity less than 4 % is used because in the chamber the relative humidity is expected to be in the same range. To determine the calibration factor necessary to calculate the relative humidity from a given output voltage, a linear function is fitted to the data points. The resulting function is

$$H = 19.9 \frac{\%}{V} \cdot U - 16.0 \%, \quad (\text{V.1})$$

where H is the calculated relative humidity. The humidity is only used as a rough safety mechanism. Therefore, a detailed estimation of the uncertainty in the calibration is not necessary. During most of the test card tests, the relative humidity remains below 1 %. The calibration results are integrated into the LabVIEW script, enabling humidity measurements using the HIH-4000 sensor.

V.1.4 Temperature profile

The left side of Figure V.4 shows the temperature and relative humidity profiles for 14 thermal cycles. The temperature measurements from the three sensors are in good agreement with each other. Only one sensor is shown in the plot. Throughout the cycles, the relative humidity levels consistently remain below 1 %. In the first 50 min there is a decline in humidity. When the chamber is opened, the relative humidity is at around 30 % like in the laboratory, and has to decrease first before the rapid temperature changes can start. Additionally to the relative humidity, the dew point is shown. It is calculated with the air temperature and the measured humidity and is always below −65 °C during the cycles. Therefore, the margin between the dew point and the measured temperature is greater than 20 K, which is sufficient to avoid condensation. The dew point profile during one cycle shows two peaks for the temperature increase and decrease, a level of −80 °C for cold temperatures, and no values for warm temperatures. This can be explained by the fact that the relative humidity is measured to 0 % which would lead to a calculated dew point of $-\infty$. At approximately minute 2000, the cycling is stopped, and the temperature returns to room temperature.

For a closer examination of the individual temperature cycles, the right plot provides an amplified view of the temperature profile. The temperature is increasing and decreasing with a slope of $3 \frac{\text{K}}{\text{min}}$. The LabVIEW program controls the temperature with discrete steps of $3 \frac{\text{K}}{\text{min}}$, but in the actual measurement, a smooth temperature behavior is evident. During the cooling phase, as soon as it reaches −34 °C, the linear temperature ramp is stopped, and the chamber is set to −35 °C. A 20 min dwell period follows, allowing the temperature to stabilize at this point. At approximately 195 min the temperature reaches the expected value and stabilizes sufficiently to start the test with test cards in the crate. The different electronic tests conducted produce

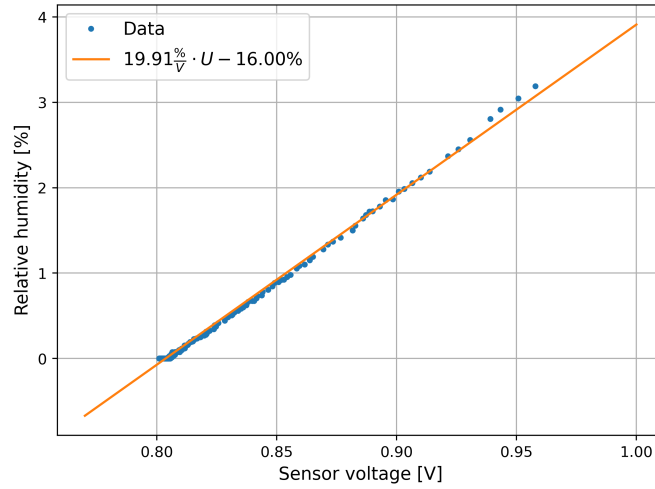


Figure V.3: Humidity calibration of the HIH-4000 sensor with a calibrated Labkit sensor.

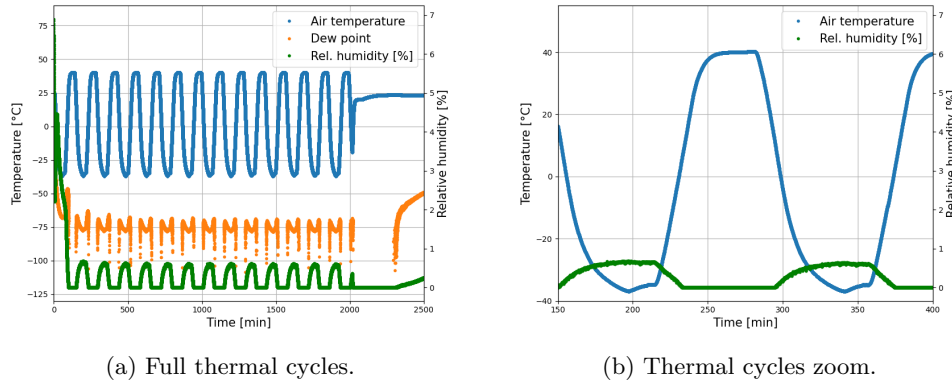


Figure V.4: Temperature and relative humidity of the thermal cycles. In total 14 cycles are measured. Additionally a zoom to show the temperature profile of one cycle is given in the right figure.

additional heat in the chamber, explaining the temperature increase at the colder level. As soon as the test concludes, the whole procedure can be repeated with heating up to the warm temperature, and a second test starts at around 260 min. This temperature profile involving two tests, both at warm and cold temperatures, defines one thermal cycle. The relative humidity at the cold temperature rises to around 0.8 %. Importantly, the dew point, while not shown in the figure, consistently remains more than 20 K below the air temperature.

V.2 Systematic test results

Similar to the quality control at room temperature, the testing process in the climatic chamber consists of two subtests. The basic electrical test, which was based on a LabVIEW script before, is now performed using a developed C++ routine. Basic electrical measurements with the test card can be performed without using a hybrid. When a hybrid is applied to the test card, additionally, a load test can be conducted. Other measurements on the test card are not influenced by the SEH. The fundamental functionality of the basic electrical test is detailed in Section IV.2.1. The second subtest is the extended SEH DAQ test, once without and once with a load current drawn from the hybrid. All the performed subtests are explained in Section III.4. To reduce the amount of time needed for the quality control of the test cards, four different hybrids are used instead of one. Among these, two hybrids feature version 0 of the lpGBT, while the other two utilize

version 1. This makes it difficult to compare the results because, as shown in Section IV.5, the measured values are dominated by the used hybrid. For the tests, the following hybrids are used:

Table V.1: Overview of the hybrids used in the climatic chamber test card tests.

SEH ID	lpGBT Version	Manufacturer	Batch
2SSEH-201000019	0	Valtronic	1
2SSEH-201000030	1	Valtronic	2
2SSEH-201000031	1	Valtronic	2
2SSEH-301000022	0	AEMtec	1

The table highlights variations in the hybrids used, encompassing differences in manufacturer, lpGBT version, and delivery batch. Despite these disparities, the hybrids remain viable for generating reliable test results in the context of test card quality control. To enhance readability, the SEH ID is abbreviated, with only the 9-digit number being used in subsequent sections. The hybrids have undergone previous testing, and those from batch 1 have some known issues. SEH 301000022 has problems with one data line on the right side and with the VTRx⁺ slow control. These issues appear on every test card and are internal features of the hybrid. Hybrid 201000019, on the other hand, presents a known issue with I^2C master 0 at cold temperatures, again stemming from the hybrid's internal characteristics. Importantly, for the purpose of test card quality control, all these known issues in the hybrids are disregarded. Therefore, the properties of the test card concerning these issues are not tested. But on no test card any similar problems occurred, and all the test cards were also tested at room temperature with a fully functional hybrid.

V.2.1 Basic electrical test

For the basic electrical measurements, no functional hybrids are needed. It allows obtaining measurements for twelve test cards within a single crate, even if only four of them are equipped with SEHs. This is an advantage because the time each test card is subjected to thermal cycles is increased by a factor of three, even if no full DAQ test is performed.

One exemplary measurement is the temperature measured by the temperature sensor T1, shown in Figure V.5. It is obtained on twelve different test cards. All of them are shown in the figure with their ID numbers. In total, 16 thermal cycles are conducted. The two different temperature levels are observable. Each data point represents the mean value derived from ten measurements, with the associated uncertainty estimated from the standard deviation. The individual temperature measurements behave quite consistently, resulting in small error bars displayed in the plot. Furthermore, the temperatures remain relatively constant across different cycles. No systematic temperature shift is evident in the figure. The warm temperature on the test card is measured to be around 40 °C, the colder temperature is −35 °C, which is equivalent to the ambient temperature. The basic electrical test is performed before the extended DAQ test. It takes around one minute, so the time is not sufficient to heat up the test card significantly.

Another illustrative example pertains to the supply voltage, U P3V3. Figure V.6 shows the measurement results for this parameter. Notably, there is a spread of approximately 10 mV among the different test cards. The individual cards show two distinct voltage levels for the different temperatures. Specifically, integer cycle numbers correspond to measurements at cold temperatures, while half-numbered cycles represent measurements at warm temperatures. For every test card, the voltage level at cold temperatures is consistently around 3 mV higher. This is a behavior observed for almost every measurement. Different temperatures have an impact on the resistance of test card components and the behavior of the used chips. This explains the dependence of the voltage and the current on the temperature. The absolute voltage level of the U P3V3 parameter is around 3.288 V, which exhibits only a slight deviation from the expected 3.3 V. The voltage is applied by the Hameg power supply in sensing mode, where additional sensing lines monitor the voltage applied to the backplane, and the set voltage is regulated to provide 3.3 V to the backplane. The small deviation of 12 mV can be attributed to voltage drops between the backplane and the test card, as well as potential inaccuracies in the measurement

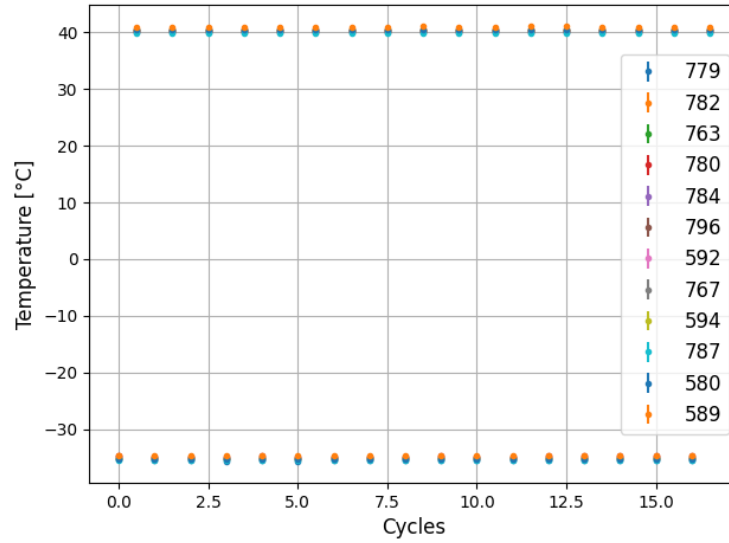


Figure V.5: Temperature measurement with temperature sensor T1 on twelve different test cards. The test card ID numbers are given in the legend.

process with the power supply or on the test card itself. However, this does not affect the functionality of the test cards.

A measurement with almost 60 thermal cycles is shown in Figure V.7. It presents the measurement of the 1.25 V voltage generated on the test card and used as a supply voltage for the I^2C communication. Again, two distinct voltage levels are evident for the different temperature conditions, with the level for the cold temperature being around 3 mV higher. For better visibility, only two test cards are presented in the plot. Among the twelve measured cards of this cycling, that are not all shown, there is a spread of approximately 10 mV around the value of 1.253 V visible, which closely aligns with the expected voltage of 1.25 V. These minor discrepancies can be attributed to variances in the manufacturing of the linear regulators that convert the voltage on the test card. The measurements took almost a week, with a single interruption in the middle. Still, the voltage remained consistently stable throughout the entire duration, with smaller fluctuations but without any significant systematic behavior. In contrast, other measurements like the voltage U P5V show a systematic drift, which is described in more detail in Section V.4.3.

The measurements collectively demonstrate that the majority of test cards perform as expected, enabling the measurement of all necessary supply voltages. Potentially problematic issues are identified and discussed in Section V.4.

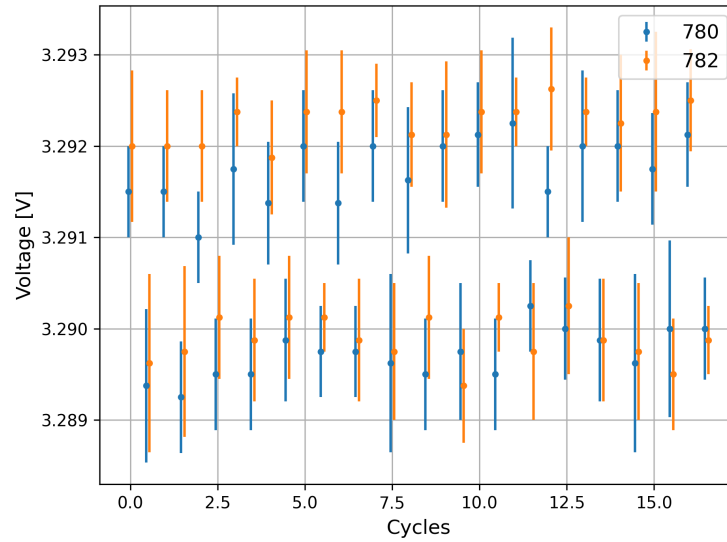


Figure V.6: Measurement of the 3.3 V supply voltage (U P3V3) on two different test cards.

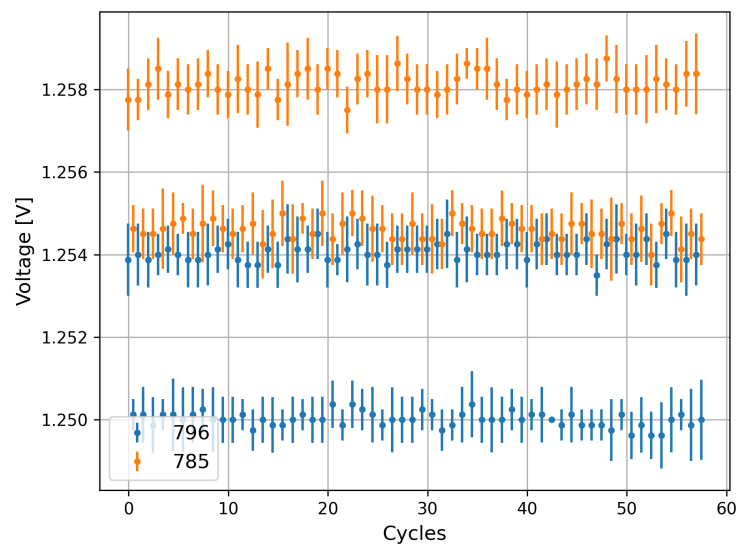


Figure V.7: Measurement of the 1.25 V voltage (U P1V25) on two different test cards.

V.2.2 Extended DAQ test

For the extended DAQ test, each test card is evaluated individually. Exemplarily, the test results for test card 780 are presented, which is tested with SEH 201000030. Figure V.8 displays the outcomes of the efficiency measurement. The red data points correspond to measurements taken at an ambient temperature of 40 °C, while the blue points represent measurements at –35 °C. It is evident that the efficiency is about 7.3 % higher at cold temperatures. This means that the DC-DC converters operate more efficiently at cold temperatures because of smaller internal resistances and more efficient chips. However, for the final grading of the test card, the efficiency must fall within a specific, narrow range. This is no longer the case for tests conducted at temperatures significantly warmer or colder than room temperature, necessitating an adjustment to the expected range, which is detailed in Section V.5.1. Within the two efficiency levels, the data points are randomly distributed across the 27 cycles. The mean and standard deviation are calculated individually for measurements at both warm and cold temperatures.

The second example is the turn-off voltage, shown in Figure V.9. Again, different voltage levels are evident. At warm ambient temperatures, the turn-off voltage hovers around 6.4 V, whereas during colder temperatures, one level emerges around 6.2 V. Two outliers fall in a lower bin at 6.0 V. These levels correspond to increments of 0.2 V by which the voltage is decreased during the test. The binning in the histogram corresponds to the same step size. The difference of the turn-off voltage between the two temperature levels is around 0.2 V. The same difference can be observed for the turn-on voltage. It's worth noting that this difference is significantly smaller in comparison to the hysteresis between the turn-on and turn-off voltage, which is approximately 3.5 V. This large hysteresis ensures that the turn-on voltage remains sufficiently distant from the turn-off voltage, thereby preventing any problematic effects with the turn-on procedure in the detector, as discussed in Section III.4.2.

Each test card is subjected to an individual analysis, with these plots generated and examined for any potentially troublesome behavior. Only two examples for one test card are given in this section. The results for all the test cards are presented in Section V.3 to provide a comprehensive view of the statistics concerning the test cards and the employed SEHs. Additionally to the measurements, all the other tests included in the extended DAQ test are performed, like the data test or the I^2C test. All the test cards perform well, and no issues are observed during these tests.

V.3 Statistical analysis

In order to gain a deeper insight into the measured results, a comprehensive analysis of all measurements from various test cards is conducted. As explained in Section IV.5 the variations between different SEHs are significantly larger than for different test cards. Therefore, the analysis has to be done for each used service hybrid individually. Exemplary results for SEH 201000030 are presented.

One example, illustrated in Figure V.10, is the measurement of the $V_{\text{Out},1\text{A}}$ output voltage of the right side of the hybrid when a load current of 1 A is drawn. As a result, two distinct levels are expected for this measurement to correspond to different temperatures because the internal resistance of the hybrid and the test card depends on temperature. The results are presented for 15 test cards using SEH 201000030. For each card, the measured values under warm and cold ambient temperature conditions are averaged, with the error bars representing the standard deviation, signifying the extent of variation between temperature levels. As expected, two levels for the different temperatures are evident. At the warm temperature level of 40 °C a higher voltage of around 1.237 V is needed to supply a load current of 1 A. This is in line with the expectation that resistance increases with warmer temperatures. At both levels, the voltages vary about 1 mV around their mean values. The difference between the two temperature levels is 23 mV explaining an increase in the internal resistance of 1.9 %. For this purpose, it was assumed that the current drawn is independent of the temperature, which was verified in the basic electrical test.

To offer a comprehensive summary of all the collected data, Table V.2 presents the average results for tests conducted both with and without load current for hybrid 2SSEH-201000030.

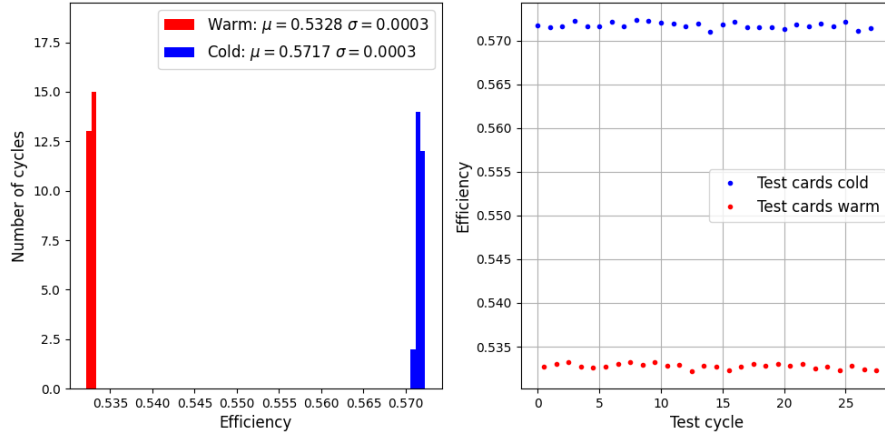


Figure V.8: Efficiency measurement at with a load current of 1 A at each side for test card 780.

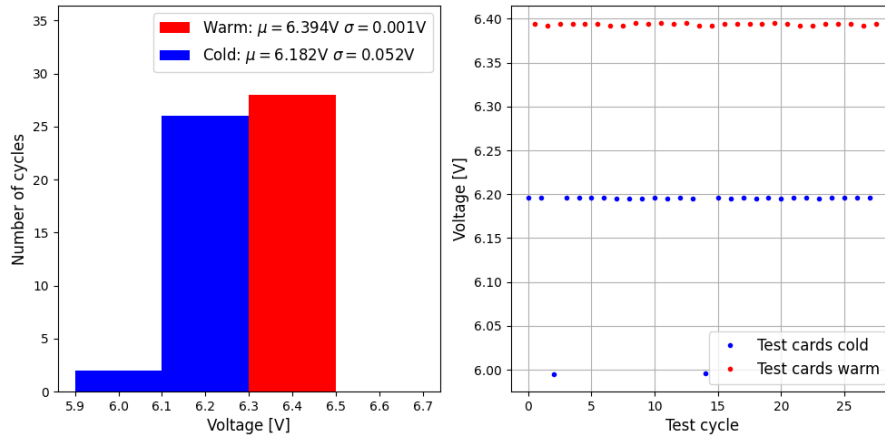


Figure V.9: Turn-off voltage for test card 780.

Not all the tests are also performed in the second extended DAQ routine with a drawn load current. Some of the parameters do not depend directly on the test card hardware. For example, the PTAT voltage is an output of the DC-DC converter on the hybrid and is measured by the lpGBT without requiring any hardware component of the test card. But the software used for the quality control is also tested, and certain software-related features are observed at different temperatures. Therefore, all the acquired values are shown in the table. A notable observation is that the ADC gain remains nearly constant for different temperatures in the test without load current. However, in the test with load current, the gain is temperature-dependent, as further detailed in Section V.5. The ADC offset remains constant at different temperatures. In contrast, for the measurements of the input voltage via a voltage divider (VMIN) and the DC-DC temperature (PTAT_BPOL2V5), a large impact of the load current is evident. The VMIN voltage decreases about 15 mV for the load test compared to the test without load. This is caused by the larger current drawn by the SEH in the case with load current, which leads to larger voltage drops in the line to the hybrid. The PTAT value increases because of the larger power converted in the DC-DC converter, leading to increased heat production.

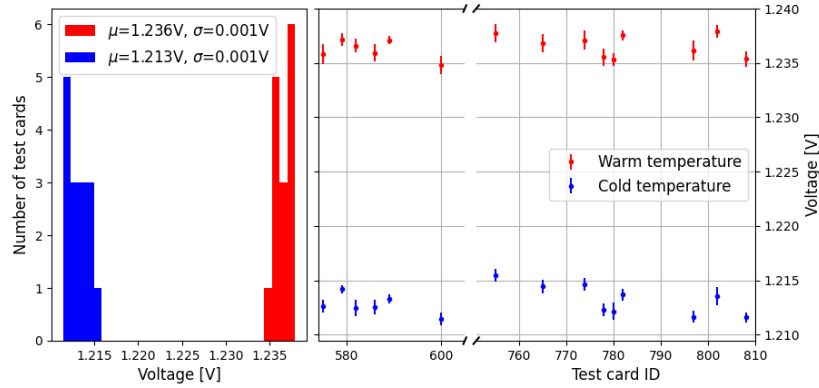


Figure V.10: $V_{\text{Out},1A}$ output voltage of SEH 201000030 with a drawn load current of 1 A. The values for all test cards that use these SEH are presented.

Table V.2: Summary of the average measured values for the two temperature levels. Measured with hybrid 2SSEH-201000030 on 15 different test cards.

Measured parameter	Cold temperature			Warm temperature		
Without load current						
Ambient temperature [°C]	−34.427	±	0.018	40.831	±	0.015
ADC gain	1.8704	±	0.0012	1.8708	±	0.0014
ADC offset	514.41	±	0.19	513.67	±	0.10
VMIN [V]	0.518	±	0.003	0.516	±	0.003
PTAT_BPOL2V5 [V]	0.553	±	0.002	0.82	±	0.04
TEMPP [V]	0.856	±	0.004	0.913	±	0.004
Turn-on current [mA]	106.2	±	0.5	116.2	±	0.3
Turn-on voltage [V]	9.83	±	0.03	10.059	±	0.010
Turn-off current [mA]	8.4	±	0.5	8.8	±	0.3
Turn-off voltage [V]	6.180	±	0.020	6.383	±	0.012
Vout_r_1A [V]	1.2131	±	0.0009	1.236	±	0.001
Vout_2V5 [V]	2.432	±	0.008	2.483	±	0.006
Efficiency [V]	0.5737	±	0.0014	0.5343	±	0.0012
With load current:						
Ambient temperature [°C]	−30.8	±	0.3	44.1	±	0.3
ADC gain	1.8716	±	0.0017	1.917	±	0.016
ADC offset	514.30	±	0.10	513.47	±	0.11
VMIN [V]	0.505	±	0.010	0.499	±	0.007
PTAT_BPOL2V5 [V]	0.542	±	0.007	1.01	±	0.04
TEMPP [V]	0.844	±	0.013	0.898	±	0.009

This set of measurements represents the first comprehensive study of various parameters measured for a hybrid at different temperatures using the test card. Most of the values align closely with the expectations obtained at room temperature. For example, the output voltages of the DC-DC converters Vout_2V5 and Vout_r_1A can be compared with the expected output voltages of 2.5 V and 1.25 V. For other values, such as the turn-on voltage, expectations are based on prior experiences with other hybrids and prototype test cards at room temperature. For some parameters, a strong temperature dependency is evident. The table serves as a valuable reference for the diverse parameters acquired with the test system, offering insight into the expected values for well-functioning test cards.

V.4 Observed effects

V.4.1 Communication fail due to missing 5 V

One of the main problems identified during the tests in the climatic chamber was due to a missing 5 V signal. The consequences on the basic electrical test are shown in Figure V.11. It illustrates the current corresponding to the 3.3 V supply voltage, and two distinct current levels are evident for different temperature conditions, measuring 1.25 A and 1.3 A respectively. One test card with the ID 777 consistently did not measure any value at cold temperatures, which is indicated by a plotted current of 0 A. After cycle 22, the test card was removed from the crate, and no measurement points were acquired after that. A second test card with the ID 783 acquired no values twice at cold temperatures. Both cards were working properly at warm temperatures. The missing measurements were a consequence of a more generalized concern with communication between the card and the PC, as it appeared that no data points were acquired. In addition to the two test cards shown, several others were found in the measurements to have similar problems.

Further investigation narrowed down the problem, and USB communication was identified as the cause. A USB-SPI bridge is required for the USB communication between the test card and the PC. It needs a 5 V supply voltage for operation. The 5 V input voltage is provided through the USB cable and is then transmitted via the backplane to chip U200 [47] on the test card. This chip acts like a switch, activating the 5 V supply when an enable signal from the micro-controller is received. The micro-controller is powered with 3.3 V, and provides the enabling signal directly after its turn-on. The 5 V voltage is necessary for the HV measurement PCB and the USB-SPI bridge. By soldering thin probe cables to different positions on the card, it became apparent that the supply voltage of 5 V for the USB-SPI bridge was missing, and therefore no communication with the test card via USB was possible. The measurement revealed that the input voltage and the enable signal were applied to the chip U200, but no output voltage was measured. The key challenge in the investigation lay in the fact that the issue could only be observed at cold temperatures. Therefore, individual measurements took a lot of time to cool down, and the test card in the chamber was not easily accessible. Various hypotheses related to soldering connections and the operation of chip U200 were examined, but ultimately proved to be incorrect.

With an oscilloscope, a time resolved measurement of the enable signal and the supply voltage of U200 was conducted at -35°C . The left side of Figure V.12 shows the results. According to the chip manual [47] the supply voltage of 3.3 V must be greater than 2 V before the enable voltage can latch the switch U200. As shown in the figure, at a time of -4 ms the enable signal was received from the micro-controller, but at this time the supply voltage was around 1.8 V, so less than the required 2 V. This discrepancy explains why the chip failed to switch, leading to the absence of 5 V distribution after chip U200 on the test card. The enable signal from the micro-controller arrived too early, demonstrating that it is functional at significantly lower voltages than initially anticipated. However, the problem was not a hardware problem but could be fixed by a new firmware for the micro-controller. A 30 ms delay was added to the software, as depicted on the right side of the figure. The enable signal is received with a delay. This adjustment could successfully solve the issue, and all the cards are working as expected at cold temperatures. This experience underscores the critical importance of quality control at various temperatures. The described issue was just at the edge of detection, and therefore it happens only at cold temperatures when the micro-controller operates slightly faster, and it affects only a subset of test cards. Without thermal quality control, this issue would have remained undetected and unsolved.

V.4.2 Problems with the USB connection

The second large issue observed during the thermal quality control was a problem with the USB communication. Some test cards failed to establish a USB connection with the PC only at cold temperatures, resulting in the test routine being aborted. This issue was visually detectable on the front panel of the test card when the USB LED remained off. The problem was observed

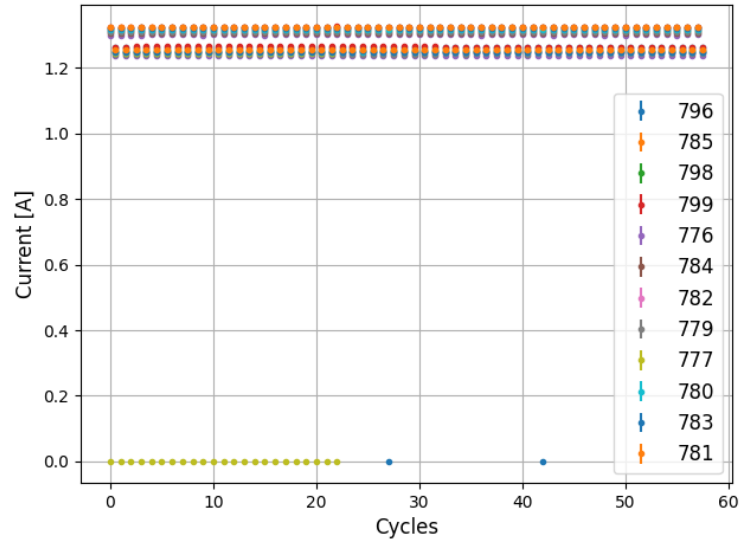
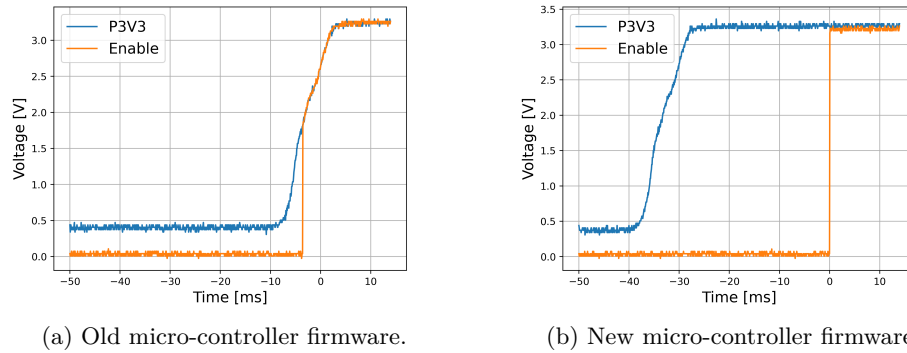


Figure V.11: Current corresponding to the 3.3 V supply voltage. Measurement of the first set of test cards.



(a) Old micro-controller firmware.

(b) New micro-controller firmware.

Figure V.12: Measurement of the enabling process of chip U200 with the old and the adapted firmware.

randomly and occurred only sometimes on some test cards, but different factors were found to have an impact. It was temperature dependent and only occurred at temperatures less than -25°C . Additionally, the waiting time between two turn-ons, the position of the test card within the crate, and the order in which the test cards in the crate started had an effect.

For each DAQ test, the results are saved into a log file. To investigate the issue with higher statistics, many tests were performed. During each test, the FC7 attempts to turn on the test card by sending a certain turn-on signal via the backplane and its buffers to the corresponding card. A software routine analyzed the resulting log files to find out if the card turned on successfully or if any problems occurred.

To further investigate the problem, the raw USB communication was monitored with the oscilloscope. This involved manipulating a standard USB cable in a way that allowed the measurement of voltage levels on the two communication lines. It was possible to see the single bits sent or received by the backplane. The voltages in the cable were cross-checked against those on the test card, and the same communication signals were measured. The signal quality was similar, and no differences were found. Therefore, to measure USB communication, it was sufficient to measure the signal voltages on the cable. On the backplane of the crate, different switches and buffers distribute the USB signal to the active test card. The Wireshark [48] program was used to analyze patterns in the USB communication and correlate them with the corresponding

USB commands being sent. When the USB connection failed, it was observable that the PC sent three identical commands addressing the USB-SPI bridge on the test card but did not receive a proper response, and the connection failed.

One difference is noticeable with cards that cannot establish a proper USB connection. During the turn-off process of the test card, the USB signal in the cable was in "reset" condition, while on the test card the signal was in "USB-suspend" mode. Both of these conditions could be detected as patterns in the raw USB communication. Therefore, the USB-SPI bridge was in "USB-suspend" mode when the test card was switched off, which was compatible with the measured power consumption of the chip. The buffers on the backplane were in a state that looked like a "reset" condition in the USB cable. The most likely theory is that due to a timing issue with the buffers on the backplane the USB bridge is in "USB-suspend" mode when the test card turns off and the buffers interrupt the connection. Then the chip gets stuck in a condition where it is impossible to communicate with it at the next turn-on process. With a sufficient waiting time between turn-off and turn-on, the problem could be solved. An additional observation is that test cards, which had a problem with the USB connection, worked well when they were inserted in the leftmost slot of each backplane. It is important to note that the crate consists of three identical backplanes, each with slots for four test cards. The different behavior in the left slot can be explained by the fact that the slot is directly connected to the USB connection without any switches or buffers.

Identifying the exact signal responsible for the problem is beyond the scope of this thesis, and further investigation would require more time and experience than was available. Most likely, an adaptation of the backplane layout would be necessary, which is not possible in Aachen-1B. The simplest solution to address this problem was to introduce a delay in the FC7 firmware. A "wait" command at the right position of the state machine allows the backplane to enable a proper USB connection to the test card before the first important USB signals are sent. The effectiveness of this firmware adaptation is demonstrated in Figure V.13. With a script, more than 40 attempts were conducted to turn on the test card. The four test cards had shown problems with the USB connection before. With the normal FC7 firmware named "old FC7 firmware", between five and 21 errors were observed when the USB connection failed during the turn-on process of the test card. With the new firmware version and an adjusted timing delay before USB initialization, the number of failures could be reduced to zero for three of the cards. The delay was increased from 500 ms to 2 s. Only the card with ID 781 continued to exhibit issues, which might be related to a distinct hardware problem, necessitating further investigation by the electronics team. For the majority of test cards, the new firmware version solves the problem, even if the exact issue during USB communication remains unknown.

During the SEH tests at the manufacturer's facility, a certain software version with a graphical user interface (GUI) is used. In this procedure, only one test with load current is conducted. Therefore, after each turn-on of one test card, the other eleven test cards are used, resulting in a sufficient time between two turn-on procedures. It was tested and found that the issue does not occur when the GUI is used.

All test cards were subsequently tested with the adapted firmware, and only two test cards experienced the USB issue. Two other cards experienced the problem just once during the cycles but will also stay at Aachen-1B.

V.4.3 Systematic drift of the 5 V voltage

Additionally to the larger issues, minor effects are also observed in the measurements. The measurement of the 5 V supply voltage for eleven cycles is shown on the left side of Figure V.14. The voltage P5V is supplied by the USB connection cable from the PC to the test card. It is measured with a certain voltage measurement chip and the micro-controller on the test card. A systematic voltage shift is evident. The voltage differs between maximum and minimum by about 20 mV. This fluctuation is not random but exhibits a systematic decrease until cycle four, followed by an increase. The behavior is observed across all the test cards simultaneously. All the other measurements in the basic electrical test show a constant behavior over all the cycles. Only the P5V voltage is systematically changing during the cycles, which can be reproduced in many measurements.

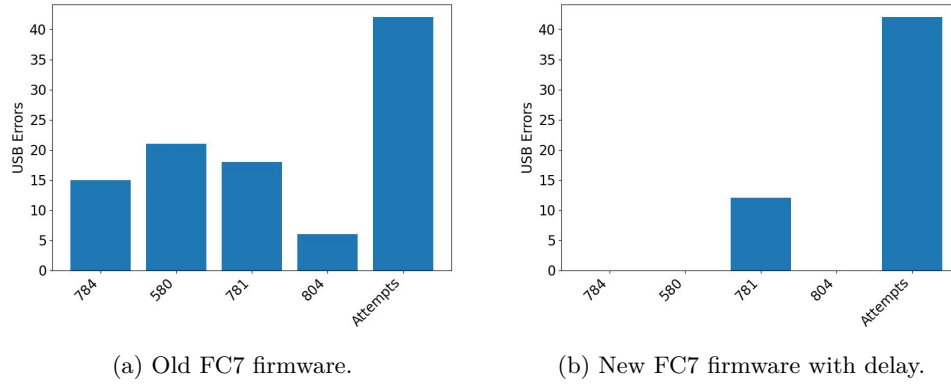


Figure V.13: Comparison of the number of problems with the USB connection for different test cards with two firmware versions.

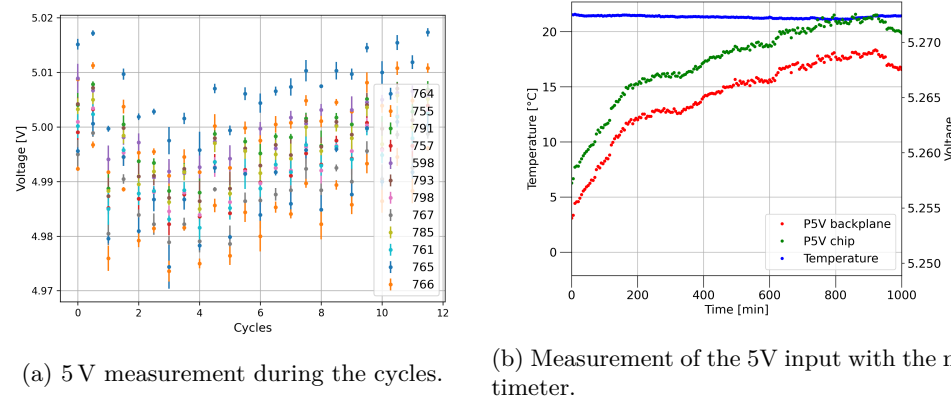


Figure V.14: 5 V supply voltage at the test card measured for a longer time to observe a systematic behavior.

While this effect is not indicative of a test card failure, it remains an interesting phenomenon for investigation. To further examine it, a second measurement is conducted, in which the P5V voltage is directly measured on the test card using thin probe cables. It is measured close to the backplane connector, allowing for the acquisition of the actual 5 V input voltage supplied by the PC and distributed via the backplane to all the test cards. This explains the consistent measurements for all twelve tested cards. The measurement with the multimeter is conducted for 1000 min overnight and is shown in the right plot. "P5V backplane" corresponds to the voltage measurement close to the backplane connector. "P5V chip" is the voltage after the chip U200, which switches the voltage, as described in Section V.4.1. Both voltage measurements exhibit a consistent difference of around 3 mV but display the same systematic behavior. The voltage is not constant but increases until minute 920 before decreasing. To exclude temperature-dependent effects, the temperature is also shown in the figure. It varies about less than 0.5 K during the night and should not have an impact on the voltage measurement. The difference between the maximum and minimum voltage is around 15 mV, which is consistent with the measurement on different test cards using the micro-controller shown in the left figure. This observation demonstrates that the physical voltage distributed from the PC is not constant, but fluctuates by around 20 mV when measured over several hours. While this finding is not a cause for concern, it does provide an explanation for the systematic results in the measurement of P5V.

V.4.4 High voltage tests

During the analysis of the high voltage tests, an additional feature came to light. One result of the HV connection test displayed in Grafana for test card 588 is shown in Figure V.15. This figure showcases the measured voltage plotted against the voltage applied by the high voltage power supply, with orange and blue data points corresponding to the two HV connections between the SEH and the test card. The expected curve is diagonal with a slope of 1, and the data points should lie within the narrow green band for a successful test. It is evident that the data points for the connector J7 are shifted to higher set voltages and do not align with the expectation band, and the test fails.

It has to be investigated why the data points are shifted to the right, although the high voltage connection is good. Similar problems with all the data points shifted towards higher set voltages can be observed on three test cards. The effect can be attributed to a timing issue within the micro-controller. When the external high voltage is set by the power supply, the delay until the measurement is started is insufficient. The timeout loop in which the micro-controller acquires values has a period of around 1 s. There is no synchronization between the measurement and the readout. When the power supply sets the voltage and the micro-controller is immediately called upon to measure the voltage, it is possible that an older voltage value from the preceding loop cycle remains in the buffer and is subsequently recorded. This explains why the data points are shifted to the right for certain tests. The slope of the data points remains as expected, only the offset changes. The same issue can happen with an individual point, resulting in a plot where a single point is shifted by 200 V to the right. The problem could be solved by adding a delay in the software after setting the voltage. With a delay longer than the loop period of the micro-controller, the problem is solved successfully. It results in a test time that is a few seconds longer.

V.5 Temperature dependency

To get a better understanding of the temperature dependency of the different measurands a thermal ramp test is performed. Instead of cycles between a warm and cold temperature level, the temperature is gradually increased from -40°C to 40°C in steps of 5 K. While the previous measurements with thermal cycles (as described in Section V.2) reveal different measurement levels for warm and cold temperatures, the temperature ramp allows for a detailed analysis of the behavior between these two levels. The observables show only small, if any, dependencies on the temperature. Most of them are very linear. The results can be compared to measurements with a module within the climatic chamber (Section VII.3.3) later. Figure V.16 shows the temperature profile. The plot displays the three temperatures measured by three different sensors. The discrete temperature steps of 5 K are clearly visible in the chart. Each time the temperature reaches a constant level, the same quality control tests that are used during the cycles are conducted. All the presented results are acquired with SEH 201000030 and test card 577.

The first example of a temperature depending behavior is the gain of the ADC calibration. It is shown on the left side in Figure V.17 and is measured while a load current is drawn from the hybrid to ensure comparability with results obtained on a module tested at different temperatures. Up to temperatures of 20°C , the gain factor remains relatively constant at approximately 1.871, with only a single outlier. The temperatures shown in the figure are not the set temperatures but the temperatures measured on the test card at the beginning of each test. Therefore, it is named "Start temperature" and is, in general, a bit higher compared to the set ambient temperature. For temperatures warmer than 20°C , the gain factor begins to rise until it reaches a value of more than 1.92. This rise in the gain factor is necessary to be taken into account to avoid a dependency of the ADC measurements on temperature. Thereby, the results for ADC-dependent measures like the input voltage VMIN are very constant. The results are in good agreement with the measurements on a module, as described in Section VII.3.3.

During the test card quality control, the thermal ramp ensures proper operation over the full temperature range. A more comprehensive analysis, featuring different approaches, is conducted with a module and is presented in Section VII.3.3.

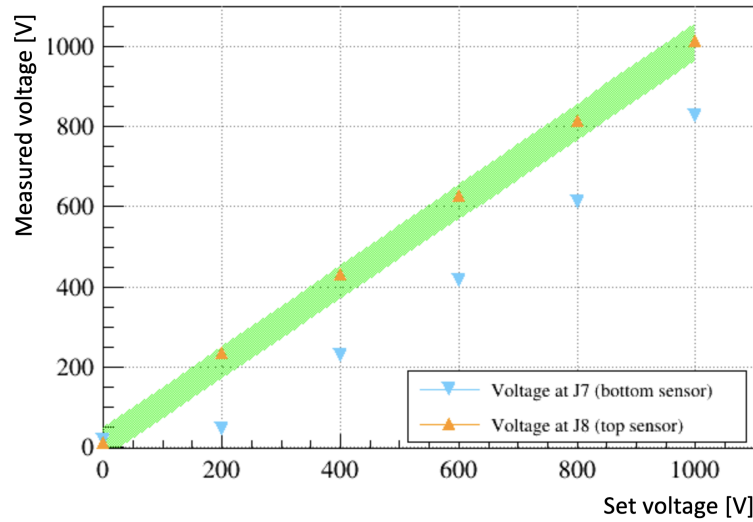


Figure V.15: Grafana result for the HV test for test card 588 with the used SEH 201000019.

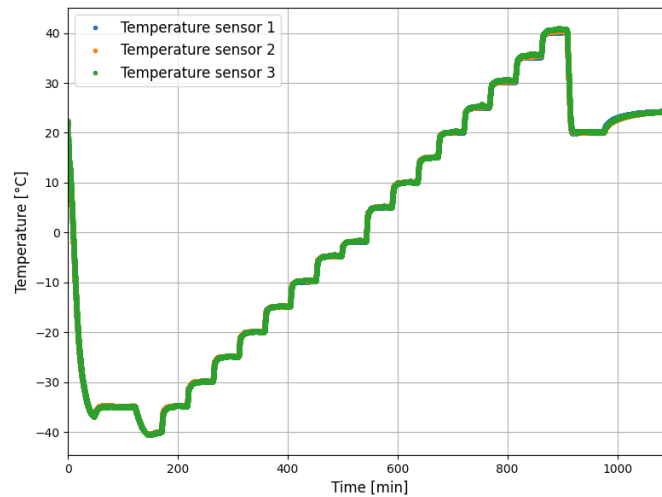


Figure V.16: Temperature profile for the temperature ramp.

V.5.1 Temperature dependence of the efficiency

The second example to highlight is the evaluation of the efficiency. During the analysis of the test card tests, it was observed that the efficiency tests failed. As explained in Section III.4.1, this test involves the calculation and plotting of efficiency for various drawn load currents. Figure V.18 illustrates the plot of the efficiency for different output currents of the hybrid for a temperature of -35°C . The test only passes if all red data points corresponding to efficiencies calculated for different total output currents fall within a predefined empirical range. The efficiency at colder temperatures is higher compared to measurements at room temperatures, and therefore the data points lie above expectations and the tests fail.

Therefore, the expectation region used for the grading of the test has to be adapted for different temperatures. In the analysis script, a fifth-degree polynomial, which was fitted to previous measurements, is used for the grading region. It is shown on the right side of the figure. The calculated efficiency points have to fall within a region of $\pm 2\%$ around the polynomial. The data points at room temperature align well with the red curve, while at colder temperatures, the efficiency surpasses the curve, and at warmer temperatures, it falls below it. The bottom

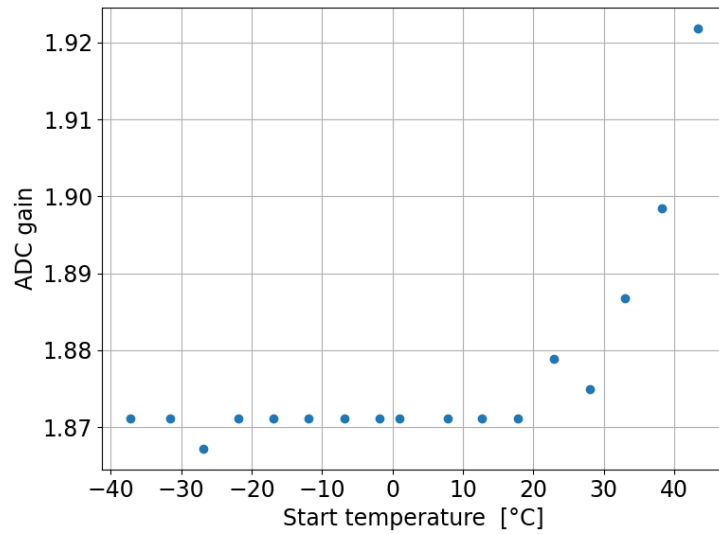


Figure V.17: Temperature dependend measurement of the ADC gain for SEH 201000030 on test card 577.

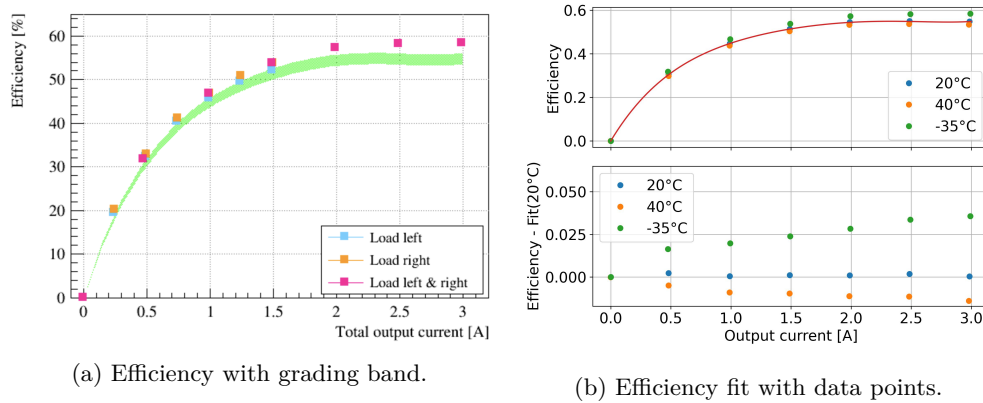


Figure V.18: Efficiency measurement with the green band used for the grading in Grafana (left) together with the polynomial and data points at three different temperatures (right). The measurement is conducted on test card 577 with SEH 201000030.

plot displays the residual, illustrating the difference between the measured efficiency and the polynomial. The discrepancy exceeds 2 % of the absolute efficiency in certain cases.

To improve the analysis and extend it to different temperatures, the fit of the efficiency has to be adapted. With the temperature ramp, the exact behavior can be determined. Figure V.19 shows the efficiency for a total load current of 1 A measured at various ambient temperatures. It exhibits a linear dependence on temperature. This behavior can be attributed to higher internal resistances and less efficient operation of the BPOL chips within the DC-DC converter at warmer temperatures. The linear dependence allows for the determination of the slope via linear fitting. The right plot in the figure shows the determined slope for various load currents. The obtained values are not perfectly linear, but it is still useful to fit a linear function to the data points. The dependence on the load current is a second-order effect, and therefore, a rough determination of the dependency is sufficient. This method enables the characterization of the efficiency's dependency on both temperature and load current.

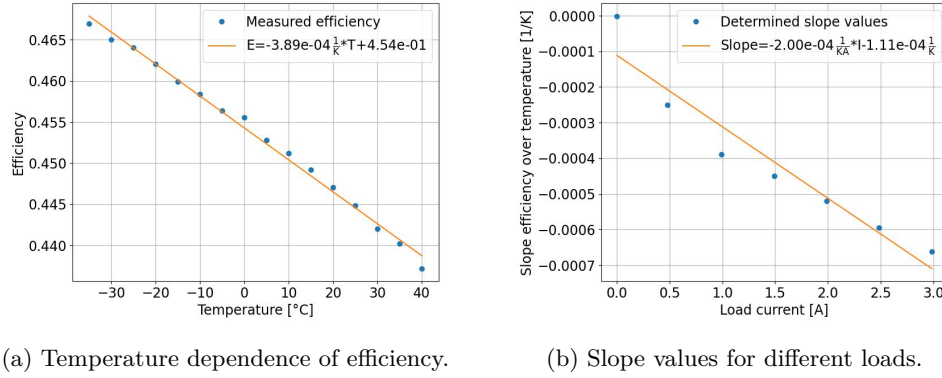


Figure V.19: Determination of the dependency of the efficiency on the temperature and the drawn load current. The left plot shows the temperature dependency of the efficiency for a total load current of 1 A. On the right, the determined slope values for different load currents are shown.

The used polynomial of grade five can be adapted by a correction factor. This factor includes the actual temperature and the load current:

$$\eta = P_5(I) + (T - 293 \text{ K}) \cdot (-2 \cdot 10^{-4} \frac{1}{\text{AK}} \cdot I - 1.11 \cdot 10^{-4} \frac{1}{\text{K}}), \quad (\text{V.2})$$

where η is the efficiency and $P_5(I)$ describes the polynomial of grade 5 determined at room temperature. The formula incorporates the difference between the actual temperature and the reference temperature (room temperature, 20 °C), at which the polynomial was initially determined. This difference is then multiplied by the slope, which depends on the load current (I) and is determined in Figure V.19.

Figure V.20 presents the result. The adapted efficiency function is compared to measured data points at different temperatures. For each temperature, an individual efficiency curve is plotted. The data point for an output current of 0 A is excluded from this analysis, as the efficiency is by definition zero at this point. The adapted curves fit very well at the different temperatures. In the bottom plot, the residual is presented for all three temperatures. The maximum difference between a data point and the corresponding fit is 0.005 for a temperature of -35 °C. The dashed black lines represent the 2 % acceptance region for a successful test result, with all data points falling within this range.

These results enable effective tests of efficiency across different temperatures. The outcomes are evaluated with different test cards and hybrids at cold and warm temperatures, and all the measurements pass the test.

V.6 Impact of thermal cycling

To assess the impact of multiple thermal cycles on the test cards, tests are repeated at room temperature, using the same setup as for the initial quality control, to make the conditions comparable. Specifically, a random sample of nine test cards that had previously undergone successful testing in the climatic chamber with 58 cycles is retested under room temperature conditions. The used hybrid is the same one with ID 201000045, allowing to investigate whether any changes had occurred in the test cards during the cycling.

The comparison between the efficiency measurements taken before and after the thermal cycling is presented in the left plot of Figure V.21. The efficiency is measured for the nine test cards before the thermal cycling (blue) and after the cycling (red). For all the cards, the efficiency is higher after the cycling. However, the maximum difference in efficiency results, which are observed for test card 776, amounts to just 0.8 %. This difference is small and can partly be explained by the different ambient temperature. Differences in cooling conditions resulting from the manual placement of the cooling fan during both sets of measurements. However, as shown

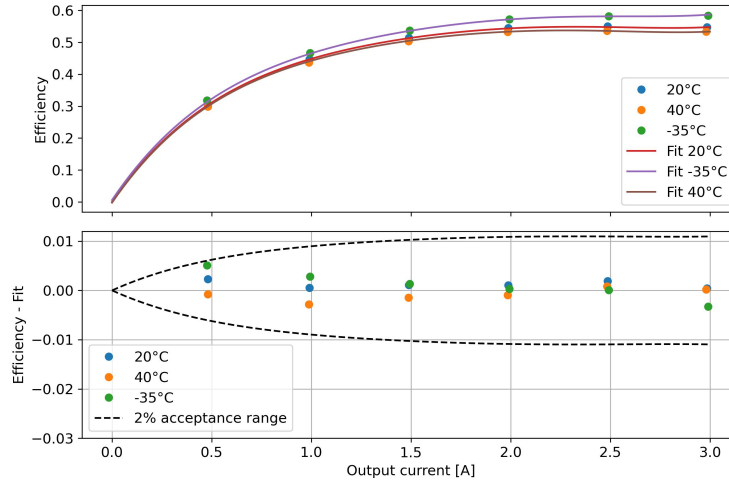


Figure V.20: Adapted expected efficiency curves for different temperatures together with the measured efficiencies. The bottom plot shows the residual between the data und the curves.

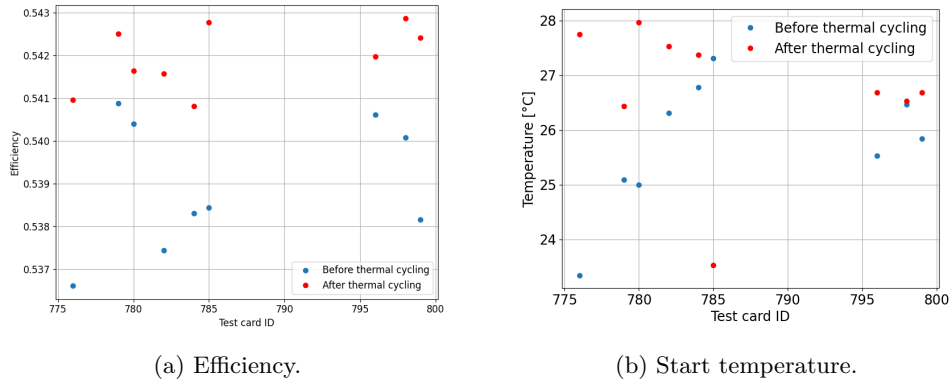


Figure V.21: Comparison of the efficiency and start temperature measured on nine test cards before and after the thermal cycles.

in the right plot, the correlation with the start temperature is not perfect. The temperature is measured directly on the test card. The temperature difference between tests before and after the cycling is up to 4.4 K for test card 776. The small differences in the efficiency results are also influenced by statistical variations between the measurements. No significant differences indicating a change on the test card can be seen.

In Figure V.22, the turn-on voltage is shown. Differences of up to 36 mV for test card 780 are evident in the plot. This corresponds to an increase of 0.35 % compared to the tests before the thermal cycling. Compared to the fluctuations between different hybrids, which are 1.08 % for the turn-on voltage, this is a small effect. All the measured observables show differences between the measurements, but compared to the variation between different hybrids, they are negligible.

In general, the comparison of the results measured before and after the cycles is successful. Despite the efforts to keep testing conditions as consistent as possible, minor differences arise due to factors like ambient temperature and cooling, as well as statistical fluctuations. The various binary tests, like data integrity tests or I^2C tests, were also conducted successfully. All used data lines, chips, and buffers withstand the thermal cycles. Phase and word alignment work properly, I^2C connections to the FC7 are possible, and all the necessary reset signals are measured correctly. Even after a large number of 58 cycles, no damages or problems could be observed on the test cards. It is essential to recognize that the nine analyzed cards represent a random sample from the pool of test cards produced.

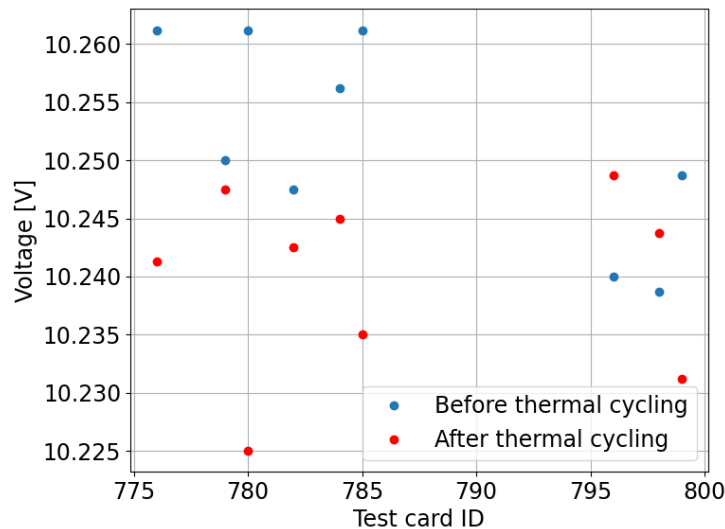


Figure V.22: Comparison of the turn-on voltage measured on nine test cards before and after the thermal cycles.

V.7 Results and conclusion

The tests with thermal cycles are an important part of the quality control procedure for the test cards. In total, 67 test cards were tested in the climate chamber. The results for the 90 test cards produced in total are summarized in the following enumeration:

- 20 test cards were already delivered to CERN in May 2023
- 3 test cards are not tested with thermal cycles due to problems observed in the first quality control
 - 2 test cards never turned on, no ID was fused
 - 1 test card has problems with the electrical connection
- 67 test cards underwent thermal testing in the climatic chamber
 - 60 test cards show a good quality
 - 3 test cards are tested successfully but have open pins observed in the X-ray test
 - 2 test cards can not establish a stable USB connection
 - 2 test cards had a USB connection failure once

These results demonstrate an overall yield for the test cards tested in the climatic chamber of 93.8%, whereby only 64 test cards with good quality are included. The test cards with issues observed with X-rays were tested in the climatic chamber but are not included in the statistics because they will not be delivered to CERN. In general, the quality control is successful, with relatively few hardware-related issues identified. The four test cards with USB connection problems have to undergo further investigation to narrow down and solve the problem. Also, the cards already delivered to CERN perform well within the test system. The most important achievement of the thermal quality control is the improvement of the test procedure. Two major problems were found, concerning a missing 5 V input signal and USB communication problems. These issues, if left unaddressed, could have caused significant problems during the hybrid tests. Their resolution is achieved through the adaptation of firmware for the micro-controller and the FC7. Additionally, minor issues concerning the test software for the HV tests were found and solved. The testing process provides valuable insights into operating in the climatic chamber and

the test system, allowing for system improvements and the sharing of experiences with colleagues at CERN. In conclusion, the quality control of the test cards has been successfully completed, and a total of 60 test cards are now ready for delivery to CERN.

VI. Voltage drops on the FEHs

VI.1 CBC, CIC, and VTRx⁺ power supply

Within the module, the SEH is responsible for supplying power to the front-end hybrids. The bPOL2V5 DC-DC converter generates a voltage of 1.25 V, and the SEH distributes it via the front-end connectors to the hybrids. The voltage is named P1V25. It is essential for the CBC readout chips and the CIC concentrator chips. Furthermore, the SEH also distributes the electrical ground to the FEHs. Due to the internal resistance of the wires, voltage drops occur between the DC-DC converter and the front-end chips. Therefore, the CBC near the SEH receives a higher voltage compared to the CBC on the opposite end of the module. In addition, the P1V25 supply voltage is also applied to the VTRx⁺, which is much closer to the DC-DC converter compared to the front-end chips. Additionally, the first-stage DC-DC converter provides 2.5 V (P2V5) for the VTRx⁺.

All the components have specified supply voltage ranges that need to be fulfilled. For the CBCs the supply voltage should be in a range of 1.08 V to 1.32 V; for the CIC it should be between 1.2 V and 1.32 V. The VTRx⁺ component requires two different voltages, falling within the ranges of 2.25 V and 2.75 V as well as 1.1 V and 1.3 V [49]. To ensure compliance with these specifications, it is important to quantify the voltage drops occurring along the wires to the various components. Additionally, the current flowing within the module has an impact on the voltage drop. According to Ohm's law, with larger currents, the voltage drops in the wires increase. Therefore, it becomes essential to assess the module's state when the drawn current is at its maximum. This ensures that the voltage meets the specifications of the components at any power configuration of the module.

VI.2 Module voltage measurement setup

The used module has the CERN ID 2S_18_5_AAC_00002. For the operation of the module, a large metal box is used. The module, mounted on a carrier plate, can be placed inside. All the wires and connections, as well as a small fan for cooling, have enough space in the box. The case is necessary to avoid light shining on the module. If high voltage is applied to the sensor, light would cause a large leakage current and could damage the sensors. This makes electrical measurements on the hybrids during operation a bit more difficult because it is not possible to access the module.

To operate the module, two power supplies are used. The 10.5 V low voltage is provided by a Hameg HMP 4040 power supply [34]. With the same device, the current is measured with a Python script. The bias voltage of 350 V is supplied by a Keithley 2410 source meter [41]. Via the two optical fibers, the module is connected to an FC7 [29] to enable the data communication and the readout. The module can be controlled by the *Ph2_ACF* software tool developed by the tracker DAQ group [50]. The voltages are measured with a multimeter with thin probe needles. They are placed to the different positions by using flexible holders.

VI.3 Measurements and results

VI.3.1 Power consumption of the module

The voltage drops on the wires are maximized for maximal current, and therefore it is important to find a state of the module with maximal power consumption. The power consumption depends on three different aspects, the occupancy, the high voltage, and the tuning.

The occupancy is the ratio of detected hits to the number of transmitted trigger signals. The CBCs convert the analog voltage signals to binary values. For this, a programmable threshold

is used. If the voltage signal is above the threshold, a hit is detected. The threshold is given in V_{Cth} -units. For a Gaussian noise in the strips, some voltage values are above the given threshold, and hits are detected. With increasing V_{Cth} -units, the physical voltage threshold decreases, and more noise hits are detected. The measured occupancy curve for a threshold scan is named S-curve which is mathematically represented by an integrated Gaussian distribution. The width of the S-curve represents the noise level. For each threshold value, the occupancy is measured ten times, and the mean and standard deviation are calculated. The occupancy has an impact on the power consumption of the module. Digital chips have a higher power consumption when the internal transistors are switching from 0 to 1 or vice versa. For an occupancy of 50%, the pedestal requires a maximum number of transistors to switch, so it is expected that the power consumption is maximal at this occupancy.

The second effect is tuning. The CBC sets a global threshold for each channel. Because of small differences in the channels, a global threshold does not hit the pedestal for each channel. Therefore, the voltage signal for a channel is amplified by an individual gain factor. Depending on the settings, the default gain factors (tuning values) can be used, or new tuning values can be determined on the module. This has an impact on the power consumption because the exact pedestal point is only hit for each channel if the channels are tuned. Otherwise, some of the channels are not working at the 50 % occupancy point, and the chips do not operate with maximum power consumption.

The third factor is the high voltage, which can be on or off and has a small impact on power consumption. But the sensor must be depleted to reduce the electrical noise in the strips, which results in steeper S-curves. In the detector, the module will be operated with an applied HV. For the measurements with high voltage, a 350 V voltage is applied to the sensors. The measurement of the low voltage input current depending on the three aspects is shown in Figure VI.1. One can see that the highest current is reached at the pedestal. The applied high voltage results in S-curves with a smaller width, and the resulting current curves also become around 75 % more narrow and around 10 % higher in the case with the default tuning compared to measurements without high voltage. As shown in the figure, the maximal current is reached for a state when using default tuning values with HV on at the pedestal. For measurements with high voltage (the right plot), one can compare the effect of using newly determined tuning values. The height of the current curve at the pedestal compared to the base level at 400 V_{Cth} is around 90 mA for both tuning values, but the base level with the default tuning values is around 80 mA higher.

The configuration with HV on and default tuning is one of the states of the module chosen for the measurements of voltage drops. The threshold is set to 595 V_{Cth} . Other aspects of these measurements, like different current base levels, are beyond the scope of this analysis because only the highest current is of interest.

VI.3.2 Measured voltage drops

For the measurement of the voltages, three different states of the module are used. A first state with minimal activity is the state directly after the turn-on of the module. The second state, "ready for data taking", is a state when the module is configured and ready for data taking. The third state is the state with maximal power consumption. This state is named "max. activity". The different measurement points used to measure the voltages on the module are presented in Figure VI.2. The different points are labeled with capital letters. The results for the measured voltages at all the seven points for the three configurations are shown in Table VI.1. The uncertainty caused by the positioning of the needles is estimated by placing the needle 10 times at the same position and calculating the standard deviation. It is around 1 mV. All the other uncertainties, like the resolution of the multimeter, are much smaller.

The measurement points A and B are the output voltages of the two DC-DC converters on the service hybrid. They are close to the specifications of 2.5 V and 1.25 V expected for the two DC-DC converters, and there are no large voltage drops occurring between the DC-DC converter outputs and the measuring points.

At point C, the input voltage of the module is measured. It is smaller than the applied 10.5 V at the power supply because there are some voltage drops on the wires to the module. This voltage drop depends on the drawn current, so higher currents should cause larger voltage

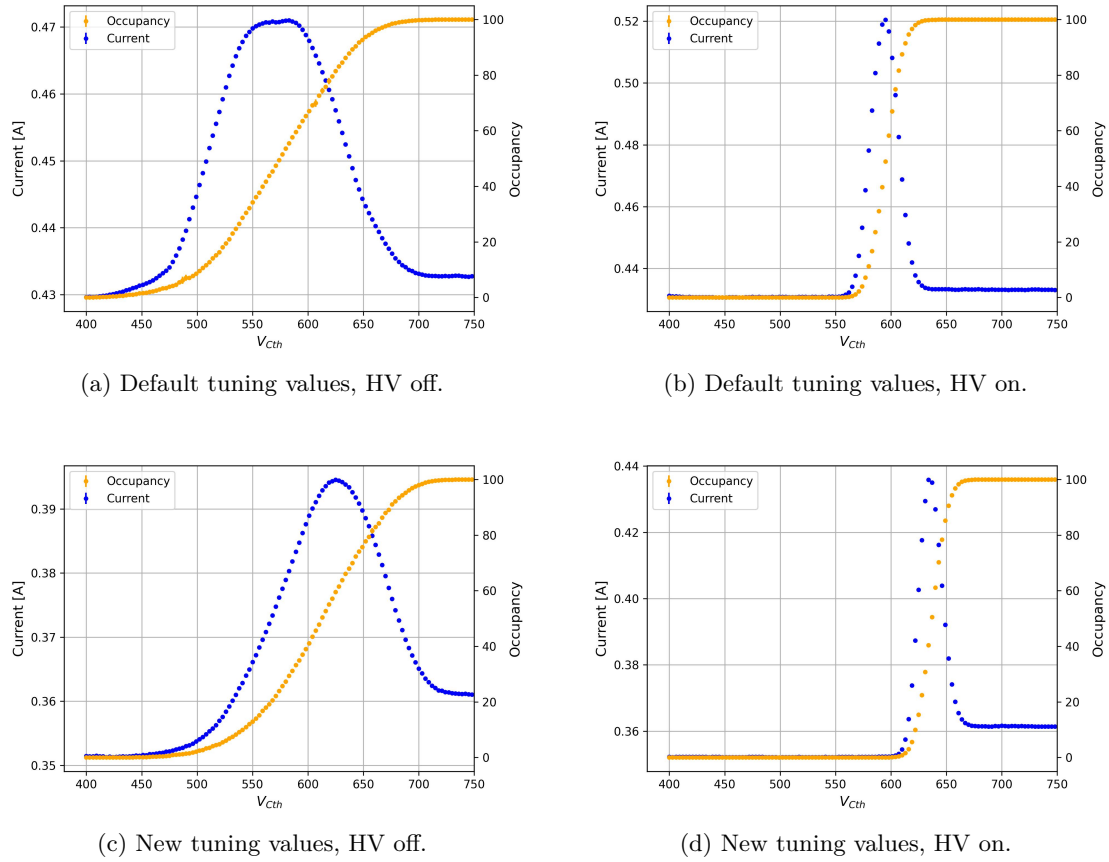


Figure VI.1: Measurement of the module current and the occupancy for different threshold values. The height of the current depends on the applied high voltage and the tuning.

drops and therefore smaller voltages measured at point C. It is worth noting that the voltage for the configuration "ready for data taking" is a bit higher than for "max. activity", although the voltage drop in the wires to the module should be higher for the "max. activity" state. This could be explained by a connection problem, maybe caused by a bad mating contact, but it has no impact on the measurements of the voltage drops on the module.

At points D and E, the voltage is measured against electrical ground at two pads on the front-end hybrids, on the side, with a maximal distance to the service hybrid. So, it is the maximal voltage drop on the FEHs. Now it is possible to compare the measured voltages with the specifications of the chips. For the CBCs, the voltages are well within the specifications. For the CIC, the voltage should not be below 1.2 V. There is a voltage of 18 mV below the given specifications for the module configuration, with maximal activity at the end points of the FEH. But the chip is mounted in the middle of the FEH and therefore the voltage drop there should be smaller than at the end of the FEH. It can be estimated that the CIC is placed at $\frac{2}{3}$ of the distance between point B and point E. Therefore, by assuming equal voltage drops on each line, the voltage for the CIC corresponds to $1.238 \text{ V} - \frac{2}{3}(1.238 \text{ V} - 1.182 \text{ V}) = 1.201 \text{ V}$, and the specifications are fulfilled at the CIC position. Even if the margin is relatively small, all CICs are working at each module condition. For the "min. activity" configuration, the measured voltage at point D is higher than the voltage directly on the service hybrid. This difference is in the order of 2 mV, which can be explained by measurement tolerances. Also, it can be observed that the voltages at point E on the left FEH are smaller than at point D on the right FEH. This is caused by voltage drops on the SEH. The lines from the DC-DC converter to the left FEH are much longer, and consumers like the lpGBT and the VTRx⁺ are supplied from the same line.

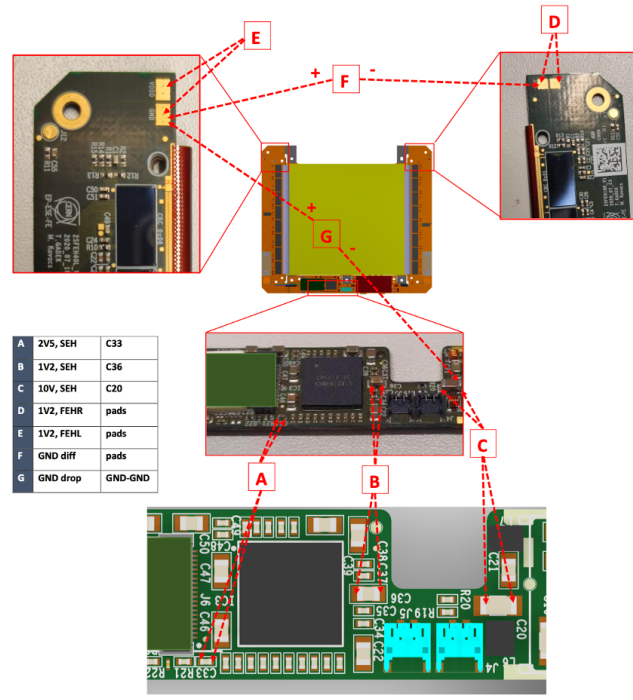


Figure VI.2: Measurement points for voltage drops on the 2S module hybrids [49].

Table VI.1: Voltages measured at the given points given for the three different module configurations with a supplied low voltage of 10.5 V. Additionally, the measured module current is shown.

	Min. activity	Max. activity	Ready for data taking
Input current	283.2 mA	516.8 mA	438.7 mA
Point A	2.529 V	2.526 V	2.527 V
Point B	1.263 V	1.238 V	1.245 V
Point C	10.30 V	10.274 V	10.170 V
Point D	1.265 V	1.236 V	1.245 V
Point E	1.237 V	1.182 V	1.197 V
Point F	0.003 V	0.005 V	0.005 V
Point G	0.011 V	0.024 V	0.020 V

At points F and G the voltage differences at different points of the electrical ground are measured. For point F it is measured between the right and left FEH. It is in the order of 5 mV, and can be explained by the fact that the electrical ground lines to the left FEH are longer and the $VTRx^+$ and $lpGBT$ are connected to the same lines on the SEH. The used prototype module is not equipped with a ground balancer. The voltage drop on the ground lines for measurement G is between the opposite side of the left FEH and the point on the SEH where the electrical ground is connected to the power supply. It is in the order of 20 mV because of current flowing over the ground line to the SEH.

The measured voltages are for all the chips within the specifications. It was shown that for every possible module state, the output voltage on the SEH was chosen correctly to supply the chips. The actual chosen output voltage at the BPOL2V5 results in a voltage for the CIC at its lower limit. Therefore, output voltages at the DC-DC converter should be in the range of actual 1.238 V and 1.3 V to avoid an overvoltage at the $VTRx^+$. Other groups performed the same measurements on other modules and confirmed the results.

VII. Thermal studies with a 2S module

After successful tests on service hybrid test cards within the climatic chamber setup, the setup was adapted to judge a module's performance under different thermal conditions. The primary objective is to evaluate the performance of the service hybrid within the module. Many of the parameters measured for the SEH on the module are also assessed on the test card. The behavior of the hybrid in the environment of a module can be compared with the SEH behavior on the test card at different temperatures. An ADC calibration equivalent to the procedure on the test card is performed, and the calibration parameters like gain and offset are analyzed. Additionally, the turn-on and turn-off voltages and currents are measured and will be compared to the measurements on the test card. Other measurements made on the module were not possible on the test card, like the sensor temperature or AMUX values from the front-end hybrids. Section VII.2 describes all the measurements in more detail.

Three different types of test are conducted with the module. First, the module is subjected to thermal cycles in a manner similar to the test card tests to observe how it responds to thermal stress. Second, by increasing the temperature in steps of 5 K before each test, the temperature dependence of the measurement parameters can be estimated. This temperature ramp provides more insights compared to thermal cycles because, with cycles, only measurements at the lower and upper temperature levels are possible. To assess the impact of temperature cycles on the module's performance, noise scans are conducted both before and after the thermal cycles. This measurement proves if thermal stress has an impact on the noise level of the whole module or of single strips, which could have a worse electrical connection after cycling.

Because the focus in the thermal measurements is set to the SEH behavior and the lpGBT slow control, no FEH readout is conducted in the climatic chamber. There is no high voltage applied to the sensors, so a light shielding of the climatic chamber is not necessary. This comprehensive evaluation will provide valuable insights into the SEH's behavior within a module under varying thermal conditions.

VII.1 Test setup

The basic structure of the setup is already used for the thermal test card tests and described in Section V.1. The temperature is alternating between 40 °C and −35 °C. These temperature levels are designated as warm and cold temperature. An identical temperature profile as outlined in Section V.1.2 is used, and 22 thermal cycles are conducted. The slope of the temperature increase is $3 \frac{\text{K}}{\text{min}}$, and at each temperature level, the waiting time is sufficient to allow for the temperature to stabilize before initiating the module tests.

The module is mounted on a carrier plate and placed inside the climatic chamber. Specific information about the module, the used components, and their IDs are given in Table VII.1.

Table VII.1: Specific information about the used module.

Module ID	2S_18_6_AAC-00004
FEH Left	2SFEH18L-301000053
FEH Right	2SFEH18R-301000007
SEH	2SSEH-201000043
Assembling date	15.05.2023

Equivalent to the test card setup the 10.5 V low voltage is supplied by a Hameg HMP 4040 [34]. The module inside the climatic chamber is shown in Figure VII.1. It is connected to the FC7 [29] via an optical fiber to control and readout the module with an adapted test routine running on

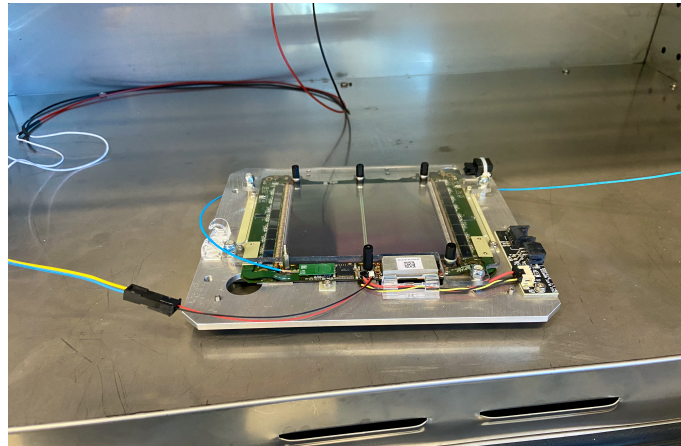


Figure VII.1: Module inside the climatic chamber. The red and black wires connect the low voltage to the module, and the blue optical fiber connects the module to the FC7.

a Linux PC. No bias voltage is applied to the sensor. Therefore, it is not necessary to shield the module inside the climatic chamber with its glass window from ambient light. On the right side of the carrier plate of the module, an interface board is mounted for easier connection of low and high voltages. This board is not used in the setup.

VII.2 Test procedure

For module testing, a customized test procedure is utilized and adapted [50]. It allows measuring many of the parameters already determined for hybrids on the test card. Most of the tests and measurements are described in Section III.4 and only differences to the test card routine are explained in this section. The ADC tuning algorithm is quite similar to the algorithm for the SEH on the test card (Section III.4.9). The tuning is necessary to measure ADC values with the lpGBT and values for gain and offset are determined. Values for V_{Ref} and the corresponding DAC value $V_{\text{Ref,tune}}$ are measured during the temperature ramp measurement.

After the ADC calibration, the measurement of different ADC values is possible with the SEH on a module. The SEH provides the possibility of monitoring different voltages. The input voltage on the hybrid is measured by using a voltage divider, and the parameter is named VMIN. The same parameter is used as a reference for the calibration, so the measured value should be constant, which is checked in Section VII.3.3. A similar measurand is VMON_P1V25_L. It is another ADC input measured with a voltage divider and provides information about the 1.25 V fed back from the left FEH as a sensing possibility. The last ADC input to control module voltages is the AMUX line. Some output voltages of the front-end chips are measured as AMUX values for both the right and left FEH. It is a multiplexed line that allows to measure voltages from each chip in sequence since all the chips share the same line. To test this functionality of the SEH, settings are chosen such that CBC0 outputs its V_{Cth} voltage, which can be measured by the lpGBT.

Other measurements using the ADC input of the lpGBT are temperature measurements. The temperature-dependent PTAT output of the BPOL2V5 is measured equivalently to the test card measurements. What is not recorded during the test card tests is the internal lpGBT temperature. On the module, it is analyzed. Additionally, it is possible to measure the sensor temperature on the module (Section III.4.11). This is achieved by connecting an NTC thermistor to the SEH via a flexible Kapton cable. The resistance of the thermistor varies linearly with the sensor temperature. Unlike on the test card, where this measurement was simulated using a resistor, on the module, temperature information can be obtained. The measurement process is identical to that of the TEMPP voltage, with the step to convert the measurement to the actual temperature included in the routine.

With the used low voltage power supply, the applied low voltage and the drawn current are measured as U_{Module} and I_{Module} . The turn-on or turn-off points of the module with the corresponding voltages and currents are also determined. Section III.4.2 explains the used procedure in more detail. All the explained measurements and parameters are analyzed, but only a few of them will be presented in the following section.

VII.3 Results

VII.3.1 Noise scan

Before exposing the module to a cold environment and thermal cycles, a noise measurement is performed at room temperature. The setup used for this measurement is identical to the one described in Section VI.2. The noise of a strip is defined as the width of a measured S-curve, as explained in Section VI.3.1. It is quantified in V_{Cth} -units. The measurement for all strips is commonly illustrated by plotting a histogram. The same noise measurement is repeated in the identical environment after the thermal measurements. The resulting noise histograms are shown in Figure VII.2. It is important to note that the results presented here are from measurements on a single front-end hybrid, and while the data for the other FEH are not shown, it exhibits similar behavior. The average noise per strip is around $6 V_{\text{Cth}}$ and the difference between the means before and after the cycles is smaller than half of a standard deviation. Additionally, the figure provides the maximum and minimum noise values, which are consistent between both measurements. No significant outliers with overflow noise bins are observed. This indicates that the thermal cycles did not introduce any notably noisy strips. In summary, no significant differences in the module noise levels are induced by 22 thermal cycles, and the module effectively withstood multiple temperature changes without encountering any issues.

VII.3.2 Thermal cycles

In total, 22 cycles with module tests at warm and cold temperatures are conducted. This results in a total measurement time of more than three days. Throughout these cycles, all the measurands show a constant behavior, mostly with two different levels corresponding to the two temperature conditions. The uncertainties are estimated by either calculating the mean and standard deviation based on ten measurement points or by considering the known binning uncertainty of the measured parameters.

The measurement of the sensor temperature and the internal measurement of the lpGBT temperature are shown in Figure VII.3. In the presented figure, the two distinct temperature levels are evident. The air temperatures within the chamber are -35°C respectively 40°C . Notably, the sensor temperature is approximately 2 K higher than the ambient temperature. This measurement is taken close to the SEH, and it is likely influenced by the heat generated by the SEH's power consumption. There is no active cooling connected to the module or the SEH and the hybrid is in contact with the sensors via the heat-conducting bridge. Interestingly, the temperature of the lpGBT is 7 K higher than the cold air temperature and nearly 20 K higher than the warm air temperatures. This difference can be explained because the lpGBT chip uses a non-calibrated conversion factor. To determine the internal chip temperature based on the voltage, which depends on the temperature, a calibration is needed [25]. This calibration determines the conversion factor between voltage and temperature and has nothing to do with the ADC calibration performed during each test. The temperature calibration is not specifically performed for the used lpGBT on the prototype service hybrid. The used conversion factor provided by the lpGBT group is based on measurements done with other lpGBT chips at CERN. This means that the conversion factor is not ideal for this particular chip, which is why these temperature differences can be seen across a wide temperature range of 75 K.

The turn-on current has only small fluctuations within the temperature levels throughout the 22 cycles. The measurement is presented in Figure VII.4. Additionally, the figure shows the measurement of the turn-on voltage, which is constant within the two temperature levels. Only the last point of the colder level falls in a different bin. The uncertainty of the current is estimated

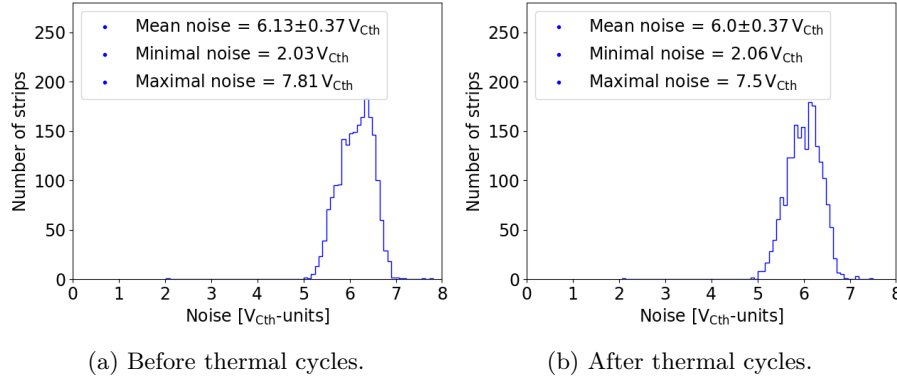


Figure VII.2: Noise measurement of the right FEH before and after the thermal cycles.

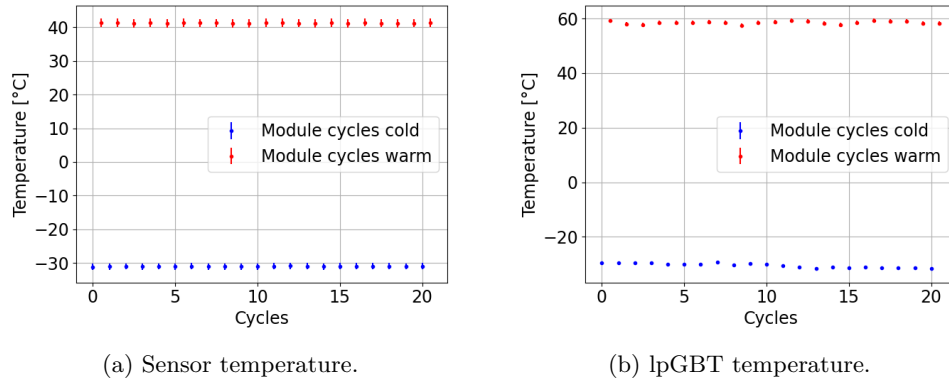


Figure VII.3: Internal temperature of the lpGBT and sensor temperature for the module cycles.

by measuring the current drawn from the module, I_{Module} , ten times and calculating the standard deviation. Given that a single measurement of the turn-on process takes several minutes, it is not practical to estimate uncertainty through multiple measurements of the whole process. The uncertainty of the voltage results from the binning of the measurement steps, in which the voltage was increased. The turn-on current and voltage depend on the temperature of the hybrid, and the DC-DC converter enables at lower voltages for colder temperatures. Moreover, the converter operates with higher efficiency at cold temperatures, resulting in lower power consumption. Both effects can explain the two temperature levels for the turn-on current. For the final tracker, it is important to measure the turn-on and turn-off points for different temperatures. The process was only measured at room temperature before, but as shown in the figure, the turn-on points shift with decreasing temperature. At -35°C in the final detector, in the worst case, it could happen that the turn-on and turn-off voltages are closer together compared to room temperature. It could result in the effect that the modules turn on, but through the drawn current and the voltage drop in the long wires, the voltage falls below the turn-off point. This could cause many problematic effects. The measured turn-off voltage is constant over the cycles, and the mean values are presented in table VII.2. Between warm and cold temperature the voltage shift is less than 0.2 V for the turn-on and turn-off voltages in the same direction. Therefore, the difference remains constant, and problematic effects in the detector caused by shifting turn-on voltages can be excluded.

Additionally to the presented results, nine further measurands were analyzed, but no unexpected behavior like outliers or jumps in the data points could be observed. Over all the thermal cycles, the measured parameters stay constant, mostly with two levels for the different temperatures. Table VII.2 summarizes the results for the two temperature levels. For the 22 recorded cycles, the mean and standard deviation are calculated separately for warm and cold measurements. Therefore, the given uncertainty in the table is the statistical uncertainty for the

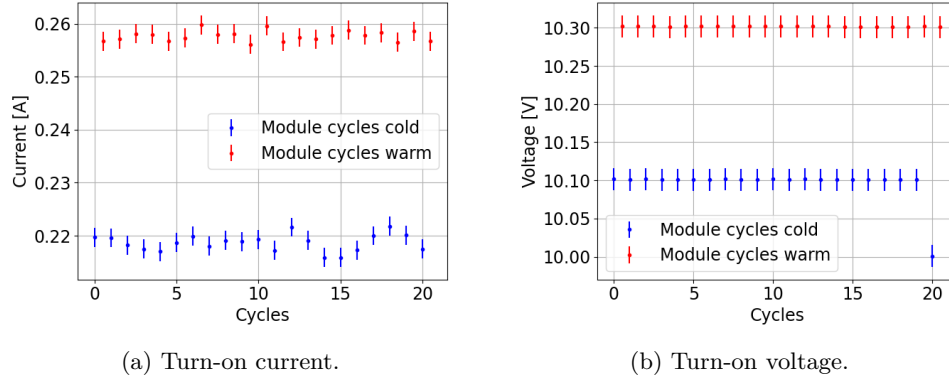


Figure VII.4: Turn-on voltage and the corresponding current measured for 22 thermal cycles.

Table VII.2: Summary of the measured values for the two temperature levels.

Measured parameter	Lower temperature level	Upper temperature level
Ambient temperature [°C]	−35	40
ADC gain	1.8715 ± 0.0017	1.9271 ± 0.0025
ADC offset	506.9 ± 0.4	508.8 ± 0.5
VMIN [V]	0.5082 ± 0.0005	0.5073 ± 0.0006
VMON_P1V25_L [V]	0.7663 ± 0.0005	0.7797 ± 0.0010
lpGBT temperature [°C]	-30.5 ± 0.8	58.5 ± 0.5
PTAT_BPOL2V5 [V]	0.1892 ± 0.0023	0.5284 ± 0.0029
Sensor temperature [°C]	-31.04 ± 0.06	41.28 ± 0.10
Turn-on current [mA]	218.6 ± 1.6	257.6 ± 1.0
Turn-on voltage [V]	10.096 ± 0.021	10.3016 ± 0.0005
Turn-off current [mA]	8.95 ± 0.05	9.5 ± 0
Turn-off voltage [V]	6.401 ± 0	6.60104 ± 0.00021

cycles. For some measurements, especially with large binning uncertainties like for the turn-on voltage, the systematic uncertainty could be higher. For almost all the measurands one can see differences between the two temperatures. Only for VMIN the differences are smaller than two standard deviations. VMIN is the measured input voltage, which is used as the reference voltage for the ADC calibration. Therefore, the measurement of VMIN is tuned towards the reference voltage, and VMIN should be constant.

VII.3.3 Thermal ramp

In the analysis of the thermal cycles, one could see a strong temperature dependency for many of the analyzed measurands. To gain a better understanding of the temperature dependence, a thermal ramp was performed. The temperature is increased from a starting temperature of -35°C in steps of 5 K up to a maximal temperature of 40°C . After allowing a brief dwelling time of 10 min at each temperature step, a test was started. For the temperature ramp, more temperature dependent effects of the parameters can be observed. The most important of them will be discussed in more detail in the following paragraphs. For the parameters presented in Table VII.2 the temperature dependency is analyzed. Some other parameters like the values for I_{Module} and U_{Module} are added in this measurement. Not all the measured parameters can be discussed in this section.

Gain and offset: For gain and offset of the ADC calibration of the lpGBT two levels in the measurement of thermal cycles for the two different temperatures are observed (see Table VII.2). With the thermal ramp, the temperature dependence in between is measured. The results are illustrated in Figure VII.5. For the offset, almost no temperature dependency is visible. The

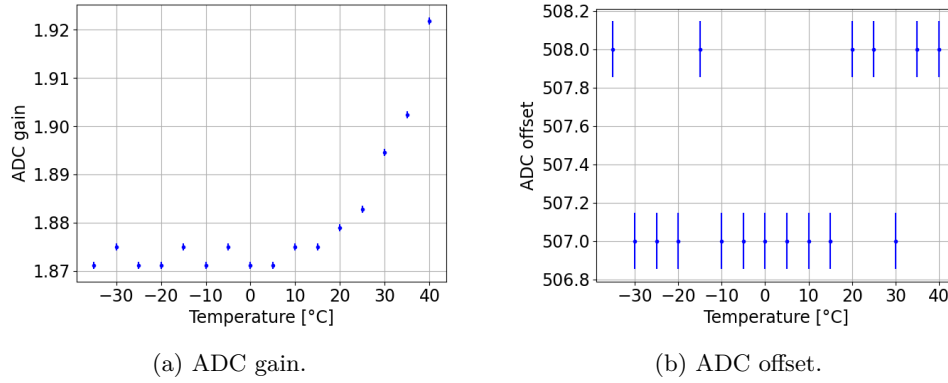


Figure VII.5: Gain and offset of the ADC calibration measured for a temperature ramp.

uncertainty of the measurement points is estimated as $\frac{1}{\sqrt{12}}$ due to the integer nature of the offset. The measured values fluctuate between two bins, and for warm temperatures, the offset falls a bit more often in the higher bin. In contrast to that, the gain has a strong temperature dependency. For temperatures up to 10 °C the gain remains relatively constant, hovering around a value of approximately 1.873. But at warmer temperatures it starts rising to more than 1.92 at 40 °C. This specific effect was also observed in the ADC calibration of SEHs on the test card with load. The final detector is operated at cold temperatures. Therefore, the raise in the gain factor for warm temperatures is far away from the operation point and will not have an effect there. Other ADC values, like the PTAT shown in Figure VII.7, show a linear behavior even for warm temperatures. This is an indicator that the ADC calibration works fine for all the temperatures and that the rising gain factor is necessary to measure correct ADC values.

Input current and V_{ref} : With increasing temperature, the input current also increases. As observed on previous tests with the test cards, the efficiency of the SEH decreases with rising temperatures, leading to an increase in power demand. The measurement of the input current is shown in Figure VII.6. To estimate the uncertainty, each data point is measured ten times, and the mean and standard deviation of these values are calculated. While the temperature-dependent behavior of the input current is expected and generally not a cause for concern, it does have implications for the ADC calibration and, consequently, all the measured ADC values. This is explained by the fact that the measured input voltage, which depends on the current, is used as a reference voltage for the ADC calibration. Therefore, the effect of current variation on the calibration needs to be estimated. Over the whole temperature range, the current rises by approximately 12.3%. By Ohm's law, this corresponds to an equivalent increase in the voltage drop between the power supply and the module. For further investigation, it is necessary to calculate the change of the actual input voltage applied to the module at cold and warm temperatures. The input voltage V_{MIN} is measured with a multimeter by using a voltage divider, allowing to deduce the actual applied input voltage at room temperature:

$$V_{\text{module}} = V_{\text{MIN}} \cdot \frac{90.9 \text{ k}\Omega}{4.7 \text{ k}\Omega} = 9.82 \text{ V} \quad (\text{VII.1})$$

The voltage drop between the Hameg power supply and the module is 0.68 V. Now, one can account for the 12% increase in this voltage drop. This estimation is conservative because it is the difference in current between cold and warm temperatures. The voltage on the module is measured at approximately 21 °C so somewhere in the middle between temperature levels. By using these numbers, the total voltage applied to the module can be calculated. It decreases to 9.74 V. This results in a relative change of 0.8% of the total input voltage. The real input voltage on the module has a direct impact on the ADC calibration. The calibration is using V_{MIN} for tuning. The calibration algorithm works in such a way that V_{MIN} measured by the ADC matches the value determined before with the multimeter at room temperature (Section III.4.9). If the real input voltage is different from the value measured with the multimeter, the calibration is tuning

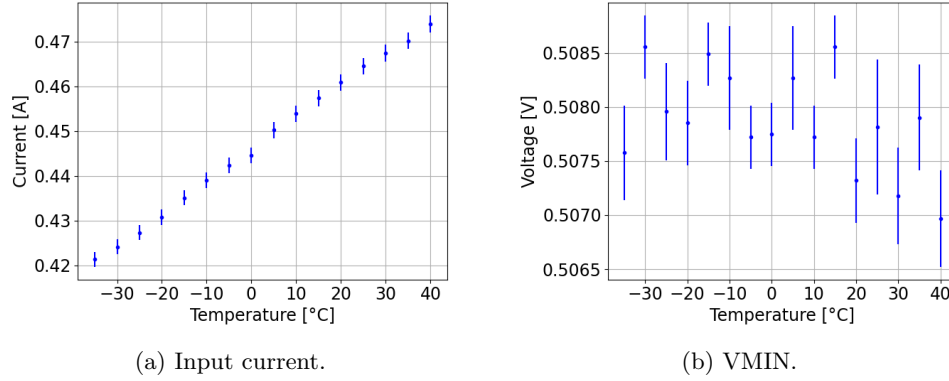


Figure VII.6: Input current and measured input voltage over a voltage divider (VMIN) depending on temperature.

to an incorrect value. By assuming the 0.8% change of VMIN over the whole temperature range as an uncertainty and using error propagation with the ADC formula used for the calculation of V_{ref}

$$V_{ref} = \frac{V_{pos} \cdot Gain \cdot 512}{ADC - Offset \cdot (1 - Gain)} \quad (VII.2)$$

(where ADC values have an initial uncertainty), one obtains the same uncertainty of 0.8% for V_{ref} . For the error propagation, the temperature dependence of the gain factor can be ignored. In a second step of error propagation with the ADC master formula (equation III.4), one gets the same uncertainty for every measured ADC value. This ultimately results in ADC measurement differences of 0.8% across the entire temperature range, attributable to the rising input current. The right side of Figure VII.6 presents the measurement of the input voltage over the voltage divider (VMIN). Per construction, it should be constant at 0.508 V, which is the case. But the actual input voltage is not constant, leading to a 0.8% deviation in the ADC measurement over the temperature range.

The result of this whole estimation means that only if measured ADC values differ more than 0.8% for the different temperatures, it is an effect in the real voltage on the module. Smaller effects can be explained by the uncertainty in the ADC calibration caused by the rising input current.

PTAT_BPOL2V5: In addition to the lpGBT, the chip of the second-stage DC-DC converter also provides information about its internal temperature. The output voltage proportional to the chip temperature is named PTAT (Proportional To Absolute Temperature), which serves as an ADC input of the lpGBT. Although the absolute calibration of the PTAT voltage is not known, conducting measurements with the temperature ramp allows for a comparison of the slope with the slope specified in the DC-DC manual [24]. The fit to the data points is shown in Figure VII.7.

The slope obtained from the temperature ramp data is $(4.42 \pm 0.05) \frac{mV}{K}$. Because it is not possible to directly measure the actual temperature inside the chip, the absolute conversion from PTAT to temperature is unknown, but temperature differences can be evaluated. In the manual of the BPOL2V5 a slope of $4 \frac{mV}{K}$ is provided. The difference in slope could be explained because, as shown above, the drawn input current rises about 12% with increasing temperature. This results in a higher power conversion in the DC-DC converters, and therefore, the actual chip temperature is warmer compared to measurements with a standalone converter with a constant power supply. The temperature shown on the x-axis in the figure is the air temperature, and because of the higher power conversion, the actual chip temperature has a different slope compared to the air temperature in the thermal ramp. This means that the incline of the PTAT against ambient temperature increases compared to the manual. The same effect with the higher current and therefore a higher temperature in the DC-DC converter could also be a part of the explanation

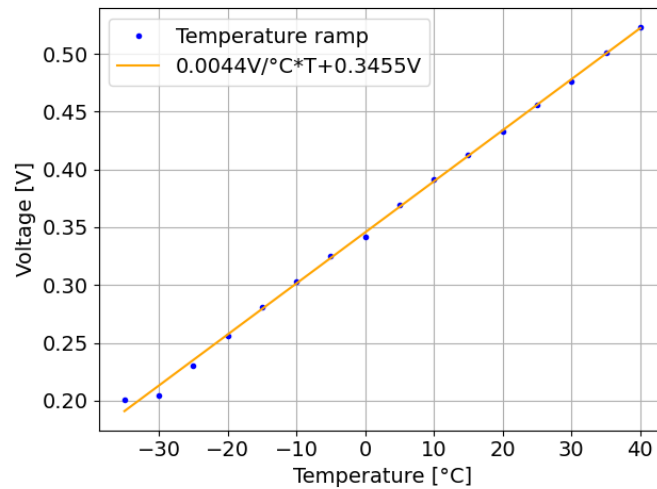


Figure VII.7: PTAT voltage of the BPOL2V5 for a temperature ramp. The slope is determined by a linear fit.

of the higher temperature difference to the ambient at the warm temperature level of the lpGBT shown in Figure VII.3. The DC-DC converter could heat up the PCB and therefore also the chip. A detailed analysis of this temperature behavior of different parts would be possible by placing temperature sensors on different parts of the SEH but this is beyond the scope of this thesis.

VII.3.4 Comparison to test card results

Many of the measured parameters for the SEH were previously determined on the test cards. It is valuable to compare these results with those obtained from the test card measurements. It's important to note that while the test card and the module both use hybrids from the same series, they are not identical. Table VII.3 displays the results measured on the module and on the test card. The test card results presented in the table represent the mean and standard deviation of measurements on two hybrids with lpGBT V1, identified by IDs 2SSEH-201000030 and 2SSEH-201000031, across 30 different test cards. Calculating the standard deviation of only two hybrids is not very meaningful but gives an idea of the variations between the hybrids. These measurements were conducted with the load current turned on, aligning them with the module measurements where the FEHs consistently draw power. Only the turn-on process is measured without load, which is evident in the turn-on current.

Most of the results are similar. The temperature values are slightly different. This disparity arises from the fact that when the test card is subjected to a load test, a prior test without a load has already raised the card's temperature by approximately 3 K. This higher temperature can potentially influence other measurements. The ADC calibration with gain and offset behaves quite similarly in both cases, and the values of VMIN differ by less than two standard deviations. Notably, the BPOL2V5 PTAT output varies between the module and the hybrid on the test card. But for this parameter, there are also substantial differences between different hybrids. The absolute temperature scale of the PTAT is unknown, and only temperature differences are possible to measure. Therefore, absolute differences should not be a cause for concern. In general, the turn-on process looks similar in both cases, with differences primarily attributed to the different load currents. Consequently, the turn-on current is twice as high on the module compared to the test card because the currents drawn from the FEHs are different compared to the currents drawn from the test card. The difference in power consumption also affects other parameters, for example, the PTAT voltage. Different turn-on/turn-off currents also explain the different turn-on and turn-off voltages. Higher current flow to the module leads to greater

voltage drops on the lines to the hybrid, resulting in higher measured voltages from the power supply, even if the turn-on voltage on the hybrid remains similar.

This comparative analysis underscores that the test card effectively simulates the module, yielding comparable results concerning the service hybrid. However, as highlighted above, some differences do exist, emphasizing the importance of recognizing and understanding them.

VII.4 Summary

By comparing the module's noise levels before and after the thermal testing, it is demonstrated that the module endured the thermal stress without encountering any issues. In total, the module was subjected to 22 cycles and a temperature ramp. For the cycles, all the measurands are consistent for all cycles, often displaying two distinct levels corresponding to the two different temperatures involved. With the thermal ramp, the temperature dependency could be analyzed in more detail. The effect of the rising input current on the ADC calibration was estimated, as well as the temperature dependence of the PTAT output of the BPOL2V5. To mitigate the effects of binning during the measurement of the turn-on voltage, a linear fitting approach to the data points was applied. Importantly, no significant outliers or unexpected behavior could be observed in the measurements. The results are compared with the measurements on the test card. Besides smaller differences, the results fit together, which shows that the test card can effectively simulate the module behavior for the SEH.

Table VII.3: Summary of the average measured values for the two temperature levels on the module compared to hybrids 2SSEH-201000030 and 2SSEH-201000031 on 30 different test cards. The test card measurements are measured with load besides the measurements of the turn-on process.

Measured parameter	Module		Test card	
	Cold temperature	Warm temperature	Cold temperature	Warm temperature
Ambient temperature [°C]	-35	40	-31.4 ± 0.8	43.6 ± 0.6
ADC gain	1.8715 ± 0.0017	1.9271 ± 0.0025	1.872 ± 0.004	1.908 ± 0.017
ADC offset	506.9 ± 0.4	508.8 ± 0.5	511.8 ± 2.6	511.1 ± 2.3
VMIN [V]	0.5082 ± 0.0005	0.5073 ± 0.0006	0.502 ± 0.008	0.496 ± 0.007
PTAT_BPOL2V5 [V]	0.1892 ± 0.0023	0.5284 ± 0.0029	0.43 ± 0.11	0.82 ± 0.20
Turn-on current [mA]	218.6 ± 1.6	257.6 ± 1.0	106.2 ± 1.5	113 ± 3
Turn-on voltage [V]	10.096 ± 0.021	10.3016 ± 0.0005	9.89 ± 0.03	10.10 ± 0.05
Turn-off current [mA]	8.95 ± 0.05	9.5 ± 0	8.4 ± 0.5	8.8 ± 0.3
Turn-off voltage [V]	6.401 ± 0	6.60104 ± 0.00021	6.188 ± 0.027	6.381 ± 0.025

VIII. Summary and Outlook

In this thesis, different aspects of service hybrids are analyzed. Thereby, the main focus is set on the quality control of service hybrid test cards. Additionally, it examines voltage drops in the power distribution from the SEH to the front-end hybrids and assesses the performance of a module within a climatic chamber.

Ninety test cards were manufactured and delivered. To ensure high quality standards, a two-stage quality control procedure is executed, involving tests at room temperature and within a climatic chamber. For the quality control at room temperature, two tests are conducted. A basic electrical test measures voltages, currents, and temperatures on the test card. Fundamental issues could already be seen with this test, and the results serve as a foundation for subsequent investigations. The second test requires a functional hybrid. An extended DAQ test, originally developed for SEH quality control, is conducted with one hybrid across all test cards. The selected hybrid has a known good quality, and any failed tests can be attributed to issues with the test card itself. Different issues, mainly concerning soldering failures on some cards, are uncovered. The yield of the first tests is summarized in Table VIII.1.

Table VIII.1: Outcome of the first stage of the test card quality control.

Number of test cards	Result
90	Tested in total
2	Fundamental issues observed by the electronics team
1	Chip rotated by 90°, already repaired
2	Incorrectly soldered resistors, already repaired
4	Open connection in the backplane connector, will stay at Aachen-1B
84	Good grading (after repair)

After the tests, 84 test cards are identified to be usable for the quality control of the SEHs. This set of test cards includes those that were successfully repaired and retested while excluding those with open connections in the backplane connector. Additionally, in this first stage, a comprehensive statistical analysis is performed, and measurements obtained with different test cards are compared to measurements with different hybrids. The statistical fluctuation of acquired values is dominated by the specific hybrid used.

Given that the test cards will undergo thermal cycling during the SEH quality control assessment, their performance across various temperatures and with thermal cycles is evaluated beforehand. A climatic chamber test setup is developed, and each test card is tested with at least eight thermal cycles. This testing protocol includes active cycling, where, during each cycle and at both temperature levels, the two quality control tests are performed. The results are summarized in Table VIII.2.

Table VIII.2: Outcome of the second stage of the test card quality control.

Number of test cards	Result
67	Tested in the climatic chamber
3	Principly workig, but open connections at the backplane connector
2	No stable USB connection
2	No USB connection in one test
60	Good grading

Only 67 test cards are tested in the climatic chamber, because 20 were already delivered to CERN. Three of the test cards are functional, but have an open connection at the backplane connector and will stay at Aachen-1B. In total, 60 test cards successfully passed the quality control assessments. Beyond evaluating individual test cards, several challenges in the testing

process became evident. To address these issues, adjustments are made to the firmware for the test cards and the FC7, ensuring a robust and reliable SEH quality control procedure.

In addition, different aspects of service hybrids within a module are investigated. A key concern is verifying the correct selection of output voltages for the DC-DC converters on the service hybrids. Various voltages on the front-end and service hybrids are measured at different module conditions. The measurements show that the voltages on the front-end hybrids fulfill the specifications of the chips. Therefore, they can be operated safely with the current output voltage of the DC-DC converters.

To gain a deeper understanding of the behavior of a module at different temperatures, one module was operated in the climatic chamber. Various parameters related to the SEH are measured and compared to measurements taken with the test cards. The effects of thermal cycling on a module are assessed by measuring the electrical noise of the module both before and after cycling, with no significant differences detected.

The next phase involves a more detailed examination of issues on individual test cards. In total, ten test cards with any kind of issues remain at Aachen-1B. Most of them are already at the electronics workshop for repair. Five problems are due to open backplane connections concerning redundant pins and rare USB connection failures during the tests. These test cards should stay at Aachen-1B, but in principle they are fully functional and can still be used for testing service hybrids. The remaining five cards require repair. Significant efforts have been invested in developing a climatic chamber setup that offers comprehensive control with a single PC. This setup could be used for further thermal studies of different components for the new Outer Tracker.

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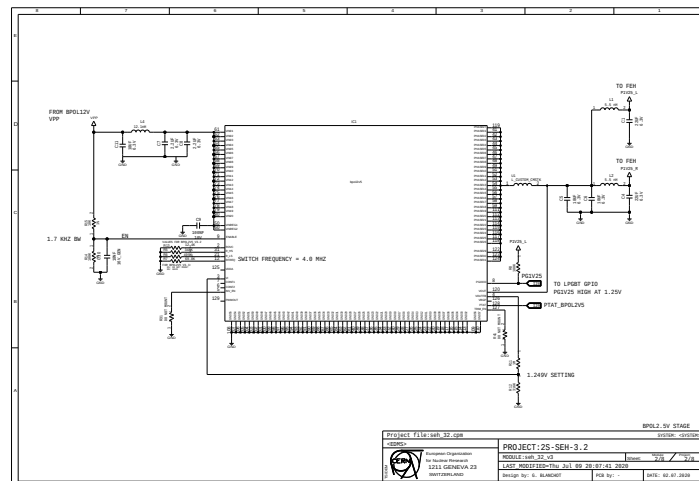
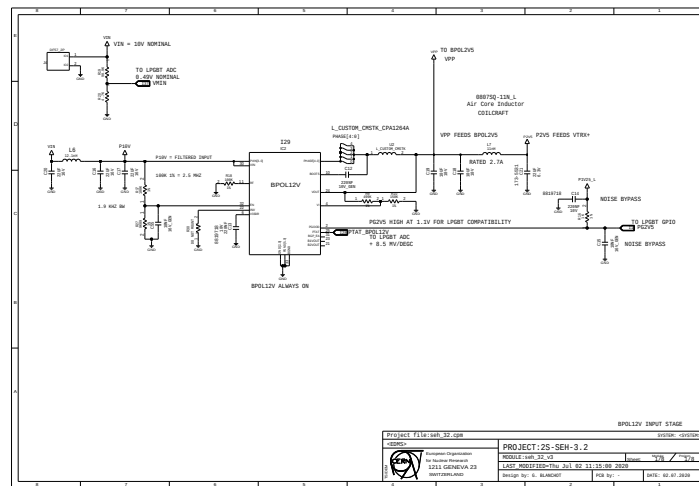
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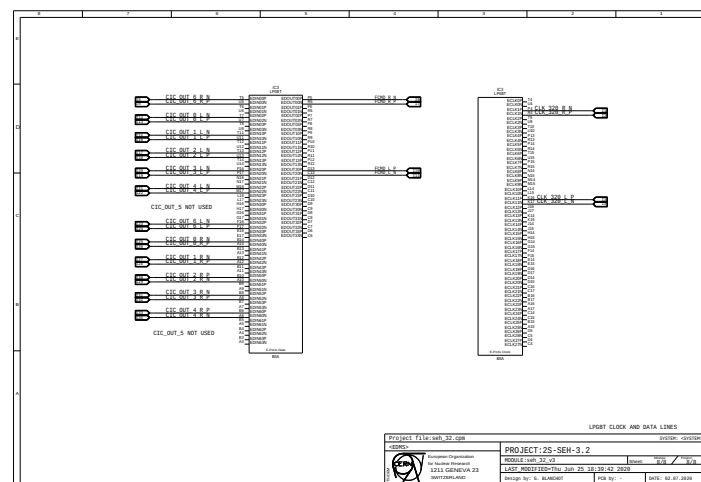
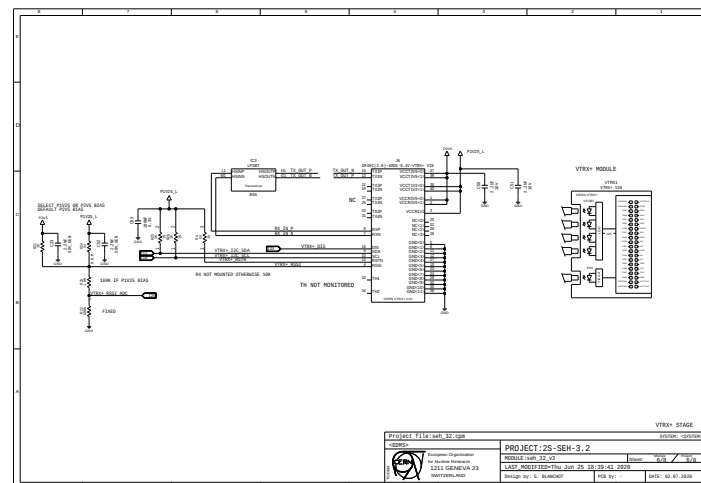
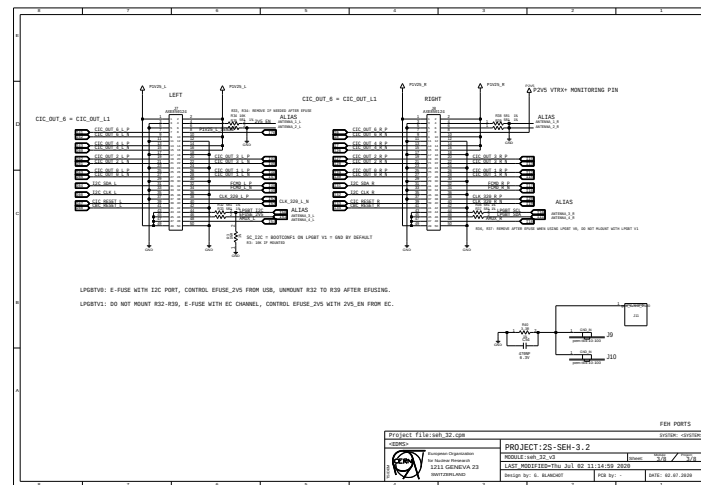
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A. Appendix

A.1 Relevant SEH schematics

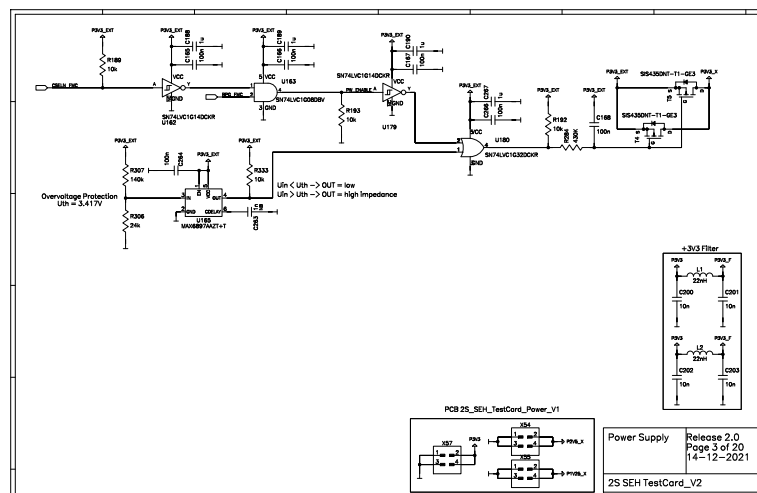
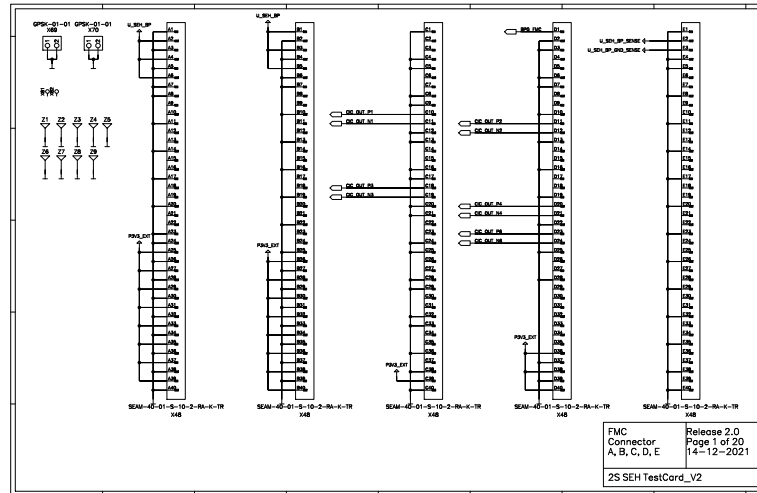
The most relevant electrical schematics of the service hybrids are shown in the following figures. All the important components can be seen.

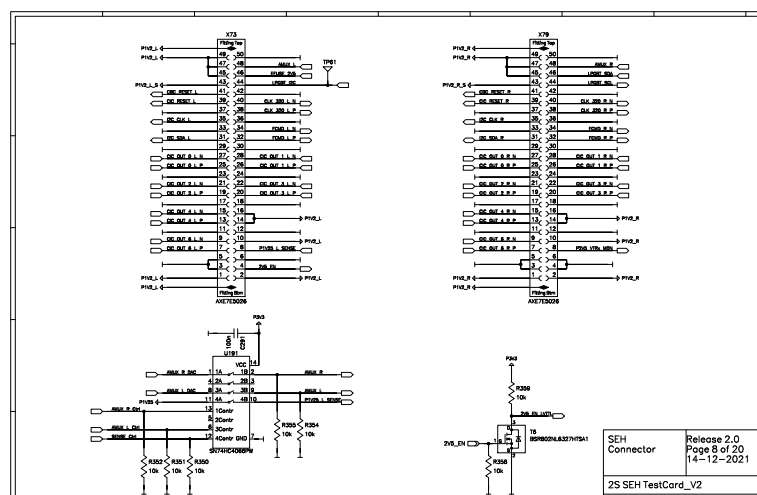
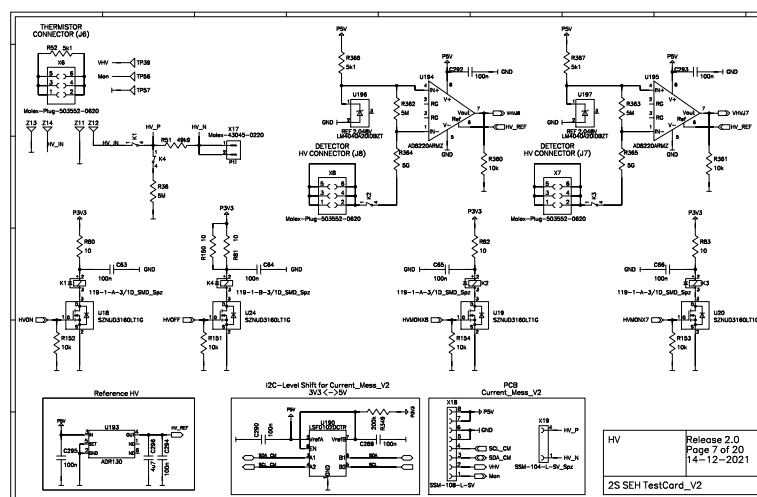
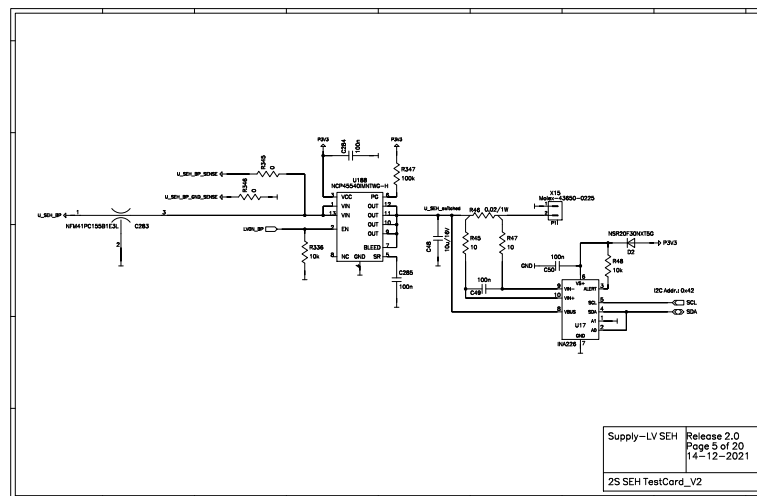


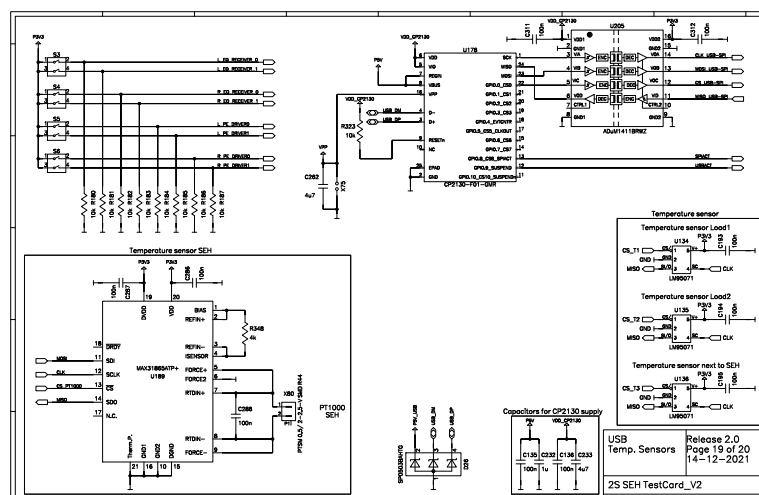
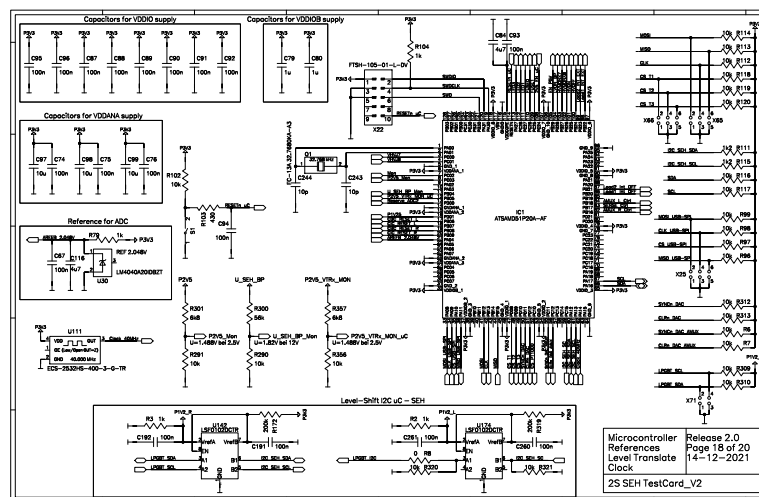
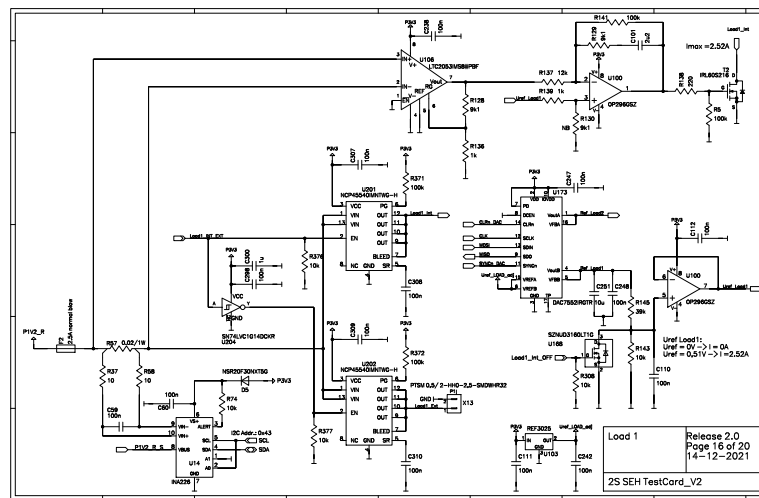


A.2 Relevant test card schematics

The most important electrical schematics of the test card are shown in the following figures. All the important components can be seen.







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