

Electronics control and signal processing for the LHCb fast calorimeter detectors

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Abstract

The aim of this thesis is to present a solution for the analogue signal processing chain to be used in the LHCb calorimeter upgrade to substitute the present electronics and adapt to the new detector conditions. An integrated circuit was designed and tested which offers a performance that fulfills the noise and shaping requirements. It includes four analog channels, a Delay Locked Loop (DLL) for signal phase synchronization for all channels and an SPI communication protocol based interface. The analog circuit is based on two fully differential interleaved channels with a switched integrator to avoid dead time and it incorporates dedicated solutions to achieve low noise, linearity and spill-over specifications. The included DLL is capable of shifting the phase of the LHC clock (25 ns) in steps of 1ns. The selected technology is AMS SiGe BiCMOS 0.35 μ m.

Detailed testing procedures were applied to check if the integrated circuit meets the specifications. Further evaluations include tests with electron beams for real detector signal. Even more, the design included radiation hardness techniques and studies were done of its reliability under a radiation environment. The production and massive quality control guidelines are proposed.

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Resum

L'objectiu de la present tesi és el desenvolupament d'una solució integrada pel processat analògic de l'actualització i millora del calorímetre de l'LHCb. El disseny del circuit haurà de complir les especificacions. El processat del senyal consisteix en integrar un pols d'un tub fotomultiplicador després de 12 m de cable coaxial de 50 Ohms als armaris d'electrònica que es troben a sobre del detector. Aquest processat s'ha de realitzar a 40 MHz, a la freqüència d'esdeveniments en l'LHC, per tant, la integració ha de durar menys de 25 ns i no tenir cap temps mort entre events consecutius. En les condicions de l'actualització del detector, la relació senyal-soroll ha d'augmentar en un factor 5, el que imposa una restricció molt forta en el soroll que pot oferir el circuit (la càrrega equivalent de soroll ha de ser menor a 4 fC). Altres limitacions inclouen un guany de 4.5 fC/LSB per un rang de 12 bits, una no linearitat menor que 1%, un nivell inferior al 1% en el residu de la senyal en events posteriors, i una estabilitat en la sortida de l'integrador millor que un 1% amb un marge de fases de 4 ns.

D'altra banda, tota l'electrònica estarà sotmesa a radiacions i, per tant, pot patir degradació o mal funcionament per efectes acumulatius de dosi o els anomenats efectes de SEL o SEU. En el disseny presentat s'hauran d'aplicar les tècniques necessàries per reduir els aquests efectes i permetre un funcionament adequat durant la vida útil del detector.

Actualització i millora de l'LHCb

L'LHCb és un dels quatre grans experiments del Gran Col·lisionador d'Hadrons (LHC) localitzat als laboratoris del CERN prop de Ginebra (Suïssa) [1]. Els camps de recerca de la col·laboració són la violació CP, física del quark charm i desintegracions del mesó B. Des de que l'experiment es va posar en marxa, s'han agafat dades per més de 3fb^{-1} . La bona qualitat de les dades han permès fer mesures importants.

D'altra banda, s'està preparant una actualització i millora de l'LHCb per millorar la precisió de les mesures en grans àrees de la física de sabor [2]. Està previst dur a terme l'actualització durant la parada llarga de manteniment del 2019. Aquesta, permetrà augmentar la lluminositat instantània fins a $2 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$ (aproximadament uns 10 cops l'actual). La modificació més important del detector és enregistrar totes les dades dels detectors a 40 MHz, la freqüència d'interaccions de l'LHC, i la conseqüent supressió del primer nivell del sistema de selecció d'events o disparador. En el nou esquema, cada sub-detector envia les dades a 40 MHz a una granja de servidors en el que hi ha en marxa els programes de selecció d'esdeveniments. S'estima que es doblarà el rendiment d'esdeveniments en desintegracions hadròniques de mesons B.

D'igual manera que altres sub-detectors, el calorímetre de l'LHCb ha d'adaptar la seva electrònica (que és comú pel pels calorímetres hadrònic i electrònic) a les noves condicions. Conseqüentment, es procedirà a revisar l'arquitectura de l'electrònica i canviar les plaques *Front-End* (FE).

Actualització de l'electrònica del Calorímetre

El processat analògic del senyal que actualment es duu a terme en les plaques de FE [1] [3] [4]) consisteix en la integració d'un pols de corrent d'un tub fotomultiplicador (PM), que ha estat retallat a la base del PM i enviat a través d'un cable coaxial de 12 m de 50Ω . Els PM es troben a la part posterior dels mòduls de detecció i les plaques FE es troben a armaris d'electrònica a la plataforma del calorímetre (per sobre del detector). Per retallar el senyal es fa servir una altra línia de transmissió amb una terminació a la base del PM, fet que permet reduir la cua del pols i el seu residu en les mesures immediatament posteriors (l'anomenat *spill-over*). La descàrrega de l'integrador es realitza fent una còpia del senyal, passant-la per una línia de retard i restant-la a l'entrada de l'integrador.

Per tant de mantenir el mateix corrent mitjà en els PM després del augment de la lluminositat i no envellir aquests PM prematurament, s'ha de baixar el guany un factor 5 respecte als nivells d'operació actuals. Així, el soroll equivalent a l'entrada del preamplificador s'ha de reduir de manera que el soroll de sortida es mantingui en 1 compte d'ADC (o un càrrega equivalent de soroll de 4 fC). Com a resultat, una resistència de terminació de 50Ω no és acceptable i es va decidir apostar per una solució integrada (ASIC) que permet el desenvolupament d'un circuit amb una terminació activa i complir amb les restriccions d'integració d'elements a les plaques d'electrònica.

Donat que les mesures del Calorímetre s'han de dur a terme a cada encreuament de feixos de protons (a 40 MHz), el sistema ha de reduir qualsevol residu de senyal que pogués afectar esdeveniments posteriors en més d'un 1% respecte el senyal (la taula 1 conté les especificacions principals de l'electrònica per l'actualització de les

plaques electròniques FE).

Requeriments	
Rang d'energia	$0 \leq E_t \leq 10\text{GeV}$ (ECAL)
Calibració/Resolució	4fC/2.5MeV per compte d'ADC
Rang dinàmic	4096-256 = 3840 LSB: 12 bits
Soroll	$\lesssim 1$ ADC cnt (ENC < 4 fC)
Terminació	$50 \pm 5\Omega$
Reducció de la línia de base	Substracció dinàmica de pedestal
Màx. pic de corrent	4-5 mA over 50Ω
Nivell de residu	$\leq 1\%$
Linealitat	$< 1\%$
Interferència entre canals	$< 0.5\%$
Sincronització	Individual (per canal)

Table 1 – Resum de les especificacions per l'electrònica analògica de les plaques FE del Calorímetre.

Soroll i terminació de línia

Es proposa una terminació activa com a solució a implementar en un circuit integrat per tal d'evitar l'ús d'una resistència passiva. La implementació escollida s'aconsegueix amb un circuit actiu amb impedància controlada.

Tot just després de la conversió digital, es realitza l'anomenada substracció dinàmica de pedestal. Aquesta consisteix en restar la mostra menor de les dues anteriors a l'actual. Així es redueix el nivell de pedestal i es filtra el soroll de baixa freqüència. Es tracta d'un tipus de soble samplejat correlat (CDS). S'ha demostrat que és crucial per fer mesures acurades, però incrementa el nivell de soroll en un factor arrel de 2 (idealment) quan les dues mostres no estan correlacionades.

L'efecte de la terminació activa o passiva en el soroll es pot comprovar en la figura 1, en la que s'hi representa el màxim de soroll sèrie acceptable respecte a l'entrada e_n especificat per un amplificador com a funció de la càrrega equivalent de soroll (ENC). Si considerem que el ENC requerit es menor que 4fC, el limit de soroll acceptable per un amplificador amb terminació per un cable és $2.25\text{nV}/\sqrt{\text{Hz}}$, mentre que pel cas d'un amb resistència de terminació i alta impedància d'entrada queda en $1\text{nV}/\sqrt{\text{Hz}}$ [5]. Resumint, un circuit amb impedància d'entrada active ofereix més marge en el disseny, mentre que el requeriment pel cas d'una terminació amb una resistència és massa restrictiu.

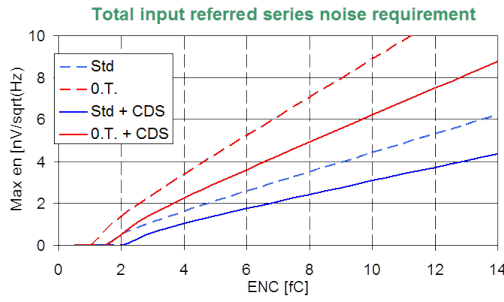


Figure 1 – Requeriment de soroll en sèrie per diferents configuracions d'amplificador i processat del senyal. El soroll en paral·lel s'ha omès.

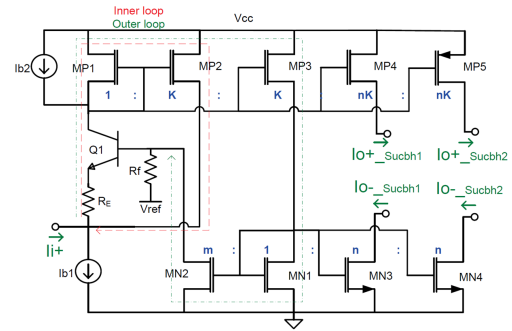


Figure 2 – Esquema simplificat de l'etapa d'entrada.

Disseny de l'ASIC i processat del senyal

La proposta d'implementació de circuit integrat (anomenat ICECAL) per processat analògic està esquematitzada en la figura 3. S'ha seleccionat una solució commutada degut a la dificultat per integrar línies de retard de qualitat i a que proporciona una manera de reiniciar l'integrador sense temps mort entre esdeveniments consecutius. Es fan servir dos camins alterns (sub-canals) amb interruptors per integrar i capturar els pulsos de corrent del PM. Aquest és un esquema implementat amb èxit en els xips del Preshower i SPD [1].

La implementació de l'ICECAL inclou quatre canals analògics amb elements clau del circuit programables per poder compensar les variacions de procés, quatre línies de retard (DLL) per sincronitzar la fase de cada canal i una interfície digital que utilitza el protocol sèrie SPI per comunicar-se.

El disseny del xip també està determinat per la radiació en el detector ja que ha de ser resistent als efectes d'acumulació de dosi i als SEU i SEL. Entre altres tècniques, es va optar per reduir els SEL incrementant la distància entre els transistors PMOS i NMOS i insertant anells de guarda. En el cas dels efectes SEU, es minimitzen implementant registres amb redundància triple i ideant una màquina d'estats finits esclau del bus SPI tolerant a errors. Finalment, els senyals de reset estan protegits de SET utilitzant supressors de pics.

Els prototips es van dissenyar en la tecnologia AMS 0.35 μ m SiGe BiCMOS amb fonts d'alimentació de 3.3 V.

Canal analògic

El canal analògic està dividit en diverses etapes. La primera, es tracta d'un preamplificador d'entrada que destaca per la terminació activa amb doble realimentació.

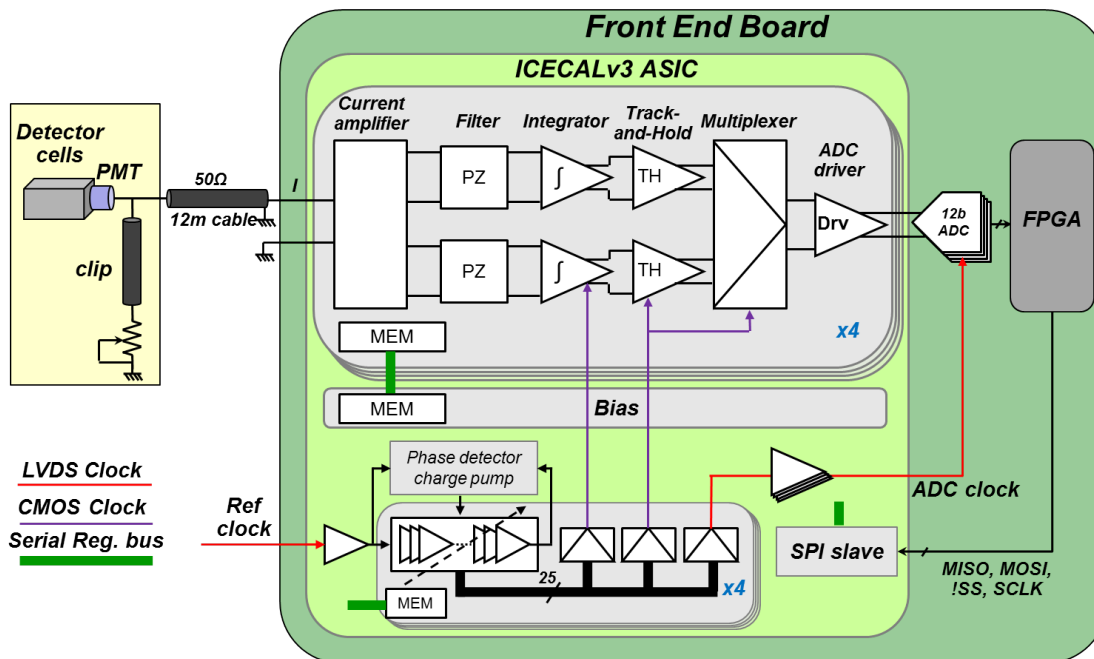


Figure 3 – Esquema de l'ASIC.

Com ja s'ha comentat, una resistència de terminació generaria massa soroll. El pols de corrent d'entrada s'amplifica i convergeix a senyal diferencial per atenuar el soroll en mode comú, que és important en un sistema amb interruptors. Tot seguit, un sistema de dos sub-canals alterns permeten la integració sense temps mort entre esdeveniments consecutius; mentre un sub-canal integra, l'altre reinicia l'integrador. Cada un d'aquests dos camins conté una etapa de processat de senyal pol-zero que compensa els efectes del cable sobre el pols, l'integrador commutat, un Track-and-Hold per mantenir el senyal estable a la sortida (per 12 bit de rang dinàmic), un multiplexor per seleccionar la sortida correcta i un amplificador per adaptar la impedància de l'ADC.

Preamplificador de corrent a l'entrada

El preamplificador a l'entrada està realitzat en mode base comú regulada i presenta una doble realimentació per aconseguir la terminació activa. Els dos llaços de realimentació de corrent [2](#) s'utilitzen per reduir i controlar la impedància d'entrada d'un transistor en base comú amb degeneració d'emissor i, proporcionar linealitat

adicional a la transconductància. La impedància d'entrada es pot calcular:

$$Z_{i_{CL}}^0 \simeq \frac{\frac{1}{g_{m1}}}{1+K} + \frac{K}{1+K} m R_f \quad (1)$$

La implementació en mode corrent aporta una sèrie d'avantatges respecte a dissenys anteriors [6]: baix voltatge, acoblament en DC (no calen components externs o pads addicionals), tots els nodes tenen baixa impedància (menor tendència a les interferències), i major fortalesa a descàrregues electrostàtiques o ESD (el pad d'entrada no està connectat a la porta d'un transistor MOS o a la base d'un de bipolar).

Etapa amb filtre pol-zero

Hi ha dues especificacions estretament relacionades amb la forma d'ona del pols d'entrada. La primera, el *plateau* fa referència al temps en el qual la sortida de l'integrador ha de variar menys d'un 1%: 4 ns. D'aquesta manera es pot mesurar amb un error petit i controlat l'energia de les partícules amb diferent temps d'arribada. La segona, ens limita a un 1% de la càrrega integrada el residu o part del pols que s'integra en els cicles immediatament anterior i posteriors. Aquest residu o part del senyal mesurat fora de la mostra correcta s'anomena *spill-over*.

El 2012 es va fer un test amb detector real (no amb generador de funcions) que inclou un feix d'electrons, canals i cables del sub-detector ECAL. Captures obtingudes amb un oscil·loscopi van mostrar que el pols utilitzat com a referència fins aquell moment no era del tot correcte; el pols mesurat presentava una amplada lleugerament major i una cua més llarga degut a efectes del cable. És per això que es va dissenyar un circuit simple amb un pols i un zero per mitigar les components lentes del pols. La figura 4 exposa les diferents ones: la mesura vella, la obtinguda el 2012 i la simulació de l'efecte del filtre. Així mateix, el pol i el zero es generen amb una resistència en paral·lel a un condensador ajustables per poder compensar per la forma d'ona i el procés de fabricació.

Integrador commutat

La integració es realitza amb un amplificador diferencial i realimentació amb capacitats. L'ús d'interruptors CMOS permet definir dos estats temporals alterns cada 25 ns: integració i reiniciació. El primer estat configura el circuit en format integrador clàssic, mentre que en estat de reiniciació connecta els condensadors a massa i els descarrega. Un senyal de rellotge amb període de 50 ns controla els interruptors. Les variacions de guanyen el canal es poden compensar amb la capacitat de valor programable.

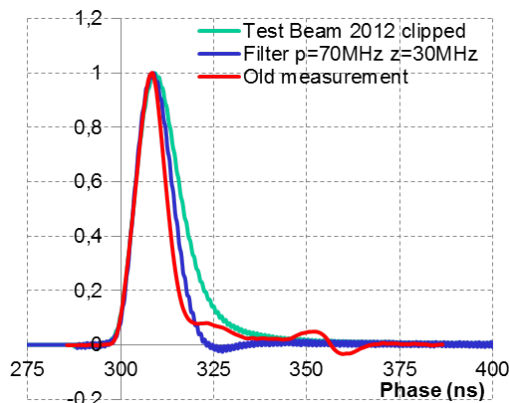


Figure 4 – Senyals d'entrada.

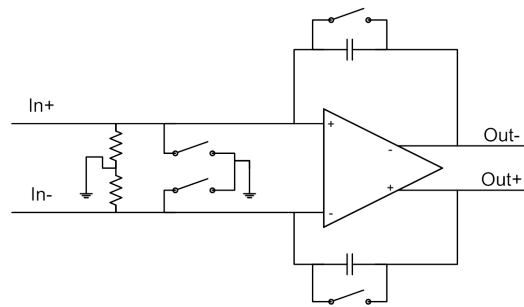


Figure 5 – Esquema de l'integrador commutat amb portes de pas.

Tot seguit s'hi afegeix un Track-and-Hold per donar estabilitat en la sortida i poder fer la conversió a digital. Un multiplexor analògic selecciona el sub-canal correcte. Cadascuna d'aquestes etapes utilitza també interruptors amb rellotges de 50 ns la fase dels quals s'ha d'ajustar per capturar el senyal en el moment adequat.

Línia de retard

Cada canal analògic inclou una línia de retard (DLL) [7] permetent a l'usuari programar diferents fases per compensar els diferents retards introduïts per la tensió d'alimentació dels PM, la longitud dels cables o els diferents temps de vol de les partícules en funció de la posició del sensor en el detector. El present disseny inclou una línia dedicada a variar la fase per l'integrador, Track-and-Hold i ADC extern de cada canal.

La DLL s'ajusta amb dos voltatges de control per assegurar que les variacions sistemàtiques o ambientals no afectin a la sincronització temporal. El disseny diferencial intenta reduir el soroll degut als interruptors produït per les línies de retard. El *jitter* del rellotge és menor que 4 ps.

Tal com s'ha comentat que anteriorment, s'han utilitzat diferent tècniques per reduir els efectes de la radiació. Els registres de redundància triple ajuden a evitar SEU. Els efectes SET es minimitzen amb supressors de pics en les línies de reinicialització. Finalment, els anells de guarda estan instal·lats en totes les cel·les digitals per evitar els SEL, el que implica un disseny totalment *custom*.

Configuració i control del xip

El bloc digital té la funció de permetre la configuració i control del xip. Aquest es compon d'una sèrie de circuits que s'utilitzen per programar paràmetres que no canvien durant la presa de dades, tal com les fases de rellotges, els corrents de bias, la impedància d'entrada, el guany del canal i les freqüències del filtre pol-zero. Està implementat seguint el protocol sèrie SPI, que permet llegir i escriure els registres interns del xip.

Entrant en més detall, el registre de control principal de l'ICECAL s'utilitza sobretot per definir els valors dels corrents de bias globals de l'amplificador operacional diferencial en les diferents etapes i del preamplificador d'entrada. Per tant, el comparteixen tots els canals. A més, cada canal té un registre propi que conté els valors dels paràmetres clau que defineixen el processat analògic del senyal i compensen pels processos de fabricació (la capacitat de l'integrador pel guany, l'offset per un major rang de sortida lineal, els valors del pol i del zero i la impedància d'entrada). Finalment, hi ha un registre dedicat a configurar la DLL per cada canal.

Mesures

Banc de proves pels prototips

El banc de proves de prototips està basat en el prototip de la placa FE i inclou connectors a plaques específiques que contenen el circuit analògic (diferents per cada prototip i per COTS). Altrament, també aporta un USB per connectar a un PC i controlar tot el test amb un programari dedicat a aquesta finalitat. El procés d'adquisició de dades està controlat per la FPGA del FE que es comunica amb el PC. El pols del PM es replica amb un generador de funcions arbitrari sincronitzat i disparat pel prototip de FE.

Sincronització temporal

Un dels reptes del detector és sincronitzar l'adquisició de dades en els diferents nivells de l'electrònica. En aquest sentit, el mateix es pot comentar sobre el prototip del FE. Primer, el rellotge d'entrada a l'ICECAL s'ha d'ajustar per fer una captura correcta del senyal que reinicia el sub-canal. Segon, s'ha de sincronitzar l'integrador respecte el moment en el que arriba el pols. En el detector, aquesta fase dependria de cada canal degut al voltatge d'alimentació del PM i la longitud del cable. El tercer nivell és el mostreig de l'ADC, que varia només en el moment del disseny de la placa on van muntats els components i de la fase d'integració. I, finalment, el quart nivell és la captura per part de la FPGA de les dades que envia

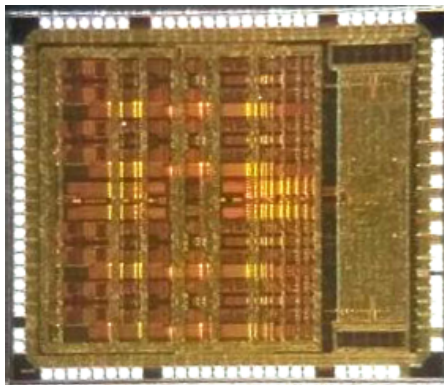


Figure 6 – Micro-fotografia del prototip ICECALv3.

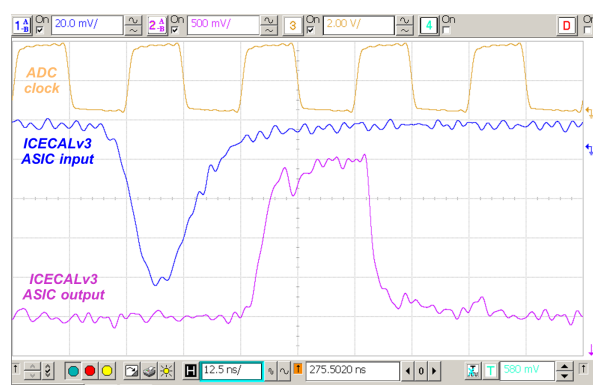


Figure 7 – Oscil·lograma amb els senyals d'entrada i sortida.

l'ADC. De cara a simplificar tots aquests detalls, es va desenvolupar un programa automàtic especialment dedicat a buscar els valors de les fases.

Resultats

Tots els resultats que es mostren en aquest apartat fan referència a les mesures realitzades de 30 prototips de la versió final del ASIC (ICECALv3).

La impedància d'entrada per diferent configuracions va ser mesurada amb un analitzador de xarxes (Rohde&Schwarz ZVL) a l'entrada (figura 6.10). Els resultats són aproximats donat que la connectivitat no era òptima. Dins d'un rang de 40 a 60 Ω , la terminació òptima correspon a 14 comptes de DAC.

Tal com està exposat a la taula 1, la sensibilitat esperada (inversa del guany) és 4.5fC/LSB. L'histograma de la figura 13 mostra la distribució de valors programats per la capacitat d'integració per tal d'obtenir el guany especificat. La desviació respecte aquest valor és menor que el 2.5%.

La no-linearitat es va trobar menor que 1% per tot el rang de sortida (figura 9). Utilitzant l'etapa d'offset, dissenyada per afegir un nivell controlable de DC als pins positiu i negatiu és possible evitar el límit en l'excursió de l'etapa del Track-and-Hold que afecta a la linealitat pels valors més alts de senyal (a partir de 1.8 o 1.9 V sobre 2 V). Cal remarcar que per valors petits de senyal, el soroll és comparable a la mesura i, per tant, l'error en el càlcul de la no-linearitat s'incrementa molt en comparació amb els propis valors de no-linealitat.

Altres especificacions importants inclouen el valor residual de senyal en les mostres anterior i posteriors (spill-over). L'ajust del pol-zero ajuda a minimitzar l'efecte del cable en la forma del pols, tal com es pot veure en la figura 11. Tal com està especificat, el valor del residu és menor a 1%, excepte pel la segona mostra després de la principal (T_2) que pot arribar fins a un 2% en alguns casos.

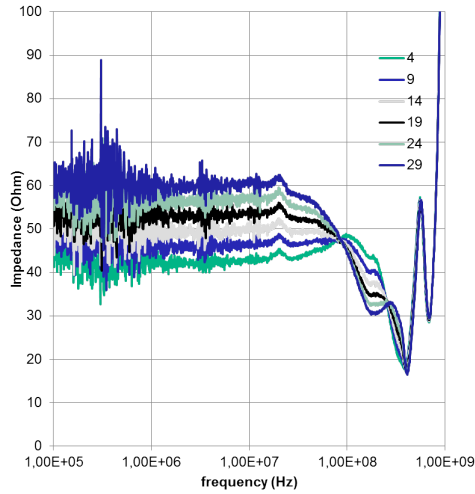


Figure 8 – Impedància d'entrada per different valors programats (5 bits).

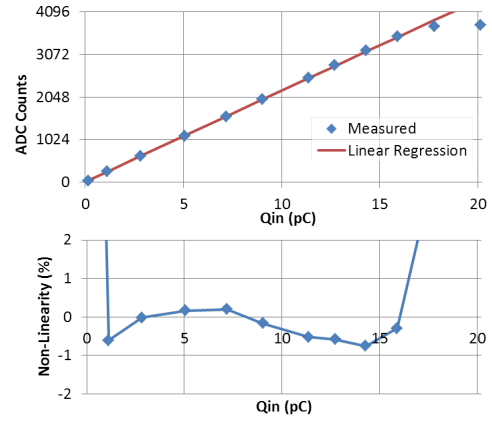


Figure 9 – No-linearitat en funció del voltatge de sortida.

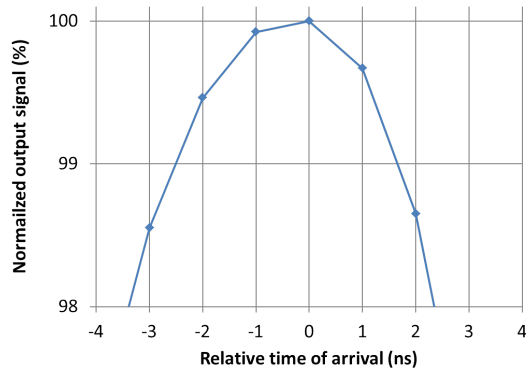


Figure 10 – *Plateau*.

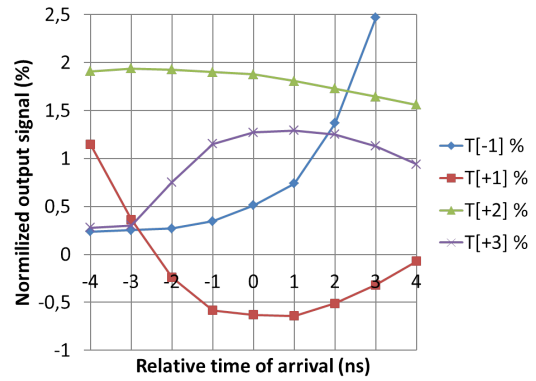


Figure 11 – Residu de senyal en les mostres anterior i posteriors.

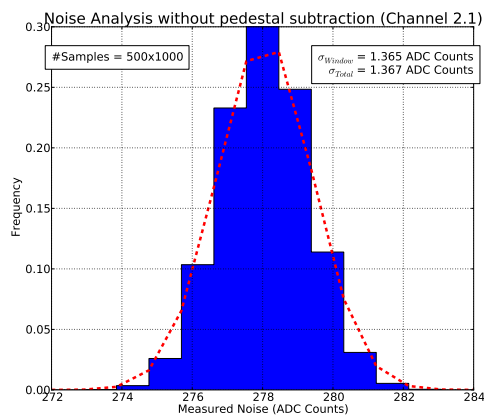


Figure 12 – Exemple de soroll per un canal.

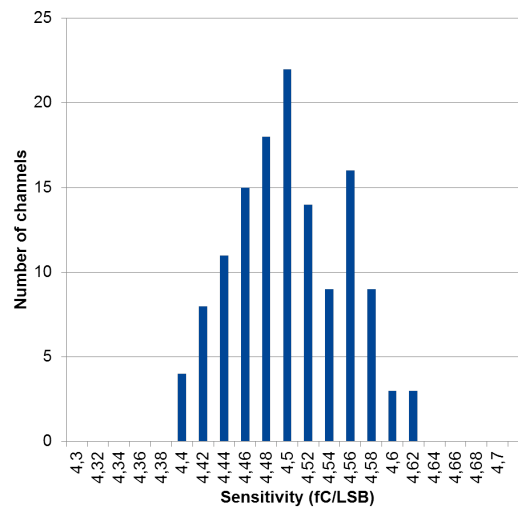


Figure 13 – Exemple de calibració del guany per un canal.

Si revisem les especificacions, el circuit integrat ha d'integrar senyals de partícules amb diferent temps d'arribada (± 2 ns) sense variar el nivell de sortida més d'un 1%. Aquest *plateau* també es veu afectat per l'acció de l'etapa amb el filtre pol-zero. De fet, entre el valor del *spill-over* i del *plateau* hi ha un equilibri; si millores les prestacions en un sentit, s'empitjora en l'altre. Un exemple d'estabilitat a la sortida de l'integrador en funció de la fase de l'arribada dels pols es mostra a la figura 10. La majoria de mesures de *plateau* estan sobre els 4 ns excepte per alguns casos (menys del 10% del total de canals) pels que sempre superen els 3.8 ns.

El soroll de cada canal depèn de la configuració dels diferents paràmetres, principalment del guany, l'*offset* i el pol-zero. Amb la configuració actual s'ha mesurat un soroll en de 1.38 i 1.70 comptes d'ADC abans i després de fer la subtracció de pedestal. El límit definit de soroll de l'electrònica estableix que aquest no hauria de ser superior a un compte d'ADC. En aquest cas, però, la condició es pot relaxar una mica ja que la font dominant de soroll en el detector és degut a l'acumulació de diverses partícules en el mateix canal i la mateixa mostra i puja, segons les darreres simulacions, fins a 5 comptes d'ADC.

Tests amb feixos d'electrons

Varis tests en condicions semblants a les de detector s'han dut a terme per contrastar els resultats amb el comportament esperat. Aquests tests consisteixen en portar canals com els del detector (incloent el PM, la seva font d'alimentació i el cable) i exposar-los a feixos de partícules en laboratoris especialment dedicats. En

el nostre cas, vam fer servir la línia de feix T4-T8 a un edifici del CERN a Prevessin (França). Es va generar polsos de senyal fent passar feixos d'electrons amb energies entre 20 i 120 GeV a través de mòduls de l'ECAL. Les captures de senyal es disparaven fent servir un sistema complementari amb dues plaques escintil·ladores. En paral·lel, un sistema integrador LeCroy i convertidor de temps (TDC) permetia en unes barraques tenir una mesura promig per comparar la linealitat i una altra per donar la fase de cada pols (veure la figura 14).

Durant els tests amb feixos de partícules es van fer estudis dels efectes de diferents energies i parts de detector en els diferents paràmetres que ja s'havien examinat al laboratori: linealitat, *plateau*, *spill-over* i resolució. En els tres tests

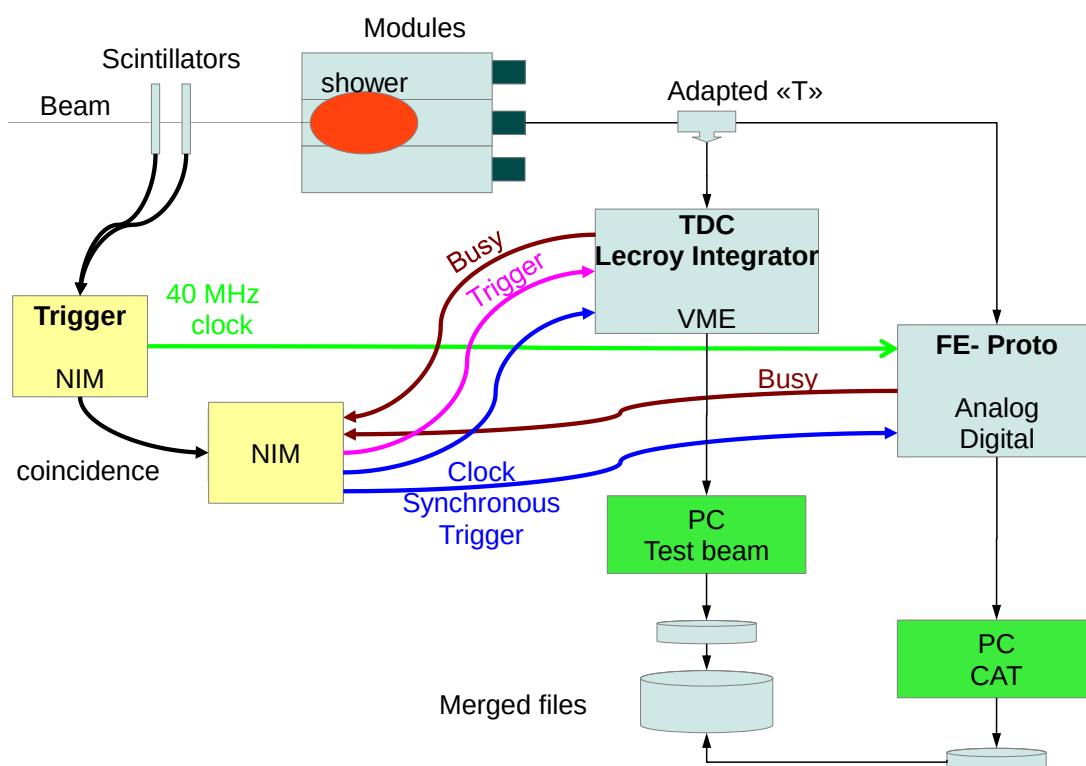


Figure 14 – Test beam setup.

amb feixos de partícules realitzats, el soroll es va mesurar amb resultats dissemblants; mentre al Novembre de 2012 el soroll es va limitar a 1.6 comptes d'ADC, aquest va pujar fins a 2.7 i 3.4 comptes d'ADC el Juny i Novembre de 2015, respectivament (figura 15). Per analitzar la linealitat, es va buscar un nivell de guany adequat en el PM i es van comparar els valors de sortida entre el sistema integrador de LeCroy i el xip ICECAL. La desviació no va superar el nivell del 1%

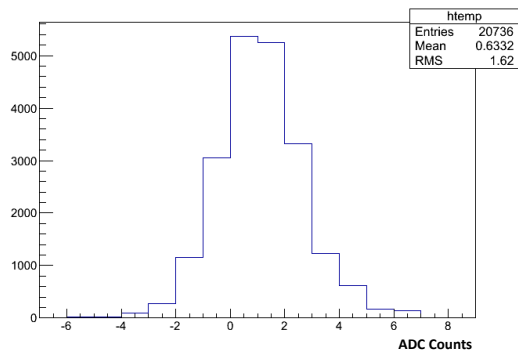


Figure 15 – Soroll després d’haver aplicat la sustracció de pedestal el Novembre de 2012 a un test amb feixos de partícules.

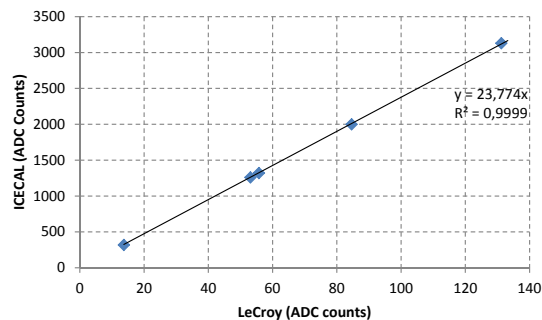


Figure 16 – Linearitat de l’ASIC.

per les diferents energies del feix (figura 16).

Adicionalment, es van fer estudis sobre el *plateau* i el *spill-over*. Donat que es tracta un sistema asíncron, en el que les partícules arriben amb qualsevol fase, cada cas de programació de paràmetres de pol i zero, voltatge de PM, cable, o energia, necessita realitzar milers de mesures per obtenir una corba energia/fase que ens permeti estudiar el valor màxim de l’integrador i el residu en les mostres anterior i posteriors. La dificultat també radica en el fet que el feix no sempre és molt pur; a part dels electrons hi ha pions que poden tenir qualsevol energia entre el valor dels electrons i zero. Els events amb electrons es poden separar dels de pions aplicant talls en les distribucions d’energia. A partir d’aquestes corbes es pot estudiar la resposta de l’integració en totes les configuracions de pol-zero, energia i PM.

A la figura 17 es mostra que la majoria de mesures de *plateaus* són de l’ordre o superiors als 3.8 ns. Tenint en compte les dificultats trobades en l’ajust de les corbes per la no sempre òptima puresa d’electrons en el feix, podem concloure que el resultat és força raonable. Es pot observar a la figura 18 que l’especificació sobre el residu de la senyal es compleix. Només hi ha un valor que està lleugerament per sobre del límit i es correspon a la mínima energia (amb una puresa d’electrons molt minsa). Una altra bona notícia és que la variació entre PM és petita, permetent-nos esperar que el mateix ajust de pol-zero és acceptable per la majoria o tots els canals un cop s’instal·li l’electrònica al detector.

Durant els tests amb feixos de partícules es va poder estudiar l’electrònica analògica en condicions molt properes a les del detector (PM real amb el cable, la base del PM, ...). Només en el cas del soroll es van veure diferències degudes

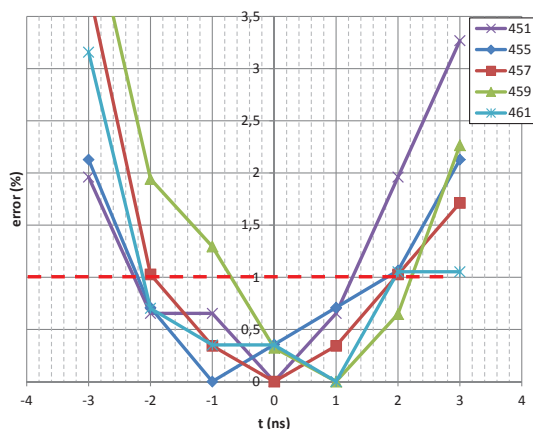


Figure 17 – *Plateau* per diferents PM.

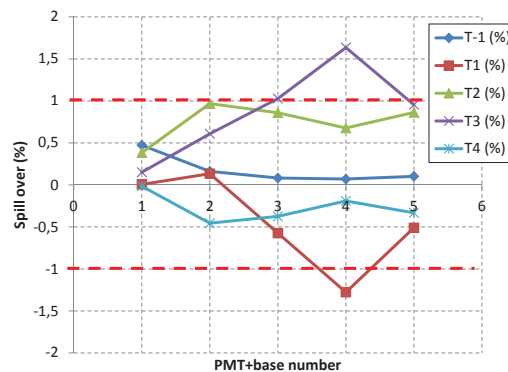


Figure 18 – *spill-over* per diferent PM.

a un mal contacte sub-òptim de massa comparat amb el detector i el laboratori. En resum, es van poder analitzar els efectes de canviar de sensors i cables, per diferents voltatges de PM. Els resultats no només reflexen que compleixen les especificacions, sinó que ho fan per les diferents condicions de mesura. Això ens permet esperar que es pugui definir una calibració a nivell de laboratori prou bona com per aplicar-la a la majoria (sinó tots) els canals del detector.

Resistència a la radiació

Els nivells de radiació esperats per l'electrònica, que està localitzada en armaria a la part superior del detector, s'estima que serà de $100\text{rad} \cdot \text{fb}^{-1}$ [8], [9]. En el present, preveu que l'experiment LHCb acumularà 50fb^{-1} en uns deu anys de funcionament després de l'actualització i millora proposada. La dosi referència mínima límit es va definir en 5krad per 50fb^{-1} , corresponent a la pitjor zona on hi ha electrònica. A part, les simulacions mostren una fluència esperada de $2.55 \times 10^{-12}\text{ cm}^{-2}$ neutrons.

La radiació en l'electrònica pot fer aparèixer problemes durant l'operació del detector deguts a l'acumulació de dosi i als esdeveniments *singulars* (SEU i SEL).

Convé fer ressaltar que la resistència a la radiació que presenta la tecnologia seleccionada ($0.35\mu\text{m}$ AMS BiCMOS) és aparentment més que suficient a partir d'estudis previs [10] [11] [12]. Tot i amb això, es van emprar tècniques específiques per ajudar a reduir els efectes deguts a la radiació [13] [14] [15]: es van afegir anelles de guarda a nivell de *layout* per prevenir SEL, es van utilitzar registres de redundància triple per minimitzar l'aparició de SEL, i es van utilitzar portes NAND sempre que va ser possible a canvi de portes NOR per millorar la immunitat a efectes d'acumulació de dosi.

Més enllà del disseny, també es va procedir a qualificar la resistència a la radiació amb els següents tests: un test de dosi ionitzant total (TID) amb un feix de protons amb 60 MeV i, un altre, d'efectes SEL i SEU amb un feix d'ions pesants. Van ser duts a terme al Centre de Ressources du Cyclotron a Louvain-La-Neuve (Bèlgica). No s'espera cap efecte de danys per desplaçament degut a neutrons degut a que la dosi en el detector serà baixa i la simulació no mostra efectes notables.

Particularment, el test de TID es va fer sobre 4 xips i s'hi va aplicar una dosi clarament superior a la esperada: 3 xips es van sotmetre a 55 krad i, un quart, a 40 krad. Es va caracteritzar els xips en cada pas d'irradiació i no es va detectar cap variació significativa en el seu rendiment ni les seves característiques: nivells de pedestal, gauny, *plateau*, *spill-over* i soroll.

En l'altre cas, el test de SEL i SEU, es va bombardejar dos xips sense encapsulat amb un feix d'ions pesants per avaluar-los sota una fluència total de 9.708×10^7 part/cm². No es va detectar cap SEL (es pot apreciar per un augment del consum o un curt-circuit). Per tant, es pot proposar un límit màxim de quants SEL es podrien donar en el detector, tenint en compte tots els xips a instal·lar i el temps de funcionament i no seria superior a 1 SEL en tota la vida del calorímetre. D'altra banda, els canvis en el valor d'un registre o SEU no es van detectar mentre l'electrònica estava en condicions de funcionament del detector, és a dir, aplicant un senyal de refresc en els registres de 10 kHz. Així, també es pot obtenir un límit de 1.3 al número de SEU que es podrien observar en tota la vida del sub-detector.

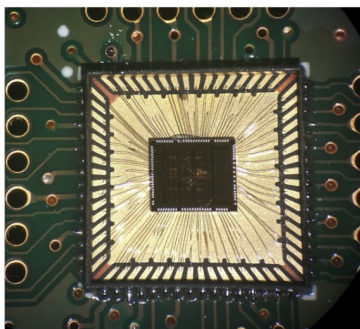


Figure 19 – Fotografia d'un xip sense encapsulat.

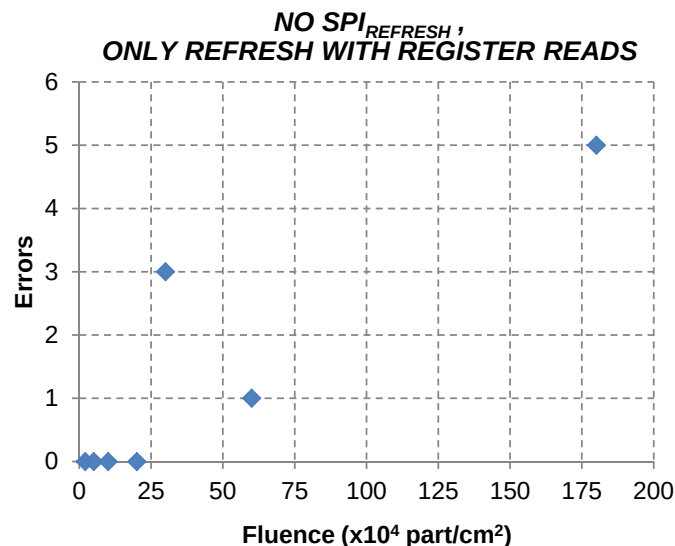


Figure 20 – Errors de lectura del protocol SPI durant un test d'irradiació sense senyal de refresc.

Conclusions

S'ha presentat el disseny d'un circuit integrat per l'actualització i millora del Calorímetre de l'LHCb. L'arquitectura del canal analògic proposada està preparada per filtrar, amplificar i integrar el senyal provinent d'un tub fotomultiplicador, després de 12 m de cable coaxial de $50\ \Omega$ a 40 MHz (freqüència d'encreuament de feixos de protons a l'LHC del CERN). Aquesta arquitectura ofereix una bona solució per capturar el senyals consecutius sense temps mort en aquest ritme. A més, el soroll que genera aquest disseny és prou baix com per compensar les necessitats tant restrictives de l'actualització del calorímetre. Tanmateix, també és capaç de corregir la component lenta dels polsos de manera que no afecti a les mesures immediatament posteriors. Altrament, en el circuit integrat s'hi inclouen línies de retard per sincronitzar tant les etapes internes com l'ADC extern de cada canal amb els senyals del detector. Finalment, una sèrie de registres interns donen valors als paràmetres clau dels canals per compensar les diferències degudes al procés de fabricació.

El xip ICECAL compleix amb els requeriments de l'electrònica analògica per l'actualització del calorímetre: una calibració de 4.5 fC/LSB per un rang dinàmic de 12 bits, un soroll $\lesssim 1$ comptes d'ADC (ENC < 4 fC), una no-linearitat menor que 1%, un residu de senyal menor que $\pm 1\%$ en les mostres anterior i posteriors (*spill-over*), i una estabilitat de l'integrador del 1% (*plateau*) durant 4 ns. Les característiques clau del processat de senyal analògic que permeten satisfer les especificacions són:

- Reducció del soroll que ofereix el circuit mitjançant l'ús d'una terminació activa en el preamplificador de corrent. En les condicions de l'actualització del Calorímetre, es reduirà el guany dels fototubs un factor 5 per reduir la seva degradació. Per tant, el soroll associat a l'electrònica s'ha de reduir també en el mateix factor.
- S'utilitzen dos sub-canals alternats per poder fer mesures consecutives sense temps mort a 40 MHz.
- S'empren una configuració diferencial per minimitzar els efectes en la integritat del senyal d'un sistema commutat.
- Un filtre amb un pol i un zero ajuda a reduir els efectes de la cua dels pols dels canals del Calorímetre. D'una banda, es minimitza la quantitat de senyal que s'integra en mostres immediatament anterior i posteriors. De l'altra, l'integrador es prou estable a la sortida com per variar poc en mesurar l'energia de partícules que arriben en moments diferents degut a la seva natura i a la posició dels canals en el detector.

- Línies de retard integrades al xip permeten una sincronització fina entre les diferents etapes de cada canal (integrador, Track-and-Hold, ADC), el detector i la resta de l'electrònica. Cada canal necessita un ajust diferent donat que el temps de propagació del senyal depèn de cada fototub, el seu voltatge d'alimentació i la longitud del cable.

Amb l'objectiu de reduir els efectes de la radiació que rebran els circuits integrats, es van aplicar tècniques específiques a nivell de disseny:

- L'ús de anells de guarda per prevenir efectes SEL en la tecnologia CMOS (incloent la modificació de les cel·les lògiques estàndard). Un altre efecte és la reducció del soroll i prevenir els efectes de l'acumulació de dosi.
- L'utilització de registres amb redundància triple per minimitzar els errors SEU en el que un bit canvia de valor, permetent mantenir la configuració del xip mentre està en funcionament.
- Fer servir portes NAND sempre que sigui possible enlloc de portes NOR, ja que millora la immunitat a efectes d'acumulació de dosi.

El disseny s'ha provat en diferents tests sobre 30 prototips de la versió final del xip: al laboratori, utilitzant el senyal referència obtingut amb un oscil·loscopi, en tests amb feixos d'electrons i canals de l'ECAL en una zona específica del CERN, i la seva resistència a la radiació al Centre de Ressources du Cyclotron a Louvain-la-Neuve.

Introduction

In order to study high energy physics, accelerators boost particles before they are collided inside the particle detectors to produce collisions which are analyzed in the search of new physics. The detectors are complex machines made of many layers of sub-detectors, each one contributing with information from the properties of the collision products. While tracking devices reveal the path of a particle, calorimeters stop, absorb and measure the energy of the particle, and particle-identification detectors use a range of techniques to find out the identity of a particle.

The calorimeters are one of those sub-systems and are commonly used to measure the energy of the particles which reach them. They are usually designed to deposit all of their energy and stop them. The calorimeter typical structure includes layers of absorbing high-density material interleaved with layers material that generate a light signal proportional to the energy of the particles crossing it. This signal is converted to an electric pulse that is processed and converted to a digital value, which is later stored. Frequently, particle detectors require a large number of channels.

Collating all the information from the different parts of the detector, physicists build up a snapshot of what was in the detector at the moment of a collision. The next step is to study the collisions looking for unusual particles, or for results that do not fit current theories.

The present document describes the work implemented to achieve a new circuit for the signal processing of the LHCb detector calorimeter upgrade, at CERN.

1.1 Thesis objectives

The objective of the present thesis is the development of an integrated solution for the analog signal processing in the LHCb Calorimeters Upgrade. The design of the circuit will have to comply with the following system specifications:

- The analogue signal processing will integrate a PMT pulse after a 12m 50 Ω coaxial cable in the crates at the calorimeter platform at 40 MHz, which is the frequency of events at the LHC at CERN. All the integration and shaping must last less than 25 ns with no dead time between consecutive events.
- In the upgrade conditions, the signal to noise ratio has to increase a factor 5 which implies a stringent condition in the noise of the circuit of $\lesssim 1$ ADC cnt (ENC < 4 fC).
- Other constraints include a gain of 4.5 fC/LSB for a 12 bit range, a non-linearity lower than 1%, spill-over less than $\pm 1\%$ and integrator plateau with 1% variation for 4 ns.
- Furthermore, the electronics will be exposed to radiation and are potentially sensitive to radiation damage due mainly to cumulated dose and single events effects. Dedicated techniques are needed in order to minimize the radiation effects and tests to be characterized.

1.2 CERN and the LHC

The European Organization for Nuclear Research, usually referred to as CERN for the French initials of *Conseil Européen pour la Recherche Nucléaire*, is a European research organization that operates the largest particle physics laboratory in the world. Created in 1954, it is situated on the Franco-Swiss border, near Geneva and has 22 member states and many other ones that are also involved in different ways. As a measure of the number of participants, CERN hosts about 10,000 scientists and engineers from 608 universities and research facilities from 113 countries around the world.

CERN's goals are to provide for collaboration among European States in nuclear research of a pure scientific and fundamental character, and in research essentially related thereto. The Organization has no concern with work for military requirements and the results of its experimental and theoretical work are published or otherwise made generally available.

CERN's main function is to provide the particle accelerators and other infrastructure needed for high-energy physics research, which is carried away in several large experiments constructed at CERN by international collaborations. CERN's largest accelerator, the Large Electron-Positron collider (LEP), which provided a detailed study of the electroweak interaction, began operating in 1989 and has a circumference of almost 27 kilometers. It was closed in 2000 to make way for the Large Hadron Collider (LHC), which became operational in 2010 and brings protons (and ions) into head-on collision at higher energies than ever achieved

before to allow scientists to study fundamental physics. Also, other colliders are part of the history of CERN, like the first proton-proton collider—the Intersecting Storage Rings (ISR)—commissioned in 1971, the first proton-antiproton collider—the Super Proton Synchrotron (SPS)—, and have provided great discoveries such as the W- and Z0 bosons or the existence of neutral currents. A part from the scientific discoveries, CERN is birthplace of the World Wide Web.

1.2.1 LHC experiments

Seven experiments at the Large Hadron Collider (LHC) use detectors to analyze the myriad of particles produced by collisions in the accelerator. These experiments are run by collaborations of scientists from institutes all over the world. Each experiment is distinct, and characterized by its detectors.

The biggest of these experiments, ATLAS and CMS, use general-purpose detectors to investigate a wide range of physics. Although they share the same scientific goals, having two independently designed detectors (they use different technical solutions) allow cross-confirmation of any new discoveries made. ALICE and LHCb have detectors specialized for focussing on specific phenomena. These four detectors sit underground in huge caverns on the LHC ring.

The smallest experiments on the LHC are TOTEM, LHCf and MoEDAL. TOTEM uses detectors positioned on either side of the CMS interaction point, while LHCf is made up of two detectors which sit along the LHC beamline, at either side of the ATLAS collision point, to focus on "forward particles". MoEDAL uses detectors deployed near LHCb to search for a hypothetical particle called the magnetic monopole.

A brief description of the four big experiments is included below:

ALICE [16] *A Large Ion Collider Experiment* is a general-purpose, heavy-ion detector designed to address the physics of strongly interacting matter and the quark-gluon plasma (QGP) at extreme values of energy density and temperature in heavy nuclei (Pb-Pb) collisions. The ALICE design (Fig. 1.1) is optimized for studying hadrons, electrons, muons, and photons from Pb-Pb collisions while being able to cope with the extreme particle multiplicity of each event.

ATLAS [17] *A Toroidal LHC Apparatus* is a general purpose experiment with the objective to test the Standard Model at the TeV scale, and to search for the Higgs boson and physics beyond the Standard Model. At 46 m long, 25 m high and 25 m wide, the 7000-tonne ATLAS detector (Fig. 1.2) is the largest volume particle detector ever constructed. It consists of a series of ever-larger concentric cylinders around the interaction point where the proton beams from the LHC collide. It

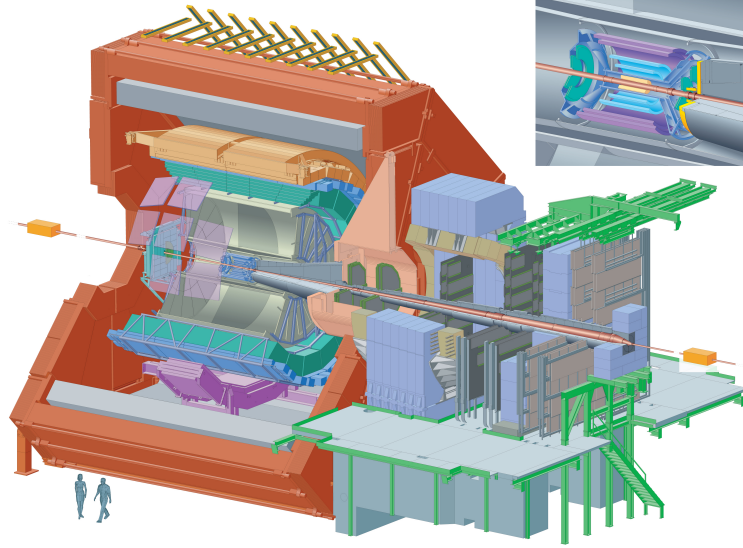


Figure 1.1 – ALICE detector (Image: CERN).

can be divided into four major parts: the Inner Detector, the calorimeters, the Muon Spectrometer and the magnet systems. They record the paths, momentum, and energy of the particles, allowing them to be individually identified. A huge magnet system bends the paths of charged particles so that their momenta can be measured.

CMS [18] The *Compact Muon Solenoid* is a multi-purpose apparatus with the main aim of elucidating the nature of electroweak symmetry breaking for which the Higgs mechanism is presumed to be responsible, as well as testing the mathematical consistency of the Standard Model at energy scales above 1 TeV. It has the parallel scientific goals to the ATLAS experiment, but it uses different technical solutions and a different magnet-system design. The CMS detector (Fig. 1.3) is built around a huge solenoid magnet. This takes the form of a cylindrical coil of superconducting cable that generates a field of 4 tesla. The field is confined by a steel “yoke” that forms the bulk of the detector’s 14,000 tons weight.

LHCb [1] The *Large Hadron Collider beauty* experiment (Fig. 1.4) is dedicated to the study of CP violation and rare decays in the b-sector. Instead of surrounding the entire collision point with an enclosed detector as do ATLAS and CMS, the LHCb is a single-arm forward spectrometer that uses a series of subdetectors to detect mainly forward particles - those thrown forwards by the collision in one direction. The first subdetector is mounted close to the collision point, with the

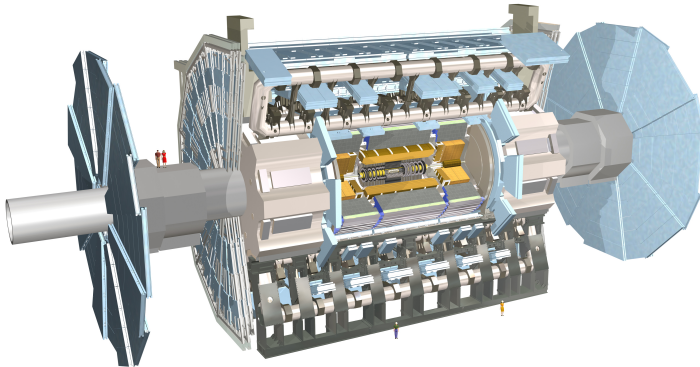


Figure 1.2 – ATLAS detector (Image: CERN).

others following one behind the other over a length of 20 metres. It is described in more detail in Sec. 1.3.

1.3 The LHCb experiment

The LHCb experiment is dedicated to the study of heavy flavor physics at the LHC [1] [19] [20]. Its main target is to make precise measurements of CP violation and rare decays of beauty and charm hadrons. In other words, the experiment specializes in investigating the slight differences between matter and antimatter by studying a type of particle called the "beauty quark", or "b quark".

An abundance of different types of quark are created by the LHC before they decay quickly into other forms. To catch the b quarks, LHCb has developed sophisticated movable tracking detectors close to the path of the beams circling in the LHC.

Contrary to the ATLAS, CMS or ALICE, that surround the entire collision point with an enclosed detector, the 5600-tonne LHCb detector is made up of a forward spectrometer and planar detectors. It is 21 metres long, 10 metres high and 13 metres wide, and sits 100 metres below ground, at Interaction Point 8 of the LHC accelerator, previously used by the DELPHI experiment from LEP.

The LHCb experiment will improve significantly results from earlier experiments both quantitatively and qualitatively, by exploiting the large number of

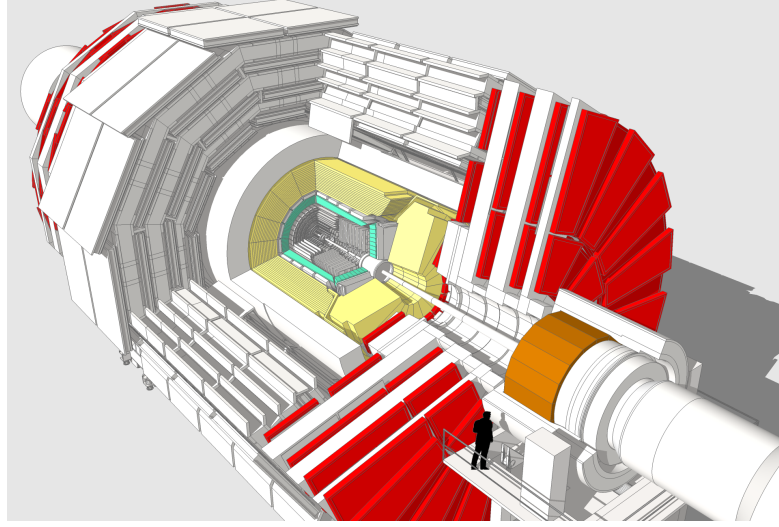


Figure 1.3 – CMS detector (Image: CERN).

different kinds of b hadrons produced at LHC, thanks to

1. A good trigger efficiencies for b -hadron final states with only hadrons, as well as those containing leptons.
2. The capability of identifying kaons and pions in a momentum range of to above $100 \text{ GeV}/c$.
3. An excellent decay time and mass resolution.

The LHCb spectrometer shown in the Fig. 1.4 consists on a beam pipe, a magnet, the Vertex Locator (VELO), four stages of tracking system, two Ring Imaging Cherenkov, the calorimeters, the Muon System, and the Trigger.

The LHCb trigger has two decision levels. Using custom made electronics, the first decision is made based on high transverse momentum hadrons or electrons found in the calorimeter system, or muons found in the muon system, at the bunch crossing rate of 40 MHz. All data from the detector are then read out at a rate of 1 MHz and sent to a CPU farm for further event reduction. For this purpose, all the detector information is available.

1.4 The LHCb Calorimeter detector

The LHCb calorimeter system [4] is designed to stop most of the particles coming from a collision as they pass through the detector, measuring the amount of energy deposited in the system until the particle stops. The technology used, named

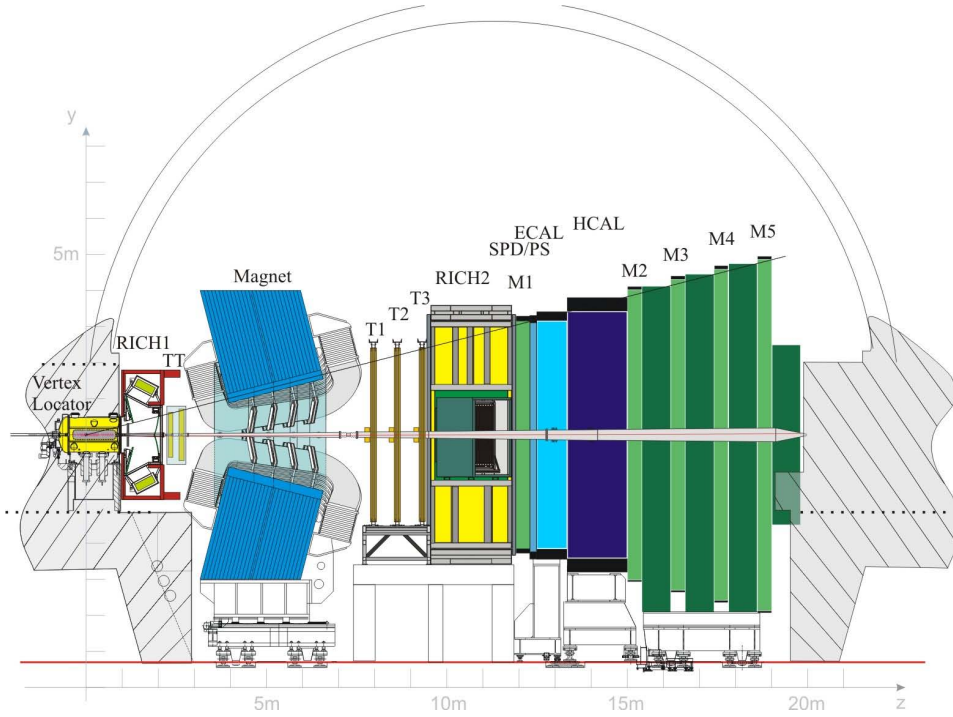


Figure 1.4 – Schematic of the LHCb detector (Image: CERN).

Shashlik (Fig. 1.6), consists of alternated layers of "passive" or "absorbing" high density material (iron and lead) and layers of scintillator. When particles hit the metal plates, they generate showers of secondary particles. Those secondary particles generate light in the scintillators, as they excite polystyrene molecules. The amount of light is proportional to the energy of the original particle that hit the channel.

The full Calorimeter (Fig. 1.8) is composed of the pad/preshower Detector (SPD/PS), the Electromagnetic CALorimeter (ECAL) and the Hadronic CALorimeter (HCAL). The electromagnetic calorimeter is responsible for measuring the energy of lighter particles, such as electrons and photons, while the experiment's hadron calorimeter samples the energy of protons, neutrons and other particles containing quarks.

The Calorimeter is used for particle identification of electrons, photons and hadrons, as well as for their energy and position measurement. The accurate reconstruction of π^0 and prompt photons is essential in the study of radiative B decays, and also in flavor tagging. Moreover, the calorimeter participates in the first level of the trigger of the detector by selecting high transverse energy hadron, electron and photon candidates.

The segmentation is approximately projective in the direction of the interaction

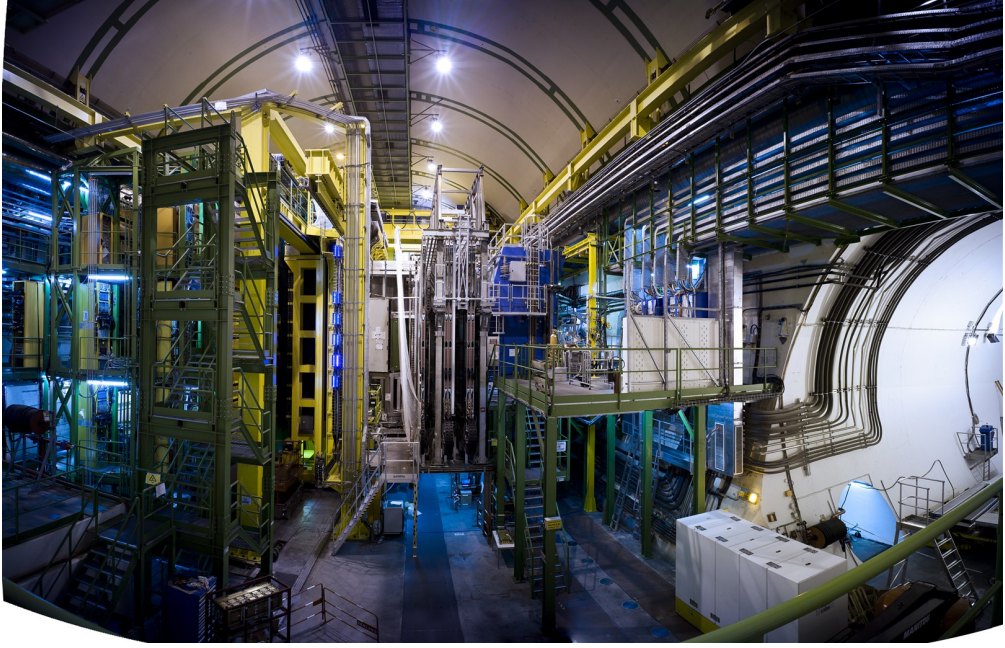


Figure 1.5 – The LHCb detector as seen from the barracks (Image: CERN).

point to get a fast evaluation of the trigger candidates. The SPD/PS, ECAL and HCAL have variable lateral segmentation to avoid a large range of cell occupancy, as the hit density varies by two orders of magnitude as a function of the distance to the z -axis. A segmentation into three different sections with different cell sizes was chosen for the ECAL, and projectively for the SPD/PS. Given the dimensions of hadronic showers, the HCAL is segmented in two zones with larger cell sizes.

All the calorimeter subdetectors are based on the same basic concept: scintillating light is transmitted to PhotoMultiplier Tubes (PMT) by wavelength-shifting (WLS) fibers. The fiber bunches in the ECAL and HCAL require individual phototubes. In order to have a constant transverse energy (ET) scale over the whole detector acceptance, the gain in the ECAL and HCAL phototubes is set as a function of their distance to the beampipe. Furthermore, since the light yield delivered by the HCAL modules is a factor 30 less than that of the ECAL, the HCAL tubes operate at a higher gain.

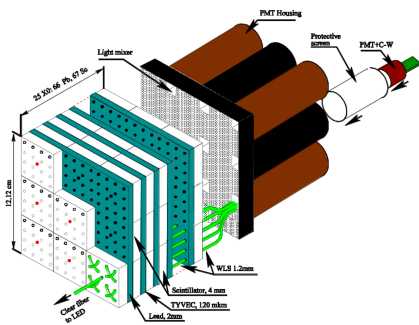


Figure 1.6 – ECAL channel Shashlik technology.



Figure 1.7 – ECAL channels.

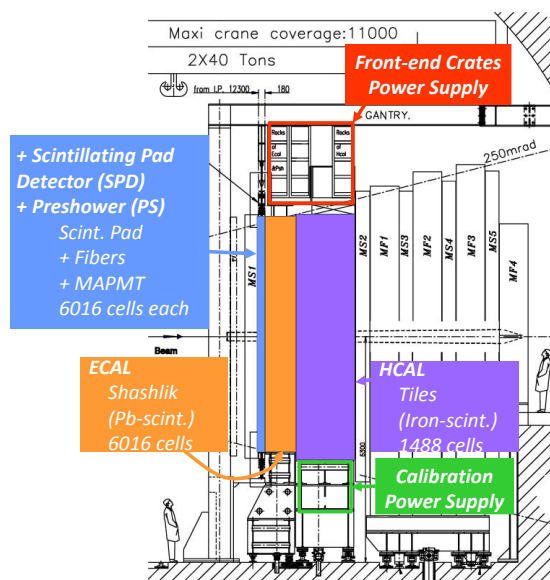


Figure 1.8 – Calorimeter system.

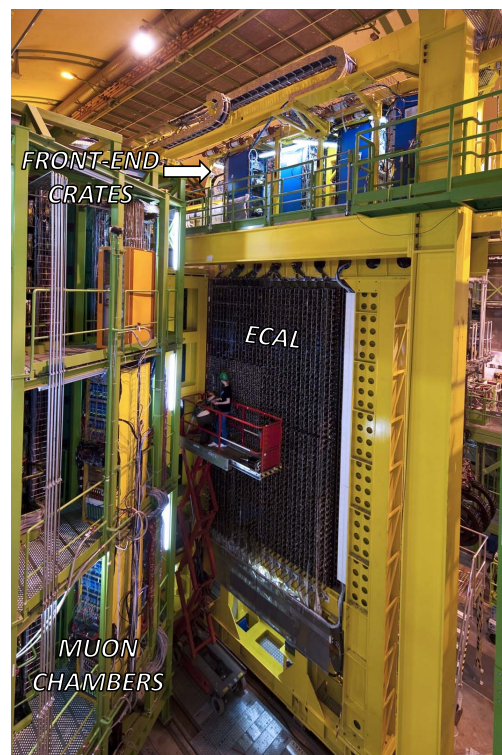


Figure 1.9 – ECAL A-side as seen from the muon chambers to the vertex (Image: CERN).

The Calorimeter Upgrade Electronics

2.1 The LHCb detector Upgrade

Significant amount of data has been taken since the LHC start-up with a data quality which permitted to make important measurements. Among others, the B_s meson decay in a pair of muons and other new decays of the B_s have been observed, the B_c mass has been measured with the best precision ever.

The performances of the detector are very satisfactory although the beam conditions have been far more aggressive than what was foreseen during the design period. The pile-up (the average number of pp interactions in visible events) was roughly 1.7 in 2012, in spite of the expected nominal conditions foreseen to be 0.4 during the installation of the detector. The confidence of the collaboration in the detector justified those conditions, the gain in statistics being larger than the relative degradation of the data quality due to the higher number of collisions per crossing.

Since a few years, the upgrade of the LHCb detector is being prepared in order to improve the measurements in major areas of flavour physics and to reach ultimately the theoretical uncertainties in several fields [21], [2]. The upgrade will take place during the long shut-down of 2019 (LS2) and should permit to increase the instantaneous luminosity up to $2 \times 10^{33} \text{cm}^{-2} \cdot \text{s}^{-1}$ (about ten times the present one). All the sub-detectors are affected by this upgrade. The pile-up leads to some drastic modifications of the tracking and particle identification systems. But, the most important modification concerns the first hardware trigger (L0) which is removed. A pure software trigger, more efficient and more flexible remains. The suppression of the L0 implies that each sub-detector sends its data at 40MHz to the computer farm on which the trigger program is running. Estimations of the impact of the software trigger (not considering the increase of luminosity) show that the event yield will be more than doubled in B meson hadronic decays (the

improvement could be larger for high multiplicity final states with up to 6 charged particles), after the suppression of the present hardware trigger.

The first level trigger disappears, but part of its electronics can be re-used and adapted in order to reduce the bandwidth at the input of the PC farm. The purpose here is not to limit the bandwidth systematically at a fixed rate like the L0 does, but to reduce the bandwidth between 1 and 40 MHz (i.e. no filtering), depending on the needs and altogether to enrich the sample. The reasons for such a Low Level Trigger (LLT) are a possible staggering of the size of the PC farm at LHC start-up or an occasional problem on the farm.

The calorimeter system of LHCb [4] (Fig. 1.8) evolves by reducing its complexity, the present scintillating pad detector and the preshower being removed. Their disappearance is compensated by the future software trigger and the improved tracking system. The module performances can be affected by radiations. Hence, some of the cells in the inner region (the closest to the beam pipe) may be replaced during LS2. The calorimeter of LHCb, like the other sub-detectors should adapt its electronics (common to the electromagnetic and hadronic calorimeters) to the new running conditions of the upgrade. The consequences of the upgrade for the electronics are:

- the readout of the data is done at 40MHz;
- the gain of the PMT is reduced by a factor 5 in order to keep them alive during the high luminosity run, this reduction is compensated by an increase of the gain of the electronics (without increasing of the noise with respect to the present system);
- the calorimeter implementation of the first level trigger is adapted to the new low level trigger.

This implies the conception of a new front-end electronics and a full revision of the electronics architecture.

2.1.1 The front-end board

The upgraded LHCb calorimeter system is made of two sub-detectors: the electromagnetic and hadronic calorimeters, ECAL and HCAL, respectively. They share the same front-end boards (FEB) [3]. A total of 248 boards is necessary, each one receiving the signal of 32 photo-multipliers. The boards are dispatched in 2×14 ECAL and 2×2 HCAL crates, the factor 2 corresponding to the 2 sides of the detector.

A couple of extra FEB are necessary to acquire the pulses from the pin-diodes producing reference signals for the calibration system of the calorimeter. The

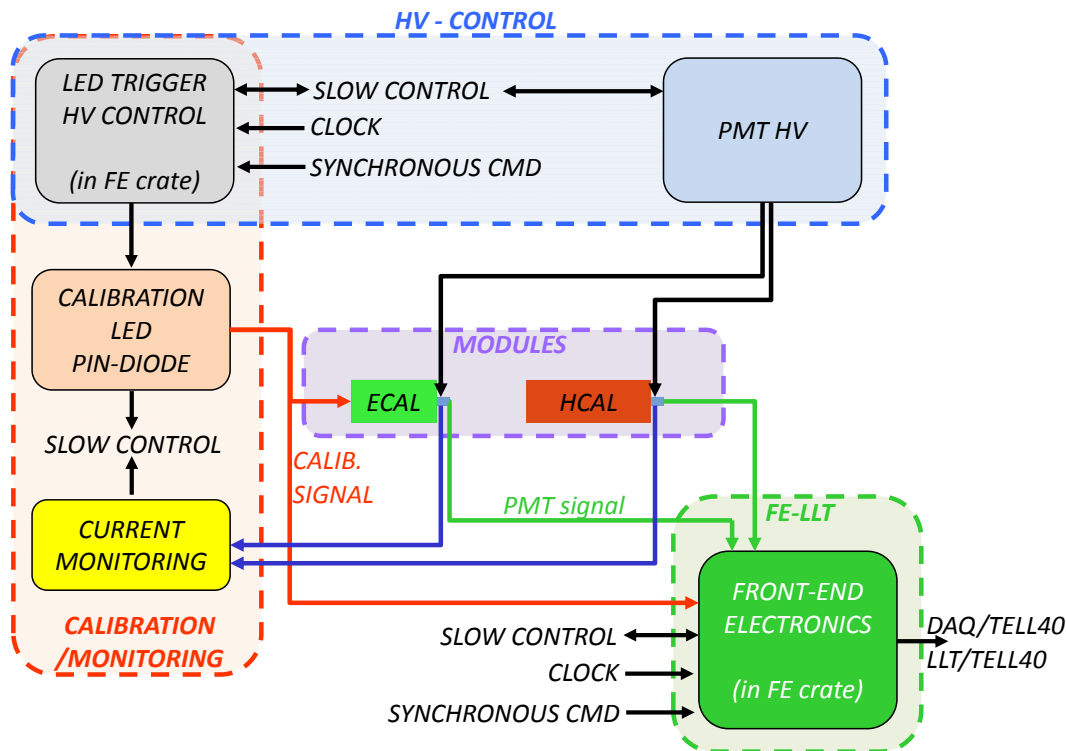


Figure 2.1 – Schematics of the Calorimeter system.

trigger of the LED is controlled by the LEDTSB boards, also plugged into the same crates and receiving the calibration synchronous commands. At the center of each crate is located the control board.

The Front-end electronics receives from the detector the signals of the photo-multipliers which are sampled at the LHC clock frequency. The sampling is done on the FEB, after shaping and integration. Sub-events corresponding to 32 channels are built and sent to the central LHCb acquisition, or TELL40 boards, through 4 fibers. In parallel, some quantities required by the Low Level trigger (LLT) are evaluated and sent to the TRIG40 boards, thanks to a fifth fiber on the boards.

The FEB must receive several signals from the counting room. Those signals are:

- the LHC (or internal LHCb when the machine is empty) clock,
- the slow control to configure and monitor the system,
- the synchronous and fast command.

Those signals are brought to each FEB crate with optical fibers and with the GigaBit Transceiver (GBT) protocol [22]. The control board receives the signals and propagate to the backplane where they are distributed the FEB and also to the other boards of the crates.

2.2 Preceding electronics

Before discussing in detail the necessity of new analog electronics, it is convenient to review several designs that provide solutions to problems similar to the ones to be found in the LHCb Calorimeter.

2.2.1 Present Calorimeter analog electronics

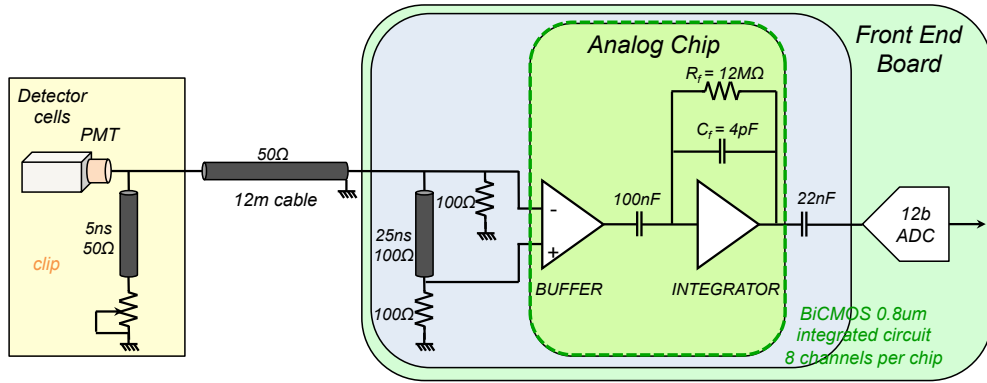


Figure 2.2 – Present analog electronics block diagram.

The analogue signal processing in the present ECAL Front End (FE) board ([1], [4], [3], Fig. 2.2) is mostly performed by a shaper ASIC that integrates the PMT pulse, which has been clipped at the PMT base. The PMT is located at the detector; the signal is transmitted through a 12m 50Ω coaxial cable to the FE board located in the crates at the calorimeter platform.

At the LHCb there can be consecutive signals at 40 MHz. In order to measure at every bunch crossing while being insensitive to spill over it is necessary to shape the signals and get rid off the small tail of the pulses extending after 25 ns. The photo multiplier pulse is narrowed by a clipping line at its base (Fig. 2.3). The length of the line is selected so the FWHM is about 10 ns. The resistor load (Fig. 2.2) is adjusted to obtain a return to a 0 V level after clipping. Of course, the cancellation of the later part of the pulse by the pulse reflected by the clipping line is only exact on average. There are fluctuations due to variations of the

number of the photoelectrons with time, but their effect is small due to the large number of the photoelectrons. The distortion of the ~ 12 m coaxial cables on the pulse-shape is compensated by a pole-zero circuit placed after the integrator (not in the scheme depicted in Fig. 2.2).

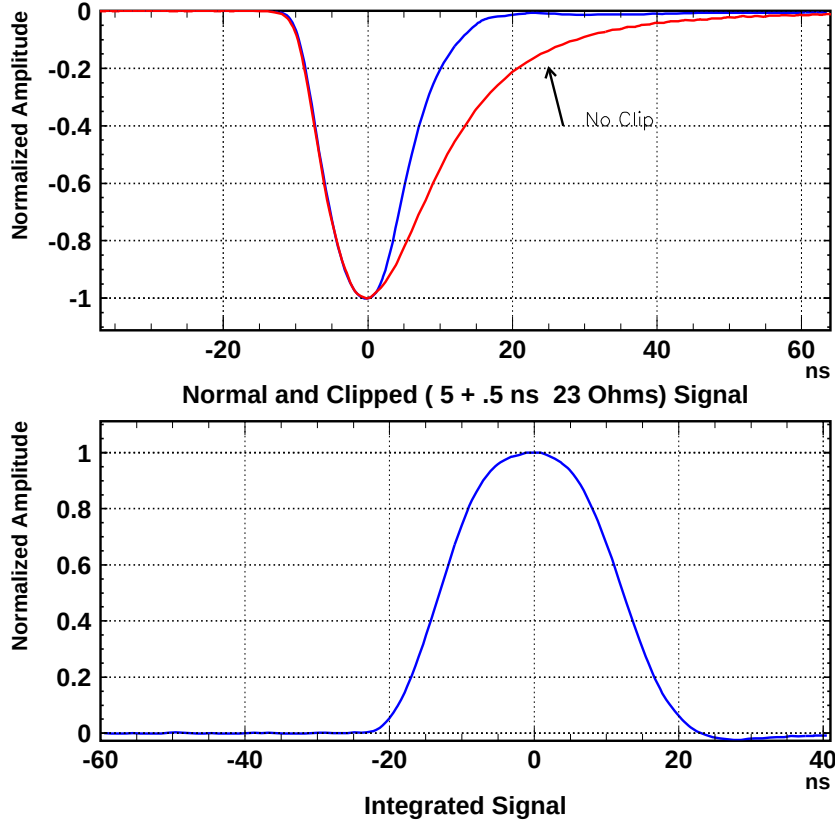


Figure 2.3 – The upper figure shows the PM signal before and after the clipping, the lower one shows the same signal at the output of the integrator.

The ASIC used for integration was designed in AMS $0.8 \mu\text{m}$ BICMOS technology. The reset or discharge of the integrator is performed with a clever circuit; the same pulse is delayed 25 ns by a lumped-element delay line, inverted in a buffer and, then, integrated.

Right after digitization, dynamic pedestal subtraction is performed. It consists on subtracting the smaller of the two previous samples. Hence, it is a type of Correlated Double Sampling (CDS), needed to cancel baseline fluctuation and low frequency (LF) pick-up noise.

2.2.2 PS and SPD electronics solutions

The SPD and PS are two subsystems of the present LHCb Calorimeter [4] (as presented in section 1.4). They are two planes of scintillator pads separated by a 12 mm thick lead sheet. The transmission of the light is done by long clear fibers to multi-anode photomultiplier tubes (MAPMT) that are located, along with the Very Front End (VFE) electronics in boxes above and below the detector in order to optimize the light yield at the MAPMTs. For economical reasons a multianode (Ma)PMT is chosen as photo detector. To handle the data for the first trigger level as quickly as possible, the signals are shaped directly at the VFEs. While on the PS the VFE just shapes and integrates the signal, the SPD VFE includes a discriminator telling whether a cell has been hit. The PS signal is digitised in the Front End (FE) electronics placed in crates on top of the calorimeter detectors after 20-30 m of cable (Fig. 2.4). The FE boards hold the data of each channel, sampled at 40 MHz, in digital pipelines waiting for the first level trigger decision. Next to the FEs, the SPD Control Boards (CB) includes the functionality necessary to configure the SPD VFEs and deliver the SPD multiplicity trigger.

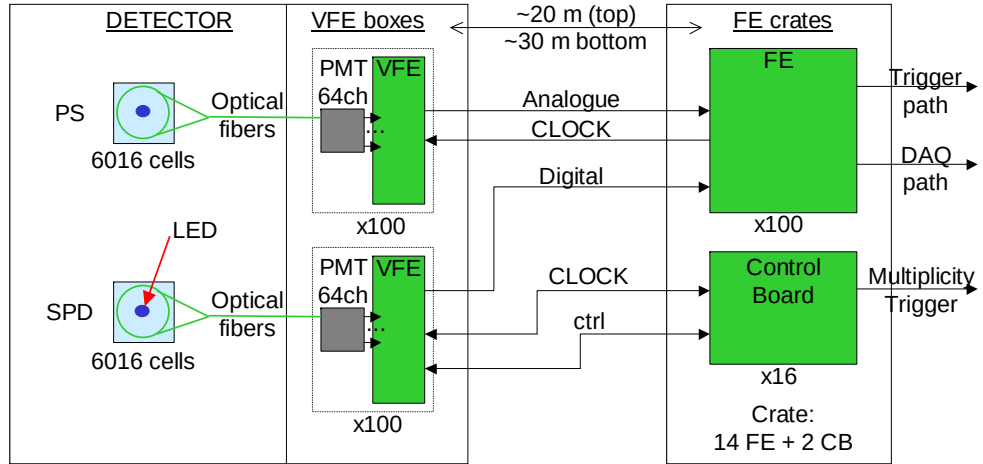


Figure 2.4 – PS/SPD readout electronics scheme.

PS

The solution adopted [23] is to alternate every 25 ns between two integrators and to reset one integrator when the other one is active (Fig. 2.5). The signal is sampled by track-and-hold circuits and the output of the active integrator is chosen by a multiplexer, followed by a twisted-pair cable driver. All circuit elements are

functioning in differential mode to improve the stability and pick-up noise rejection. The amplifier integrator circuits were realized in monolithic AMS 0.8 μm BiCMOS technology implementing 8 channels per chip.

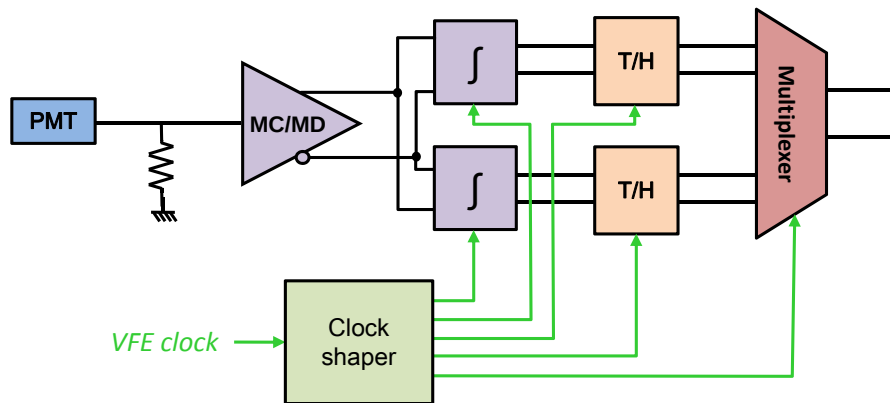


Figure 2.5 – PS ASIC diagram.

SPD

In the SPD [24] [25], the PMT signal is amplified, shaped and discriminated through an 8 channel ASIC (AMS BiCMOS 0.8 μm technology). Figure 2.6 shows the functional architecture of each channel. The configuration is based on two interleaved processing units per channel to avoid any dead time and to be able to perform the pile-up compensation. The bunch-crossing clock is divided (outside the chip) and then used to multiplex by level the two paths of the channel each 25 ns. To prevent digital crosstalk on sensitive analogue parts, all the blocks are fully differential. Each path uses an independent DAC to be able to compensate the offsets due to process variations between different sub-channels.

Both PS and SPD solutions do not require external components such delay lines, which is important for room reasons. The bunch crossing clock is divided and then used to multiplex by level the two paths of the channel each 25 ns. To prevent digital crosstalk on sensitive analogue parts, the latter are fully differential.

2.2.3 ATLAS LAr

Due to its low now noise requirements, the ATLAS Liquid Argon (LAr) electronics design approach was considered. LAr calorimeters [26] in ATLAS (Sec. 1.2) are

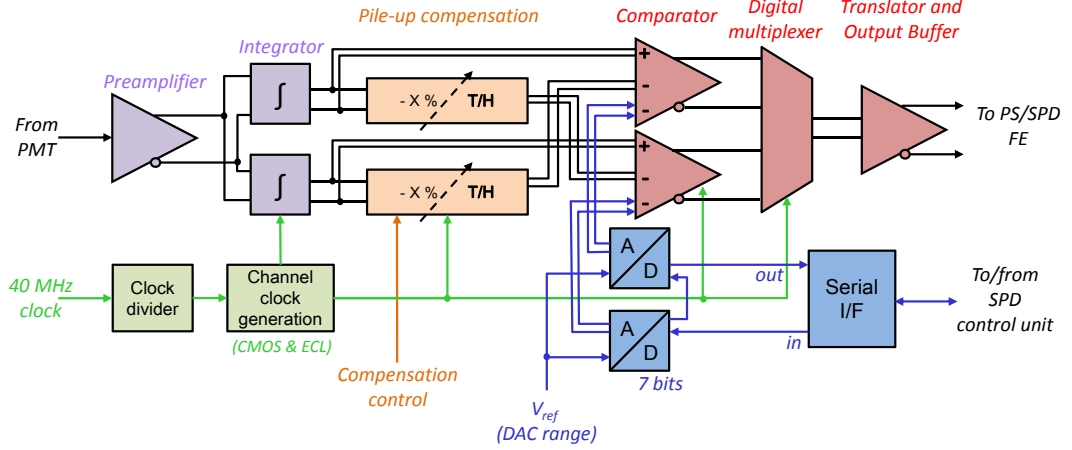


Figure 2.6 – SPD ASIC scheme.

high precision, high sensitivity and high granularity detectors designed to provide precision measurements of electrons, photons, jets and missing transverse energy. The LAr calorimeters consist of four sub-detectors and are contained within three cryostats between the inner tracking detectors and the outer muon chambers. It is constructed of a series of cathode and anode plates submerged in liquid argon. Charged particles traversing it ionize argon atoms and create a current pulse on the positively charged anode that lasts for the 400 ns electron drift time. The signal is conveyed to the front end electronics, located outside the detector via a 5 m and 25 Ω cable.

To prevent multiple reflections, the transmission lines must be terminated in its characteristic impedance. A passive component resistor should not be used as, in this case, it would be the dominant noise source. The discrete components preamplifier installed in the LAr front-end boards provides an electronically "cooled termination". The circuit is a common gate with double voltage feedback. The inner loop reduces the input impedance preserving the linearity and with low noise performance. The outer loop is designed to control the input impedance accurately.

$$Z_{in} = \frac{\frac{1}{g_{m1}} + R_{E1}}{G} + \frac{R_{C1}}{1 + \frac{R_2}{R_1}} \quad (2.1)$$

where

$$G \simeq \frac{1}{\frac{1}{g_{m2}} + R_1} R_{C2} \quad (2.2)$$

Transimpedance gain of the circuit is given by R_{C1} and a low noise performance

0.5 nV/ $\sqrt{\text{Hz}}$ is achieved.

For the ATLAS upgrade, an analog front-end chip LAPAS (Liquid Argon PreAmplifier Shaper) was designed for IBM 8WL 0.13 μm SiGe (silicon-germanium) BiCMOS technology [27]. The preamplifier design of LAPAS chip is based on low noise line-terminating circuit topology presently used in LAr calorimeters [28]. It has full 16-bit dynamic range and very low noise (~ 0.26 nV/ $\sqrt{\text{Hz}}$). The shaper design of LAPAS chip is fully differential and based on $CR - (RC)^2$ topology with two gain settings ($\times 1$ and $\times 10$). The output driver is adjustable, it is compatible with both gain selector block and differential ADC, either 2.34 V or 1.2 V.

2.3 Proposed Calorimeter Upgrade analog electronics

In order to reduce the PMT ageing, the gain has to be decreased by a factor 5 with respect to the present operation HV in order to keep the same average current after the increase in luminosity¹. Therefore, the preamplifier input equivalent noise must be decreased accordingly so that output noise is at the level of 1 LSB, or an input referred Equivalent Noise Charge (ENC) < 4 fC. The dynamic pedestal subtraction is calculated once the signal has been digitized. Although it has proven to be decisive for pedestal cancellation and low frequency pick-up noise, it increases the noise in the signal bandwidth, ideally by a factor $\sqrt{2}$ provided both samples are not correlated.

Table 2.1 summarizes main requirements for the analogue FE of the calorimeter system. Except for PMT current and noise, the other requirements are similar to the ones for the current ECAL front end ([1], [4], [3]).

Several options were studied to meet noise requirements [5] [29]. Considering the required ENC (4 fC), the noise requirement for a standard high input impedance voltage amplifier and a 50 Ω termination resistor is not acceptable. Line termination can be achieved also by an active circuit with controlled input impedance, which is usually referred as “electronically cooled termination”, which helps reducing the noise requirements of following the electronics in more than a factor 2 (a detailed explanation can be found in Sec.3.2). An ASIC development was proposed because the FE board has 32 channels and a transistor level approach was required for any active termination scheme.

However, it is important to take into account that currently the PMT signal is clipped in the base, i.e. at the detector, and about 2/3 of the signal charge

¹According to Hamamatsu PMT specifications, a 20% gain reduction may be expected per integrated charge of 100C (the expected charge in total in present conditions and worst PMT position).

Requirements	
Energy range	$0 \leq E_t \leq 10\text{GeV}$ (ECAL)
Calibration/Resolution	4fC/2.5MeV per ADC count
Dynamic range	4096-256 = 3840 cnts: 12 bits
Noise	$\lesssim 1$ ADC cnt (ENC < 4 fC)
Termination	$50 \pm 5\Omega$
Baseline shift prevention	Dynamic pedestal subtraction
Max. peak current	4-5 mA over 50Ω
Spill-over residue level	$\pm 1\%$
Integrator peak plateau	<1% variation in $\pm 2ns$
Linearity	< 1%
Cross-talk	< 0.5%
Timing	Individual (per channel)

Table 2.1 – Summary of the requirements for the calorimeter analog FE.

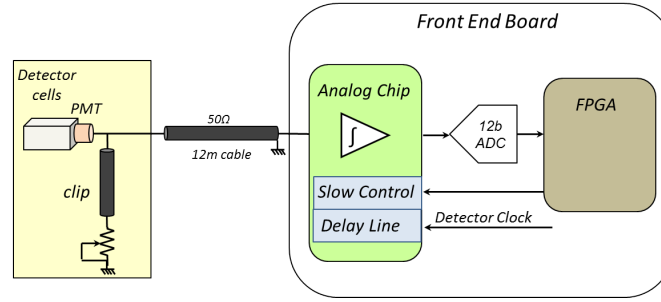


Figure 2.7 – Integrated solution block diagram.

are lost. An alternative solution consists in removing the clipping of the PM base and perform it after amplifying the signal in the FE card. This would relax by a factor 3 the noise requirement of the front end amplifier, thus allowing a passive termination. Although this solution requires intervention in the detector, the operation is feasible. Such a solution, based on Commercial Off-The-Shelf (COTS) Op Amps and analogue delay lines was tested and kept as a back up solution in case severe problems arise during radiation qualification of the integrated solution [30].

After analogue signal processing, the signal must be digitized through a 12 bit ADC at 40 MHz. Baseline candidate is the AD9238 ADC, which is a dual pipeline ADC. Its sampling frequency ranges from 20 to 65 MHz. And it has been qualified for the radiation environment levels expected in the front-end boards.

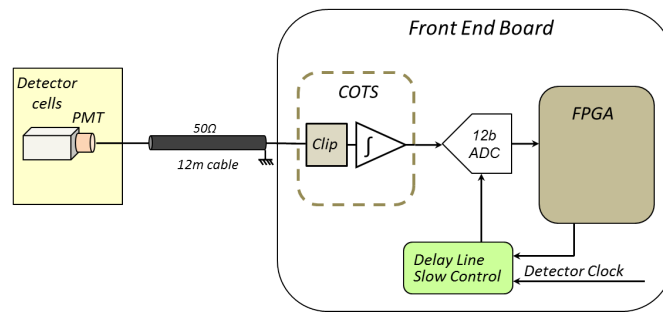


Figure 2.8 – COTS solution block diagram.

2.4 LHCb Calorimeter Upgrade COTS

By removing the clipping from the PMT base and performing it at the front-end level, the signal to noise ratio at the input stage is improved. Removing the clipping is a simple operation which can be done by cutting a PCB track on the bases. Their replacement is not foreseen as it would require a much more involved operation on the detector with a higher risk for its integrity. Under these conditions the actual clipping-subtraction-integration scheme might be kept, provided all steps are performed at the FEB level. Delay lines are necessary in this case and a discrete component solution, preferably with Commercial Out-of-The-Shelf (COTS), was envisaged [31] [30]. Its scheme is shown in figure 2.9.

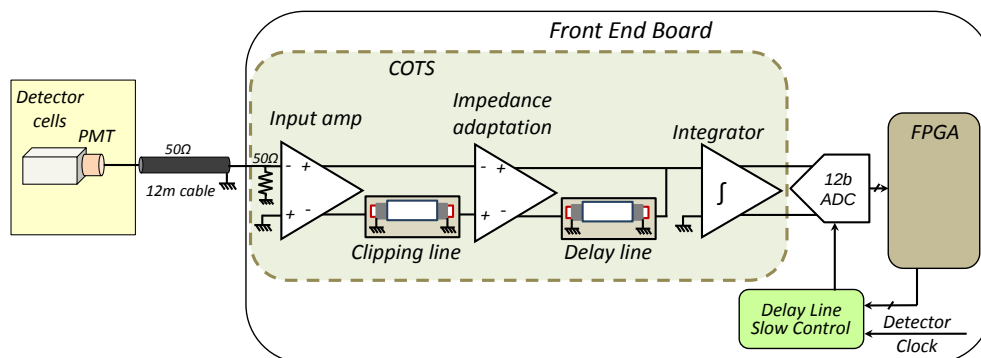


Figure 2.9 – COTS solution schematics.

The clipping being done on the FEB, the input signal is amplified before. It is important that the first amplifier has a low noise and not too large a bandwidth to avoid that the noise is amplified in irrelevant parts of the spectrum. The scheme used to clip the signal on the FEB is composed by a first amplifying stage

and by an operational amplifier subtracter that receives appropriately scaled and delayed signals. This clipping scheme is similar to the one described in [4] but using differential operational amplifiers to generate both polarities for the signals instead of using transmission line reflections. The parameter value is chosen after studying the response to the actual signal shape in order to obtain the desired clipping.

The next step in the analog processing is the integration, which is performed by a differential operational amplifier with capacitive feedback loop. Its structure is similar to the clipping one. The main difference is that the delay line is much longer (25 ns) and that there is no attenuation. The clipped signal is integrated and then disintegrated dynamically with a 25 ns delay without involving any switch.

Then, the analog levels are adapted to the ADC input through an AC coupling and bias resistances. However, some drawbacks must be taken into account. The system is AC coupled and thus will suffer a baseline shift. The shift will depend on the pulse amplitude, the pulse rate and the speed at which the capacitors discharge. Hence, relatively big capacitors have been chosen for this purpose, both because they should have a small influence in the concerned frequency domain and because, in the time domain, undershoots will last longer and have a lower amplitude. Anyway, the related time constant was decided to be 5 μ s in order not to be too long and avoid the effects of the empty fill period between collisions. This affects the ADC adaptation specifically, but may also be applied to the rest of the AC couplings of the system. Five percent of the dynamic range of the ADC has been reserved to prevent any saturation. Also an extra two percent have been reserved for the noise.

Finally, special care was taken to keep the inputs of the operational amplifiers balanced. Both polarities have equivalent impedances. The power integrity and EMI have been carefully studied to avoid ruining a low noise circuit with external interferences.

2.5 ASIC solution: ICECAL

The integrated solution is implementation on an ASIC named ICECAL. The third version of the chip, ICECALv3, includes (figure 2.10): four analog channels with programmable values to control the key parameters and compensate for process variations; a dedicated Delay Locked Loop (DLL) to synchronize each channel signal phase and a digital interface using SPI protocol [32].

The analog channel is based on two alternated switched signal paths where the input current is first amplified and converted to differential signals in order to be integrated through a fully differential amplifier with capacitive feedback. The integration is performed by two alternate integrators running at 20 MHz,

one being readout and reset while the other is active. A fully differential signal processing is adopted in order to minimize the impact of common mode noise, which is important in a switched system.

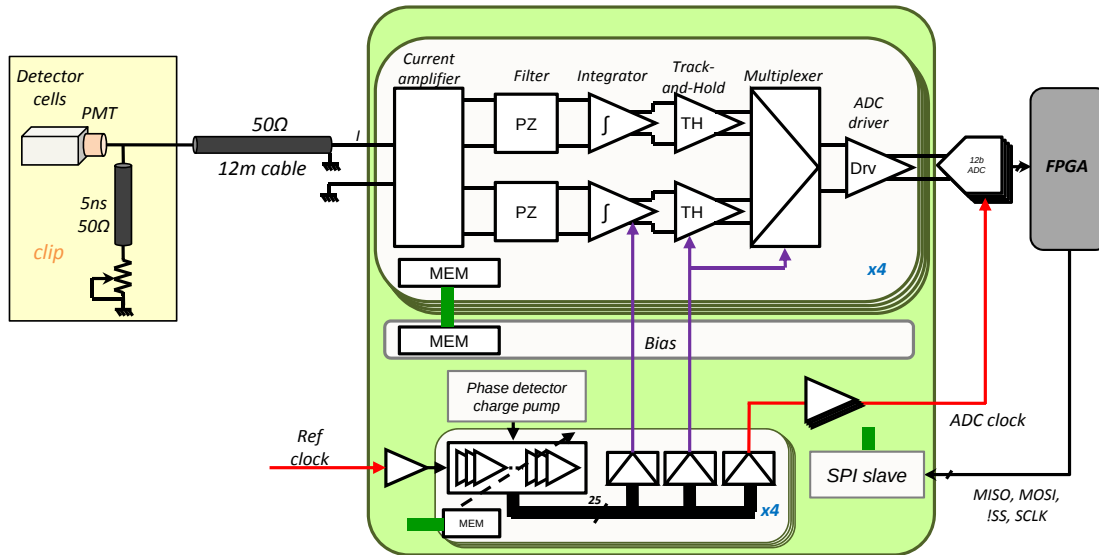


Figure 2.10 – ASIC schematics.

The input stage is a current preamplifier with a cooled termination to reduce the noise. The input impedance has to be fixed at $50\ \Omega$.

A pole zero filter stage helps to remove the effects produced by the twelve meter cable in order to meet the spill-over and integrator output stability specifications.

Then, the signal is integrated with the switched integrators. Two differential 20 MHz clock signals open or close the switches to set two states: integration and reset. Integration of the full pulse should be finished during the 25 ns to minimize the spill over in the following clock cycles. The reset sets to zero the integrator stage output. Programmable feedback capacitors not only integrate, they are a simple tool to calibrate the gain of the channel.

A Track-and-Hold samples the integrated signal and provides a stable output. The accuracy required for 12 bit and by using half of the clock for slewing and settling the output signal fixes its gain specifications. The non-linearity has to be less than 1% for the full output range (up to 2V). The FDOA used for the integrator is also used for the Track and Hold. An analog multiplexer selects the correct sub-channel to be processed further. Finally, an output buffer provides the adequate output impedance to be connected to the ADC.

The full description of the stages is treated in detail in section 3.

As each channel of the detector presents different latencies due, essentially, to the PMT high voltage, it is necessary to be able to select the sampling time for each one. The exact delay is hard to evaluate at design time, so tunable delays are recommended. The need to automate the synchronization procedure and the accessibility limitations of the electronics imply using digital programmable delay lines, which in the present design are included in the ASIC (figure 2.10). Each channel includes a DLL which generates 3 independent LVDS clock signals with configurable clock phases in order to delay the LHC clock (40 MHz) in intervals of 1 ns, between 0 and 24 ns, for the switched integrator, the track-and-hold, and the external ADC. The DLL implementation is fully differential, so that switching noise is lower in comparison with single mode one. This block receives the reference differential CMOS clock signal that passes through a Voltage Controlled Delay Line (VCDL), then a multiplexer selects the desired output, and implements the phase comparator which generates the fine-grain control voltage. Two signals, V_{coarse} , which is an external and fixed bias voltage, and V_{control} ensure that the introduced delay by each VCDL stage is 1 ns.

Three ASIC prototypes have been designed, fabricated and tested in Austriamicrosystems 0.35 μm SiGe BiCMOS technology. This technology allows a 3.3 V operation and has fast HBT transistors, which are quite useful for high dynamic range operation, such as the one we require. In particular the high transconductance versus bias current ratio of bipolar transistors is very useful to achieve good linearity in current mode solutions.

Analog channel

3.1 Analog channel design

From all the specifications (table 2.1), there are mainly two constraints that will define the approach for the design of the analog channel:

1. Low noise.
2. Shaping and integration must last less than 25 ns
3. No dead time between consecutive events.

It is possible to reduce the noise at the channel by using an active termination, avoiding resistor termination and its thermal noise (see section 3.2). It is usually referred as "electronically cooled termination". Conventionally it is created by an operational amplifier with capacitive feedback. This solution works well, provided that the input signal amplitude is not large enough to produce significant changes in the input amplifier transconductance. In the case of calorimeters for high energy experiments, this may not be the case as large dynamic range is usually required. An example of a solution for such an scenario is the ATLAS LAr calorimeter preamplifier, which creates the electronically cooled termination through a "super common base" input stage with an additional feedback loop [6]. An ASIC in IBM's 8WL 130nm SiGe process has been designed for the ATLAS calorimeter upgrade [27].

The LHCb Preshower chip relies also on a super common base stage [4], however no cooled termination is used in this case because the chip is located in the PM base. The input current is amplified and converted to differential signaling in order to be integrated through a fully differential amplifier with capacitive feedback. Since no dead time is allowed and high quality delay lines can not be easily

integrated, the solution adopted for the PS is to alternate every 25 ns between two integrators and to reset one integrator when the other one is active.

The proposed implementation of the analog channel is based on a combination of the two previous solutions [33]. In the first place a "regulated common base" input stage with additional current feedback creates the electronically cooled termination as shown in Fig. 3.9. Then two alternated switched signal paths are used to integrate and sample the input current with no dead time, as in the Preshower sub-detector. The full channel scheme is depicted in figure 3.1 and is composed

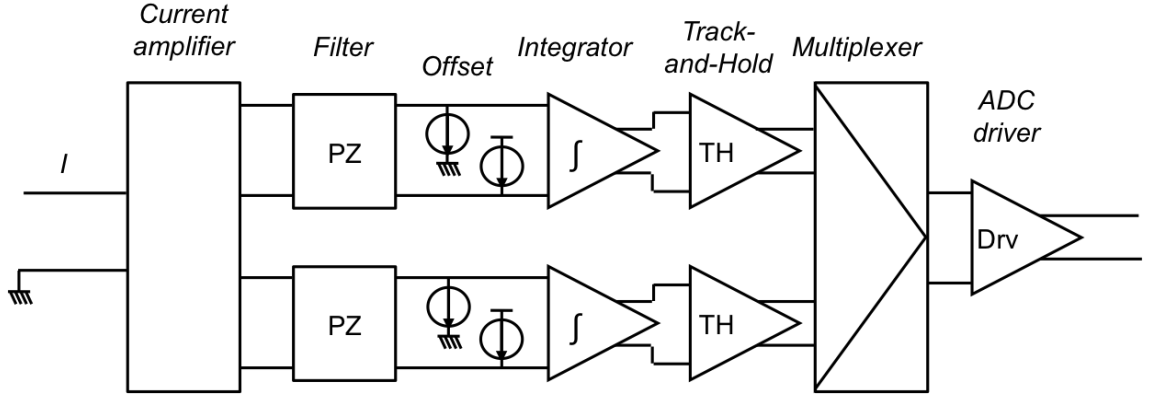


Figure 3.1 – One complete analog channel including the stages: current preamplifier, pole-zero filter, offset, switched integrator, Track-and-Hold, multiplexer and ADC driver.

by the blocks:

- The current preamplifier has an active cooled termination at the input for reduced noise.
- A pole-zero filter is used to help reducing the width of the signal to keep the spill over lower than 1% and to broaden the integral plateau.
- The switched integrator is based in a fully differential operational amplifier with 500 MHz GBW and better than 65 degree phase margin for moderate capacitive loads (below 15 pF).
- The Track-and-Hold is designed following the flip-around architecture for better linearity.
- An analog multiplexer selects the sub-channel to be digitized.
- An ADC buffer to drive the ADC capacitive input.

A simulation waveform plotted in Fig. 3.2 with the signal at the different stages (PM, current amplifier, pole-zero, integrator, Track-and-Hold and channel output) depicts the basics of the working of the analog channel. The signal is shaped at the pole-zero stage and then it is integrated during a half-clock cycle in one sub-channel. The effect of the current offset lowers the integrator value linearly with time. Afterwards, the Track-and-Hold maintains the voltage level of the integrator which will be selected by an analog multiplexer. In the presented simulation, the first sub-channel integrates most of the signal and, the second sub-channel integrates the tail of it. The tail is minimized by the pole zero and an optimum synchronization.

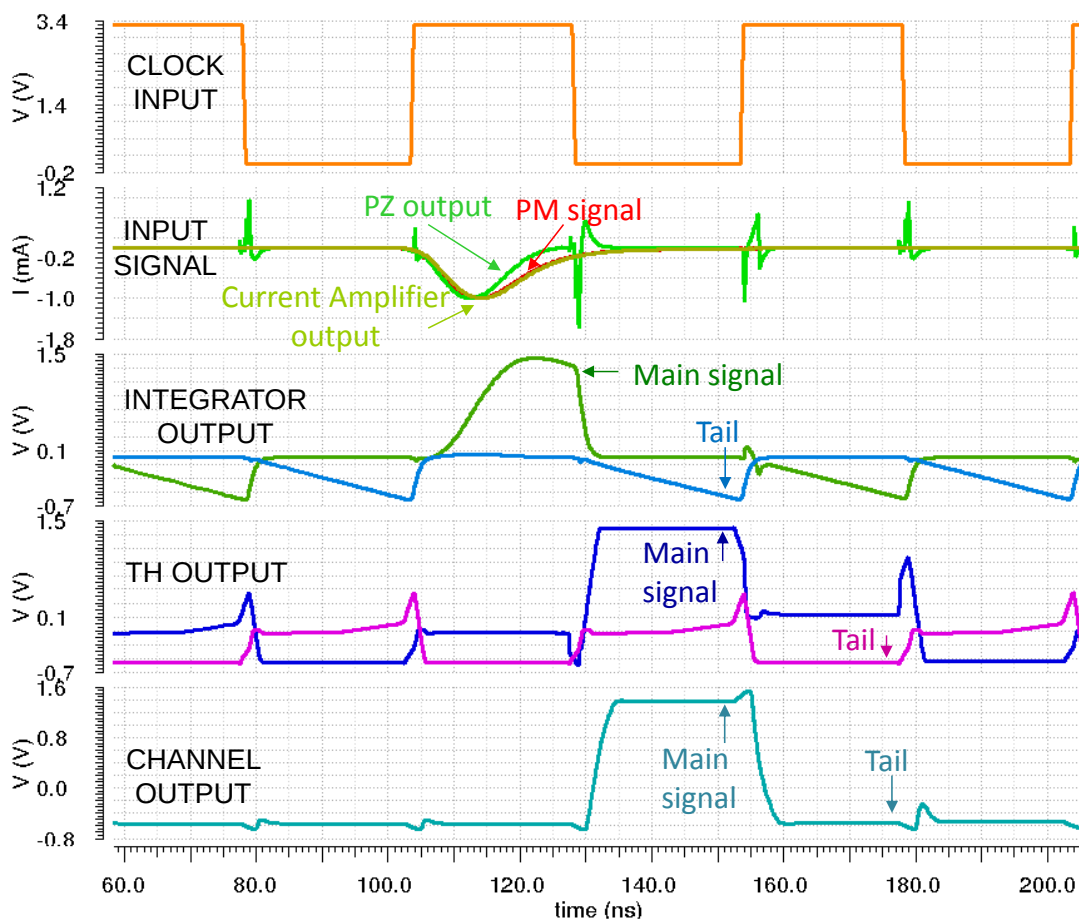


Figure 3.2 – Waveform simulation with the signal at different stage levels.

3.2 Noise and line termination

3.2.1 Preamplifier

An electronically cooled termination is required to meet noise requirements. Line termination can be achieved just by a terminating resistor or by an active circuit with controlled input impedance, which is usually referred as *electronically cooled termination*. The ATLAS LAr calorimeter preamplifier preamplifier creates the electronically cooled termination through a *super common base* input stage with an additional feedback loop [6]. In Fig. 3.3 the noise contributors for both schemes are shown. i.e. for a standard high input impedance voltage amplifier with terminating resistor R_T and for a cooled terminating preamplifier.

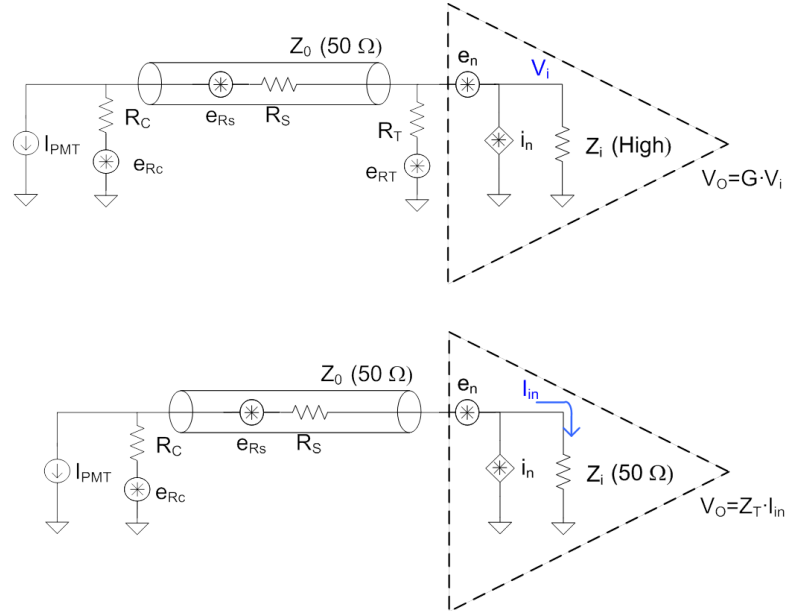


Figure 3.3 – Noise contributors for resistive termination (top) and electronically cooled termination (bottom).

Cable thermal noise PSD increases with frequency because of the skin effect. However it can be approximated by a lumped element R_S [6]. In this case, calculations and Spectre simulations indicate that $R_S \simeq 18 \Omega$. It is assumed that the impedance seen by the amplifier looking towards the detector can be approximated by the cable characteristic impedance Z_0 [34]. The noise contribution of the clipping line at the PMT base is modeled as a resistor $R_C = 25 \Omega$, so only 1/3 of the PMT pulse will be transmitted to FE.

With $R_T = Z_0$, the noise contributors referred to the PMT input current which is left after clipping, are, for the voltage amplifier with resistive termination

$$i_{nCLIP}^2 = \frac{e_n^2}{|Z_0|^2} + i_n^2 \left| \frac{1}{2} \right|^2 + \frac{4KT}{R_T} \left| \frac{1}{2} \right|^2 + \frac{4KT}{R_C} \left| \frac{R_C}{Z_0 + R_C} \right|^2 + \frac{4KTR_S}{|R_S + Z_0|^2} \quad (3.1)$$

And, with $Z_i = Z_0$, the contributors referred to PMT clipped current are, for the amplifier with cooled termination

$$i_{nCLIP}^2 = \frac{e_n^2}{|2Z_0|^2} + i_n^2 \left| \frac{1}{2} \right|^2 + \frac{4KT}{R_C} \left| \frac{R_C}{Z_0 + R_C} \right|^2 + \frac{4KTR_S}{|R_S + Z_0|^2} \quad (3.2)$$

Effect of parasitic capacitances will be negligible in the signal BW, therefore both series and parallel noise terms will be white noise contributors, which is not the typical case for capacitive detector readout with charge preamplifiers. Low frequency $1/f$ noise is negligible because of large bandwidth and correlated double sampling (CDS). CDS or pedestal subtraction is a technique which consists in subtract the output value of the previous sample to the present one to correct for pedestal and low frequency noise (mainly pick-up noise). Its effect on noise is detailed in section 3.2.3

Comparing equations 3.1 and 3.2, it is clear that cooled termination scheme has two advantages. The first one is obvious; thermal noise of R_T does not contribute. The second one, which could be even more important, is that amplifier input referred series noise contribution e_n is two times smaller.

In addition, a current amplifier input referred series noise contribution e_n

$$e_{noI} = Z_T i_{ni}|_{e_n} = e_n \frac{Z_T}{Z_i + Z_0} = e_n \frac{GZ_i}{Z_i + Z_0} \simeq e_n G \frac{1}{2} \quad (3.3)$$

is about factor two less than a voltage amplifier (Fig. 3.4):

$$e_{noV} = G e_{ni}|_{e_n} = e_n G \quad (3.4)$$

3.2.2 Gated integrator

For the noise study of the gated following stages is not straight forward; the gated systems are better defined in the time domain, but some of the noise sources are better described in the frequency domain. Therefore, as proposed in [35], the gated integrator transfer function will be computed in the time domain, then derived in the frequency domain to analyze its effect on the channel noise.

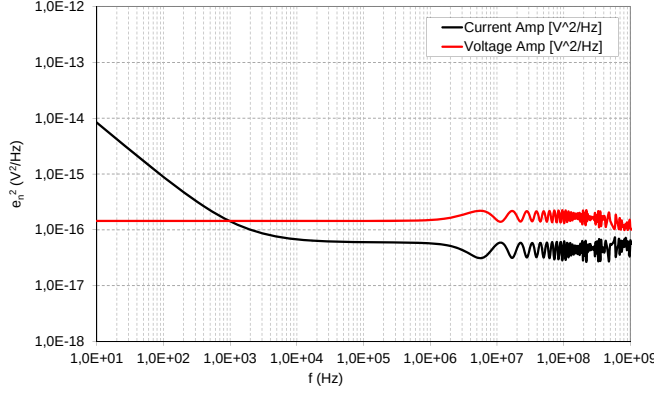


Figure 3.4 – Current and a voltage amplifier PSD for the same input referred series noise.

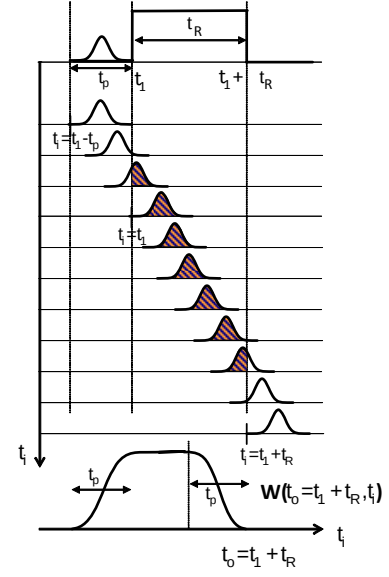


Figure 3.5 – Gated integrator noise weighting function with t_i , t_1 and t_R definitions.

A gated integrator is a case which is better described in the time domain and make use of the noise weighting function. The transfer function of the pre-filter, $p(t)$, is defined as the response at the gated integrator input (preamplifier output) to a unit noise impulse, $\delta(t)$. It depends on both the preamplifier transfer function ($G(s)$) and the source impedance. In the present circuit, with the clipping and, for the bandwidth of interest, the source impedance can be approximated to a resistor. For a resistive source impedance, the function $p(t)$ is the same (but with different coefficients) for series noise, parallel noise and the source resistance thermal noise; in all cases it is of the type $(1/\tau)e^{-t/\tau}$. We will continue the analysis taking a generic impulse response of the form:

$$p(t) = A \frac{1}{\tau} e^{-\frac{t}{\tau}} u(t) \quad (3.5)$$

where A is the DC gain for a given noise source and $u(t)$ is the step function.

From the definition of the noise weighting function it is possible to derive its value by parts. The noise weighting function $w(t_i, t_0)$ is defined as the output at the measuring time $t_0 = t_1 + T$, which results from a unit impulse $\delta(t_0 - t_i)$ delivered by an input noise generator at a time $t = t_i$; t_i is the time when the signal arrives, t_1 when the integration starts, and t_R is the integration duration (Fig. 3.5). The noise weighting function $\omega(t_0, t_i)$ at the end of integration is given

by the area of the shaded region of the signal induced at the pre-shaper output by a δ -pulse of the parallel noise generator. In fact the portion of this signal entering the gate is integrated and stored in the integrator therefore contributing to the noise at $t_0 = t_i + t_R$.

The integrator can be approximated by an ideal integrator with constant $1/\tau_i$. As the pre-filter function $p(t)$ has infinite duration, we consider only three cases:

1. If the current impulse is produced after the end of the integration, the contribution is null:

$$\omega(t_0, t_i) = 0 \quad t_i > t_1 + t_R \quad (3.6)$$

2. If the current impulse is produced before the start of the integration, part of the tail of the pulse is inside the integration window:

$$\begin{aligned} \omega(t_0 = t_1 + t_R, t_i) &= \frac{A}{\tau} \int_{t-t_i}^{t_1+t_R-t_i} p(x) dx \\ &\simeq \frac{A}{\tau} \left(e^{-\frac{t_1-t_i}{\tau}} - e^{-\frac{t_1+t_R-t_i}{\tau}} \right) \quad -\infty < t_i \leq t_1 \end{aligned} \quad (3.7)$$

3. If the current impulse arrives after the start of the integration, only the initial part of the pulse is integrated and contributes to the noise response at $t_0 = t_1 + t_R$:

$$\begin{aligned} \omega(t_0 = t_1 + t_R, t_i) &= \frac{A}{\tau_i} \int_0^{t_1+t_R-t_i} p(x) dx \\ &\simeq \frac{A}{\tau_i} \left(1 - e^{-\frac{t_1+t_R-t_i}{\tau}} \right) \quad t_1 < t_i \leq t_1 + t_R \end{aligned} \quad (3.8)$$

The white noise variance at the output can be computed:

$$\begin{aligned} \sigma_{white}^2(t_0 = t_1 + t_R) &= \frac{1}{2} e_{ni,white}^2 \int_{-\infty}^{+\infty} \omega^2(t_0, t_i) \\ &= \frac{1}{2} e_{ni,white}^2 \left(\frac{A}{\tau_i} \right)^2 \left[t_R - \tau \left(1 - e^{-\frac{t_R}{\tau}} \right) \right] \end{aligned} \quad (3.9)$$

If the pre-shaper time constant is much smaller than the integration time the expression can be simplified:

$$\sigma_{white}^2(t_0 = t_1 + t_R) \simeq \frac{1}{2} e_{ni,white}^2 \left(\frac{A}{\tau_i} \right)^2 t_R \quad (3.10)$$

This is true for our case, $\tau \simeq 4$ ns. If we compute the white noise variance at ambient temperature we obtain a noise sigma of 2.3 mV. With a gain 1,15 mV/fC

at the end of integration this is translated to an equivalent input noise charge of 2 fC as required.

In the case of the Flicker noise, a frequency domain analysis is needed. Depending on the authors it is not clear if this analysis is possible for time variant shapers because there are no valid representations of time variant circuits in frequency domain. Other authors claim that it is possible to do perform such calculation based on the Fourier transform of the weighting function $\omega(t_i, t_0)$. In [35] a simple method was proposed. The time variant transfer function is the Fourier transform of the time variant impulse response:

$$H(j\omega, t) = e^{-j\omega t} \int_{-\infty}^{+\infty} h(t_i, t) e^{-j2\pi f t_i} dt_i = e^{-j\omega t} F \{h(t_i, t)\} \quad (3.11)$$

The time variant impulse response $\delta(t - t_i)$ is defined as the output response at a time t of a given system to an impulse applied at $t = t_i$; this is the same definition of the noise weighting function of a time variant shaper. Therefore, the Fourier transform of the noise weighting function can be used as the time variant transfer function:

1. Compute $\omega(t_0 = t_1 + t_R, t_i)$ for a particular measurement time t_0 .
2. Then we perform the Fourier transformation:

$$W(j\omega, t_0) = e^{-j\omega t} F \{h(t_i, t)\} \quad (3.12)$$

3. Finally, compute the output noise with $G_{yy}(f, t_0) = |W(j\omega, t_0)|^2 G_{xx}(f)$:

$$\sigma^2(t_0) = \int_0^{+\infty} |W(j\omega, t_0)|^2 G_{xx}(f) df \quad (3.13)$$

For our system with pre-filter and gated integrator, the Fourier transform of the noise weighting function can be computed as the product of the Fourier transform of the gate function and the mirror of the pre-filter impulse response (times the integrator time constant $1/\tau_i$) $F \{p(t) \otimes g(t)\} = F \{p(t)\} F \{g(t)\}$. Then,

$$W(\omega, t_0 = t_R) = \frac{A}{\tau_i} \left(\frac{\frac{1}{\tau}}{\frac{1}{\tau} - j\omega} \right) \left(\frac{1 - e^{-j\omega t_R}}{j\omega} \right) e^{j\omega t_1} \quad (3.14)$$

It is important to remember that the PSD given above cannot be directly measured with an spectrum analyzer or computed by Fourier transform of a signal time record because it is only defined for a specific integration time $t_0 = t_R$.

The computation of the noise variance is done with the square of the modulus of the noise weighting function:

$$|W(\omega, t_0 = t_R)|^2 = \left(\frac{A}{\tau_i}\right)^2 \left(\frac{\frac{1}{\tau^2}}{\frac{1}{\tau^2} + \omega^2}\right) \left(\frac{2(1 - \cos(\omega t_R))}{\omega^2}\right) \quad (3.15)$$

First, the noise variance corresponding to the white noise component $e_{ni,white}$ of the input noise PSD, which is the same simplified expression that was derived using time domain analysis:

$$\begin{aligned} \sigma_{white}^2(t_0 = t_1 + t_R) &= \frac{1}{2} e_{ni,white}^2 \left(\frac{A}{\tau_i}\right)^2 \left(t_R - \tau \left(1 - e^{-\frac{t_R}{\tau}}\right)\right) \\ &\simeq \frac{1}{2} e_{ni,white}^2 \left(\frac{A}{\tau_i}\right)^2 t_R \end{aligned} \quad (3.16)$$

where the approximated result is valid for an integration time much greater than the preamplifier time constant: $t_R \gg \tau$.

The Flicker noise is relevant at low frequency ($\omega < 2\pi f_{Ceni} \ll 1/\tau$). As the preamplifier bandwidth $1/\tau$ is much higher than the Flicker noise corner frequency, the preamplifier has a flat response for the range of interest. If the Flicker component of the PSD of the total input equivalent noise is described as $e_{ni,Flicker}^2(f) \simeq \frac{C_F}{f}$, then the noise variance related to the Flicker noise is:

$$\begin{aligned} \sigma_{Flicker}^2(t_0) &= \frac{1}{2\pi} \int_0^{\frac{1}{\tau C_{eni}}} e_{ni,Flicker}^2(\omega) |W(\omega, t_0 = t_R)|^2 d\omega \\ &= \left(\frac{A}{2\pi}\right)^2 \int_0^{\frac{1}{\tau C_{eni}}} \frac{C_F}{\omega} \frac{4 \sin^2\left(\frac{\omega t_R}{2}\right)}{\omega^2} d\omega \end{aligned} \quad (3.17)$$

where $\tau_{Ceni} = 1/2\pi f_{Ceni}$. As in the region of interest $2\pi f_{Ceni} \ll 1/t_R$, then ωt_R . Therefore, $\sin\left(\frac{\omega t_R}{2}\right) \simeq \frac{\omega t_R}{2}$. So, for low frequencies, the PSD of the flicker noise at the output of the integrator is proportional to $1/\omega$. The approximation is valid for $f < 1$ MHz, i.e., for frequencies up to 100 times higher than the corner frequency f_{Ceni} . Then,

$$\sigma_{Flicker}^2(t_0) \simeq C_F \left(A \frac{t_R}{\tau_i}\right)^2 \ln\left(\frac{T_{OP}}{\tau C_{eni}}\right) \quad (3.18)$$

A PSD inverse to the frequency seems suggest “infinite” noise at DC. This is not the case because the “zero” frequency does not exist; any electronic circuit or equipment is turned on (and off) at some moment. Therefore, the minimum frequency is $1/T_{OP}$ where T_{OP} is the time the circuit is kept powered on. No matter T_{OP} is 1 day or 1 year, white noise dominates for integration times smaller than 1 us.

From these results, it can be concluded that the noise is proportional to the integration time for the flicker case ($\sigma_{flicker}$) and to the square root of the integration time for the white noise.

3.2.3 Dynamic pedestal subtraction effect on noise

The dynamic pedestal subtraction or Correlated Double Sampling (CDS), consists in subtracting the lowest of the two previous samples to the present sample. It is used to correct the baseline shift and to filter the low frequency noise (essentially pick-up noise) which has proven to be crucial in the LHCb experiment. On the other hand, the dynamic pedestal subtraction increases the high frequency noise in a factor $\sqrt{2}$.

The pedestal subtraction in the discrete domain can be described by

$$h_{CDS}[z] = \delta[z] - \delta[z] \quad (3.19)$$

Using the Z transform

$$H_{CDS}[z] = 1 - z^T \quad (3.20)$$

The CDS frequency response is obtained with $z = e^{j\omega}$

$$|H_{CDS}[j\omega]| = |1 - e^{j\omega T}| = 2\sin\left(\frac{\omega T}{2}\right) \quad (3.21)$$

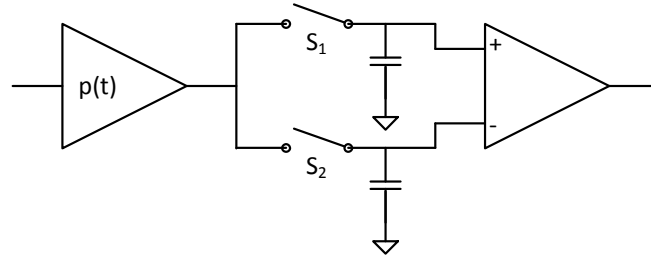


Figure 3.6 – Dynamic pedestal subtractor shaper.

Otherwise, using the method proposed in [35]. A correlated double sampler shaper is presented in Figure 3.6. The pre-filter $p(t)$ represents any circuit before CDS and is necessary to limit the noise bandwidth. It is assumed that S_1 samples the signal at $t = 0$ and S_2 at $t = T$. Three cases can be defined in function of the noise pulse arrival time t_i :

1. If the current impulse is produced after S_2 , with $t_i > T$, the contribution is zero:

$$\omega(t_0, t_i) = 0 \quad t_i > T \quad (3.22)$$

2. If the current impulse is produced before S_1 , then, with $t_i \leq 0$, the pulse is sampled by both switches:

$$\begin{aligned} \omega(t_0 = T, t_i) &= p(t - t_i)|_{t=0} - p(t - t_i)|_{t=T} \\ &= \frac{1}{\tau} \left(e^{\frac{t_i}{\tau}} - e^{\frac{t_i - T}{\tau}} \right) \quad -\infty < t_i \leq T \end{aligned} \quad (3.23)$$

3. If the current impulse arrives after S_1 , with $0 < t_i < T$, so it is only sampled by S_2 :

$$\omega(t_0 = T, t_i) = p(t - t_i)|_{t=T} = -\frac{1}{\tau} e^{\frac{t_i - T}{\tau}} \quad 0 < t_i \leq T \quad (3.24)$$

To compute $W(\omega, t_0)$ we can integrate for each t_i range:

$$\begin{aligned} W(\omega, t_0 = T) &= \int_{-\infty}^{\infty} \omega(t_i, t_0) \\ &= \frac{1}{\tau} \int_{-\infty}^0 \left(e^{\frac{t_i}{\tau}} - e^{\frac{t_i - T}{\tau}} \right) e^{-j\omega t_i} dt_i \\ &\quad - \frac{1}{\tau} \int_0^T e^{\frac{t_i - T}{\tau}} e^{-j\omega t_i} dt_i \end{aligned} \quad (3.25)$$

Resulting

$$W(\omega, t_0 = T) = \frac{\frac{1}{\tau}}{\frac{1}{\tau} - j\omega} [1 - e^{-j\omega T}] \quad (3.26)$$

Where its modulus is:

$$|W(\omega, t_0 = T)| = |2\sin(\pi f T)| \left| \frac{\frac{1}{\tau}}{\frac{1}{\tau^2} + \omega^2} \right| \quad (3.27)$$

which is in agreement with the previous result with the Z transform.

3.2.4 Total noise

Provided that the amplifier BW is much higher than the inverse of the integration time t_R , it can be shown [35] that the ENC of a amplifier with total input referred noise current power spectral density (PSD) i_{nCLIP} followed by a gated integrator shaper is, assuming i_{nCLIP} PSD is flat (white noise),

$$ENC_{A+I}^2 \simeq \frac{1}{2} i_{nCLIP}^2 t_R \quad (3.28)$$

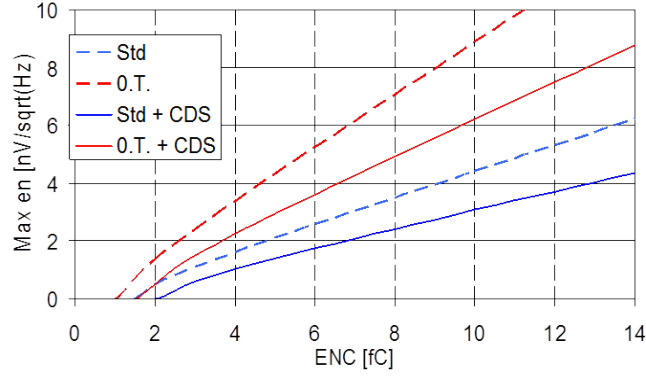


Figure 3.7 – Series noise requirement for different amplifier and signal processing configurations. Parallel noise contribution is neglected.

This expression is valid both for a delay line and a switched integrator. If CDS is performed after integration, and assuming that samples are uncorrelated,

$$ENC_{A+I+CDS}^2 \simeq i_{nCLIP}^2 t_R \quad (3.29)$$

The amplifier noise requirement (maximum allowed series input referred noise e_n) as function of the required ENC is depicted in Fig. 3.7 for both termination configurations: termination resistor and active input impedance termination (Please note that *std.* refers to a resistor termination and *0.T.*, to the active cooled input termination). Parallel noise contribution is neglected since source impedance (Z_0) is small. Considering the required ENC (4 fC), the noise requirement for a cable terminating amplifier is $2.25\text{nV}/\sqrt{\text{Hz}}$ whereas the one for a standard high input impedance voltage amplifier is $1\text{nV}/\sqrt{\text{Hz}}$. An active termination configuration will be pursued since it leaves room for further refinements such as pseudo differential input configuration.

The expected noise PSD of the analog channel is exposed in Fig. 3.8 and an integral of each noise is summarized in Table 3.1. The current preamplifier at the input presents a relatively low noise performance. Then, the cable adds some noise at high frequencies (due to the Skin effect, more on Appendix A). After that, the pole-zero shaping stage increases more notably the noise at high frequencies. Next stage is the switched integrator, which reduces the PSD approximately proportional to $1/f$ from about 10 MHz to higher frequencies. Consequently, the effect of the pole-zero stage is diminished to levels close to the channel without this stage. Finally, a correlated double sampling (CDS) or pedestal subtraction (detailed analysis in Section 3.2.3) will be used to remove the low frequency pickup noise at the detector along with the baseline. It consists in removing the lowest of the previous two samples to the present one, as the probability to have two

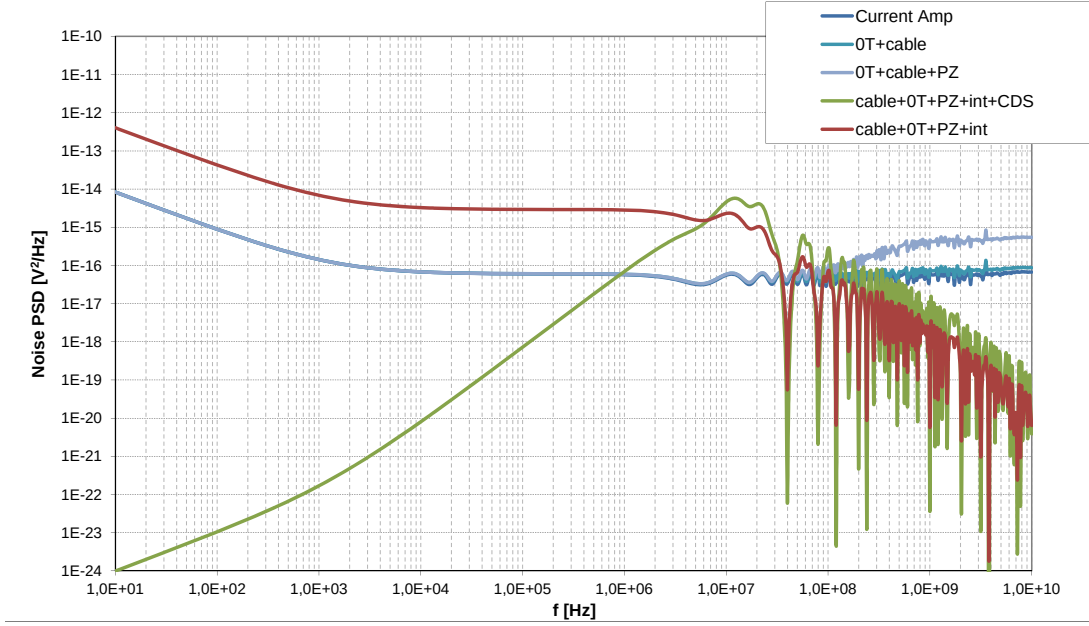


Figure 3.8 – Expected noise PSD calculation with all stages.

consecutive events at the detector in the same channel is considered to be negligible. The CDS reduces notably the low frequency noise, which is correlated for signal time constants greater than the CDS time (time between subtracting sample and integrated sample), but it increases the uncorrelated noise. If the noise is computed again taking into account the CDS, it results:

$$\sigma_{no,CDS}^2(t_0) \simeq e_{ni,white}^2 \left(\frac{A}{\tau_i} \right)^2 t_R \quad (3.30)$$

When compared to the previous result (Eq. 3.16), there is an increase of $\sqrt{2}$ in noise.

The results in Table 3.1 reflect the effects on noise in a more straight-forward way; the noise is integrated and shown in ADC counts. As commented above, a relative low noise is obtained from just the preamplifier with the active termination input. But it increases, if we take into account the cable noise effects in high frequency due to the skin effect. As the pole-zero acts as a high-pass filter, its repercussion is important until the switched integrator is accounted. Nevertheless, once the pedestal is subtracted, the noise is increased in about $\sqrt{2}$. The overall result is within the 1 ADC count specification.

Stages	Integrated noise (10 Hz to 1 G Hz) (μVrms)	Noise (ADC counts)
Voltage preamp	377	0.77
Current preamp	221	0.45
Current preamp + cable	882	1.81
Current preamp + cable + PZ	2170	4.44
Current preamp + cable + PZ + int	230	0.47
Current preamp + cable + PZ + int + CDS	337	0.69

Table 3.1 – Expected noise calculations of the analog channel stages.

3.3 Preamplifier input stage and input cooled termination

3.3.1 Preamplifier circuit design

As commented above, the Input amplifier is made of a "super common base" input stage with double feedback and it presents an electronically cooled termination, as in the ATLAS LAr calorimeter preamplifier [6]. However, this preamplifier is based on voltage feedback, with AC coupling requiring off chip components and additional pads. A novel DC coupled current mode scheme has been developed for this application. A simplified schematic of the differential half circuit of the input stage is shown in Fig. 3.9. Two current feedback loops are used to decrease and control the input impedance of a common base transistor (Q1) with emitter degeneration (R_E) to provide additional transconductance linearization. The inner loop decreases the open loop input impedance by a factor $K + 1$, where K is the aspect ratio of MP1 and MP2 current mirror [5]. Low frequency open loop impedance is $Z_{i_{CL}}^0 = \frac{1}{g_{m1}} + R_E$. Conversely, the outer loop increases the output impedance by a factor K_m , where K is the aspect ratio of MP1 and MP3 current mirror and m is aspect ratio of MN1 and MN2 current mirror. Thus, low frequency closed loop input impedance $Z_{i_{CL}}^0$ is,

$$Z_{i_{CL}}^0 \simeq \frac{1}{1+K} \frac{1}{g_{m1}} + \frac{K}{1+K} m R_f \quad (3.31)$$

If $K \gg 1$, $Z_{i_{CL}} \simeq m R_f$ and, hence, the input impedance can be controlled

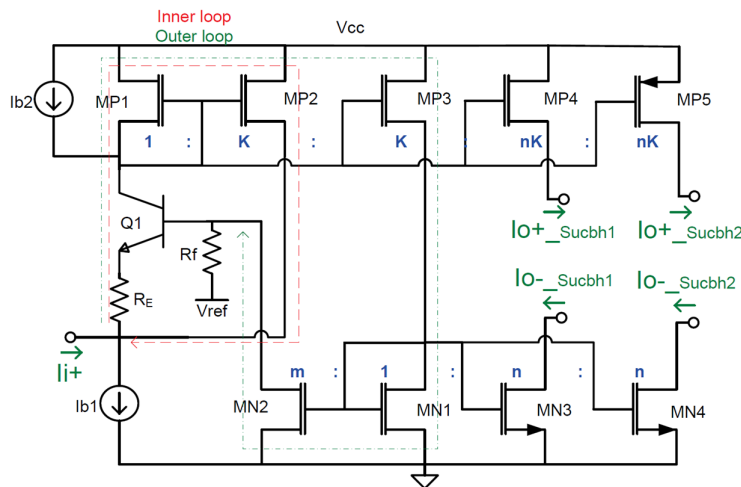


Figure 3.9 – Super common base amplifier with current feedback.

through m and R_f .

In order to achieve the required noise, linearity and bandwidth performances the current mirrors are cascode current mirrors with internal feedback, which is depicted in Fig. 3.10 left. Input impedance is very low, especially at LF.

The feedback loop must be compensated by dominant pole compensation C_C , and that imposes a trade-off with the BW. The non-dominant pole is given by the input capacitance C_{IN} , thus high BW can be achieved for moderate values of C_{IN} , as can be noticed in Fig. 3.10 right.

The current mode implementation has several advantages with respect to previous designs [27]:

- Low voltage operation. On the one hand, $1 V_{be}$ is saved using a current mode inner loop instead of a voltage one. On the other hand, a voltage amplifier requires a higher voltage excursion in a high impedance node.
- Low power. Because of low voltage operation and because of current mode feedback, the consumption of the preamplifier is about 10 mW, for a BW well above 100 MHz and 12 bit dynamic range.
- The feedback is DC coupled, so, external components or additional pads are not required.
- All nodes are low impedance nodes, which is very convenient to achieve high BW. It also makes the circuit less prone to pick up noise and crosstalk.

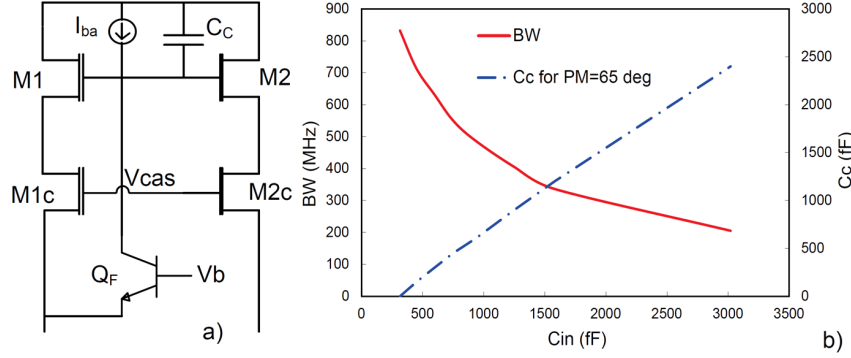


Figure 3.10 – Low voltage cascode current mirror with common base feedback (left) and BW and C_C as function of input capacitance (C_{IN}).

- ESD robustness is improved since no MOS transistor gate or bipolar base is connected to the input pad (series resistors are not allowed for noise reasons).

In order to be able to compensate the process variations that could lead to different input impedances, the current feedback is equipped with a 5 bits programmable gain.

3.3.2 Small signal analysis of the input stage

The preamplifier has two main feedback loops, besides some local ones (in current mirrors for instance, Fig. 3.10 left). In some special cases, however, stability of a multiple-loop circuit can be determined from a single return ratio [36]. The first special case applies to circuits with any number of local feedback loops inside one global feedback loop. If each embedded local feedback loop is stable by itself, then stability can be checked by breaking the global feedback loop while keeping all the local feedback loops intact and calculating the gain and/or phase margins. The other special case of multi-loop feedback applies to circuits in which there exists a single break point that simultaneously breaks all feedback loops.

Definitely, the design of a current mode preamplifier presented in section 3. A fulfils both conditions, because both inner and outer global feedback loops can be broken at the collector of Q1. Then, a single return ratio $T(s)$ can be computed by simple circuit analysis, yielding

$$T(s) \simeq 2K\alpha \frac{(sz^{-1} + 1)}{(sp_d^{-1} + 1)(sp_{nd1}^{-1} + 1)(sp_{nd2}^{-1} + 1)} \quad (3.32)$$

where $\alpha = (R_{in}) / (R_{in} + R_E)$, dominant pole p_d is the pole associated to PMOS current mirrors in Fig. 3.9, first non-dominant pole p_{nd} is the pole associated

to NMOS current mirrors, second non-dominant pole is $p_{nd} = (1) / (\alpha Z_{i_{OL}}^0 C_{in})$ and the zero is $z = (2p_{nd1}) / (mR_f C_{in} p_{nd1} + 1)$. Input capacitance C_{in} accounts mainly for input pad capacitance and stray capacitances. Assuming that the cable impedance looking from the emitter is Z_0 , $R_{in} = r_{OIbias1} \parallel Z_0 \simeq Z_0$, where $r_{OIbias1}$ is the output impedance of the current source (Fig. 3.9). The simulated return ratio $T(f)$ as function of is shown in Fig. 3.11.

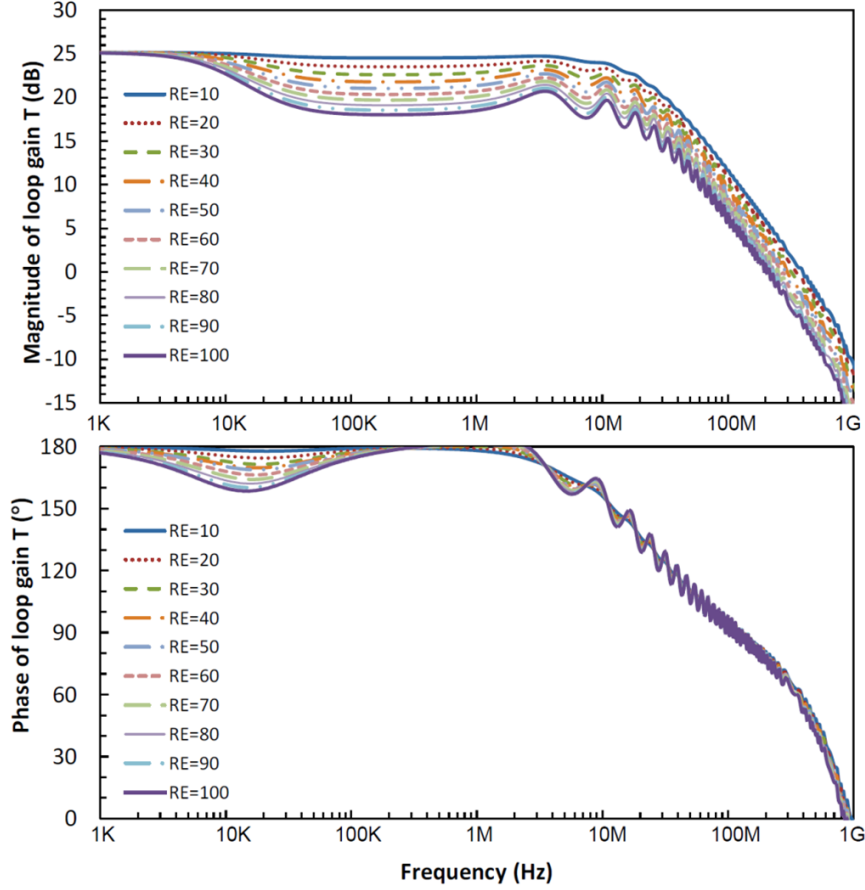


Figure 3.11 – $T(f)$ as function of R_E : magnitude (top) and phase (bottom).

Cable is modeled as a Spectre “mtline” element. The characteristics used in the cell were obtained from a detector cable data sheet and are listed in Table 3.2.

Low frequency (LF) loop gain is $T(0) \simeq 2K\alpha$, so dependent on R_E . The effect of input signal AC coupling is visible at low frequency ($< 1KHz$). Dominant pole p_d is around $30MHz$, as expected. There are two basic methods to compensate $T(s)$:

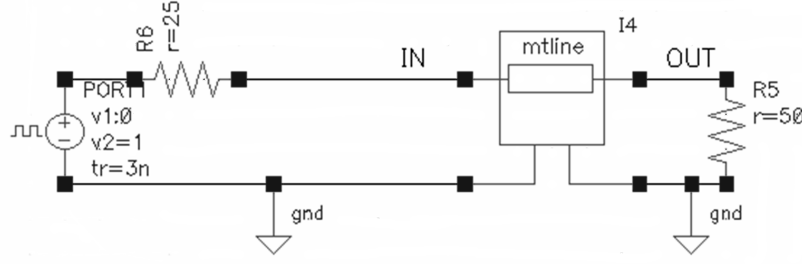


Figure 3.12 – Cadence Spectre simulations of the cable using the cell *mtline*.

Table 3.2 – Parameters to be configured in the *mtline* cell.

Parameter	Name	Value
Cable physical length	l	12m
Normalized velocity	v	0.659 c
Corner frequency	f_{corner}	18.446kHz
DC series resistance per unit length	R_{DC}	0.031Ohm/m
Conductor loss measurement frequency	f_C	200MHz
Conductor series resistance per unit length at f_C	R_S	2.411 Ohm/m

- Perform dominant pole compensation, decreasing α . This can be done increasing C_C of PMOS mirror (Fig. 3.10). However, signal bandwidth is $p_d (K + 1)$ [37], thus, there is a bandwidth-versus-stability compromise.
- Decrease the LF loop gain $T(0)$ by increasing R_E (α is decreased) for $f > 1KHz$ (AC coupling). As discussed in next section, there is a trade-off with noise performance in this case.

Phase and gain margin as function of C_C and R_E are shown in Fig. 3.13. A reasonable compromise to fulfill BW and noise requirements is achieved while having a PM $> 60^\circ$, with $C_C = 300fF$ and $R_E = 36\Omega$.

Closed loop input impedance can be computed using Blackman's expression [38], after lengthy analysis,

$$Z_{i_{CL}}(s) = Z_{i_{OL}}(s) \frac{1 + T_{SC}(s)}{1 + T_{OC}(s)} \simeq Z_{i_{CL}}^0 \frac{(sz_z^{-1} + 1)}{(sp_{z1}^{-1} + 1)(sp_{z2}^{-1} + 1)} \quad (3.33)$$

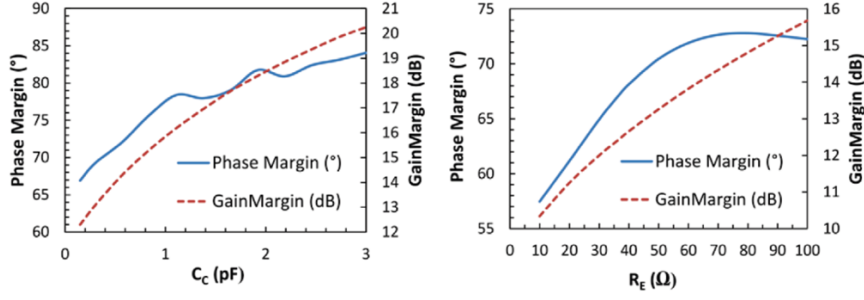


Figure 3.13 – Phase margin and gain margin as function of C_C (left) and R_E (right).

where $T_{SC}(s)$ and $T_{OC}(s)$ are the return ratio functions with shorted and open circuited input, respectively. Poles are $p_{z1} = p_d K \| p_{nd1}$ and $p_{z2} = (p_d K + p_{nd1}) / (Z_{i_{OL}}^0 C_{in})$ and the zero is $z_z = p_d (1 + (K M R_R / Z_{i_{OL}}^0))$.

Fig. 3.14 shows simulated $Z_{i_{CL}}(f)$ for different values of R_E . There is no induc-

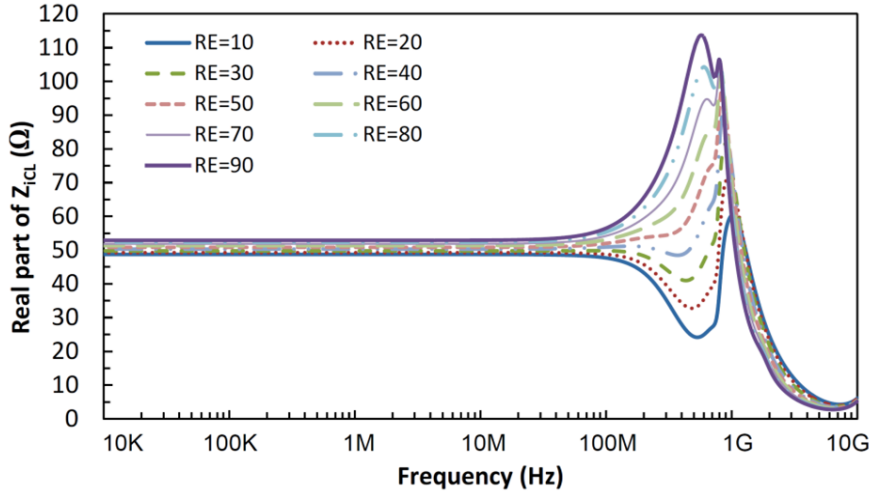


Figure 3.14 – Real part of closed loop input impedance Z_{ICL} as function of R_E .

tive behavior in the signal BW, there is no effect of the dominant pole of $T(s)$. As R_E is increased, z_z moves to low frequency ($Z_{i_{OL}}^0$ increases), even canceling the effect of the lowest frequency pole of Eq. 6.2, which is p_{z1} .

Knowledge of closed loop input impedance offers an alternative method to assure the stability of the current input amplifier. It has been shown [39] that a sufficient condition for the stability of cable couple amplifier is $Real[Z_{i_{CL}}(f)] >$

0, for signal BW. Therefore, increasing R_E compensates the effect p_{z1} , so that $\text{Real}[Z_{i_{CL}}(f)] \geq 0$ for full signal BW.

Stability has been extensively checked by simulation using both methods:

- For different cable lengths, from 2 m to 24 m.
- For different stray capacitances (up to 30 pF).
- As function of the input peak current. Operating point is computed at the far extreme of the transient signal swing.
- Taking into account the effects of bonding wire and package inductances up to 3 nH (nominal value < 1 nH).

In any case, stability is assured by both methods, with a minimum phase margin of 60° .

The circuit is robust against temperature variations thanks to the differential configuration, this is verified by simulation. The effect of process variations and mismatch has been studied through extensive Monte Carlo simulations. The most sensitive parameter is the input impedance, since it depends on the absolute value of a poly-silicon resistor. The last version of the chip design adds the possibility to tune the outer loop gain in order to compensate for that.

3.3.3 Noise analysis

The output noise of the ASIC is mainly determined by the noise contributors of the input current preamplifier. Input referred series and parallel noise generators have been computed for the half circuit of the preamplifier (Fig. 3.9). Since source impedance is rather low (50Ω), series noise will dominate.

For series noise generator we have,

$$\begin{aligned}
 e_n^2 \simeq & 4KT [R_E + r_{bQ1} + R_f] + 2qI_{CQ1} \left(\frac{1}{g_{mQ1}} + R_E \right) \\
 & + 4KT \frac{2}{3} (Z_{i_{CL}}^0 C)^2 g_{mMP5} \left[\frac{2}{K} \left(\frac{Z_{i_{OL}}^0}{Z_{i_{CL}}^0 C} \right)^2 + \frac{3}{4} \right] \\
 & + 4KT \frac{2}{3} (Z_{i_{CL}}^0 C)^2 g_{mMN4} \left[\frac{2}{m} + \frac{1}{4} \right]
 \end{aligned} \tag{3.34}$$

where $C = K + 1/K$. First and second terms are the dominating ones and correspond to the input common transistor Q_1 base resistance thermal noise, to the collector current shot noise, and to R_E and R_F thermal noise. Conversely to classical cooled impedance preamplifier [34], these contributions are not divided by

the inner loop gain. Third and fourth terms correspond to the thermal noise of the transistors of PMOS and NMOS current mirrors, respectively.

As discussed in previous section, in order to achieve high BW and stability, R_E has to be relatively large. Thus, it will dominate series noise, as can be noticed in Fig. 3.15.

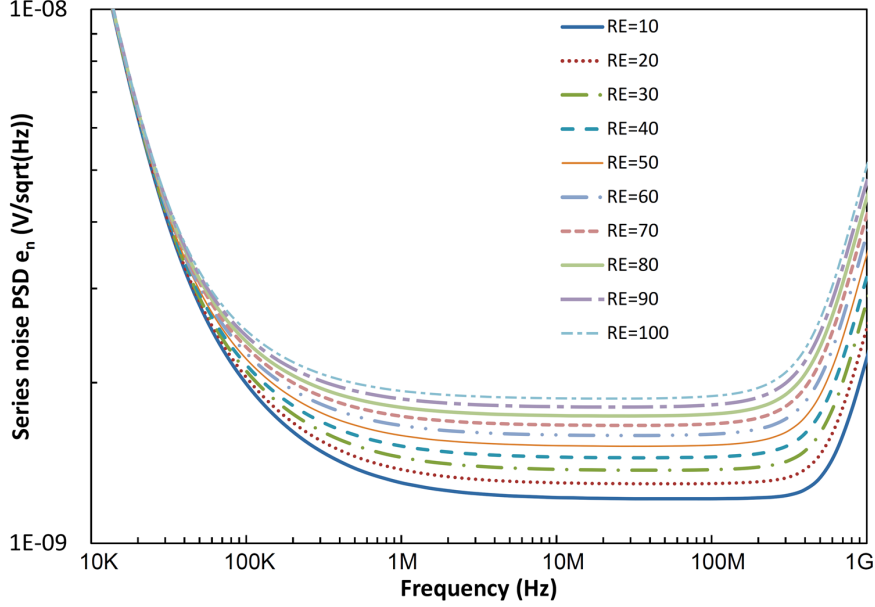


Figure 3.15 – Simulation series noise PSD as function of R_E .

For stability considerations, the largest R_E possible has been used so that series noise for half circuit is $1.4nV/\sqrt{Hz}$ and $2nV/\sqrt{Hz}$ for the differential configuration, yielding a final ENC of 3.6 fC (with CDS) and an output noise of 0.9 LSB.

Main contributors to the parallel noise are

$$\begin{aligned}
 i_n^2 \simeq & 4KT \frac{2}{3} g_{mMN1b1} \\
 & + 4KT \frac{2}{3} g_{mMP5} \left[\frac{2}{K} + 2 + 2 \left(\frac{mR_f}{r_{OIbias1}} \right)^2 + \frac{1}{4} \right] \\
 & + 4KT \frac{2}{3} g_{mMN4} \left[\frac{1}{8} + m \left(\frac{R_f}{r_{OIbias1}} \right)^2 + \frac{1}{4} \right] \\
 & + 4KT \left[\frac{R_E + r_{bQ1} + R_f}{r_{OIbias1}^2} \right]
 \end{aligned} \tag{3.35}$$

The contribution of base resistance of Q_1 , of R_E and of R_f is negligible since

$r_{OIbias1}$ is much larger than those resistors. Parallel noise is very dependent on bias current, as remaining terms in expression 3.35 depend on g_m . This dependence can be noticed in simulation results of Fig. 3.16. Parallel noise contribution to the

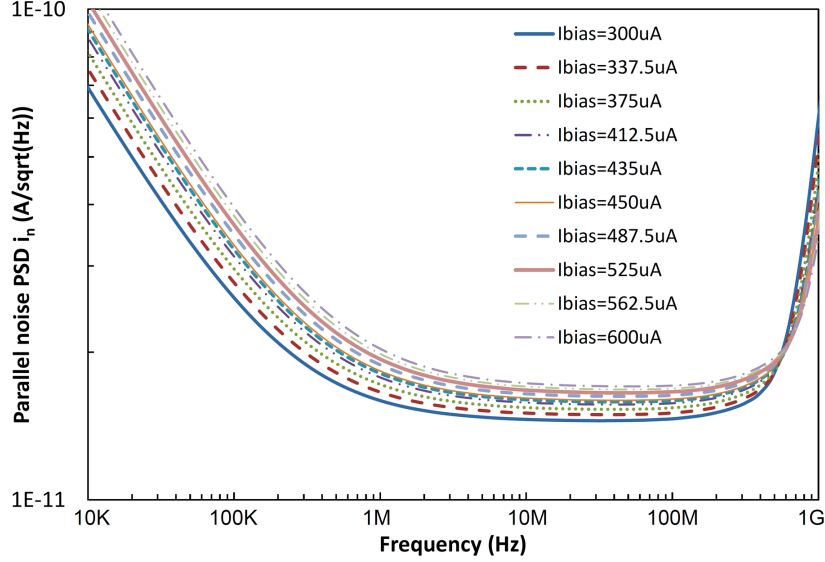


Figure 3.16 – Simulation of parallel noise PSD as function of I_{bias} .

total input referred noise current i_{nCLIP} is, by expression 3.1, 7 to 8 $pA/\sqrt{Hz}$; whereas series noise contribution is 14 to 18 $pA/\sqrt{Hz}$. Since both terms add in quadrature, series noise contribution will dominate, as said above.

3.3.4 Preamplifier layout

The use of adequate layout techniques [40] is necessary to reduce the mismatch effects. The simulation and estimation of device mismatch effects accounts for local variations and mismatched devices can degrade the input common-mode to output differential-mode rejection, power supply rejection and offset, especially in fully differential circuits like the analog channel to which the current preamplifier belongs.

The final current preamplifier layout is represented in Figure 3.17:

- All the current mirrors are distributed to optimize matching in PMOS and NMOS groups.
- Resistors R_E and R_f are the sum of parallel resistors interleaved with dummy resistors at the sides.

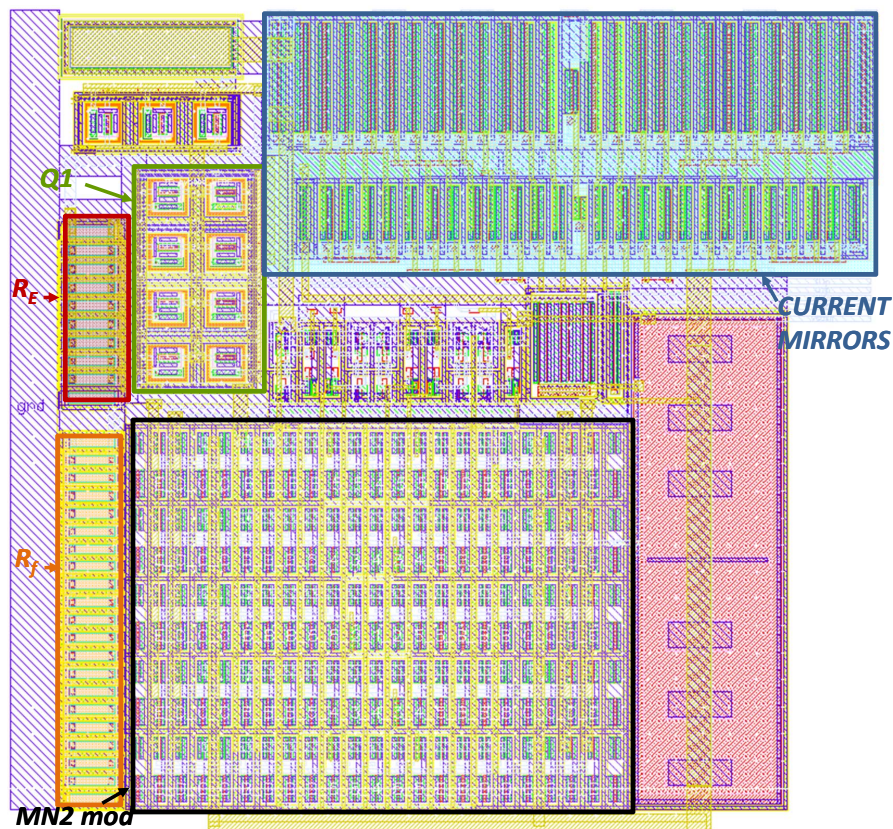


Figure 3.17 – Current preamplifier layout.

- Transistors MN2 and MP2 were divided in parts for adjustable Z_{in} via a programmable register. The minimum current step corresponds to the size of one transistor. As each bit increase corresponds to a 2^n step, the current is obtained by adding parallel transistors and a switch. In the end, there is a 2D net of distributed transistors in the best matching layout disposition.

3.4 Fully differential operational amplifier

Before presenting the next channel stages it is worth to review in detail a common building block used in the pole zero filter, the integrator and the Track-and-Hold (Fig. 3.1): a fully differential operational amplifier (FDOA). In order to use the same FDOA on the three stages it has to meet the specifications listed in the table 3.3. Both high accuracy and high speed is necessary for the amplifier. The high accuracy is obtained with a large DC open loop gain. Together with a high

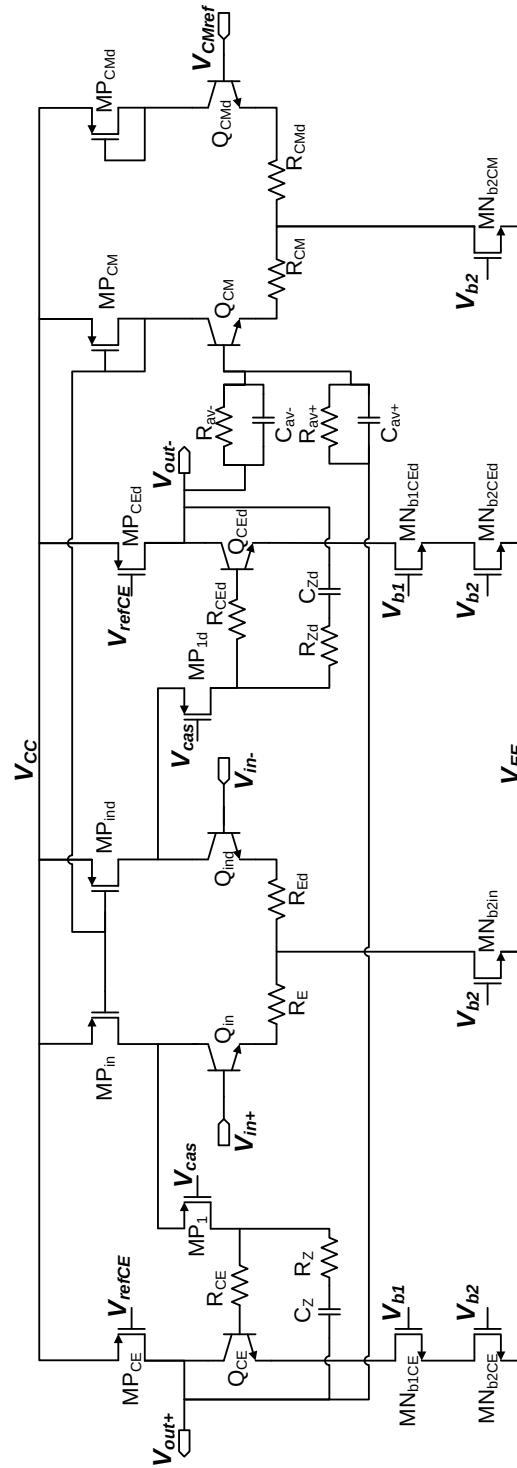


Figure 3.18 – Schematic of the OTA

speed implies that a high gain bandwidth (GBW) and slew rate (SR) are required. Such a performance translates to a high power consumption of the amplifier.

Table 3.3 – Summary of the requirements for fully differential operational amplifier.

Requirements	
Low frequency gain	$> 70\text{dB}$
GBW	$> 500\text{MHz}$
PM	$> 65^\circ$
SR	$> 0.5\text{V/ns}$
V_{CM}	$\sim 1.5\text{V}$

The FDOA (Fig. 3.18) is made of two stages and a common mode feedback (CMFB) circuit. First, there is bipolar pair input ($Q_{\text{in(d)}}$) with emitter degeneration ($R_{\text{E(d)}}$) in a folded cascode configuration ($\text{MP}_{1(\text{d})}$). Emitter degeneration resistors improve the input impedance, slew rate and the matching. Fast and accurate continuous time common mode feedback is provided by an error amplifier.

The output stage is a Miller stage with pole compensation ($C_{\text{Z(d)}}$ and $R_{\text{Z(d)}}$). Using a bipolar transistor ($Q_{\text{CE(d)}}$) instead of of a PMOS, a smaller compensation is required, increasing the GBW. It also reduces the resistance of the node at the first stage output, which would lower its gain, so a resistor is added ($R_{\text{CE(d)}}$).

A cascode current source ($\text{MN}_{\text{b1CE(d)}}$, $\text{MN}_{\text{b2CE(d)}}$, MN_{b2in} and MN_{b2CM}) is used to obtain a high CMRR. The current source is biased through an improved high-swing cascode circuit which allows to have high output range (from $2V_{\text{SAT}}$ to V_{CC}) and to compensate the Early effect, thus improving the current matching. The biasing of the FDOA circuit is depicted in Fig. 3.19. The gate voltages (V_{b1} and V_{b2}) for the cascode transistors are generated from an input reference current (I_{bCas}). The gate voltage (V_{refCE}) is obtained from a reference current (I_{bCE}).

Post-layout simulations are shown in Fig. 3.20 and 3.21. As the FDOA will be used for different applications, the simulations were made with different capacitance load values. Specifications are met except for the phase margin for load capacitances higher than 4 pF.

3.4.1 FDOA layout

The FDOA layout is represented in Figure 3.22.

- On the top, a bus for the voltage source and ground allows for later isolation of the switches and any clock generation circuits in a central region between the two sub-channels.

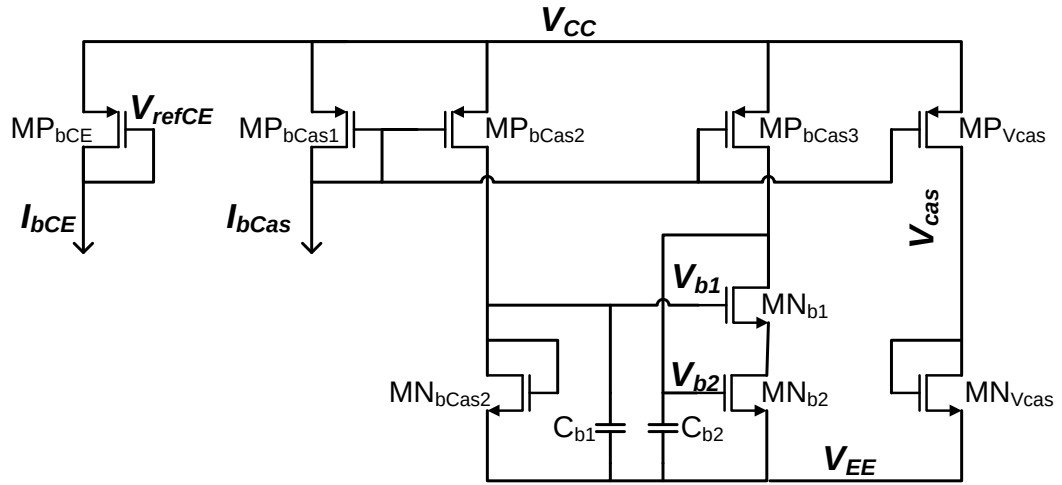


Figure 3.19 – Schematic of the bias circuit for the FDOA.

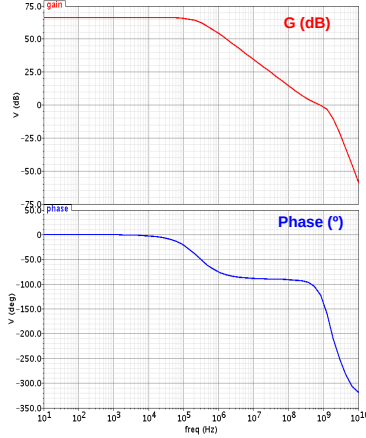


Figure 3.20 – FDOA gain and phase post-layout simulations.

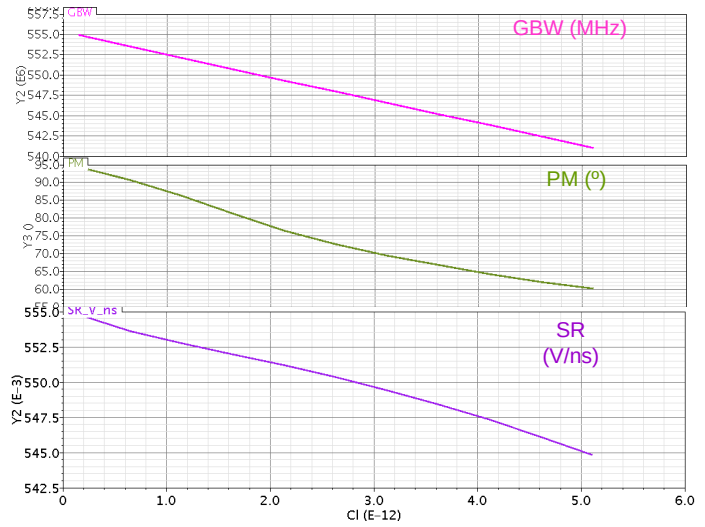


Figure 3.21 – FDOA gain bandwidth, phase margin and slew rate post-layout simulations for different load capacitor values.

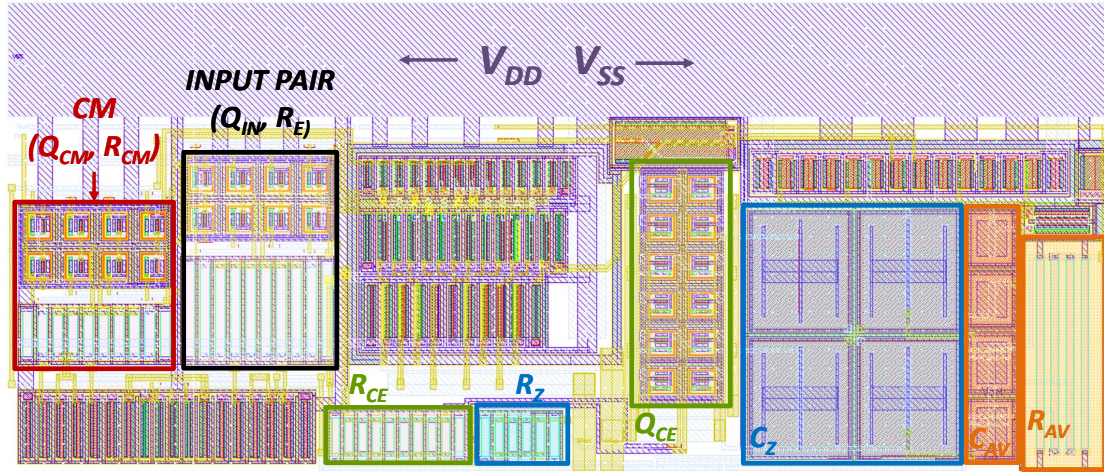


Figure 3.22 – FDOA layout.

- The input pair (left) made with 4 basic NPN transistors each distributed in a two-row common centroid. Under them the degeneration resistors are also split in four, mixed in a common centroid with dummies on the sides. The common mode feedback NPN transistors and its resistors are placed in a similar disposition.
- The common emitter transistors can be found in the central region of the layout distributed in a two-row common centroid.
- The pole compensation resistors R_Z and capacitors C_Z are made with two parts in parallel each. The resistor is interleaved in a common centroid with dummies at the sides, while the capacitors common centroid is distributed in a 2D disposition.

3.5 Pole zero filter

There are two specifications that are affected by the shape of the input pulse signal. First, the integrator output should be stable at the 1% level for $\pm 2\text{ns}$ arrival time fluctuations with respect the integration clock (usually referred to as plateau) so the energy from particles with different time of arrival to the detector is measured correctly. Second, the integrated signal on previous and next clock cycles should be less than 1% of the main signal. The part of the signal included in other clock cycles is known as spill over.

A test beam in 2012 (chapter 7) showed that the pulse signal presented a longer tail than an old measurement [41] used as the reference due to the long cable effect.

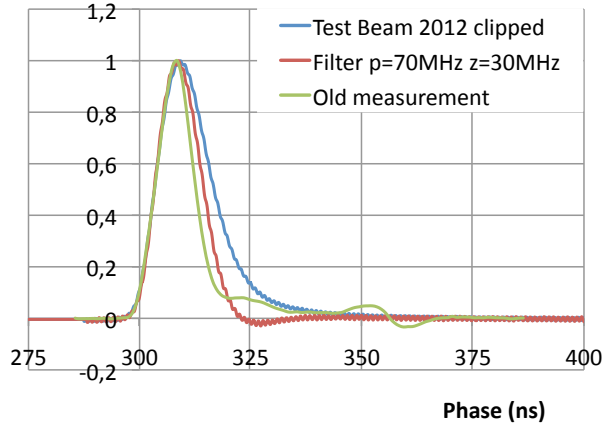


Figure 3.23 – Input signals used for simulation include an old measurement and another one from the 2012 Test Beam. An ideal pole zero filter reduces the effect of the long tail.

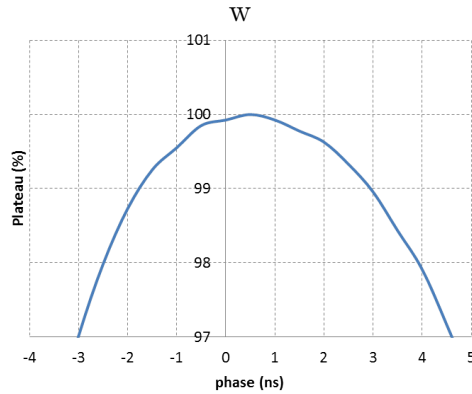


Figure 3.25 – Simulation output of the analog channel with a tuned PZ filter allows a plateau with a deviation lower than 1% for phases ranging more than 4 ns.

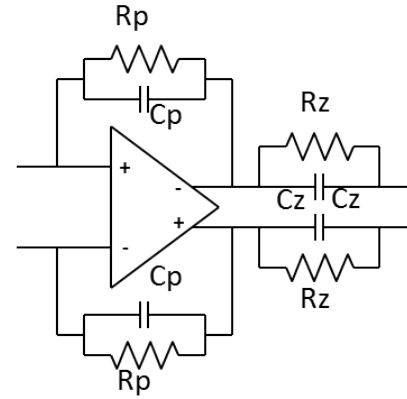


Figure 3.24 – Simplified schematic of the pole-zero filter.

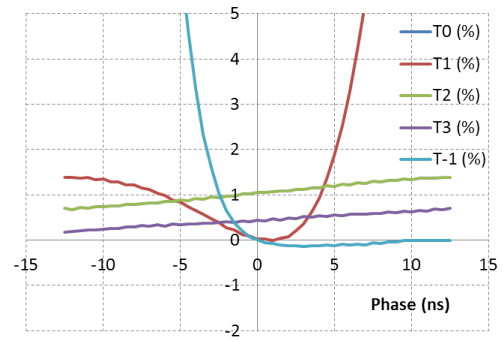


Figure 3.26 – Simulated output of the analog channel with a tuned PZ results in spill over values up to 1%.

As a consequence the plateau and the spill over requirements were not fulfilled. Therefore, a filter stage was designed to cope with the cable effects. A single pole and a single zero can help reducing the long exponential decay of the pulse. Figure 3.23 plots the old measurement, the one obtained in the 2012 test beam, and the simulation of the pole zero filter.

The scheme of the block is shown in figure 3.24. The filter is obtained with a single pole and a single zero with a differential amplifier and in current mode, as it is placed before the integrator. The differential current transference function is:

$$H(s) = \frac{R_p R_z C_z s + 1}{R_z R_p C_p s + 1} \quad (3.36)$$

The pole and zero are obtained with resistors in parallel to variable capacitors (6 bits for the pole and 5 bits for the zero) that lets the user adjust for the different signals in figure 3.23 and compensate for fabrication process. It is even possible to compensate the signal without the clipping at the PMT bases, but with a worse plateau and fixed spill over that could be compensated easily in the digital domain.

Simulations showed that the inclusion of the filter stage caused an estimated noise impact of a 10% increase.

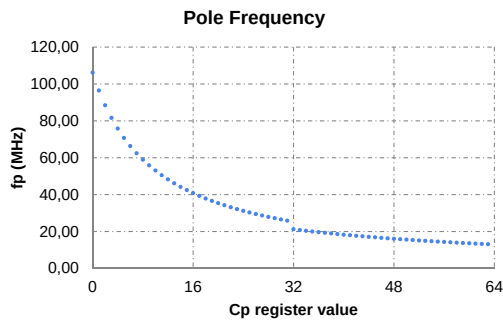


Figure 3.27 – PZ filter pole frequency for each register value.

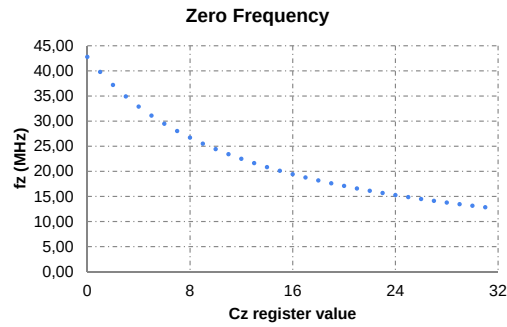


Figure 3.28 – PZ filter zero frequency for each register value.

Multiple simulations were performed for the different pulse signals at hand to find values of the pole and zero capacitors which would reduce the spill over values below 1% and expand the plateau to 4 ns (Fig. 3.25 and 3.26). Only in the case of a non-clipped signal, for which the pulse is wider and the long tail is more pronounced, it was not possible to meet the spill over specifications better than the 2% level. The optimal pole and zero frequencies are summarized in Table 3.4.

Table 3.4 – Optimal frequencies for the different detector signal pulses.

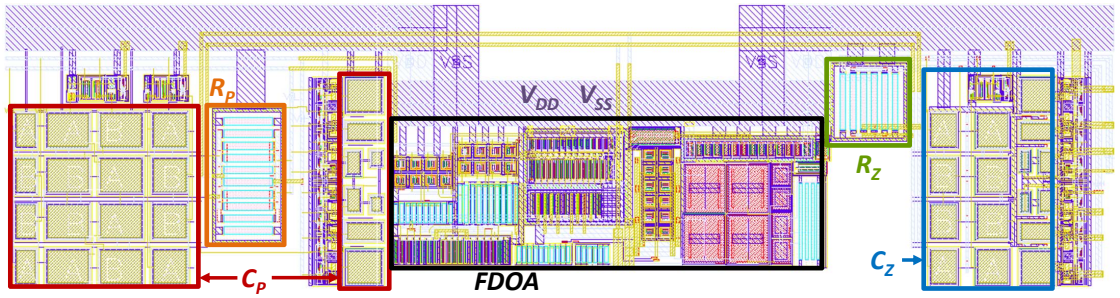
Signal	f_{pole} (MHz)	f_{zero} (MHz)
2012 clipped	53.1	21.2
2012 not clipped	55.6	12.9
Old measurement	14.5	11.3

3.5.1 Register values

The pole-zero filter can be adjusted through the pole and zero capacitors. The register values and their frequency correspondence is pictured in figures 3.27 and 3.28. The values selected to cover the different pole-zero optimum values for the the different waveforms known (Fig. 3.23) and to cope with the 20% and 10% possible deviation on the capacity and resistor values due to the technology process variations.

3.5.2 Pole zero filter layout

The final pole zero filter layout (Fig. 3.29) is doubled on each channel. A Voltage source bus with the source V_{DD} and ground is placed in the inner part of the channel, allowing a better isolation between sub-channels. The fully differential operational amplifier is placed at the center. Following the signal path, the pole capacitor and resistor are at the input, on the left, while the zero capacitor and resistor are at the output, on the right. The capacitors are divided in groups that correspond to the different sizes for the programmable steps. When the sizes are large enough, they are split and placed following a common centroid to maximize the matching. In the case of the resistors, they are the sum of parallel pieces and distributed in a common centroid with dummies at the sides.

**Figure 3.29** – Pole zero filter layout.

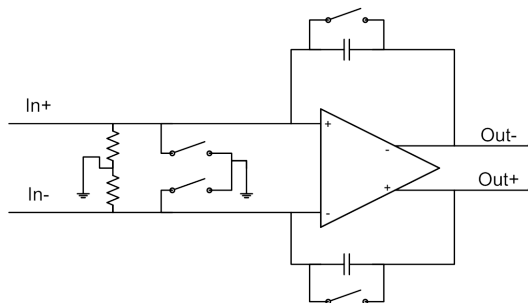


Figure 3.30 – Simplified scheme of the switched integrator.

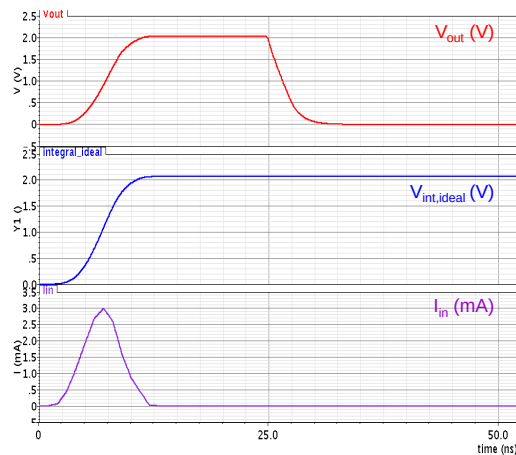


Figure 3.31 – Simulation of the switched integrator for a short pulse input.

3.6 Switched integrator

Integration is performed by the fully differential operational amplifier (FDOA) presented in section 3.4 with capacitive feedback (Fig. 3.30). As it has already commented, the use of two sub-channels with switched integrators permits the the measurement of consecutive detector pulses. Since no dead time is allowed, each sub-channel carries out the integration while the other is in reset every 25 ns. CMOS switches are used with a 50 ns cycle clock to carry out the integration. Feedback switches are on during the integration cycle. When the integration finishes, the reset cycle starts: two switches connect the inputs to ground and the feedback ones are off. In order to obtain a fast reset and avoid residual amplification, low impedance switches are used. The integrator capacitors are discharged in less than 10 ns. The variations in gain are compensated with an adjustable capacitor at the integrator using 5 bits.

$$\frac{V_{od}}{I_{id}} = \frac{R}{Cs} \quad (3.37)$$

The simulation of the integration of a short pulse is displayed in Fig. 3.31. Ideally, the integrator output would be proportional to the input pulse charge and remain in that state. The switched version integrates during the first 25 ns (one detector bunch crossing) and resets to zero in the next 25 ns.

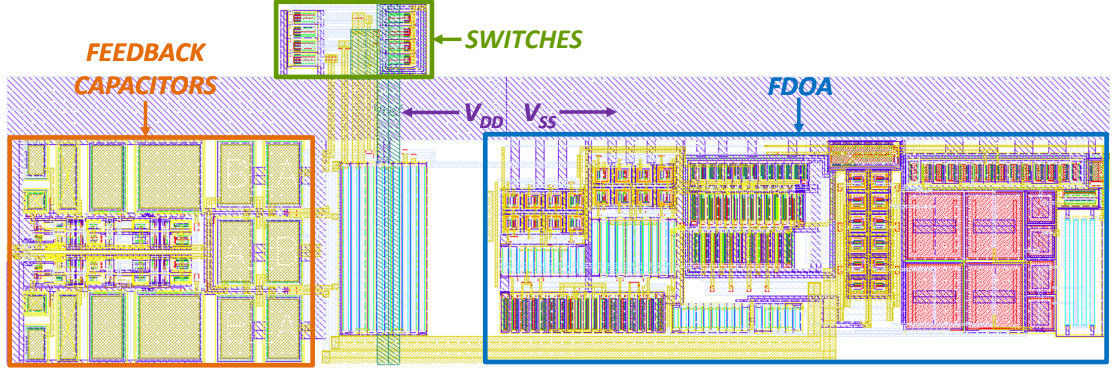


Figure 3.32 – Layout of the switched integrator.

3.6.1 Switched integrator layout

Figure 3.32 shows the layout of the switched integrator. Same layout techniques described for the previous stages were used to improve device matching of the resistors and capacitors. The capacitors are programmable, hence, they are divided in different sizes and connected through switches to the channel register.

This cell is duplicated in each channel. When placed in the final layout, the voltage source and ground bus separates them from an inner zone where the switches and clock signals are isolated from the analog circuits.

The feedback capacitors are programmable from a minimum value to a maximum. There are two capacitors which are always connected for the minimum value. The programmable parts are divided in sizes ranging from the minimum step to the maximum size and connected to switches controlled by the register values.

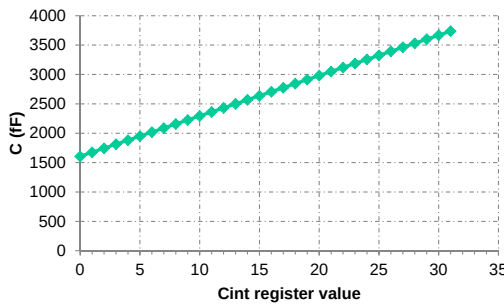


Figure 3.33 – Capacitor values defined by the C_{int} 5 bit of the configuration register.

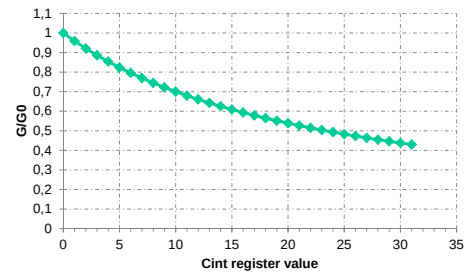


Figure 3.34 – Integrator relative gain Vs. C_{int} . G_0 is defined as the maximum gain and lowest capacitor value.

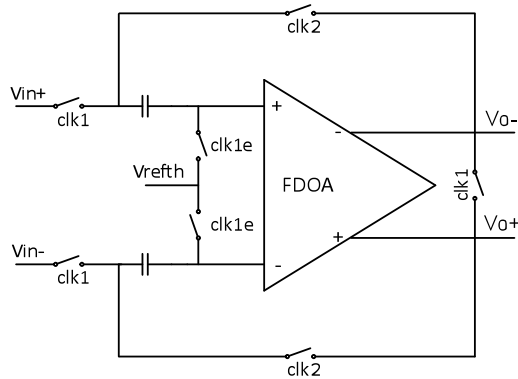


Figure 3.35 – Simplified scheme of the Track-and-Hold.

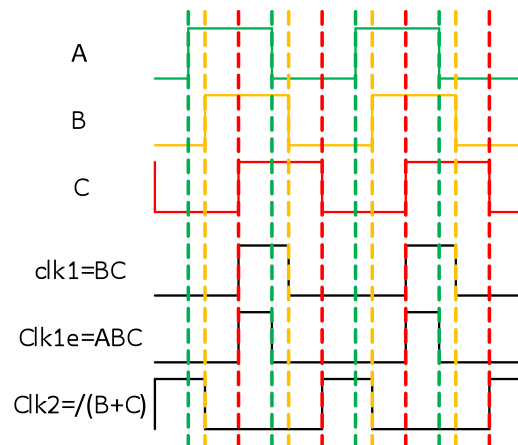


Figure 3.36 – Track-and-Hold clock signals. Phases have been exaggerated for better discrimination between clock edges.

3.6.2 Programmable values of the integrator

The gain objective is set by the sensibility (inverse of gain) specification of 4.5 fC/LSB. The ADC LSB is determined by the fact that the 12 bit ADC input voltage range is 2 V. The integrator feedback capacitor is inversely proportional to gain (Eq. 3.37) and needs to be settled to a known value. The capacitors can vary from 1.5 pF to almost 4 pF in steps of 70 fF using 5 bits of the channel configuration register (Fig. 3.33) with the objective of compensating for fabrication processes variability. Also, the lower 3 bits are different for each sub-channel to be able to have a uniform gain within one channel and to compensate mismatch.

3.7 Track-and-Hold

A Track-and-Hold (TH) providing a stable output is added after the switched integrator. The specifications are driven by the 12 bit accuracy required and by the fact of using half of the clock for slewing and settling the output signal. It is based on the flip around architecture with bottom plate sampling as it helps reducing the tracking capacitor charge error and getting better linearity. The feedback design is preferred with respect to an open loop to improve the linearity and the accuracy. The FDOA used for the integrator is also used for the Track and Hold.

The amplifier needs to meet the following requirements:

- Slew rate of 0.6 V/ns: The time allocated for slewing is about 1/8 of the

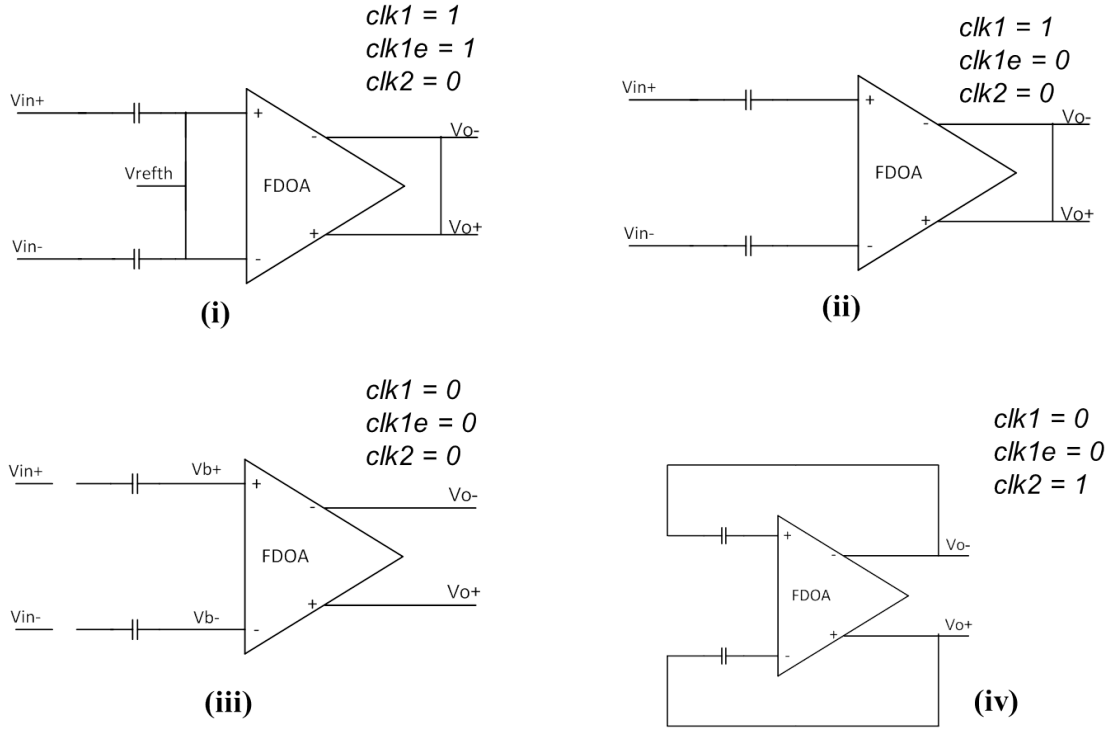


Figure 3.37 – Track-and-Hold phases.

sampling time and with a maximum output swing of 2 V.

- DC gain > 72 dB for an accuracy of 1 bit.
- Gain bandwidth product of 190 MHz.

3.7.1 Track-and-Hold phases

The TH clock signals (Fig. 3.36) are defined in order not to connect directly the input and the output of the amplifier at the same time and, also, to help reduce the non-linearities. All clock signals are derived internally from the global TH clock using 1 ns delay units and logic elements in the same TH block.

- Tracking phase:** The input voltages are sampled into the capacitors through input switches. It is noteworthy that the TH output in the tracking phase it is not equal to the input.
- Bottom plate off:** The switches at the amplifier inputs (driven by $clk1e$ clock signal) close slightly before the input switches ($clk1$), so the charge in

the sampling capacitor cannot change because there is no other DC path, this is called bottom-plate technique which makes the charge injection signal independent.

- (iii) **Input switches off:** The input switches are turned off. As long as the amplifier input voltages are constant (V_{b+} and V_{b-}) the charge stored in the capacitors will be proportional to the TH input voltages (V_{i+} and V_{i-}).
- (iv) **Hold phase:** The feedback switches are activated and the output voltage level is defined by the charge stored in the capacitors.

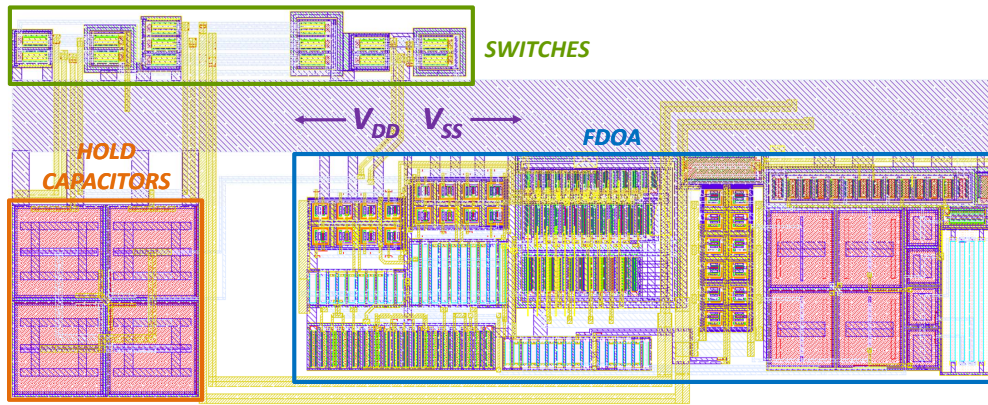


Figure 3.38 – Track-and-Hold layout.

3.7.2 Track-and-Hold layout

The Track-And-Hold layout is represented in Fig. 3.38:

- A bus for the voltage source and ground is placed on the top.
- The ground and V_{DD} separates the central part with the switches and clock generation logic of the channel from the analog part of the two sub-channels.
- The hold capacitors are split in two each one and distributed in a simple common centroid.

3.8 Output buffer

After the multiplexer an output buffer is required for ADC signal adaptation. It is a pseudo-differential capacitive driver made with two class AB Miller operational amplifiers (Fig 3.41) in follower configuration.

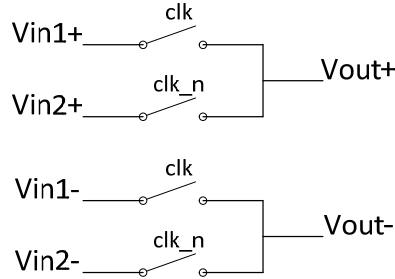


Figure 3.39 – Simplified scheme of the MUX.

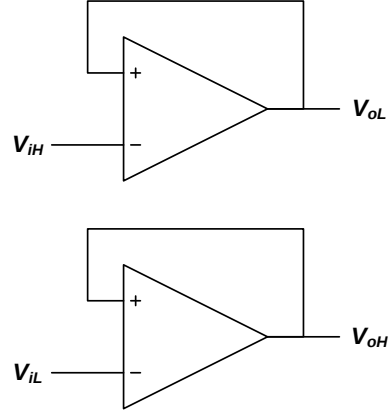


Figure 3.40 – Pseudo-differential capacitive output driver.

3.8.1 Output buffer layout

As in previous layouts, the matching of the transistor pairs has been taken special care on the output buffer layout (Fig. 3.42). All transistors have been placed following common centroids and with the same orientation:

- The differential input PMOS pair was placed in an interleaved two-row layout, with extra dummies at the sides.
- The cascode loads, MN_0 , MN_1 , MN_2 were also placed in two rows.
- The MP_{IN} were divided each in four and placed and matched together.

3.9 ASIC to ADC interface

The ASIC is connected to the ADC with an AC coupling circuit (Fig. 3.43). The AC coupling is composed of three different capacitors of 100 nF, 10 nF and 1 nF to move their inductive behavior to higher frequencies compared to the bandwidth of the circuit. Also, it allows the use of the ADC reference voltages in voltage dividers to define the baseline level at the ADC input to optimize its input range.

After the AC coupling, a low pass filter in differential mode is used to reduce high frequency aliasing.

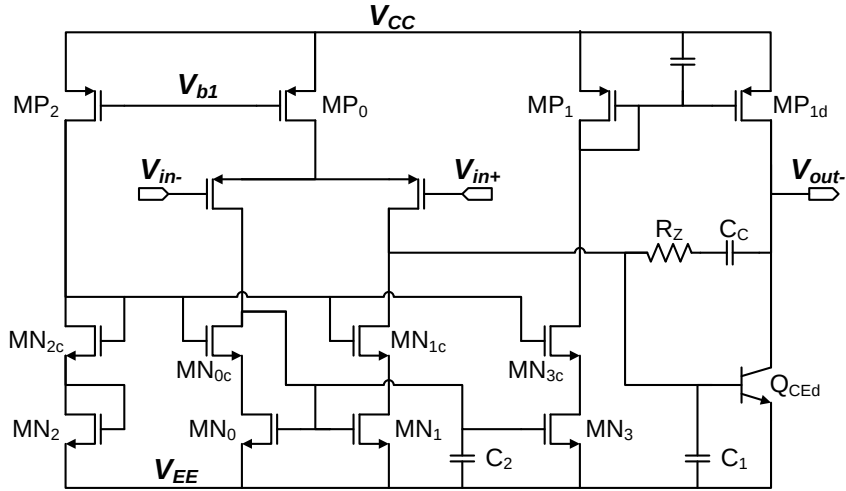


Figure 3.41 – Schematic of the output buffer amplifier.

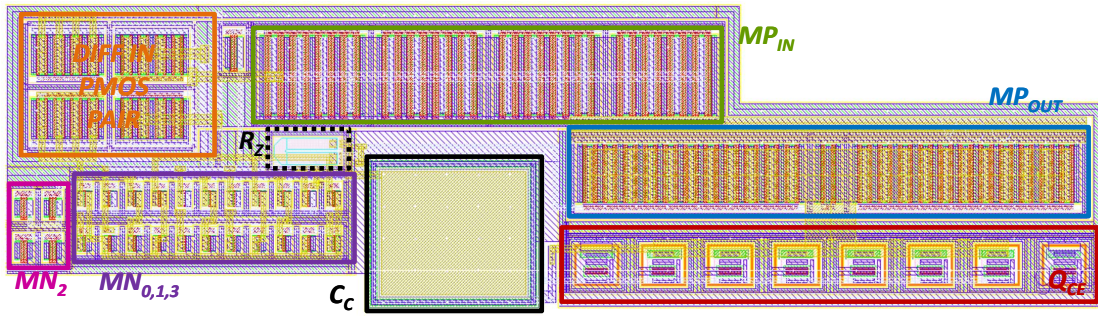


Figure 3.42 – Output buffer layout.

3.10 Full channel simulations

3.10.1 Temperature and voltage variations effect on channel gain

Simulations on a full channel show that the variations of the integrator gain are about 5% between 0 and 80°C, or 0.063 %/°C (Fig. 3.44). In the experiment, the electronics will have a cooling system. In the current crates, the temperature is quite stable (probably less than 1°C variation). Consequently, it is not expected to observe variations in gain during the data taking. Besides, the main variations of gain will be due to the photomultiplier tubes.

The effects of the voltage variations are at the 0.2% level when varying between

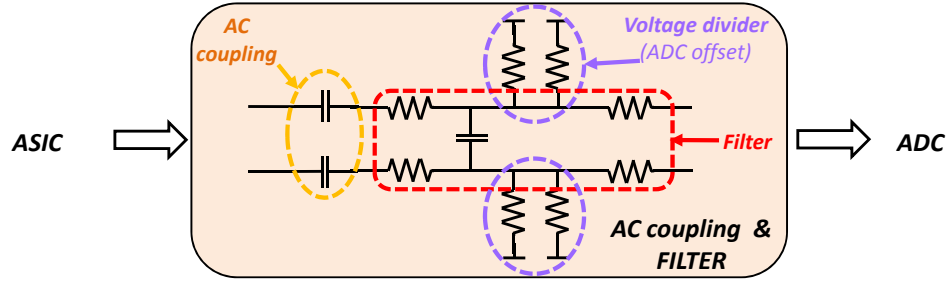


Figure 3.43 – ASIC/ADC interfacing includes an AC coupling, a high frequency filter and voltage divider to set the DC operation point at the ADC input.

3.2V and 3.4V (Fig. 3.45).

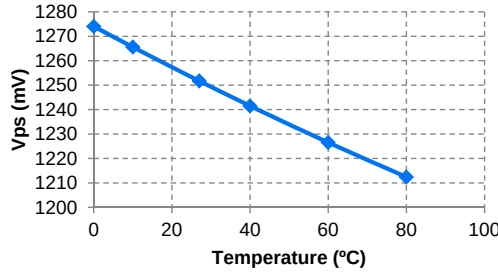


Figure 3.44 – Simulations of the analog channel of the gain variations with temperature.

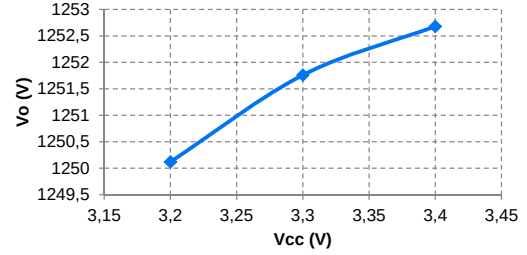


Figure 3.45 – Simulations of the analog channel of the gain variations with voltage source.

3.10.2 Linearity and offset

A programmable offset created by current at the integrator input (Fig. 3.46) is added before the integrator stage. It modifies the integrator output DC voltage by integrating a fixed current in order to exploit the full dynamic range of the differential circuit. As simulations show (Fig. 3.47), without offset the linearity is lost at 1,8V of the output signal (the voltage range is 2V). The cause is the single-ended limit to the maximum output voltage of the FDOA at the NMOS stage used in the TH block. After the application of the offset at the integrator output, the linearity error is below 1% for all the signal range.

The programmable voltage level ranges from 0 to 1.5 V in differential mode and it is fixed with 6 bits: 4 MSB common and 2 LSB different for each sub-channel. As a result, it is possible to compensate up to 71 mV difference between

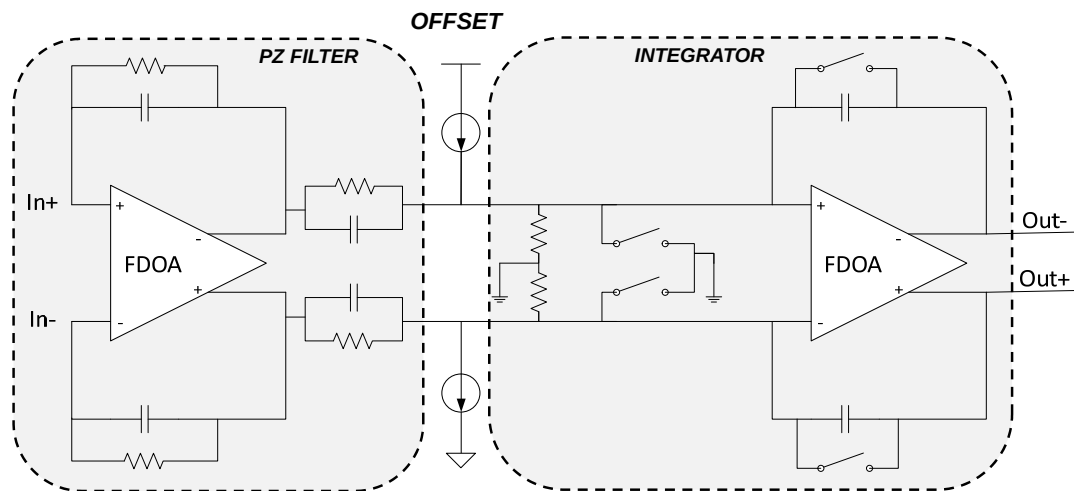


Figure 3.46 – The offset at the integrator output is generated by the integration of a constant current source at the integrator input.

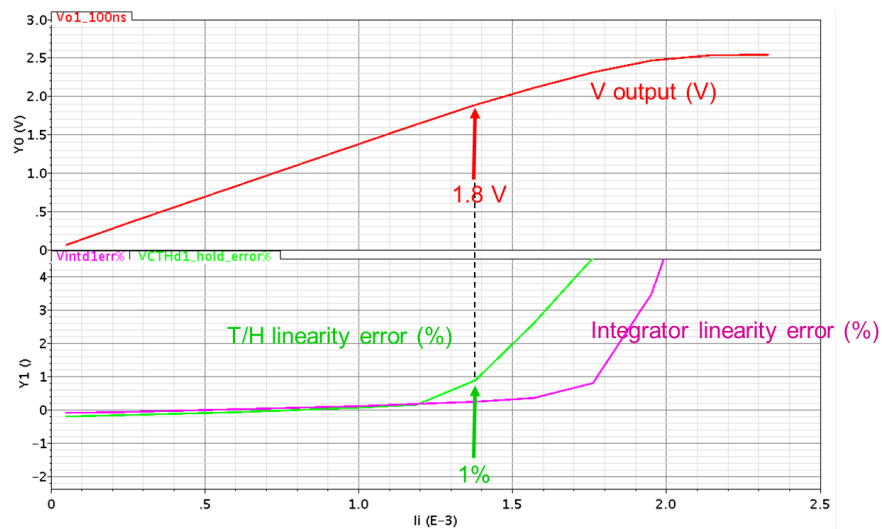


Figure 3.47 – Simulations results showing the non-linearity error after the integrator stage vs. the TH stage before applying an offset to increase the linearity range.

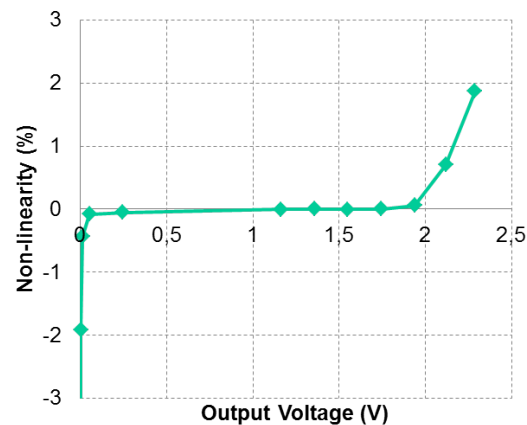


Figure 3.48 – Linearity after adding offset.

subchannels. This feature can be really useful to distinguish between sub-channels (programming the maximum and minimum offset for each).

The price to pay for a better linearity is an excess noise for large offsets. Simulations of the full channel show that for low offsets, which are enough to ensure good linearity for the full signal range, noise is still within specifications (Section 3.10.4). Obviously, if higher offsets are programmed, noise is increased as a consequence.

3.10.3 Temperature and voltage variations effect on the offset

It is planned to access to an acclimatized chamber space to measure the effects of temperature on the analog channel. Otherwise, simulations show that the variations of the integrator offset are about 0.1% between 0 and 80°C compared to the 2V maximum amplitude (Fig. 3.49).

The effects of the voltage variations are at the 0.4% level when varying the analog source between 3.2V and 3.4V (Fig. 3.50).

3.10.4 Channel noise simulations

Noise simulations can be performed using dedicated Spectre tools. The classic approach to obtain the PSD is not well suited for the case of a switched system. The main tool used was the transient noise simulation. It is an intuitive method, since it simply relies on injecting transient noise waveforms for each noise source present in the circuit. The transient noise waveforms are automatically generated

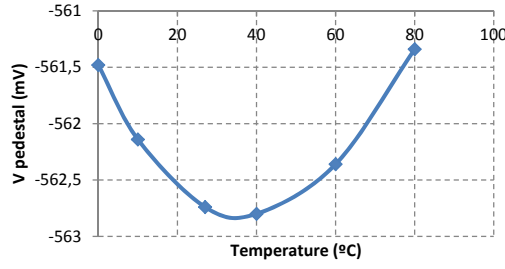


Figure 3.49 – Simulations of the analog channel of the offset variations with temperature.

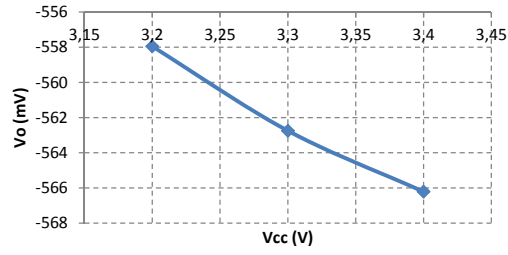


Figure 3.50 – Simulations of the analog channel of the offset variations with voltage source.

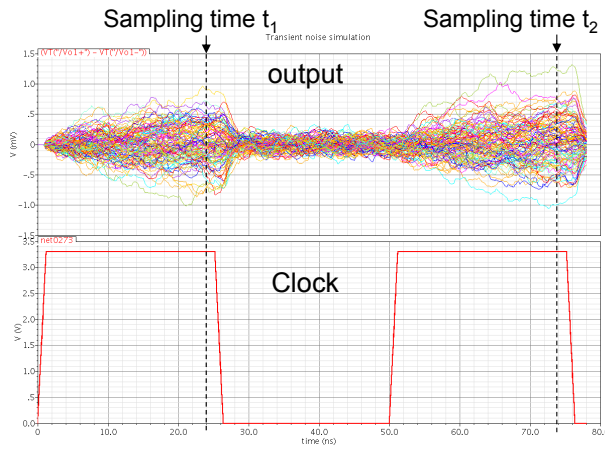


Figure 3.51 – Transient noise simulation of one integrator output.

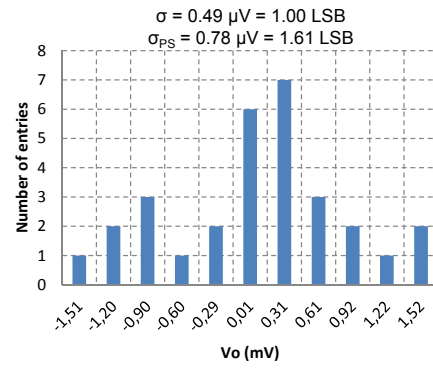


Figure 3.52 – Full analog channel noise after pedestal subtraction from transient analysis.

by the tool and superimposed onto the noiseless transient waveforms. The larger the number of waveforms generated, the more statistics are obtained for the study. Transient noise simulations are relatively easy to set up. The two most important settings relate to the maximum and minimum noise frequencies of interest. All other settings are similar to the conventional transient analysis. An example transient noise output voltage of one sub-channel integrator waveform is presented in Fig. 3.51. The quiet periods of the waveform correspond to the integrator reset phase. In the integration phase time slots, the output is not connected to ground through switches and is charging the feedback capacitors and the noise increases. To estimate the variance of the noise samples, one can run a simulation over many cycles (e.g., 500), and compute the sample variance of the output near the end of the hold phase. It is also possible to compute the variance after applying the pedestal subtraction or CDS comparing the sampling times $V(t_1) - V(t_2)$.

The results of a transient post-layout simulation for the full analog channel is presented in the histogram of Fig. 3.52. The process is slow and it requires a great part of the resources of the design dedicated servers. The simulated noise obtained is 1.0 and 1.6 ADC counts with pedestal subtraction.

3.11 Radiation protection techniques at layout level

The radiation level expected for the electronics located on the gantry suffers a dose estimated to be $100\text{rad} \cdot \text{fb}^{-1}$ [8], [9]. This is a limited dose. The problems that may be observed during operation are mainly cumulated dose effects, single event effects (single event upset (SEU) and single event latch-up (SEL)).

The radiation hardness expected from the selected technology (0.35 μm AMS BiCMOS) is enough [10] [11] [12], but design techniques are used to help reduce its effects (Sec. 3.11.2 and 4.3.6).

3.11.1 Radiation effects

Radiation effects on electronic components are usually divided in three categories [42] [43]:

1. **Total ionizing dose (TID):** Total Ionizing Dose effects on integrated circuits are the origin of variations of the threshold voltage of MOS transistors. Energy deposited by radiation in the form of ionization causes trapped charges in the silicon dioxide gate insulator. For sub-micron devices these trapped charges can potentially "escape" by tunneling effects. Leakage currents are also generated at the edge of (N)MOS transistors and potentially between neighbor N-type diffusions. Commercial digital CMOS processes can normally stand a few krad without a significant increase in power consumption. Modern sub-micron technologies tend to be more resistant to total dose effects than older technologies. Otherwise, high performance analog devices (e.g. amplifiers, ADC, DAC) may potentially be affected at lower doses. The International System unit for TID is the Gray (Gy). One Gray is defined as the absorption of one joule of energy, in the form of ionizing radiation, per kilogram of matter. Nevertheless, it is quite common to use the rad unit. The conversion between these units is direct: $1 \text{ Gray} = 100 \text{ rad}$.
2. **Displacement damage:** Hadrons may displace atoms in the silicon lattice of active devices and thereby degrading the electrical characteristics of

semiconductor devices. Bipolar and especially optical devices (e.g. Lasers, LEDs, Optical receivers, Opto-couplers) may be very sensitive to this effect. CMOS integrated circuits are normally not considered to suffer degradation by displacement damage. The induced damage is a function of the particle nature and energy, the Non-Ionizing Energy Loss (NIEL) is used as a parameter. It takes into account the total effect of different types of hadrons at different energies are translated into a simpler mono-energetic equivalent, namely 1 MeV neutrons.

3. **Single event effects (SEE):** Single Event Effects refer to the fact that it is not a cumulative effect but an effect related to single individual interactions in the silicon. Single Event Effects (SEEs) are induced by the interaction of an ionizing particle with electronic components. Ionizing particles can be primary (such as heavy ions in space environment or alpha particles produced by radioactive isotopes contained in the die or its packaging), or secondary (recoils) created by the nuclear interaction of a particle, like a neutron or a proton with silicon, oxygen or any other atom of the die. In the LHCb, the SEE are mainly generated by secondary ionizing particles. The different SEE effects are normally characterized by an energy threshold and a sensitivity cross-section at energies well above the threshold.
 - (a) **Single event upset (SEU):** The deposited charge is sufficient to flip the value of a digital signal. Single Event Upsets normally refer to bit flips in memory circuits (RAM, Latch, flip-flop) but may also in some rare cases directly affect digital signals in logic circuits.
 - (b) **Single event latchup (SEL):** Bulk CMOS technologies (not Silicon On Insulator) have parasitic bipolar transistors (Fig.3.54) that can be triggered by a locally deposited charge to generate a kind of short circuit between the power supply and ground. CMOS processes are made to prevent this to occur under normal operating conditions but a local charge deposition from a traversing particle may potentially trigger this effect. Single event latchup may be limited to a small local region or may propagate to affect large parts of the chip. The large currents caused by this short circuit effect can permanently damage components if they are not externally protected against the large short circuit current and the related power dissipation.
 - (c) **Single event burnout (SEB):** Single event burnout refers to destructive failures of power MOSFET transistors in high power applications. For HEP applications this destructive failure mechanism is normally associated to failures in the main switching transistors of switching mode power supplies.

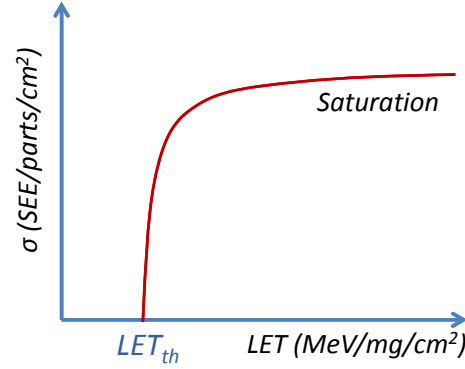


Figure 3.53 – Typical cross-section vs. LET measurement.

SEE are statistical effects. Two main concepts are used to study them: the device (or bit) cross-section as a function of the energy deposited in it. When a particle strikes the device and has enough energy to deposit a charge that is able to trigger a single event if it passes through a sensitive volume. The energy transferred to the silicon is called Linear Energy Transfer (LET). Device immunity is determined by its linear energy transfer threshold (LET_{th}). The LET_{th} is defined as the minimum LET to cause a single-event effect at a given particle fluence. For different LET the integrated circuit presents a cross-section which can be defined per device (or per bit):

$$\begin{aligned}\sigma_{dev} &= \frac{\text{Number of SEE recorded during the experiment}}{\text{Fluence of the experiment} \times \text{Number of devices}} \\ \sigma_{bit} &= \frac{\text{Number of SEE recorded during the experiment}}{\text{Fluence of the experiment} \times \text{Number of bits}}\end{aligned}\tag{3.38}$$

As a consequence, the SEE testing product can be plotted in an interaction cross-section vs. particles' LETs (Fig. 3.53).

3.11.2 Radiation hardness techniques

In order to reduce the radiation effects on the ASIC, some techniques were considered during the design phase [13] [14] [15]:

1. At layout level, add guard rings to prevent latch-up effects. It also helps protecting against noise and cumulative effects. All transistors, gates, resistors and capacitors in the design included guard rings. Typical rings are composed by a metal line, contacts and P⁺ diffusion. In case of PMOS transistors, there is another inner ring with N⁺ diffusion (Fig. 3.55).

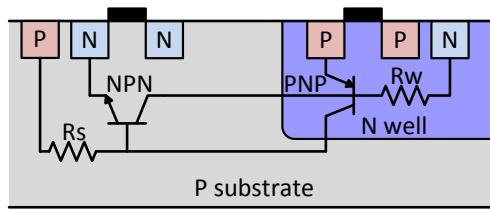


Figure 3.54 – CMOS cross section showing parasitic bipolars.

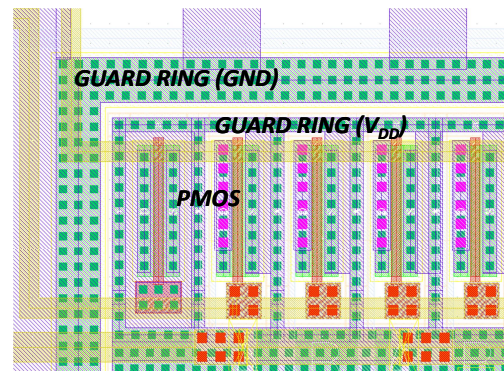


Figure 3.55 – PMOS guard rings example.

2. The use of Triple Voting Redundancy (TVR) to minimize the single event effects in the registers that keep the internal configuration of the chip. The TVR registers consist in adding redundant flip-flops for each bit and include comparator logic that filters 1 error (a more detailed explanation can be found in Sec. 4.3.4).
3. Use NAND gates wherever possible instead of NOR gates, improves the immunity because these last are more sensitive to accumulative effects.

Although other techniques to improve the hardness radiation exist, they imply different manufacturer technologies and using non standard libraries and foundries, with a significant increase of the cost (for example SOI, DMILL, ELT). Taking into account the radiation levels expected, it seems not necessary to implement the design with the use these techniques or search for a smaller technology move for radiation damage considerations. Anyway, radiation tests are always necessary to certify the levels which can be acceptable for the electronics.

Digital block

In this chapter the digital block is presented. An overview schematic of the digital block is pictured in Fig. 4.1. The main sub-blocks are:

- The delay line (DLL), in grey at the center of Fig. 4.1, implements 4 channels (one per analog channel) with 3 independent clock sub-channels (for the integrator, Track-and-Hold and external ADC). Each channel can be configured in one of the 25 clock phases of 1ns step.
- The fast control. It fixes the analog sub-channel in use for each clock phase using reset circuit.
- The slow control, which includes the Serial Peripheral Interface (SPI) slave interface and the serial registers to configure the chip. The chip SPI communication protocol offers a bit rate up to 20 Mbps. For reliability reasons, the registers are designed with triple modular redundancy (TMR) architecture and they can be read-only or read-write for status information or configuration purposes.
- The reset of the chip can be triggered in two ways which are routed to an *OR* gate. One is a power-on reset circuit takes 1ms to take effect. The other is an external signal which is filtered with a glitch suppressor ($\leq 8\text{ns}$) ensuring that SETs do not accidentally reset the chip.

4.1 Delay line

This section describes the implementation of a digital programmable delay line which has been integrated into the ICECALv3 chip. This delay line not only

4.1.2 Analog channel synchronization

As it can be observed in figure 2.10, every analog channel requires four clock phases to sample data without committing errors. Moreover, the integrator, the TH and mux expect a constant high or low level depending on the defined states during a clock cycle. Consequently, the clocks sent to those stages have half the detector clock frequency (20 MHz instead of 40 MHz).

The first step is to synchronize channel input data coming from the PMT. Signal phase arrival cannot be fixed a priori since it depends on many factors such as, PMT bias voltages, cable lengths or fiber dispersion, among others. Therefore, we have to assume that input signal may arrive at any phase within the 25 ns LHC clock period. The first parameters to be set are the integrator reset and TH phases: when integrator reset is at low level the input pulse is integrated, and one instant before the integrator reset goes high TH holds the integrator signal. As both clock events are certainly related and as seen in Fig. 3.2, while TH clock is able to cover the 25 clock input phases, integrator clock is referenced to the TH clock can only be tuned in a range from 0 to 4 ns. During system synchronization at the initial stages of the ICECAL tests (section 6.3.1), experimental results revealed that the optimal phase (in terms of planarity) between hold and integrator reset was 1 ns.

Once the signal is shaped, the ASIC channel alternatively switches each of the two sub-channels outputs by means of a multiplexer. The same clock as TH is used for this purpose.

Finally, each ASIC analog output has to be sampled with an external ADC. Despite the fact that timing differences between ASIC analog outputs and ADC inputs may not vary substantially between different ASIC channels, we considered to make it adjustable for two reasons: the first is that the optimal phase delay between ASIC output and ADC input depends on the Front-End PCB design, which has not been defined yet. The second reason regards to the phase between and FPGA clocks; ADC clock phase can be set in a region where track-to-track skew and other timing uncertainties do not affect data transmission reliability.

4.1.3 Voltage controlled delay lines (VCDL)

Each delay line channel (see Figure 4.2) contains two VCDLs: the first one provides 25 phases of the input clock in steps of 1 ns (to cover a full LHC clock cycle), while the second only provides 5 phases of the TH clock output in steps of 1 ns, enough to produce a small delay between TH and integrator clocks. The main feature of a VCDL is its dependence on an external control voltage which enables a fine adjust of the internal Delay Elements (DE). Each VCDL has as many adjustable DEs as output phases and each stage provides a delay of 1 ns. DE is controlled by means of two signals: Vcoarse and Vcontrol. The former is

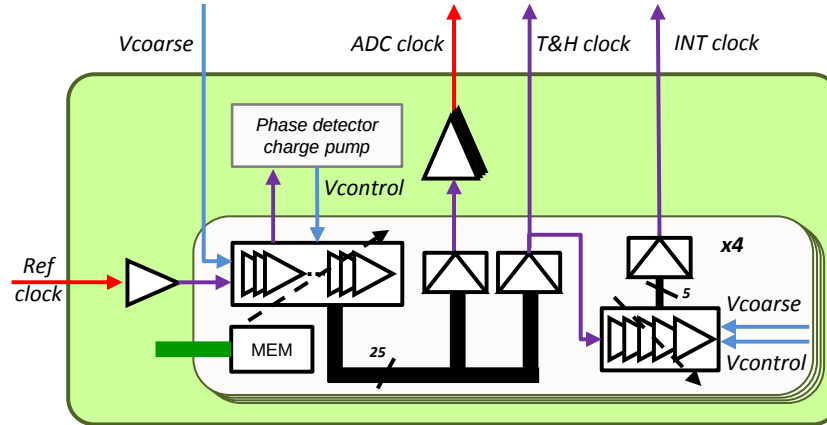


Figure 4.2 – Delay line schematics.

externally adjusted by the user and aims to compensate process variations while the later is automatically generated by the phase comparator and charge pump circuit to compensate dynamic variations.

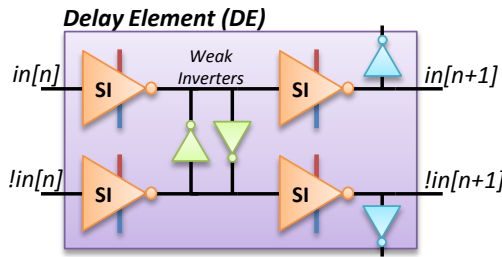


Figure 4.3 – Delay line basic element

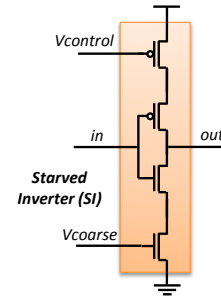


Figure 4.4 – Starved inverter

During the Engineering Design Review of the ICECAL at CERN it was recommended to increase the number of delay-cells in the DLL's charge pump loop by a factor two to reduce the accumulated non-linearity error in the last phase step (the Integral Non-Linearity or INL). An increase of the feedback loop regulation to go across two BX cycles would aim of forcing all 25 used DLL clocks to be well within their respective 1ns windows. This suggestion would be taken into account in case of a new version of the chip, but it is not considered a reason for a new chip version per se because:

1. The non-linearity error is very low and can be reduced by means of the VCOARSE control signal.

2. It is possible to send the clock or the inverted clock to the ASIC DLL to reduce the error.

Figure 4.3 shows the structure of the adjustable DE: starved inverters not only invert the input signal but also apply a delay as a function of V_{control} and V_{coarse} signals. Weak Inverters (WI) ensures that differential signals are in phase. This becomes critical in the latest VCDL stages, where the INL due to mismatches between counterpart starved inverters may produce different clock phases. Finally, common inverter is placed at the end of each stage to isolate DE from the input capacitance of the multiplexer.

The starved inverter schematic is shown in Figure 4.4. It is based on a common CMOS inverter where the PMOS/NMOS sources are not directly connected to power rails but they pass through a MOS transistor acting as an adjustable resistor. The starved inverter speed will decrease with the increase of the impedance. The impedance adjust, i.e. delay adjust, of these MOS transistors is done by varying the input voltage of their gates.

The main advantages of using of two control transistors versus the use of only one NMOS transistor are the range of delays that can be achieved and the slew rate symmetry, critical to achieve an end to end delay of 25 ns. The main disadvantage is obviously the area overhead and the need to control an additional signal.

4.1.4 Phase detector and charge pump

The aim of this block is to determine the VCDL performance and generate a control voltage (V_{control}) according to this performance. Phase detection is done in two steps (see Figure 4.5): on the one hand a flip-flop detects whether the reference clock signal $n+1$ rising edge arrives before or after the expected 25 ns delayed clock signal n rising edge. To do so, the reference clock is used to sample the delayed clock; if delay is lower than 25 ns, when the reference clock latches the input, the output is high (charge), otherwise the output is low (discharge). On the other hand, an XOR between the previous two clock signals will determine the amplitude of the pulse. Combining clock phase module and sign information, we generate a charge/discharge signal that increases or decreases the stored charge in the capacitor that generates V_{control} . As for the locking time, we cannot give a precise value (it depends on the initial delay) but we can range it between 2.5 and 10 μs . Capacitor RMS ripple voltage was measured to be 6.64 mV.

Previous DLL prototype measurements revealed that V_{control} values did not changed substantially between the four delay line prototype chip channels. Therefore, in order to save die area in the final prototype (ICECALv3) we considered to use only one phase detector per chip which monitors the VCDL from channel 0 and generates a common V_{control} for all the delay line channels (see Figure 4.2).

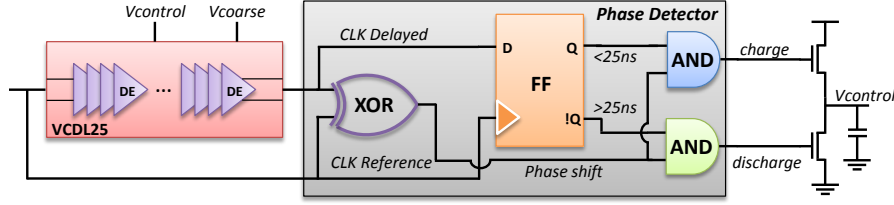


Figure 4.5 – DLL phase detector and charge pump scheme.

4.2 Fast Control

The fast control system of the chip takes care of the control signals synchronous to the LHC clock. In the case of the ICECAL, an analog channel consists in two sub-channels. It is necessary to define which analog sub-channel is on for every bunch crossing to define its correspondence to the pedestal and gain calibrations. At the LHCb detector level, it is common to refer to every particle bunch crossing or LHC clock cycle with a number known as the Bunch Crossing ID [44], or, from now on the present text, as the BXID.

In order to proceed (Fig. 4.6), the FE FPGA generates a 1-cycle width synchronous reset cycle which is captured and resynchronized with the input clock in the ASIC. It is imperative to always obtain the same sub-channel for each BXID parity (even or odd) once all the DLL phases are set or else, it will not be possible to define the correspondence to the analog sub-channel offset and gain calibrations. It is possible to achieve this condition discarding all the metastable phases between the FPGA and the ASIC. Consequently, an important constraint is added to the synchronization of the ICECAL chip (as it will be seen in section 6.3.1).

Other options for the sub-channel tagging would include a dedicated synchronous signals and they would increase the number of pads of the ICECAL chip and the complexity at the FPGA dedicated to capture the ADC data. So it is preferred to use a sub-channel reset and define the sub-channel parity respect the BXID for each DLL settings, as it will only be done once with the definitive FE design.

Otherwise, the fast control block is completed with two debug signals:

- An external pad (*SubChRstSync*).
- A status slow control bit (*Detected*).

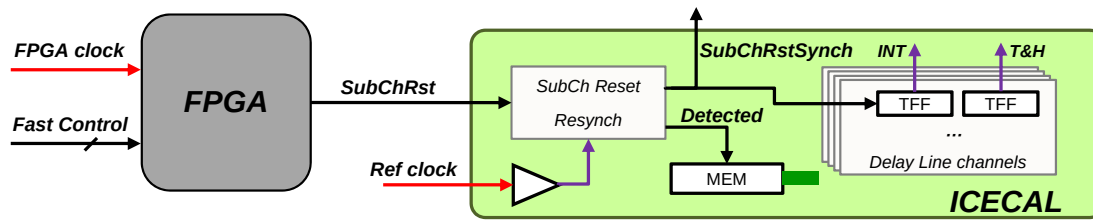


Figure 4.6 – Analog sub-channel reset.

4.3 Slow Control

The slow control system of the chip is the set of circuits that are used to control the configuration parameters which do not change during the data taking, like clock phases, biasing points, input impedance, channel gain and the pole-zero frequencies. It is implemented using a standard serial signals and protocol. This interface permits to read/write the ICECAL internal registers.

4.3.1 SPI interface

The major challenge of the slow control is the robustness against single events. For this reason we use SPI (Serial Peripheral Interface) protocol instead of I2C, since synchronous protocols such as SPI are less likely to fail due to SETs [7]. In order to tolerate SEUs, the SPI Slave Control Unit (CU) uses redundant bits in the state machine, and serial control registers are implemented using TMR. SELs are prevented by using double guard rings between PMOS and NMOS transistors. The goal of SPI Slave is the address decoding and register selection. It can map up to 32 configuration registers (16b read/write) and 32 status registers (16b read only). It also generates read/write signals to the serial registers and also implements a software reset command that enables the user to reset the charge pump of the DLL, and a bypass MOSI-MISO command for troubleshooting purposes.

4.3.2 Data transmission

As observed in Figure 4.7, each SPI frame consists in 3 bytes: 1 byte for addresses or commands and 2 bytes for data. The first bit in the transmission determines the data direction (read+write operation). When low, data is written to the selected register through MOSI pin while previous data can be read simultaneously from MISO pin (read+write operation). When high, data is read from the MISO pin (read only operation).

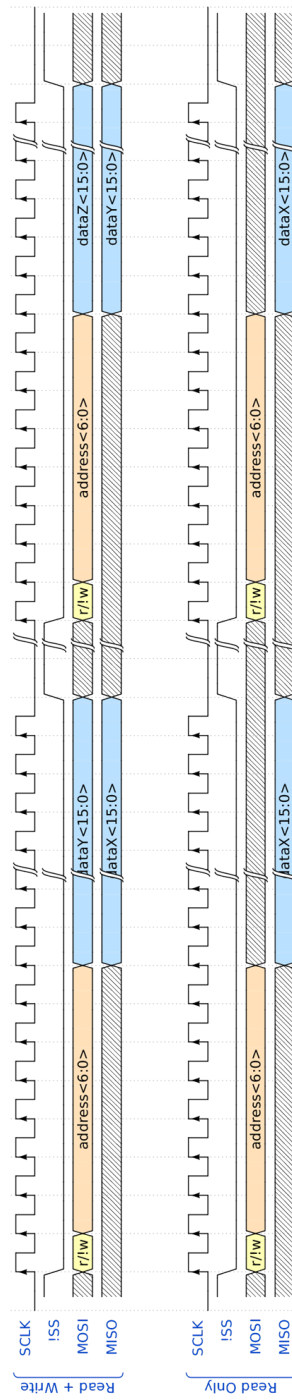


Figure 4.7 – An example of register read+write access (top) and register read only access (bottom).

4.3.3 Register addresses and functionality

There are four different types of slow control frames according to the SPI address: soft reset command, SPI bypass command, status register access (read only), and configuration register access (read only and read/write). The latest can be for an ICECAL channel configuration, a DLL channel configuration or a global chip configuration. Table C.1 defines the values of the 8-bit SPI address frames, while Tables C.2 and C.3 list the exact address for each of the status and configuration registers (Appendix C). In one hand, the status registers provide information about the ICECAL operation and they can only be read. On the other hand, the configuration registers store the parameters that set the parameters of the different circuits of the chip.

When software reset command is issued, the internal charge pump which controls delay lines is reset, and therefore, it forces the delay lines to be resynchronized with the reference clock. This is useful to recover delay lines without a hard reset (which implies register data configuration loss).

The SPI bypass message command loopbacks MOSI and MISO lines during the transmission of the next 16 data bits. This message eases the troubleshooting procedure.

The main control register of the chip is essentially used for bias currents of the operational amplifier at the different analog channel stages and the input preamplifier and it is shared by the four analog channels (see Table C.4 in appendix C for details). The bias values are then common to all channels. If differences in the channel response arise, it is possible to minimize them with the parameters on each of the analog channel register. The different bias currents used at each stage of the channel are exposed in Table C.5 (Appendix C). A 6-bit DAC varies the current value (maximum value is $m \times 135\mu\text{A}$).

Each analog channel register contains the corresponding bits to control the key parameters and compensate for process variations (Table C.6 in appendix C) for each analog channel. In some cases, the LSB are separated for sub-channel to sub-channel compensation. It is possible to vary the values:

- The integrator capacitor (for gain variations).
- Offset for linearity range increase.
- The pole and zero frequencies of the PZ filter.
- The input impedance.

A delay line channel configuration register is defined for each analog channel. The values of the integrator, TH and ADC clock lines used are defined in Table C.7 (Appendix C). It is also possible to configure four different output current modes

in order to reduce the power consumption of the lines (and of the chip). The downside of reducing the current output is the reduction of the differential voltage values (it is necessary to check if the connected components can properly capture the clocks) and that the jitter could be increased.

4.3.4 Triple voting registers

As previously commented, due to the radiative environment where the final implementation will operate implies the use of different techniques to reduce its effects. One of them is the redundancy of data that needs to be stored. The Triple Modular Redundancy (TMR) consists in replicating three times the same memory bit and selecting the output that corresponds to the majority. Thus, even if one (and only one) SEU occurs not only the output data will be corrected, but also the erroneous bit will be automatically revised in the next clock rising edge. The probability of more than one SEU in the redundancy flip-flops for one memory bit is considered very low. Fig. 4.8 shows the schematic of the TMR implemented, including three flip-flops and a feedback (*b0*).

In order to make TMR registers more resilient, flip-flops were physically interleaved in a factor 4, i.e. the first set of 4 registers corresponds to the first input bit of the majority voting circuit of four different output bits, the second set of 4 to the second input bit, and so. In this way, the distance between redundant flip-flops is higher than $100\mu\text{m}$. Hence, the basic TMR block is 4-bit wide.

Configuration Registers are merely an array of four 4-bit TMR blocks and parallel-serial registers that interface with the SPI. Notice that TMR register is recovered from SEUs only after the rising clock of the SPI clock. Therefore, the simplest way to minimize the probability of suffering two SEUs in the same TMR block is periodically reading any of the SPI registers, since SPI Master will generate several clock pulses and TMR bits will be updated.

Finally, TMR register simulation (Fig.4.9) shows how the register output is not affected by the SEU that one of the internal registers suffers. Moreover, this corrupted register is automatically recovered after the next rising clock edge.

4.3.5 Finite State Machine

The SPI slave is controlled by a Finite State Machine (FSM) (Figure 4.10). The Hamming distance between the states is more than one bit difference to be resistant to one SEU. For example, when a SEU occurs during the idle state (binary coded 101), none of the possible fake states (binary coded 001, 100, 111) are involved with the address decoding procedure. Once next rising clock edge arrives, FSM is automatically recovered.

Notice that FSM and TMR registers refresh the internal register value, to prevent

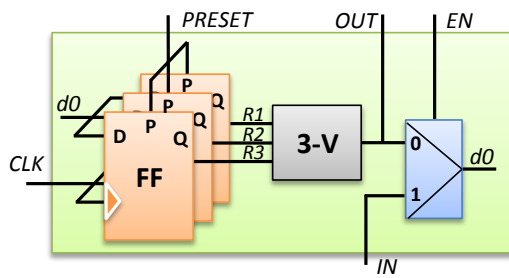


Figure 4.8 – TMR register diagram

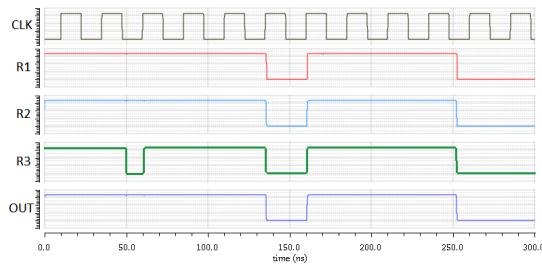


Figure 4.9 – No SEU effect in register output

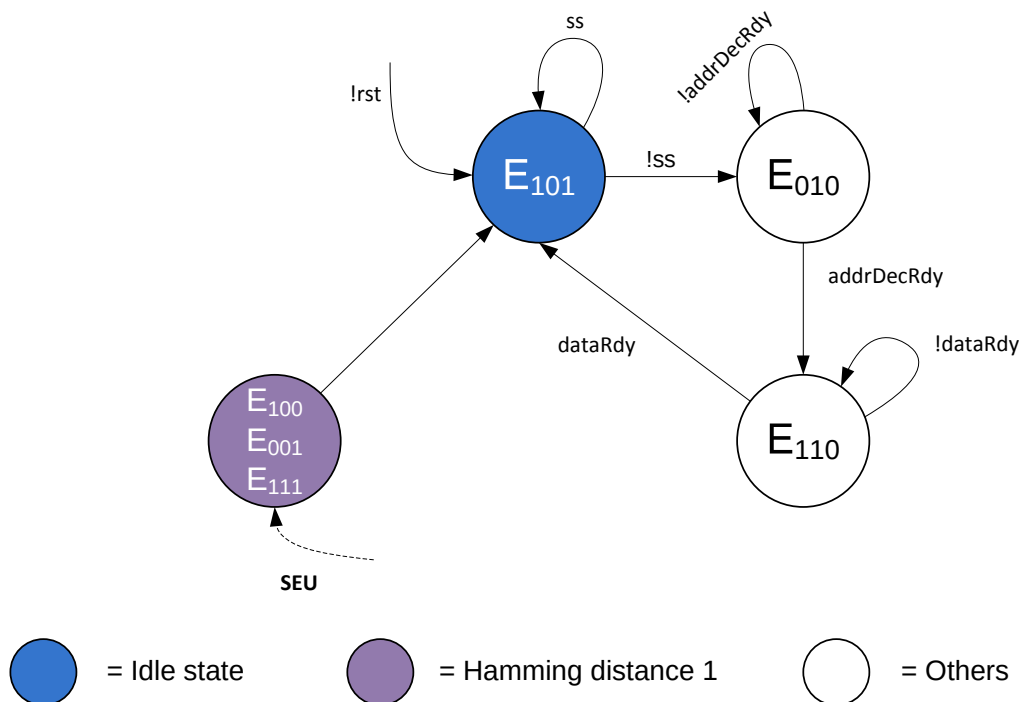


Figure 4.10 – Slow control finite state machine

from suffering SEUs, as long as slow control clock signal is active (SPI serial clock, *SPISCLK*, pin 40). Therefore, if the same bit in a TMR register suffers two (or more) consecutive SEUs during a long idle period of the SPI bus (during data taking, for example), data might be corrupted. To overcome this problem ICECALv3 is provided with an external pin (41 *SPI_Refresh*) that unclogs the

FSM as well as the TMR registers in case that SEU occurs. This pin is used as a clock signal only when SPI FSM is idle, otherwise refresh signal is ignored (to avoid transmission errors). Moreover, this feature can be enabled or disabled by software by changing the !ClkRefresh.EN bit of the ICECAL main register (see Fig. 4.11).

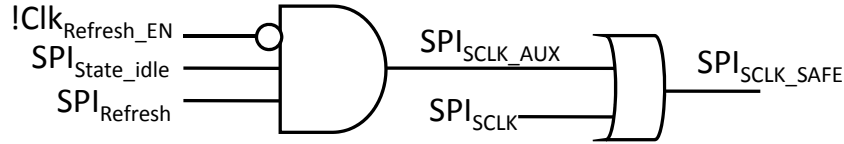


Figure 4.11 – SPI safe clock generation.

4.3.6 Radiation protection techniques at layout level

Regarding the protection against SELs, that may permanently damage the system, one must resort directly to the layout design: the following design rules have been adopted in our layouts to reduce the SEL probabilities.

- The distance between P Diffusion and N-Well must be larger than $5\mu\text{m}$.
- Guard rings are used between PMOS and NMOS transistors.

Fig. 4.12 shows the layout design of 1ns Delay Element (DE) where it can be observed the guard rings between PMOS and NMOS transistors. This illustrates the impossibility of using standard cells and automated layout generation tools. However, in order to make scalable layouts and speed-up the layout design time, a set of basic standard cell-like radiation hard gates (NOT, NOR, NAND, XOR, FF) were implemented to ease the placement procedure. The price to pay is mainly area: each radiation hard cell is around $4.5\mu\text{m}$ higher in comparison with the counterpart standard cell. What is more, the use of guard rings makes not possible the use of POLY to join PMOS and NMOS gates which implies the intensive use of M2 for intra-cell connections, and thus limiting the inter-cell routability of M2. Another obvious drawback is the required manpower to do the manual digital layout synthesis.

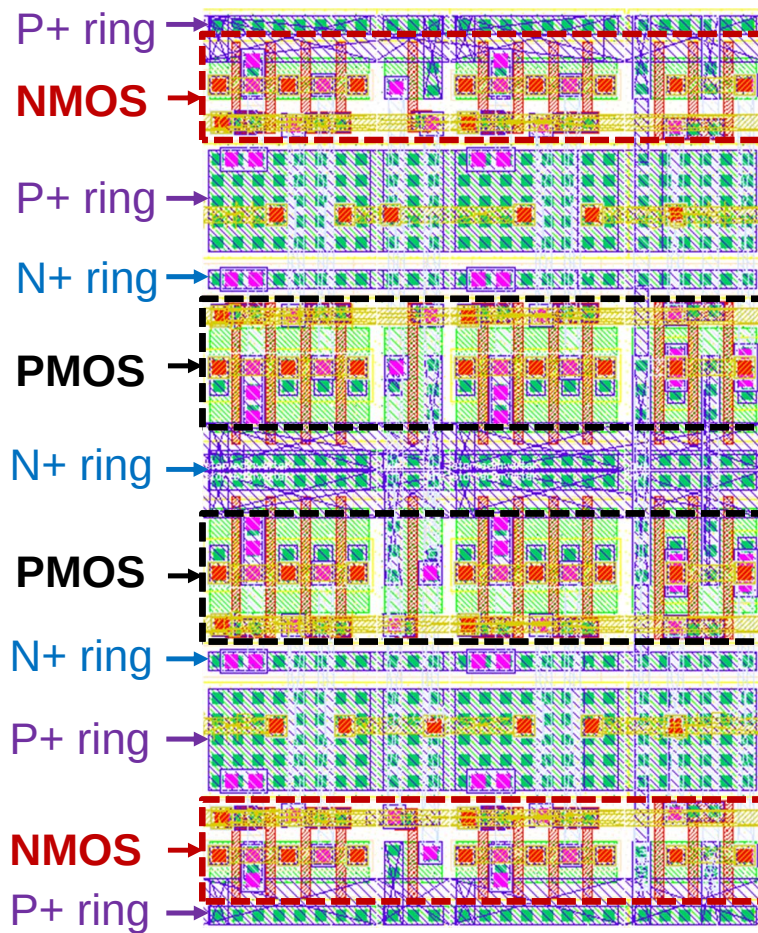


Figure 4.12 – Layout of a 1 ns Delay Element following the radiation tolerance prescriptions.

Chip implementation

5.1 Choice of Technology

Taking into account the design, a SiGe BiCMOS technology was preferred. There were two main reasons for this decision. First, SiGe heterojunction bipolar transistors (HBTs) have higher g_m/I_{bias} than MOS transistors which allows obtaining low noise designs and lower input impedance variation for the same power. And, second, SiGe HBTs display higher transition frequency ($f_T > 50\text{GHz}$), easing the high gain bandwidth product (GBW) amplifiers design. This technology allows 3.3 V operation and the HBT transistors are quite useful for high dynamic range operation. In particular the high transconductance versus bias current ratio of bipolar transistors is very useful to achieve good linearity in current mode solutions.

	IBM	IHP	AMS
HBT f_t	>100 GHz	190 GHz	60 GHz
CMOS	0.13 μm	0.13 μm	0.35 μm
Proto Cost [$\text{€}/\text{mm}^2$]	>3 K	>3 K	1 K

Table 5.1 – Technologies comparison .

AMS BiCMOS 0.35 μm was the technology selected. Although this technology can be considered obsolete by digital standards, there are a number of reasons to support the choice of such a technology. Analog designs do not require the small device dimensions that are essential for complex digital designs, as they use mostly transistors that are considerably larger and/or longer than the minimum dimensions offered by current technologies, as needed to get high performance devices. With four channels per chip the transistor integration density is not an issue.

Also, it offers a transition frequency high enough, and deeper submicron CMOS technology was not needed. Deeper submicron would imply the use of smaller voltage power supply and worse matching. Otherwise, 0.25-0.35 μm technologies are widely used by the automotive industry and other high-reliability and long product-life applications. In those markets, foundries are often requested to maintain technologies available for time spans considerably longer than those required for consumer electronics. Moreover, at the moment of the decision, some preliminary measurements seemed to indicate the AMS technology radiation hardness was robust enough for the project [10].

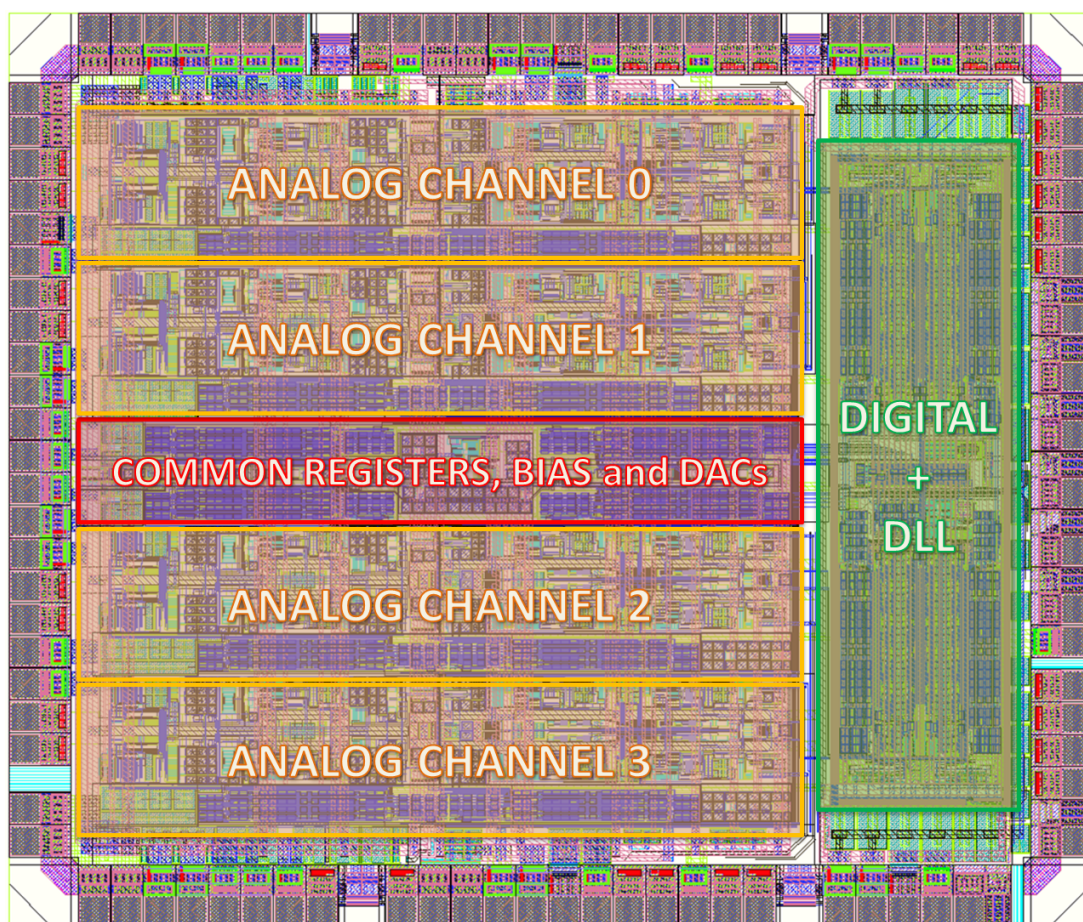


Figure 5.1 – Final ICECALv3 layout.

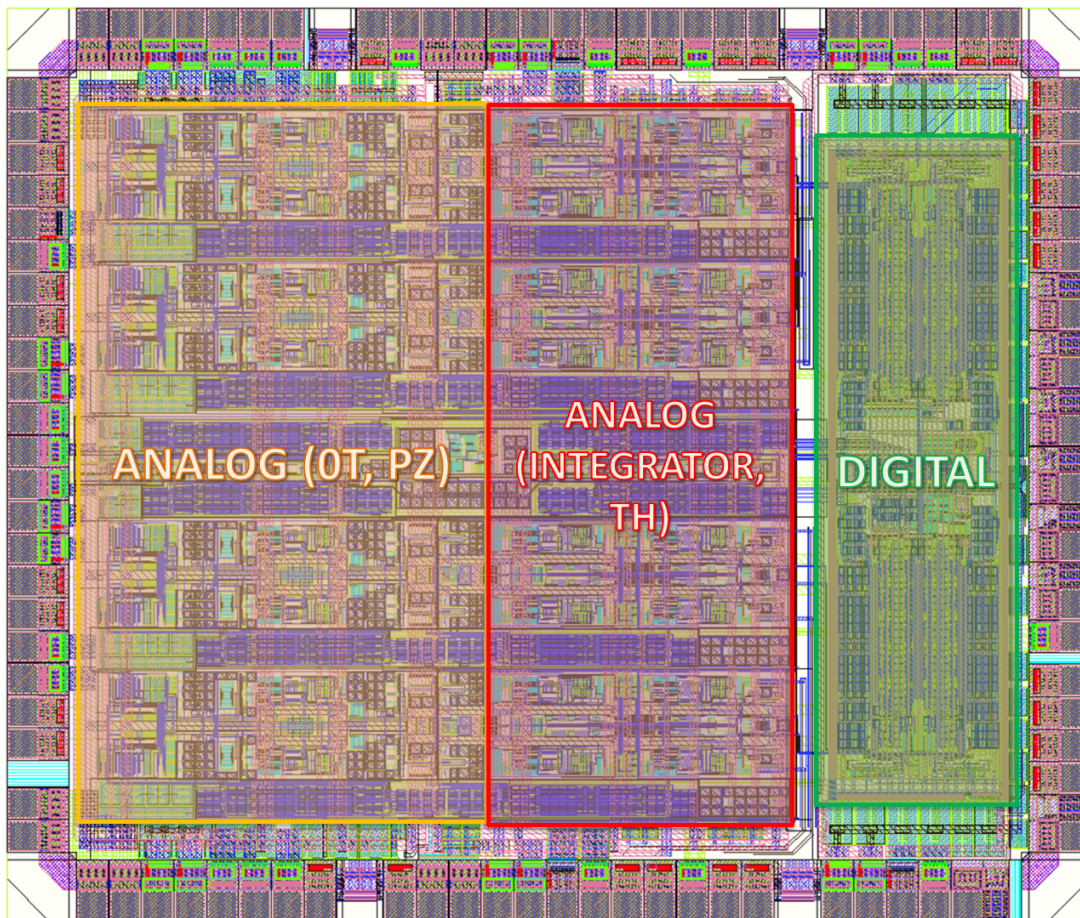


Figure 5.2 – ICECALv3 power domains.

5.2 Chip layout

Full layout of final prototype with a size of 3500u x 2950u can be seen in figure 5.1. The channel processing line is from left to right. In the middle of the chip, the common registers, bias and DACs are placed. On the right part of the chip, the digital block and the DLL are separated from the analog channels using a ring with all metal levels connected to ground to reduce the switching noise.

To avoid coupling through power supply, separated supplies for only analog, analog with switches (integrator and TH) and digital pads have been defined. The grounding is also separated and different substrates are defined at layout design level. The different power domains are the digital 3.3 V and the analog 3.3 V, which is divided in two parts to separate the switched stages from rest (Fig. 5.2). Power supplies are connected from top to bottom, allowing a good connection and

lowering the parasitic resistance by duplicating pads. Decoupling capacitors are placed wherever possible for all power supplies.

The voltages to be used are the analog channel preamplifier reference, V_{ref} , the common mode of the operational amplifier, V_{cm} , and the delay line external coarse adjust, V_{coarse} . They will be common for all chips. At the front-end level, the V_{ref} can be generated using a voltage reference or a voltage divider plus an operational amplifier. The V_{cm} can be obtained with just a voltage divider. And, the V_{coarse} can be implemented with a DAC and an operational amplifier.

5.2.1 Power consumption

Measurements of the power consumption were done with the radiation hardness setup (sec.8), which is designed for current monitoring of the voltage sources and references. Measurements on 3 chips show currents of 16.3 mA, 185.3 mA and 37.0 mA for the V_{ref} , V_{analog} and V_{digital} respectively. Therefore, there is a power consumption of 760 mW per chip.

5.2.2 Pinout

A QFN64 encapsulation with central pad connected to ground has been selected for lower parasitic impedances, better grounding and good thermal connection. The pinout is displayed in figure 5.3. A detailed description is presented in appendix B. Pins are distributed depending on their function:

- **Differential input pins** (2, 3, 5, 6, 11, 12, 14 and 15) are placed on the left side of the chip in pairs separated by ground pins.
- **Differential outputs** (25, 26, 27, 28, 53, 54, 55 and 56) are on top and bottom to avoid the digital region of the layout.
- **Common mode inputs** (20 and 61) are placed on top and bottom.
- **Voltage sources and references:**
 - **Ground** connections (4, 9, 13, 19, 24, 30, 51, 57 and 62) are distributed on top, bottom and left sides. As it can be observed at the bonding diagram (Fig. 5.4), the internal ground pads are not connected directly to the encapsulation ground pins. Instead of that, the ground is shared and all the pads and pins are connected to the central pad. Both analog and digital grounds were separated at layout level, but are connected together in order to have a good global grounding following the LHCb detector approach [45].

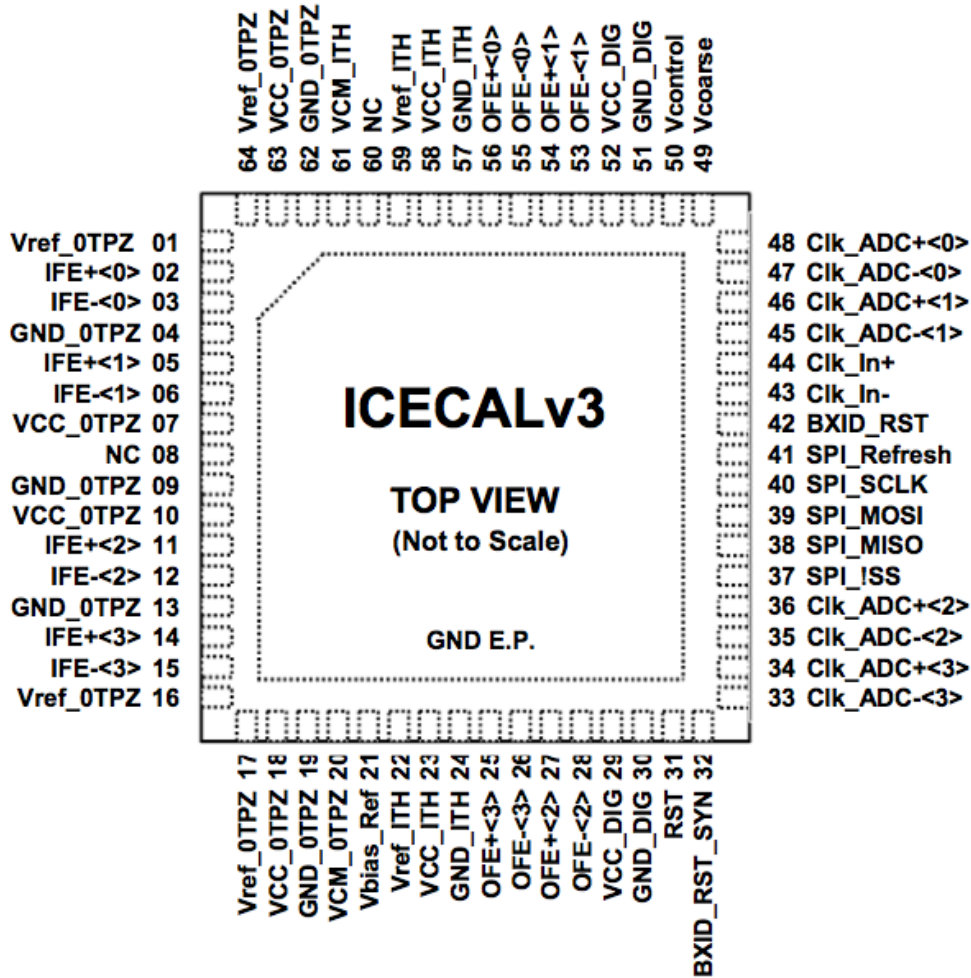


Figure 5.3 – ICECALv3 pin configuration.

- **Reference voltage** pins (1, 16, 17, 22, 59, and 64) have been doubled to reduce the parasitic inductance of the reference voltage at the input preamplifier.
- **Analog voltage** (7, 10, 18, 23, 58 and 63) and **digital voltage** (29 and 52) sources are doubled on top and bottom sides.
- Digital I/Os:
 - **Reset** signals, including chip reset (31) and Bunch crossing reset input (42) and output (32) Are separated from the rest.

- **DLL control** connections (49, 50) are the coarse input and control output.
- **LVDS clock** input (43 and 44) and outputs (33-36 and 45-48) are on the right side to facilitate the connection to ADCs.
- **SPI** signals (37 to 41) are also on the right side, next to the digital region of the layout.

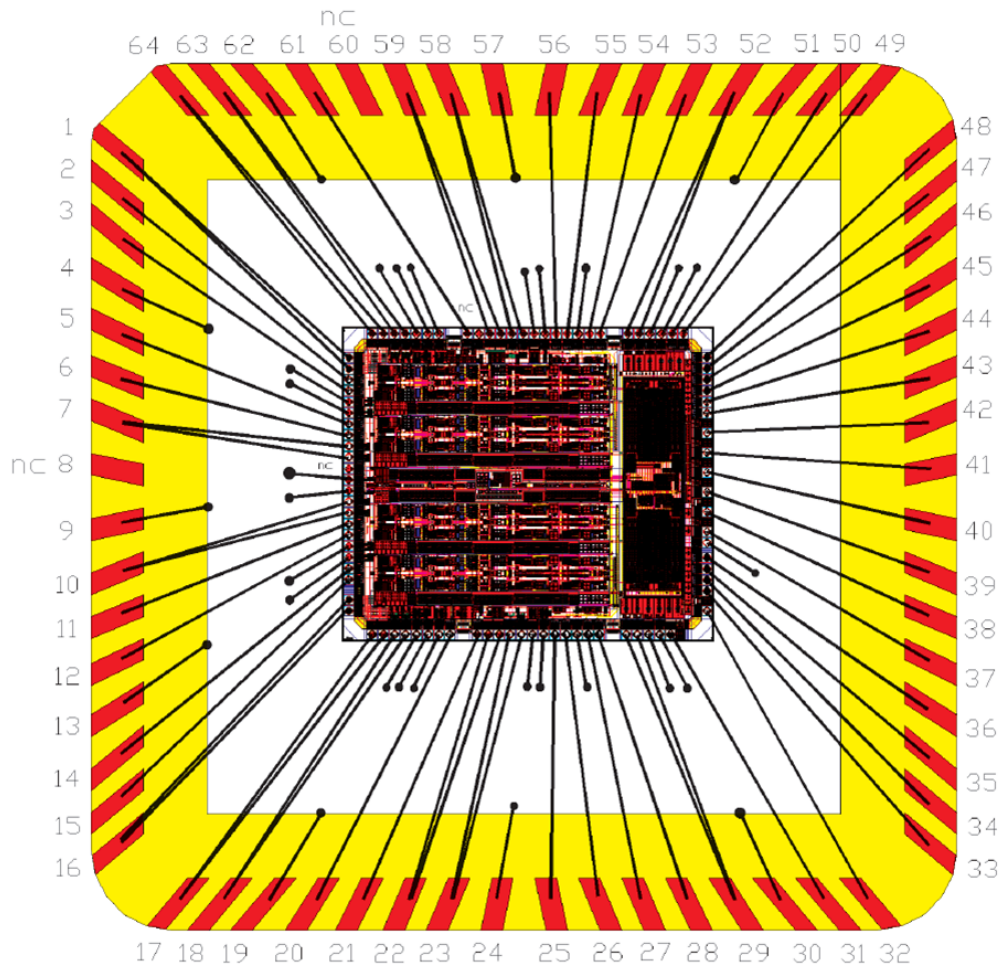


Figure 5.4 – ICECALv3 bonding diagram.

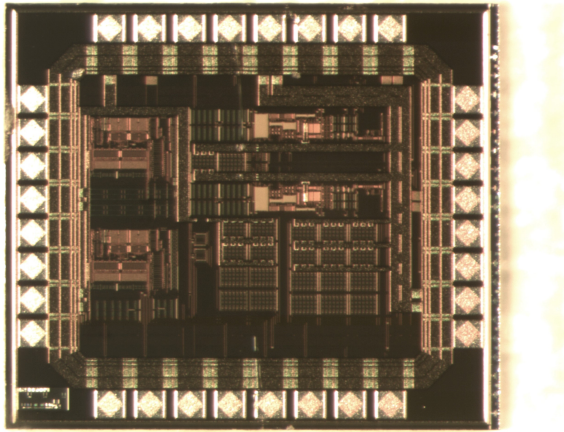


Figure 5.5 – ICECALv1 chip photograph.

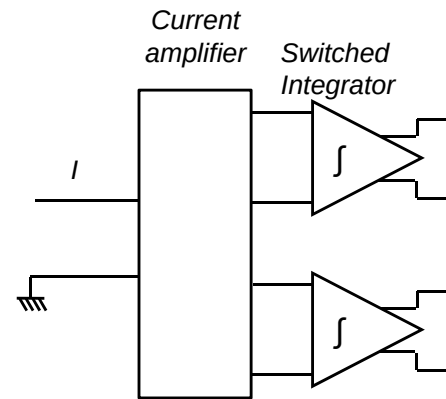


Figure 5.6 – ICECALv1 schematic.

5.3 Test stages and prototypes

Three prototypes of the chip have been designed in Austriamicrosystems 0.35 μm SiGe BiCMOS technology. The last, and definitive, was received in July 2014 (Fig. 5.9). The main purpose for the prototypes was to test the key points of the circuit. Even more, a dedicated DLL prototype was made to check the characteristics of that circuit before a fully functional chip including the analog channel and the digital parts would be done.

5.3.1 ICECALv1

The first prototype, the ICECALv1 (Fig. 5.5), included one channel with the basic stages: the current preamplifier and the switched integrators (Fig. 5.6). It was enclosed in QFN 32 package. The objective was to prove the general design and test the crucial points of the circuit:

- Input impedance control by current feedback.
- Noise performance.
- Dynamic range: Linearity.
- Offset between sub-channels.
- Effect of the clock jitter versus signal.

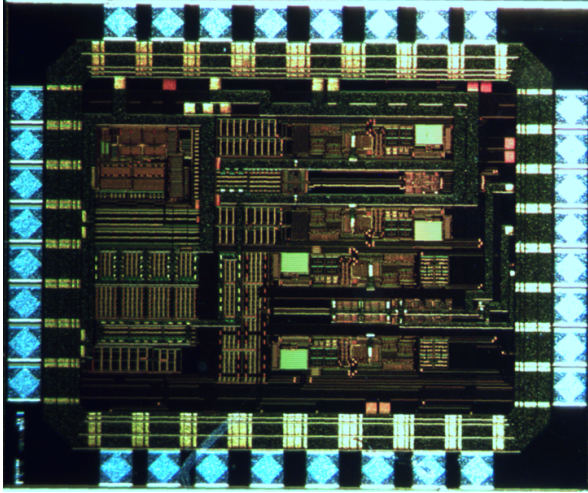


Figure 5.7 – ICECALv2 chip photograph.

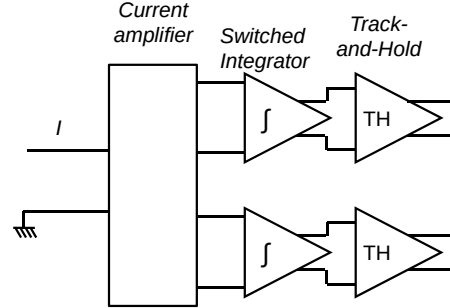


Figure 5.8 – ICECALv2 schematic.

5.3.2 ICECALv2

In order to test the complete analog signal processing, the Track-and-Hold block was added to each interleaved path in the second prototype 5.8. Also, a resistor in parallel to the integration capacitor showed in simulations a better plateau and lower spill over. As in the previous prototype, the main features of the circuit were tested (input impedance, noise, linearity, offset between sub-channels). Moreover, dedicated studies of the plateau and spill over behavior of the circuit were carried out.

The second prototype included two differences respect the ICECALv1 (Fig. 5.8 and Fig. 5.7):

- A Track-and-Hold to help understand the effect of the jitter respect to the signal.
- A feedback resistor in the integrator to improve the plateau.

5.3.3 ICECALv3

The final prototype 5.10 includes four analog channels, a Delay Locked Loop (DLL) for signal phase synchronization for all channels and an SPI communication protocol based interface. It also adds the final analog channel stages with programmable parameters (especially useful for the shaping, gain, noise and linearity). The included DLL is capable of shifting the phase of the LHC clock (25 ns) in steps of 1 ns.

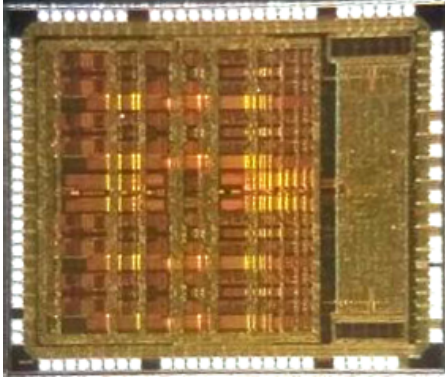


Figure 5.9 – ICECALv3 chip photograph.

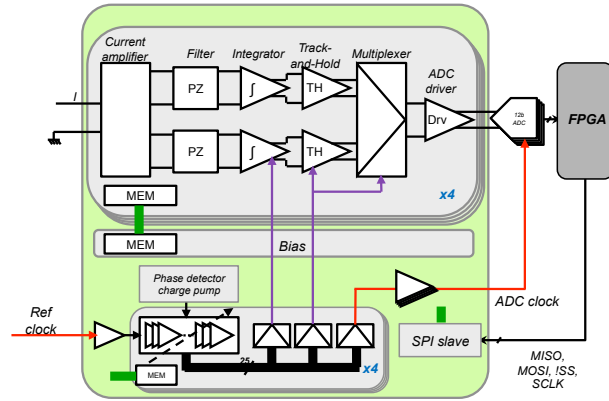


Figure 5.10 – ICECALv3 schematic.

5.3.4 Delay chip prototype

Just before the design of the final ICECAL ASIC, another chip prototype was designed and fabricated to check the implementation of a SPI-programmable clock delay based on a Delay Locked Loop (DLL). The objective of the DLL was to shift the phase of the LHC clock (25 ns) in steps of 1ns, with less than 5 ps jitter and 23 ps of DNL. The delay lines chip was intended to be integrated into ICECAL. This 5.7 mm² chip was been implemented in the same technology as the ICECAL.

The DLL2013 was designed to be integrated afterwards into the ICECAL chip, it included 4 channels, each one with a set of clock outputs to be sent to the correspondent integrator, TH and ADC. The clocks enable the user to configure delays in steps of 1 ns, between 0 and 24 ns, being 25 ns the clock period. An SPI interface allows for reading and or writing the serial registers of DLL channels. It also enables the user to reset charge pumps by software.

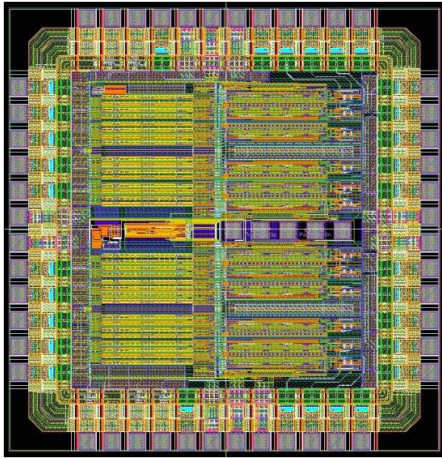


Figure 5.11 – DLL2013 ASIC prototype layout.

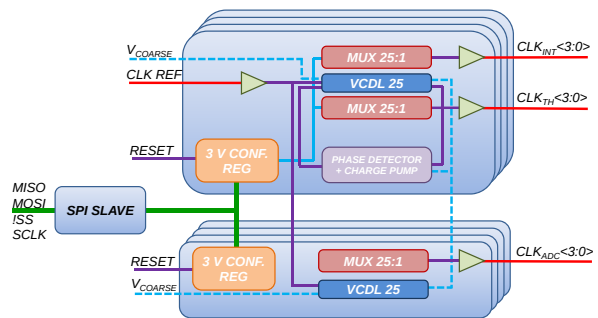


Figure 5.12 – DLL2013 ASIC schematic.

The purpose of the tests performed at the laboratory was to check all the requirements as proposed in table 2.1. The key points of the tests include: the input impedance control by current feedback, the noise performance, the dynamic range and linearity. Also, it is necessary to test the critical aspects of a switched solution: offset between sub-channels, plateau and spill over of the integrator output.

6.1 Main test set-up

During the process of checking the key points of the circuit implemented in the ICECAL, three different prototypes (plus a DLL prototype) have been designed and checked with their specific setups [5] [33] [32]. For simplification of the document, we will only comment on the last and most complete setup for test, unless otherwise noted.

The test setup is based in a FE board prototype with connectors to a chip dedicated mezzanine and USB to PC communication port. All the data acquisition process is controlled by the means of the FE FPGA and the custom software. The signal is replicated from the test beam measurements by an arbitrary function generator synchronized and triggered by the FE prototype. Fig. 6.1 shows the setup scheme: the analog mezzanine (where the ASIC is placed), the waveform generator and a PC to control the data acquisition.

One of the challenges of the detector is to synchronize the data acquisition at the different electronic levels. This is also true inside the FE prototype. First, the clock input to the chip has to be adjusted in order to capture correctly the sub-channel reset. Second, as commented before, the signal has to be integrated at different times for different channels due to PMT high voltage and signal cable length differences, which is taken care by a dedicated internal phase. Third, the sampling time of the ADC will vary due to the board design and the integration

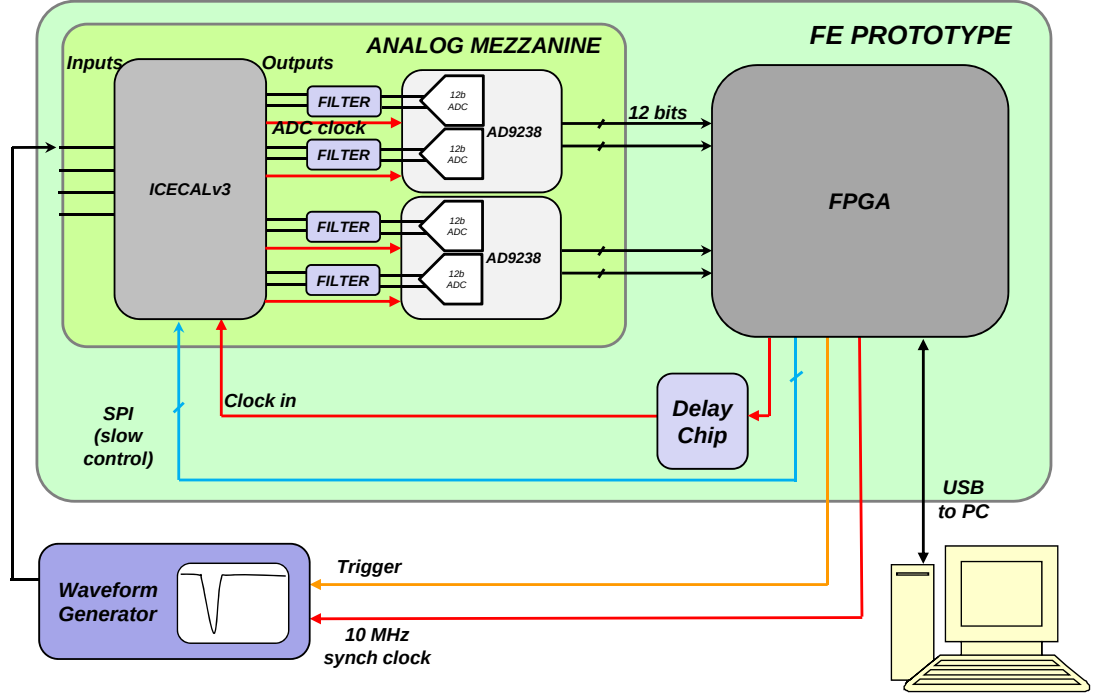


Figure 6.1 – Scheme of the test setup used at the lab to test the ICECALv3 chip.

time. And fourth, the FPGA will capture the data from the ADC. A dedicated software script ensures, step by step, that all synchronization levels are fulfilled.

6.1.1 Front End Prototype

A first prototype of the Front-end board has been designed and is used to:

- test the capabilities of the candidate FPGA (A3PE from ACTEL) for our design,
- acquire the data from the analog part in order to test in realistic conditions the functioning of a front-end block,
- test the radiation tolerance of the components and of the firmware in particle beam.

The prototype has been successfully used with the analog part either on test benches (several boards have been fabricated and have been used in Barcelona and Orsay with the FPGA firmware) and also during test beam tests. A picture of

the Front End prototype is displayed in Fig. 6.2: the analog mezzanine is visible on the left, the power regulators are on the bottom right, the phasers are at the top left and the SPECS mezzanine is on the top right. The 2 FPGA (models A3PE and AX from ACTEL) are situated in the central part of the board. The prototype

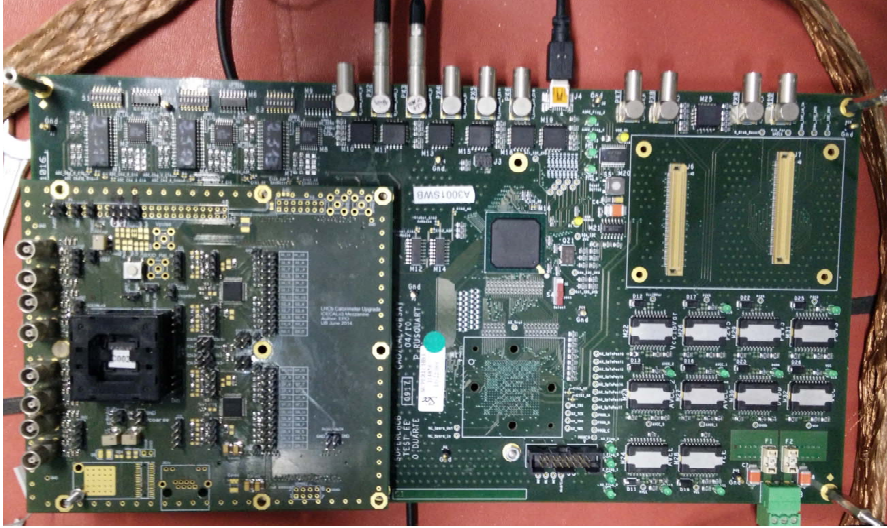


Figure 6.2 – Picture of the prototype of the Front-end board.

includes several regulators for powering and delay chips in order to perform all the necessary time adjustments. The acquisition can be done either through a USB interface or SPECS (to be used essentially during radiation tolerance tests). Two FPGA are located on the PCB: a A3PE and a AX FPGA from ACTEL.

6.1.2 Analog mezzanine

The FE prototype is designed in order to connect an analog mezzanine which allows the test of different solutions, whether they are different boards for the corresponding ASIC versions or the COTS solution. The analog mezzanine used for testing the ICECALv3 was designed to allow the direct measurement at each step of the circuit of:

- Analog signal: inputs, outputs of the ICECAL and input of the ADC.
- Digitized ADC outputs
- Clock signals: board differential input clock, ICECAL differential input and output clocks and ADC single ended input clocks
- Voltage supplies, bias, reference voltage and common mode input.

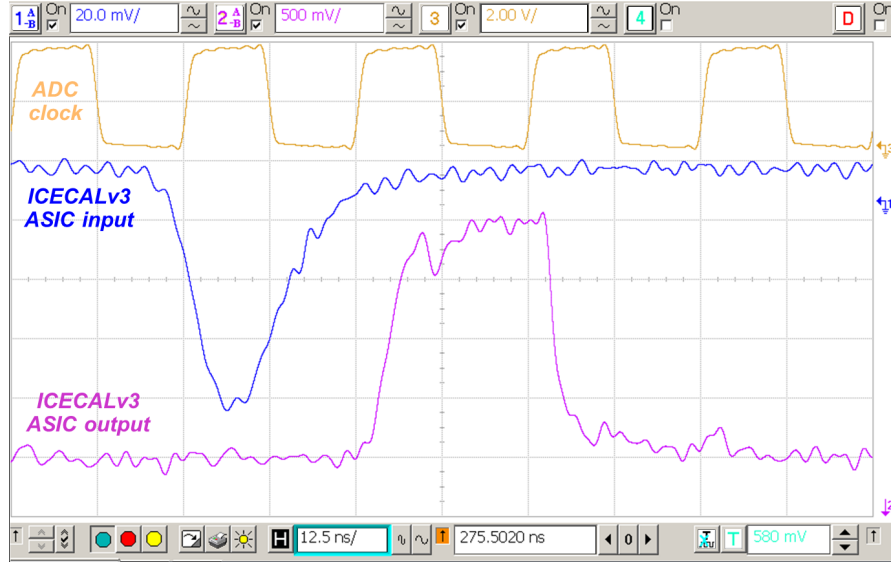


Figure 6.3 – Oscillogram with input and output signals.

6.2 Delay line measurements

Experimental results showed that the operating range of 14.3 to 28.6 ns, wide enough to ensure that systematic process or environmental variations will not prevent working properly with the LHC clock.

Differential Non Linearity (DNL) was measured in a previous chip prototype [7]. Linearity was measured by sweeping the 25 possible phases of each delay line, and performing delta time measurements between a fixed reference and each clock output. In the absence of process variations each stage is expected to have a delay of 1 ns. DNL is defined as the difference between the expected delay and the measured delay.

$$DNL_i = \text{abs}(\text{Delay}_i - \text{Delay}_{i-1} - 10^{-9}) \quad (6.1)$$

Figure 6.4 shows the DNL distribution of the whole delay element population (7200 samples distributed into 25 prototype chips with 12 delay lines of 24 stage-to-stage delta time measurements) and its gaussian fit. Measured σ_{DNL} is 23 ps.

VCDL RMS jitter (Fig. 6.5) was also measured and it was reported to be lower than the oscilloscope resolution (5 ps).

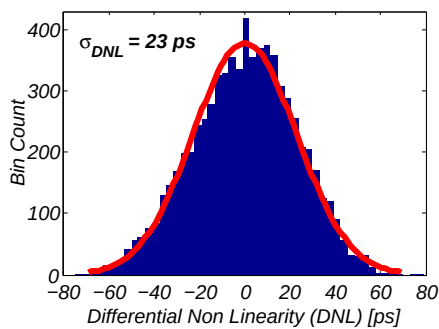


Figure 6.4 – Delay line DNL Histogram

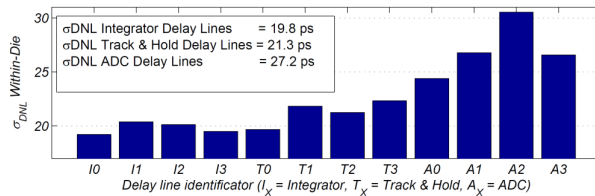


Figure 6.5 – Delay line output clock DNL measurements (within-die).

6.3 Analog channel results and characterization

6.3.1 Test system clock synchronization

The synchronization in prototype comprises the same steps that will be needed in the final Front End electronics, although the procedure to set the different DLL phases can be fundamentally different. In the detector, the whole front-end electronics system must be perfectly synchronized to the bunch collisions of the LHC machine to capture correctly the signals from the different detector elements. A complicated system with different delays for each channel to compensate for differences in photomultiplier tube biasing voltages, different cable lengths and fibers, must be aligned to each other, using timing parameters extracted during special calibration runs of the system.

Fig.6.6 depicts the different phases to be adjusted in the test setup:

1. Clock in: modify the input that feeds the ICECALv3 so that the sub-channel reset (*SubChRst*, pin 42) is captured correctly. As explained in section 4.2, the sub-channel reset is designed to only proceed for the phases that allow a predictable effect. That is, to have always the same sub-channel bunch-crossing (BXID) parity for a fixed phase of clock and reset. Once fixed, it is possible to apply any gain or offset calibration within a channel. It depends on the relative phases between the input clock and the reset signal generated at the FPGA. The method to fix the clock phase is to perform a scan and check the reset has been done in the *BXIDRST_SYN* pin (32).
2. Integrator and TH clock: the objective is to fit all the signal (up to the 1% level). It is achieved maximizing the integrator output. The two phases are treated together because the optimal phase between the integrator and the TH is fixed by the chip design, it does not depend on external factors.

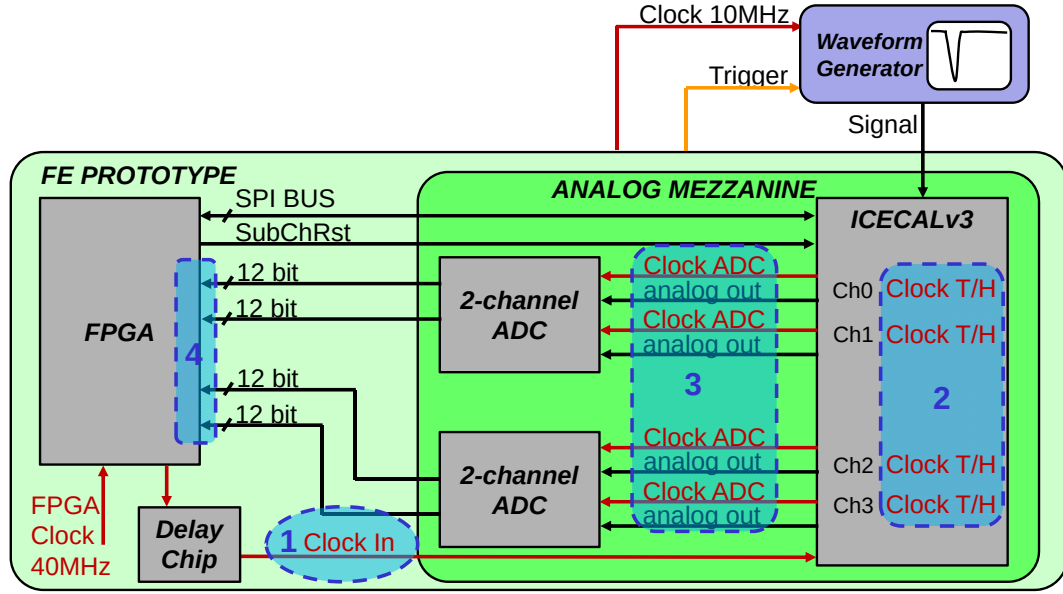


Figure 6.6 – Test setup synchronization steps.

Therefore, in the corresponding scan of phases the integrator and TH phases change in parallel.

3. **ADC clock:** The ADC clock phase allows to synchronize the digitization at the FPGA and TH output. It depends essentially in the FE board routing. The time margin in which the signal is stable at the ADC input for each clock cycle depends on the output impedance for each signal output of the chip and the load effective capacitor at the ADC input. Measurements show that there are about 9-10ns with the TH output signal stable enough to help in the next synchronization stage.
4. **Data capture at the FPGA:** It is still possible to adjust the FPGA parameters in order to modify the phase to ensure a correct capture of the 12 bits coming from each ADC output.

Once all the synchronization steps are done and the signal is both reliable and the digital information is transmitted correctly it is possible to proceed with the measurements.

6.3.2 Input impedance

An input impedance study was performed by measuring the input and output signals. The input was measured at the generator and after 10m cable at the chip input (Fig. 6.7). If the input impedance Z_{in} is 50Ω , the reflections should be minimal. Otherwise, if, for example the chip is off, the input termination is not adapted and large reflections appear (Fig. 6.7 right). We define the reflection coefficients, γ for source, IC input, and output signals as:

$$\gamma = \frac{\text{1st pulse integral}}{\text{2nd pulse integral}} \quad (6.2)$$

As defined in Fig. 6.7 (left) and in the schematic on Fig. 6.8, there will be a coefficient for each signal measurement. The first signal pulse ($A1$) is captured at the output of the waveform generator and shows a first reflection ($A2$). The second signal is measured at the ASIC input (after 12m cable) with the reflection ($B2$), which has an effect on the output ($C2$). In the measurements setup, the PCB input circuit with AC coupling includes an adjustable resistor R_p that helps to fine tune the input impedance (simulations of ICECALv1 showed a Z_{in} a little higher than 50Ω). The optimal R_p is between 360 and 390Ω . The dynamic variation of input impedance (Fig. 6.9) is below the 0.5% for full dynamics (50 pC), proving that the 2 loops of the 0T amplifier operate quite linearly for the whole dynamic range. The measurement error for the second reflection is quite high for low amplitudes due to the differential probe noise and low signal.

Input impedance for different configurations was measured (figure 6.10) with a network analyzer at the input (Rohde&Schwarz ZVL) with approximate results due to parasitics influence. Ranging approximately from 40 to 60Ω , the optimum termination impedance corresponds to 14 DAC counts.

6.3.3 Offset

Offset between channels is below 5% of the full range for each subchannel. But the relevant value is the difference between subchannels, which is below 2%.

6.3.4 Crosstalk

Crosstalk between channels is below 0.5% for all the output range. In the example of the figure 6.11 the crosstalk is well below the limit defined. The relative error in the measure for low output values is much higher than the crosstalk value itself.

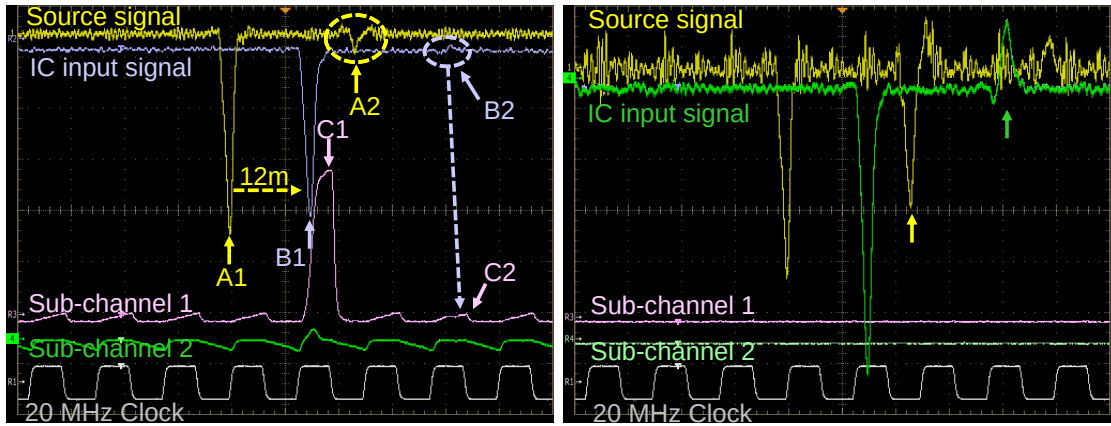


Figure 6.7 – Oscillogram with input and output signals of the ICECALv2 with the chip ON (left) and chip OFF (right).

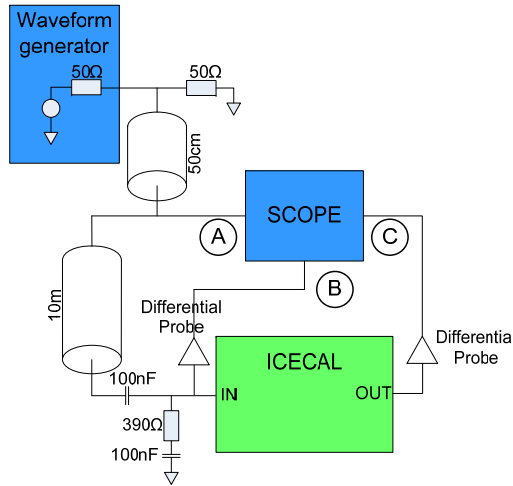


Figure 6.8 – Reflection coefficients measurements setup.

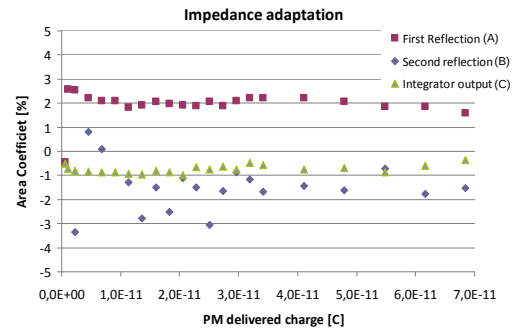


Figure 6.9 – Reflection coefficient at the input (first reflection measured at the pulse generator output) and at the integrator output (after second reflection).

6.3.5 Sensitivity

As presented in table 2.1, the expected sensitivity (inverse of gain) is 4.5fC/LSB. It is possible to adjust the channel gain through the integrator capacitor. The results for all channels are plotted in the histogram in figure 6.12 leading to a mean value of 4.488 ± 0.051 fC/LSB. The standard deviation of the value is lower than 2.5%.

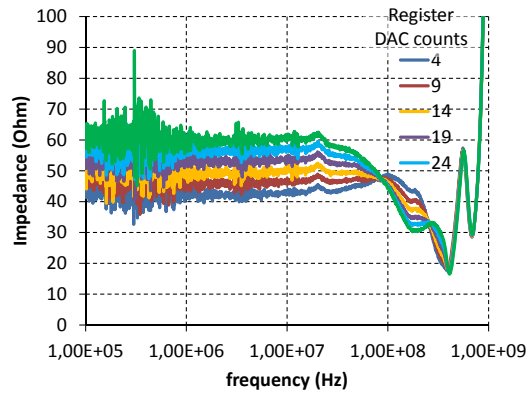


Figure 6.10 – Input impedance for different programmed values (5 bits).

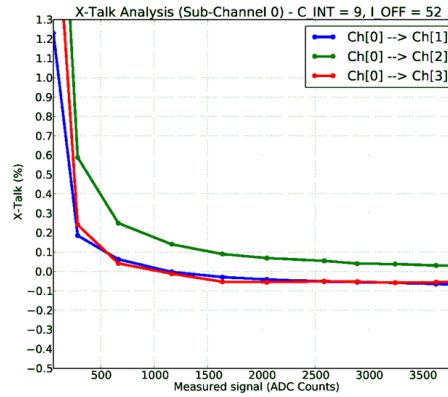


Figure 6.11 – Crosstalk measure.

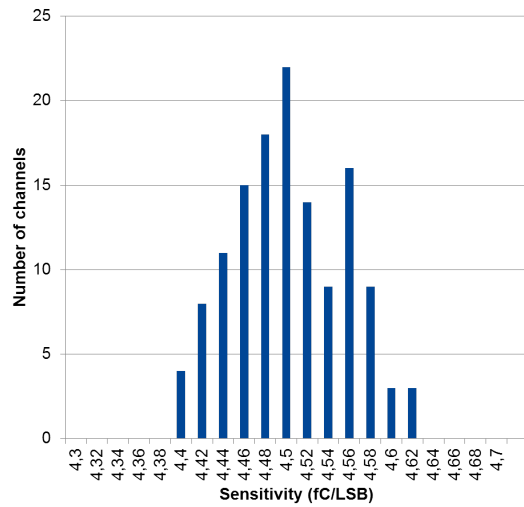


Figure 6.12 – Sensitivity histogram of all channels.

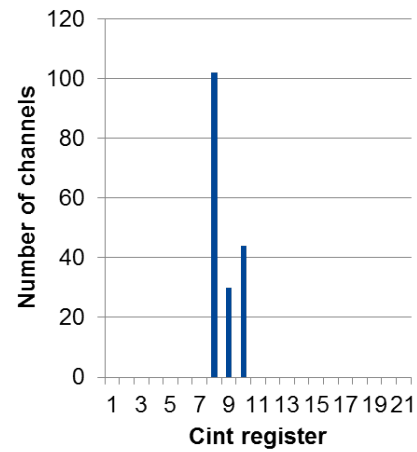


Figure 6.13 – Optimum integrator capacitor values.

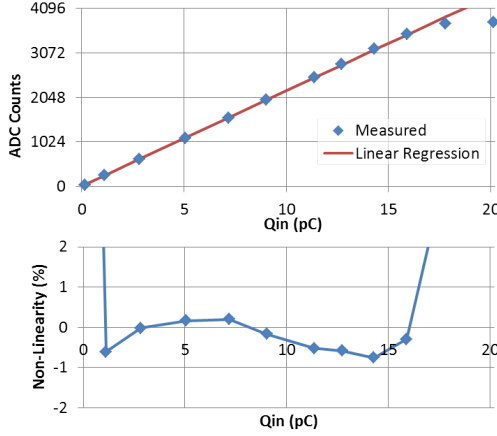


Figure 6.14 – Non-linearity as a function of the input charge.

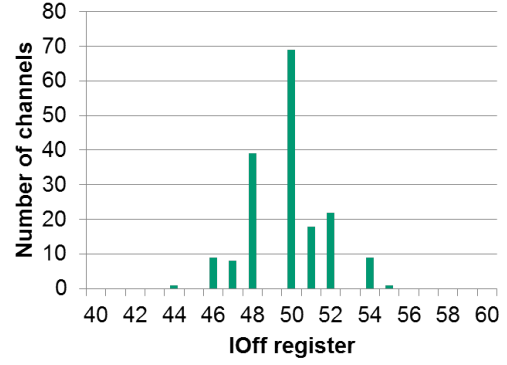


Figure 6.15 – Optimum differential DC current offset register values.

6.3.6 Linearity

Non-linearity has been checked to be $< 1\%$ for the full output range (figure 6.14). Using the offset stage, designed to add controllable offset levels to the positive and negative pins, it is possible to avoid a limit on the excursion of the Track-and-Hold stage which affects linearity for the higher signal levels. Linearity measurements at low signal values are affected by a large relative error due to the measurements setup noise. The offset current value (Fig. 6.15) is adjusted as the minimum offset with correct linearity in order to reduce any effects in the noise performance.

6.3.7 Spill over

Other important checks include the spill over. In order to have all the signal inside the 25 ns time window, a clipping is added at the PMT base. But, as the long cable to the FE widens the signal pulse, the pole zero stage is adjusted to minimize the output in the previous and next clock cycles, as shown in figure 6.16. As specified, the spill over is less than 1%, except for the second next clock cycle, which can be up to 2% in some cases (Fig. 6.17).

6.3.8 Plateau

As commented in section 3.5, the ASIC is expected to integrate signals from particles arriving with at different times ($\pm 2ns$) without varying the output more than 1%. This plateau is also affected by the values of the pole and zero. An example

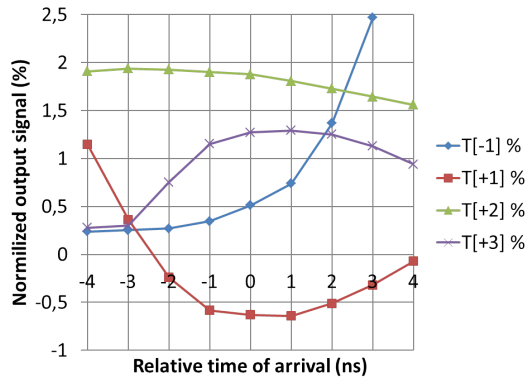


Figure 6.16 – Spill over in the previous and next clock cycles.

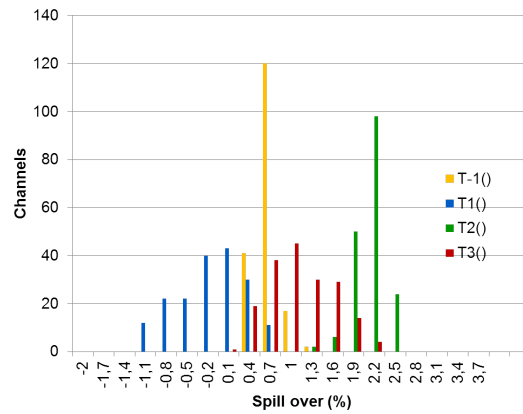


Figure 6.17 – Spill over values for all ASICs and channels measured.

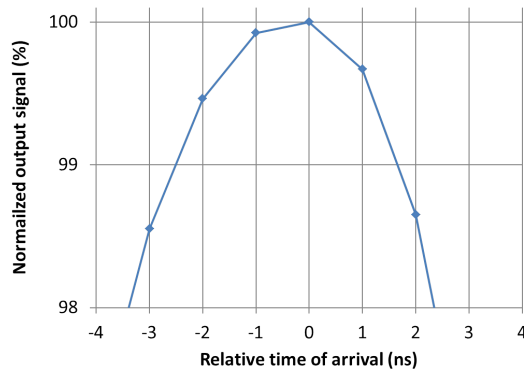


Figure 6.18 – Plateau.

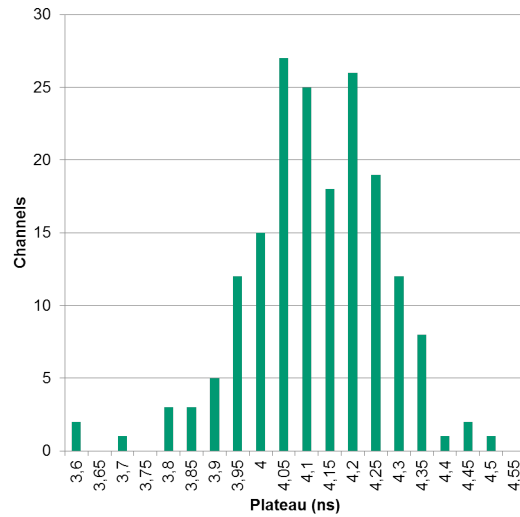


Figure 6.19 – All plateau measurements.

of the plateau is shown in figure 6.18. Most of the plateau values are over 4ns wide except for a few (less than 10% of the total) which are always more than 3.8ns (Fig. 6.19). The results in plateau and spill over are a trade-off; obtaining better results in one implies a worsening on the other.

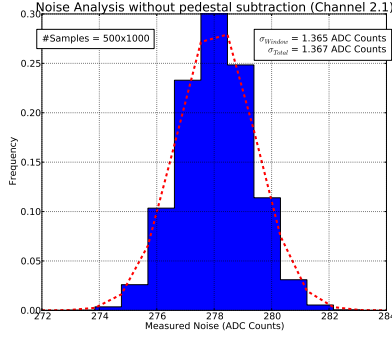


Figure 6.20 – Noise example from a channel.

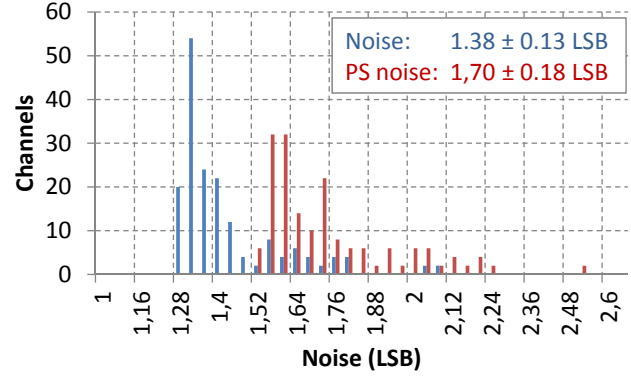


Figure 6.21 – All noise measurements before and after pedestal subtraction.

6.3.9 Noise

The output noise of the ASIC depends of the configuration of the different parameters, mainly gain, offset and pole-zero. With the optimal configuration found during the tests, the noise is in average 1.38 ± 0.13 ADC counts and 1.70 ± 0.18 ADC counts with pedestal subtraction (Fig. 6.21). The specification states that it should be not greater than 1 ADC count. But this condition can be relaxed, as the noise should be less than the 5 ADC counts expected for the pile up noise.

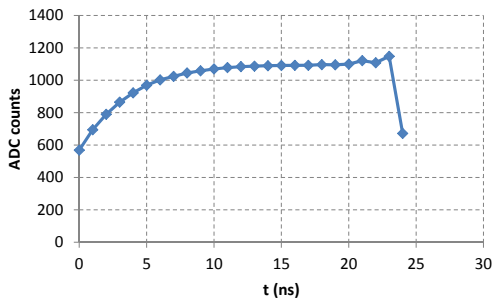
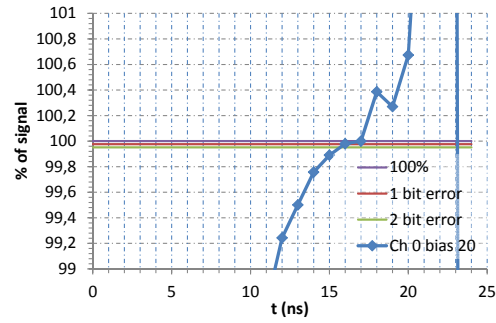
The voltage sources of the chip will be generated at the front-end with a specific DC-DC converter developed at CERN. It is designed to add very low noise [46] and to perform similarly to the linear regulators included in the present detector electronics. The front-end prototype was designed with the linear regulators instead of the DC-DC converters due to their non-availability. Dedicated circuitry in the analog mezzanine made possible to attach a DC-DC converter for testing with the final voltage source. Particularly, noise measurements on the ICECALv2 showed similar results with linear regulators and DC-DC converters. Table 6.1 shows the results in LSB. The noise was measured as an rms value at an oscilloscope and the last column is the corrected value, which is the noise multiplied by a correcting factor due to the fact that the gain was lower than the specification.

6.3.10 ADC interface and output impedance

In order to settle to within 1 LSB for a varying input signal at the input of the ADC, it is necessary to consider the capacitance of the network (strays, aliasing capacitor and ADC equivalent input capacitance, etc.) and the output impedance of the driver. In the case of the ADC's switched Track-And-Hold, the system can be modeled as a simple RC circuit where the we take into account the chip

Table 6.1 – ICECALv2 noise measurements with linear regulator and with DC-DC converter.

Conditions	Channel	Pedestal (Subtraction)	Noise (LSB)	Corrected Noise (LSB)
Chip #6 + DC-DC	2	No	0.9531	1.506
Chip #6 + DC-DC	3	No	0.9562	1.511
Chip #6 + DC-DC	2	Yes	1.148	1.814
Chip #6 + DC-DC	3	Yes	1.132	1.789
Chip #7 + linear reg	2	No	0.9061	1.411
Chip #7 + linear reg	3	No	0.8806	1.372
Chip #7 + linear reg	2	Yes	1.133	1.765
Chip #7 + linear reg	3	Yes	1.105	1.721

**Figure 6.22** – Measured ADC input/ICECAL output signal.**Figure 6.23** – TH error at the ICECAL output/ADC input.

output impedance and the ADC capacitance (in parallel with all the parasitic ones). Then, the voltage at the ADC input when a pulse with a final voltage V_0 is $V(t) = (1 - e^{-t/RC})$. If the maximum error is 1 bit, the input needs to settle to within .024% of full scale (12 bits) before conversion is complete. This is about 8.3 time constants for a driver with linear, time independent, output impedance.

Supposing that the total input capacitance is 10 pF equivalent and the sampling speed is 25 ns the (simplistic) output impedance of the driving buffer should be 300 Ω . A first analysis was performed using simulations of the output buffer which showed that the output impedance varied from 290 to 450 Ω depending on the bias current.

Moreover, measurements on the test setup board were performed with different bias values. Fit time constant is approximately 3.7 ns, which corresponds to an output impedance of about 370 Ω if we suppose that there is only the 10 pF capacitor, with no other parasitic capacitor.

If we calculate the amount of signal and compare to the limit (zooming the plot) it is possible to see that the output is stable for the last two points (1ns) varying less than the 1 bit error (Figs [6.22](#) and [6.23](#)).

There is a trade-off between the noise level and the output precision due to the value of the filter capacitor: the larger the capacitor, more noise is filtered but the larger the time constant is and, therefore, the lower the precision at the ADC input.

Test beam

Several test beams have served to check the ICECAL chip in more realistic conditions. The beam line T4-H8 at CERN Preveessin was used. An ECAL module equipped with aphotomultiplier tubes and their bases generated the signal from electrons ranging from 20 to 120 GeV. The signal was triggered using two scintillators and sent to the FEB prototype and, in parallel, to a Lecroy integrator and a Time-to-Digital Converter (TDC) in the barracks (see picture [7.1](#)).

The first test beam was carried out with the second version of the design in November 2012. The ASIC prototype only included one analog channel with just the input preamplifier, the switched integrator and the Track-and-Hold (Fig. [5.8](#)). Even though the laboratory results had been positive, both the results of the measurements and the signal obtained with a scope showed that the circuit was not completely prepared to fulfill the plateau and spill over requirements.

Two test beams followed in June and November 2015. The tests were performed with the last version of the chip at the same beam line, using the same setup. The objective of these tests were to validate the performance of the chip, specially to check the plateau and the spill over. Obviously, other important parameters like the linearity and noise were included in the studies. The following sections refer to the definitive design unless otherwise noted.

7.1 Test beam setup

In order to perform the envisaged tests of noise, resolution, linearity, spill over, and integrator plateau, it was required a reference both in time and for linearity. Therefore, the experimental setup (Fig. [7.1](#)) included two parallel measurements of the signal of the PMT:

- Measurement from the electronics prototype (with fast integration over 25

ns).

- A Lecroy ADC for an independent measurement for calibration (with integration over a long time range which results independent of the particle time arrival).
- An *adapted* "T" replicates the signal for the two DAQ branches. It increases the noise, so it would be retired (along with the Lecroy ADC) for the noise measurements.

The trigger of the system is generated from two scintillators in the beam line in NIM module which checks for coincidence. Then, other NIM modules implement the logic used to discard triggers if one of the two parallel data acquisition systems is busy processing a previous acquisition.

The data is stored in the corresponding PCs for each of the two DAQ systems. Afterwards, when the run is finished, it is merged and analyzed.

During the test beam the particles used were electrons ranging from 20 to 120 GeV offering the possibility to check the effects of different signal amplitudes, particularly useful on the measurement of linearity, plateau, spill over, resolution and in the timing on the shower integration.

A TDC was also needed to correlate each individual event time with the prototype outputs, which compared the 20 MHz clock to the trigger.

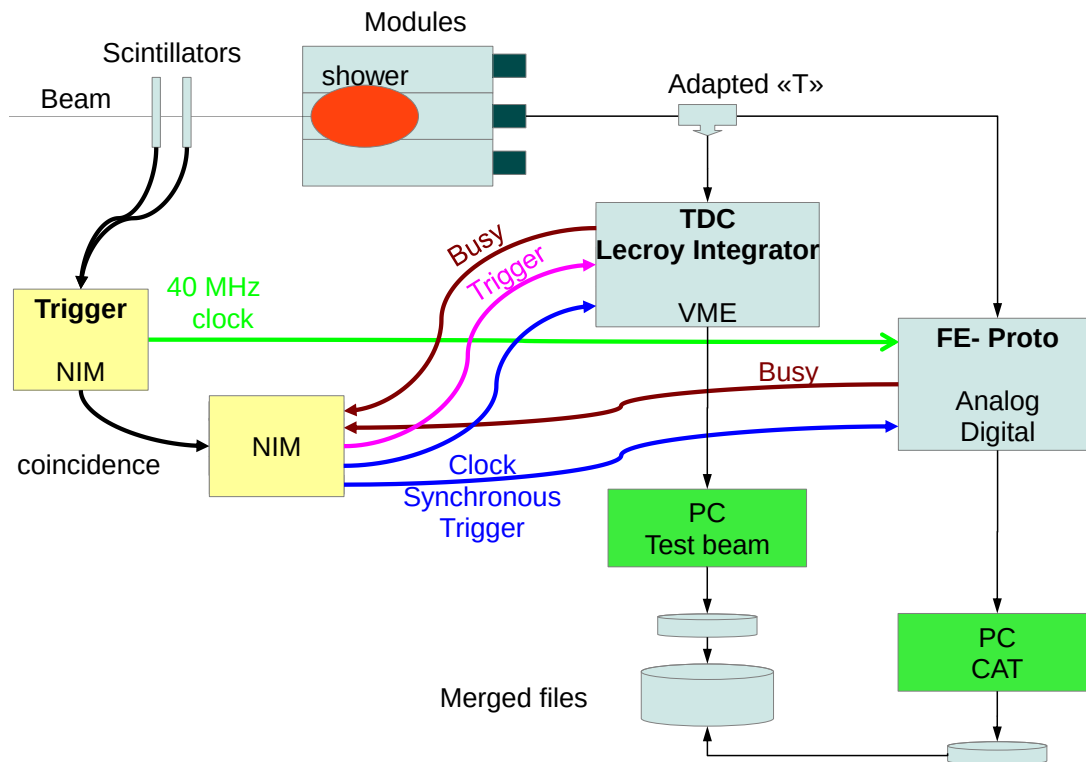
7.2 Purity of the electron beam

For testing purposes is crucial to work with particles of the same type and same known energy. An electron beam was obtained by inserting a lead target into the beamline. The magnetic optics following the converter again selected particles of equal energy. The optics was optimised for particles with production point at the plate, but still the electron beam had a pion contamination greater than 60% (Fig. 7.2). The initial target was a lead plate of 6mm deep, but it was changed to another one of 12mm which improved the electron purity. Increasing the energy of the beam, decreased the purity and made difficult to analyze the data (for further details, check section 7.3.4).

7.3 Tests beam results

7.3.1 Noise

The noise was checked in four different conditions: with and without the adapted "T" and with and without clipping. The specification states that the noise should



be of about 1 ADC count. The measurements at the lab prove it at 1.4 and 1.7 ADC counts with direct analysis and after pedestal subtraction, respectively.

In the three test beams, the noise behavior of the system was not the same; while in November 2012 the measured noise was 1.6 ADC, its amount increased in June and November 2015 to 2.7 and 3.4 ADC counts, respectively. These results are plotted in 7.3 and 7.4. The signal has low frequency noise that is reduced by a pedestal dynamic subtraction (subtract the lower of the two previous samples to the signal).

If we compare the noise between channels (Fig. 7.5), the noise it is not correlated. Also, the noise was quantified in different configurations and the PMT bias voltage generation was part of the source. These discrepancies in the measurements are probably the outcome of the changes in the setup between the tests, as the ASIC is sensible to any noise introduced by the ground of the system. Therefore, a good compromise and more realistic check was to measure it at the detector itself, connecting to a channel at the crates level and a copper braid to local ground.

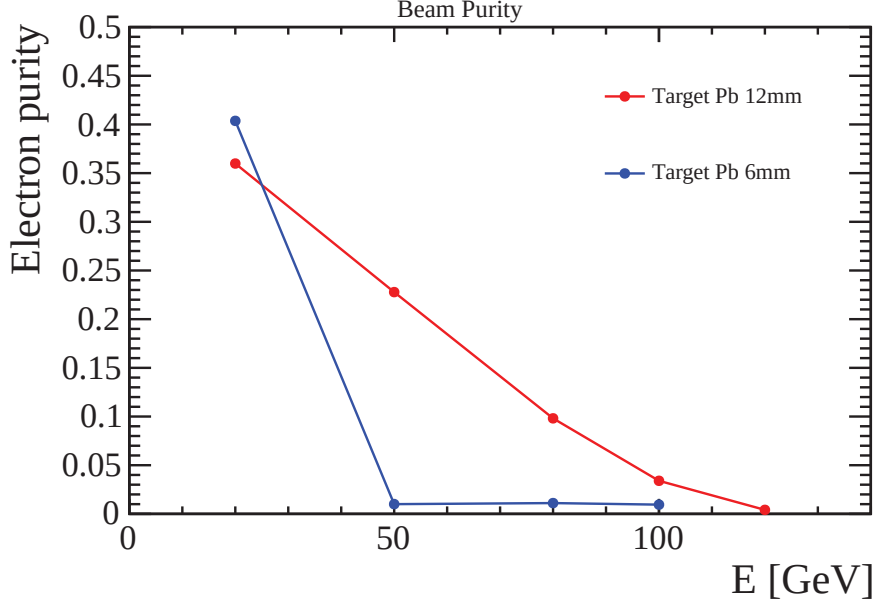


Figure 7.2 – Beam electron purity.

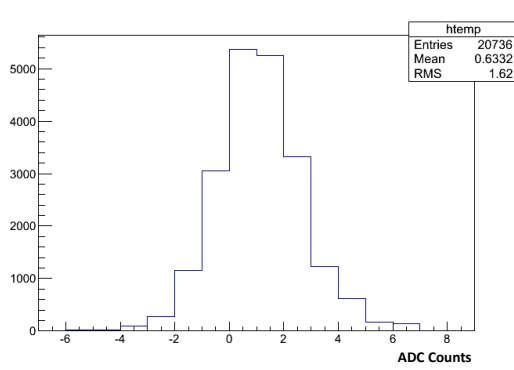


Figure 7.3 – ASIC electronics noise after pedestal dynamic subtraction in November 2012 test beam.

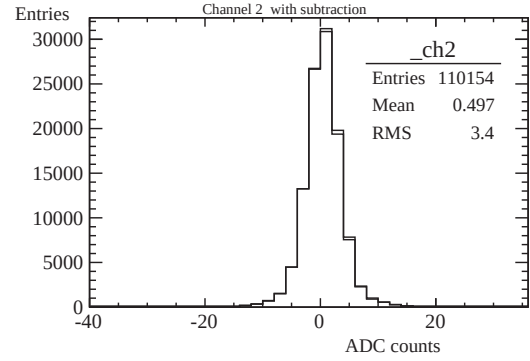


Figure 7.4 – ASIC electronics noise after pedestal dynamic subtraction in November 2015 test beam.

7.3.2 Noise at the detector

The analog channel is sensitive to noise at ground. The different measurements at the laboratory and at the test beam area offer different grounds compared to the detector. A good approximation of the final noise was to connect the prototype FE (with its analog mezzanine and ICECAL) to an actual detector channel cable and crate ground. The cable was connected to the mezzanine input with an adaptor

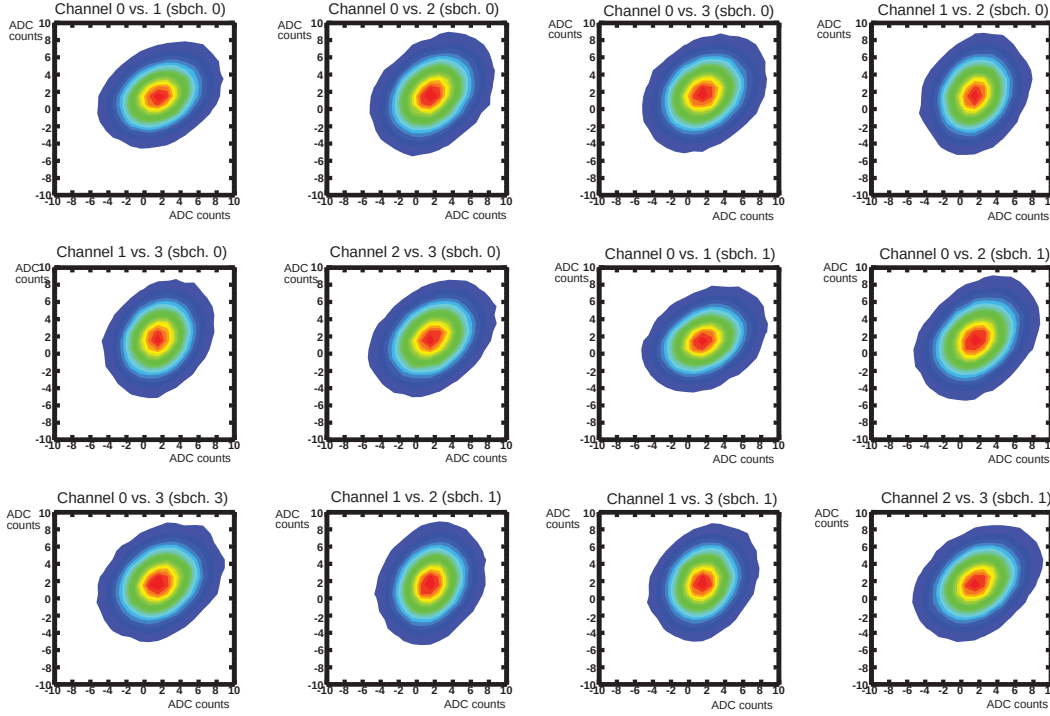


Figure 7.5 – Noise correlation study between channels.

to LEMO and the ground with a 2 cm wide copper braid.

Table 7.1 summarizes the noise measurements. Then, measurements were done for 10 ECAL and 4 HCAL channels. The typical and worst cases are presented. Observing the table, the main conclusions are:

- At first, the noise of the prototype by itself is 1.3 and 1.6 ADC counts with pedestal subtraction (PS) for the prototype itself. Connecting the ground did not modify the results. Then, once the channels are connected, the noise added by the cable and the PM bias is about 1 ADC count after pedestal subtraction.
- The effect of the PM biasing voltage, which determines the gain, is not very important after pedestal subtraction because it affects mainly for low frequencies. The difference between upgraded and present PM biasing conditions can be observed for ECAL channel 200904. Obviously, the effect on the signal-to-noise ratio is still a factor five. The rest of the measurements were done with present PM voltage for practical reasons.
- In the ECAL channels the noise without pedestal subtraction is more than

two times the one after applying the correction. Probably there is an important effect of the low frequency noise from the PM biasing sources. On the contrary, the HCAL channels present a similar amount of noise with and without pedestal subtraction, which implies that the noise induced by the PM voltage sources is relatively low.

Table 7.1 – ICECALv2 noise measurements at the detector.

Detector	Channel	PM Biasing	Copper Braid	Noise (LSB)	PS Noise (LSB)
Not connected			No	1.32	1.59
Not connected			Yes	1.34	1.61
ECAL	200904	Upgrade	Yes	5.83	2.63
ECAL	200904	Present	Yes	6.22	2.69
ECAL	210100	Present	Yes	7.14	2.91
HCAL	251726	Present	Yes	2.25	2.20
HCAL	240609	Present	Yes	3.28	2.91

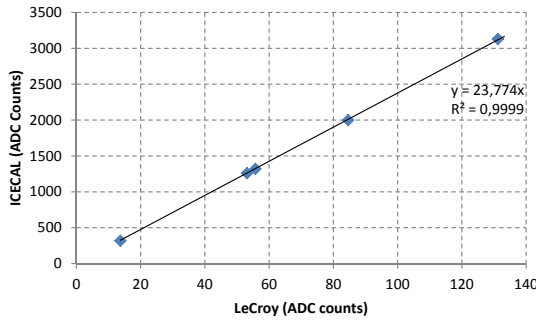


Figure 7.6 – ASIC prototype linearity.

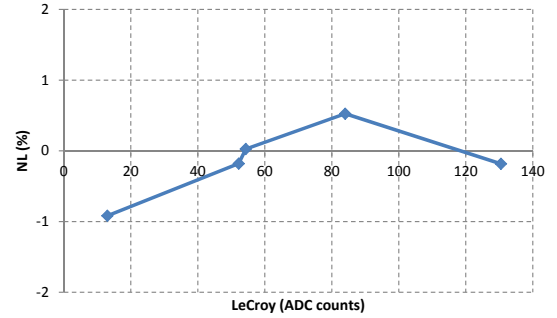


Figure 7.7 – Non-Linearity is below 1% for the energy range measured.

7.3.3 Linearity

Linearity was checked to be better than 1% deviation by comparing the Lecroy and the FEB prototype readings for the different energies of the electrons (Figures 7.6 and 7.7). As a reminder, the non-linearity is calculated as:

$$NL(\%) = 100 \frac{E_{expected} - E_{measured}}{E_{expected}} \quad (7.1)$$

7.3.4 Integrator plateau and spill over

There are two specifications for the analog signal shaping to limit the amount of integrated signal of one particle in one clock cycle (or bunch crossing): a plateau of 4 ns and a spill-over less than 1%.

Both the plateau and spill over are sensitive to changes in the signal shape, so it is fundamental to understand how it is affected and how the pole-zero filter responds when changing the PMT, PMT biasing voltage, the PMT base, the signal cable and when particles with different energies are sensed.

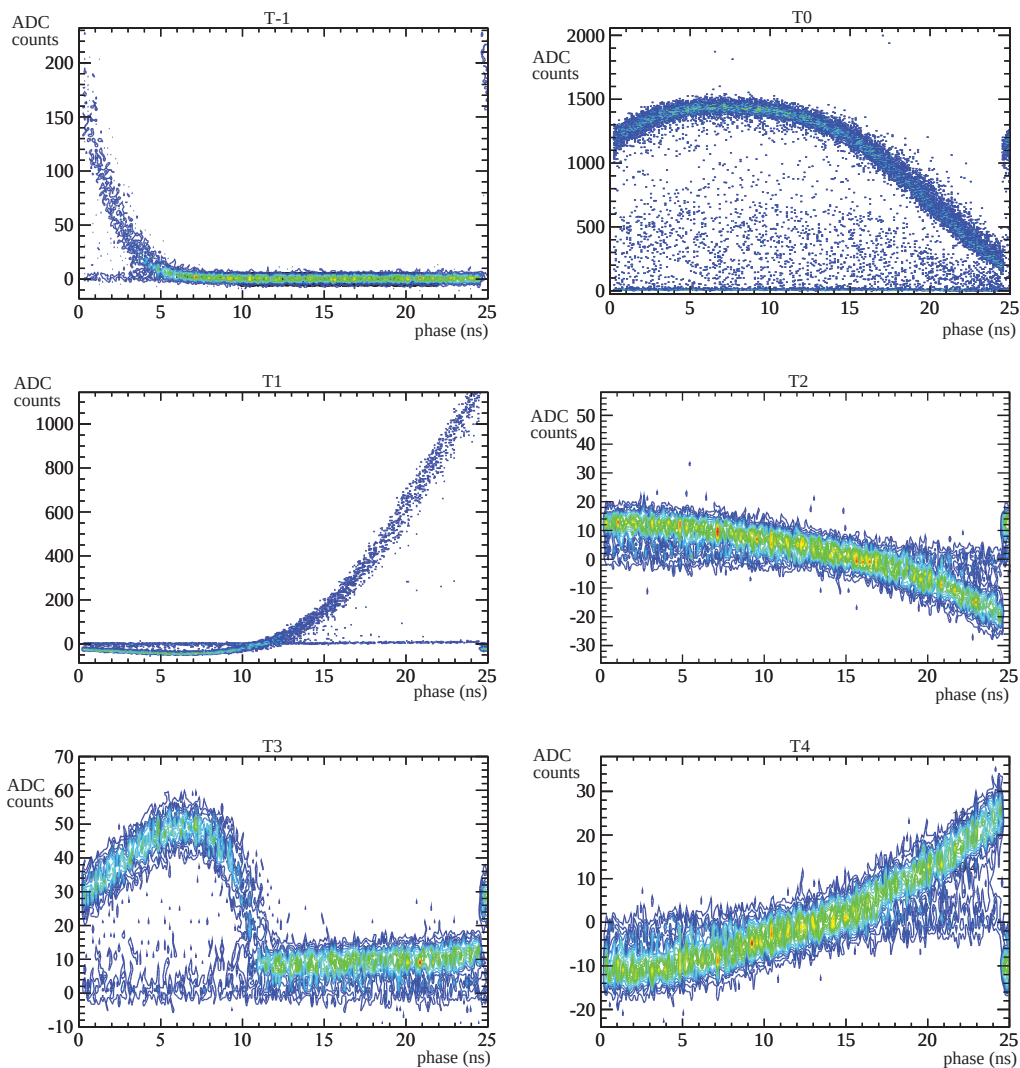


Figure 7.8 – Accumulated events for samples before, at, and after the main signal clock cycle ($T-1$, $T0$, $T1$, $T2$, $T3$, $T4$).

The method to measure the above defined effects requires the ADC value of each event in each of the clock cycles (previous and following ones included) and the timing from the TDC. On each trigger, a set of consecutive samples is stored with its corresponding phase within one clock cycle (0 to 25 ns). The reference sample is named $T0$ and it includes the maximum output value, which corresponds to the main signal of the event. The other samples are named $T1$, $T2$, $T3$, ... for the following samples. For the previous ones, a minus is used ($T-1$, $T-2$, ...). The Plateau is studied in $T0$, while the spill over is the % of the signal at each of the other samples referred to the main signal of the event in $T0$. Fig. 7.8 shows the samples corresponding to a run with the accumulated points for each phase.

Thousands of triggers were acquired on each measurement run with the same conditions (PMT, bias voltage, cable, beam, ASIC configuration,...). Each event places a point in each of the samples studied with an output value in ADC counts at a known phase. All of the events are represented together and cut is applied to separate the electrons respect to the pions, which is not always easy depending on the electron purity of the beam (Fig. 7.9). The electronics output in ADC counts is proportional to the energy in the linear range of the circuit. The energy depends on the integration time, so output will change with the phase and a different cut has to be applied for each phase (Fig. 7.10). Once the cuts are done, the electron peak is fitted resulting in a point in ADC counts for each phase value. Then the curves are studied to obtain the experimental values for the Plateau and spill over.

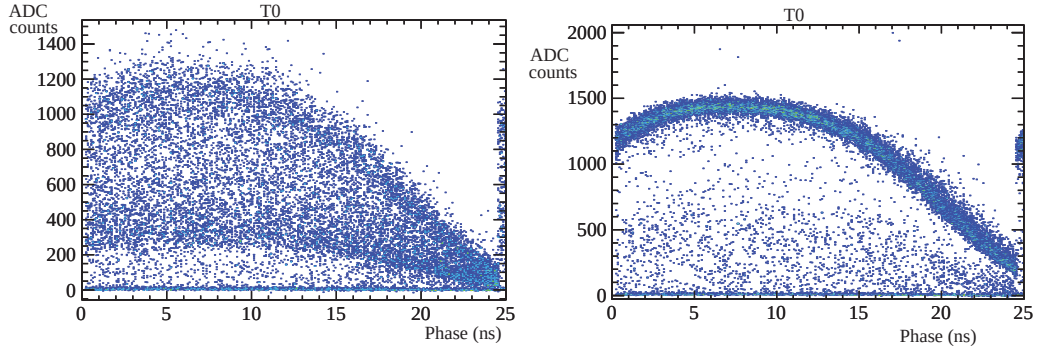


Figure 7.9 – Accumulated events on $T0$ for low (left) and high (right) electron purity beam.

Plateau results

Using the fitted curves at $T0$, the plateau is the amount of phase time in which the output is within the 99 to 100% of the maximum. The specification establishes a minimum of 4 ns of time. Figures 7.11 and 7.12 correspond to measurement

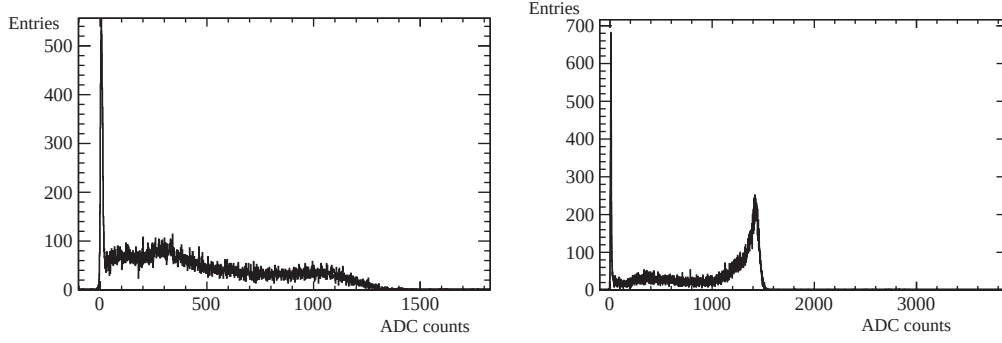


Figure 7.10 – Histograms for a determined phase showing the electron peak and pion background with low (left) and high (right) electron purity beam.

runs which were performed with the same chip configuration, but with changes in the PMT and the PMT base or for different beam energies. As plotted in figure 7.13, most of the plateaus are equal or above 3.8 ns and taking into account the difficulties on the fitted curves and cuts due to a not always optimal electron purity, the specification is reasonably fulfilled.

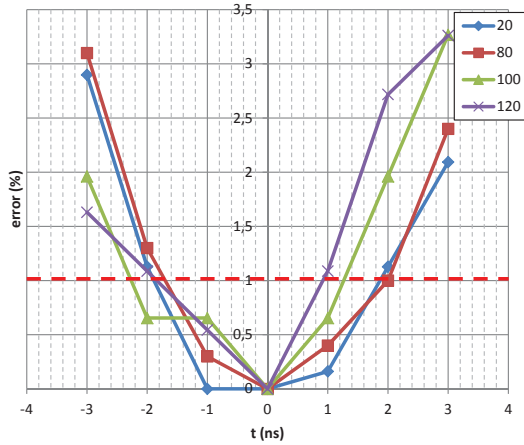


Figure 7.11 – Output plateau for different beam energies.

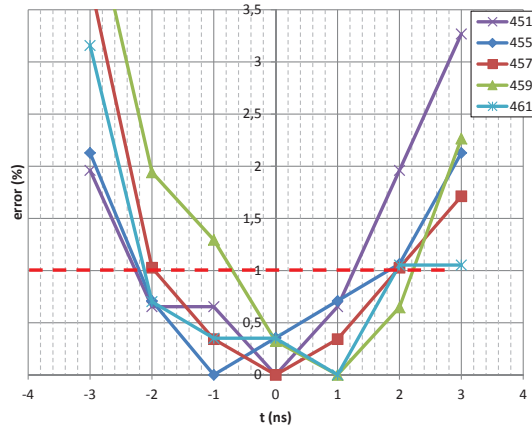


Figure 7.12 – Output plateau for different PMTs and PMT bases.

Spill over results

As with the plateau, the fitted curves are used for the analysis. But this time, the $T-1$, $T0$, $T1$, $T2$, $T3$, $T4$ are studied. The spill over specification sets an upper limit on its value of about 1%. As with the plateau, the measurements were performed with the a fixed chip configuration, but with different PMT and

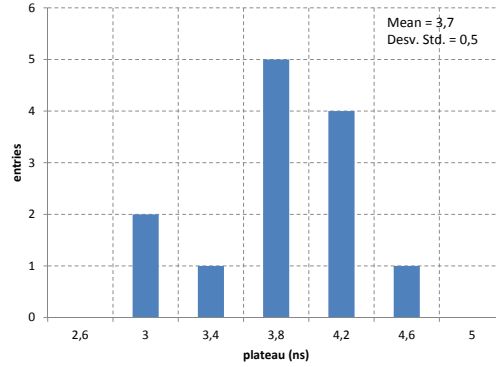


Figure 7.13 – Histogram of all the plateau values measured.

the PMT base or for beam energies of increasing values. As it can be observed in figures 7.14 and 7.15, the specification is mainly fulfilled. The only values that are slightly increased correspond to the lowest energy, which is difficult to fit due to the proximity of the electron peak to the rest of the background. Otherwise, the variation due to the different PMT and its base is low, with one of the slightly above the limits in *T1* and *T3*.

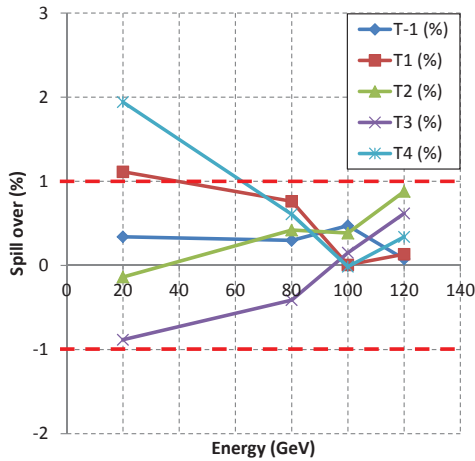


Figure 7.14 – Output spill over for different beam energies.

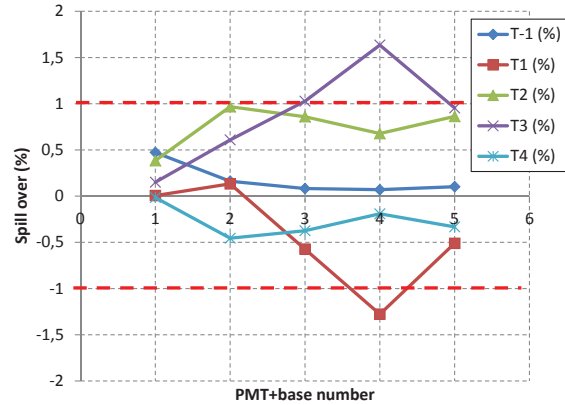


Figure 7.15 – Output spill over for different PMTs and PMT bases.

7.3.5 Conclusions

The test beams conducted allowed to study the analog electronics with detector conditions (real PMT, base, signal cable, ...) except for the grounding which

affected the noise performance. During the test beam the particles used were electrons ranging from 20 to 120 GeV offering the possibility to check the effects of different signal amplitudes and different channel hardware, particularly useful on the measurement of linearity, plateau, spill over, resolution and in the timing on the shower integration.

The measurements above exposed show a behavior within specifications. Special effort was done to understand the effect of pole zero and the different detector conditions on the signal shape and the output of the ASIC. The expected noise levels were not completely reproduced correctly compared to the laboratory results due to a not optimal grounding. Consequently, a measurement at the detector cavern was performed obtaining typical values of about 2.6 and 2.2 ADC counts after pedestal subtraction for ECAL and HCAL channels, respectively.

Radiation qualification

The upgraded electronics will be installed in the gantry, over the ECAL and HCAL detectors. They will be exposed to radiation levels which strongly depend on the position with respect to the interaction point and to other materials producing secondary particles. All components of the LHCb CALO system that are potentially sensitive to radiation damage have to pass radiation hardness tests in order to ensure stable operation over the expected lifetime of the LHCb experiment after the upgrade.

8.1 Radiation effects

As already exposed before [3.11.1](#), radiation effects on electronic components are usually divided in three categories:

1. Total ionizing dose (TID).
2. Displacement damage.
3. Single event effects (SEE):
 - (a) Single event upset (SEU).
 - (b) Single event latchup (SEL).
 - (c) Single event burnout (SEB).

8.2 Expected radiation levels

In the upgrade, the dose on the electronics will be higher than the present electronics due to the higher energy and rate of the interactions. Currently, it is foreseen

that the LHCb experiment will accumulate 50fb^{-1} over 10 years after the upgrade, and all numbers contained in this section refer to this total integrated luminosity.

Simulation of the radiation levels in the LHCb experiment is performed using FLUKA [47]: results are available with reasonable statistics for most points around the experiment and given in terms of Total Ionizing Dose (TID), 1 MeV neutron equivalent fluence per cm^2 and high energy hadrons (>20 MeV) fluence per cm^2 . Geometry and materials used in the simulations of the whole LHCb experiment are the current ones, with a few modifications to match the LHCb configuration foreseen after the upgrade.

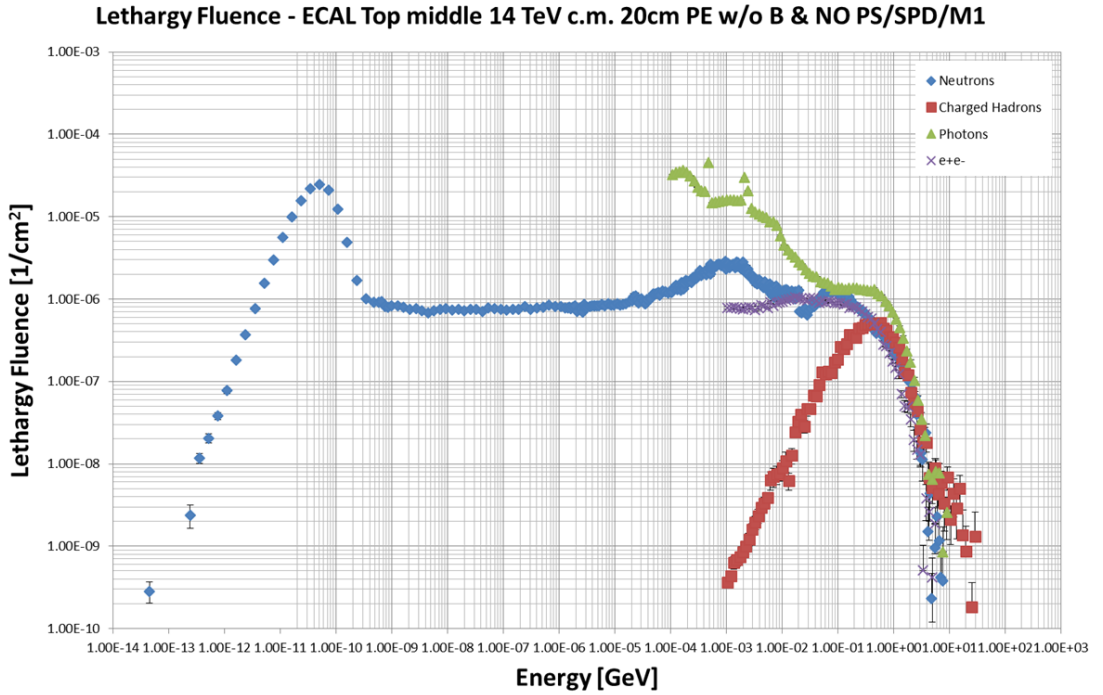


Figure 8.1 – Simulation of the expected irradiation levels at the Calorimeter Gantry.

The simulation indicates an estimated dose of $100\text{ rad per fb}^{-1}$ in the worst case, the bottom part of the electronics above the calorimeter at the calorimeter gantry (Fig. 8.2). Typical statistical errors of 10-30% have to be assumed on the numbers presented here, and a safety factor of two is considered.

Although cross-checks between simulations and dosimeter readings show a relatively satisfactory agreement away from the beam pipe, the detector geometry changes for the upgrade. Therefore, there will be an impact on the dose estimates and the simulations should be revised. Meanwhile, the minimum limit reference was established as $5\text{ krad for } 50\text{fb}^{-1}$. Otherwise, a total fluence of $2.55 \times 10^{-12}\text{ cm}^{-2}$ neutrons is expected.

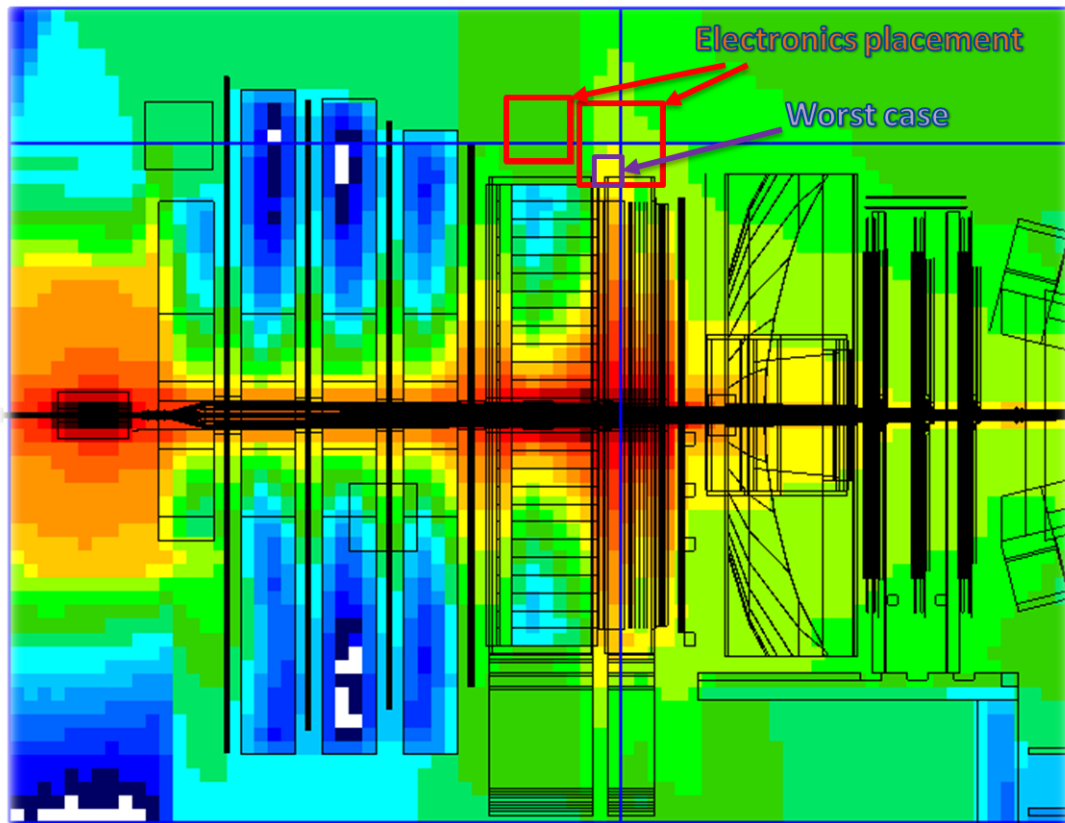


Figure 8.2 – Simulation of the expected irradiation levels.

8.3 Radiation qualification

The radiation hardness qualification of electronic components is usually a complicated task made difficult by limited access to radiation testing facilities and the observed variability of the radiation hardness of normal commercial components. A whole set of radiation tests normally needs to be performed to ensure sufficient immunity to the different effects. A full radiation hardness qualification normally consists of the following tests:

1. Total ionizing dose (TID) test using a X-ray or gamma source.
2. Displacement damage using neutrons from a nuclear reactor or special neutron sources.
3. Single event effects (SEE) test using high energy proton beams and/or ion beams.

The radiation qualification for relatively low radiation levels can in some cases be performed by a single test using high energy protons. High energy protons will give a combined effect of displacement damage, total dose damage and will finally be the potential cause of single event effects via nuclear reactions within the silicon.

Previous irradiation procedures on the electronics currently running in the cavern were done a few years ago [48] [49], at the Centre de Protonthérapie of Orsay (CPO), at the Paul Scherrer Institut (PSI) or at CERN with protons (efficient to get a estimation of the resistance to the dose). Heavy ion beams (GANIL) was also very efficient to test SEL or SEU tolerance.

Moreover, the CLARO chip, for the LHCb RICH Upgrade has been radiation qualified [50] [51]. This chip is build in AMS 0.35 μ m CMOS but with no SiGe bipolar transistors as in the ICECAL case. So CLARO tests show that we should expect that the ICECAL would be radiation qualified, except for neutron irradiation which was not been checked (BJT transistors are not used in that chip).

The tests carried out for the Calorimeter Upgrade electronics radiation qualification, and specially for the ICECALv3, included a TID with 61 MeV protons and a SEE with heavy ion at the Cyclotron Resource Centre of the Université Catholique de Louvain (Louvain-la-Neuve, Belgium). They were performed in the 13th and 14th of July 2016.

8.4 Total Ionizing Dose test

The total ionizing dose (TID) tests were carried out in the Proton Irradiation Facility (LIF) using a 61 MeV proton beam. The particle flux is 5×10^8 pcm⁻²s⁻¹. The TID test is performed in two phases which are iterated until the proposed maximum dose is achieved:

1. **Irradiation:** during the irradiation of the electronics, all the source and reference voltage currents are monitored to check SEL. In parallel and regularly, the internal registers are written and read back to check SEU. And also the clock outputs phase delays are continuously measured to check the internal DLL. The irradiation setup is represented in the figure 8.3. There are two physical zones separated: one with the electronics being exposed to the beam and, another one, separated by a concrete wall, with all of the power sources, PC and scope.
2. **Chip characterization:** characterize the ASIC using the test and setup as in the ASIC global characterization (Sec. 6, Fig. 6.1) with fixed internal parameters (gain, pole-zero,...) to reduce time between irradiations.

The general procedure, then, starts with the characterization of each chip and continues with interleaved irradiations and characterizations until the total dose

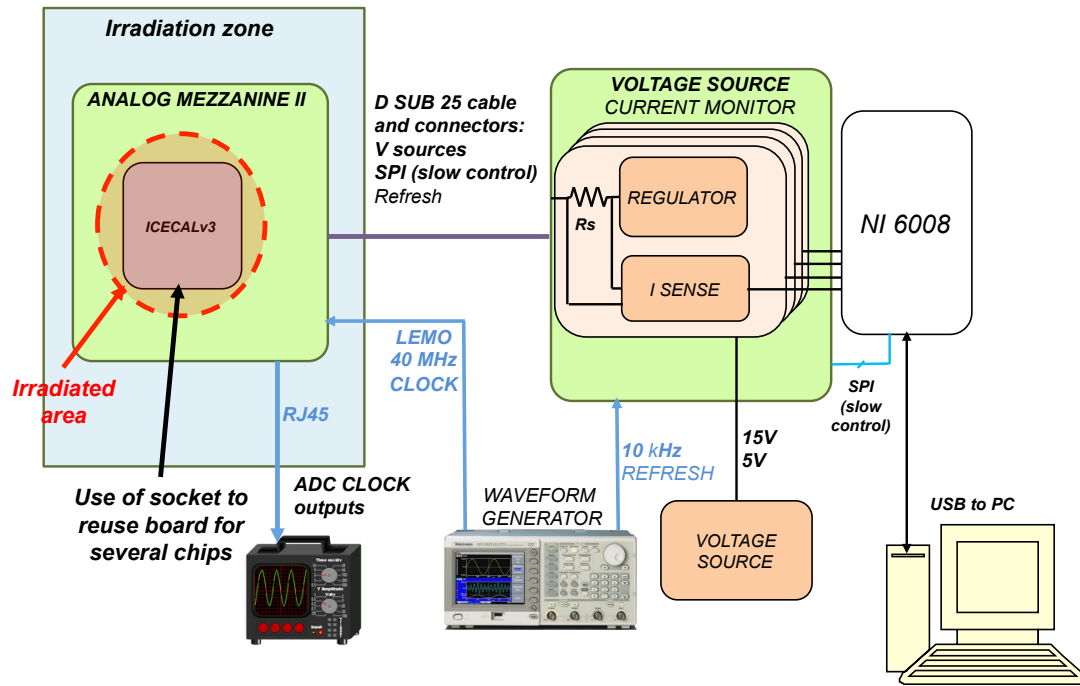


Figure 8.3 – TID test irradiation setup.

is achieved. A 61 MeV proton beam was used to check four chips. Due to time constraints in the use of the beam, three chips were checked with four steps of different doses (up to an accumulated of 55 krad) as described in table 8.1, and another one in one step of 40 krad.

Step	Dose (krad)	Accumulated dose (krad)
1	5	5
2	10	15
3	20	35
4	20	55

Table 8.1 – TID test irradiation steps.

8.4.1 Irradiation effects

At each step of irradiation a basic characterization of the chip was performed to check any changes in gain (linearity), plateau and spill over, and noise. The detailed results are below. During irradiation no SEU or SEL was detected. Also, no change in any ICECALv3 output clock delay was detected.

Channel sensibility

From the linearity measurement, the sensibility (fC/ADC counts) is obtained. All channels are programmed with the same internal parameters. As it can be observed (Fig.8.4), there is a general slight increase for all channels ($\sim 2\%$) after 55 krad which is comparable to the dispersion on the measurements.

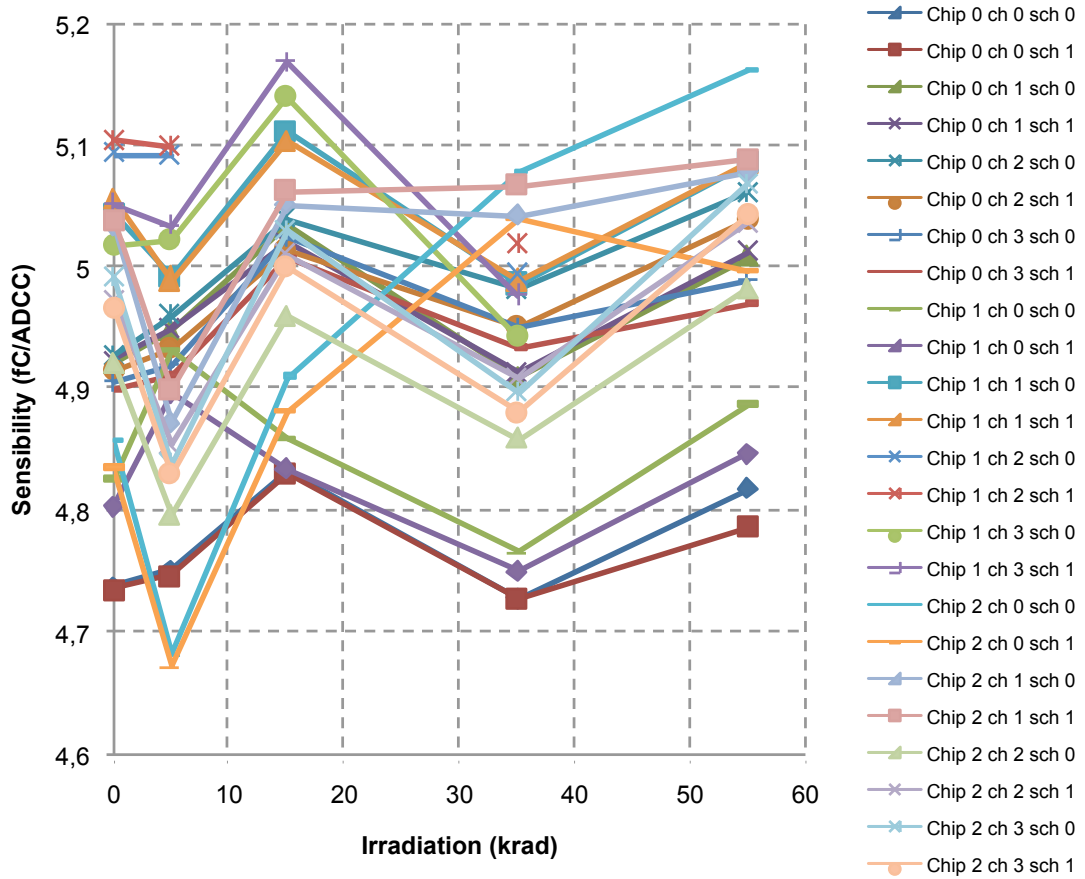


Figure 8.4 – Channel sensibility at different steps of irradiation.

Pedestal

As with all the previous checks, the pedestal of all channels studied seems to be unaffected (Fig. 8.5).

Plateau and spill over

As in the linearity case, the same configuration is applied to all the channels. The radiation effects on the shaping of the signal seem to be not relevant. The results

are plotted in figures 8.6 and 8.7.

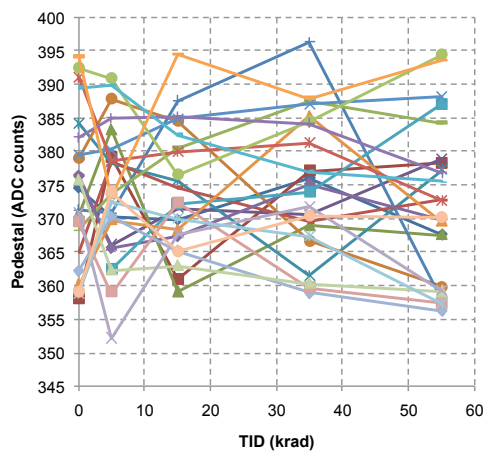


Figure 8.5 – Channel pedestal levels at different steps of irradiation.

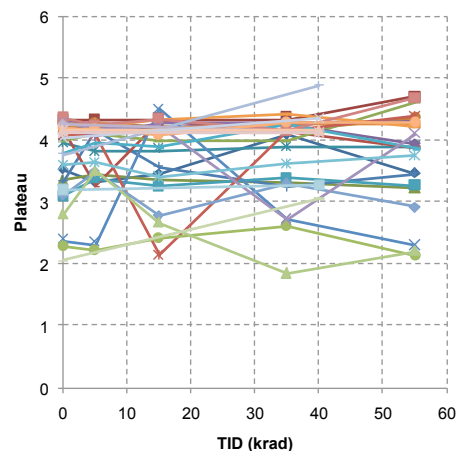


Figure 8.6 – Channel plateau at different steps of irradiation.

Noise

The noise values were acquired with the same conditions. No relevant variation is observed in any of the steps (Fig. 8.8). One of the chips showed low frequency noise in the measurement before the irradiations (a higher noise is observed which is removed when the pedestal is subtracted).

8.5 Single Event Effects test

SEU and latch-up (SEL) measurements have been performed at the Heavy-Ion Irradiation Facility (HIF). Tests used the $^{58}\text{Ni}^{18+}$ ion from the cocktail #2, which allows to reach a compromise value of Linear Energy Transfer (LET), higher than the expected in the detector, but still comparable. The maximum linear energy transfer (LET) that can be reached at the cavern is 15 MeV/mg cm^2 . Properties of the ions in this cocktail are indicated in Table 8.2. At each run, a whole calibration and quality assurance procedure is performed by the HIF responsible; ion fluence, beam profile and energy are monitored.

At the HIF, the beam interacts with the device under test (DUT) inside a vacuum box. As the beam homogeneity is of 10% on a 25 mm diameter, the electronics were placed on a dedicated support which can be centered with a reference. In order to apply the known amount of ions, the chip must be naked (Fig. 8.10). Otherwise, the ions interact with the package and the interaction with the silicon

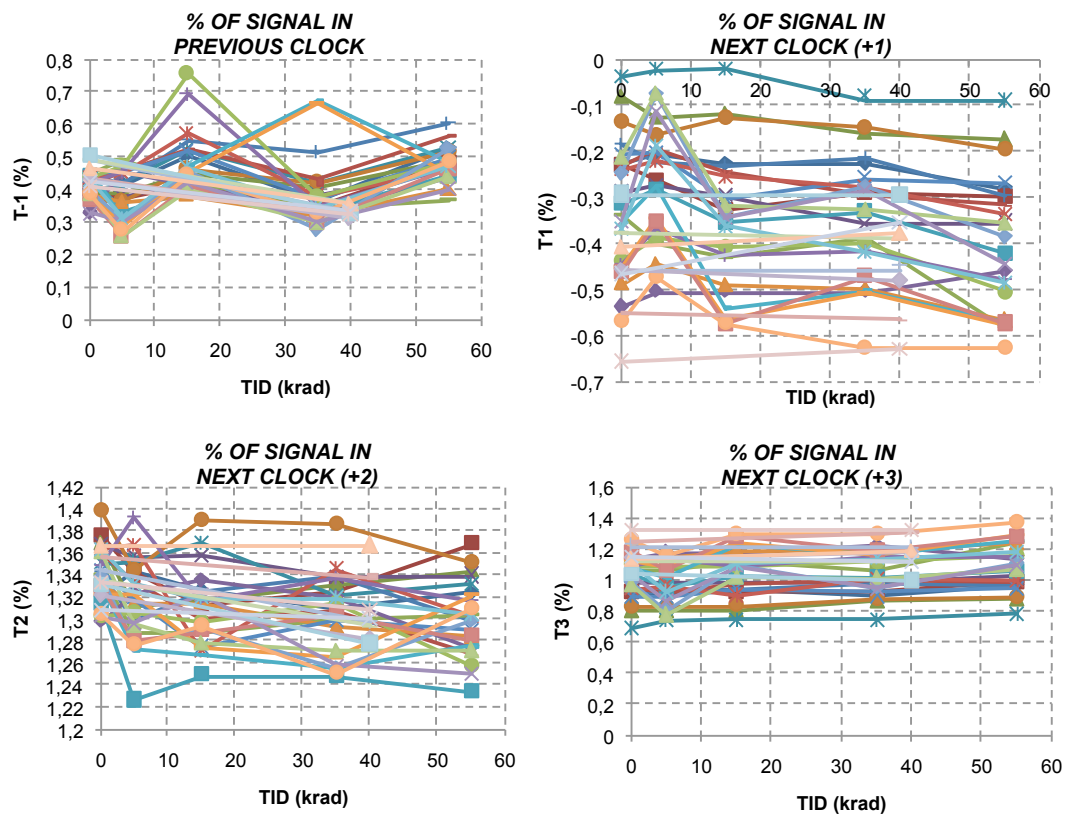


Figure 8.7 – Channel spill over levels at different steps of irradiation.

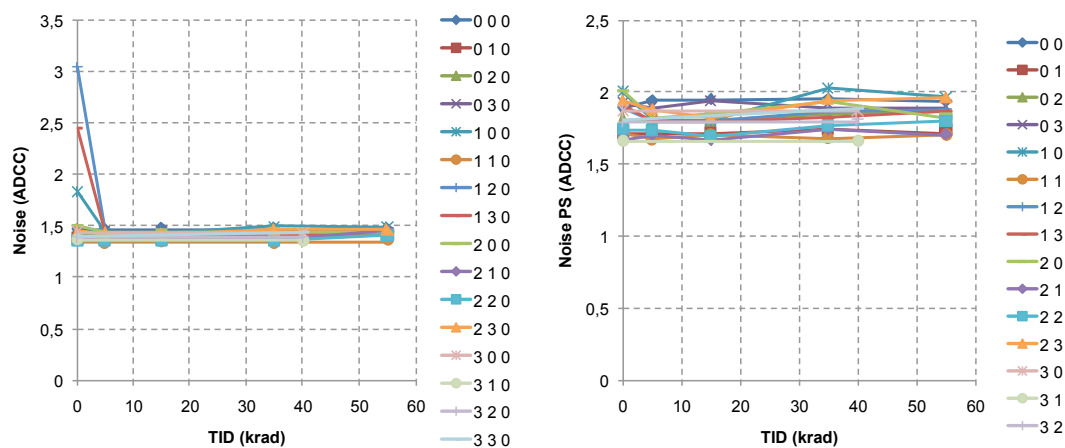


Figure 8.8 – Channel noise levels at different steps of irradiation.

is too much reduced so the test is inviable. We opted to remove the lid of the open

M/Q	Ion	DUT energy (MeV)	Range (um Si)	LET (MeV/mg/cm ²)
3.25	¹³ C ⁴⁺	131	292	1.1
3.14	²² Ne ⁷⁺	235	216	3
3.33	⁴⁰ Ar ¹²⁺	372	117	10.2
3.22	⁵⁸ Ni ¹⁸⁺	567	100	20.4
3.32	⁸³ Kr ²⁵⁺	756	92	32.6
3.54	¹²⁴ Xe ³⁵⁺	995	73	62.5

Table 8.2 – HIF cocktail #2: high penetration.

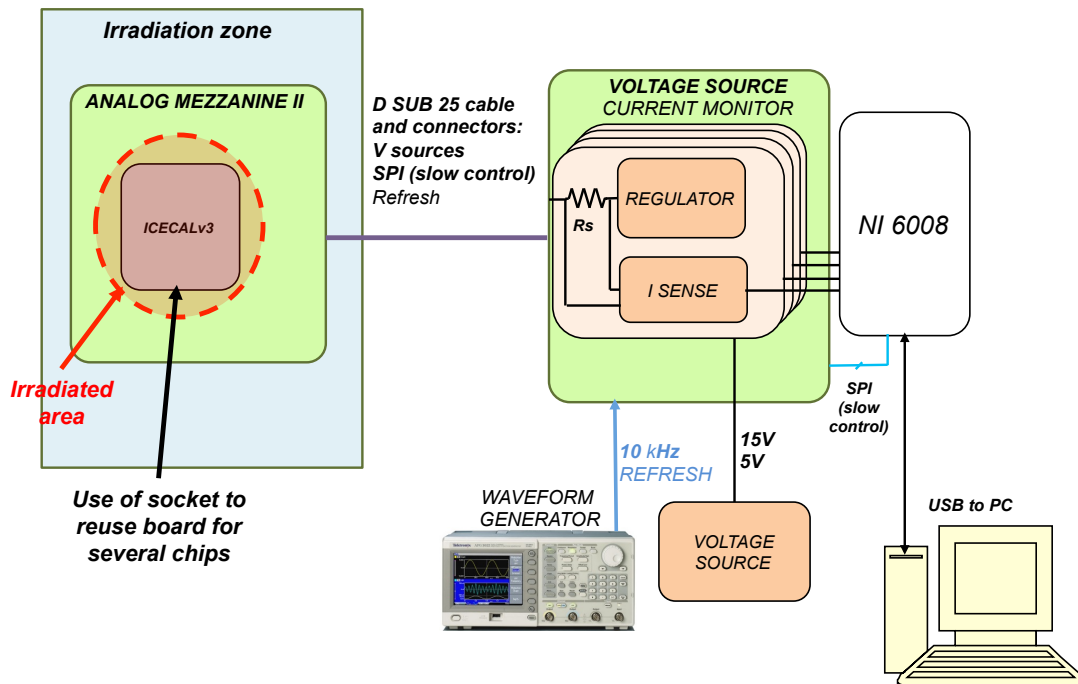


Figure 8.9 – SEE test setup.

cavity packaging. It requires a delicate methodology which consists in applying solvents and heating with hot air (at lower than soldering temperatures). After several iterations, when the glue is soft enough, the lid can be delicately extracted with a vacuum pick up tool.

The complete test setup is depicted in figure 8.9. The elements used are the same of the TID, but without DLL monitoring and characterization between irradiation periods. Inside the vacuum box there is a PCB with the naked chip. This PCB is connected to a voltage source and monitoring PCB which is controlled by a NI6008 [52] [53] and a PC with dedicated software. The refresh signal of the triple

voting registers was obtained from a waveform generator with a square 10kHz wave.

8.5.1 SEU protection on ICECALv3

The ICECALv3 chip registers are protected protection against SEUs with triple voting redundancy (Sec. 4.3.4). This technique reduces the single events by correcting 1 error when the register is refreshed (Figs. 4.8 and 4.9). The refresh event happens when there is a read or write operation or when the $SPI_{REFRESH}$ receives a pulse. During the normal operation of the Calorimeter detector it is planned to connect the $SPI_{REFRESH}$ to the bunch crossing reset signal of the detector fast control to ensure a refresh at about 10 kHz (Fig. 4.11).

8.5.2 Irradiation procedure and SEE results

The SEE studies were divided in two different approaches: with and without refresh of the chip registers. Using the 10 kHz signal there should not be any SEU, but without it, there could be some in the form of register errors.

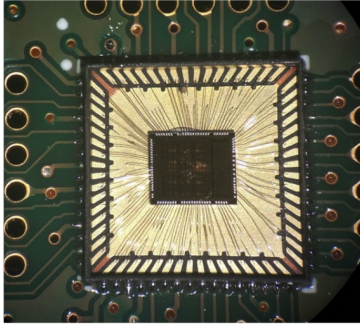


Figure 8.10 – Picture of a naked chip.

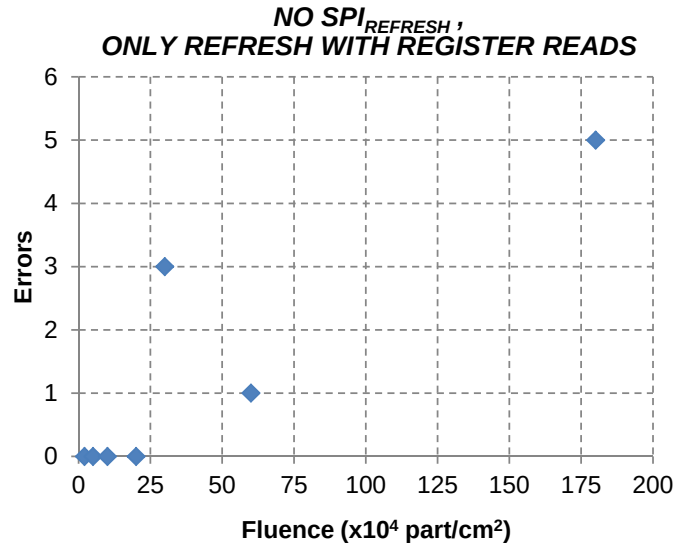


Figure 8.11 – SPI errors during ion irradiation without $SPI_{REFRESH}$.

SEU without $SPI_{REFRESH}$

When the refresh signal is not used, it is possible to study the probability of errors on the registers as a function of the ion fluence. Therefore, irradiation periods of

increasing time (with the corresponding increased fluence) were applied. Although it is not the final implementation of the design, a minimum refresh time can be deduced from this data.

One bit error implies at least two errors in the triple voting flip-flops. As long as it is not possible to account for single errors in the flip-flops, the convention on this text will be $1 \text{ SPI error} = 1 \text{ register bit error}$ (no from flip-flops). Figure 8.11 shows the relation between SPI errors and fluence. For fluences lower than 3×10^5 part/cm² no error was detected, but, for higher fluences, errors were present. We would expect an increase of errors with fluence as it increases the probability of SEU. Contrary to other studies, no cross-section versus LET is presented because it would require the use of only one type of ion for the beam for each LET and the beam used is a combination of various ions (table 8.2). Also, it is not required as the objective is to define a limit on the SEU expected in the detector.

SEU with SPI_{REFRESH}

In case the refresh is connected, it is possible to obtain an estimation of the robustness of the final system against SEU. Two chips were irradiated in this configuration up to 6.45×10^7 part/cm² without any SEU nor SEL (Table 8.3).

Chip	Δt between SPI Reads (s)	Fluence (part/cm ²)	SEL	SEU
41	180	1.8×10^6	0	0
41	600	6.0×10^6	0	0
44	180	2.7×10^6	0	0
44	600	9.0×10^6	0	0
44	1200	1.8×10^7	0	0
44	1800	2.7×10^7	0	0

Table 8.3 – HIF runs with SPI_{REFRESH}.

From simulations included in [4] it is expected an amount of 420 particles per second at a luminosity of 5×10^{32} 1/cm²s. Therefore, approximately 1680 particles per second could be foreseen at the upgrade maximum instantaneous luminosity (2×10^{33} 1/cm²s), from which mostly would be neutrons. Then, considering that the 50 fb⁻¹ would be reached in 2.5×10^7 s, the total fluence to be received by the electronics would be 4.2×10^{10} particles per cm².

During the radiation tests, the chip held beams of protons and heavy ions. Compared to the effect of a heavy ion, 10^6 protons are needed to break a silicon nucleus with a fraction able to trigger a SEE. So, although the fluence is clearly inferior, 1.476×10^{12} protons/cm² compared with 9.708×10^7 ions/cm², there is clearly a benefit in using the ion beam of about 70 times more statistics.

It is possible to extract a rough estimation of the limits corresponding to the irradiation test performed with both heavy ions and protons in detector conditions (with the $SPI_{REFRESH}$). Although no SEU was detected during the irradiations, a maximum limit for upsets happening at the detector can be derived. In Table 8.4 both the protons and heavy ions fluences are compared with the total fluence to be exposed to at the detector and then, with total the number of chips, the SEL limit is calculated. From the heavy ion case, it is foreseen about 1.30 SEU in all the upgraded detector life. If proton beam results are included, the number is almost the same (SEU limit for protons and ions is 0.27).

$$N_{SEU, LIMIT} = \frac{\Phi_{test}}{\Phi_{upgrade}} \times N_{chips} \quad (8.1)$$

Beam	Φ (part/cm ²)	$\Phi_{test}/\Phi_{upgrade}$	# chips	# SEU (limit)
p	1.48×10^{12}	35.14	8×250	56.91
heavy ion	6.45×10^7	1535.71	8×250	1.30

Table 8.4 – Expected amount of SEU limit for the ICECAL chip at the Calorimeter Upgrade from the TID and the SEE tests, when $SPI_{REFRESH}$ signal is used.

Expected SEL limit

No SEL was detected during all the irradiations, both for the TID test with protons and the SEE test with heavy ions. All the ASIC source and reference voltages were monitored. An example of the stable current consumption is shown in the plots of the figure 8.12

In the case of SEL, it is also possible to extract a rough estimation of the limits corresponding to the irradiation test performed with both heavy ions and protons (using Equation 8.1). No SEL was detected during the irradiations, but a maximum limit for latch-ups happening at the detector can be calculated in a similar way as in the case of SEU. Table 8.5 the SEL limit calculations are exposed: it is foreseen about 1 SEL in all the upgraded detector life. Proton beam results represent a little; the number is almost the same (SEL limit for protons and ions is 0.85).

8.6 Neutron effects

Monte Carlo simulations show that the expected thermal neutron fluency at the Calorimeter Gantry, where the electronics will be located, will be about 2.02×10^{11} cm⁻² for an integrated delivered luminosity of 50 fb⁻¹.

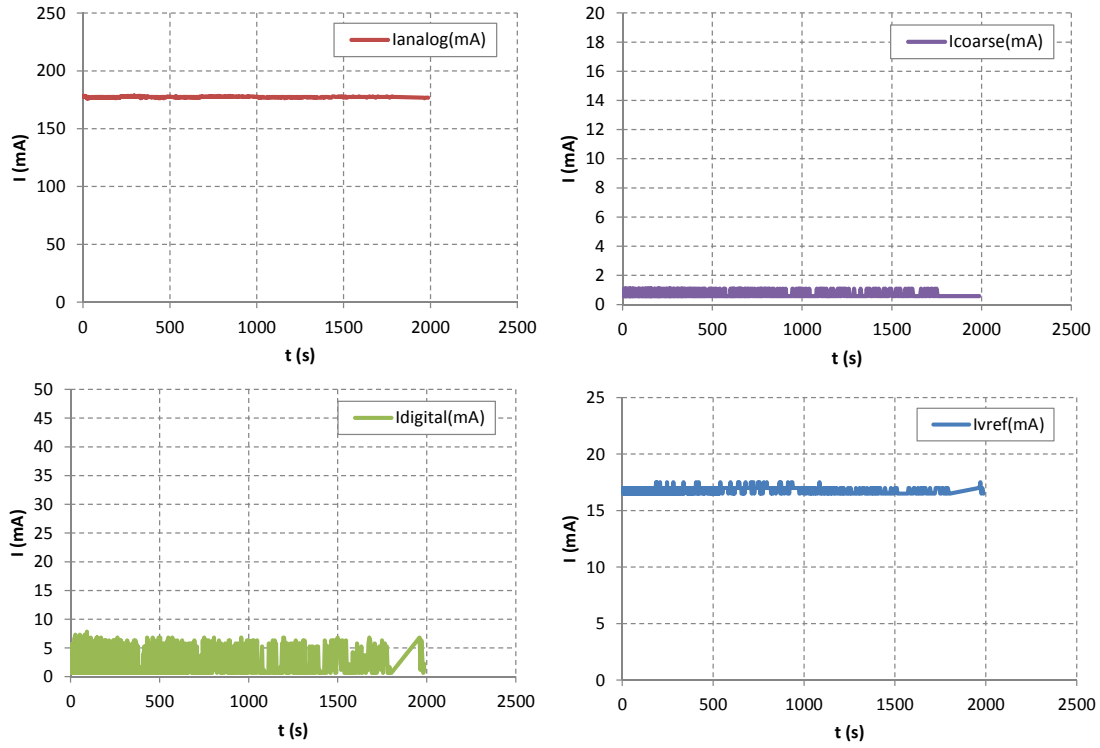


Figure 8.12 – Current plots during irradiation.

Beam	Φ (part/cm ²)	$\Phi_{test}/\Phi_{upgrade}$	# chips	# SEL (limit)
p	1.48×10^{12}	35.14	8×250	56.91
heavy ion	9.71×10^7	2311.43	8×250	0.87

Table 8.5 – Expected amount of SEL limit for the ICECAL chip at the Calorimeter Upgrade from the TID and the SEE tests.

The effect on BJT transistors is described for the ATLAS semiconductor tracker (SCT) [54] [55]. Large degradation of common emitter current gain $\beta = I_{collector}/I_{base}$ caused by thermal neutrons was reported. The damage $1/\beta$ scales linearly with fluence and it can be about a factor 3 larger compared to the deterioration due to same 1-MeV neutron NIEL equivalent fluence. This indicates that thermal neutrons also cause bulk damage in the transistor base. Bulk damage can be qualitatively explained by thermal neutron capture on boron and the associated NIEL of the reaction products.

Comparison of irradiations with protons, thermal, epithermal and fast neu-

trons, showed that beta can be estimated using equation

$$\frac{1}{\beta} = \frac{1}{\beta_0} + k_{eq}\Phi_{eq} + k_T\Phi_T \quad (8.2)$$

where k_{eq} and k_T are 1 MeV equivalent and thermal neutron damage factors and Φ_{eq} and Φ_T are the corresponding fluences. This relation can be used to estimate beta degradation of these transistors in radiation environments with significant fraction of thermal neutrons as will be the case in the ATLAS inner detector. In the LHCb Calorimeter Gantry, the thermal neutron fluence is the main neutron contribution (Table 8.6).

	Fluence (n/cm ²)
Thermal neutron fluence (<0.5 eV)	1.73×10^{12}
Slow and fast neutrons (<20 MeV)	7.06×10^{11}
High energy neutrons (>20 MeV)	1.18×10^{11}

Table 8.6 – Neutron fluence at the Calorimeter Gantry for 50 fb⁻¹.

If we suppose a similar effect for the ICECALv3 technology, in the case of the expected thermal neutron fluency of 1.73×10^{12} cm⁻², the degradation of beta is about 13.7%, and 15.3% if we take into account the 1 MeV equivalent neutron fluence (using similar considerations). For example, the operational input bipolar transistors present a β_0 of 173.1 and would degrade to a β of 146.6.

When we translate the effects over the simulations of the full channel the effects are minimal because the variation of the beta is far from the corner cases (worst case of beta) due to the process variations. Additionally, some decisions at design level help reduce the beta degradation effects: the use of closed loop amplifiers and local feedback with emitter degeneration.

The present technology uses a VBIC model for the simulations in Cadence Spectre. Therefore, it was not straight forward to manually modify the beta for the simulations. In the case of linearity was possible to find a seed in the Monte Carlo model libraries, but for the transient noise analysis the worst corner case was used.

Noise simulations show a 1.069 LSB of noise, which is almost the same as the nominal beta noise of 1.045 LSB. In the case of the linearity, the beta degradation seems to favour very lightly the maximum range without modifying the calibration of the LSB (Fig. 8.13).

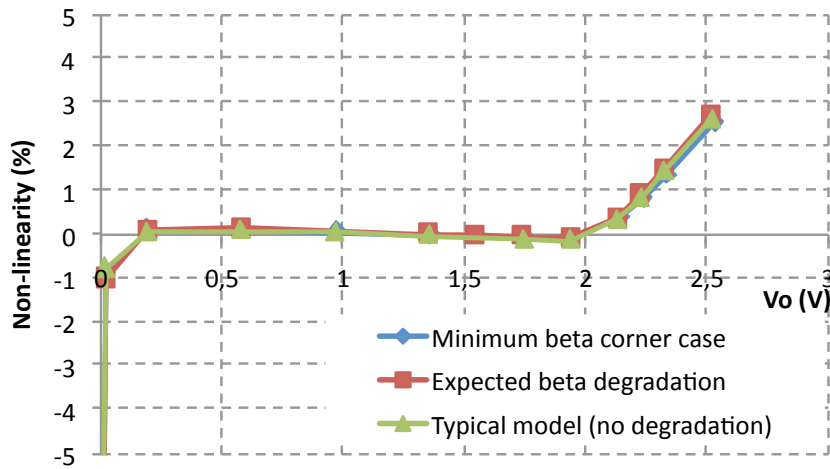


Figure 8.13 – Linearity simulations after neutron effects modeled as variations on BJT.

8.7 Conclusions

Using the LIF facility at the UCL at Louvain-La-Neuve, a 61 MeV proton beam was used to perform a TID test on several ICECALv3 chips well over the expected dose of 5 krad:

- 3 chips with a total dose of 55 krad
- 1 chip with a dose of 40 krad

No significant variation of the chip performance was detected for pedestal levels, gain, plateau, spill over and noise. Also, no SEU or SEL was noticed during irradiation.

In order to characterize the radiation hardness to single events, another test was executed in the HIF facility of the same installations in the UCL. This test consisted in irradiate two chips with a heavy ion beam to evaluate them up to a total fluence of 9.708×10^7 part/cm². No SEL was detected after a total fluence of 9.708×10^7 part/cm².

The SEE studies were divided in two parts. First, analysis were done without a register refresh to measure the resilience of the registers to SEU. No SEU was detected for fluences lower than 3×10^5 part/cm². In the second part, the chips were exposed to the ion beam under detector running conditions (with the register refresh signal at 10 kHz) and no more SEU were spotted, leading to an expected limit of 1.3 SEU in the full detector during the upgrade.

No latch-up was reported during all irradiations. Consequently, a rough maximum limit of 1 SEL was established for all chips of the upgraded Calorimeter during the planned functioning.

Production and quality control

9.1 Production

There are 6016 and 1488 channels on ECAL and HCAL subdetectors respectively. Therefore, the amount of chips needed is 1876. If we consider a yield of 80% (much lower than expected) and a 30% of spares, a total of 3050 dies are needed.

9.1.1 Yield estimates

In the design phase, care was taken in respecting not only all the design rule checks (DRC), but also most of the design for manufacturability (DFM) rules. The area of the chip was filled with POLY and MIM coupling capacitors. This, combined with the fact that the die area is relatively small and that the technology is mature, is expected to result in a high yield. Despite of the fact that the production will be probably done in a shared engineering run for costs reduction, it is possible to extract an approximated yield estimation from the tool on the AMS website (<http://asic.ams.com/gelato/>). This tool offers various options to calculate the probability of wafer defects. In the worst case, the tool gives a 96.96% yield for the ICECALv3 chip (Fig. 9.1). It includes all wafer defects (from valid wafers). The packaging process yield can be considered to be above 99%. These estimations are compatible with the 30 chips tested positively, for which the expected functional chips would have been 29.

The molded plastic packaging in $9 \times 9 \text{ mm}^2$ QFN64 will be done at ASE (Taiwan). It has already been ordered a short run to package 40 chips in order to be checked. So far, the packaging used for the prototypes has been plastic open cavity.⁴

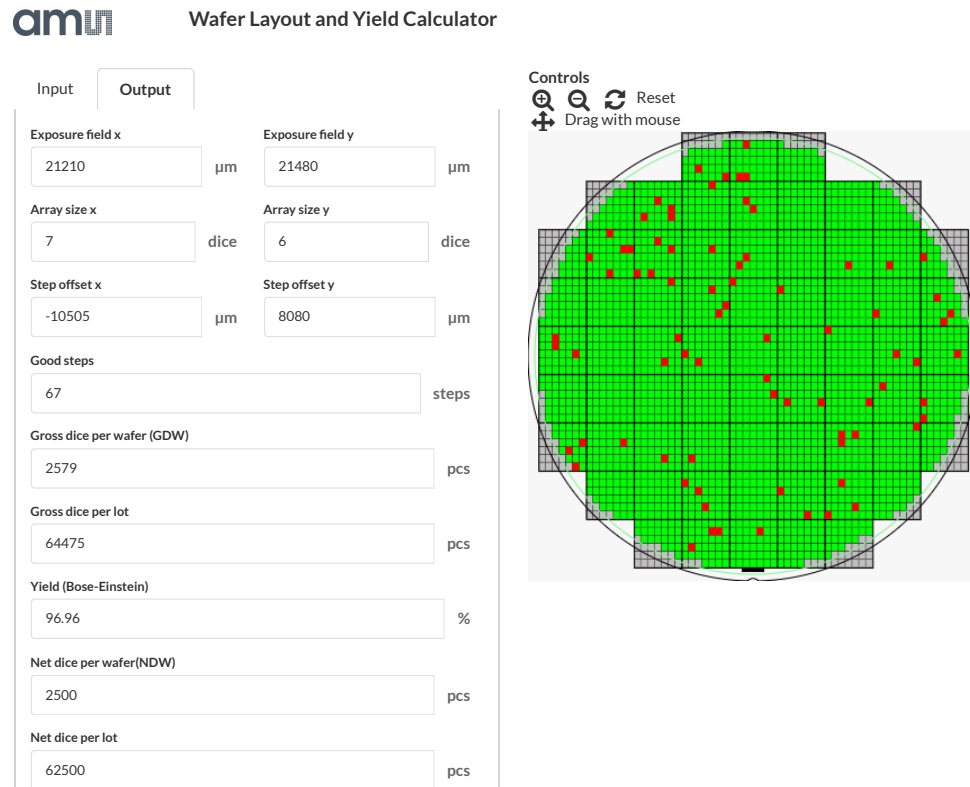


Figure 9.1 – Yield simulation from the Gelato tool at the AMS website.

9.1.2 Production staging

AMS uses 8-inch wafers for this technology. It is expected to place 2000 dice in the shared project wafer, which represents about a 60% of the area. In engineering runs, 6 wafers are fabricated, but only 2 are guaranteed to satisfy to be “good wafers”, i.e. to satisfy the wafer quality checks at AMS. In practice, 5 or 6 “good wafers” are expected.

9.2 Quality control in mass production

A mass production of the ASIC would imply to test about 3000 pieces taking into account the amount of channels, the yield of the chips and the spare parts. It is necessary to redesign and optimize the test setup in order to be able to test all the chips in time enough to be ready for the Front End board production. The test would consist in measure each channel behavior in the same terms as in the section 6 but with a previously fixed values for all the configuration registers. Also,

there will be a PCB dedicated to replicate and distribute the input pulses to the different channels instead of changing the input cable position manually.

One option would be to use the full set of 8 data channels offered by the FE prototype (Fig. 9.2). Then, the analog mezzanine would be composed essentially of 2 chip sockets and 4 ADC chips.

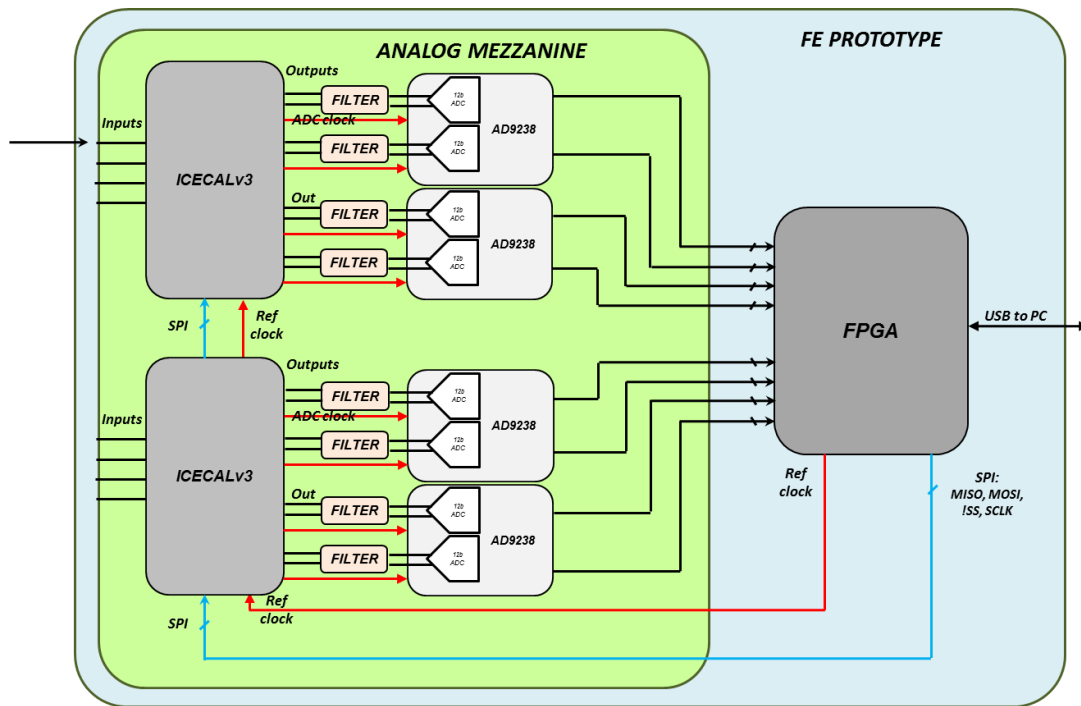


Figure 9.2 – Proposed scheme for the quality control in mass production.

In any of the options considered, the level of automation of the test procedure and the chip handling will allow an optimization of speed, efficiency and the decrease of operator errors. It has been planned to use a robotic system for the chip handling. Although it is not designed, the basic scheme is already decided:

- Motorized horizontal gantry system to move the chips from tray to the test PCB and to final tray.
- Motorized stage in the vertical direction.
- Pneumatic suction.
- Pressure sensor.

The idea is to pick the chip from its original location in tray, align it, lower the chip in the PCB test board, proceed with the test, remove it from the PCB and leave it in the *pass-tray* or in the *no-pass-tray*.

9.2.1 A chip test for the quality control

The test setup and procedure for the characterization of the 30 first prototypes searches for the best channel parameters in order to achieve the specifications (Table 2.1). Consequently, the test for each chip takes an amount of time not suited for all the production; a 4000 chip test would last about 2 years. Still, another approach is possible that reduces drastically the test time: to program only one set of parameters for all the chips. Finding the set of parameters is possible if the mean parameters values are obtained from a statistically reasonable amount of chips. Then, the ASICs which will not pass the quality control would be the ones at the tails of the measurement distributions. Therefore, some cuts based on the specifications would be defined.

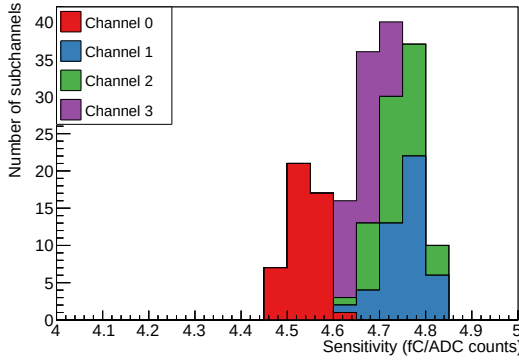


Figure 9.3 – Stacked histogram of all the sensitivity measurements with fixed channel parameters.

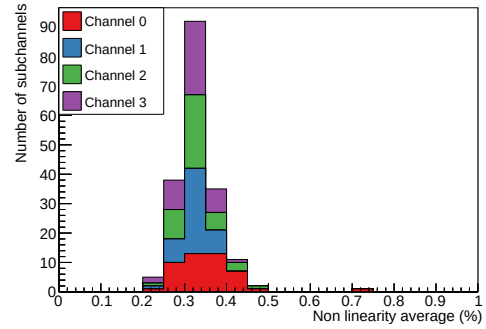


Figure 9.4 – Stacked histogram of all the mean non-linearities with fixed channel parameters.

In order to study the viability of such an approach. A fixed channel parameters test was performed to compare the characteristics for the first prototypes. The analog channel main characteristics measured include the sensitivity (inverse of gain), offset, linearity, crosstalk, plateau, spill over and noise. They all depend on the tunable values of, mainly, the integrator capacitor (gain), the pole and zero of the filter (plateau and spill over), the input impedance and the offset (linearity and noise). In the present section, the detailed results of the measurements are presented. It is possible to summarize that, for at least the first 30 prototypes, it is feasible to perform an accelerated test for qualifying the ICECALv3 in about 5 weeks time (with ~ 3 minutes per chip).

Linearity, sensibility and crosstalk The output signal is measured in ADC counts for different input amplitudes, which are calibrated and correspond to integrated charges (or energies). Then, the non-linearity and the crosstalk are computed for each amplitude. Also, from all the lineal values, is possible to obtain the sensitivity. Figures 9.3 and 9.4 show stacked histograms of the sensitivity and non-linearity. Notice a small difference between channel 0 and the rest for all chips. Otherwise, the linearity is below 1% deviation and the cross-talk below 0.5%.

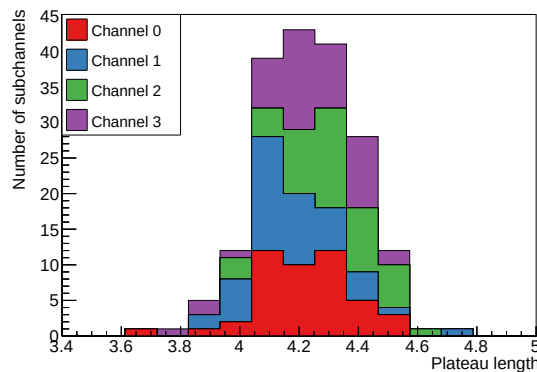


Figure 9.5 – Stacked histogram of all the plateau measurements with fixed channel parameters.

Plateau The plateau represents the capacity of the system to assure a stable output for the detection of particles with different arrival time. The typical plateau values can be seen in figure 9.5. They are mostly above of the 4 ns and there is no noticeable difference between channels.

Spill over The amount of input signal which is integrated in the previous and following detector clock cycles is defined as the spill over. It has been measured below the 1% level except for the +2 cycle, which is about 1.5%(Fig. 9.6). There is a trade-off between the plateau and spill over values; a better plateau implies a worse spill over and vice versa.

Noise Noise measurements were done obtaining similar results to the characterization campaign. The most remarkable characteristic can be easily observed in the stacked histograms (Fig. 9.7). Due to slight differences in gain, the noise at the output is smaller for channel 0 than the rest. In a final test it would be recommendable to modify the parameters of channels to have a more uniform results.

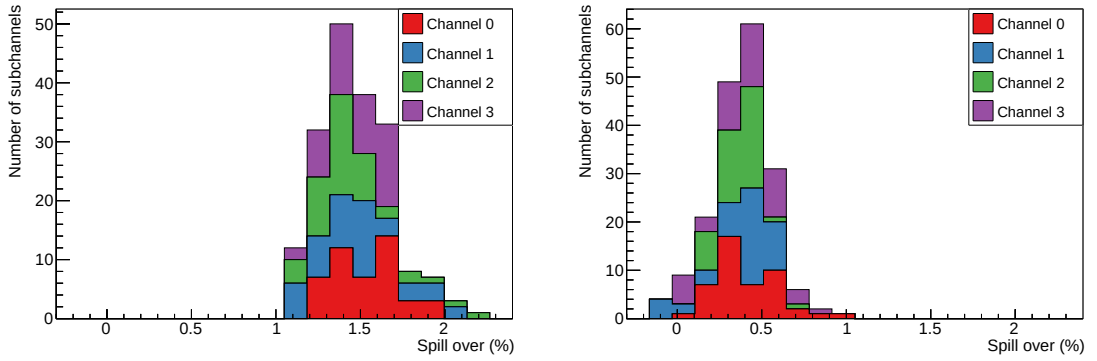
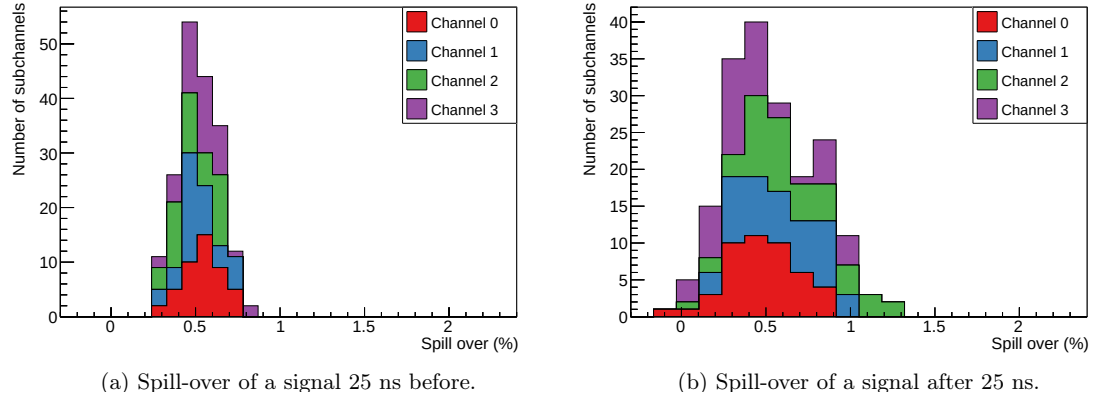


Figure 9.6 – Stacked histogram of all the spill over measurements with fixed channel parameters.

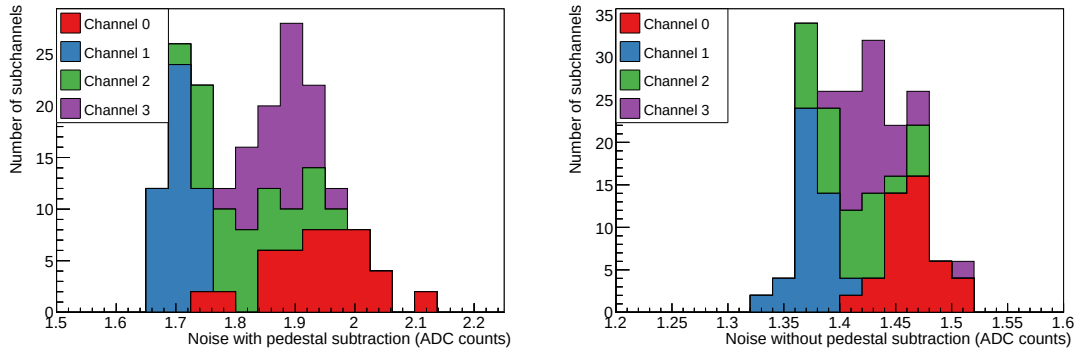


Figure 9.7 – Stacked histograms of all the noise, with and without pedestal subtraction, measurements with fixed channel parameters.

9.3 Stress and reliability tests

The failure rate of the electronics can be represented by the bathtub curve [56] (Fig. 9.8). It comprises three parts:

1. **Early failure:** it includes the defective ASIC, handling errors and installation errors.
2. **Useful life:** represents the normal and low failure rate (almost constant).
3. **Mean-life:** it is the time when the devices wear out.

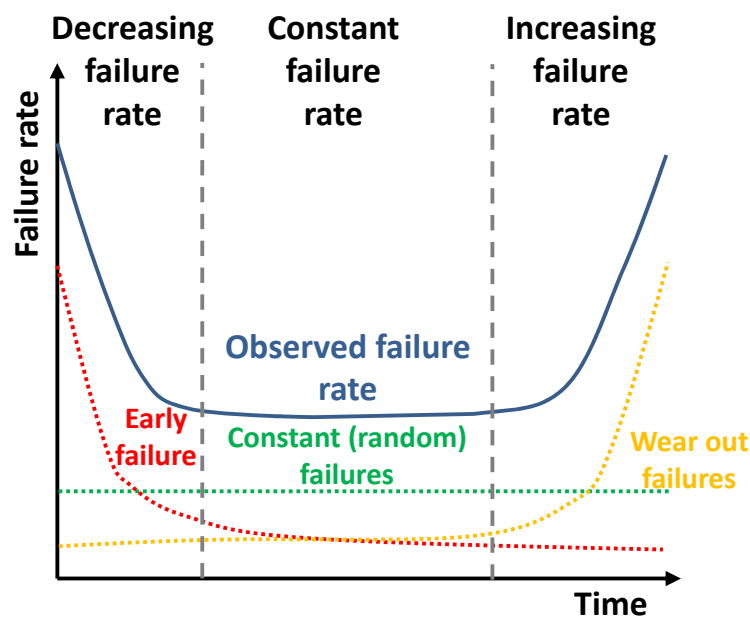


Figure 9.8 – Bathtub curve.

In case of a high early failure rate of the electronic component, it is necessary to undergo a burn-in process and avoid the early corruption of the system. From the prototype series of 30 pieces, no defective chip was detected. So, a low early failure rate is expected. Nevertheless, accelerated aging tests are envisaged on a statistically significant amount of chips to estimate this rate and the average life of the system.

The stress test can be done by combining:

1. Increase the power consumption.

2. Increase the biasing voltage over the defined value o 3.3 V.
3. High temperature operation.

Increasing the temperature from the expected operating junction temperature $\sim 25^\circ\text{C}$ to $\sim 125^\circ\text{C}$ causes an accelerated aging of the system that can be described by the Arrhenius equation. It states an acceleration factor:

$$A_F = \exp \left[\frac{E_A}{k_B} \left(\frac{1}{T_{chip}} - \frac{1}{T_{high}} \right) \right] \quad (9.1)$$

where E_A is the activation energy (which is approximately 0.7 eV for chips). The acceleration factor for these values is 940, meaning that the 1 years of normal functioning of the detector would correspond to a 10 hours of test.

The stress qualification will be divided in two steps. First, a complete stress test on a statistically significant amount of chips, which will consist in apply the accelerated aging conditions until the devices fail, to allow to estimate their average life. A second test, with softer conditions and limited time of stressing conditions, will be applied to all of the front end production in order to highlight the defects in the ASIC or in the PCA soldering.

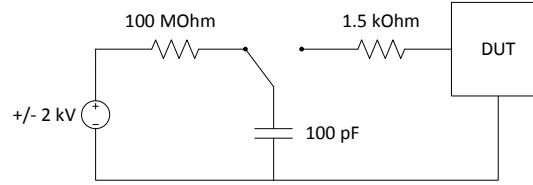


Figure 9.9 – Human-body model circuit for delivering a current pulse to a device.

9.4 ESD test

The ICECALv3 is mostly protected against Electro static discharge (ESD) at the pad ring level because standard AMS pads are used, except for the input signals, which offer low ESD protection as they present no impedance. Therefore, tests over a limited number of chips are envisaged. There is some experience in our group related to prototypes of the LHCb SPD chip which suffered variations in the offset due to ESD problems [57] solved after adding protection in the sensitive pads. The plan is to apply a series of 2 kV discharges on input channels and other pins which could be affected (Fig. 9.9).

9.5 Commissioning and calibration of the chip in the experiment

The procedure of commissioning and calibration of the chip in the experiment will be limited as the chip will have been already calibrated to an established value of the different configuration parameters during the chip production test. Further adjustment procedures of the parameters of the analog channel will be studied.

The synchronization at all the different levels has been proposed and is under discussion within the Calorimeter group.

In the detector, the whole front-end electronics system must be perfectly synchronized to the bunch collisions of the LHC machine to capture correctly the signals from the different detector elements. A complicated system with different delays for each channel to compensate for differences in photomultiplier tube biasing voltages, different cable lengths and fibers is used. The timing parameters are extracted during special calibration runs of the system. There are 4 main levels to fix:

1. The input clock has to be fixed so that the sub-channel reset is captured correctly.
2. The Integrator and TH clock: the objective is to fit most of the signal (up to the 1% level) in one clock cycle. It is achieved maximizing the integrator output.
3. The ADC clock: The ADC clock phase allows synchronizing the digitization at the FPGA and TH output. It depends essentially in the FE board routing.
4. The data capture at the FPGA input: It is still possible to adjust the FPGA parameters in order to modify the phase to ensure a correct capture of the 12 bits coming from each ADC output.

The input signal phase (2) will be different for all the channels, but the valid phases to synchronize the different levels commented depend only on the front-end board. Therefore, it is possible to study the board and prepare those correlated phases beforehand.

The aim of this thesis was to present a solution for the analogue signal processing chain to be used in the LHCb calorimeter upgrade to substitute the present electronics and adapt to the new detector conditions.

10.1 Main achievements

An integrated circuit for the LHCb Calorimeter electronics upgrade has been presented, designed and tested. The analog channel architecture is intended to shape and integrate photomultiplier tube signals at 40 MHz, which is the event rate at the LHC at CERN. It offers a novel circuit solution to meet the requirements of the system. A current amplifier input stage includes an active termination controlled by two feedback loops to reduce the input referred noise. It is followed by two alternated switched integrators allow capturing the signal when no dead time is allowed for a range of 12 bits. Moreover, the analog channel is capable of correcting for the slow components of the signal in order to not affect the following measurements. In addition, the chip includes a dedicated delay line that synchronizes all of the internal stages, as well as the external ADC data acquisition. Finally, the circuit offers some programmable parameters to compensate for process variations and adjusting the signal shape for correct integration.

The ICECAL achieves the requirements for the analog electronics of the Calorimeter Upgrade: a calibration of 4.5 fC/LSB for 12 bit range, noise $\lesssim 1$ ADC cnt (ENC < 4 fC), non-linearity lower than 1%, spill-over less than $\pm 1\%$ and integrator plateau with 1% variation for 4 ns. The key characteristics of the signal processing which allow meeting the requirements are:

- Reduced input noise to meet the Calorimeter Upgrade conditions by using an active line termination in a current pre-amplifier. The photomultiplier tubes

will reduce the gain in a factor 5, so the noise has to be reduced accordingly.

- The use of two interleaved sub-channels avoids any dead time.
- A fully differential configuration is adopted to minimize the the effects of a switching system on signal integrity.
- A pole-zero shaper helps reducing the effects of the long tail of the calorimeter pulses. The integrator signal is stable for particles arriving at different times due to different paths and placement of the detector channel. Also, the spill over is minimized.
- The internal delay line allows fine synchronization tuning for each channel integration, Track-and-Hold and ADC from just one common clock signal. Each channel requires independent synchronization because of different photomultiplier tube biasing voltages and signal cable length.

Special care has been taken in the design in order to reduce the radiation effects on the ASIC. Specifically, the use of:

- Guard rings to prevent latch-up effects in CMOS technology (including the modification of the logic standard cells). It also helps protecting against noise and cumulative effects.
- Triple Voting Redundancy (TVR) to minimize the single event effects in the registers that keep the internal configuration of the chip.
- NAND gates wherever possible instead of NOR gates, improves the immunity to accumulative effects.

The design was checked at different tests of a total of 30 units of the final prototype at the laboratory using a signal obtained with a scope, with electron beams and ECAL channels in a dedicated facility at CERN, and its radiation hardness at Centre de Ressources du Cyclotron at Louvain la Neuve. Dedicated boards were developed and the results were positive.

10.2 Possible improvements and outlook

Out of the scope of the thesis, the next steps and possible improvements are discussed in next lines.

The design presented is certainly capable to fulfill its role in the analog electronics for the LHCb Calorimeter Upgrade. It has passed the tests for its functionality

and radiation hardness. Otherwise, there are still some steps before the final detector electronics are installed and commissioned. First, an ESD test is necessary to prove the electronics resilience at the inputs. Second, to validate the production of the chips, some stress and reliability tests are envisaged which include temperature and voltage sources cycles. And, third, the final production test in all ASIC.

Possible improvements of the chip could include some minor changes to reduce the amount of external parts of the board. For instance, an internal reference voltage generation block could be added. It would reduce the circuit that generates it on the board, but it is still necessary to have decoupling capacitors too big to be feasible inside the ASIC, so the reference voltage would still require some circuitry on board.

Another interesting feature to be eventually added to the chip, would be a pulse generation circuit which would be used at the detector to check the photomultiplier tube output, the signal cable and the ASIC input. The measurement of this pulse is different depending if there is a problem and where it is located (as the pulse reflections change). A similar circuit is in use in the present electronics and it has proven to be of great use to determine and localize problems. Both the reference voltage and the test pulse circuit have been discarded for the present production due to time constraints and the relative benefits of it, as long as there are already proven on board versions for them.

Otherwise, the possibility of increasing the dynamic range of the detector for the study of other physics not targeted initially by the LHCb can be considered. In this context, different proposals have been made that affect the analog electronics design at different levels:

- Use the present ICECAL design and program the lowest gain using the lowest possible integrator capacitor and reducing slightly the gain at the photomultiplier tube. Then, the maximum transverse energy that could be measure would increase from 12 to 20 GeV. Unfortunately, the signal to noise ratio would worsen and the effective noise would be increased from 3.8 to 4.5 MeV. A 12 bit ADC would still be enough.
- Reduce the gain at the current preamplifier stage. The modification at in the ASIC design is feasible with the present schedule. It requires to reduce the current in the inner loops. Obviously, this modification would reduce the signal to noise ratio. It is the most reasonable solution without major changes in the analog circuit that would require a new approach (much more time and an increase in budget) and it will be developed before the start of the production. It is proposed to include the standard solution and this one in the final fabrication. The decision of which one would be installed would be done afterwards.

10.3 Publications

The list of publications is detailed next:

1. Gascon, D.; Picatoste, E.; Abellan, C.; Duarte, O.; Garrido, L.; Grauges, E.; Lefrancois, J.; Machefert, F. & Vilasis, X. Low noise front end ASIC with current mode active cooled termination for the Upgrade of the LHCb Calorimeter *Proceedings, 2011 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC 2011)*, **2011**, 1445-1452
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3. Picatoste, E.; Gascon, D.; Abellan, C.; Lefrancois, J.; Machefert, F.; Duarte, O.; Grauges, E.; Garrido, L. & Vilasis, X. Low noise front end ICECAL ASIC for the upgrade of the LHCb calorimeter *JINST, Electronics for particle physics. Proceedings, Topical Workshop, TWEPP-11, Vienna, Austria, September 26-30, 2011*, **2012**, 7, C01080
4. Picatoste, E. LHCb Calorimeter Upgrade Electronics *Proceedings, International Conference on Calorimetry for the High Energy Frontier (CHEF 2013)*, **2013**, 363-368
5. Picatoste, E.; Bigbender-Beau, C.; Duarte, O.; Garrido, L.; Gascon, D.; Grauges, E.; Lefrançois, J.; Machefert, F.; Mauricio, J. & Vilasis, X. Low noise 4-channel front end ASIC with on-chip DLL for the upgrade of the LHCb Calorimeter *JINST, Proceedings, Topical Workshop on Electronics for Particle Physics (TWEPP14)*, **2015**, 10, C04017

Appendices



Cable effects on SNR

Before designing the analog system to amplify and shape the calorimeter PMTs signal, it should be taken into account that cables provide some constraints for fast shaping signals. Specifically, the cable effects on signal to noise ratio (SNR) are:

- Attenuation due to the skin effect which generates a long tail in the step response of the cable so part part of the signal is delayed and does not contribute in the same clock cycle.
- Resistance of the cables which adds a noise source distributed along the cable.

A.1 Skin effect

The Skin Effect is the tendency of AC current to distribute itself within a conductor so that the current density near the surface of it is greater than at its core, instead of flowing uniformly over the entire cross sectional area of the conductor. The higher the frequency, the greater the tendency for this effect to occur.

Skin effect is due to the circulating eddy currents canceling the current flow in the center of a conductor and reinforcing it in the surface.

A.2 Signal attenuation due to Skin Effect

The penetration or “skin” depth δ is defined as the distance over which the current falls $1/e$ of its original value:

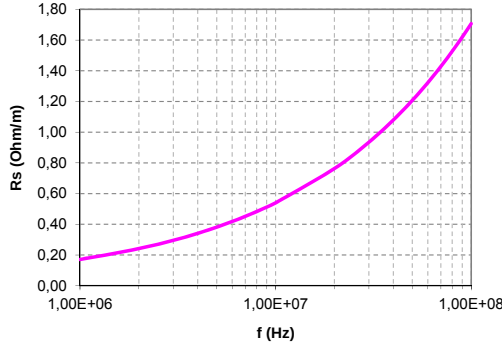


Figure A.1 – Surface resistance per unit length as a function of frequency.

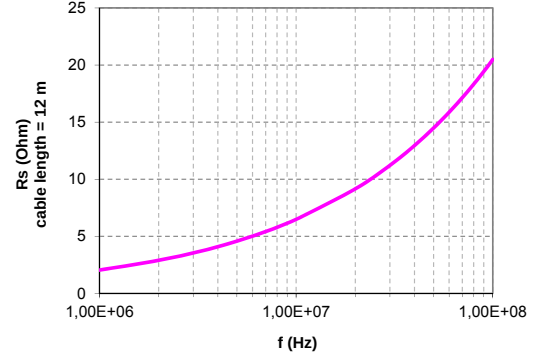


Figure A.2 – Surface resistance as a function of frequency for a 12m cable

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \quad (\text{A.1})$$

where $\mu = 4\pi \times 10^{-7}$ H/m is the magnetic permeability and ρ its permeability. The series resistance of a conductor and its inductance increase at high frequencies. The internal impedance of the conductor is given by

$$Z_S = R_S + j\omega L_i \quad (\text{A.2})$$

where R_S and L_i are the resistance and the inductance per unit length, respectively. It can be shown [34] that

$$L_i = \frac{R_S}{\omega} \quad (\text{A.3})$$

Assuming all conductor thicknesses much larger than the penetration depth, the resistance per unit length is

$$R_S = \frac{1}{\pi D} \sqrt{\frac{\omega\mu\rho}{2}} \quad (\text{A.4})$$

The resistance per unit length R_S can be calculated from the equations shown and the information provided by the cable manufacturer. In Fig. A.1 the cable resistance due to skin effect is plotted as a function of the frequency.

It can be shown that the internal cable impedance becomes:

$$Z_S = \frac{\sqrt{\mu\rho}}{\pi D} \sqrt{j\omega} \quad (\text{A.5})$$

Applying the transmission line model based on the telegrapher's equations, the general expression for the characteristic impedance of a transmission line for high

ω is:

$$Z_0 = \sqrt{\frac{Z_S + j\omega L}{j\omega C}} \simeq \sqrt{\frac{L}{C}} \quad (\text{A.6})$$

The propagation constant is:

$$\gamma = \sqrt{(Z_S + j\omega L) j\omega C} \simeq \frac{\sqrt{\mu\rho}}{2Z_0 W} \sqrt{j\omega} + \sqrt{LC} j\omega \quad (\text{A.7})$$

The transfer function of a length of line is then:

$$\frac{V(x+l, \omega)}{V(x, \omega)} = e^{-\gamma l} = e^{-\frac{\sqrt{\mu\rho} l}{2Z_0 W} \sqrt{j\omega}} e^{-\sqrt{LC} l j\omega} \quad (\text{A.8})$$

The second exponential describes a pure delay and will be disregarded in the following discussion. The first exponential describes the waveform distortion due to skin effect. Its inverse Fourier transform gives the line delta response in the time domain Inverse Fourier transform:

$$h(t) = \frac{\tau_0}{2\sqrt{\pi}} t^{-\frac{3}{2}} e^{-\frac{\tau_0}{4t}} U(t) \text{ with } \tau_0 = \frac{\sqrt{\mu\rho} l}{2Z_0 W} \quad (\text{A.9})$$

where τ_0 is the "cable rise time" and U the Heavyside unity step. More interesting is the step response of the transmission line, obtained by integration of eq. A.9 And the step response of the transmission line:

$$u_1(t) = \text{erfc} \left[\frac{1}{2} \sqrt{\frac{\tau_0}{t}} \right] \quad (\text{A.10})$$

where $\text{erfc}(x) = 1 - \text{erf}(x)$ is the complementary error function. The major effect is the introduction of long time constants in the system which cause a strong attenuation of the shaped signal.

A.3 Impedance after the cable

In this section, a study of the impedance after the cable, at the Front-end input, is presented when the detector impedance is the corresponding to PMT and a clipping line (detector impedance $Z_d = R_d$). Rearranging the propagation constant from equation A.11

$$\gamma = \frac{R_S(\omega)}{2R_0} + j \frac{\omega}{v_p} \quad (\text{A.11})$$

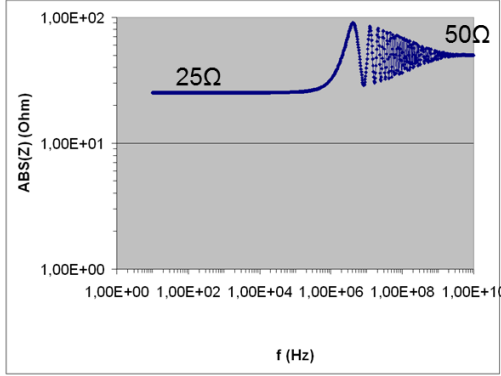


Figure A.3 – Impedance module for a 12m cable.

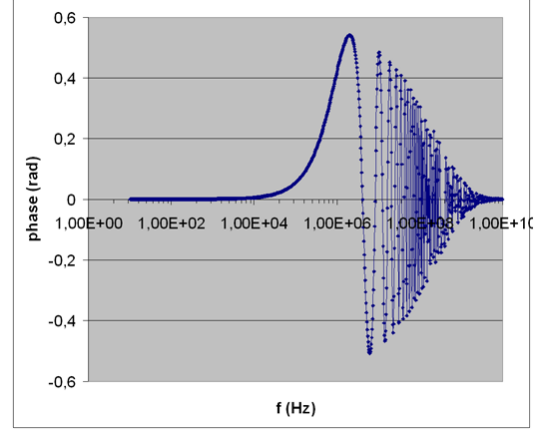


Figure A.4 – Impedance phase for a 12m cable

where v_p is the phase velocity of the electromagnetic wave. Then, the impedance seen at position x towards the detector is

$$Z(x, \omega) = R_0 \frac{R_d + R_0 \tanh(\gamma x)}{R_0 + R_d \tanh(\gamma x)} \quad (\text{A.12})$$

where $R_0 = 50\Omega$ is the impedance of the cable and $R_d = 25\Omega$ is the impedance of the detector (due to the clipping).

As expected, for very short cables, the impedance at the end of the cable is almost unaffected by it and is essentially equal to the detector impedance $Z \simeq Z_d$. In the other extreme situation, for very long cables, the impedance observed is mainly the same as the one of the cable, $Z \simeq Z_0$.

In the case of the LHCb Calorimeter, the cables are about 12m long. The impedance seen after this distance of cable towards the detector is then:

- $f < 2 - 3\text{MHz} \rightarrow |Z| \sim R_d$ (as without the cable).
- $2 - 3\text{MHz} < f < 1\text{GHz} \rightarrow |Z|$ oscillates between 25 and 100Ω .
- $f > 1\text{GHz} \rightarrow |Z| \sim 50\Omega$.

The module and phase of the impedance seen at the Front End electronics (i.e. with a 12m cable) are presented in Figs. A.3 and A.4, respectively.

A.4 Noise contribution due to skin effect

The noise generator per unit length associated with a length dx of line is:

$$e_{n,l}^2(\omega) = 4KTR_S(\omega) \quad (\text{A.13})$$

The noise corresponding to a 12m cable is presented in Fig. A.5. We can apply a fast shaping times approximation which allows to model the skin effect noise by a single noise generator at preamp input and a lumped element with an approximated value at the channel (preamplifier and shaper) central frequency, $R_S \simeq 18\Omega$ (Fig. A.2).

The noise current per unit length through a the terminating resistor R_0 at the

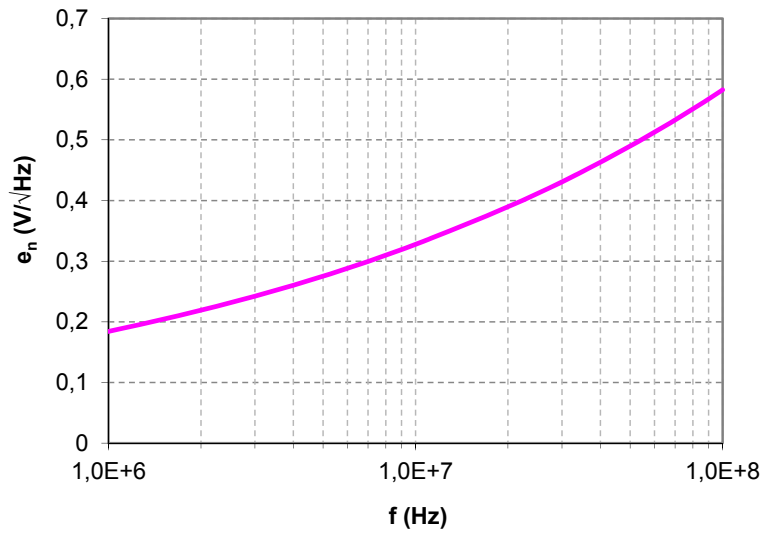


Figure A.5 – e_n noise calculations due to cable skin effect.

Front End:

$$i_{n,l}^2(x) = e_{n,l}^2 \frac{1}{|Z(x, \omega) + R_0|^2} |e^{-\gamma(l-x)}|^2 \quad (\text{A.14})$$

where $e_{n,l}$ is defined in Eq. A.13, R_S in Eq. A.4, γ in Eq. A.11 and Z in Eq. A.12. The total noise current can be, then, computed by integration along the length of the line, from the detector to the preamp:

$$i_n^2(\omega) = \int_0^l i_{n,l}^2(x) dx \quad (\text{A.15})$$

The case of a 12m cable (shown in Fig. A.6) is:

$$i_n^2(\omega) = \frac{e_{n,l}^2}{4R_0^2(R_0 + R_d)^2} \left[(R_0 + R_d)^2 \frac{1 - e^{-4\alpha l}}{2\alpha} + R_0 R_d \frac{e^{-4\alpha l} - 2e^{-2\alpha l} + 1}{\alpha} + (R_0^2 + R_d^2) e^{-2\alpha l} \frac{\sin 2\beta l}{\beta} \right] \quad (\text{A.16})$$

It is worth mentioning that the calculations are correct for frequencies clearly above the corner frequency f_C , defined as the frequency at which skin depth equals the conductor's width. A $f_C = 18.4\text{kHz}$ is expected for the detector cables.

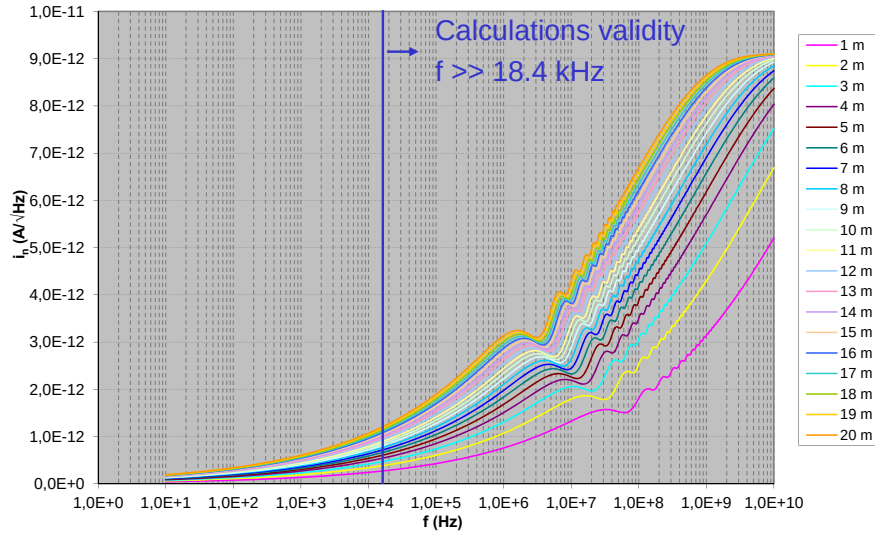


Figure A.6 – i_n^2 noise calculations due to cable skin effect.

If we take into account the preamplifier, the PSD of the cable due to the skin effect:

$$e_{no}(\text{cable}) = Z_T i_n \quad (\text{A.17})$$

where the preamp transimpedance gain is $Z_T \simeq 500\Omega$.

So, the current noise can be obtained from the calculations (Fig. A.6) or using the lumped resistor approximation ($R_S \simeq 18\Omega$):

$$i_{ni}^2|_{e_{tR_S}} = \frac{4KTR_S}{|R_S + Z_0|^2} \quad (\text{A.18})$$

Apart from the calculation, it is also possible to obtain the cable skin effect noise from simulations using the *mtline* cell in the Cadence Spectre software. The characteristics used in the cell were obtained from a Lemo cable data sheet and are listed in Table A.1. Simulation results in Fig. A.8 show the noise respect the frequency for different lengths. As expected, the out PSD is more important for longer cable lengths and higher frequencies.

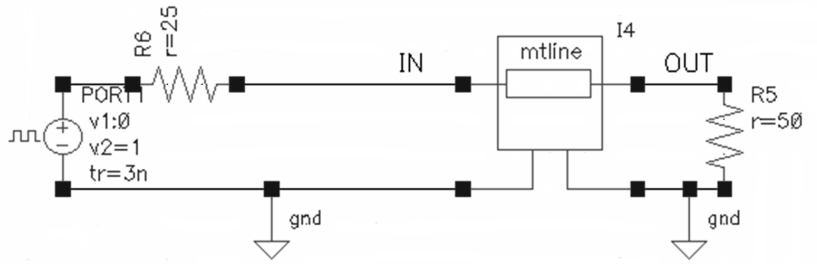


Figure A.7 – Cadence Spectre simulations of the cable using the cell *mtline*.

Table A.1 – Parameters to be configured in the *mtline* cell.

Parameter	Name	Value
Cable physical length	l	12m
Normalized velocity	v	0.659 c
Corner frequency	f_{corner}	18.446kHz
DC series resistance per unit length	R_{DC}	0.031Ohm/m
Conductor loss measurement frequency	f_C	200MHz
Conductor series resistance per unit length at f_C	R_S	2.411 Ohm/m

Fig. A.9 plots the different methods already described to obtain the noise of the cable skin effect: calculation, simulation and the R_S lumped approximation. It can be observed that simulated and calculated noise are almost the same for frequencies above the corner frequency, which is the point from which the calculations are expected to be correct. Also, the approximation of the lumped element overestimates the noise except for high frequencies, so it can be adopted as a su-

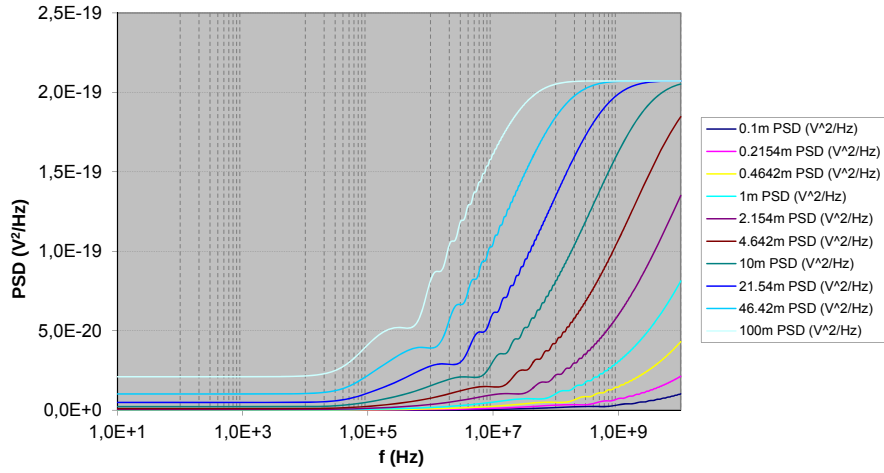


Figure A.8 – Cadence Spectre simulations of the cable noise for different lengths (from 0.1 to 100m) using the cell *mtline*.

perior limit for our system.

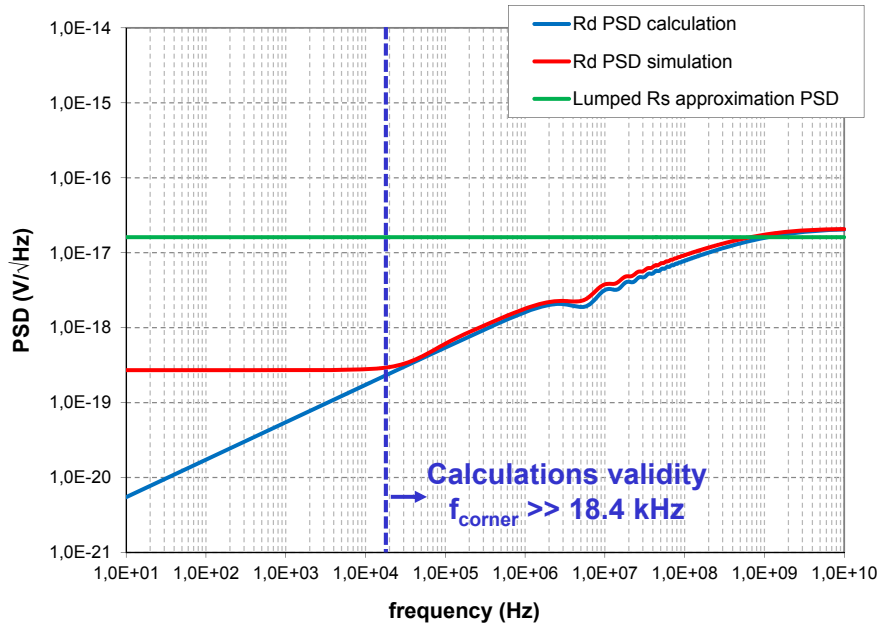


Figure A.9 – Comparison of the different ways of obtaining the PSD for a $Z_d = R_d$ and a cable of 12m: calculation, simulation, and $R_S = 18\Omega$ lumped approximation.

Detailed pinout

The detailed pinout is defined in table [B.1](#):

Table B.1 – Pin function description.

Pin number	Mnemonic	Description
1, 16, 17, 64	VRef_0TPZ	0T and Pole/Zero voltage reference.
2, 5, 11, 14	IFE+ < 0 : 3 >	Noninverting differential Input. Typically ac-coupled.
3, 6, 12, 15	IFE− < 0 : 3 >	Inverting differential Input. Typically ac-coupled.
4, 9, 13, 19, 62	GND_0TPZ	Exposed Pad is internally connected to GND and must be soldered to a low impedance ground plane.
7, 10, 18, 63	VCC_0TPZ	Positive 3.3 V power supply for 0T and Pole/Zero.
8, 60	NC	Not connected.
20	VCML_0TPZ	0T and Pole/Zero Common Mode Voltage.
21	VBias_Ref	Bias voltage of the chip to be connected to a decoupling capacitor.

Continued on next page

Table B.1 – *Pin function description (Continued from previous page).*

Pin number	Mnemonic	Description
22, 59	VRef_ITH	Integrator and Track-and-Hold voltage reference.
23, 58	VCC_ITH	Positive 3.3 V power supply for Integrator and Track-and-Hold.
24, 57	GND_ITH	Exposed Pad is internally connected to GND and must be soldered to a low impedance ground plane.
25, 27, 54, 56	OFE+ < 3 : 0 >	Non-inverting differential output. Typically ac-coupled.
26, 28, 53, 55	OFE– < 3 : 0 >	Inverting differential Output. Typically ac-coupled.
29, 52	VCC_DIG	Positive 3.3 V power supply for the digital blocks (slow control and delay line).
30, 51	GND_DIG	Exposed Pad is internally connected to GND and must be soldered to a low impedance ground plane.
31	RST	Chip reset (active high). Resets the SPI interface, restores the default value of serial registers and resets the charge pump of the delay line.
32	BXIDRST_SYN	Outputs the BXID synchronous reset signal resynchronized by the input reference clock. For testing purposes.
33, 35, 45, 47	ClkADC– < 3 : 0 >	Inverting LVDS Output Clock to synchronize the external ADC data sampling. A termination resistor of 100Ω is required between inverting and non-inverting pins.

Continued on next page

Table B.1 – *Pin function description (Continued from previous page).*

Pin number	Mnemonic	Description
34, 36, 46, 48	ClkADC+ < 3 : 0 >	Non-inverting LVDS Output Clock to synchronize the external ADC data sampling. A termination resistor of 100Ω is required between inverting and non-inverting pins.
37	SPI!SS	SPI slave select. Input signal. Active low.
38	SPIMISO	SPI Master Input / Slave Output. External pull-up resistor of 500Ω.
39	SPIMOSI	SPI Master Output / Slave Input.
40	SPISCLK	SPI Serial Clock. Input signal.
41	SPIRefresh	SPI Auxiliary Clock. Used to refresh TMR registers and correct SEUs (if any) during data taking. Input signal.
42	BXIDRST	BXID synchronous reset signal that allows sub-channel identification. Input signal.
43	ClkIn-	Inverting LVDS Input Clock reference.
44	ClkIn+	Noninverting LVDS Input Clock reference.
49	VCoarse	Delay line external coarse adjust. Input signal.
50	VControl	Delay line internally generated control voltage. Output signal. For testing purposes.
61	VCM_ITH	Integrator and Track-and-Hold Common Mode Voltage.

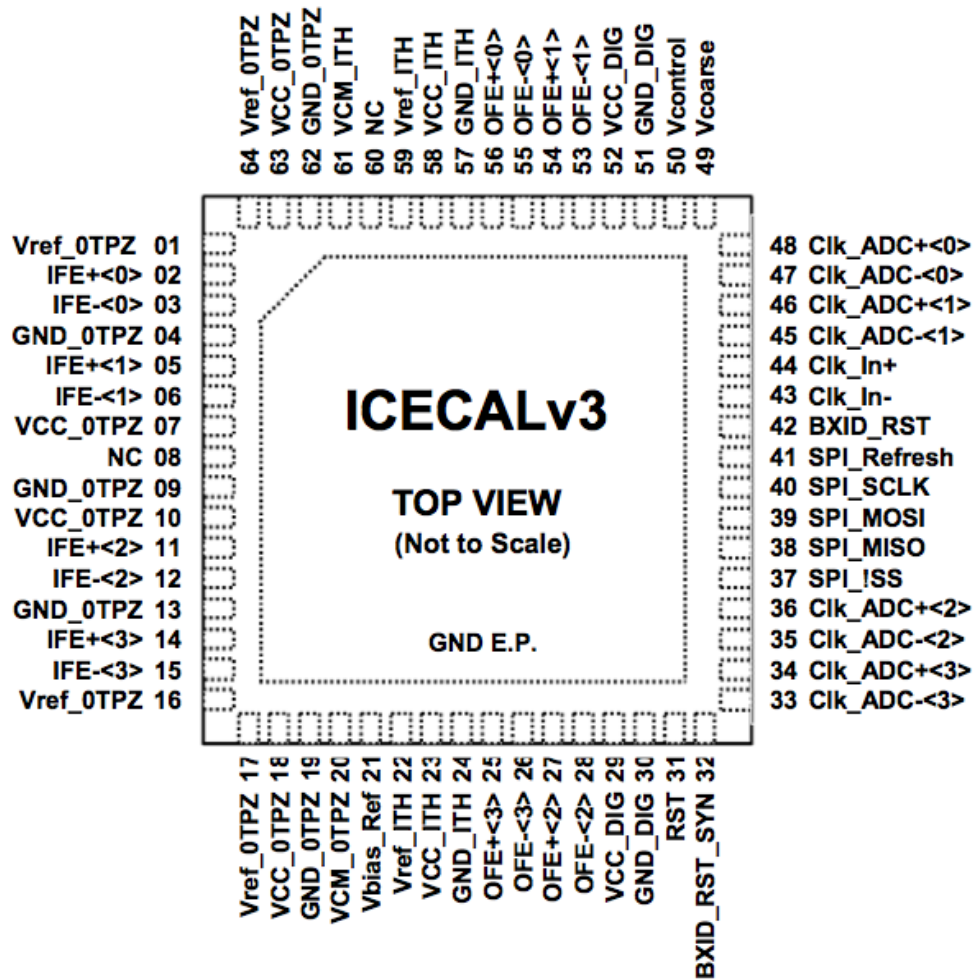


Figure B.1 – ICECALv3 pin configuration reviewed.



SPI interface and registers

The present appendix contains the tables that define the slow control frames and the configuration registers addresses and bit functions.

- Table C.1 defines the values of the 8-bit SPI address frames.
- Tables C.2 lists the address for each status register.
- Table C.3 list the exact address for each of the configuration register.
- The main control register of the chip is described in table C.4.
- The different bias currents used at each stage of the channel are exposed in Table C.5.
- The analog channel register contains the corresponding bits to control the key parameters and compensate for process variations (Table C.6).
- A delay line channel configuration register is defined for each analog channel. The values of each clock line used is defined in Table C.7.

Table C.1 – Slow control frame types according to the SPI address bits.

Description	R/!W (b ₇)	PUMP _{RST} (b ₆)	!CONF (b ₅)	REG _{SEL} <4:0> (b _{4:0})
Soft Reset	0	1	0	X
SPI Bypass	1	1	1	0x1F
Status Register	1	0	1	X
Config. Register	X	0	0	X

Table C.2 – Status registers address mapping.

Description	REG _{SEL} <4:0>	Function
ICECAL version	0×10	Bits <15:12> ICECAL major revision number. Bits <11:8> ICECAL minor revision number.
BXID resynch	0×11	Bit 15 returns 1 if the synchronous BXID _{RST} signal (pin 42) is being properly resynchronized with the input reference clock (pins 43 and 44).

Table C.3 – Configuration registers address mapping.

Description	REG _{SEL} <4:0>
Analog Ch0<15:0>	0×00
Analog Ch1<15:0>	0×01
Analog Ch2<15:0>	0×02
Analog Ch3<15:0>	0×03
Analog Ch0<31:16>	0×04
Analog Ch1<31:16>	0×05
Analog Ch2<31:16>	0×06
Analog Ch3<31:16>	0×07
Main<15:0>	0×08
Main<31:16>	0×09
Main<47:32>	0×0A
Main<63:48>	0×0B
Delay Line Ch0	0×1C
Delay Line Ch1	0×1D
Delay Line Ch2	0×1E
Delay Line Ch3	0×1F

Table C.4 – ICECAL main register bits function and default values.

Name	Bits	Default value	Function
$\text{!}V_{\text{Control_EN}}$	63	0x0	This bit enables/disables control voltage output pin (59). Active low.
$\text{!}BXID_{\text{Syn_EN}}$	62	0x0	Enables or disables the output debug pin $BXID_{\text{RST_SYN}}$ (32). Active low.
$\text{!}Clk_{\text{Refresh_EN}}$	61	0x0	Enables or disables clock refresh of the TMR registers. If enabled, auxiliary clock pulses coming from SPI_{Refresh} pin (41) will be forwarded to the serial registers while SPI slave is idle. Otherwise, two consecutive SEUs on the same TMR register might cause data corruption. Active low.
	60		Not Used.
$I_{\text{Bias_OB}}$	59:54	0x29	Output buffer bias.
$I_{\text{Bias_CETH}}$	53:48	0x27	Track-And-Hold OpAmp bias.
	47:44		Not Used.
$I_{\text{Bias_TH}}$	43:38	0x1E	Track-And-Hold OpAmp bias.
$I_{\text{Bias_INT}}$	37:32	0x1E	Integrator OpAmp bias.
	31		Not Used.
$I_{\text{Bias_CEINT_H}}$	30:28	0x3	3 MSB of the integrator OpAmp bias.
$I_{\text{Bias_CEPZ}}$	27:22	0x11	Pole-Zero OpAmp bias.
$I_{\text{Bias_0T}}$	21:16	0x1E	0T bias.
	15		Not Used.
$I_{\text{Bias_CEINT_L}}$	14:12	0x4	3 LSB of the integrator OpAmp bias.
$I_{\text{Bias_PZ}}$	11:6	0x1E	Pole-Zero OpAmp bias.
$I_{\text{Bias_V0T}}$	5:0	0x1C	0T bias.

Table C.5 – Biasing the different channels.

Stage	Bias	p/n	$\times m$	Value	Ib (μA)	IbMax (μA)
OT	Ib	p	6	30	435	810
OT	IbV	p	1	28	75	135
PZ	IbPZ	n	3	30	210	405
PZ	IbCEPZ	n	4	17	390	540
Int	IbInt	n	3	30	210	405
Int	IbCEInt	n	4	28	300	540
TH	IbTH	n	3	30	210	405
TH	IbCETH	n	6	39	310	810
OB	IbOB	p	1	41	15	45

Table C.6 – ICECAL channel control register bits function.

Name	Bits	Default value	Function
Cint _{MSB}	31:30	0x1	Integrator capacitor 2 MSB common for both sub-channels.
Cint _{LSB0}	29:27	0x7	Integrator capacitor 3 LSB for sub-channel 0 only.
Cint _{LSB1}	26:24	0x7	Integrator capacitor 3 LSB for sub-channel 1 only.
IOff _{MSB}	23:20	0xA	Offset current 4 MSB common for both sub-channels.
IOff _{LSB0}	19:18	0x0	Offset current 2 LSB for sub-channel 0 only.
IOff _{LSB1}	17:16	0x0	Offset current 2 LSB for sub-channel 1 only.
Zero	15:11	0x5	Capacitor bits for the zero of the PZ filter. Zero frequency ranges from 12.84 MHz to 42.78 MHz.
Pole	10:5	0x8	Capacitor bits for the pole of the PZ filter. Pole frequency ranges from 13.10 MHz to 106.10 MHz.
Z _{In}	4:0	0x13	Input impedance control.

Table C.7 – Delay Line channel control register.

Name	Bits	Default value	Function
Phase _{ADC}	15:11	0x00	ADC clock delay in ns.
Phase _{TH}	10:6	0x00	TH clock delay in ns.
Phase _{INT}	5:3	0x2	Integrator clock delay in ns. This clock signal is referenced to the TH clock. Hence, a 2ns Integrator clock delay means 2ns between TH clock rising/falling edge and Integrator clock rising/falling edge.
L _{OCSEL}	2:1	0x0	LVDS clock output current selector. 0x0: 3.0 mA ($V_D = \pm 150\text{mV}$) 0x1: 2.3 mA ($V_D = \pm 115\text{mV}$) 0x2: 1.4 mA ($V_D = \pm 70\text{mV}$) 0x3: 0.35 mA ($V_D = \pm 17.5\text{mV}$).
LVDS _{OEN}	0	0x1	This bit enables/disables the LVDS clock output that drives the ADC.

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