



UNIVERSITY OF AGDER

A reliability analysis of the BLEAC signal acquisition card for the LHC injectors

Vegard Joa Moseng

Supervisors:

William Viganò (CERN)

Arild Haglund (UoA)

Linga R. Cenkeramaddi (UoA)

CERN-THESIS-2014-053
27/05/2014



Date: 27.05.2014

University of Agder, 2014
Faculty of Engineering and Science
Department of Information and Communication Technology



This work has been carried out as part of the Technical Student Programme at the European Organization for Nuclear Research, CERN, Geneva, Switzerland.

Abstract

As a required part of an Electronics and Mobile Communications Bachelor's degree at the University of Agder, all students have to complete a Bachelor's Thesis within the framework of a course named ELE300, in order to obtain their degree. This Thesis is thus my effort to complete this course. The Bachelor's Thesis was done as part of a Technical Student Programme, which was provided by the European Organization for Nuclear Research, CERN, and was hosted at their particle physics laboratory in Geneva, Switzerland. This Thesis describes the work that was done to obtain the best approach for completing the Bachelor's Thesis within the guidelines of the University of Agder, and the requirements given by CERN as the task giver.

The task was to make a number of reliability analyses in order to estimate the overall reliability of a new mission critical beam loss monitoring system which is being developed for the new particle accelerator injector system located in the laboratory's particle accelerator complex. This system is a quite sophisticated electronics acquisition system which incorporates both analogue and digital electronics and works by acquiring, processing and publishing the results from the numerous beam loss monitors located on the accelerators. The task required the use of system reliability theory to calculate the reliability for the electronics on a hardware level, and thus also a decent understanding of the behaviour of analogue circuits. The need for this analysis was based on the criticality of the continuous protection during operation of the LHC injectors.

Acknowledgements

This work could not have been done without the help of my CERN supervisor, William Viganò. First and foremost for allowing me the opportunity for working at CERN, and for his guidance and support during my stay. Thank you for sharing your knowledge about electronics, for helping me with my Thesis work, and for showing me so many things in the lab and on the site. For all of this I am and will be, extremely grateful.

I also want to say thank you to the rest of the people in my section, who were really friendly and helpful, both about work and non-work related topics. I really enjoyed being surrounded by you and will miss my time there.

My stay at CERN required a lot of small and big special treatment, which the people at my university were very generous to provide. I therefore have to say a big thank you to the people at the University of Agder, who helped me and gave me the opportunity to focus my attention on CERN.

Last but not least I have to say a huge thank you to all the friends from all over Europe that I made at CERN. Thank you for making the life in Geneva so incredible enjoyable. For all the picnics, trips, parties, dinners and events, it's hard to land in normal life after such an amazing year.

Kristiansand,
Vegard Joa Moseng

27.05.2014

Contents

1	Introduction	2
1.1	About CERN	2
1.2	The task	3
1.3	Planning and Premises	4
1.4	ELE 300	9
1.5	Project organisation	9
1.6	The accelerator complex	10
2	Beam Loss Electronics	11
2.1	Beam loss detection systems	11
2.2	Beam Loss Monitoring system for the LHC injectors	12
2.3	Reliability aspect for the BLMs on the system level	14
2.4	Beam Loss Electronics Acquisition Crate	15
2.5	Beam Loss Electronics Double Polarity card	17
2.5.1	Circuit breaker	19
2.5.2	Input monitor	20
2.5.3	ADC-channel	22
2.5.4	Filters & Protection	23
2.5.5	Power supply	24
2.5.6	Connectors	25
2.5.7	Relays & Calibrations	26
2.5.8	Misc. circuits	27
2.5.9	FPGA	28
2.6	Detectability and severity ranking	30
2.7	Crosstalk protection	33
3	Reliability	34
3.1	Introduction	34
3.2	Definition of reliability	35
3.3	Basic concepts	36
3.4	Software	38
3.5	Prediction	39
3.5.1	Project parameters for the Prediction	40
3.5.2	Prediction module report structure	41
3.6	FMECA	43
3.6.1	Rationale for choosing to use the FMECA	44
3.6.2	Tailoring the FMECA	44
3.6.3	Project parameters for the FMECA	46
3.6.4	FMECA module	47
3.6.5	FMECA report structure	47
3.7	Fault Tree Analysis	48
3.7.1	Project options and structure for the FTA	49
3.7.2	Constructing the FTA	50

4	Results and conclusion	51
4.1	Results from the Prediction	51
4.2	Results from the FMECA	52
4.3	Results from the FTA	53
4.4	Conclusion	54
5	References	55
6	Appendix	56
6.1	Literature list	57

List of Figures

1	CERN member states.	2
2	Plan for how to construct the methodology.	4
3	Main work aspects.	5
4	Divide and conquer strategy to minimize complexity.	6
5	Levels of protection for the core functionality.	7
6	Process leading up the reliability analyses.	8
7	CMS, the second largest detector at CERN.	10
8	CERN accelerator complex.	10
9	Detectors (yellow) on the LHC.	11
10	Block diagram of the signal propagation.	12
11	A unit of CERN's Beam Loss Monitoring system. [1]	13
12	Scope of the reliability analysis.	14
13	Prototype BLEAC crate.	15
14	Power supply handling [1].	16
15	Beam loss monitors to BLEDP cabling [1].	16
16	List of all 49 individual sub-blocks in the BLEDP.	17
17	The block system.	18
18	Circuit of the Circuit Breaker.	19
19	Reliability values and summary for the Circuit Breaker.	19
20	Combination algorithm plot [1].	20
21	Input monitor block diagram [1].	20
22	Reliability values and summary for the Input Monitor.	21
23	ADC circuit.	22
24	Reliability values and summary for the ADC-channel.	22
25	Filters and protection circuit with connectors.	23
26	Reliability values and summary for the Filters & Prot.	23
27	Circuit of the on-board Power supply.	24
28	Reliability values and summary for the Power supply.	24
29	Circuit of the SFP and I2C Connectors.	25
30	Reliability values and summary for the SFP and I2C Connectors.	25
31	Circuit of the Relay Activation and Status.	26
32	Reliability values and summary for the Relay Activation and Status.	26
33	Miscellaneous circuits.	27
34	Reliability values and summary for Miscellaneous circuits.	27
35	Circuit of the FPGA and support components.	28
36	Reliability values and summary for Miscellaneous circuits.	29
37	Consequences of main failure types.	30
38	Severity matrix for the BLEDP, using RPN.	31
39	State progression of the BLMs hardware checks.	32
40	Crosstalk [1].	33
41	Isograph GUI and the parameters for a ceramic capacitor	38
42	Project tree	39
43	Project options	40
44	Prediction report example	41
45	A 'Most significant failure rate' diagram example	42
46	Example of a FMECA worksheet	43

47	FMD-91 failure mode distribution example	45
48	Project options	46
49	Interface of the FMECA-module.	47
50	Report structure of the FMECA.	47
51	Example of the FTA structure.	48
52	Fault Tree Analysis-module options.	49
53	Construction of a FTA.	50
54	The various MTTF-values which makes up the BLEDP-card, on a logarithmic scale.	51
55	Bathtub curve.	51
56	FTA of the blind failure and maintenance.	53
57	FTA of the false dump.	53

List of Acronyms:

CERN - Conseil Europeen pour la Recherche Nucleaire
 BLEAC - Beam Loss Electronics Acquisition Crate
 BLEPC - Beam Loss Electronics Processing Crate
 BLM - Beam Loss Monitors
 LHC - Large Hadron Collider
 eV - Electron Volts
 LINAC 2 - Linear Accelerator 2
 PSB - Proton Synchrotron Booster
 PS - Proton Synchrotron
 SPS - Super Proton Synchrotron
 LS1 - Long shutdown 1
 FPGA - Field-programmable gate array
 BIS - Beam Interlock System
 BLEDP - Beam Loss Electronics Double Polarity card
 ADC - Analog to Digital Converter
 ECTS - European Credit Transfer and Accumulation System
 MTTF - Mean time to failure
 MTBF - Mean Time Between Failures
 FMEA - Failure Modes and Effects Analysis
 FMECA - Failure Modes, Effects and Criticality Analysis
 FTA - Fault Tree Analysis
 FFT - Fast Fourier Transform

Preface

The process, methodology and results of these analyses are documented here, and is the foundation of my Bachelor's Thesis. As a consequence of the general similarities in methodology between the different parts of the BLEAC, as well as the higher circuit complexity, this Thesis is limited to the study of an electronics card in the acquisition crate called the Beam Loss Electronics Double Polarity card (BLEDP). My attempt is to describe the process of the work and the development of the methodology used, by dividing the Thesis into three main parts which builds on each other hierarchically.

Section 1 is a superficial introduction to CERN and it's particle accelerators so that it may help explain the needs and challenges surrounding this system, as well as help describe the organisational aspects of the work. It also describes the task, how I planned the work and the premises as given to me. I've also written a short overview of the project organisation.

Section 2 is about the electronics. Here I have written an introduction to beam loss detection systems, and used that to show how CERN's Beam Loss Monitoring system is built from that. I've also written a description of the BLEAC, it's cards and functionalities, so that the consequences of failures on a system wide viewpoint could be explained. I have then put in a detailed description of the electronics card, BLEDP. Here I go over the functionalities, and write a short summary of some of the numbers in the analysis. I have added some of the checks used for detection, in order to explain the "defence system" against critical failures.

In Section 3 I have written a short introduction to reliability, a little bit of it's history and general usage. I have added a definition and explanation of what it is, and some of the basic mathematical concepts used in reliability theory, and this work by proxy. After that I have explained the software used, and the three different modules within the software; how they work, what options I used and how the analyses are constructed.

In the last main section, Section 4, I have added an assessment of the results from the reliability analyses, and written a conclusion.

Section 5 holds the references used.

The appendix hold all the things I have not included in the report, such as the analyses, the circuit diagrams and a list of literature.

The Thesis is a little over 25000 words, but as it is for 30 ECTS credits, and a big topic, it was needed. I would also like to note, that the Thesis is also intended for documentation at CERN, for future analyses in the system. So the design and explanation is serving two purposes and might differ a little bit from a standard Thesis because of this.

1 Introduction

Here follows a short description of CERN [2], its mission, some of its scientific research and the scientific tools being used. It also describes some of the organisational aspects of the work I did by explaining the Technical Student Programme briefly and the general project organization. This is to help describe the circumstances for this work.

1.1 About CERN

The European Organization for Nuclear Research, to many known by its French acronym CERN, is a large international research collaboration which conducts research on the fundamental structure of the universe. It's mission includes hosting a large number of engineers and physicists who study the basic constituents of matter - the elemental particles.

CERN is located right on the French-Swiss border in Geneva, Switzerland, and was officially founded in 1954 as an intergovernmental European science collaboration. Not long after its founding it grew from the original 12 member states (one of which was Norway) to today's 20 member states. The reason it required such a large collaboration was because particle physics was getting so complicated, and the research instruments so large and expensive, that no single country in Europe could reasonably build and maintain one alone. In addition to a few states which are in the pre-membership stage, there are more than 600 institutes and universities from over 110 different countries who contribute to the scientific research as users of CERN's facilities. As a result of this, CERN continuously host more than 10.000 visiting scientists and engineers, in addition to its around 2500 permanent staff. For this reason, as well as its historic successes, its counted as one of the largest and most respected centres for scientific research in the world.



Figure 1: CERN member states.

During the last 60 years, scientists at CERN have made several important discoveries such as: producing and trapping very small amounts of anti-hydrogen which was also the first creation of antimatter in a lab; discovering a few new elemental particles such as the W- and Z-boson; and just now in 2012, discovering one of the most sought after particles in physics - a Higgs-boson. This led to a Nobel Prize in Physics in 2013 for the scientists who first proposed it's possible existence. In addition CERN is also famous for being the birthplace of the World Wide Web and for keeping it royalty free.

Note: CERN has nothing to do directly with Nuclear Research and is therefore often called the European Laboratory for Particle Physics to avoid confusion.

1.2 The task

This Thesis is the end result of my Technical Student Programme which I conducted at CERN, the European Organization for Nuclear Research, over 14 months from January 2013 to the end of February 2014. CERN, located in Geneva, Switzerland, is the host of the largest particle accelerator complex in the world and with the completion of the Large Hadron Collider (LHC) in 2008, the series of accelerators are also counted as one of the biggest and most complex machines ever constructed. Its purpose, as the pillar-stone of a huge international scientific collaboration, is to provide scientists with the tools needed to study the basic constituents of matter; the fundamental particles, how they interact, and how they connect with the fundamental laws of nature.

The particle accelerators are used to accelerate particles, here protons and heavy ions, to almost the speed of light before they are made to collide inside massive detector experiments. These experiments studies the aftermath of the collisions by looking at the elemental particles that are ejected out of the protons and ions. As a result of the potentially damaging energy which can be released locally by particles colliding with items such as the accelerator magnets, a lot of work is put into the safe detection and prevention of debilitating or catastrophic losses. At CERN, this is done by the successful operation of a custom designed detection system. This system is known as the Beam Loss Monitoring system (BLMs) and it's job is to acquire information about losses through detectors which are placed at strategic locations around the accelerators. It then processes and sends the information to a special interface system which can order a safe particle dump by sending the accelerated particles smashing into special carbon blocks at the end of a tunnel going into the mountain.

One such BLM system is currently under development and implementation for the LHC injectors. A part of this new system, called the Beam Loss Electronics Acquisition Crate (BLEAC), is the first step in the processing chain and is, along with the rest, considered mission critical. Due to this, a number of safety and integrity preserving measurements have been put in place during the design process. To complement this, it was suggested to add a complete reliability analysis in order to systematically validate the reliability of the system. I was invited, though the aforementioned programme, to conduct this reliability analysis on this crate. For this Thesis, one of the electronics cards in the crate has been selected by me to demonstrate the reliability process within the frameworks of my university degree. The card chosen is the Beam Loss Electronics Double Polarity card, as it is the best fit for the requirements related to the size and complexity of the Bachelor's Thesis.

The task was to use three specific analyses:

- MTTF Prediction - Mean Time To Failure.
- FMECA - Failure Mode, Effects and Criticality Analysis.
- FTA - Fault Tree Analysis.

A suitable software, Isograph Reliability Workbench 11 [3], had already been acquired, and was to be used for the reliability analyses. Also a military handbook, MIL-HDBK-217, had been pre-selected for the work, and was to be used as the foundation for the calculation of the failure rates.

1.3 Planning and Premises

The Technical Student programme is a programme targeted at engineering and applied physics students, and gives successful candidates the opportunity to come and spend between 6 to 12 months at CERN as a technical intern. The programme itself, considered highly competitive, has two annual intakes which results are decided on by a selection committee. It's a requirement that the student is enrolled in a university programme, and it's also common that the end result of the Technical Student programme will be used in a Bachelor's or Master's Thesis. Once a student has been selected, he or she is presented with the task and if the student and project stakeholders agree on the terms, the student will be given a contract.

I was very fortunate to be asked to perform a reliability analysis on an electronics project that was under design and construction at CERN. However, as reliability is a rather complementary field within engineering, it's not generally something which is studied in detail at most engineering undergraduate programmes, at least in Norway. I was therefore not sufficiently acquainted with the theories and practices of reliability from beforehand, as expected. So, once I started at CERN, I had to create a plan for how to acquire the competences I needed in order to complete my task.

The planning structure I created is as follows:

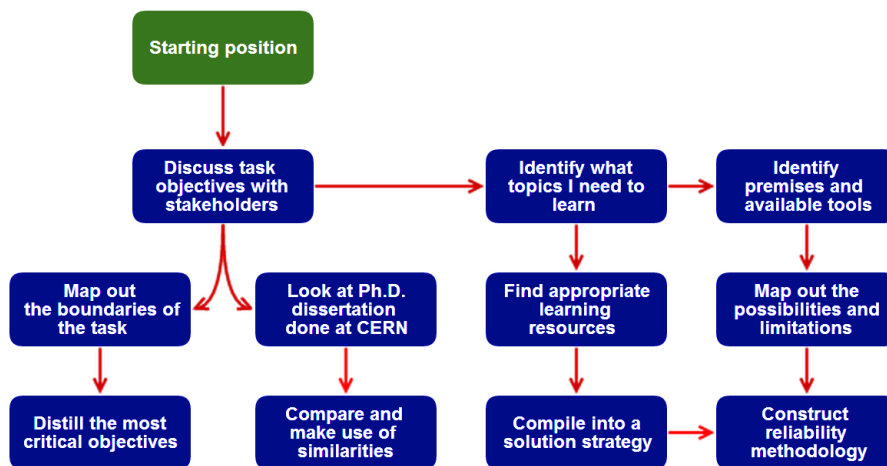


Figure 2: Plan for how to construct the methodology.

As with most projects, the most important aspect for me to begin with was of course to make sure I understood what the task entailed. And so, as this was a complicated task with many large topics, this meant to first and foremost get a general understanding of what the main goals consisted of, as well as what the most critical objectives were. This was done by discussing the project with the stakeholders, mainly the designer and the project leader. In addition, I was also given a Ph.D. Thesis which was conducted at CERN on the topic of reliability for the LHC. I was subsequently asked to make comparisons between the tasks, and extract relevant similarities, especially related to the methodology. Incidentally, as my project progressed, our methodologies didn't correlate very well since I was performing my analyses on all individual components, while the previous work was more focused on key parts and bigger blocks due to its larger scale.

So in the end, although we independently ended using similar approaches, the differences in scale and purpose were too big to make any big extrapolations in terms of methodology, outside of what was already a part of the task description. In addition, as the previous work was done almost 10 years earlier, there were a lot structural changes now related to the software we used, which also made it more difficult to use the older work as a distinctive foundation, although it of course was useful as a case example. Consequently, for the most part I constructed a different methodology based on the specific challenges and goals for this work, and from on the resources at hand, mainly the reliability text books, software functionalities which also were adapted specifically to the desired military handbook I was using, and other military handbook guidelines.

In addition to distilling out what the task and critical objectives were, and looking at the previous work example, I also had to map out the areas I had to learn more about in order to get a full understanding of the circumstances related to my work. These topics, which I've divided into three main blocks, mirrors the main subjects in this Thesis. All of the blocks are big topics and complicated in their own way, and so required substantial amount of time and practice to familiarise with.

The blocks are as follows:

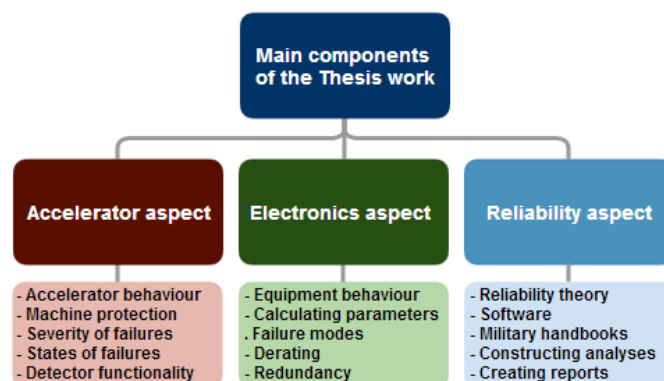


Figure 3: Main work aspects.

The accelerator aspect, which I will describe later in this section, is a challenging topic by any standard. In order to construct the reliability analyses, I had to get a good understanding of what was actual happening in the accelerator complex as a whole, and more importantly on the topics related specifically to the machine protection, accelerator behaviour, the severity of the different end results of the different beam loss detection malfunctions, what could cause such a malfunction, and how the beam loss detectors operated or malfunctioned. In other words, what are the end effects in the accelerator if something goes wrong, an essential part of this work. The process of becoming sufficiently aware of the important information was a gradual one, and was mediated by reading scientific papers and asking a lot of questions to the better informed. It was very important to try and focus on what was relevant and ignore the rest, in order not to drown in information. The reason for all of this was to classify the "end effects" into levels of severity, and attribute each possible end effect to a class of severity. This is very useful to do early on, as this is essential information in both the FMECA and FTA.

The severity classes, which I will explain in more practical terms in the reliability section of this Thesis, are weighed and defined as such:

1. **No effect:** Non-critical failure which does not cause a problem with the performance.
2. **Maintenance:** Failure in redundant components and other failures that allow for continued operation, but should be fixed as soon as possible.
3. **False dump:** Failures that causes loss of critical detection functionality. This will cause the system to abort (dump the beam).
4. **Blind failure:** Failures that would be classified as a false dump if detected, but remains undetected because of a very critical error.

The second topic I had to acquaintance myself with, was the electronics aspect of the task. This was again a really large and complicated task. The electronics, which was under design and construction by my supervisor, was an electronics crate (BLEAC) made with strict requirements in terms of both reliability and functionality standards. The reliability analyses which I was going to do, required a bottom-up FMECA as well as a quantitative & qualitative FTA, at a component level. This means that I needed to learn the system wide effect of each particular major failure mode for every component. Understandably, this was one of the most challenging parts and summarised up to over 800 potential failure modes for the BLEDP alone on a severity class of 2 or higher.

The number of actual FMECA considerations are probably much higher, considering the majority of the failure modes were judged to be in the first severity class and therefore omitted from the reports so that the relevant information was not drowned in noise. It is not an easy thing to jump into such a big and complex electronics crate and then figure out what every component does, but the process was extremely helpful for my understanding of electronics design, and was also mediated by my supervisor giving me guidance. It was again a gradual process, and done with a divide and conquer strategy, starting with the easier circuits. Meaning that, I would start with one circuit and learn each block of the card individually and then do the Prediction and FMECA on said blocks. The FTA required all the FMECA's so it was done at the end.

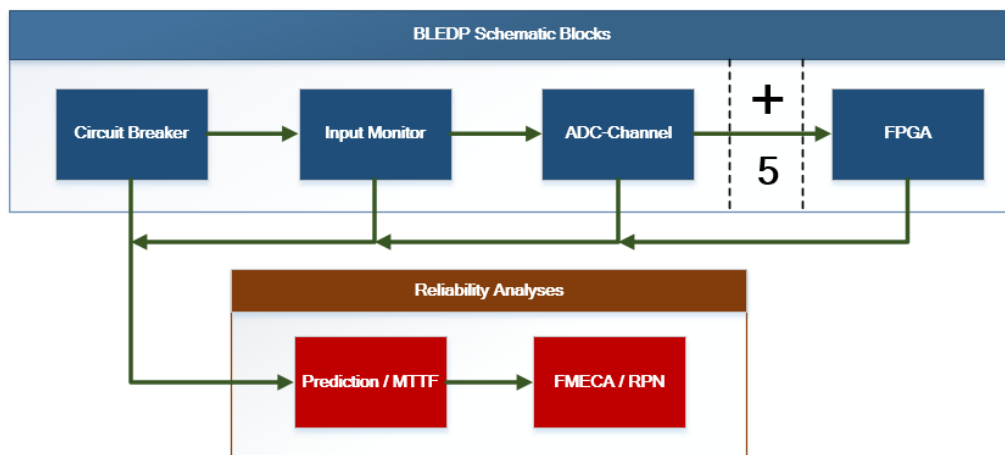


Figure 4: Divide and conquer strategy to minimize complexity.

So to summarise, first I learned the accelerator aspect in order to understand what the consequences of failure were. Secondly, I studied the electronics aspect in order to understand the functionality of the system which was being custom made to detect particle losses and therefore ultimately assisting in maintaining the system integrity.

The third layer, arguably the second tier of protection for the accelerators, is the reliability aspect. When constructing an electronics system, or almost any physical system in general, you can get far in terms of reliability by adding things like redundancy on critical parts or just by being thorough with the installation of the components and so on. This is usually called good "craftsmanship", and being careful and professional is of course very important. However, it is hard to really validate the reliability aspect of a system without using systematic tools which really defragment a system into it's most fundamental states. And so, when it came to learning and mapping out how I should proceed with the reliability aspect, I had to make sure to really understand the uses and limitations of reliability. In contrary to the previous two aspects which were already defined and had system specifications that

I could study, here I had to create my own system based on proper reliability theory. Therefore, this task had two critical parts. One was to make sure the reliability methodology I was creating was performed correctly, meaning that the tools I collected were actually set up correctly. This meant validating the analyses processes, the selection of electronics standards and handbooks, what information the reports should contain and so on.

The other thing I had to make sure of was that the reliability approach was fit for the task, meaning that I correctly used the tools for a task they are intended for. This is because there are many different options which usefulness is dependant on what you actually want to measure within each analyses, as well as where you are in the design or construction process. An example could be the choice of whether to include the repair time in the MTTF calculations and therefore get a MTBF calculation, or to measure availability versus unavailability. The analyses themselves were already picked out for the BLEAC. The Prediction (MTTF) was requested because it is a good way to measure both a statistical inference for a components failure rate within a certain time period of it's life, and since the repair time was not relevant, the BLEDP is a card which can be switched with a replacement, there was no need to use a MTBF-calculation. The choice of a FMECA is fairly self-evident, considering the "mission critical" nature of this equipment, and the FTA is in many ways an extension of both a Prediction and a FMECA, as it shows the extended failure propagation and is therefore very useful.

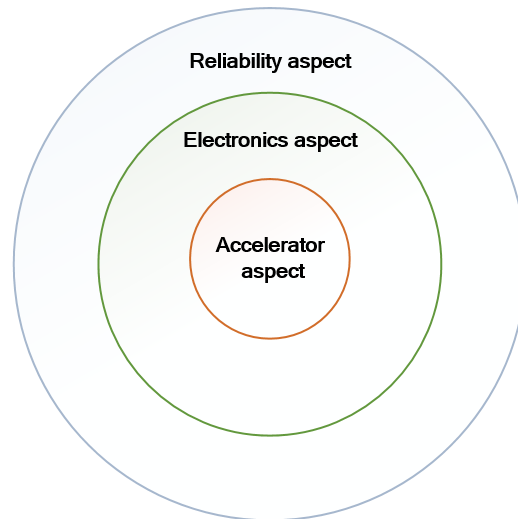


Figure 5: Levels of protection for the core functionality.

In addition to the pre-selected analyses that was requested for this work, another two task premises were already chosen as well. One was the software to be used for all the analyses, and the other was the military handbook to use for the MTTF-calculations. The software, Isograph Reliability Workbench 11, is one of the most advanced reliability software packages there is. It is built up on modules for the various analyses you want to use, and is also bundled up with relevant handbooks. This was a very important part of why the methodology is what it is, as the majority of the actual work was to be done here and therefore, generally, was bound to it's possibilities and limitations. The software is very extensive, and can be quite complicated depending on your need of the most advanced functions, but it was also a good platform to experiment on and practice with, for the different analyses.

So, outside of all the information I gathered about the general workings of the reliability analyses, the blocks I had to actually build it with was the blocks I had available in Isograph. That may sound like a limitation, but the possibilities presented in this software was far more extensive than I had need for, so it was more a question of finding the relevant parts to use. The ability to work across the modules, so that I could bring on the information I collected in one analysis, into another, is one such example. Also since the analyses had their own special modules within the programme and the handbook could be selected with all it's specific options available, with all the Prediction values implemented as well, I was able to greatly reduce the repetitive manual work. The process of learning the software was intuitive, but complicated due to it's many options.

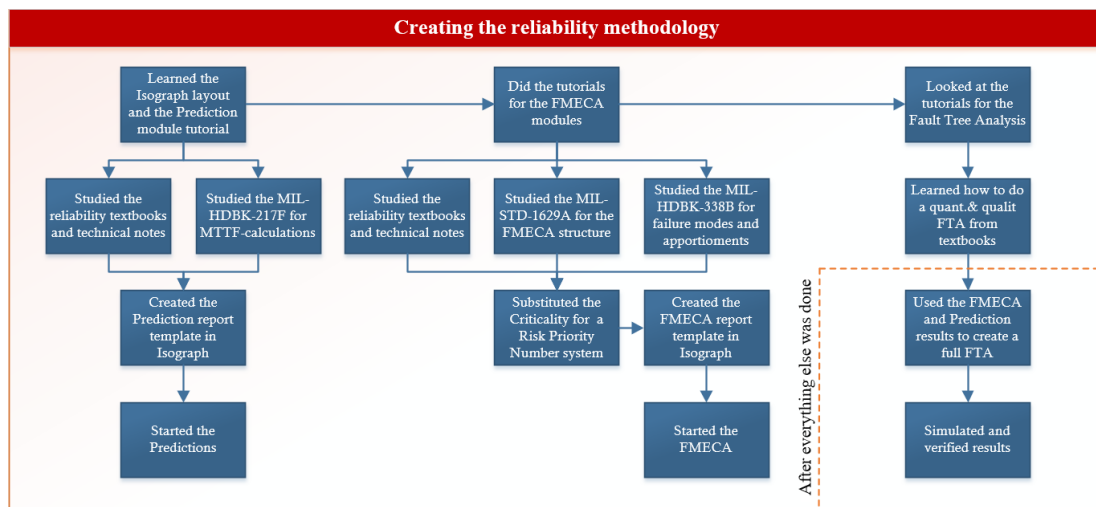


Figure 6: Process leading up the reliability analyses.

The military handbook, MIL-HDBK-217F, is a relatively famous and often used handbook for calculating the probability for failure in many generic electronics component. The calculations are given as a equation, and provides parameters derived from laboratory testing of various kinds of components. Isograph provided these equations and allowed me to pick the pre-defined parameters from a drop-down menu, and insert the values for the variables. It would then calculate both the component failure rates, and calculate the weighted average of the blocks and system. As such, the main use I had from the handbook directly, was to study the equations to see what factors affects the results, and to learn how to obtain the variables.

1.4 ELE 300

As a consequence of me being a part of this programme, the standard process of completing a Thesis under the rules and premises of the University of Agder, was complicated by the fact that the scale and time of the assignment didn't really match the requirements and description of ELE 300, the Thesis project course. Whereas the normal Bachelor's Thesis was typically 15 ECTS credits, or about a quarter of a semester, my Technical Student programme was set at 40 hours per week for around 50 weeks in total, over a period of 14 months. This is the equivalent, in time, to above 60 ECTS credits. However, as this was under special circumstances, the University of Agder agreed to upgrade my Thesis project into a 30 ECTS credits course, the equivalent of one full semester. As such, in addition to the BLEDP card being the most complicated card in the BLEAC and therefore a fitting card to write the Thesis on, the time equivalent spent on this card was the most fitting to at least cover the workload of 30 ECTS credits.

1.5 Project organisation

As a part of the programme [4], the organisational aspect of this work was also already partly predefined from the start. Some of these things made it a challenge to combine the requests of UiA, and the rules of contract with CERN as it was difficult to maintain the same level of contact due to the distance and time scale. Thankfully, UiA has been very forthcoming in giving me extra space and room, which helped me a lot.

The structure at CERN is divided into several departments, each with their own area of responsibilities. These departments are then divided into smaller groups which typically are responsible for a main area within their group responsibility. These groups are again divided into sections, and each section is then normally responsible for a limited area within their group. For my part, I was in the Beams Department, in which I belong to the Beam Instrumentation group. As the names suggest, they focus on matters related to instrumentation for the beam system. In this group, I was a part of the Beam Loss section, who are responsible for subjects related to CERN's Beam Loss Monitoring system.

Here there are several smaller working groups. I am working indirectly on the Beam Loss Electronics Acquisition Crate (BLEAC), which is an electronic crate designed to hold several cards of both the same and different functionality. This crate is still under development and will be the acquisition crate the beam loss detectors, the Beam Loss Monitors (BLM) are connected to. For this design process we have a designer of the hardware, which is also my supervisor, and several Technical- and Ph.D.-students in addition to Fellows, who are working on the FPGA programming. My role was to do the reliability analyses for estimating the reliability of this acquisition system and I am the only one working on this, with assistance of my supervisor. As such, all the work itself is done by me, with regard to the analysis. However, I get help with some of the planning, as my supervisor has experience with reliability from before. I also could ask for help if I couldn't understand a part of the circuit, but for the most part I tried really hard to work it out by myself, from reading data sheets and textbook. As such, I think it's fair to say that I have done most of the work by myself, as intended.

1.6 The accelerator complex

The particle accelerators [5], located under CERN's various compounds on both sides of the border between Switzerland and France near Geneva, are mostly placed in long circular tunnels which have been dug out almost 100 meters underground. The distance they cover is truly massive, with the longest one, the LHC, going over 27 km around in a circle. Therefore, combined with the other accelerators and the experiments themselves, it's arguably the biggest and most complex machine ever constructed. Consequently, to describe it as briefly as I will attempt to is indeed a challenge but I feel it's beneficial to have some idea of the basic blocks which make up the accelerator complex before moving on to the details on my task. Hopefully it will aid in explaining some of the choices and reasons taken during this work.

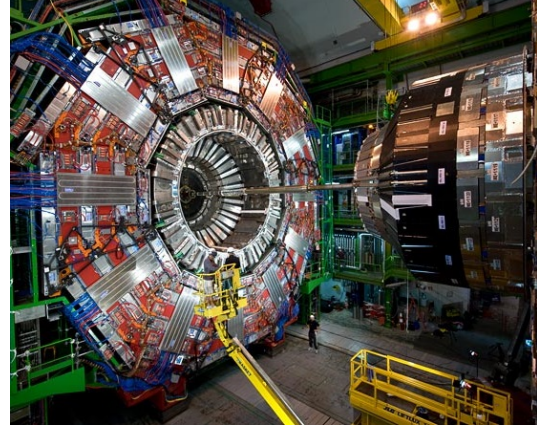


Figure 7: CMS, the second largest detector at CERN.

The accelerators have been modified and refurbished since the start; both the first and following accelerators are still in the accelerator chain and is directly in use with the exception of the predecessor of the LHC; the LEP. As it stands now, it is mostly used to accelerate so called Hadrons, a group of particles which incorporates among other the proton which is the ingredient used for the collisions. It is extracted from a small canister of hydrogen gas and is sent through a linear accelerator called the LINAC which accelerate the particles to about 50 MeV before passing it to the Proton Synchrotron Booster (PSB).

This is then accelerated further up to 1.4 GeV and is passed to the Proton Synchrotron which pushed it up to 25 GeV and after sends it to the Super Proton Synchrotron who will press the particles up to 450 GeV and finally release them into the Large Hadron Collider. Here the particles will reach about 4 TeV and a speed of 0.999999991 of c , which is about 3 m/s slower than the speed of light. After the upgrade, which the accelerators are currently in, are finished, the goal is to reach up to the designed 7 TeV in each direction. The particles are made to collide inside one of the 7 experiments along the LHC; for example ATLAS and CMS which are used to study the effects of high the speed collisions.

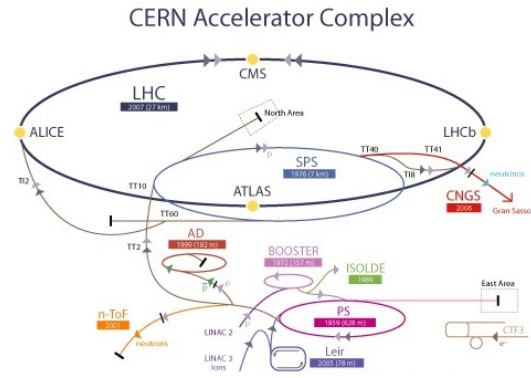


Figure 8: CERN accelerator complex.

2 Beam Loss Electronics

Here follows a description of the system used to protect the accelerators from damage. A general description of the Beam Loss Monitoring system will give a short overview of the rationale behind such a system. Further, a more detailed description for the system used for the LHC injectors will be shown, and one of the electronics cards used, the BLEDP, will be explained in greater detail.

2.1 Beam loss detection systems

The accelerators are essentially very powerful magnetic blocks which focus or defocus the particle beam in a way that allows for it to be controlled fairly effectively. However, no particle accelerators are perfect at controlling the bunches of particles that accelerate within the machines. Because of the mission of the particle accelerators at CERN, a range of beam intensities, which varies from low energy test beams up to very high energy beams used for the experiments, will be used. In addition, there are some inherit variations in the accelerators themselves, as some are many decades old and run at different energy levels. As a consequence of this, periodically there will be beam losses that escapes their designated trajectories and potentially damage the interior of the machines. Such a damage might cause the entire accelerator system to be inoperable for an extended period of time due to the repair being challenging, and will, in addition to very high repair costs, cause precious run time to be shortened. To prevent this as best as possible, a beam loss detection system is required to detect and consequently deal with beam losses in a preservative manner.

Moreover, as the particles obtain more energy, the loss of merely a fraction of the beam can have a detrimental effect on the machine, and consequently a potential stop in the operation of the particle accelerators [6]. As such, a beam loss detection system is usually desired to fulfil several criteria. Most importantly is the protection from direct damage, as already mentioned. Secondly, beam loss detection systems also need to prevent indirect damage that can cause escalating problems due to rogue particles hitting magnets or surrounding instrumentation. Thirdly, for the purpose at CERN, the beam loss detection system should be able to be used with various beam intensities. Lastly, it should be able to diagnose the particle beams.

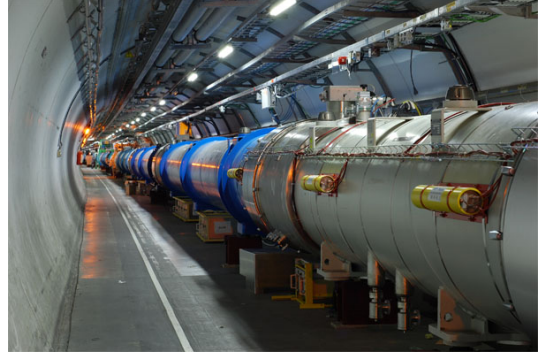


Figure 9: Detectors (yellow) on the LHC.

At CERN, this detection system is called the Beam Loss Monitoring system. As described earlier in this Thesis, there are many challenges related to the construction and implementation of this system, and due to the protection systems critical importance for the safe operation of the accelerators, a special focus on reliability was taken. The following section describes the systems functionality.

2.2 Beam Loss Monitoring system for the LHC injectors

At the time of writing, the accelerators at CERN are in a shut down time period named Long Shut-down 1 (LS1), and in this time period, all of the particle accelerators and much of their surrounding installations, are undergoing upgrades and repairs. As a consequence of these upgrades, the system will be expected to handle even higher beam energies. To match these new challenges, a new Beam Loss Monitoring system [7] is also under development to match the new attributes, in order to maintain the necessary machine protection for the future operation. This system is designed to match the required high performance and configurability, and due to it's mission critical nature, reliability was also prioritized.

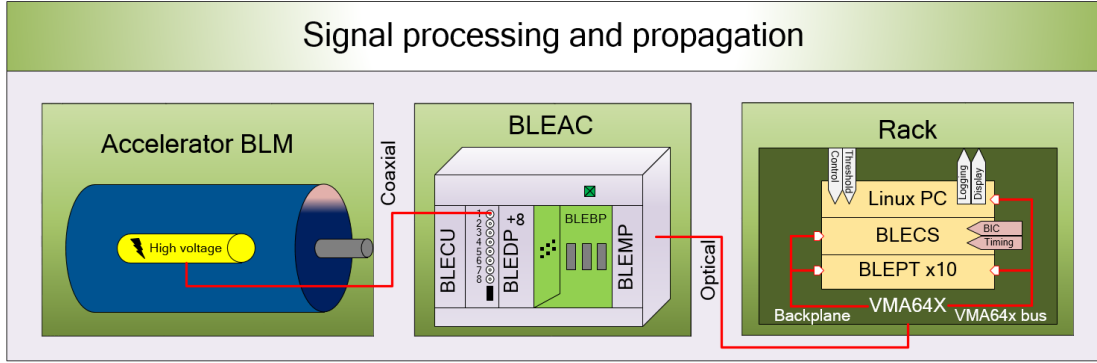


Figure 10: Block diagram of the signal propagation.

This system is built up by three main blocks. The first one is the beam loss detectors themselves which are placed on strategic spots around the particle accelerators. The second is the acquisition crate, BLEAC, which is responsible for acquiring, processing and publishing the values of the measured signals. The third block is the processing crate, the BLEPC, which then decides how to interpret the values in pre-defined actions, and also stores diagnostic information, provides timing information and returns Thresholds to the acquisition crate. It is evidently a complicated system which incorporates a lot of functionality, so for the purpose of the Thesis, I will try to focus on the relevant functions and then explain the BLEDP-card in more details.

The detectors are placed around the accelerators as shown in Figure 9. There are several types of detectors, and the type used at any given spot is matched to its surroundings. Each detector is connected by coaxial cable to the acquisition system, here the BLEDP-card in the acquisition crate. For each crate, there are 10x BLEDP cards, and each of the card can be connected to 8 detectors. So for every 80 detectors there is a need for a crate. How the detectors measure beam losses depends on it's type, but for the most part the detectors will be so called "ionisation chambers [8]". These detectors will react to particles hitting the detectors by generating a current which is sent to, and measured by the BLEDP-card. Due to the use of many different types of detectors, the acquisition crate has to be able to accommodate each type, and this means that the system needs to detect a current input from 10pA to 200mA, a dynamic range of 10^{11} . This level of sensitivity means that crossover protection and noise reduction was critical in the design process, as well as shielding when possible for the cabling.

Very simplified, once the signal reaches the BLEDP-card in the acquisition crate, it will be sent through the input monitor block which uses one out of two different measurement methods to obtain a value. The reason there are two methods is related to the very wide measurement range, as each method has it's own designated range in which it operates. The first method is called the Fully Differential Current to Frequency Converter, FDFC, and is responsible for the measurement window between 10pA to 30mA. The second method is called the Direct ADC acquisition, DADC, and measures between $80\mu\text{A}$ and 200mA. These methods are chosen by the on-board FPGA, based on the measured value in the previous measurement window. This means that if the measurement in the previous window was above or below a certain given threshold, it would select the corresponding method for the follow windows, until it detects otherwise.

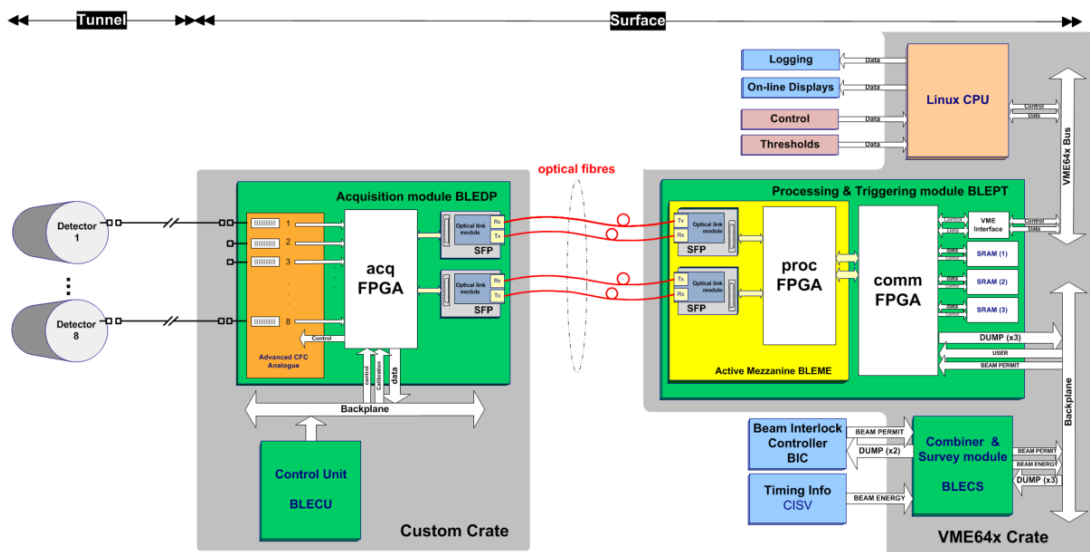


Figure 11: A unit of CERN's Beam Loss Monitoring system. [1]

Once it's been measured in the relevant branch, it will be sent to an ADC, and pushed through to the Processing crate, BLEPC, via optical links. Also two comparators are used separately to provide another value called COUNT, which are also sent to the BLEPC, via optical links. The COUNT value and the ADC value will then be combined through an algorithm and checked up again the thresholds. Depending on the value, if it is within the permitted threshold, it will continue to give the system a beam permit, and if not, it will cause a dump as well as deny any additional particle injections. The dump, when triggered by the BLMs, is an emergency procedure and will cause some very powerful magnets, called kicker magnets, to essentially blast the particles into a path which leads to some special blocks of carbon and concrete that absorbs much of the energy.

As such, it's an important defence mechanism [9] to protect the accelerators and equipment from damage and potential activation, but an important goal is also understandably, to reduce the number of false dumps as much as possible. In addition to the beam permit via the Beam Interlock Controller, BIC, the processing crate will also provide the system with Thresholds levels and Timing info and their function will be described when I go over the BLEAC, and in particular the BLEDP.

2.3 Reliability aspect for the BLMs on the system level

In order to start with the reliability analysis on only a part of this system, it was important to both isolate the desired area, and to make sure that the reliability analysis didn't suffer from this limiting. Not only was I to study the workings of the BLEDP, as a part of the BLMs, but it was also the plan to divide the BLEDP itself into smaller and more manageable pieces, so as to reduce the complexity further. As explained earlier, this divide-and-conquer strategy meant that I would separate the cards functionalities into schematic blocks, and through this, gain the benefits of focusing on fewer system consequences of failures, as many would be the same.

For the most part, this meant that I could follow the schematics as they were laid out, though taking precautions to include parts from other schematics which would be directly related. Further, in terms of not letting the analysis suffer from this division, it was also important to include the relevant parts of the rest of the BLMs, from an end effect point of view. Also, not all aspects of the BLMs is equally important in terms of directly assisting in maintaining the core protection functionalities. Therefore, after studying the BLMs, I would map out all the outputs of the BLEDP-card and see what effects their individual and collective failures had on the BLMs. The point was to only include the failure propagation from the BLEDP, that also caused a problem with the detection of losses. In other words, treating these key parts as a sub-system within the BLMs.

Fortunately, the system wide end effects of BLEDP failures were fairly simple to categorize, as most of the important parts of the BLMs rely directly on the BLEDP-card. The end effects were therefore divided into the four end effects which I've described earlier. Failures in the BLEDP that ended up causing problems with the "housekeeping" diagnostics, such as logging room temperature, and therefore could be found and fixed at the next maintenance run, were given the lowest priority. This is outside of the failures which are non-critical for functionalities, such as one non-essential filtering capacitor failing. More critical were failures in the BLEDP that meant the system would cause a dump and therefore disrupting valuable operation time. Most critical was the failures which should cause the system to dump the beams, but is not detected.

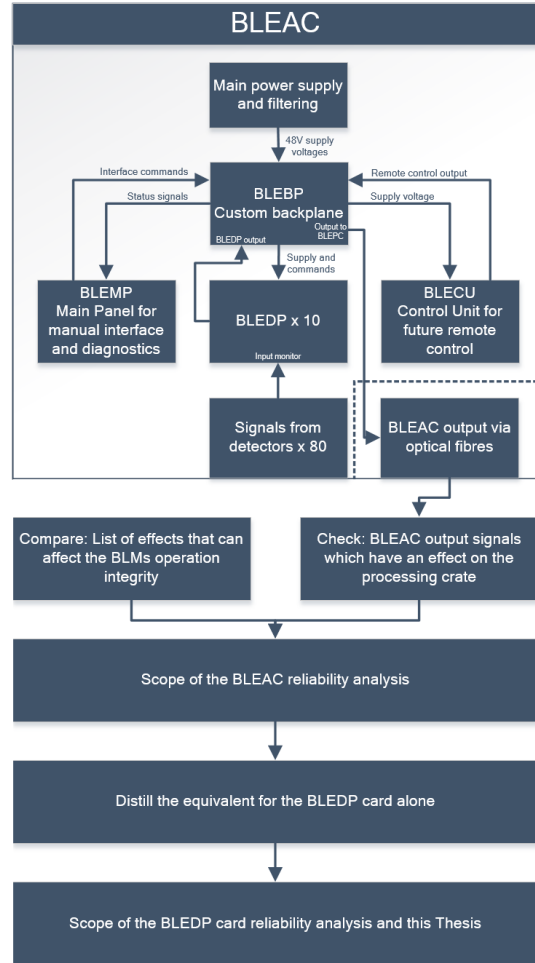


Figure 12: Scope of the reliability analysis.

2.4 Beam Loss Electronics Acquisition Crate

The acquisition crate, BLEAC, is a crate containing the acquisition system for the BLMs. The crate is made up of three different types of custom designed electronics cards, as well as one custom designed backplane and the power supply. There is also the possibility to include a redundant power supply through the use of a jumper. The crate is arranged so that proper grounding connections are made throughout the crate and special care is taken regarding cleaning and installation of the components.

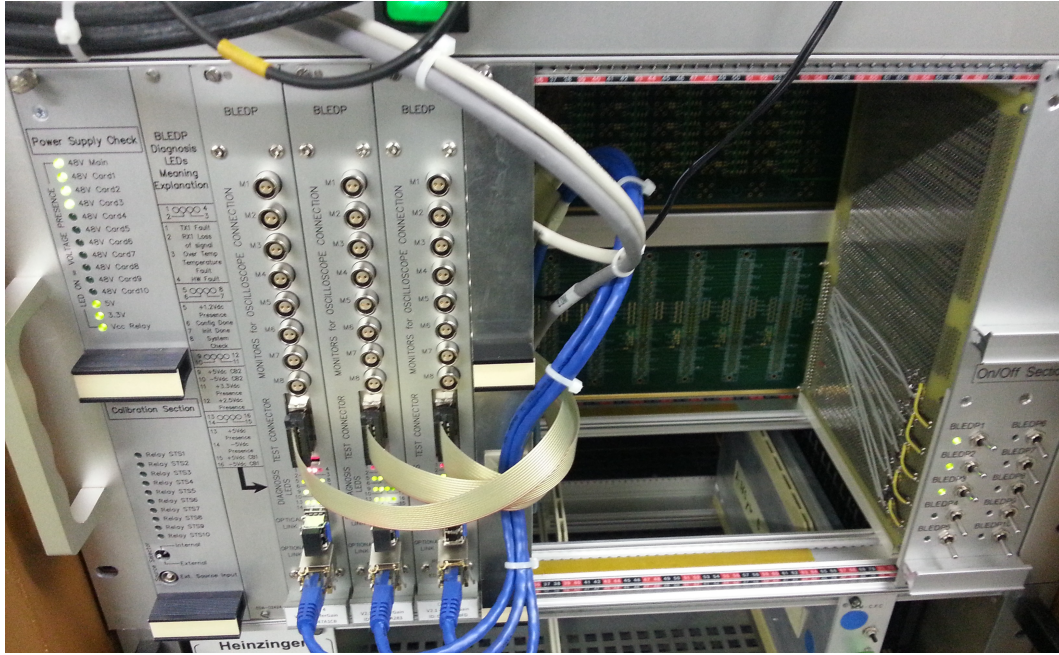


Figure 13: Prototype BLEAC crate.

Here follows a short description of the other parts in the BLEAC:

BLEMP The main panel, in Figure 13 located on the far left, is providing several features to the BLEAC. It functions as a visual diagnostics tool, where it provides both an indication of the 48V presence in the different BLEDP cards, and it also gives the current relay status for the reference current system. This reference system is one of the checks to see if the system is functioning correctly, by sending a known current through the same equipment as the signals from the detectors. This can then be measured for each card before operation to verify that the output is within the threshold of error. The threshold of error is set at $\pm 10\%$. Outside of the internal reference current, the main panel also gives the opportunity to switch to an external reference current, which can be provided to the system by a dedicated input.

BLECU The control unit, here on the right side of the crate in Figure 14, is responsible for the possibility to remote control the BLEAC. This card is not yet fully implemented in the system but once it's done, it will benefit the handling of this system, as the need to go to the crate's respective locations to make adjustments to, for example, the reference current will be reduced. It will also have a tuning knob to adjust the internal reference current and the option to manually disable or enable the BLEDP-cards.

BLEBP The backplane is another custom designed board which binds all the cards together. While the BLEMP and the BLECU have mostly supporting roles, the backplane is equally critical for the operation as the BLEDP, at least from a reliability point of view. All of the signals processed in the BLEDP-cards will be sent through the BLEBP, so the consequences of failures are the same, with either distorting the measurements, or not passing on the measurements to the BLEPC at all. The job of the BLEBP is also to provide the cards with the necessary 48V supply voltages, as well as monitor the current supply levels, among other things such as diagnostics and ID handling. While a failure in one BLEDP can be fixed by changing the card itself, a failure in the backplane will cause a bigger operation and consequently a longer operational downtime for the accelerators. Therefore, a lot of thought have been put into the design and implementation of the board itself, especially regarding connections, noise reduction and similar. Another example is the use of several dedicated ground planes in the PCB layers and the use of special VIAS.

Power supply The power supply provides the backplane with 48V, and from the backplane it will be routed, through circuit breakers and current monitors, to the BLEDP card which will convert the 48V to the needed voltage levels. These are 5V for the analog components, and 3.3V to be converted further into 2.5V and 1.2V which is used to supply the on-board logics and FPGA. 48V was chosen to limit the current flowing in the backplane and reduce the ripple noise from the AC/DC conversions. There are also a lot of filters to try and keep the noise as low as possible. The power supply can also be set to be single failure tolerant as there is an option to have a redundant power supply connected in parallel. This option can be opted for by adding a jumper.

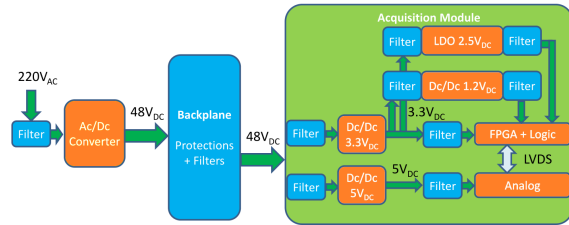


Figure 14: Power supply handling [1].

Cables In the spirit of the high reliability and low noise design, also the cables used from the beam loss detectors have shielding. More specifically, the cable has internal shielding to protect against low frequencies, as well as external shielding to protect against high frequencies.

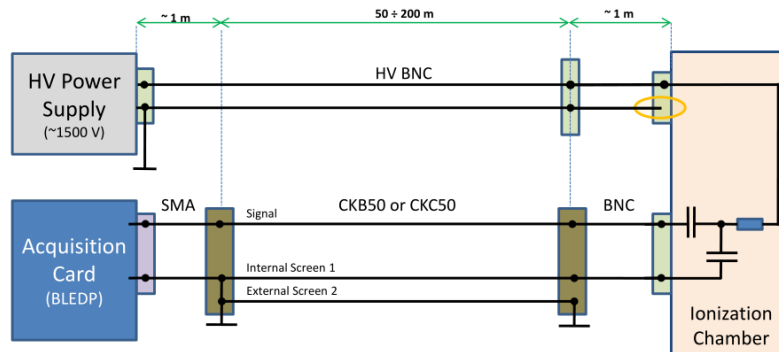


Figure 15: Beam loss monitors to BLEDP cabling [1].

2.5 Beam Loss Electronics Double Polarity card

So to recap, everything mentioned previously in this section was intended to explain the environment of the BLEDP-card and show it's role in a larger system. To make an informed judgement on the consequences of failures, the failures had to be examined to their final end effects. And so, the card's role in a bigger and more complicated system made it challenging to isolate it for a reliability analysis, without at the same time losing important details. The solution was to treat the sequencing parts as perfectly functional, and then see what the consequence of each failure in the BLEDP would mean for the system end effects. Due to the importance of the BLEDP-cards, the consequences of failures was often incompatible with the safe operation of the particle accelerators, but was at the same time detectable. The failures would many times manifest itself in the form of either no signal or erroneous signal being sent imposing as a measurement.

Reliability blocks in the BLEDP		
	Sub-blocks	Reliability numbers
Circuit breaker	+5V - Feedback -5V - POWERGOOD_CB - ON_CB	Overall MTTF(hours) per block: <u>1.713e+07</u> Number of blocks per BLEDP: <u>2</u> Number of components: <u>37</u> Worst component: <u>Capacitor 1uF Ceramic</u> Worst component MTTF value: <u>1.535e+08</u>
	- Dig. Potentiometer - Saturation monitoring - Stop - Switch FDFC/DADC to ADC - Buffer amplifier - Voltage ref. generator - Comparators - Offset current and detector input - Switch FDFC/DADC to switch - Input switch - Fully diff. Integrator - Power supply for pot. - Flip-flop - Input voltage filter - Filters 6x capacitors - Filters 4x capacitors - Filters 2x capacitors	Overall MTTF(hours) per block: <u>2.771e+06</u> Number of blocks per BLEDP: <u>8</u> Number of components: <u>155</u> Worst component: <u>Capacitor 1uF Ceramic</u> Worst component MTTF value: <u>1.722e+08</u>
ADC-channel	- ADC - Voltage level converter - ADC ref. voltage	Overall MTTF(hours) per block: <u>7.442e+06</u> Number of blocks per BLEDP: <u>8</u> Number of components: <u>41</u> Worst component: <u>Capacitor 10uF Ceramic</u> Worst component MTTF value: <u>1.195e+08</u>
	- JTAG - Channel and voltage supply connectors	Overall MTTF(hours) per block: <u>6.544e+06</u> Number of blocks per BLEDP: <u>1</u> Number of components: <u>24</u> Worst component: <u>Backplane connector</u> Worst component MTTF value: <u>3.417e+07</u>
Power supply	+48V input voltage 5V DC/DC 3.3V DC/DC - Voltage conv. 3.3/2.5V - Step down current mode converter	Overall MTTF(hours) per block: <u>3.497e+05</u> Number of blocks per BLEDP: <u>1</u> Number of components: <u>70</u> Worst component: <u>DC/DC converter 3.3V</u> Worst component MTTF value: <u>1.33e+06</u>
	- SFP connectors - Light indicators	Overall MTTF(hours) per block: <u>3.301e+05</u> Number of blocks per BLEDP: <u>1</u> Number of components: <u>37</u> Worst component: <u>Optical Transceiver</u> Worst component MTTF value: <u>7.556e+05</u>
Relays and calib	- Relay activation - Relay status	Overall MTTF(hours) per block: <u>1.25e+07</u> Number of blocks per BLEDP: <u>1</u> Number of components: <u>37</u> Worst component: <u>Capacitor 100uF Ceramic</u> Worst component MTTF value: <u>2.153e+08</u>
	- Serial number generator - Temp and humidity sensor - ADC for housekeeping - HV feedback	Overall MTTF(hours) per block: <u>1.267e+07</u> Number of blocks per BLEDP: <u>1</u> Number of components: <u>28</u> Worst component: <u>Capacitor 100uF Ceramic</u> Worst component MTTF value: <u>1.158e+08</u>
FPGA	- FPGA chip - FPGA external memory - FPGA reset - FPGA filters - FPGA oscillators	Overall MTTF(hours) per block: <u>1.076e+06</u> Number of blocks per BLEDP: <u>1</u> Number of components: <u>92</u> Worst component: <u>FPC code chip</u> Worst component MTTF value: <u>3.701e+06</u>

Figure 16: List of all 49 individual sub-blocks in the BLEDP.

How the card is divided Now, as the BLEDP is the main focus of this Thesis and the reliability analysis, I have provided a description of each of the blocks the BLEDP-card was divided into. However, although my intention is to make these following pages as an overview of the specific results of the analyses, the work itself is the reports which is included in the appendix. Therefore, the intention is to use the following description and reliability assessment as a supplement for the report. The report structure, which I have described in more detail in the reliability section, will follow the same hierarchy as in this section for easier comparison. For the reliability aspects pertaining the analysis themselves, I have described the process in Section 3.

The blocks which makes up the BLEDP-card was chosen by me, based on their role in the card and is as such not necessarily "official" blocks outside of the reliability report. The benefits of creating these blocks is that I could group the main components, the ones which provides the functions, as well as their support components such as filters.

This made it a lot easier to organize the report and also makes it much easier to back-track the individual components, compared to stacking all the similar components into one block. Another simplification I made was to highlight the overall MTTF-values for the schematic blocks, as well as the worst individual component, relative to the others. This makes it easier to relate to the schematic blocks as there is no need to adjust the components if the worst one is above an acceptable threshold. This then makes it easier to infer the status of the blocks without going over every single component and should prove beneficial with a large reliability analysis. On the same note, as the overall MTTF-value for the entire BLEDP-card is made up of the weighted average of each tier, from the components to the sub-blocks to the schematic blocks, an acceptable value should allow the designer to infer the good standing of the system.

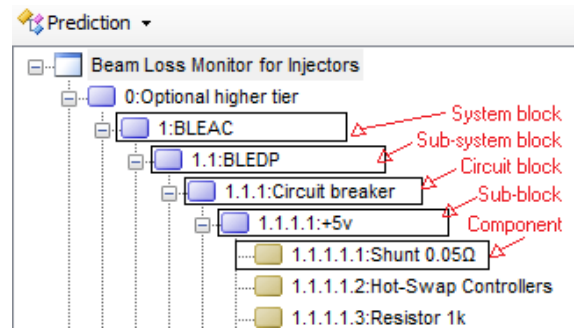


Figure 17: The block system.

How to read the following assessments The work was done by completing each circuit-block independently, and then combining everything at the end. As such, the following subsections on the parts of the BLEDP-card, will be focused on the same circuit-blocks, and will be centred mostly on the FMECA. The Prediction and the FTA is also important, but the Prediction, as explained above, is a statistical inference and is more interesting in this case, on the sub-system level. It will therefore be discussed a little more in the results overview. However, I have added some MTTF-data in Figure 16, which can be used as an overview.

The FTA is constructed as a whole tree based on all the FMECA's, all the Predictions and the block diagrams. It is therefore explained in more details by it's own, as is in many ways the end result of the analysis. The following sections is intended to be a more in-depth overview regarding the functions of the BLEDP.

2.5.1 Circuit breaker

Functionality In each BLEDP card there are two circuit breakers which also functions as current limiters for the +5V and -5V going out to the card. The acquisition card receives its input voltage from the power supply and supplies the 5V for a total of 4 input monitors and ADC-channel circuits. The circuit breaker utilize a current sensing hot-swap controller for opening and closing the MOSFET which allows the 5V to pass to the BLEDP. The controller is enabled by ON_CB, which then allows the MOSFET to open after the controller has checked everything is within the operational parameters in terms of over-voltage and temperature. It then sends a POWERGOOD signal to the FPGA to indicate everything is working. If this stops, the FPGA will send 3x retry signals to see if it was a limited time error. If there is still a failure, the FPGA will stop trying to start the circuit breaker.

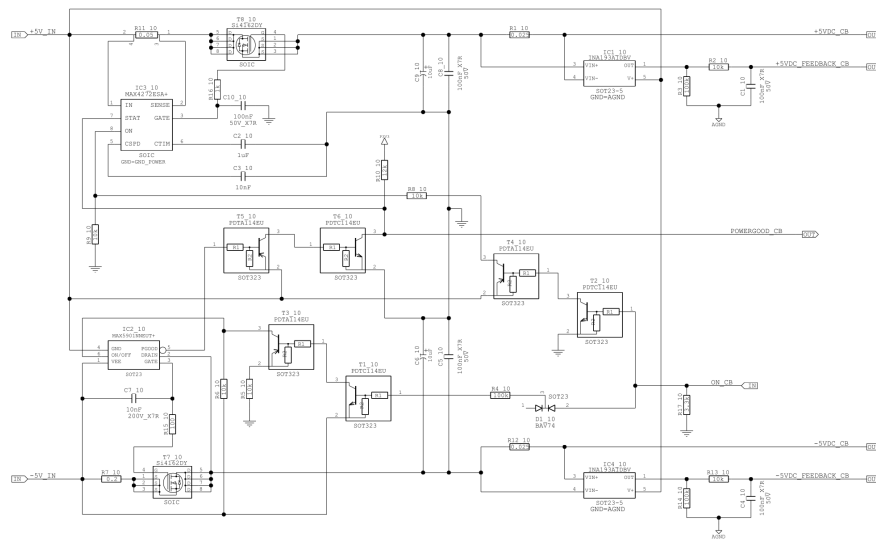


Figure 18: Circuit of the Circuit Breaker.

Reliability assessment The circuit breaker provides the necessary 5V to 4 out of 8 Input Monitors and ADC-channels, and is therefore essential for the correct operation of the system. Any erroneous voltage output, either no output or at a different voltage, will cause the loss of 4 detectors. Therefore a generalization can be made that if the consequence of failure is so that the output is changed or denied, the system will cause a false dump. Detection is done by connectivity checks.

FMECA		RPN - Worst FM		Failure rate		Summary
Total failure modes	40	Sum SxOxD	4	Total MTTF	1.713e+07	- Probability of failure is low - Detectable failures - Low RPN number No changes warranted
Category 2: Maintenance	8	Severity	2	Worst comp	1.535e+08	
Category 3: False dump	32	Occurence	1	> 20 years	Yes	
Category 4: Blind failure	0	Detection	2	Failure type	Random	

Figure 19: Reliability values and summary for the Circuit Breaker.

2.5.2 Input monitor

Functionality The input monitor is the entry point of the signal from the detectors. The circuit is essentially responsible for processing the signal in either the FDFC or DADC measurement method which can handle a range of 10^{11} . The Fully Differential Current to Frequency Converter [10] is responsible for the measurement window between 10pA to 30mA while the Direct ADC acquisition measures between $80\mu\text{A}$ and 200mA. These methods are chosen by the FPGA, based on the measured value in the previous measurement window. This means that if the measurement in the previous window was above or below a certain given threshold, it would select the corresponding method for the follow windows, until it detects otherwise. After it's been measured, the result will then be sent to the ADC-channel as well be measured as a COUNT-value obtained from the comparators. The ADC-channel value and the COUNT-value will be combined in the FPGA using a special algorithm [11] and the result will be measured up against the given Threshold and from confirm to the BIC that there is a beam permit, or deny any further injections.

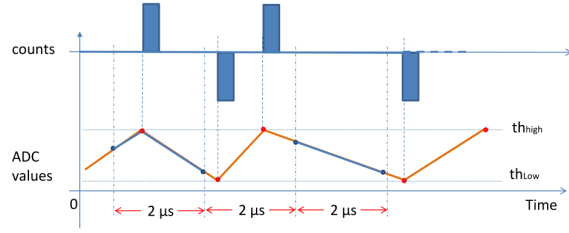


Figure 20: Combination algorithm plot [1].

The card has many functions to make this process happen, and is by far the most complex circuit block in the BLEDP-card. To write a description of all would take many pages, so for simplicity I've added a block diagram and from there I will explain each step briefly.

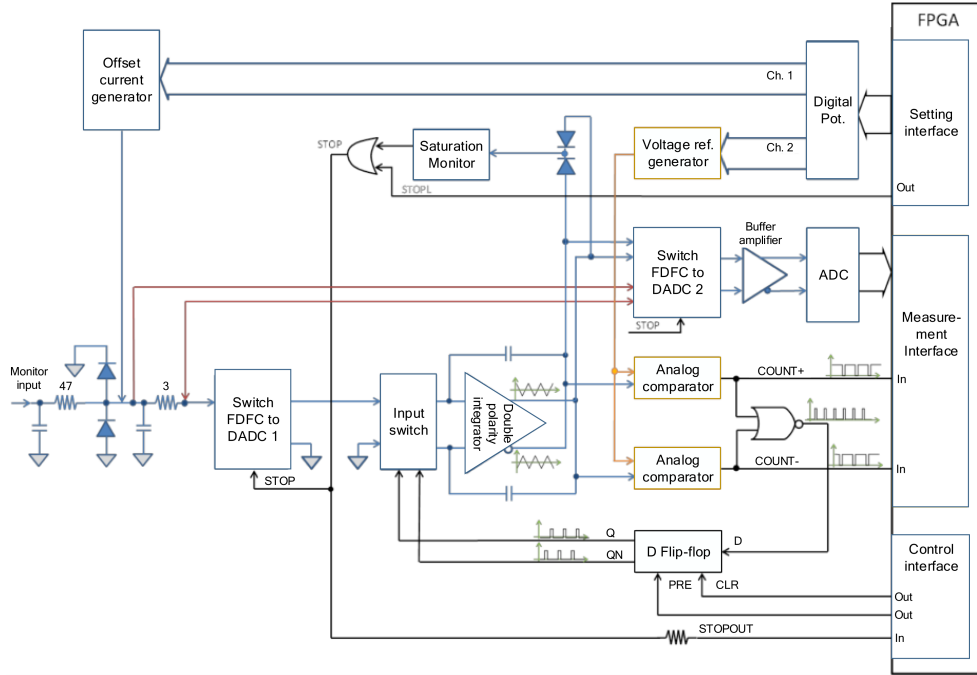


Figure 21: Input monitor block diagram [1].

The design is so that the two measurement methods can use many of the same components. The digital potentiometer controls two outputs, one channel is for the offset current generator which is used to limit the current leakage from the cables, backplane and components. It's also used as a check to see the module is working correctly as mentioned earlier. The second channel in the digital potentiometer is for the voltage reference generator, which provides the threshold levels for the analogue comparators. These then in turn control the switches, through the use of the D flip-flop, which is used to activate the desired measurement method. The comparators also provides the differential COUNT-value which is used by the FPGA as mentioned earlier. The saturation monitor is used as protection from pulses on the input which might damage the system. If it detects such a situation, it will switch automatically to the DADC and clamp the current to ground. Afterwards, it will be given a command to try and reset, in order to see if it's safe to operate.

The FDFC consists of the specially selected low noise, fast input switch, a fully differential integrator, the two analogue comparators, filters and an NOR-gate. Since the FDFC has to work all the way down to 10pA, a special focus on leakage was needed, which is why the fully differential integrator was selected by adding two high impedance op-amps for filtering and buffering a fully differential amplifier. The pulses generated in the comparators are sent to the FPGA. The DADC is used on the higher measurements, and can go up to 200mA. It consists of the 47 Ω and 3 Ω resistors on the input where the 3 Ω is used as a shunt, and the current passing will be picked up directly by the 10 Msps, 16-bit ADC.

Reliability assessment There are 8 Input Monitors per BLEDP, one for each channel. As the failures are often directly related to the main functions of the circuit, the majority will cause a false dump. The maintenance cases are single failure tolerant components dealing with input protection, so a failure here would cause any following damage to produce a false dump. A critical failure would cause the loss of one detector. Because of the diagnostics, the critical failures can be detected. However, the 47 Ω and the cables leading up to it is considered a single failure tolerant Blind Failure, because if there is a problem with the external diagnostics, the internal system would not know anything was wrong. However, the probability of this occurring at the same time as having a beam loss exactly here is extremely small, so no changes to the design is needed.

There are also possibilities for digital failures, but unless they are attributed by a physical error in a component, they are not counted. Software related failures are considered separate from hardware failures for the purposes of an FMECA.

FMECA		RPN - Worst FM		Failure rate		Summary
Total failure modes	114	Sum SxOxD	8	Total MTTF	2.771e+06	• Probability of failure is low • One low risk BF • Low RPN number • <u>No changes warranted</u>
Category 2: Maintenance	2	Severity	4	Worst comp	1.722e+08	
Category 3: False dump	111	Occurence	1	> 20 years	Yes	
Category 4: Blind failure	1	Detection	2	Failure type	Random	

Figure 22: Reliability values and summary for the Input Monitor.

2.5.3 ADC-channel

Functionality As with the Input Monitor, there are 8 ADC-channels, one for each Monitor. The ADC is a high speed, 10 Msps, 16-bit ADC and is responsible for sending the digital measurements to the FPGA. It gets it's clock frequency from the FPGA, and is supplied with a 5V from the on-board DC/DC-converters. The ADC is fully differential, giving it a good dynamic range, and is consequently driven by the fully differential amplifier as described earlier. Most of the other components are filters or voltage level converters. The 2.5V which is generated is for the ADC I/O and the output common-mode voltage, Vocm, which goes to the fully differential amplifier.

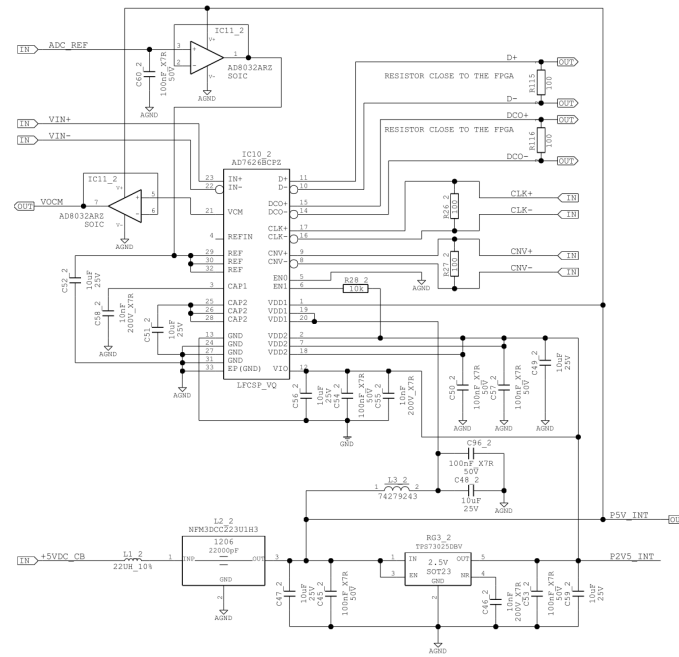


Figure 23: ADC circuit.

Reliability assessment The importance of having a functional ADC-channel is essential for the safe operation of the system. The circuit is fairly simple, but a number of failures would cause an erroneous or non-existing output to the FPGA. The most probable failure is one of the filtering capacitors failing closed, meaning it will cause the voltage to pass to Ground. The end result would usually be the loss of either the 5V or 2.5V, and in both cases the lack of either supply voltage or I/O possibilities would cause the loss of one channel.

FMECA		RPN - Worst FM		Failure rate		Summary
Total failure modes	30	Sum SxOxD	3	Total MTTF	7.442e+06	- Probability of failure is low - No BF or Maintenance - Low RPN number No changes warranted
Category 2: Maintenance	0	Severity	3	Worst comp	1.195e+08	
Category 3: False dump	30	Occurence	1	> 20 years	Yes	
Category 4: Blind failure	0	Detection	1	Failure type	Random	

Figure 24: Reliability values and summary for the ADC-channel.

2.5.4 Filters & Protection

Functionality This circuit blocks contains the connectors going to the backplane, as well as ESD protection diodes, channel input filters and fuses. It's also the input location for the JTAG which is used for local programming and diagnostics. One connector is responsible for providing the BLEDP-card with channel commands, relay status, card-localisation, enable, and the 48V input. The relay activation is done through the cmd_ch. As mentioned before, the relays are used for the self-diagnosis and are controlled by the FPGA. The same is the EN_CARD which goes to the on-board power supply and allows for remote control of the card. The localisation is used to provide each BLEDP-card with an unique ID which allows for control of the many cards. The testpoints are for diagnostics and the single connectors are for the signal channels.

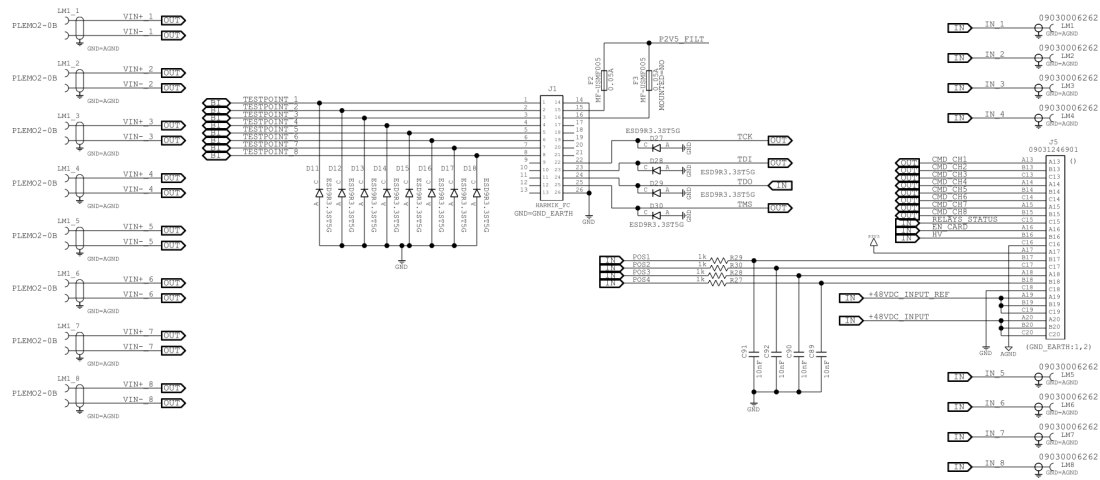


Figure 25: Filters and protection circuit with connectors.

Reliability assessment The failure of the connectors are serious in that it will cause the loss of either 1 input channel if the failure is in the single connectors, or up to 8 if the failure is in the main connector to the backplane. The probability of failure is fairly low as the connectors will not be unplugged unless there is a maintenance situation, and there are not a lot of functionality here outside of protection and filtering. Many of the failures are single failure tolerant, meaning that the ESD-diode will have to fail closed and there would need to be ESD introduced in the channel, before it could cause a problem. There are also 11 Maintenance cases here, but these are related to the secondary functionality of the card, such as the JTAG and testpoints.

FMECA		RPN - Worst FM		Failure rate		Summary
Total failure modes	21	Sum SxOxD	4	Total MTTF	6.544e+06	- Probability of failure is low - Many are Maintenance - Low RPN number No changes warranted
Category 2: Maintenance	11	Severity	2	Worst comp	3.417e+07	
Category 3: False dump	10	Occurence	1	> 20 years	Yes	
Category 4: Blind failure	0	Detection	2	Failure type	Random	

Figure 26: Reliability values and summary for the Filters & Prot.

2.5.5 Power supply

Functionality The power supply provides the voltage levels needed in the BLEDP-card and is derived from the 48V 300W power supply in the crate. The 5V and 3.3V is created from the DC/DC-converters and is sent to the components in the card which is needing these respective voltages. The EN_CARD controls the 48V input and is enabled by the FPGA. The 2.5V is derived from the 3.3V to 2.5V voltage converter and is used by the FPGA and logic, as well as the I/O on the ADC. There is also a DC/DC-converter which makes the 1.2V out of the 3.3V. As a lot of focus has been put on reducing noise, a large number of filters have been added and make up a large share of the components.

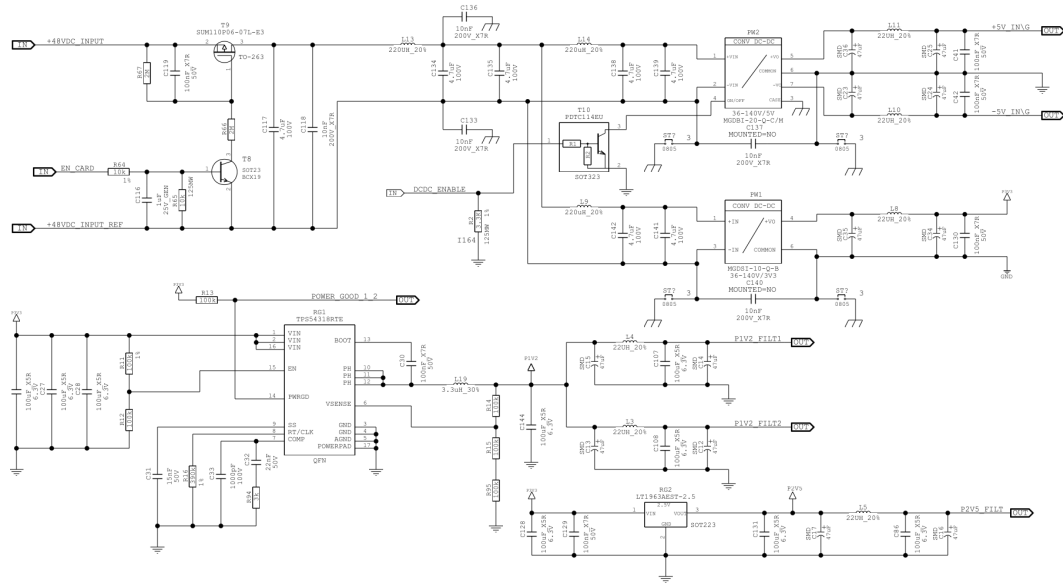


Figure 27: Circuit of the on-board Power supply.

Reliability assessment The voltage supply is understandably very important, and the consequence of failure will often cause the BLEDP-card to be rendered useless and important components will not function. The large numbers of filtering capacitors especially can often cause one or all of the voltage levels to be drained to Ground. This therefore means that the consequence will be the loss of all 8 detector channels. The 5V and 3.3V DC/DC-converters are also the lowest rated components, meaning highest failure rates, on the BLEDP-card and are heavy factors in the weighted average. However, the failure rates are good enough in terms of inferred life time expectancy from the documentation of the supplier, to not warrant changes.

FMECA		RPN - Worst FM		Failure rate		Summary
Total failure modes	49	Sum SxOxD	3	Total MTTF	3.497e+05	- Probability of failure is low - All FM is for 8 chan - Low RPN number No changes warranted
Category 2: Maintenance	0	Severity	3	Worst comp	1.33e+06	
Category 3: False dump	49	Occurence	1	> 20 years	Yes	
Category 4: Blind failure	0	Detection	1	Failure type	Random	

Figure 28: Reliability values and summary for the Power supply.

2.5.6 Connectors

Functionality The SFP-connectors, as there are 2, can be fitted with a optical and Ethernet module, depending on the desired connection. The SFP provides the link to the BLEPC and can therefore be used to send the digitalised data from the measurements, to the Processing Crate. The distance is not very long as the BLEAC and the BLEPC are in the same rack. The I2C connection is used to configure the SFP [12]. The rest of the components are mostly filters.

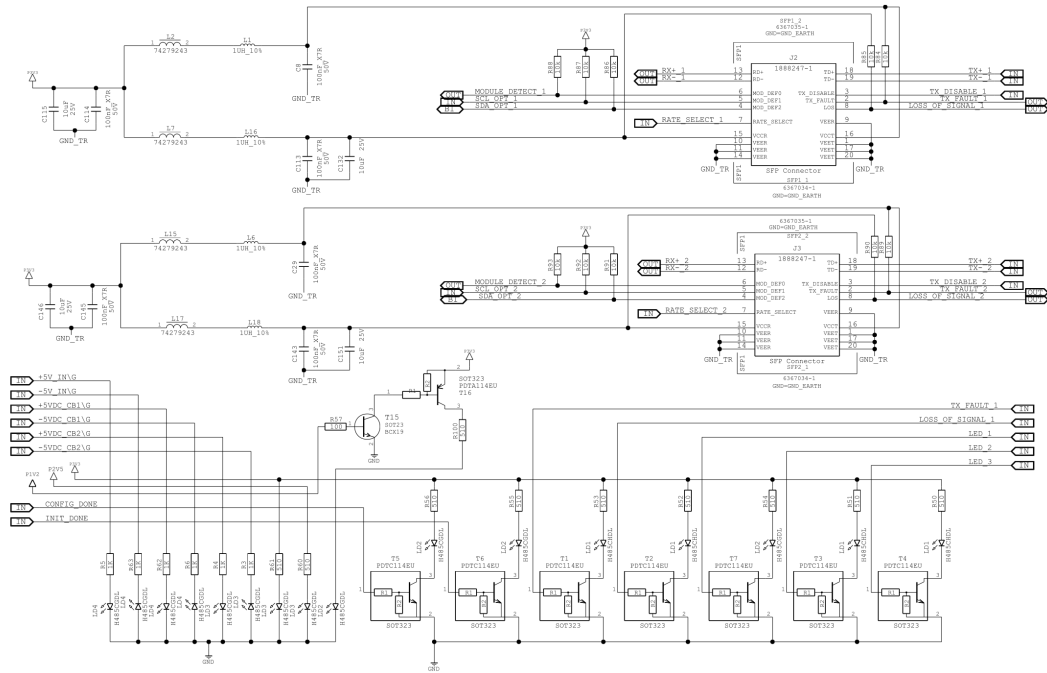


Figure 29: Circuit of the SFP and I2C Connectors.

Reliability assessment The connections are essential as the loss of a signal would cause the BLEDP-card to be unable to send out the measurements. Here there are many components who do the same job as well, so although many of the failures would cause the same end effect, a false dump, they would fail in the same manner, depending on it's location. A failure related to the transportation of data digitally is not generally included in the FMECA, but an erroneous signal would be detectable by the same self-diagnostics as for the BLEDP. There is also the same connectivity check as is used for the LHC [13].

FMECA		RPN - Worst FM		Failure rate		Summary
Total failure modes	10	Sum SxOxD	3	Total MTTF	3.301e+05	- Probability of failure is low - All FM is for 8 chan - Low RPN number No changes warranted
Category 2: Maintenance	0	Severity	3	Worst comp	7.556e+05	
Category 3: False dump	10	Occurence	1	> 20 years	Yes	
Category 4: Blind failure	0	Detection	1	Failure type	Random	

Figure 30: Reliability values and summary for the SFP and I2C Connectors.

2.5.7 Relays & Calibrations

Functionality In addition to the injection of a known current to verify that the measurement channel and that the following chain of equipment is working correctly, this reference current system is also used to calibrate the system at start. The BLEDP-card will, on start-up, go through a chain of tests and checks, including the calibration procedure which is used to make sure that there is a known reference point in each channel. The failure of such a calibration and the lack of relay activation commands will cause the system to be unable to start.

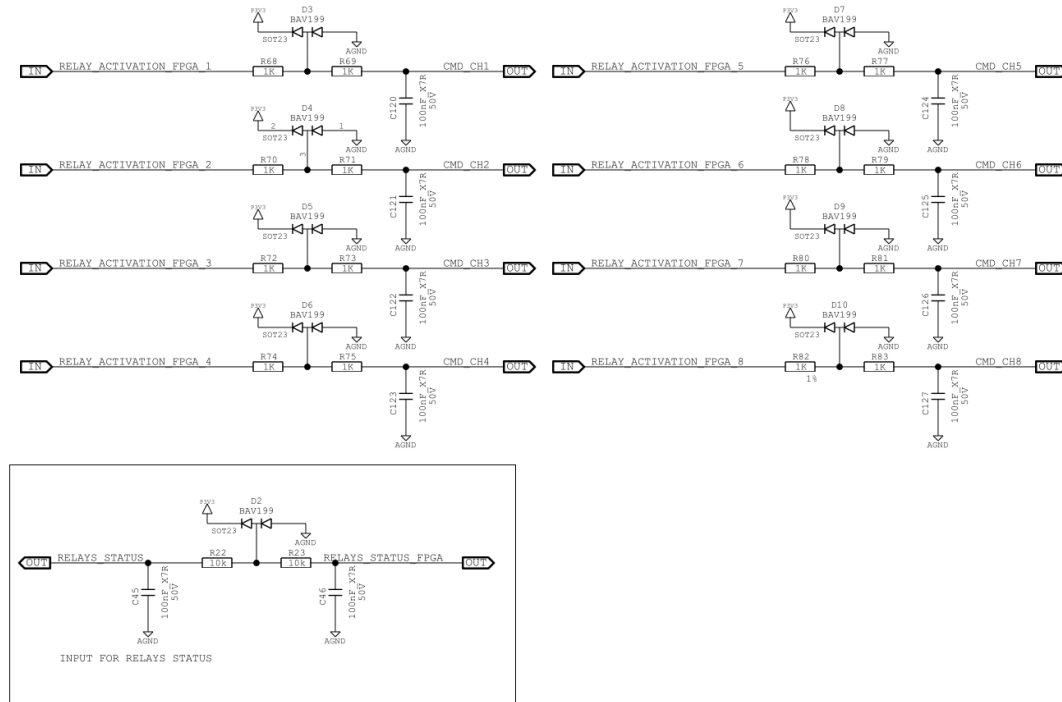


Figure 31: Circuit of the Relay Activation and Status.

Reliability assessment In terms of reliability, there are a total of 8 failure modes where 2 are maintenance cases for the clampers, as they are for protection. For the filters, if any of them fail, especially if the resistors fail open or the capacitors fail shorted, it will cause the signal to either be distorted or denied which will cause the system to fail calibration checks at start. Due to this circuit block having very few components, the overall weighed failure rate is relatively low.

FMECA		RPN - Worst FM		Failure rate		Summary
Total failure modes	8	Sum SxOxD	3	Total MTTF	1.25e+07	- Probability of failure is low - No Blind Failures - Low RPN number <u>No changes warranted</u>
Category 2: Maintenance	2	Severity	1	Worst comp	2.153e+08	
Category 3: False dump	6	Occurence	1	> 20 years	Yes	
Category 4: Blind failure	0	Detection	1	Failure type	Random	

Figure 32: Reliability values and summary for the Relay Activation and Status.

2.5.8 Misc. circuits

Functionality This is a collection of secondary functions which are not directly related to the essential measurement chain, but still provide beneficial functions which should be fixed as soon as possible, if broken. The temperature and humidity sensor provides local temperature and relative humidity values, and is continuously logged and stored. This makes it possible to map temperature variations for use in diagnostics purposes. The Serial Number Generator provides the BLEDP-card with it's unique ID, which allows for geo-localisation of measurements and diagnostics values, as well as a quick way to identify the correct card when there is a need for maintenance. Outside of the main components, both of these have just basic filtering and pull-up resistors and their output goes to the FPGA. The High Voltage indicator provides a method to detect the continuous presence of high voltage in the detectors. Finally, there is the 12-bit housekeeping ADC which sends housekeeping data to the FPGA; that the circuit breakers are working and the HV_value.

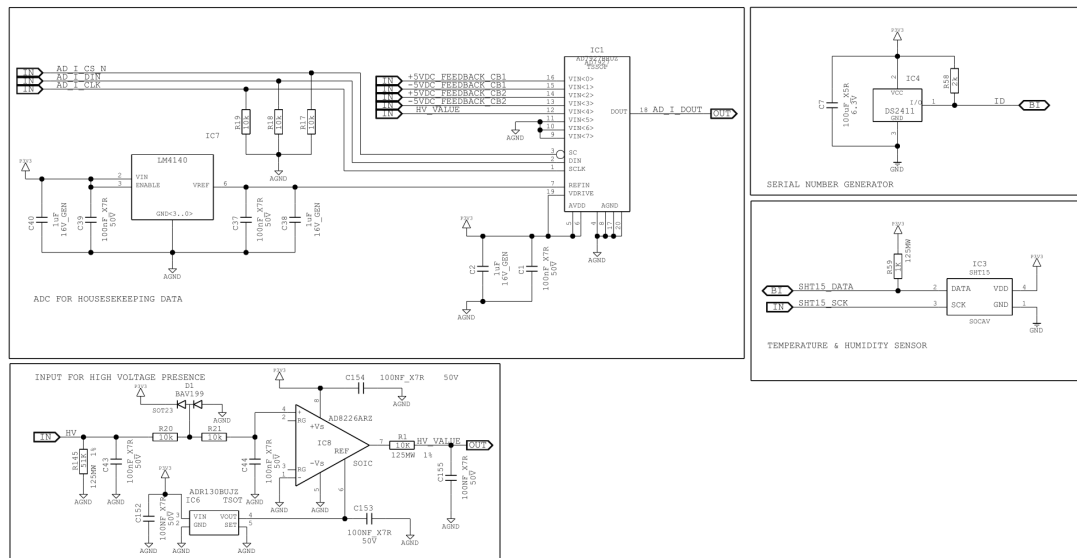


Figure 33: Miscellaneous circuits.

Reliability assessment Although the loss of the housekeeping ADC is critical, it will not mean that the system is not capable of operating safely, only that the connectivity check is not working. It is therefore a single failure tolerant system, meaning that there would also have to be a secondary failure for there to be an issue. This can however lead to a Blind Failure as explained in the Input Monitors and will cause the circuit breakers to fail to start at the next run and should be fixed ASAP.

FMECA		RPN - Worst FM		Failure rate		Summary
Total failure modes	37	Sum SxOxD	2	Total MTTF	1.267e+07	- Probability of failure is low - Only Maintenance - Housekeeping data No changes warranted
Category 2: Maintenance	37	Severity	2	Worst comp	1.158e+08	
Category 3: False dump	0	Occurence	1	> 20 years	Yes	
Category 4: Blind failure	0	Detection	1	Failure type	Random	

Figure 34: Reliability values and summary for Miscellaneous circuits.

2.5.9 FPGA

Functionality The FPGA is integral for the operation of the BLEDP. The chip is an Altera Cyclone IV, and it controls most of the analogue circuitry and control operations. The FPGA defines the start and stop of the acquisition period, it keeps a count of the number of pulses occurred in the acquisition period, as well as clocks the ADC circuitries, directs which acquisition technique is active for each channel and makes differences of the recorded ADC values. Finally, it processes the data, meaning it merges the values acquired in the counter and the ADC for each measurement channel, and provides the integral of the losses measured for each channel over the last $2\ \mu\text{s}$ period. The algorithm it uses is defined here [11]. To operate the FPGA there is also an EPC code chip for memory, an FPGA reset block, and an oscillator. Outside of this, most of the other components are related to filtering.

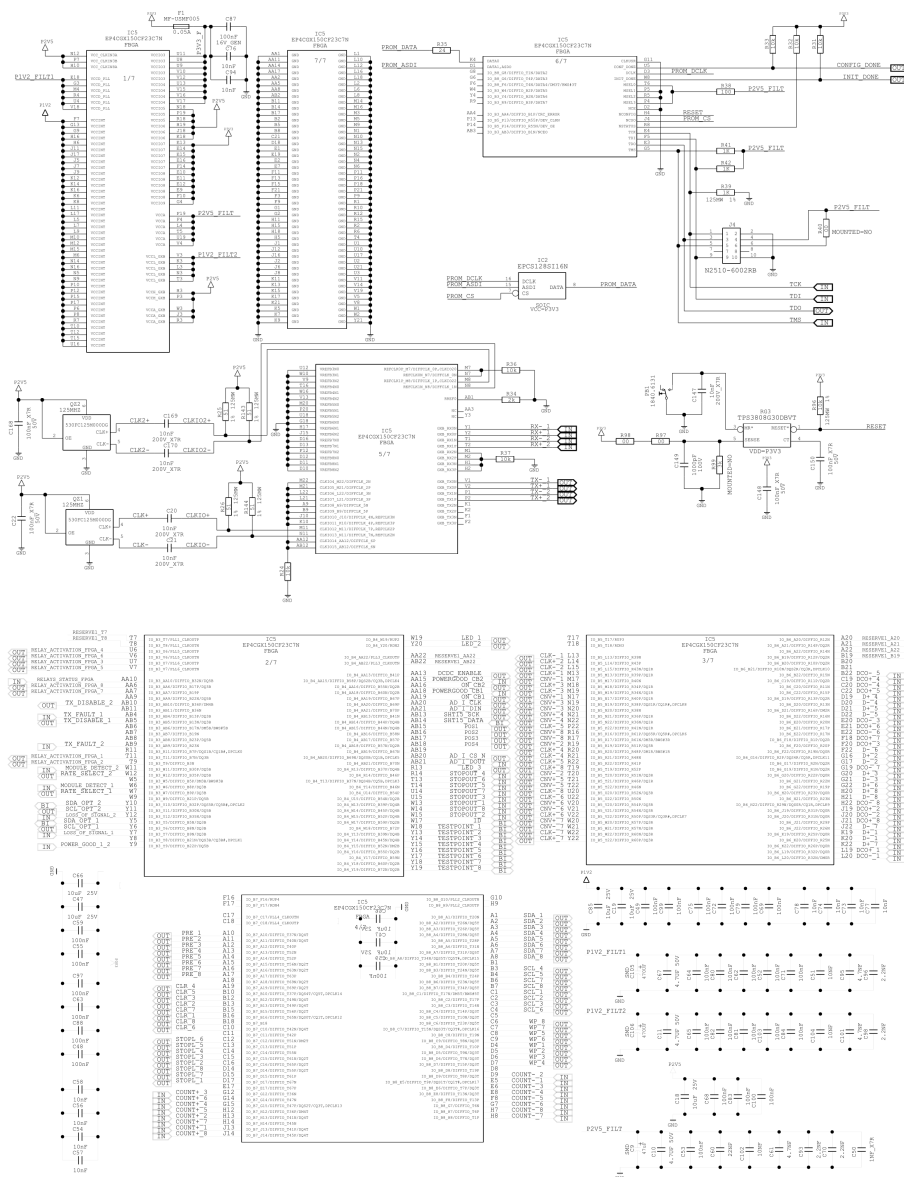


Figure 35: Circuit of the FPGA and support components.

Reliability assessment As the FPGA is controlling and performing [11] many of the important functions in the card, it's vitality is unquestionable. However, to include the FPGA can be a bit challenging as there is a certain necessary boundary between the mechanical errors of a physical system, and what can go wrong in the programming. As such, a solution was to look at the FPGA as a black box which produces a certain output. At the same time, this FPGA was 420 I/O pins, and to map out the failure modes of every single output would be a massive task, and serves no real purpose as the end results of the failures would still follow the main end effects of the system. Therefore, the FPGA has been treated as a black box with a focus on the end effects. But, as the card is to be used as a front end acquisition module for particle accelerators, there are certain failure modes which can cause problems within the FPGA, that is not the case of generic random failures. Therefore I've added some failure modes which are more related to particle physics and especially for equipment in radiation environments [14].

This is a complicated field and so I've only added the failure modes and assessed their consequences. To calculate failure rates and so on requires careful manual study and radiation testing, and that was a little over the intention of the reliability analysis which is looking at this from the design process. Also issues like mitigation techniques in FPGA's has been left out for the same reason.

The failure modes are related to what is known as Single Event Effects and are as follows:

- Single Event Upset (**SEU**) - A change of state caused by radiation striking a sensitive node in a micro-electronic device.
- Single Event Functional Interrupt (**SEFI**) - Special SEU, which affects one specific part of the device and causes the malfunction of the whole device.
- Single Event Latch-up (**SEL**) - A parasitic PNP-structure (thyristor) gets triggered, and creates a short between power lines.
- Single Event Gate Rupture (**SEGR**) - Destruction of the gate oxide in the presence of a high electric field during radiation (for example during EEPROM write).
- Single Event Burnout (**SEBO**) - Destructive and occurring in power MOSFETs, BJTs, and power diodes.

Most failures in either the FPGA directly or the support circuitry, will cause the FPGA to malfunction and consequently this means the loss of the BLEDP-card entirely. The FPGA itself has a relatively high failure rate compared to the other components on the board, and statistically speaking it should fail first, but the expected operational time is still higher than the 20 years required. The maintenance cases are related to the reset.

FMECA		RPN - Worst FM		Failure rate		Summary
Total failure modes	26	Sum SxOxD	4	Total MTTF	1.076e+06	• Probability of failure is low • Loss of 8 detectors • FPGA will fail first • <u>No changes warranted</u>
Category 2: Maintenance	3	Severity	2	Worst comp	3.701e+06	
Category 3: False dump	23	Occurrence	1	> 20 years	Yes	
Category 4: Blind failure	0	Detection	2	Failure type	Random	

Figure 36: Reliability values and summary for Miscellaneous circuits.

2.6 Detectability and severity ranking

An important factor in the reliability analysis is the systems ability to detect and act on failures as soon as possible after they happen. Therefore, an effort has been put into providing the system with a number of checks, in order to better guarantee the important safe operation and to avoid the critical Blind Failures. The definition and qualification requirements for the severity cases are slightly broad, as failures was put into three reaction brackets which leaves limited room for manoeuvring. Blind Failures are nonetheless placed so high as to normally warrant special focus on this area from a design point of view.

For the False Dumps, there are two main end effects which make up the consequences and the qualifications of being labelled a False Dump. One is when there is an erroneous measurement, with the system being aware of such an error. This means that some part of the measurement chain fail in such a way that there is a measurement, but it's distorted by the error. This is partially continuously detectable, if there exist an instance in the measurement chain which is capable of recognising a measurement out of proportion or within reasonable behaviour. If no such function will be implemented, it's still detectable with the calibration checks.

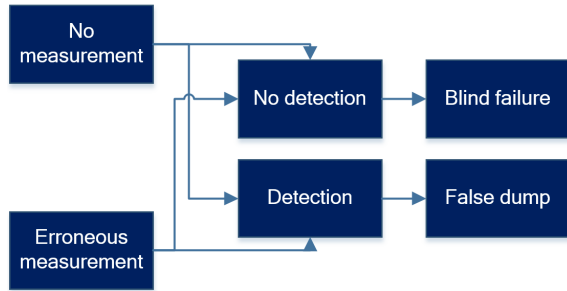


Figure 37: Consequences of main failure types.

The second one is the failures which causes some part of the system to fail entirely, for example the FPGA dying or one Circuit Breaker failing. These are easier to detect as many functions will stop to work and leave the system inoperable. Many can be detected as diagnostics will show something is wrong. However, some specific scenarios can cause a problem for either of these two: If one part of the system fails in a way that makes it look like there are no beam losses, meaning no current, and the diagnostics can't detect that there is a failure, or if the measurements are wrong or unable to cause a protective Beam Dump and this error can't be detected. In other words, a Blind Failure caused by, for example, a component failing open that can't be detected. Such failures are the main goal to prevent with the FMECA-analysis and the analysis of the checks.

At the current iteration of the BLM-system, some False dumps might technically be a Blind Failure for a short amount of time, but such failures in the detection process chain, will be picked up at least after 10 hours which is the run time of one mission. This is because the BLMs will, before each run, check itself so that it can be viewed "as good as new". As such, a Blind Failure by definition is difficult to guarantee to avoid entirely. But if they are detected at least within the run time of 10 hours, or before the start of the next run, they are judged to be a False Dump as the system aborted or failed to get beam permits due to detected failure of the detection system.

The idea then is that there is a difference in the Blind Failures caused by permanent undetectability, and temporary Blind Failures which can be detected quickly but not instantaneous. As such there can be an undetectable False Dump, meaning that there is a failure which causes the system to abort, perhaps due to the Threshold being met because of some processing error. And there can as well be a detectable Blind Failure, as these are detected within the next run. There are also some other mitigating factors, such as that debilitating Blind Failures are not possible for the vast majority of components, cabling or detectors due to the checks and diagnostics. The result is that a Blind Failure in these ultra rare cases and chains of events, are so statistically unlikely to cause a problem due to a same time critical beam loss, that it's hard to warrant costly counter measures.

Outside of the two mission critical severity cases, there are also the Maintenance cases. These are not threatening to the system or the mission, but they should be fixed as soon as reasonably possible. Because they are not critical, it's OK if they are detected at dedicated maintenance checks, but detection of these can also be made with the diagnostics feedback, since many would also cause consequences which are inconsistent of normal behaviour such as showing an impossible temperature.

Risk Priority Number Matrix

1	Severity				
	X	1	2	3	4
	Detectability	1	1	2	3
	2	2	4	6	8

2	Severity				
	X	1	2	3	4
	Detectability	1	2	4	6
	2	4	8	12	16

3	Severity				
	X	1	2	3	4
	Detectability	1	3	6	9
	2	6	12	16	24

4	Severity				
	X	1	2	3	4
	Detectability	1	4	8	12
	2	8	16	24	32

RPN System
SxOxD = RPN

Severity
1. No effect
2. Maintenance
3. False dump
4. Blind failure

Detection
1. Detectable
2. Not detectable

Occurrence
1. > 20 years
2. > 10 years
3. > 1 year
4. < 1 year

Figure 38: Severity matrix for the BLEDP, using RPN.

All of these severity cases has been put into a system for reliability called the Risk Priority Number, or RPN. This system is useful for getting a better overview of the different acceptable or unacceptable circumstances for the failures. The system, which is a multiplication of Severity, Occurrence and Detection, provides a quick way to assess the reliability aspect, and to see what effect changes has on the value. The values themselves can be obtained through various combinations, so it's not something to use blindly, but if used correctly it can be a good way to get a notion of the situation. This system can be found in the FMECA-analysis which is in the appendix.

The difference between the Maintenance cases and the No Effect cases is that Maintenance cases is a failure in a higher order function and should perhaps warrant an intervention in between a run, while the No Effect cases are of very minute things like one filtering capacitor failing in a way which have little effect on the overall performance.

However, these components are there for a reason, and should such components fail often or in a great number, they might cause problems. As such, although the severity is not as high as the other severity cases, it's not desired to have many such components failing every year, or to have a large number of Maintenance cases every 3-4 years. As such, all the RPN-numbers are subject to a independent and relative estimation which also affects the recommended actions.

Detection is again really important for this system, so in addition to the checks that are already in place, another task is to see if there can be added any new checks to the system which can decrease the likelihood of Blind Failures. However, before I do that, I will make a short list of the checks that are already in place, explain them briefly, and then try to add to that.

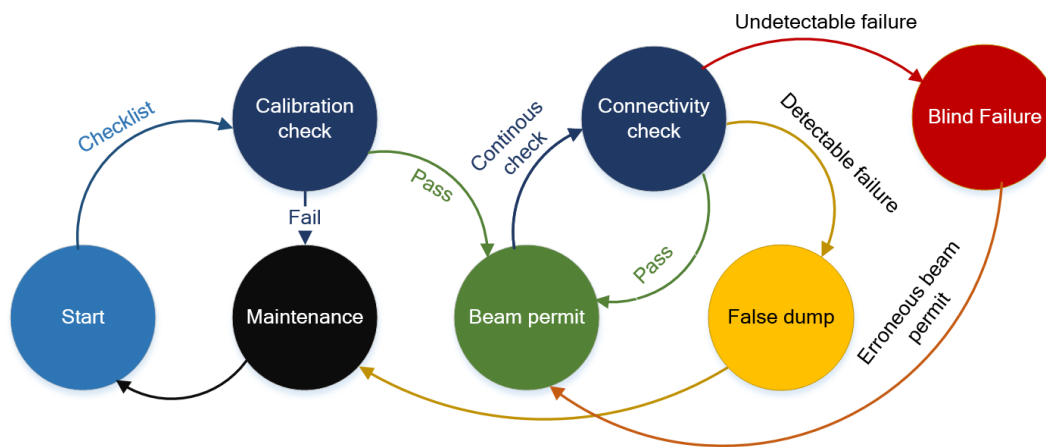


Figure 39: State progression of the BLMs hardware checks.

Calibration Check - Included The calibration check is the check which uses an adjustable current on the input of the acquisition card to test and see that the electronics are working correctly. This has been described earlier in the subsection related to the Input Monitor. At the start of every run, the reference current is injected and measured by digitising it as a normal measurement would be, and sending it to the BLEPC as normal. After passing this test for every channel, the BLM-system will continue with the start-up check-list and will ultimately lead to a Beam Permit being given by the Beam Interlock if everything is OK. This test is good for the purpose of checking the BLM-system, but it does not include the detectors themselves, the cables and one shunt on the input monitor which is before the current injection.

Connectivity check - Included The connectivity check [13] is something which was implemented for the BLM-system used in the LHC and is to be implemented for the LHC-injectors as well. Here the high-voltage supply for the two most used beam loss detector types are used to check their connectivity, as well as the integrity of the acquisition system. This is done by adding an harmonic modulation signal of 0.03Hz which will cause a current signal of around 100pA to be produced, and can be measured by the acquisition system. The connectivity check will be used for all the detectors every 12 hours, and lasts about 20 min. By checking this for every channel, it can verify the conformity of the detector system, or if non-conform, deny the Beam Permit to be give.

Continuous low current input test - Recommended The LHC BLM-system uses a 10pA input current which is created by the ADC for each channel, and causes a bit change every 5 milliseconds or a CFC-count (the equivalent to the BLEDP measurement system) every 20 seconds. If no count arrives in 22 seconds, the FPGA increases the current by 1pA and if nothing is detected after 5 iterations it will be declared Blind, and cause a False Dump. Such a continuous check of the system is of great help towards validating the on-going correct operation of at least the front-end electronics of the acquisition card.

2.7 Crosstalk protection

Another critical part of the BLM-system is that there isn't any crosstalk [10] noise between the channels. Therefore a crosstalk test between acquisition channels has been done. The execution of these tests required to inject in a sinusoidal waves in one of the channels of the BLEDP, square waves (at several frequencies), and fast pulses, leaving the other channels unconnected. Then the 2ms samples collected by the BLEDP-card have been treated in MATLAB to make a FFT-analysis. The worst case crosstalk is 130 dB at 10 kHz with a square wave signal injection. In figure 40 it is possible to see the result of the crosstalk performance when several current frequencies are injected (on the top side), or the crosstalk performance converting the injected current at certain frequency in loss Protons per time (on the bottom side).

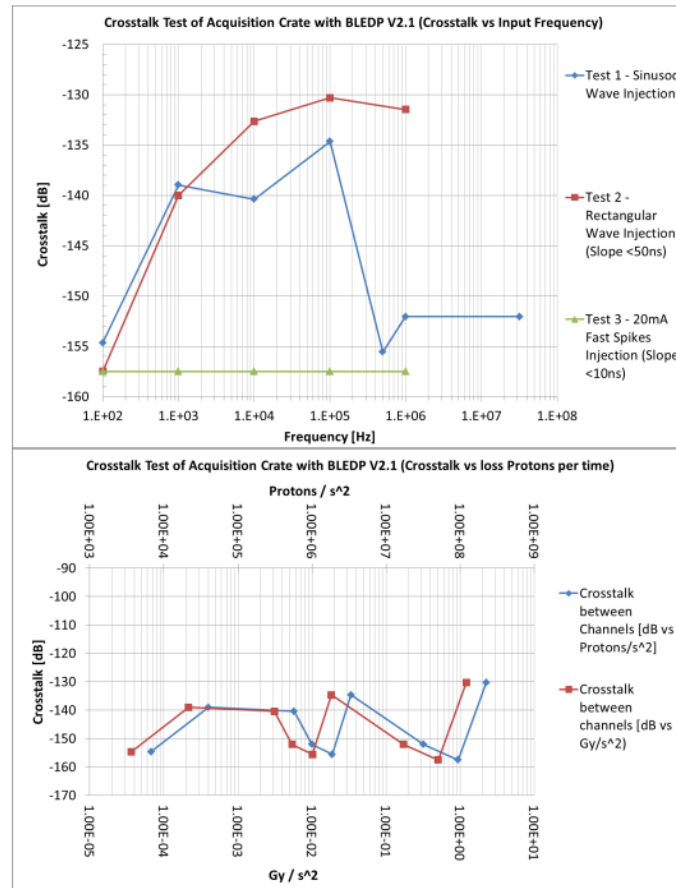


Figure 40: Crosstalk [1].

3 Reliability

Here follows a description of the reliability tools used in the work. The idea is to give a short presentation of what reliability is, some of the key points regarding the theory and definitions, and to explain both how the analyses work in general and how they were implemented by me for the purpose of this work. This is therefore not intended to discuss the direct results of the work, but what choices I made to create the reports.

3.1 Introduction

For a long time, the common quality target for manufactures and the desired quality target for customers, was merely that the manufactured item was free of defects and systematic failures at the time it left the manufacturer or reached the customer. But as technology progressed and evolved, equipment and systems continued to become more and more complex, and with that, also more costly when the equipment or system had a loss of operation as a consequence of failure. To combat this, and to try and reduce things like systemic failures and defects, a lot of progress was made, primarily since the early 1960's, in the fields of Reliability, Availability, Maintainability and Safety which is also collectively known as RAMS. They are often grouped together because they are many times either closely linked or even crossing over in each other.

Today, the expected quality target of equipments or systems are not only that they are without problems after construction ($t=0$), there is also now a strong want, a requirement, that the equipment or system is free from defects and systematic failures and capable of performing it's intended task problem free, for a stated time interval. In addition, it's also often required to have a fail-safe function to prevent damage to the system itself and others, and so protect itself from critical or catastrophic failures. To make such a prediction on whether or not the equipment or system is capable of performing its task until the end of a desired time interval, it's not enough to simply try and achieve a direct yes or no answer. Only a probability of a failure occurrence can be given with a certain amount of confidence. This probability is a measurement of an item's reliability and is described as follow:

"If n statistically identical items are put into operation at time $t=0$ to perform a given mission and $v \leq n$ of them accomplish it successfully, then the ratio $\frac{v}{n}$ is a random variable which converges for increasing n to the true value of the reliability." [15]

This shows that the reliability value is a function of the ratio between working units and total units after the intended time period is finished, and that the higher amount of samples you have, the closer you get to the true value of it's reliability. This also shows that when dealing with statistical inferences, the value outputted is not better or worse than the data used to do the calculations and so the values don't mean anything without an intimate understanding of the process upon which they were obtained. And even then, it's important to remember that the statistical inferences are inductive approximations and have to be used correctly in order to be valuable. But, once a methodology which adheres to the reliability theory has been chosen, and once the tools decided on has been form-fitted to the task, the analysis can be very profitable as a preventive and validity measure.

3.2 Definition of reliability

Reliability is also commonly defined as:

"The ability of an item to perform a required function, under given environmental and operational conditions and for a stated period of time" [ISO 8402]

This basically means that reliability is an item's resistance to failure over time. Reliability applies to both repairable and non-repairable systems as one can, for example, have a failure in a redundancy component which does not impede system operation and can be repaired. To make any sense, the numerical statement of reliability, for example $R = \frac{\text{Operational units}}{\text{Total units}} = \frac{94}{100} = 0.94$, must be accompanied by the definition of the required functions, the operating conditions and the mission duration. The required function is defining the task of the item, for example the role of a capacitor and its operational parameters. From this you also define failures, and so this is the foundation of most reliability analyses. The operating conditions are also hugely important as they affect the failure rate of items a lot. An example is the operating temperature, radiation environment, mechanical effects and so on. Lastly is the time factor which indicates a representative mission profile.

Reliability is often denoted simply as R , and since mission duration is usually considered a parameter, the reliability function is then defined by $R(t)$, where $R(t)$ is the probability that no failure will occur in an item in the interval $(0, t]$. Evidently, the condition (for example if its used before) of the item at the measured $t=0$, also matters a lot. Another consideration which is important to bring out is the distinction between predicted and estimated / assessed reliability. Predicted reliability are calculated values based on the item's reliability structure and failure rate of its components, while estimated reliability is based on a statistical evaluation of reliability tests or from field data by known environmental and operating conditions. Which to use depends on the intended role of the analysis, where in the creation process you are and what data is available.

For the BLEDP-card the reliability values related to the obtained MTTF-values, are of the predicted variety, and is therefore often called simply the Prediction in this Thesis. The intended use and value of such an analysis then, can be both to estimate the current reliability of the system based on what is obtainable, and to view how design changes will affect the system. So even outside of any proclamations of estimated life time, such an analysis can be useful as a reference tool in the creation process as it can give a objective value between different types of priorities. An example can be to sacrifice on the electrical MTTF so to speak, in order to obtain a better resistance to radiation. Meaning, choosing components which have a lower MTTF-value than other options, but also has a better resistance to radiation, and how to balance the pro's and con's. As such, a reliability analysis can have a multitude of uses and dilemmas which are not always obvious or intuitive.

Regarding mission time, the BLM-system has a lifetime of about 20 years, and so the individual items is designed to match this as best as possible. Yet, given that the failure modes are mostly triggered by random failures, certain problems will occur periodically. So the goal is to limit the errors and their consequences as best as possible. But, due to the self-checks and diagnostics after each run, the strict $R(t)$ is 10 hours, the same as the mission time of the particle accelerators, per run.

3.3 Basic concepts

The mathematical part of the reliability theory is founded heavily on probability theory. One important concept in reliability is the cumulative distribution function $F(t)$ [16], where it is defined as the probability in a random trial that the random variable is not greater than t , or:

$$F(t) = \int_{-\infty}^t f(t)dt$$

where $f(t)$ is the probability density function of the random variable, time to failure. $F(t)$ is known as the "unreliability function" when speaking of failure and can be thought of as representing the probability of failure prior to a time t . If the random variable is discrete, the integral is replaced by a summation. Since $F(t)$ is 0 until $t=0$, the integration above can be from 0 to t .

The reliability function $R(t)$, meaning the probability of a device or component not failing prior to a time t , is defined as:

$$R(t) = 1 - F(t) = \int_t^{\infty} f(t)dt$$

After differentiating the equation above, it can be shown as:

$$\frac{-dR(t)}{dt} = f(t)$$

The probability of failure in a given time interval between t_1 and t_2 can be expressed by the following reliability function:

$$\int_{t_1}^{\infty} f(t)dt - \int_{t_2}^{\infty} f(t)dt = R(t_1) \cdot R(t_2)$$

The failure rate $\lambda(t)$ is the ratio of probability that failures occur in the interval t_1 to t_2 , provided that it has not failed prior to the start of the interval, divided by the interval length. And so:

$$\lambda(t) = \frac{R(t_1) - R(t_2)}{(t_2 - t_1)R(t_1)}$$

or rewritten:

$$\lambda(t) = \frac{R(t) - R(t + \Delta t)}{\Delta t R(t)}$$

where $t = t_1$ and $t_2 = t + \Delta t$.

The hazard rate $h(t)$, also known as the instantaneous failure rate, is defined as the limit of the failure rate as the interval length approaches zero:

$$h(t) = \lim_{\Delta t \rightarrow 0} \left[\frac{R(t) - R(t + \Delta t)}{\Delta t R(t)} \right]$$

giving:

$$h(t) = \frac{-1}{R(t)} \left[\frac{dR(t)}{dt} \right] = \frac{1}{R(t)} \left[\frac{-dR(t)}{dt} \right]$$

Knowing that

$$f(t) = \frac{-dR(t)}{dt}$$

we can substitute this into the $h(t)$ equation, giving us:

$$h(t) = \frac{f(t)}{R(t)}$$

This relationship is one of the most fundamental relationships in reliability analysis. From this, if you have, for example, the density function of the time to failure, $f(t)$, and the reliability function $R(t)$, you can find the hazard rate function for any time t , and conversely.

Mean-Time-To-Failure MTTF is often used interchangeably with Mean-Time-Between-Failures, MTBF, but there is a difference in their areas of application. MTTF is used for systems which are not repaired, but instead exchanged after a failure has occurred. Alternatively, the MTBF value is used for systems which are repaired upon failure and includes the expected repair time in-between failures. MTTF is known as the expected value of time to failure, and is derived as follows:

$$MTTF = \int_0^{\infty} tf(t)dt = \int_0^{\infty} t \left[-\frac{dR(t)}{dt} \right] dt$$

By integrating by parts and applying "L'Hopital's rule", you get the following expression:

$$MTTF = \int_0^{\infty} R(t)dt$$

If you know the reliability function $R(t)$, the MTTF can then be obtained by directly integrating $R(t)$.

Example[17]:

An item with a reliability function $R(t)$:

$$R(t) = \frac{1}{(0.2t + 1)^2}$$

where t is measured in months, gives a probability density function:

$$f(t) = -R'(t) = \frac{0.4}{(0.2t + 1)^3}$$

and a failure rate function of:

$$h(t) = \frac{f(t)}{R(t)} = \frac{0.4}{0.2t + 1}$$

The mean time to failure is then:

$$MTTF = \int_0^{\infty} R(t)dt = \underline{\underline{5 \text{ months}}}$$

3.4 Software

Isograph is a company that develops software applications for reliability, availability, maintainability and safety (RAMS) focused systems. For reliability purposes they have developed the Reliability Workbench (RWB) tool. This is an application that allows the user to perform a variety of different reliability functions that you will normally find in a reliability focused project. The different reliability topics are split up in modes which allows the user to either do a singular analysis, such as finding failure rates as a function of time, or implement the modes together and inherit properties as you progress down your different analyses, such as identifying failure rates and easily bringing the items to a FMECA or Fault Tree analysis. The RWB modes used are:

- Prediction (Failure rates / MTTF)
- Failure Mode, Effects (and Criticality) Analysis (FMEA / FMECA)
- Fault Tree Analysis (FTA)

It also can use other types of analyses that aren't included in this Thesis. These are Reliability Block Diagram; Weibull; Markov; Reliability Allocation; and Reliability Growth. In addition the software allows you to either use SQL, or choosing your preferences from a check box list, to automatically create reports from the desired information you have pointed out and wish to have in your report. There is also a very handy library system that allows you to store the configurations for a large number of items / components which you expect will be used often. This library you can also share to other users who may also be a part of the project, or whom work with the same components. The project itself can be configured to include more users, and a supervisor can add or remove project members to better manage a more complex project.

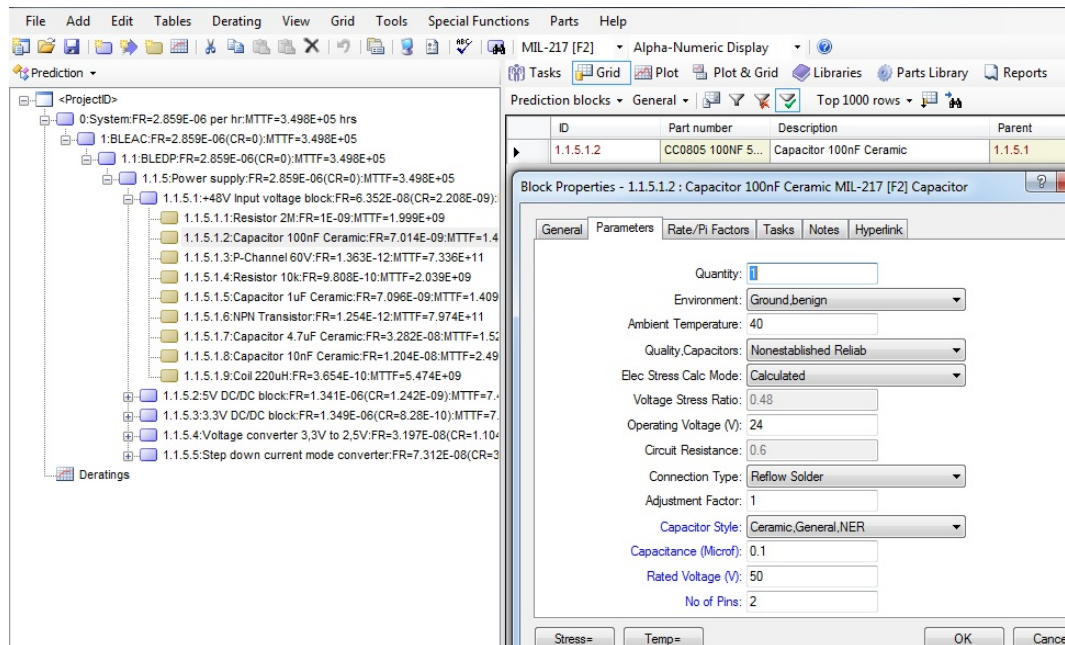


Figure 41: Isograph GUI and the parameters for a ceramic capacitor

3.5 Prediction

The Prediction analysis in general is the analysis which deals with the prediction of failure rates in components or equipment. The Prediction module in Isograph Reliability Workbench is a reliability prediction programme which uses internationally recognized methods for calculating electronic equipment reliability, including the MIL-HDBK-217 (F2), which is one of the most used standards for electronics failure rate calculations. The standards use a range of different models for various categories of electronic components which are affected by environmental conditions, quality levels, stress conditions and numerous other parameters. Each model is described in the standard used. One of the hugely beneficial thing about using a software like Isograph for large collections of components is the scalability and re-usability of component data.

In the handbooks, you would have to reproduce each calculation for each component, even if the parameters only change a little bit. Many of the component models use some ten or more parameters to calculate the component failure rate. Needless to say, this would take a very long time for a large number of components and would be inconvenient and inefficient especially when one is focusing on reusing the same type of components in order to, for example, reduce production cost. The values chosen to be focused on, here the MTTF, are automatically summarized in the tree structure as shown in Figure 6, where each tier shows a weighted average of all the following tiers. The blue boxes represent system blocks, and in this case, they are circuit blocks that have been identified in the schematics. They are subjectively chosen by the reliability analyst based on function, or agreed upon in the project group. System blocks have global parameters, meaning they affect all components connected to the block, which can be used to set certain parameters automatically on new components or change all variables in the existing block.

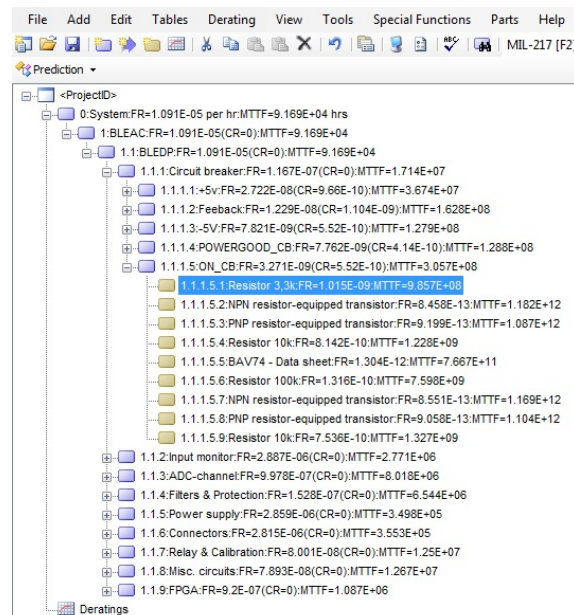


Figure 42: Project tree

The component blocks, the yellow boxes connected to the system blocks, are directly tied up to the MIL-HDBK-217 which has been used for this work. This means that when a new component is added, you are given a range of component types and choose the correct one from a list. From time to time you have components which does not really correspond to any of the possible choices. For this purpose you have three different types of custom component blocks where you can choose to put in a external reference failure rate (for instance supplier given), and if need be also adjust things like temperature stresses to take into account local parameters.

3.5.1 Project parameters for the Prediction

When deciding to produce a Prediction report for a piece of equipment or system, it is important to first identify and properly define the information needed from the analysis. This means that you need to know what type of information you wish to calculate, for example failure rate vs availability, and then decide which variables are important to take into consideration, outside of the circuits themselves. Normally this is subjective, but within a certain methodology, and requires a thorough understanding of the system and it's environment. As such, a Prediction analysis can vary greatly and because of this, it is very important to declare both what precautions have been taken in terms of discovering variables which might affect the integrity of the analysis and what exactly you are calculating, as a report without the possibility to backtrack this is virtually useless. Therefore, below follows what settings and variables have been used for the Prediction module.

Project Options: The System ID is set to the BLEAC, even though the reliability analysis is limited to the BLEDP, and this is because the BLEAC is the current highest tier on a system level in this project. The project is small enough to not warrant an elaborate labelling system. However, a higher tier has been included as an inactive option, just in case it is desirable to expand the reliability analyses in the future. No targeted failure rate is being used as the objective is to discover the current failure rate of the BLEAC, and not work towards a certain explicit limit. System lifetime is only used for unavailability values which is not used in this work, however the mission time is 10 hours, so it is set to 10 hours for potential future use.

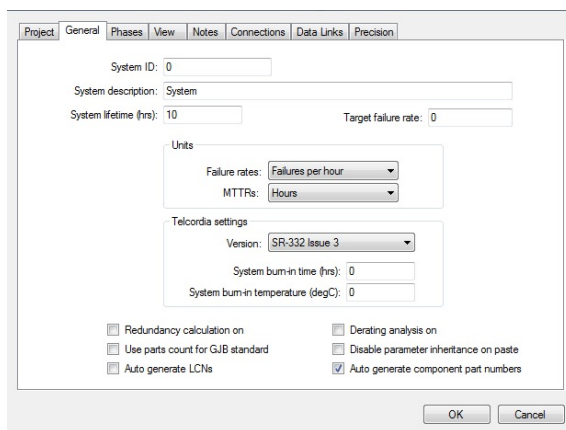


Figure 43: Project options

The desired unit is set to Failure rates / MTTF and the failure rates are set to FAILURES PER HOUR as this is required with the mix of values of military standards and supplier given values. Changing to, for example, per million hours, causes the military handbook values to be calculated in this form (much smaller number), while the supplier given failure rates continue to be in the per hour form which makes the calculation wrong because the supplier given values will seem, literally, a million times better in terms of failure rate, than they actually are. Derating analysis is not set as all components are well within their operational range by design, and therefore does not require a sensitivity check outside of just auto-detection of overloaded components. Redundancy calculations are not necessary as no redundancy is present, this because damage to a BLEDP card will cause the particle accelerators to abort operation and dump the beam, and the BLEDP card will be replaced. Phase cycling due to temperature variations have been enabled to two cycles, representing one day of 24 hours. One cycle for 12 hours is set to 30 degrees Celsius and the other for 12 hours and 40 degrees Celsius. These temperatures are seasonal measurements of the room in which the crates will be placed.

3.5.2 Prediction module report structure

The end result of a Prediction analysis is the report. A number of factors have been considered in the construction of the Prediction report. Firstly, a major emphasis have been put on giving the report a transparency and data resolution which should give the reader a broad level of relevant details in order to give an indication of what is a problem in potential problem areas, without having to go through the software. Secondly, given the high amount of components, a strong emphasis have also been put on readability, meaning that it should also be easy to pinpoint what is affecting the failure rates of the components, how the components affect the sub-block they are in, and so on. The report itself is a heavily modified template report which utilizes SQL to correctly list the actual Prediction information in the report.



System: BLEAC
Sub-system: BLEDP
Circuit block: Power supply
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	PI Values
			3.498e+5	System block	BLEAC	1	1	3.498e+5		40		
System block		1	3.498e+5	Sub-system block	BLEDP	1.1	1	3.498e+5	EDA-02365 -V3	40		
Sub-system block	BLEDP card	1.1	3.498e+5	Schematic block	Power supply	1.1.5	1	3.498e+5	N/A	40		
Schematic block		1.1.5	3.498e+5	Sub-block - 3.3V DC/DC	3.3V DC/DC block	1.1.5.3	1	7.414e+5	N/A	40		
				Sub-block - 5V DC/DC	5V DC/DC block	1.1.5.2	1	7.455e+5	N/A	40		
				Sub-block - Step down	Step down current mode converter	1.1.5.5	1	1.368e+7	N/A	40		
				Sub-block - +48V Input voltage	+48V Input voltage block	1.1.5.1	1	1.574e+7	N/A	40		
				Sub-block - Voltage converter	Voltage converter 3.3V to 2.5V	1.1.5.4	1	3.128e+7	N/A	40		
Sub-block - +48V Input voltage	+48VDC Input	1.1.5.1	1.574e+7	CC1210 10uF 25V 10%	Capacitor 1uF Ceramic	1.1.5.1.5	1	1.409e+8	C116	40	Ceramic, General, NE R	Base Failure Rate=9.9E-10, Environment=1, Quality=3, Temperature=1.922, Capacitance=1.23, Stress=1.011, Circuit Resistance=1
				CC0805 100nF 50V 10%	Capacitor 100nF Ceramic	1.1.5.1.2	1	1.426e+8	C119	40	Ceramic, General, NE R	Base Failure Rate=9.9E-10, Environment=1, Quality=3, Temperature=1.922, Capacitance=0.6128, Stress=1.512, Circuit Resistance=1

Figure 44: Prediction report example

The report is divided into two unofficial blocks; an information block and the actual report structure itself. The report structure is divided into three color coded sub structures depending on function. Firstly the information part on **the top**:

- **System, Sub-system and Circuit block** depict the structure as found in the project tree, which is based on the structure extrapolated, partly subjectively, from the schematics of the BLEDP. There is therefore a System level which depicts the overall system name, here the BLEAC, and from there the sub-system, here the BLEDP-card which is in the crate, and finally which sub-block in the BLEDP card. This is therefore a three-tier top to bottom system in order to pinpoint where we are exactly in the complex system.
- **Responsibilities, Prediction number, Date, Revision and Standard** is describing general information which is useful later for documentation especially when there is more distance between the users of the report and the analyst and designer. For example, the description of which standard is used is already important for understanding on which foundation the analysis is conducted and should always be included.

For the report structure itself, there are three parts:

- **Parent section** and the **Current section** are both four rows which indicate the same things: Type; Name; ID and MTTF. However, the blue one is always one tier higher than the red section. Meaning that if I am looking at a component, the parent section will show in which sub-block it is located. If I am looking at the sub-block, the parent section will tell me the details of the schematic block. Also, the rows are ranked from worst to best, so in each sub-block, you can always see which component is the worst, or if you are looking at the schematic block, you can easily see which sub-block is worst in terms of MTTF.

This gives a huge benefit as you can quickly detect, based on the knowledge that the values are a weighted average of all the lower-tier blocks or components, where there is a potential problem. This also means that if a sub-block is with a good number, all the components are therefore also good and you don't have to focus on them. This gives you the ability to quickly map out the problem areas and at the same time have the detail that allows you to check all the other components as well.

- **Parameters section** of the report is designed to provide additional information about the component in question. Firstly, if one want to find the component in question in the schematics, the schematic number gives a searchable opportunity to quickly locate component. In some cases, the components got the same name, but combined with the knowledge of what sub-block it is supposed to be it, it should not cause confusion. Following this is the Temperature used in the MTTF calculation. The standard value chosen is 40 degrees for all the components in this project, as it is on the conservative side which follows the methodology chosen for this project.

The last two rows show the Sub-category and the Pi values. In the sub-category you can see what kind of component category has been chosen. In the Pi values follows the parameters which belongs to the component category, and is derived from the standard used. The Pi values shows how the different parameters affect the base failure rate, and can give a picture on where the problem lies.

Most significant failure rates: As an addition, a graphical overview of the component failure rates measured on a logarithmic scale has been included for each sub-block in order to easier identify the failure rate distributions of the components.

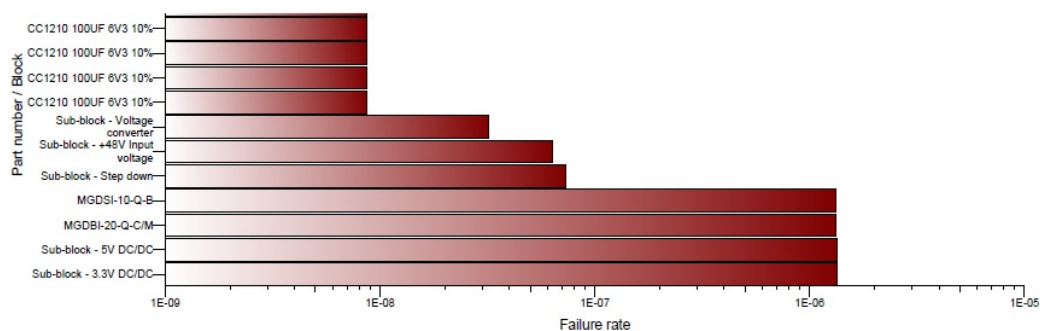


Figure 45: A 'Most significant failure rate' diagram example

3.6 FMECA

The Failure Mode and Effects Analysis (FMEA) was one of the first techniques for failure analysis, and was developed in the 1950s by reliability engineers who studied the problems that might occur from malfunctioning military systems [17]. The FMEA is many times the very first step in a systems reliability study. It involves reviewing as many components and sub-systems as possible in order to identify the failure modes and causes, and the effects of such failures. In order to make the analysis more systematic, each component are recorded in a special worksheet, which there are numerous variations of as they often are customized based on case specific requirements.

System:

Performed by:

Ref. drawing no.:

Date:

Page: of

Description of unit			Description of failure			Effect of failure		Failure rate	Severity ranking	Risk reducing measures	Comments
Ref. no	Function	Operational mode	Failure mode	Failure cause or mechanism	Detection of failure	On the subsystem	On the system function				
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)

Figure 46: Example of a FMECA worksheet

The FMEA will become an Failure Modes, Effects and Criticality Analysis (FMECA) if the criticalities or priorities are assigned to the failure mode effects. Even if there is a difference between the analyses, it's **most common to use the term FMECA for both situations**. The FMECA is used to identify and analyze:

- All potential failure modes of the various parts of a system.
- The effects these failures may have on the system.
- How to avoid the failures, and / or mitigate the effects of the failures.

As such, there are several usages for the FMECA, and some of the key points is that it can help in selecting design alternatives with high reliability especially early in the design process. It can also ensure that all conceivable failure modes and the resulting effects on the operational integrity have been considered. It can help with the development of criteria for test planning and also requirements for test equipment as well as maintenance planning. There is also the added benefit of creating historical documentation for future reference in order to aid in the analysis of actual field failures and planned design changes. From a reliability standpoint, doing an FMECA can be hugely beneficial. In effect, it is used to identify, prioritize and eliminate potential failures from the system, design or process before the equipment is being used in a critical system or, for example, is sold to a customer. This is a qualitative analysis, and is normally carried out by either the designer or the reliability responsible.

The FMECA can vary not only just depending on ones system requirements, but also where in the design process one is. As such, there are often three main types of FMECA which can be utilized. The first one is the one used for this work and is called the **Design FMECA**. It is carried out to eliminate failures during equipment design while taking into account different types of failures during the lifespan of the equipment.

The second type is the **Process FMECA** which focuses on problems originating from the equipment manufacturing, maintenance or operation. Third and last one is the **System FMECA** which is used to look for problems and bottlenecks in larger processes, such as entire production lines. From the type of task in this Thesis, the Design FMECA has been chosen.

Also depending on where you are in the design process, there are several ways to create the FMECA. One is a **Functional approach**, which focuses mostly on sub-systems in terms of their functions within the system you are working on, and is often applied when hardware components can not be uniquely identified. Required sub-functions can however be identified and might be set up in a top-down fashion to get a picture of potential problems and is therefore often called a "top-down FMECA". The second way of doing an FMECA is when you got a full system breakdown of all the lowest level components, and can do a detailed FMECA, also called the **Hardware approach**. Here you can identify all the failure modes on the lowest level, and proceed upwards in the hierarchy. This is therefore also sometimes referred to as a "bottom-up FMECA".

3.6.1 Rationale for choosing to use the FMECA

The BLEDP-card is a technically advanced and complex electronics card due to it's many built in functions. As a consequence to the high number of intricate functions there are also a large number of components which have a small but inherit risk of failure. In addition, because of the BLEDP-cards roles as acquisition modules, a high emphasis was put on their capability to correctly measure, process and publish the beam loss measurements, and through this assist in the continuous protection of the system from potentially damaging beam losses. This means that, as far as reasonably possible, a failure in the BLEDP-card should not cause a problem which meant the loss of protection of the system while the machine is operating. As a result, it was important to get a thorough understanding of the consequences of failures. To do this, it was decided to also include an FMECA in the reliability analyses, which would build upon the work done in the Prediction analysis, and further explore the cause and effects of the different failures.

Therefore, in addition to figuring out what kind of failure rate the components, blocks and systems have, it's thought to be very beneficial, especially in safety critical systems, to map out the different ways the components can fail in order to better understand the failure propagation or consequences which might put the mission and its equipment at risk. Consequently, a decision was made to complement the failure analyses with a full bottom-up FMECA to better understand and prevent failures that may occur, especially damaging ones.

3.6.2 Tailoring the FMECA

For most FMECA's, it's very important to tailor the analysis to the task. For this project, in order to produce an analysis which could deliver the wanted answers, it was important to first acquire as much relevant information as possible, especially regarding the systems functionality and technical specifications. This meant reading the different scientific papers, textbooks and studying schematics, as mentioned earlier. With this it's much easier to get a picture of what is needed, and it can also give clues how to progress through the analysis from a strategy point of view.

Perhaps most valuable outside of the schematics, is a good and detailed block diagram which can be used to build up the different end effects and also connect them to the initial effects as shown in the FMECA report structure I have constructed. In addition to having the resources pre-defined and available, it was important to create proper limitations for the analysis. This means that it's important to understand what is relevant for the analysis itself and to establish what should be included for documentation purposes regarding both data resolution and readability, in the report. With all of this, it was possible to mould the FMECA to my needs.

The FMECA was decided to be based on a military standard for these types of analyses - the MIL-STD-1629A, which was also included in the functionality of Isograph, in the FMECA-module. This allowed the use of a good and time efficient functionality in Isograph, to produce the FMECA based on an already created Prediction analysis (by transporting the components and failure rates to the FMECA project tree). I also decided to follow the ID scheme used in the Prediction analysis in order to allow for data links which would update the values in the FMECA automatically as failure rates might be changed in the Prediction module.

In addition it was decided that failure modes should be identified using a military standard, MIL-HDBK-338B which included a table of failure modes derived from a military issued Failure Mode Distribution analysis, FMD-91. This is a list of the most common failure modes in electronic components.

DEVICE TYPE	FAILURE MODE	MODE PROBABILITY (α)
Capacitor, Ceramic	Short	.49
	Change in Value	.29
	Open	.22
Capacitor, Mica/Glass	Short	.72
	Change in Value	.15
	Open	.13
Capacitor, Paper	Short	.63
	Open	.37
Capacitor, Plastic	Open	.42
	Short	.40
	Change in Value	.18
Capacitor, Tantalum	Short	.57
	Open	.32
	Change in Value	.11

Figure 47: FMD-91 failure mode distribution example

For special items not included on the list, apportionments was obtained by using supplier given information, estimates from similar types of components, or simply using a linear failure mode probability distribution if nothing else could be derived. As a part of a future planned Fault Tree Analysis (FTA), it was also decided to include failure rate apportionments using the failure mode probability as a function of the total component failure rate, in order to obtain a quantitative analysis for the FTA. Finally, in order to go from an FMEA to an FMECA, I had to add the criticality assessment to the analysis. This was done by adding a Risk Priority Number system, as described earlier. The levels for the three components of the RPN-system were selected so it fit the severity cases for the system, as well as detection and consequences of failure rates.

3.6.3 Project parameters for the FMECA

Regarding the implementation and construction of the FMECA in Isograph RWB 11, there was a number of options to be chosen in order to get the properties needed. The software provided all the necessary tools required to perform the analyses, and was especially convenient for this analyses as it was of a certain complexity and size. The elaborate report facility for creating documentation was also useful and time saving. The FMECA-module provided the opportunity to follow the methodology of several recognized standards, but as these analyses often need to be customised to the task, it also gave a lot of room to customize the analyses, and especially the report, to meet the requirements for the project.

As the FMECA is the Failure Mode, Effects and Criticality Analysis it is naturally to start the analysis with these three areas. But before the work can be started, the module requires certain options to be chosen. The ID structure, project tree and project description all follows the same format as in the Prediction module, and therefore need not be adjusted. The TOP-events are the main end effects used for the Fault Tree Analysis, and contains the severity cases as well as an description to what causes the severity case. This is therefore the top-level of the tree structure, as it will be the best fit when used to create the FTA. System lifetime is still 10 hours, the same time as one run, as the system will be able to check itself to "as good as new" status before each run. Failure rate is set to hours as it needs to match the time frame used in the Prediction for it to be correct in the implementation of both the FMECA and Prediction module, to the FTA.

Figure 48: Project options

There are several options for what structure you want the FMECA to follow, but as my planning was based on using the MIL-STD-1629, I chose this one. The MIL-STD-1629 version of the FMECA uses failure apportionments and failure rates instead of the RPN-system and was chosen as this fits best with the future desire to construct a quantitative and qualitative FTA. However, I decided the RPN-system in this project was better suited for the severity assessments given the severity, detection and failure rate requirements of the BLM, instead of just one Criticality ranking. As a result the FMECA used in this reliability analysis is modified. To enable this duality, the option "Display rankings as preference" was used. The summation of apportionments to 100% is useful as it allows to run a Model Integrity analysis inside the module which looks if there is some error in terms of summation, missing failure modes and the like. This allows for a quick and systematic verification that all the needed information in each failure mode, is provided. The rest of the options are used to customise either the results, the tree structure, how the relationships between the blocks are, or if you want to use a special ID-system. As none of these were necessary for the task, they were all left to default and not used in the work nor report.

3.6.4 FMECA module

The interface is constructed similar to the Prediction. The tree structure shows the different blocks, portraying the levels of the system. The bottom layer is chosen to be the sub-blocks instead of the individual components, but with every sub-block holding the failure mode of the components related to said sub-block. This allowed for a more natural comparison to the schematics and reduced the number of pages in the FMECA-report considerably.

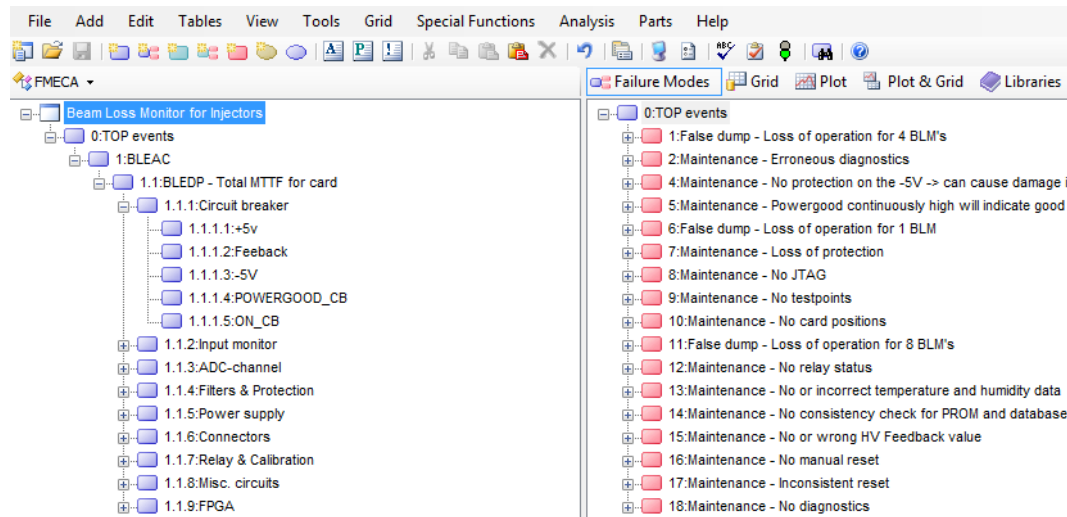


Figure 49: Interface of the FMECA-module.

Each of the sub-blocks failure modes are given the Occurrence and Detection ranking, while the Severity ranking is set at the TOP-events level. Each failure mode has a box in which I put the Recommended Actions. This was a short description of if it's detectable, and if any modification or mediating action is warranted by the designer to improve the reliability. All the RPN-values can be calculated automatically by the use of the Analysis-button and this also allows me to see the total summarised RPN-value for each block, and also the overall RPN-value. This will be put into a log automatically which makes it easier to see how changes affects the overall value.

3.6.5 FMECA report structure

The report structure is similar to the one used in the Prediction, and so I will not describe it in any special detail. The different parts of the report is described in this section about the FMECA and how I constructed it.



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 004
FMEA Date (Orig.): 15.05.2013
Date: 30.08.2013
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.1.1.1	Sub-block - +5v	2,722e-8	0.050 Shunt - Open	Random failure	No voltage can pass out of the circuit breaker	False dump - Loss of operation for 4 BLM's	3	1	1	3	Maintenance fix. Detectable, no special action is warranted.
1.1.1.1.2			0.050 Shunt - Short	Random failure	No current measurements -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.1.3			0.050 Shunt - Parameter Change	Random failure	Shunt tolerance is 1%, but if the parametric drift is > 10%, load measurement is out of the error threshold	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.1.4			Defective MAX4272	Random failure	No current measurements -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.

Figure 50: Report structure of the FMECA.

3.7 Fault Tree Analysis

The Fault Tree Analysis, FTA, is one of the most commonly used techniques for risk and reliability studies. It's a very useful and powerful top-down deductive approach to failure analysis, where you start with a main undesirable event called a TOP-event and then go through the system in order to map all the causes to the TOP-event [?]. All the causes, or initial effects, are then connected together using boolean logic gates. The causes can be many different conditions, such as environmental, human error or just expected failures due to the nature of your system.

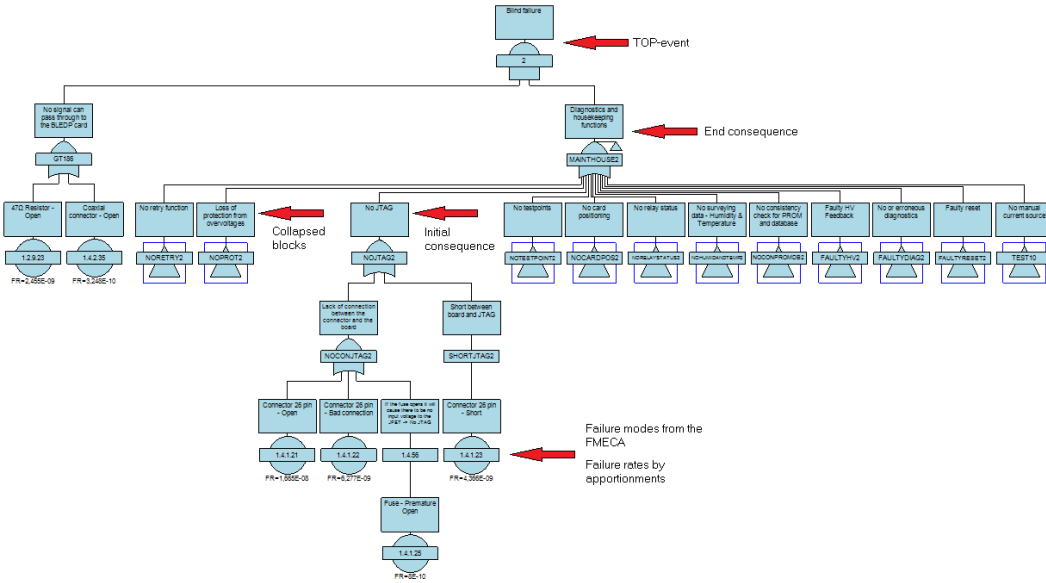


Figure 51: Example of the FTA structure.

The analysis typically focuses on either one or two aspects. The first one, the qualitative analysis, is the one already mentioned, with the creation of the logical structure which shows the movement from the causes to the effects. The second one is a quantitative analysis which builds upon the structure by adding different types of data, depending on what you want to find out, and then see how each step can affect the rest of the blocks. For example, if one has available the failure rate of the system and the apportionments of the failure modes, one can target a certain type of failure and calculate the probability of a specific end effect. In addition, it's common to try and reduce the complexity of the analysis by applying what is known as the minimum cut sets. This means that sometimes it's possible to decrease the number of steps by using bigger or different blocks, without losing any critical data. This analysis can often be used as an alternative, or as a complimentary analysis to a FMECA. The main difference is that the FMECA starts at the bottom and moves upward, while the FTA starts with the end effects and goes down towards the effects.

The FTA tends to be accurate on the top, and become more prone to errors as one move down, while the FMECA is fairly accurate on the lowest tiers, while becoming less accurate at the top. Another difference is that FMECA's only focus on one failure at a time, while the FTA allows for multiple failures to be analysed at the same time. In general, it's also more difficult to perform a full FTA compared to an FMECA [16].

3.7.1 Project options and structure for the FTA

Before I started the construction of the FTA, I had to decide on some project options. Life for the Prediction and FMECA modules, Isograph RWB 11 has a special module for the Fault Tree and Event Tree Analysis. The benefits of using Isograph are many, especially when you are using different types of reliability analyses on the same system. For instance, once I had completed the two previous analyses, I could use a special option for copying a lot of the relevant information, from the Prediction to the FMECA, and from the FMECA to the FTA. I will describe this in more detail a little later.

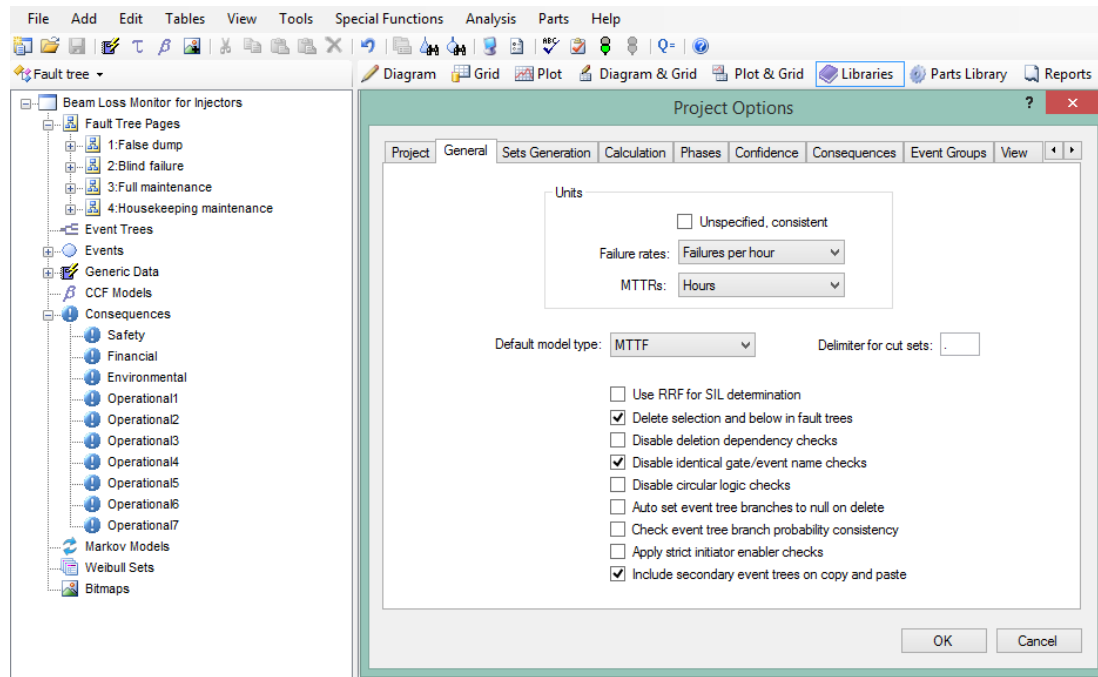


Figure 52: Fault Tree Analysis-module options.

From the FMECA I had already the end effects, here called the TOP-events. However, as the FTA can show many failures at once, it was beneficial to structure the tree structure a little different than before. Here, the tree structure is made up of the 4 main categories in which the FTA is divided. The first one is only failure modes and initial consequences which propagate to a False Dump. The second is for the Blind Failures. The third one is for everything that would lead to a maintenance, meaning all failure modes and all end effects. The last one is for non-critical maintenance cases which does not elicit an immediate response. Due to these fault trees being very large, it's not possible to get everything in on an A4 format. Neither does it make sense to split such a fault tree out on many papers. Therefore, the results are published with a focus on the highest tiers, as the quantitative aspect is one of the main areas of interest for this particular analysis.

Regarding the options, failure rates are set to per hour as for the previous analyses, and for the same reason. The MTTR is inconsequential as it is not calculated for this analysis. The quantitative output is desired to be the MTTF, and so this is the setting chosen for the FTA. The rest of the options are for the practical adjustments wanted, and is left at a setting beneficial to my specific task.

3.7.2 Constructing the FTA

My work was done using the fault tree module in Isograph. There are several ways to start a fault tree analysis, but one good way is to combine a FMECA, where you already have mapped all the failure modes of all the components in the system and therefore have a good understanding for how the failures happen, and a general block diagram of the system you are building to give a better picture of how all the events are connected.

When I started the FTA, I had already completed the Prediction and FMECA for the BLEDP-card, and both of these were conducted so that I could profit as much as possible from that work, in my FTA. Because of this, I did not have to complete the normal first step, which is to find out the problem and boundaries of the FTA. Normally, as this is a top-down analysis, one would then start with the TOP-event and work yourself down the failure propagation. However, the TOP-events were already available as I had already decided upon the severity cases and the end effects. Due to me planning this in advance, once I used the special function inside the FMECA-module which allows me to inherit a lot of information from my FMECA, to my FTA, I had all the failure modes with the modified failure rate from the apportionments ready in the FTA. This was however just a huge line of every single failure mode I had created in the FMECA. So my starting point was then the TOP-events, and all the failure rate adjusted failure modes, and from here I had to create the Fault Tree by connecting the failure modes to the TOP-events. This required me to add in the steps in between the failure modes and the TOP-events. Regarding the gates used, there are many options regarding the type, but for the purpose of my work, using AND and OR gates was already sufficient.

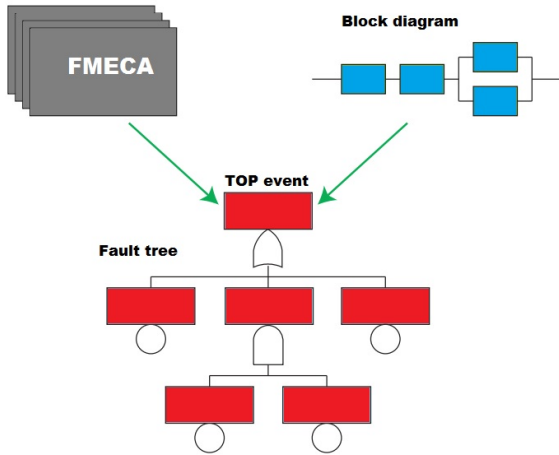


Figure 53: Construction of a FTA.

Once that was completed I could go over the FTA and try to create a minimal cut set. The minimal cut set can be obtained by several methods, and depending on the size and complexity of the FTA, one solution can be to use a Karnaugh map. However, as my FTA was essentially many hundreds of logical gates, and each represented a functional consequence, I instead opted for a more practical approach of trying to explain each step as fundamental as possible. The resulting minimal cut is therefore as reduced as can be while balancing readability and resolution. The end result is then the qualitative analysis which is read by investigating the minimal cut sets. After this was completed, I could also perform the quantitative analysis since the data input was already present. Depending on what you want as output, there are several options to what you can calculate. For my work, I was mostly interested in calculating the MTTF for each propagation up the fault tree, and then finally seeing what the failure rate was for each of the TOP-event. This calculation could be done inside the FTA-module.

4 Results and conclusion

Here follows a presentation and discussion of the results of the reliability analysis. The results will progress from the Prediction and the calculation of the MTTF, to the FMECA and finally the FTA. The data represented here is collected from the reports which are included in the appendix.

4.1 Results from the Prediction

The results of the Prediction is automatically calculated by the software. My goal with this section is to show both the overall calculated value, as well as describe how the results vary in between the different blocks. The intention is to show what factors affect the value, as the main result is the weighted average of all the lower tiers summarised upwards. Also note that the MTTF-value includes maintenance cases.

The BLEDP-card has a total calculated MTTF of: 89220 hours.
Converted to 8760 hour years, this means: 10.1 years.

The distribution between the circuit blocks are as follows:

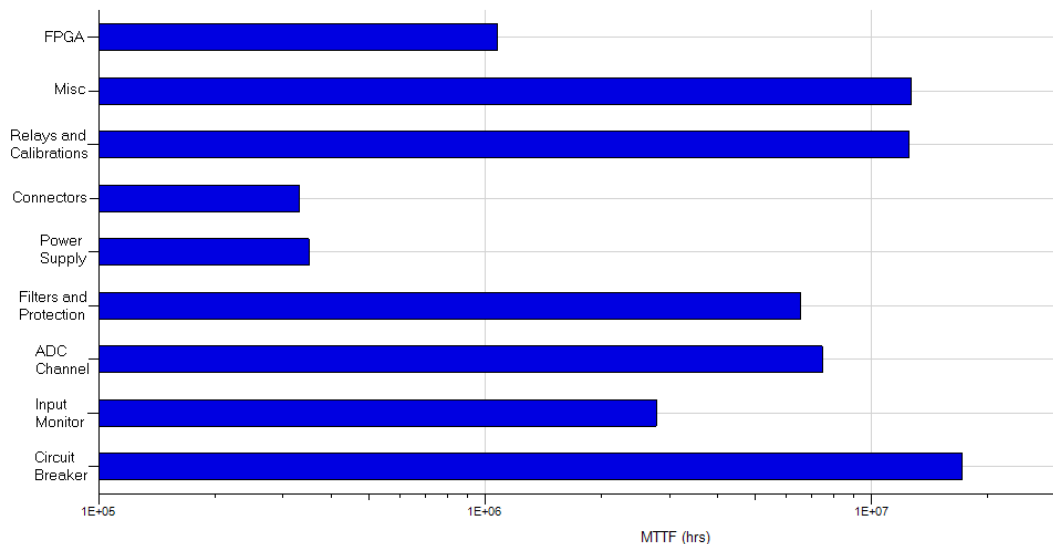


Figure 54: The various MTTF-values which makes up the BLEDP-card, on a logarithmic scale.

Comments: The MTTF-value is derived from the failure rate, which in turn is based on the assumption of a constant failure rate, or that the value is in the so called "useful life" period of it's lifetime. At the same time, many of the values selected are considered conservative, and there is a system wide good derating margin. 10.1 years is therefore considered absolute worst case.

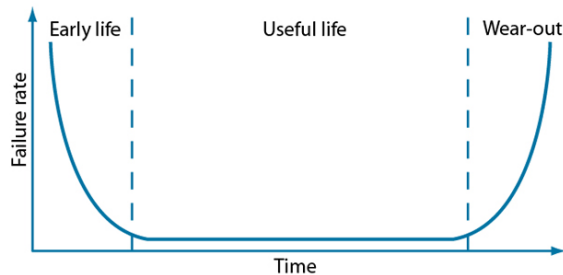


Figure 55: Bathtub curve.

4.2 Results from the FMECA

The FMECA is divided into the most relevant information for this work. The first and most important is the number of Blind Failures. Second is the prevalence of failures which causes the system to abort or deny a Beam Permit. Outside of this, I've provided some data on the number of failure modes for each end effects, and if there are any changes warranted.

Total number of different failure modes with severity class 2 or higher: 335.

Total number of different initial effects with severity class 2 or higher: 287.

Total number of different end effects with severity class 2 or higher: 18.

Blind failures: As of now, there are two potential blind failures. However, both are detectable within the start of the next run. The first blind failure is on the very start of the BLEDP, and is for the 47Ω resistor and capacitor right before the offset current input. This can be avoided entirely if a low current "pinging" system is implemented, as with the LHC system. However, the probability of there being a dual failure of exactly this component, and a beam loss at the same time, within the 10 hour run, is very very low. The second blind failure is a transferring error or complete stop of transfer, in the optical links between the crate, BLEAC, and the rack, BLEPC and VME-crate. This is however already being mitigated by adding a triple lane, voting system, where two out of three transfer lines will detect a single failure. As such it's A single failure tolerant system and most errors will therefore be detected and so **no redesign action is warranted.**

Frequent maintenance cases: Regarding failure rates, **there are no single components who's failure rate leaves it below the threshold of 20 years.** In combination with the systems focus on no derating, it's protected environment, the focus on proper grounding, choosing components from different batches to avoid common-mode failures etc, it's fair to say that failures which does come up, will be various random failures which are not triggered solely by an environmental or systematic error. Therefore, based on this data, **no redesign action is warranted.**

RPN-system: Given the results of the previous two paragraphs, the data provided by the RPN-system should bring no surprises. As there are no other blind failures, and those are partially detectable, the detection and occurrence has to be 1 and 1. The end result then is that the vast majority is with a 3 in severity level giving a total number of 3. There are a few cases where there is a maintenance case, like a protection diode dying, which can not be discovered outside of a proper maintenance schedule. Such maintenance schedules will be added.

Comments: The results of the FMECA is also shown earlier in the Thesis, for each of the circuit blocks. The analysis itself is in the appendix, and is 37 pages. The FMECA only allows for us to view the individual failures, and so the data is fragmented compared to the results of the FTA. However, based on the results of the FMECA, all failure modes outside of the blind failures, are functions that can fail, but there are no clear cause for said failures. As such, the failure causation is considered random, and the focus then is on the probability of such a random failure, which is statistically improbable.

4.3 Results from the FTA

The fault tree shows another side of the calculation. The blocks shown here are only the biggest ones, as the full fault tree is many hundred such blocks wide. The false dump alone is almost 300 blocks. Therefore the full scale is impossible to fit to paper, but the lower tier follows the same structure as the FMECA. The most bottom tier is the components, and the second most bottom tier is the initial effects. These are not shown in the summary on this page.

Blind failure and maintenance

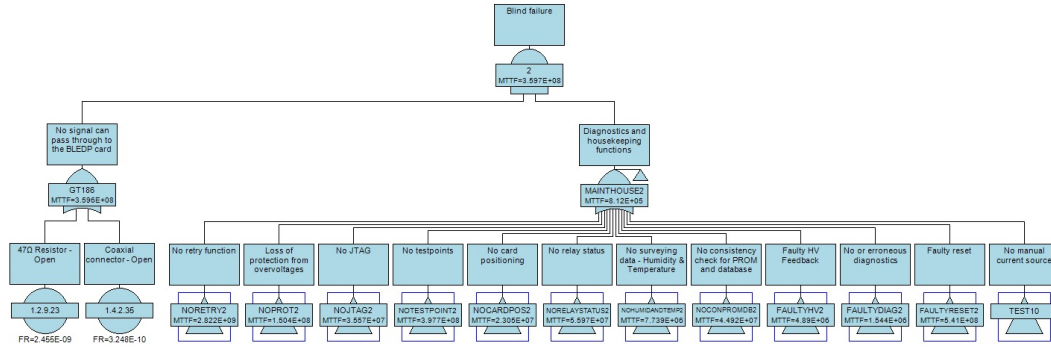


Figure 56: FTA of the blind failure and maintenance.

The blind failure has a very low probability of occurrence. It's single failure tolerant as it is in an AND with the diagnostics. Granted, not all the blocks connected to the diagnostics OR will cause the double failure with the blind failure to be a problem, but as the difference in the MTTF-value for this specific case is so strong, the probability value of the OR-gate is negligible. This is therefore more a demonstration of the blind failure in an AND with the diagnostics, and their MTTF-value of almost 360 million hours.

False dump

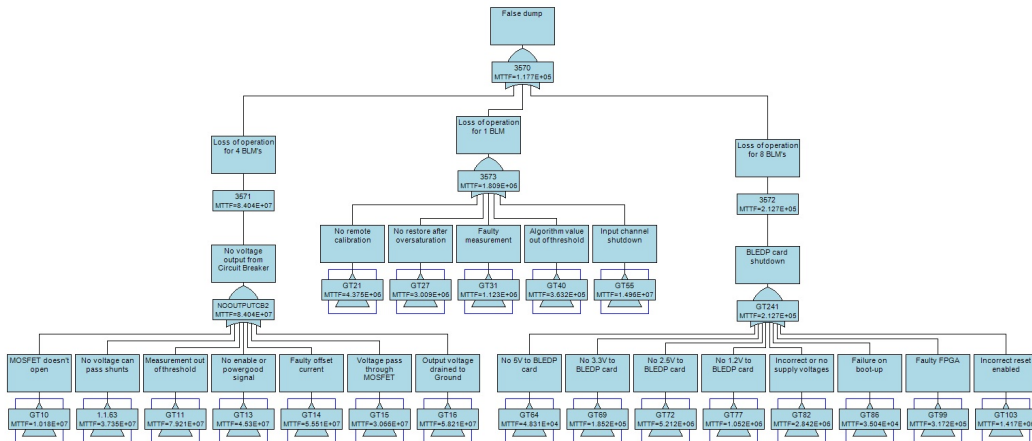


Figure 57: FTA of the false dump.

The results of the false dump shows that the BLEDP-card has a probability of interruption due to a false dump, of about 117000 hours, or 13.5 years. An improvement of almost 3 years from the Prediction alone, which made it hard to differentiate between the different failures.

4.4 Conclusion

The reason for this work as to estimate and validate the reliability of this electronics card. After looking at the design and premises systematically, and after performing the analyses empirically, within the framework of a conservative, military framework, the results show that the card has very low individual failures rates and that the system wide MTTF is 10.1 years. The probability of a stop in operation is about one in every 13.1 year, per BLEDP-card. This value is mainly the consequence of having many, but necessary, components. The failure modes shows that there are virtually no blind failures, and that weak spots have or will be mitigated. Overall, this card is, from a design point of view, very reliable given it's requirements of functionalities, and it's circumstances.

From a personal point of view, this work has been extremely insightful and made me learn a lot. Reliability is a challenging, tedious and not always intuitive field, but as I've progress through the work and studied many electrical schematics and data sheets, I've seen what a profound effect it can have on the reliability of a system. In my opinion, the knowledge from this work is something that I can profit from in the rest of my professional career in electronics. Also, in my opinion, I think reliability and perhaps Quality Assurance in general is not something that is adequately present in the education of electrical and electronics engineering. I think that even some introductory key points in reliability theory, or just some of the main analyses, is something that can have a very positive effect on someone's understanding of electronics design and therefore increase the value of a student to an employer or organisation.

5 References

Picture by William Vigano. *Various sources*.

About CERN. <http://home.web.cern.ch/about>.

Isograph. <http://www.isograph-software.com/2011/software/reliability-workbench/>.

About the Technical Student Programme. <http://jobs.web.cern.ch/join-us/technical-student-programme>.

The accelerator complex. <http://home.web.cern.ch/about/accelerators>.

W. Friesenbichler E. Gschwendtner B. Dehning, G. Ferioli and J. Koopman. *LHC Beam Loss Monitor System Design*. 2002.

. B. Dehning S. Jackson M. Kwiatkowski W. Vigano C. Zamantzas, M. Alsdorf. *System Architecture for measuring and monitoring Beam Losses in the Injector Complex at CERN*. 2012.

C. Fabjan E. B. Holzer D. Kramer M. Stockner, B. Dehning. *Classification of the BLM ionization chamber*. 2007.

O. Berrig E. Carlier L. Ducimetière B. Goddard A. Koschik J. Uythoven T. Kramer, G. Arduini. *Studies of beam losses from failures of SPS beam dump kickers*. 2007.

B. Dehning M. Kwiatkowski G.G. Venturini C. Zamantzas W. Vigano, M. Alsdorf. *10 Orders of Magnitude Current Measurement Digitisers for the CERN Beam Loss Systems*. 2014.

M. Alsdorf B. Dehning W. Vigano M. Kwiatkowski, C. Zamantzas. *A Real-Time FPGA based Algorithm for the combination of Beam Loss Acquisition Methods used for Measurement Dynamic Range expansion*. 2012.

C. Zamantzas M. Alsdorf B. Dehning E. Angelogiannopoulos W. Vigano M. Kwiatkowski, S. Jackson. *Development of a Beam Loss Measurement System with Gigabit Ethernet Readout at CERN*. 2012.

E. Effinger G. Ferioli C. Zamantzas CERN Geneva Switzerland H. Ikeda KEK Ibaraki Japan; E. Verhagen IceCube UW-Madison USA J. Emery, B. Dehning. *LHC BLM single channel connectivity test using the standard installation*. 2012.

CERN C. Zamantzas. *Designing electronics for use in radiation environments*. 2011.

Alessandro Birolini. *Reliability Engineering: Theory and Practice*. Springer, 2010.

MIL-HDBK-338B: Electronic Reliability Design Handbook.

A.Hoyland M.Rausand. *System Reliability Theory: Models, Statistical Methods, and Applications*. 2003.

6 Appendix

Here follows a litteratur list, the BLEDP circuits, the full Prediction analysis, and the full FMECA analysis.

6.1 Literature list

Although the knowledge for the construction of the reliability methodology came from many different places, I would like to point out the main resources I've used to help explain the choices I've made for the work itself. This is meant to complement the reference list.

System Reliability Theory - by M. Rausand and A. Hoyland

This textbook was my main resource related to learning the field of reliability in general, and also an introduction to the analyses. Many of the theoretical considerations used in this Thesis is based on this book, and many of the practical approaches are also adapted from the chapters dedicated to the analyses I've used.

Reliability of Electronic Components - by T. Bajenescu and M. Bazu

I used this book for the reliability related to the electronics components themselves. While the textbook provided what I needed to learn how to perform the analyses, this one was very helpful for providing understanding of different kinds of failure modes. This also contained some general reliability theory, and so I also used it as a secondary "opinion" to see if there were differences between a standard analysis and one that was focused on electronics exclusively.

MIL-HDBK-338B - Department of Defence (USA)

This is a very extensive handbook on the topic of Electronic Reliability Design, and is in many ways a compilation of a lot of the other relevant military handbooks and standards. As such, this was very useful as a reference tool to get a concise picture of relevant elements in electronics reliability.

MIL-STD-1629A - Department of Defence (USA)

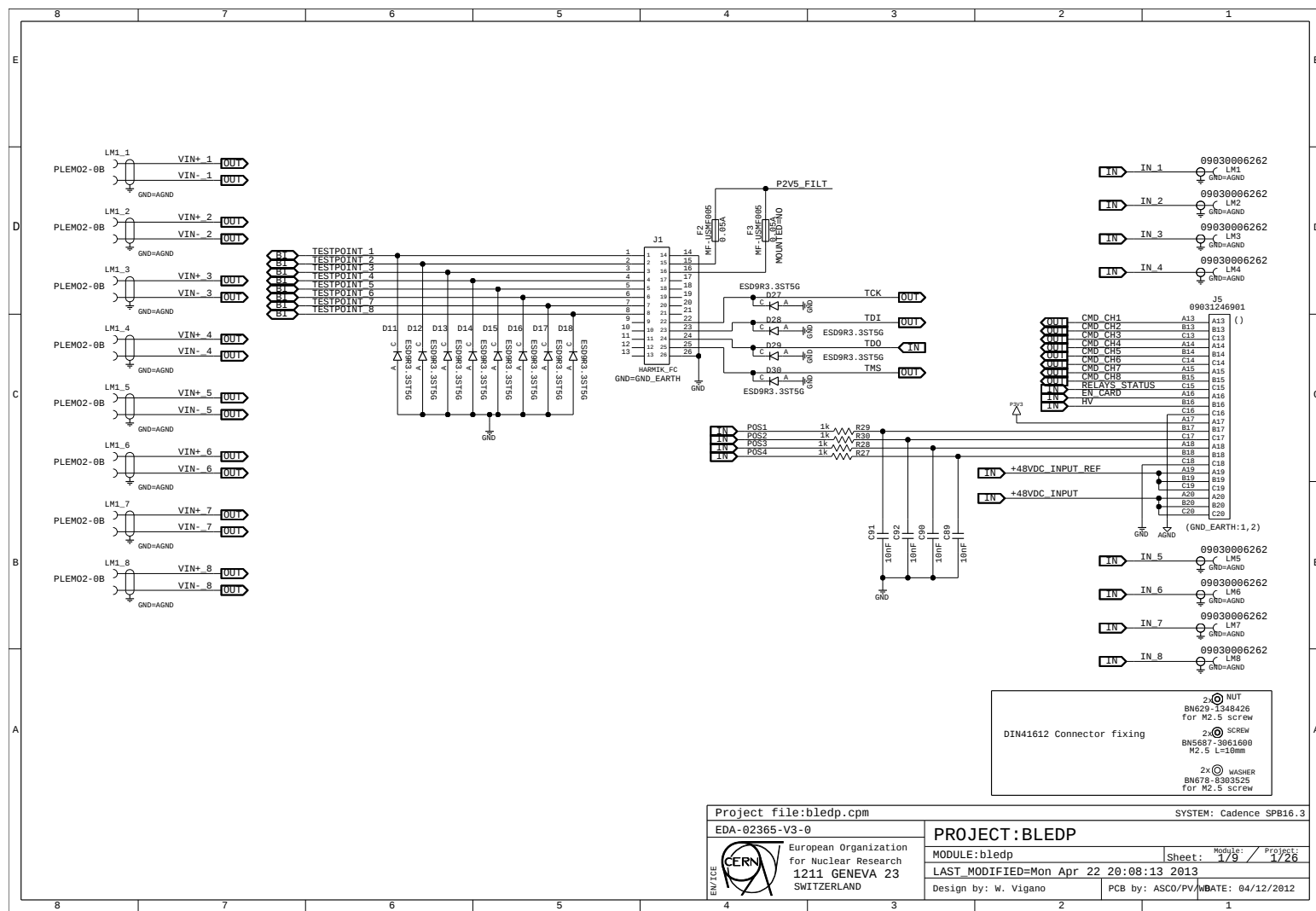
In addition to the textbook, I used the military standard 1629A for the process of doing the FMECA. Isograph RWB 11 had the option of using this standard as the frame work for the FMECA. It is very important that the FMECA is custom tailored for the system it is to be used on, and so was chosen by me for it's level of detail and fitting possibilities.

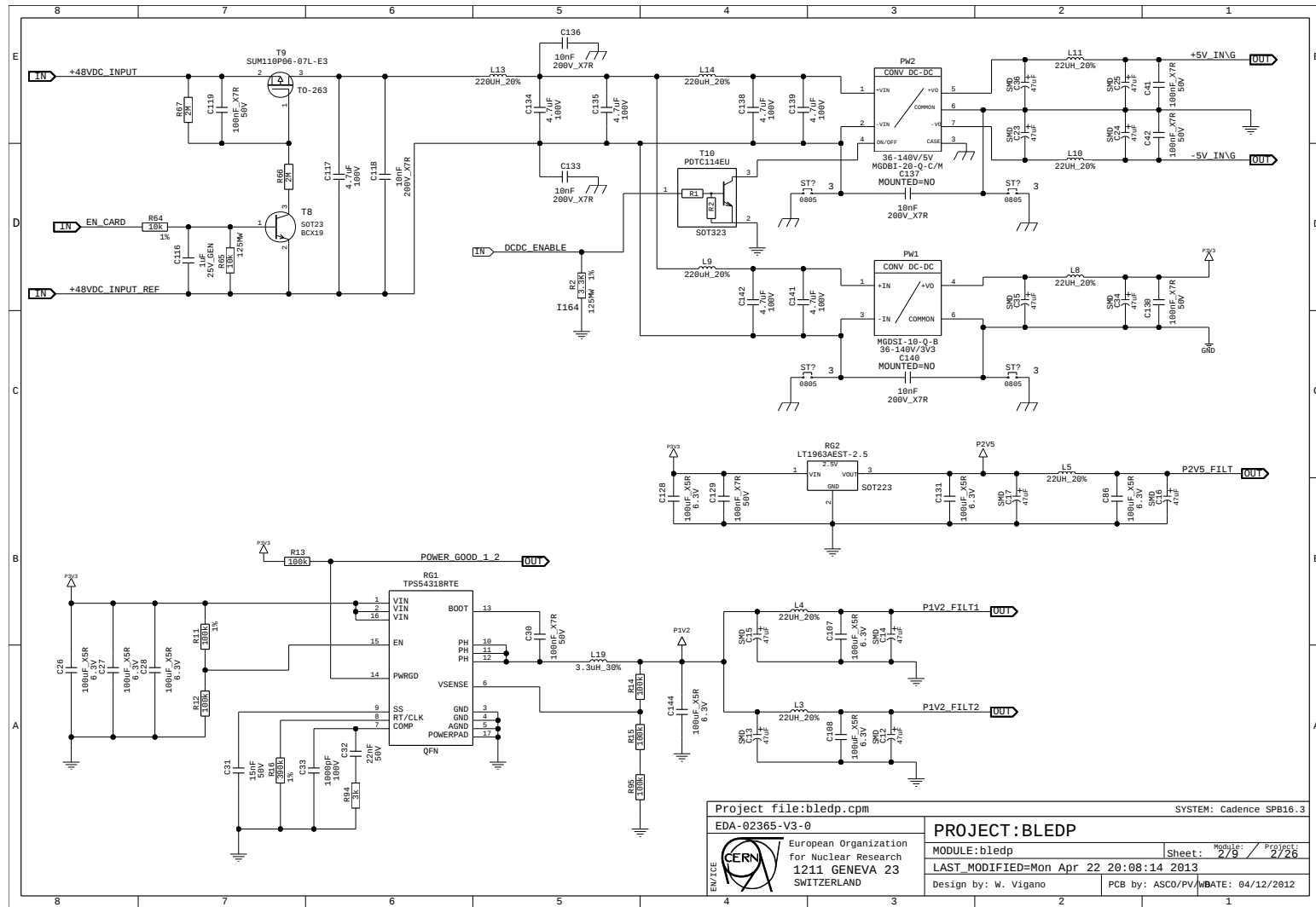
MIL-HDBK-217F Note 2 - Department of Defence (USA)

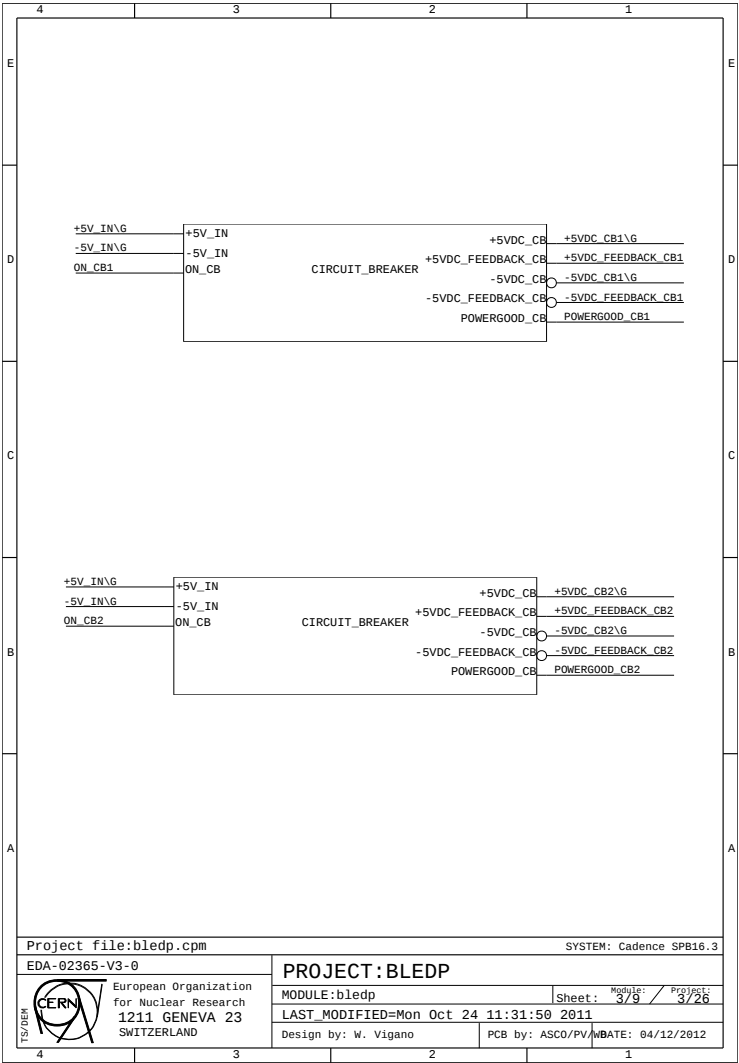
The handbook is widely popular for reliability prediction procedures for electronics. It contains many of the most used components, and also covers many of the different variations of the different components, such as different types of capacitors and alike. It was also integrated in Isograph RWB 11, and was used for the calculation of the MTTF. It was last updated in 1991, and is therefore considered to be conservative. For the MTTF calculation, a priority list was used, meaning that the handbook was mostly used for the passive components, as supplier given failure rates were used whenever possible.

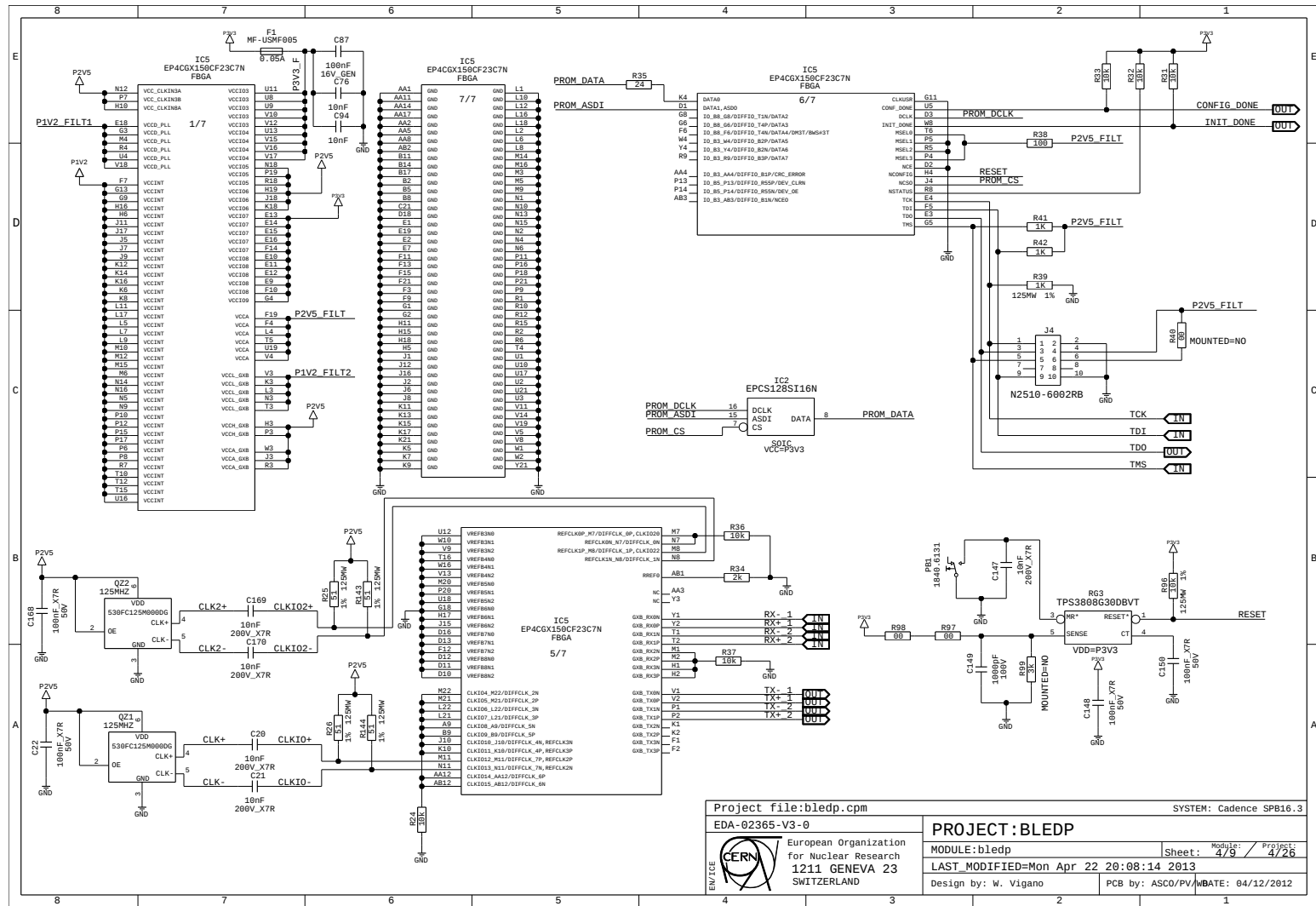
FMD-97 - Department of Defence (USA)

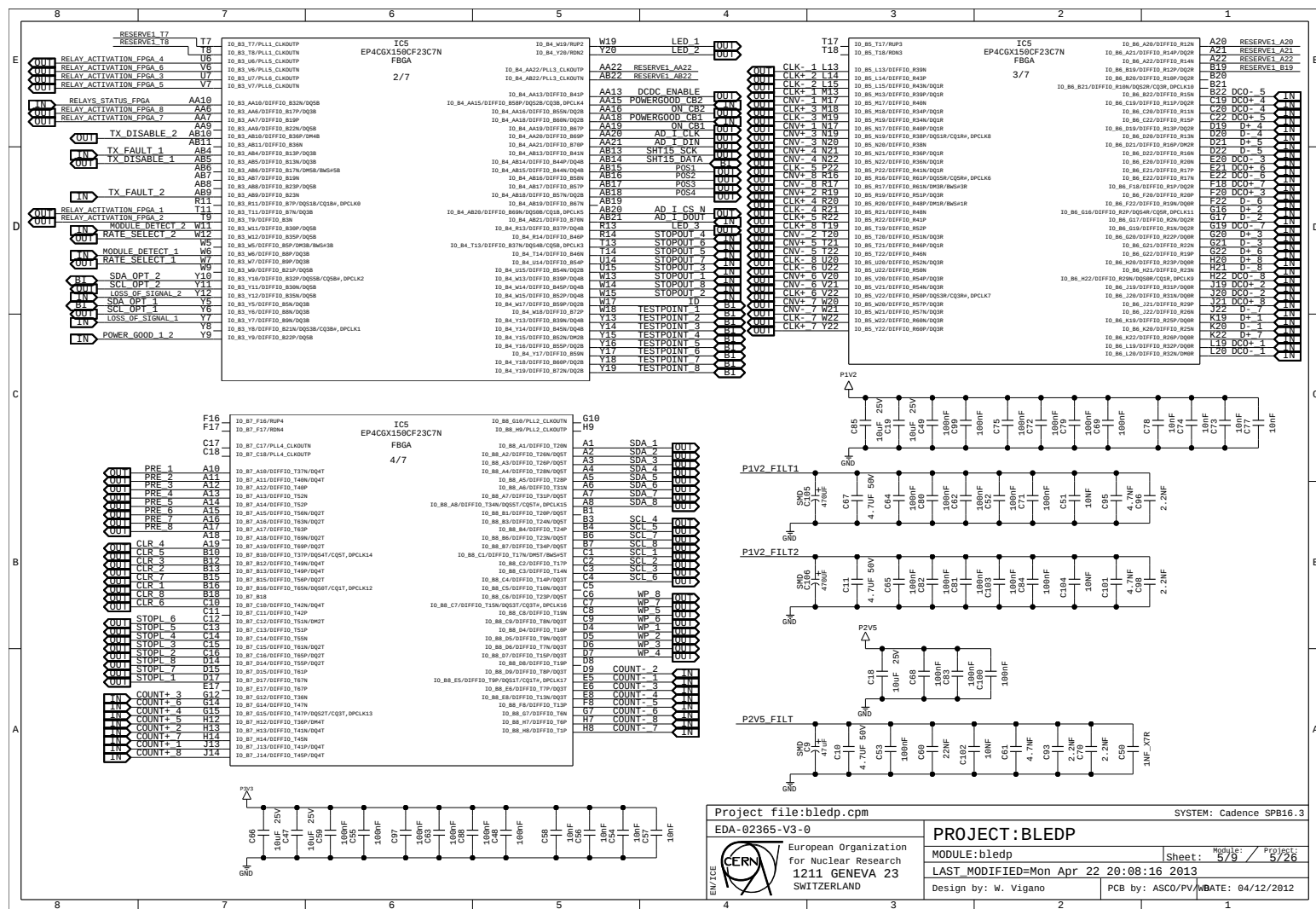
The Failure Mode / Mechanism Distribution 1997 standard is another book from the Department of Defence and is focused on the topic of failure modes and their distribution, both of which is a key part of the reliability thesis work. It contains many explanations on different types of failures for components, and also has a data collection of failure rate estimates, in this Thesis called the Apportionment, of the different failure modes.

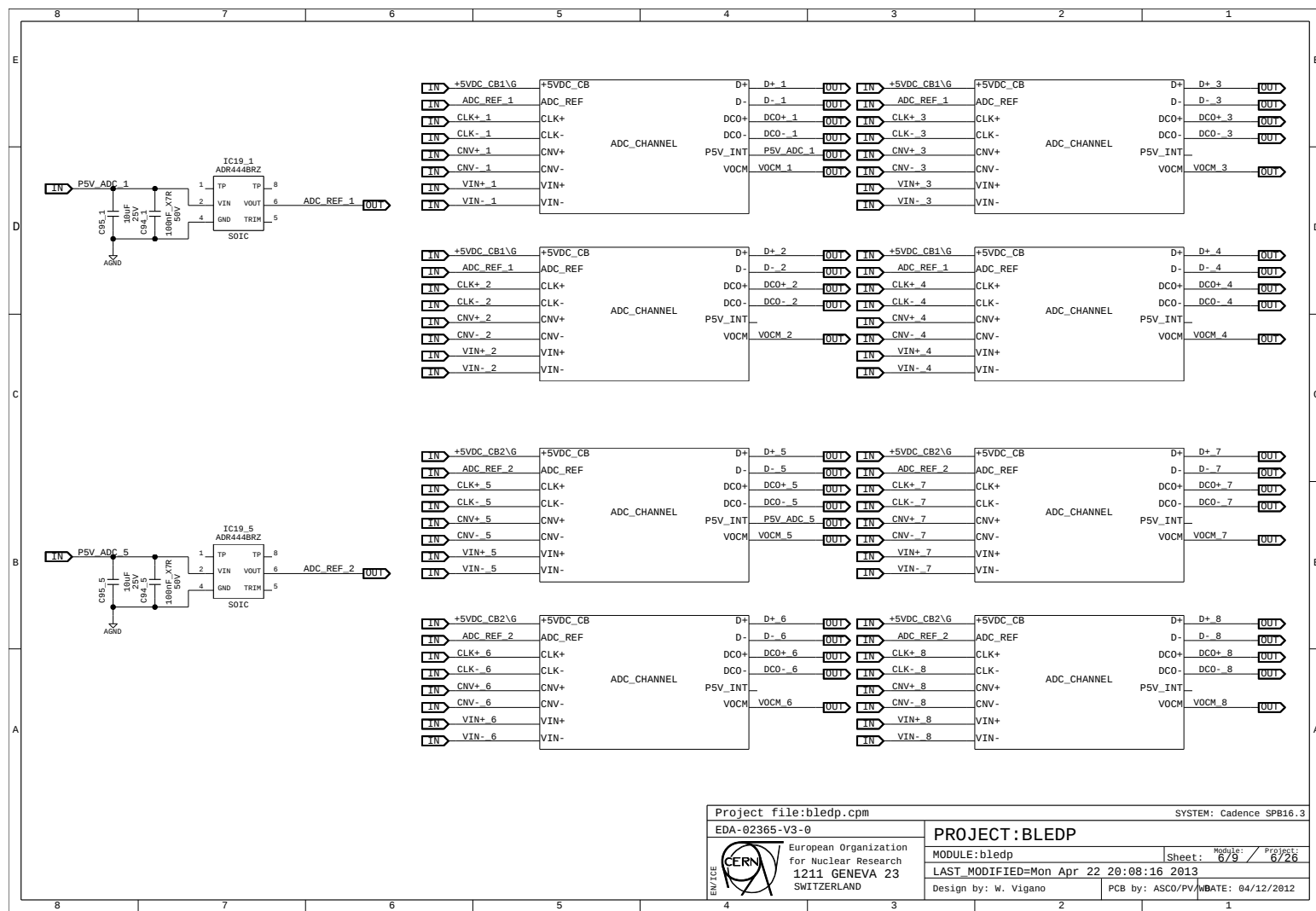


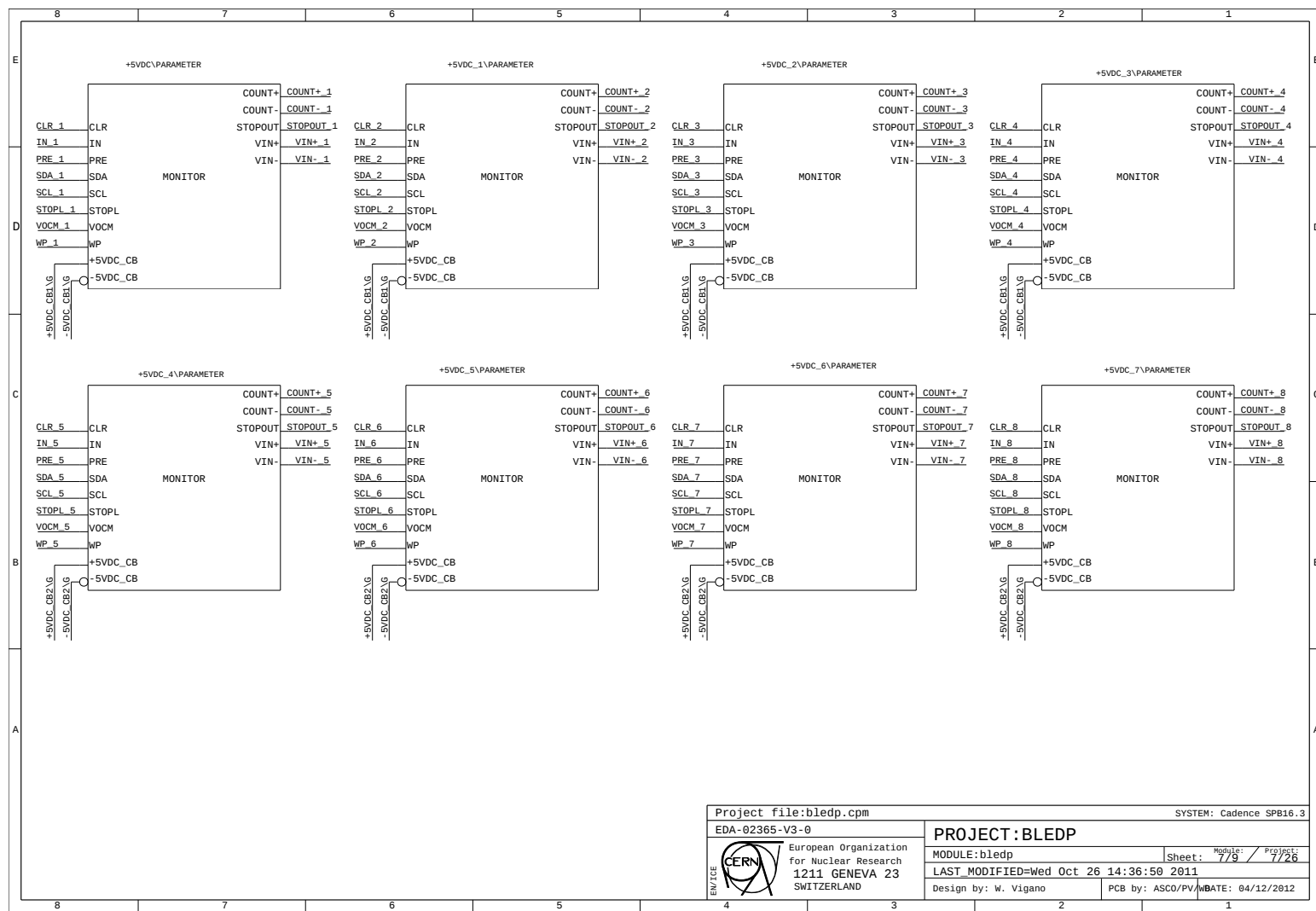


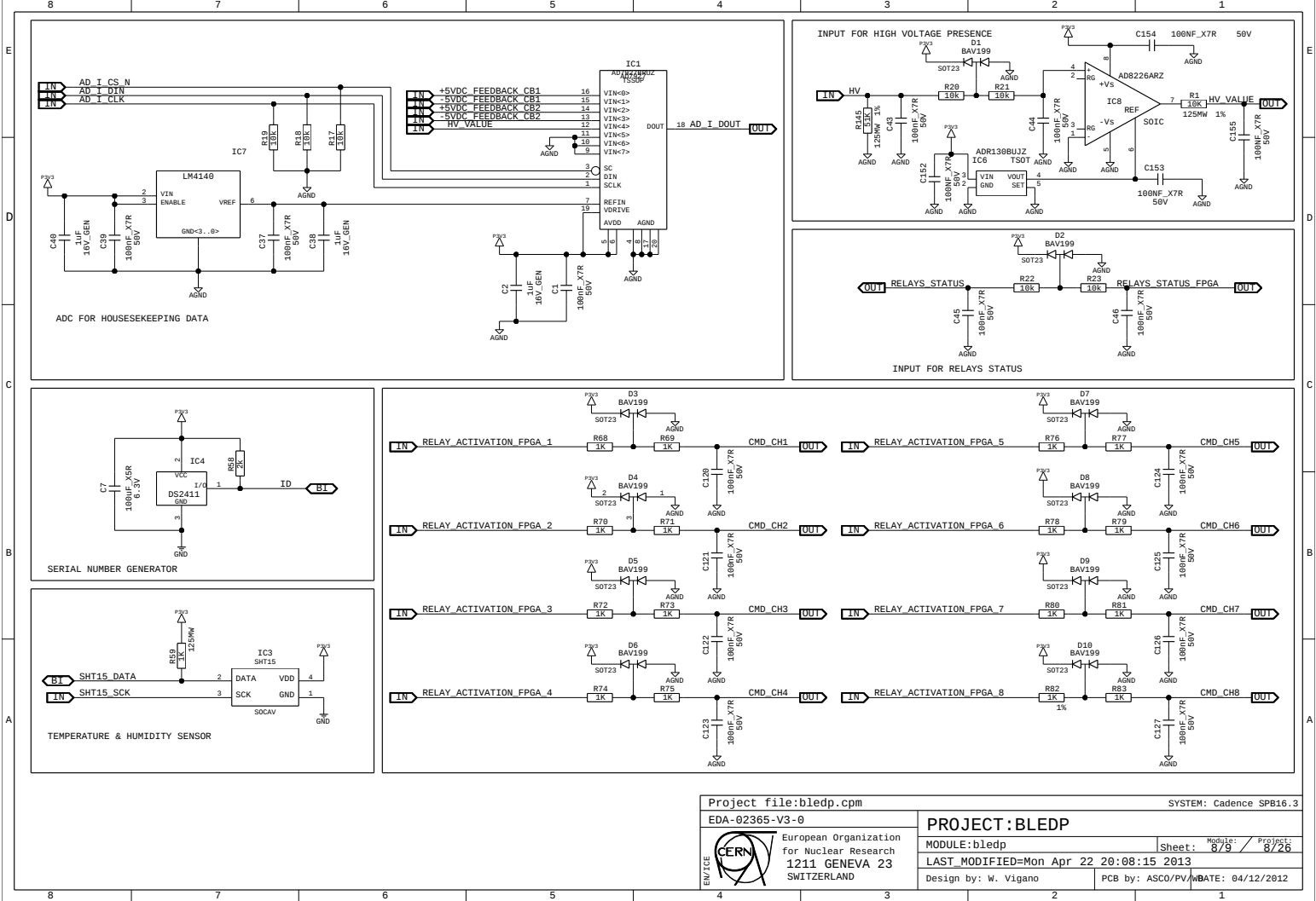


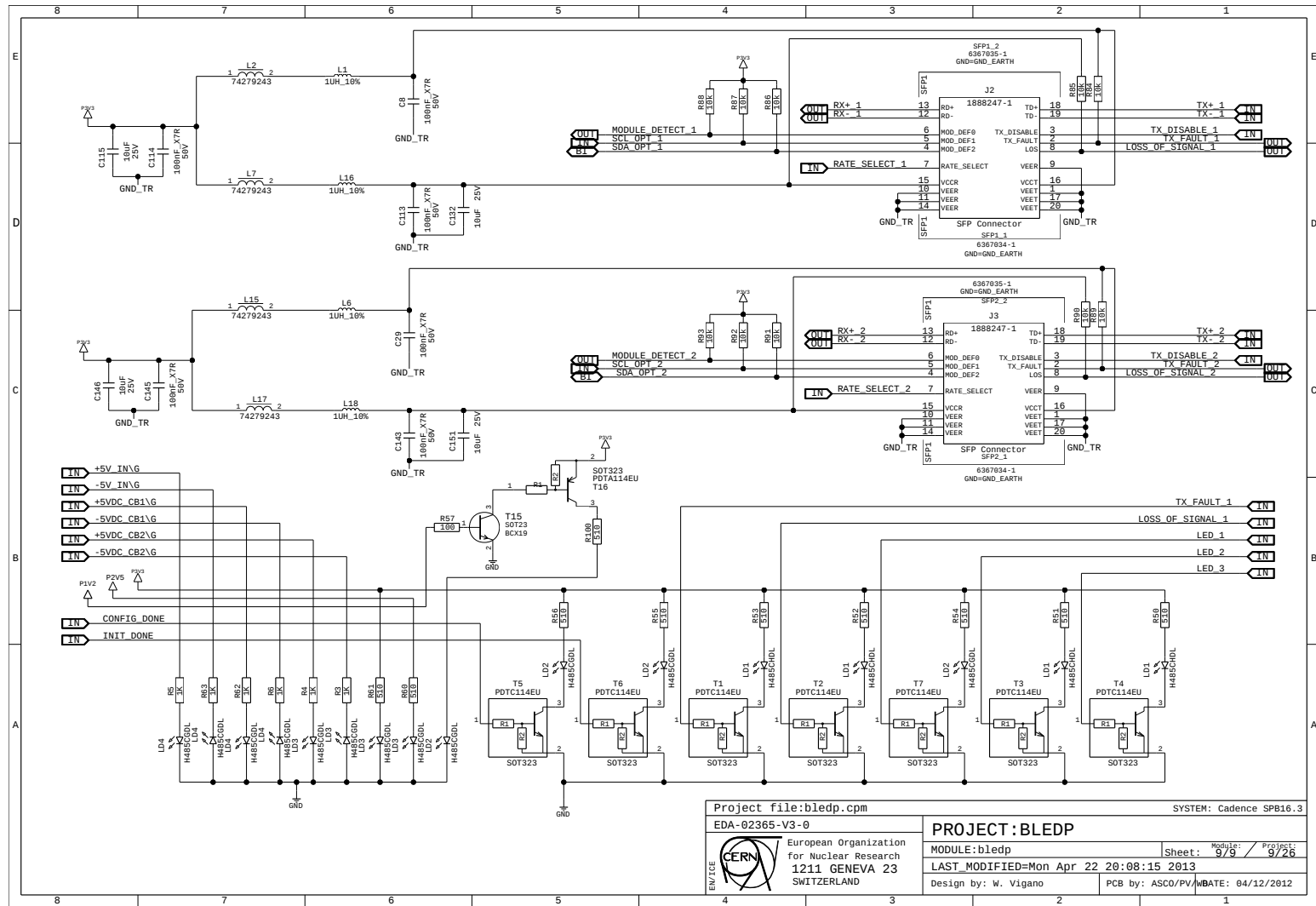


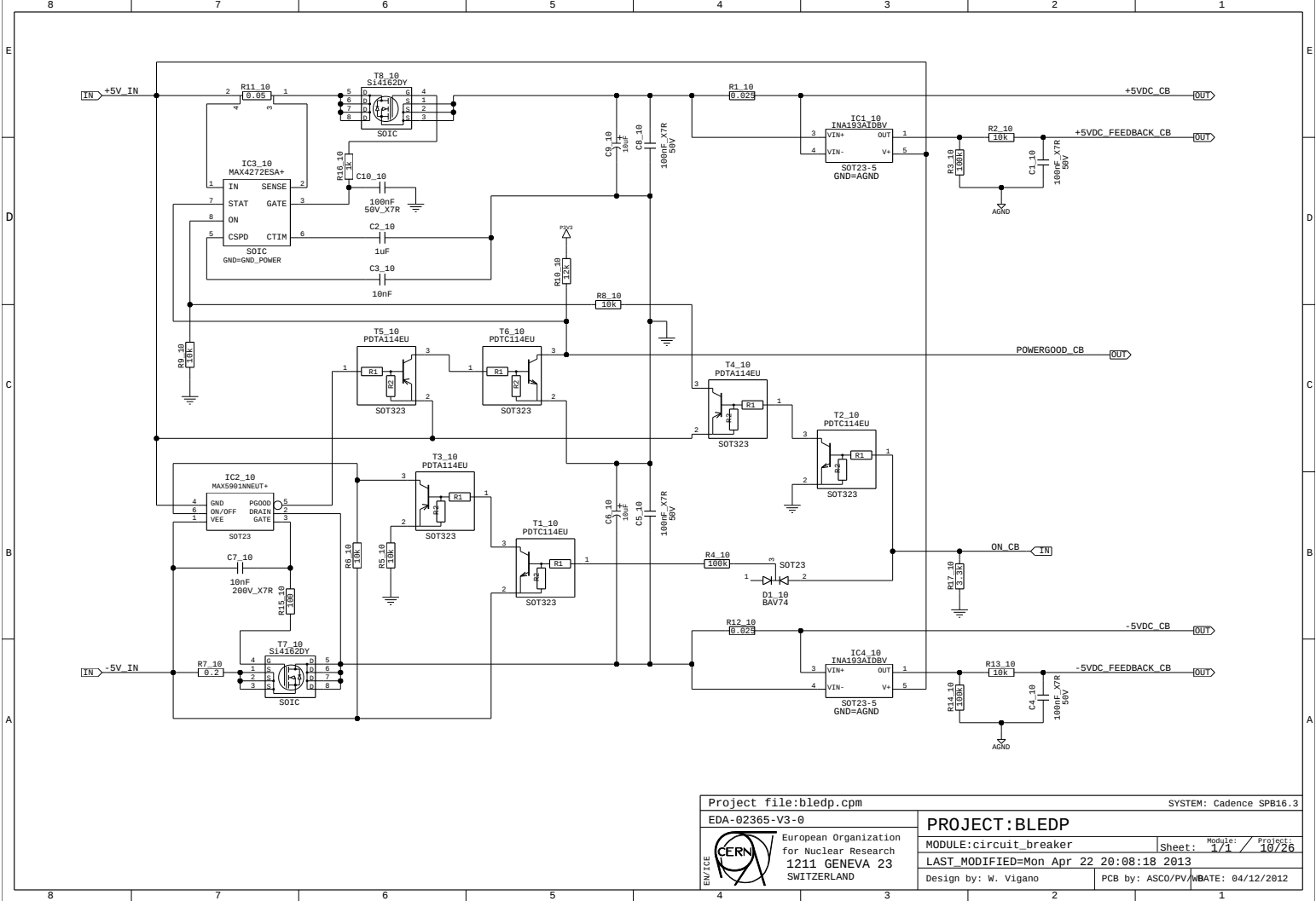




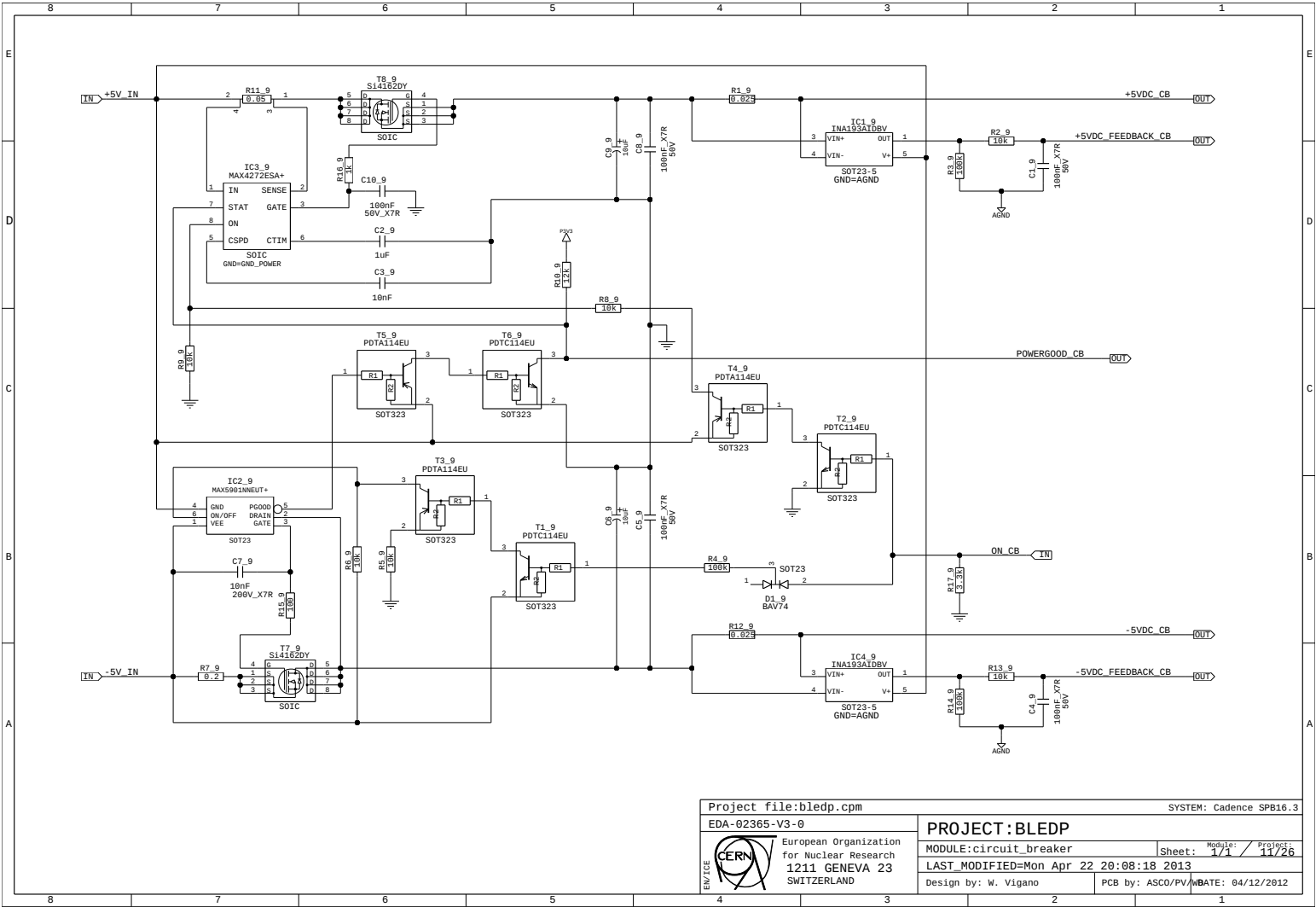








Project file:bledp.cpm		SYSTEM: Cadence SPB16.3	
EDA-02365-V3-0		PROJECT: BLEDP	
 EN/ICE	European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND		Sheet: 1/1 / 10/26
	LAST MODIFIED=Mon Apr 22 20:08:18 2013		Module: /
	Design by: W. Vigano		PCB by: ASCO/PV/MBATE: 04/12/2012



Project file:bledp.cpm

SYSTEM: Cadence SPB16.3

EDA-02365-V3-0

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

EN/ICE



PROJECT: BLEDP

MODULE: circuit_breaker

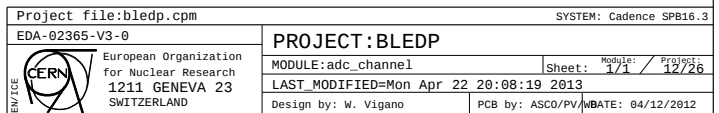
LAST_MODIFIED: Mon Apr 22 20:08:18 2013

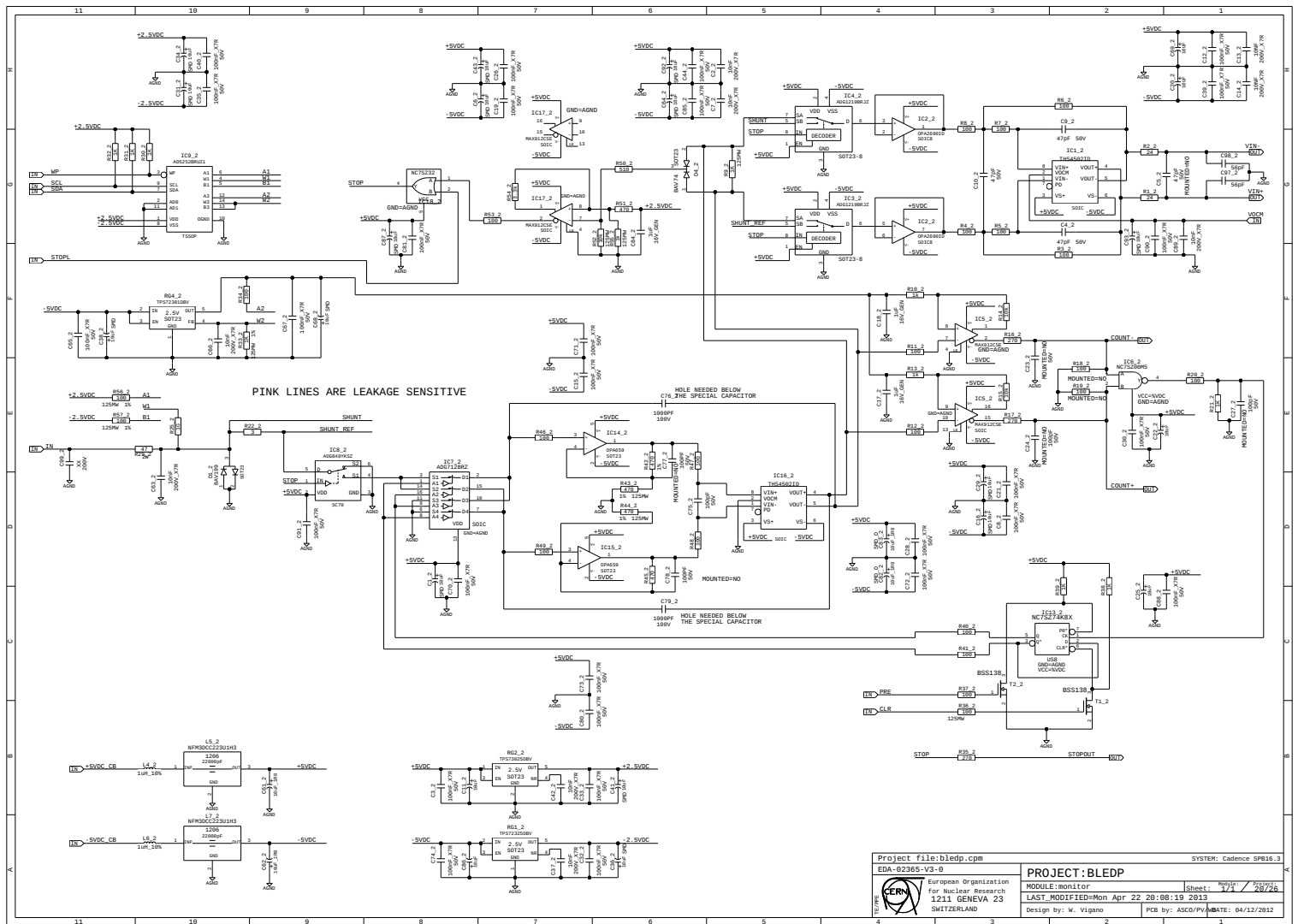
Design by: W. Vigano

Sheet: 1/1

Module: 11/26

PCB by: ASCO/PV/MBATE 04/12/2012







System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
			8,922e+4	System block	BLEAC	1	1	8,922e+4	N/A	40	N/A	N/A
System block		1	8,922e+4	Sub-system block	BLEDP	1.1	1	8,922e+4	EDA-02365-V3	40	N/A	N/A
Sub-system block	BLEDP card	1.1	8,922e+4	Schematic block	Connectors	1.1.6	1	3,301e+5	N/A	40	N/A	N/A
				Schematic block	Power supply	1.1.5	1	3,497e+5	N/A	40	N/A	N/A
				Schematic block	FPGA	1.1.9	1	1,076e+6	N/A	40	N/A	N/A
				Schematic block	Input monitor	1.1.2	8	2,771e+6	N/A	40	N/A	N/A
				Schematic block	Filters & Protection	1.1.4	1	6,544e+6	N/A	40	N/A	N/A
				Schematic block	ADC-channel	1.1.3	8	7,442e+6	N/A	40	N/A	N/A
				Schematic block	Relay & Calibration	1.1.7	1	1,25e+7	N/A	40	N/A	N/A
				Schematic block	Misc. circuits	1.1.8	1	1,267e+7	N/A	40	N/A	N/A
Schematic block	Circuit breaker	1.1.1	1,713e+7	Schematic block	Circuit breaker	1.1.1	2	1,713e+7	N/A	40	N/A	N/A
				Sub-block - +5v	+5v	1.1.1.1	1	3,674e+7	N/A	40	N/A	N/A
				Sub-block - -5v	-5V	1.1.1.3	1	1,279e+8	N/A	40	N/A	N/A
				Sub-block - Powergood	POWERGOOD_CB	1.1.1.4	1	1,288e+8	N/A	40	N/A	N/A
				Sub-block - Feedback	Feeback	1.1.1.2	2	1,627e+8	N/A	40	N/A	N/A
Sub-block - +5v	+5v	1.1.1.1	3,674e+7	Sub-block - ON_CB	ON_CB	1.1.1.5	1	3,057e+8	N/A	40	N/A	N/A
				CC0805 1uF 16V 10% X	Capacitor 1uF Ceramic CTIM	1.1.1.1.6	1	1,535e+8	C2	40	Ceramic, General, NE R	Base Failure Rate=9.9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1, Stress=1,141, Circuit Resistance=1
				CC0805 100nF 50V 10%	Capacitor 100nF Ceramic	1.1.1.1.9	1	2,146e+8	C8	40	Ceramic, General, NE R	Base Failure Rate=9.9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - +5v	+5v	1.1.1.1	3,674e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.1.1.4	1	2,146e+8	C10	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.1.1.7	1	2,652e+8	C3	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				LVK12R050FER	Shunt 0.05Ω	1.1.1.1.1	1	4,399e+8	R11	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,2354, Stress=0,7493
				T491B196K006AS	Capacitor 10uF Tantalum	1.1.1.1.8	1	4,796e+8	C9	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=117,2, Circuit Resistance=0,66
				MAX4272ESA	Hot-Swap Controllers	1.1.1.1.2	1	7,231e+8	IC3	40	Supplier given	Temperature=0,04614
				R0805 1K 1% 0.125W	Resistor 1k	1.1.1.1.3	1	1,106e+9	R16	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,09665, Stress=0,7258
				SI4162DY	N-Channel MOSFET	1.1.1.1.5	1	7,813e+11	T8	40	Supplier given	Temperature=0,001193
Sub-block - Feedback	Feedback	1.1.1.2	1,627e+8	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.1.2.5	1	2,146e+8	C1, C4	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				WSL1206R0250FEB	Shunt 0.025Ω	1.1.1.2.1	1	2,389e+9	R1, R12	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=1, Temperature=1,161, Power=0,1338, Stress=0,7282



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Feedback	Feedback	1.1.1.2	1,627e+8	R0805 100K 1% 0.125W	Resistor 100k	1.1.1.2.3	1	2,77e+9	R3, R14	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,03937, Stress=0,7116
				R0805 10K 1% 0.125W	Resistor 10k	1.1.1.2.4	1	6,812e+9	R13, R2	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,01604, Stress=0,7102
				INA193AIDBV	Current Shunt Monitor	1.1.1.2.2	1	1,782e+11	IC1, IC4	40	Supplier given	Temperature=0,001935
Sub-block - -5v	-5v	1.1.1.3	1,279e+8	CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.1.3.5	1	2,652e+8	C7	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				R0805 100R 1% 0.125W	Resistor 100 ohm	1.1.1.3.4	1	6,031e+8	R15	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,166, Stress=0,7753
				WSL1206R2000FEB	Shunt 0.2Ω	1.1.1.3.1	1	8,889e+8	R7	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=1, Temperature=1,161, Power=0,3011, Stress=0,8696
				R0805 10K 1% 0.125W	Resistor 10k	1.1.1.3.6	1	1,434e+9	R6	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,07534, Stress=0,7183
				MAX5901NNEUT	Hot-Swap Controller	1.1.1.3.2	1	6,195e+10	IC2	40	Supplier given	Temperature=0,00119
				SI4162DY	N-Channel MOSFET	1.1.1.3.3	1	7,857e+11	T8, T7	40	Supplier given	Temperature=0,001186
Sub-block - Powergood	POWERGOOD_CB	1.1.1.4	1,288e+8	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.1.4.5	1	2,146e+8	C5	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Powergood	POWERGOOD_CB	1.1.1.4	1,288e+8	T491B196K006AS	Capacitor 10uF Tantalum	1.1.1.4.4	1	4,796e+8	C6	40	Tant Elect,Dry,ER	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=117,2, Circuit Resistance=0,66
				R0805 12K 1% 0.125W	Resistor 12k	1.1.1.4.3	1	1,666e+9	R10	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,0651, Stress=0,7157
				PDTA114EU	PNP resistor-equipped transistor	1.1.1.4.1	1	1,181e+12	T5	40	Supplier given	Temperature=0,001192
				PDTC114EU	NPN resistor-equipped transistor	1.1.1.4.2	1	1,19e+12	T6	40	Supplier given	Temperature=0,001183
Sub-block - ON_CB	ON_CB	1.1.1.5	3,057e+8	R0805 3.3K 1% 0.125W	Resistor 3,3k	1.1.1.5.1	1	9,857e+8	R17	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1077, Stress=0,7309
				R0805 10K 1% 0.125W	Resistor 10k	1.1.1.5.4	1	1,228e+9	R8	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,08748, Stress=0,7222
				R0805 10K 1% 0.125W		1.1.1.5.9	1	1,327e+9	R6	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,08121, Stress=0,7201
				R0805 100K 1% 0.125W	Resistor 100k	1.1.1.5.6	1	7,598e+9	R4	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,01438, Stress=0,7101
				BAV74	BAV74 - Data sheet	1.1.1.5.5	1	7,667e+11	D1	40	Supplier given	Temperature=0,001175
				PDTA114EU	PNP resistor-equipped transistor	1.1.1.5.3	1	1,087e+12	T4	40	Supplier given	Temperature=0,001296



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - ON_CB	ON_CB	1.1.1.5	3,057e+8	PDTA114EU	PNP resistor-equipped transistor	1.1.1.5.8	1	1,104e+12	T4	40	Supplier given	Temperature=0,001276
				PDTC114EU	NPN resistor-equipped transistor	1.1.1.5.7	1	1,169e+12	T1	40	Supplier given	Temperature=0,001204
				PDTC114EU		1.1.1.5.2	1	1,182e+12	T2	40	Supplier	Temperature=0,001191
Schematic block	Input monitor	1.1.2	2,771e+6	Sub-block - Buffer amplifier	Buffer amplifier	1.1.2.5	1	1,819e+7	N/A	40	N/A	N/A
				Sub-block - Filter 4x capacitor	Filter 4x capacitor	1.1.2.16	1	1,923e+7	N/A	40	N/A	N/A
				Sub-block - Filter 6x capacitor	Filter 6x capacitor	1.1.2.15	1	2,287e+7	N/A	40	N/A	N/A
				Sub-block - Filter 2x capacitor	Filter 2x capacitor	1.1.2.17	1	3,009e+7	N/A	40	N/A	N/A
				Sub-block - Comparators	Comparators	1.1.2.7	1	3,231e+7	N/A	40	N/A	N/A
				Sub-block - Power supply for dig.pot	Power supply for digital potmeter	1.1.2.13	1	3,594e+7	N/A	40	N/A	N/A
				Sub-block - Voltage reference generator	Voltage reference generator	1.1.2.6	1	4,502e+7	N/A	40	N/A	N/A
				Sub-block - Fully diff. integrator	Fully differential integrator	1.1.2.12	1	4,695e+7	N/A	40	N/A	N/A
				Sub-block - Saturation monitoring	Saturation monitoring block	1.1.2.2	1	6,513e+7	N/A	40	N/A	N/A
				Sub-block - Digital potentiometer	Digital potentiometer block	1.1.2.1	1	7,68e+7	N/A	40	N/A	N/A
				Sub-block - Stop	Stop block	1.1.2.3	1	9,128e+7		40	N/A	N/A
				Sub-block - Offset current & det. input	Offset current and detector input	1.1.2.9	1	1,111e+8	N/A	40	N/A	N/A
				Sub-block - Flip-Flop	Flip-Flop	1.1.2.8	1	1,23e+8	N/A	40	N/A	N/A
				Sub-block - Input switch	Input switch	1.1.2.11	1	1,424e+8	N/A	40	N/A	N/A



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Schematic block	Input monitor	1.1.2	2,771e+6	Sub-block - Input voltage filtering	Input voltage filtering	1.1.2.14	1	1,805e+8	N/A	40	N/A	N/A
				Sub-block - Switch FDFC / DADC to Input	Switch FDFC - DADC to Input Switch	1.1.2.10	1	2,083e+8	N/A	40	N/A	N/A
				Sub-block - Switch FDFC / DADC to ADC	Switch FDFC / DADC to ADC	1.1.2.4	1	1,311e+9	N/A	40	N/A	N/A
Sub-block - Digital potentiometer	Digital potentiometer block	1.1.2.1	7,68e+7	R0805 100R 1% 0.125W	Resistor 100Ω	1.1.2.1.3	2	1,859e+8	R56, R57	40	Fixed,Film, Insulated,NER	Base Failure Rate=3.7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,3392, Stress=1,231
				R0805 1K 1% 0.125W	Resistor 1k	1.1.2.1.2	3	1,913e+9	R32, R31, R30	40	Fixed,Film, Insulated,NER	Base Failure Rate=3.7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,05681, Stress=0,714
				AD5252BRU1	Digital Potentiometer	1.1.2.1.1	1	1,748e+11	IC9	40	Supplier given	Temperature=0,01168
Sub-block - Switch FDFC / DADC to Input	Switch FDFC - DADC to Input Switch	1.1.2.10	2,083e+8	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.2.10.2	1	2,146e+8	C91_2	40	Ceramic,General,NER	Base Failure Rate=9.9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				ADG849YKSZ	CMOS SPDT switch	1.1.2.10.1	1	3,738e+11	IC8_2	40	Supplier given	Temperature=0,003934
Sub-block - Input switch	Input switch	1.1.2.11	1,424e+8	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.2.11.2	1	2,146e+8	C70_2	40	Ceramic,General,NER	Base Failure Rate=9.9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				T491B196K006AS	Capacitor 10uF Tantalum	1.1.2.11.3	1	4,796e+8	C1_2	40	Tant Elect,Dry,ER	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=117,2, Circuit Resistance=0,66



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Input switch	Input switch	1.1.2.11	1,424e+8	ADG712BRZ	CMOS Low Voltage SPST Switch	1.1.2.11.1	1	4,051e+12	IC7_2	40	Supplier given	Temperature=0,001176
Sub-block - Fully diff. integrator	Fully differential integrator	1.1.2.12	4,695e+7	CC0603 1000PF 100V	Capacitor 1nF Ceramic	1.1.2.12.4	2	3,261e+8	C76, C79	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,537, Stress=1,001, Circuit Resistance=1
				CC0805 100pF 50V 10%	Capacitor 100pF Ceramic	1.1.2.12.6	1	3,995e+8	C75	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,4365, Stress=1,005, Circuit Resistance=1
				R0805 100R 1% 0.125W	Resistor 100Ω	1.1.2.12.5	2	6,031e+8	R47, R48	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,166, Stress=0,7753
				R0805 470R 1% 0.125W	Resistor 470Ω	1.1.2.12.3	4	6,696e+8	R42, R43, R44, R45	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1521, Stress=0,7618
				R0805 100R 1% 0.125W	Resistor 100Ω	1.1.2.12.1	2	2,109e+9	R46, R49	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,05159, Stress=0,7131
				OPA659DBV	JFET-Input Op-Amp	1.1.2.12.2	2	2,22e+9	IC14, IC15	40	Supplier given	Temperature=0,04433
				THS4502ID	Wideband, Low-Distortion Fully Differential Amplifiers	1.1.2.12.7	1	1,571e+11	IC1	40	Supplier given	Temperature=0,005786
Sub-block - Power supply for digital pot	Power supply for digital potmeter	1.1.2.13	3,594e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.2.13.1	2	2,146e+8	C3, C74	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Power supply for dig.pot	Power supply for digital potmeter	1.1.2.13	3,594e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.2.13.5	2	2,154e+8	C33, C32	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.2.13.4	1	2,652e+8	C37	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				T491B196K006AS	Capacitor 10uF Tantalum	1.1.2.13.2	2	4,796e+8	C11, C86	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=117,2, Circuit Resistance=0,66
				T491B196K006AS		1.1.2.13.6	2	5,615e+10	C41, C36	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=1,001, Circuit Resistance=0,66
				TPS73025DBV	Linear regulator	1.1.2.13.3	2	1,415e+12	RG2, RG1	40	Supplier given	Temperature=0,001766
Sub-block - Input voltage filtering	Input voltage filtering	1.1.2.14	1,805e+8	T491B196K006AS	Capacitor 10uF Tantalum	1.1.2.14.3	2	4,796e+8	C61, C62	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=117,2, Circuit Resistance=0,66
				NFM3DCC223U1H3	Capacitor 22000pF	1.1.2.14.1	2	7,377e+9	L5, L7	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=0,1, Temperature=1,922, Capacitance=0,7093, Stress=1,005, Circuit Resistance=1
				B82432A	Coil 1uH	1.1.2.14.2	2	7,377e+9	L4, L6	40	Supplier given	Base Failure Rate=3E-11, Environment=1, Quality=3, Temperature=1,506



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Filter 6x capacitor	Filter 6x	1.1.2.15	2,287e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.2.15.2	4	2,146e+8	C85, C44, C12, C39	40	Ceramic, General, NE R	Base Failure Rate=9.9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.2.15.3	4	2,652e+8	C7, C2, C13, C14	40	Ceramic, General, NE R	Base Failure Rate=9.9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				T491B196K006AS	Capacitor 10uF Tantalum	1.1.2.15.1	4	4,796e+8	C64, C92, C69, C20	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=117,2, Circuit Resistance=0,66
Sub-block - Filter 4x capacitor	Filter 4x capacitor	1.1.2.16	1,923e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic - 5V	1.1.2.16.2	6	2,146e+8	C26, C19, C28, C72, C21, C8	40	Ceramic, General, NE R	Base Failure Rate=9.9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic - 2.5V	1.1.2.16.4	2	2,154e+8	C40, C35	40	Ceramic, General, NE R	Base Failure Rate=9.9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				T491B196K006AS	Capacitor 10uF Tantalum - 5V	1.1.2.16.1	6	4,796e+8	C43, C6, C83, C82, C29, C16	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=117,2, Circuit Resistance=0,66
				T491B196K006AS	Capacitor 10uF Tantalum - 2.5V	1.1.2.16.3	2	5,615e+10	C34, C31	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=1,001, Circuit Resistance=0,66



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Filter 2x capacitor	Filter 2x capacitor	1.1.2.17	3,009e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.2.17.1	6	2,146e+8	C71, C15, C88, C80, C73, C30	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				T491B196K006AS	Capacitor 10uF Tantalum	1.1.2.17.2	2	4,796e+8	C25, C22	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=117,2, Circuit Resistance=0,66
Sub-block - Saturation monitoring	Saturation monitoring block	1.1.2.2	6,513e+7	CC0805 1UF 16V 10%	Capacitor 1uF Ceramic	1.1.2.2.8	1	1,722e+8	C84	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1, Stress=1,018, Circuit Resistance=1
				R0805 100R 1% 0.125W	Resistor 100Ω	1.1.2.2.1	1	2,697e+8	R53	40	Fixed, Film, Insulated, N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,285, Stress=1,01
				R0805 100R 1% 0.125W	Resistor 510Ω	1.1.2.2.7	1	7,487e+8	R50	40	Fixed, Film, Insulated, N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1382, Stress=0,7501
				R0805 3.3K 1% 0.125W	Resistor 3,3k	1.1.2.2.2	1	7,568e+8	R54	40	Fixed, Film, Insulated, N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1369, Stress=0,7492
				R0805 1K 1% 0.125W	Resistor 1k	1.1.2.2.5	1	1,06e+9	R55	40	Fixed, Film, Insulated, N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1006, Stress=0,7275
				R0805 470R 1% 0.125W	Resistor 470Ω	1.1.2.2.6	1	1,373e+9	R51	40	Fixed, Film, Insulated, N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,07857, Stress=0,7192
				MAX912CSE	Comparators	1.1.2.2.3	1	3,709e+9	IC17	40	Supplier	Temperature=0,1066



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Saturation monitoring	Saturation monitoring block	1.1.2.2	6,513e+7	R0805 10K 1% 0.125W	Resistor 10k	1.1.2.2.4	1	4,131e+9	R52	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,02643, Stress=0,7106
				BAV74	BAV74 - Data sheet	1.1.2.2.9	1	3,134e+10	D4	40	Supplier given	Temperature=0,02875
Sub-block - Stop		1.1.2.3	9,128e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.2.3.2	1	2,146e+8	C81	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				R0805 270R 1% 0.125W	Resistor 270Ω	1.1.2.3.4	1	2,697e+8	R35	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,285, Stress=1,01
				T491B196K006AS	Capacitor 10uF Tantalum	1.1.2.3.3	1	4,796e+8	C87	40	Tant Elect,Dry,ER	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=117,2, Circuit Resistance=0,66
				NC7SZ32M5	Two-Input OR Gate	1.1.2.3.1	1	1,137e+10	IC18	40	Supplier	Temperature=0,1256
Sub-block - Switch FDFC / DADC to ADC	Switch FDFC - DADC to ADC	1.1.2.4	1,311e+9	R0805 1K 1% 0.125W	Resistor 1k	1.1.2.4.1	1	1,602e+9	R9	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,06761, Stress=0,7163
				ADG1219BRJZ	SPDT-switch	1.1.2.4.2	2	3,984e+12	IC3, IC4	40	Supplier	Temperature=0,001195
Sub-block - Buffer amplifier	Buffer amplifier	1.1.2.5	1,819e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.2.5.8	1	2,154e+8	C90	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				R0805 100R 1% 0.125W	Resistor 100Ω	1.1.2.5.2	6	2,22e+8	R8, R4, R7, R5, R6, R3	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,3138, Stress=1,114



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Buffer amplifier	Buffer amplifier	1.1.2.5	1,819e+7	CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.2.5.9	1	2,652e+8	C89	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				R0805 24 ohm 1% 0.125W	Resistor 24Ω	1.1.2.5.5	2	3,6e+8	R2, R1	40	Fixed, Film, Insulated, N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,2413, Stress=0,8933
				CC0603 56PF 50V 5%	Capacitor 56PF Ceramic	1.1.2.5.6	2	4,212e+8	C98, C97	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,415, Stress=1,002, Circuit Resistance=1
				CC0603 47pF 50V 5%	Capacitor 47pF Ceramic	1.1.2.5.3	3	4,291e+8	C10, C9, C4	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,4078, Stress=1,001, Circuit Resistance=1
				T491B196K006AS	Capacitor 10uF Tantalum	1.1.2.5.7	1	5,615e+10	C93	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=1,001, Circuit Resistance=0,66
				OPA2690ID	Voltage Feedback Amplifier - Dual	1.1.2.5.1	1	7,875e+10	IC2	40	Supplier given	Temperature=0,00125
				THS4502ID	Wideband, Low-Distortion Fully Differential Amplifiers	1.1.2.5.4	1	2,13e+11	IC1	40	Supplier given	Temperature=0,004268
Sub-block - Voltage reference generator	Voltage reference generator	1.1.2.6	4,502e+7	R0805 100R 1% 0.125W	Resistor 100Ω	1.1.2.6.6	1	1,859e+8	R34	40	Fixed, Film, Insulated, N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,3392, Stress=1,231



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Voltage reference generator	Voltage reference generator	1.1.2.6	4,502e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.2.6.1	1	2,146e+8	C65	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				CC0805 100NF 50V 10%		1.1.2.6.7	1	2,154e+8	C67	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.2.6.4	1	2,652e+8	C66	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				T491B196K006AS	Capacitor 10uF Tantalum	1.1.2.6.2	1	4,796e+8	C38	40	Tant Elect, Dry, ER	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=117,2, Circuit Resistance=0,66
				R0805 1K 1% 0.125W	Resistor 1k	1.1.2.6.5	1	1,443e+9	R33	40	Fixed, Film, Insulated, NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,07489, Stress=0,7182
				T491B196K006AS	Capacitor 10uF Tantalum	1.1.2.6.8	1	5,615e+10	C68	40	Tant Elect, Dry, ER	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=1,698, Stress=1,001, Circuit Resistance=0,66
				TPS72301DBV	Negative Output Low-Dropout Linear Regulator	1.1.2.6.3	1	1,428e+12	RG4	40	Supplier given	Temperature=0,003503
Sub-block - Comparators	Comparators	1.1.2.7	3,231e+7	CC0805 1UF 16V 10%	Capacitor 1uF Ceramic	1.1.2.7.1	2	1,722e+8	C18, C17	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1, Stress=1,018, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Comparators	Comparators	1.1.2.7	3,231e+7	R0805 100R 1% 0.125W	Resistor 100Ω	1.1.2.7.5	2	1,859e+8	R12, R11	40	Fixed,Film, Insulated,N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,3392, Stress=1,231
				R0805 270R 1% 0.125W	Resistor 270Ω	1.1.2.7.6	2	8,051e+8	R16, R17	40	Fixed,Film, Insulated,N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1296, Stress=0,7439
				R0805 1K 1% 0.125W	Resistor 1k	1.1.2.7.2	2	9,492e+8	R10, R13	40	Fixed,Film, Insulated,N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1115, Stress=0,7329
				R0805 10K 1% 0.125W	Resistor 10k	1.1.2.7.4	2	1,212e+9	R14, R15	40	Fixed,Film, Insulated,N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,08859, Stress=0,7226
				MAX912CSE	Single/Dual Precision TTL Comparators	1.1.2.7.3	1	3,288e+9	IC5	40	Supplier given	Temperature=0,1202
				R0805 1K 1% 0.125W	Resistor 1k	1.1.2.7.9	1	6,344e+9	R21	40	Fixed,Film, Insulated,N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,01722, Stress=0,7102
				R0805 100R 1% 0.125W	Resistor 100Ω	1.1.2.7.8	1	7,432e+9	R20	40	Fixed,Film, Insulated,N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,0147, Stress=0,7101
				NC7SZ00M5	Two-Input NAND Gate	1.1.2.7.7	1	1,137e+10	IC6	40	Supplier given	Temperature=0,1256
Sub-block - Flip-Flop	Flip-Flop	1.1.2.8	1,23e+8	R0805 100R 1% 0.125W	Resistor 100Ω	1.1.2.8.5	2	4,625e+8	R37, R36	40	Fixed,Film, Insulated,N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,2036, Stress=0,8238



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Flip-Flop	Flip-Flop	1.1.2.8	1,23e+8	R0805 1K 1% 0.125W	Resistor 1k	1.1.2.8.2	2	7,487e+8	R39, R38	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1382, Stress=0,7501
				R0805 100R 1% 0.125W	Resistor 100Ω	1.1.2.8.3	2	9,74e+9	R40, R41	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,01122, Stress=0,7101
				NC7SZ74K8X	Flip-Flop	1.1.2.8.1	1	1,07e+10	IC13	40	Supplier	Temperature=0,1038
				BSS138	N-channel Enhancement mode FET	1.1.2.8.4	2	1,847e+11	T2, T1	40	Supplier given	Temperature=0,001547
Sub-block - Offset current & det. input	Offset current and detector input	1.1.2.9	1,111e+8	RC2512JK-7W47RL	Resistor 47Ω	1.1.2.9.2	1	2,403e+8	R29	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,4074, Stress=0,7926
				CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.2.9.3	1	2,651e+8	C63	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				R0805 3R 1% 0.125W	Shunt 3Ω	1.1.2.9.5	1	2,578e+9	R22	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,04227, Stress=0,7119
				BAV199	Low-leakage double diode	1.1.2.9.4	1	1,181e+10	D1	40	Supplier given	Temperature=0,07627
				R1206 1G 10% 0.250W	Resistor 1G	1.1.2.9.1	1	2,391e+10	R25	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,004571, Stress=0,71
Schematic block	ADC-channel	1.1.3	7,442e+6	Sub-block - ADC	ADC	1.1.3.1	1	1,306e+7	N/A	40	N/A	N/A
				Sub-block - Voltage level converter	Voltage level converter	1.1.3.2	1	3,205e+7	N/A	40	N/A	N/A



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Schematic block	ADC-channel	1.1.3	7,442e+6	Schematic block-1	ADC reference voltage	1.1.3.3	1	3,757e+7	N/A	40	N/A	N/A
Sub-block - ADC	ADC block	1.1.3.1	1,306e+7	CC1210 10uF 25V 10%	Capacitor 10uF Ceramic	1.1.3.1.1 3	1	1,195e+8	C48	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,037, Circuit Resistance=1
				CC1210 10uF 25V 10%		1.1.3.1.9	1	1,214e+8	C52	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,02, Circuit Resistance=1
				CC1210 10uF 25V 10%		1.1.3.1.1 1	1		C51	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,02, Circuit Resistance=1
				CC1210 10uF 25V 10%	Capacitor 100nF Ceramic	1.1.3.1.6	2	1,233e+8	C59, C56	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				CC0805 100NF 50V 10%		1.1.3.1.1 2	1	2,146e+8	C96	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				CC0805 100NF 50V 10%		1.1.3.1.3	1	2,15e+8	C60	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,003, Circuit Resistance=1
				CC0805 100NF 50V 10%		1.1.3.1.7	2	2,154e+8	C50, C54	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - ADC	ADC block	1.1.3.1	1,306e+7	CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.3.1.10	1	2,652e+8	C58	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				CC0805 10NF 200V 10%		1.1.3.1.8	2		C58, C55	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				R0402 100R 1% 0.063W	Resistor 100 ohm	1.1.3.1.4	4	1,589e+9	R103, R104, R26, R104	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,06761, Stress=0,7225
				R0805 10K 1% 0.125W	Resistor 10k	1.1.3.1.5	1	1,931e+9	R28	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,05629, Stress=0,7139
				74279243	74279243	1.1.3.1.14	1	2,463e+10	L3	40	N/A	Base Failure Rate=3E-11, Environment=1, Quality=1, Temperature=1,353
				AD7626BCPZ	AD7626BCPZ	1.1.3.1.1	1	2,901e+10	IC10	40	Supplier	Temperature=0,04788
				AD8032ARZ	AD8032ARZ	1.1.3.1.2	1	1,636e+11	IC11	40	Supplier	Temperature=0,04702
Sub-block - Voltage level converter	Voltage level converter	1.1.3.2	3,205e+7	CC1210 10uF 25V 10%	Capacitor 10uF Ceramic	1.1.3.2.3	1	1,195e+8	C47	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,037, Circuit Resistance=1
				CC1210 10uF 25V 10%		1.1.3.2.8	1	1,233e+8	C49	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,005, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Voltage level converter	Voltage level converter	1.1.3.2	3,205e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.3.2.4	1	2,146e+8	C45	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				CC0805 100NF 50V 10%		1.1.3.2.7	1	2,154e+8	C50	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.3.2.6	1	2,652e+8	C46	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				7447709220 - 22uH	7447709220 - 22uH	1.1.3.2.1	1	3,658e+9	L1	40	Supplier given	Base Failure Rate=3E-11, Environment=1, Quality=1, Temperature=9,113
				NFM3DCC223U1H3	Capacitor 22000pF	1.1.3.2.2	2	7,377e+9	L5, L7	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=0,1, Temperature=1,922, Capacitance=0,7093, Stress=1,005, Circuit Resistance=1
				TPS73025DBV	Linear regulator	1.1.3.2.5	1	7,859e+11	RG3	40	Supplier	Temperature=0,003181
Schematic block-1		1.1.3.3	3,757e+7	CC1210 10uF 25V 10%	Capacitor 10uF Ceramic	1.1.3.3.2	2	1,195e+8	C95	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,037, Circuit Resistance=1
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.3.3.3	2	2,146e+8	C94	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				ADR440BRZ	XFET Voltage Reference	1.1.3.3.1	1	3,759e+11	IC19	40	Supplier given	Temperature=0,00665



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Schematic block		1.1.4	6,544e+6	Sub-block - JTAG	JTAG	1.1.4.1	1	9,763e+6	N/A	40	N/A	N/A
				Sub-block - Channel and volt. suppl. con	Channel and voltage supply connectors	1.1.4.2	1	1,985e+7	N/A	40	N/A	N/A
Sub-block - JTAG		1.1.4.1	9,763e+6	J1	Connector 26 pin	1.1.4.1.2	1	3,665e+7	60 11 026 51	40	Rack and Panel	Base Failure Rate=1,05E-08, Environment=1, Quality=1, Mating/Unmating=2, Temperature=1,299
				MF-USMF005	Fuse for 2.5V	1.1.4.1.3	1	1e+8	F2, F3	40	Supplier given	Base Failure Rate=1E-08, Environment=1
				ESD9R3.3ST5G	TVS Diode (ESD protector)	1.1.4.1.1	12	1,95e+8	D11-D18, D27-D30	40	Transient Suppressor	Base Failure Rate=1,3E-09, Environment=1, Quality=2,4, Temperature=1,644, Stress=1, Contact Form=1
Sub-block - Channel and volt. suppl. con		1.1.4.2	1,985e+7	0903124x901	Backplane Connector - DIN 41612	1.1.4.2.3	1	3,417e+7	J5	40	Rack and Panel	Base Failure Rate=1,05E-08, Environment=1, Quality=1, Mating/Unmating=2, Temperature=1,394
				10nF Capacitor	10nF Capacitor	1.1.4.2.2	4	2,652e+8	C89-C92	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				09030006262	Coaxial connections	1.1.4.2.4	1	1,878e+9	LM1-LM8	40	RF Coaxial	Base Failure Rate=2,05E-10, Environment=1, Quality=1, Mating/Unmating=2, Temperature=1,299
				RC2512JK-7W47RL	1k Resistor	1.1.4.2.1	4	1,888e+9	R27-R29	40	Fixed, Film, Insulated, N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=1, Temperature=1,161, Power=0,1716, Stress=0,7186
Schematic block		1.1.5	3,497e+5	Sub-block - 3.3V DC/DC	3.3V DC/DC block	1.1.5.3	1	7,414e+5	N/A	40	Supplier given	
				Sub-block - 5V DC/DC	5V DC/DC block	1.1.5.2	1	7,455e+5	N/A	40	Supplier	



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Schematic block		1.1.5	3,497e+5	Sub-block - Step down	Step down current mode converter	1.1.5.5	1	1,372e+7	N/A	40	N/A	N/A
				Sub-block - +48V Input voltage	+48V Input voltage block	1.1.5.1	1	1,548e+7	N/A	40	N/A	N/A
				Sub-block - Voltage converter	Voltage converter 3,3V to 2,5V	1.1.5.4	1	3,128e+7	N/A	40	N/A	N/A
Sub-block - +48V Input voltage	+48VDC Input	1.1.5.1	1,548e+7	CC1210 10uF 25V 10%	Capacitor 1uF Ceramic	1.1.5.1.5	1	1,226e+8	C116	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,011, Circuit Resistance=1
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.5.1.2	1	1,426e+8	C119	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,512, Circuit Resistance=1
				CC2220 4UF 100V 10%	Capacitor 4.7uF Ceramic	1.1.5.1.7	5	1,523e+8	C117, C134, C135, C138, C139	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,149, Stress=1,001, Circuit Resistance=1
				CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.5.1.8	3	2,492e+8	C118, C136, C133	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1,064, Circuit Resistance=1
				R1206 2M 1% 0.25W	Resistor 2M	1.1.5.1.1	2	1,999e+9	R67	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,05452, Stress=0,7118
				R0805 10K 1% 0.125W	Resistor 10k	1.1.5.1.4	2	2,039e+9	R64	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,05334, Stress=0,7134



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - +48V Input voltage	+48VDC Input	1.1.5.1	1,548e+7	SRR1210-221M	Coil 220uH	1.1.5.1.9	2	5,474e+9	L14, L13	40	Supplier given	Base Failure Rate=3E-11, Environment=1, Quality=3, Temperature=2,03
				P-Channel 60-V	P-Channel 60V	1.1.5.1.3	1	7,336e+11	T9	40	Supplier	Temperature=0,0005582
				BCX19	NPN Transistor	1.1.5.1.6	1	7,974e+11	T8	40	Supplier	Temperature=0,001766
Sub-block - 5V DC/DC	+48V to +5V DC/DC converter	1.1.5.2	7,455e+5	MGDBI-20-Q-C/M	DC/DC Converter 5V	1.1.5.2.3	1	7,519e+5	PW2	40	Supplier given	
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.5.2.6	2	2,146e+8	C41, C42	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,005, Circuit Resistance=1
				R0805 3.3K 1% 0.125W	Resistor 3,3k	1.1.5.2.1	1	3,965e+9	R2	40	Fixed, Film, Insulated, N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,02754, Stress=0,7106
				7447709220	Coil 22uH	1.1.5.2.5	2	5,474e+9	L11, L10	40	Supplier given	Base Failure Rate=3E-11, Environment=1, Quality=3, Temperature=2,03
				597D476X0050Z2T	Capacitor 47uF Tantalum	1.1.5.2.4	4	1,999e+10	C36, C23, C25, C42	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=2,424, Stress=1, Circuit Resistance=1,3
				PDTC114EU	PDTC114 - Data sheet	1.1.5.2.2	1	7,215e+11	T10	40	Supplier given	Temperature=0,001952
Sub-block - 3.3V DC/DC	Voltage converter 3,3V to 2,5V	1.1.5.3	7,414e+5	MGDSI-10-Q-B	DC/DC Converter 3,3V	1.1.5.3.2	1	7,519e+5	PW1	40	Supplier given	
				CC2220 4UF 100V 10%	Capacitor 4.7uF Ceramic	1.1.5.3.1	2	1,524e+8	C141, C142	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,149, Stress=1, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - 3.3V DC/DC	Voltage converter 3,3V to 2,5V	1.1.5.3	7,414e+5	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.5.3.5	1	2,153e+8	C130	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				7447709220	Coil 22uH	1.1.5.3.4	1	6,923e+9	L8	40	Supplier given	Base Failure Rate=3E-11, Environment=1, Quality=3, Temperature=1,605
				597D476X0050Z2T	Capacitor 47uF Tantalum	1.1.5.3.3	2	1,999e+10	C35, C34	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=2,424, Stress=1, Circuit Resistance=1,3
Sub-block - Voltage converter	Voltage converter 3,3V to 2,5V	1.1.5.4	3,128e+7	CC1210 100UF 6V3 10%	Capacitor 100uF Ceramic	1.1.5.4.1	1	1,158e+8	C128	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,514, Stress=1, Circuit Resistance=1
				CC1210 100UF 6V3 10%		1.1.5.4.4	2		C131	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,514, Stress=1, Circuit Resistance=1
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.5.4.2	1	2,153e+8	C129	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				LT1963AEST-2.5	Voltage level converter	1.1.5.4.3	1	1,246e+10	RG2	40	Supplier given	Temperature=0,08446
				7447709220	Coil 22uH	1.1.5.4.6	2	1,642e+10	L5	40	Supplier given	Base Failure Rate=3E-11, Environment=1, Quality=1, Temperature=2,03



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Voltage converter	Voltage converter 3,3V to 2,5V	1.1.5.4	3,128e+7	597D476X0050Z2T	Capacitor 47uF Tantalum	1.1.5.4.5	2	1,999e+10	C17,C16	40	Tant Elect,Dry,ER	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=2,424, Stress=1, Circuit Resistance=1,3
Sub-block - Step down	Step down current mode converter	1.1.5.5	1,372e+7	CC1210 100UF 6V3 10%	Capacitor 100uF Ceramic	1.1.5.5.1	3	1,158e+8	C26, C27, C28	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,514, Stress=1, Circuit Resistance=1
				CC1210 100UF 6V3 10%		1.1.5.5.14	1		C144	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,514, Stress=1, Circuit Resistance=1
				CC1210 100UF 6V3 10%		1.1.5.5.17	2		C108, C107	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,514, Stress=1, Circuit Resistance=1
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.5.5.10	1	2,155e+8	C30	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1, Circuit Resistance=1
				CC0805 22NF 50V 10%	Capacitor 22nF Ceramic	1.1.5.5.7	1	2,468e+8	C32	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,7093, Stress=1,001, Circuit Resistance=1
				CC0805 15NF 50V 10%	Capacitor 15nF Ceramic	1.1.5.5.3	1	2,554e+8	C31	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6852, Stress=1,001, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Step down	Step down current mode converter	1.1.5.5	1,372e+7	CC0603 1000PF 100V	Capacitor 1000pF Ceramic	1.1.5.5.5	1	3,262e+8	C33	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,537, Stress=1, Circuit Resistance=1
				R0805 3K 1% 0.125W	Resistor 3k	1.1.5.5.6	1	1,026e+9	R94	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1038, Stress=0,729
				R0805 100K 1% 0.125W	Resistor 100k PWRGD	1.1.5.5.8	1	3,835e+9	R13	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,02847, Stress=0,7107
				R0805 100K 1% 0.125W	Resistor 100k EN	1.1.5.5.2	2	5,044e+9	R11, R12	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,02166, Stress=0,7103
				VLCF5020T-3R3N2R0-1	Coil 3.3uH	1.1.5.5.1 1	1	6,923e+9	L19	40	Supplier given	Base Failure Rate=3E-11, Environment=1, Quality=3, Temperature=1,605
				R0805 100K 1% 0.125W	Resistor 100k+100k	1.1.5.5.1 3	1	1,519e+10	R15, R95	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,007195, Stress=0,71
				R0805 100K 1% 0.125W	Resistor 100k	1.1.5.5.1 2	1	1,991e+10	R14	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,00549, Stress=0,71
				B82432A1102K	22uH Coil	1.1.5.5.1 6	2	2,077e+10	L4, L3	40	Supplier given	Base Failure Rate=3E-11, Environment=1, Quality=1, Temperature=1,605
				R0805 390K 1% 0.125W	Resistor 390k	1.1.5.5.4	1	2,846e+10	R16	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,003841, Stress=0,71



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Step down	Step down current mode converter	1.1.5.5	1,372e+7	47nF 50V 10%	Capacitor 47nF Tantalum	1.1.5.5.1 5	4	9,789e+10	C15, C13, C12, C14	40	Tant Elect,Dry,ER	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=0,495, Stress=1, Circuit Resistance=1,3
				TPS54318	Step down current mode converter	1.1.5.5.9	1	1,001e+12	RG1	40	Supplier given	Temperature=0,004997
Schematic block		1.1.6	3,301e+5	Sub-block - SFP connector	SFP connector	1.1.6.1	1	3,326e+5	N/A	40	N/A	N/A
				Sub-block - Light indicators	Light indicators	1.1.6.2	1	4,397e+7	N/A	40	N/A	N/A
Sub-block - SFP connector		1.1.6.1	3,326e+5	FT3A05D	Optical Transceiver	1.1.6.1.7	2	7,556e+5		40	N/A	N/A
				1888247-1	SFP - Connector	1.1.6.1.6	1	4,813e+6	J2, J3	40	Card Edge (PCB)	Base Failure Rate=4E-08, Environment=1, Quality=2, Mating/Unmating=2, Temperature=1,299
				74279243 - FERRIT, SMD 75OHM, 3A	75 Ohm ferrite bead	1.1.6.1.2	4	4,545e+7	L2,L7,L15,L17	40	Supplier given	Base Failure Rate=2,2E-08, Environment=1, Quality=1
				CC1210 10uF 25V 10%	Capacitor 10uF Ceramic	1.1.6.1.1	4	1,226e+8	C115, C114, C132, C151	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,011, Circuit Resistance=1
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.6.1.4	4	2,153e+8	C8, C113, C29, C143	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				R0805 10K 1% 0.125W	Resistor 10k	1.1.6.1.5	10	1,549e+9	R84-R93	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,06989, Stress=0,7168



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - SFP connector		1.1.6.1	3,326e+5	B82432A1102K	1uH Coil	1.1.6.1.3	4	2,077e+10	L1, L16, L6, L18	40	Supplier given	Base Failure Rate=3E-11, Environment=1, Quality=1, Temperature=1,605
Sub-block - Light indicators		1.1.6.2	4,397e+7	H485CGDL	Light diodes	1.1.6.2.3	0	0e+0	LD2-LD4	40	Diode Array	Base Failure Rate=8,13E-10, Environment=1, Quality=2,4, Temperature=2,177
				R0805 1K 1% 0.125W	Resistor 1k	1.1.6.2.1	6	3,697e+8	R3-R6, R63	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,2372, Stress=0,8847
				R0805 510R 1% 0.125W	Resistor 510 ohm	1.1.6.2.2	2	3,697e+8	R60, R61	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,2372, Stress=0,8847
Schematic block		1.1.7	1,25e+7	Sub-block - Relay activation	Relay activation	1.1.7.1	1	1,454e+7	N/A	40	N/A	N/A
				Sub-block - Relay status	Relay status	1.1.7.2	1	8,914e+7	N/A	40	N/A	N/A
Sub-block - Relay activation		1.1.7.1	1,454e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.7.1.3	8	2,153e+8	C120 - C127	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				R0805 1K 1% 0.125W	Resistor 1k	1.1.7.1.1	16	5,788e+8	R68 - R83	40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1716, Stress=0,7814
				BAV199	Low-leakage double diode	1.1.7.1.2	8	1,181e+10	D3 - D10	40	Supplier given	Temperature=0,07627
Sub-block - Relay status		1.1.7.2	8,914e+7	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.7.2.3	2	2,153e+8	C45 - C46	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - Relay status		1.1.7.2	8,914e+7	R0805 10K 1% 0.125W	Resistor 10k	1.1.7.2.1	2	1,549e+9	R22, R23	40	Fixed,Film, Insulated,N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,06989, Stress=0,7168
				BAV199	Low-leakage double diode	1.1.7.2.2	1	1,181e+10	D2	40	Supplier given	Temperature=0,07627
Schematic block		1.1.8	1,267e+7	Sub-block - ADC for housekeeping	ADC for housekeeping	1.1.8.3	1	2,841e+7	N/A	40	N/A	N/A
				Sub-block - HV feedback	HV feedback	1.1.8.4	1	3,163e+7	N/A	40	N/A	N/A
				Sub-block - Serial number generator	Serial Number Generator	1.1.8.1	1	9,798e+7	N/A	40	N/A	N/A
				Sub-block - Temp. and humidity sensor	Temp. and humidity sensor	1.1.8.2	1	5,215e+8	N/A	40	N/A	N/A
Sub-block - Serial number generator		1.1.8.1	9,798e+7	CC1210 100UF 6V3 10%	Capacitor 100uF Ceramic	1.1.8.1.3	1	1,158e+8		40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,514, Stress=1, Circuit Resistance=1
				R0805 2K 1% 0.125W	Resistor 2k	1.1.8.1.2	1	7,957e+8	R58	40	Fixed,Film, Insulated,N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1309, Stress=0,7448
				DS2411R	Silicon Serial Number Generator	1.1.8.1.1	1	2,897e+10	IC4	40	Supplier given	Temperature=0,03836
Sub-block - Temp. and humidity sensor		1.1.8.2	5,215e+8	R0805 1K 1% 0.125W	Resistor 1k	1.1.8.2.2	1	5,788e+8	R59	40	Fixed,Film, Insulated,N ER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1716, Stress=0,7814
				Sht15	Humidity and Temperature Sensor	1.1.8.2.1	1	1,932e+10	IC3	40	Supplier given	Temperature=0,004174



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - ADC for housekeeping		1.1.8.3	2,841e+7	CC0805 1uF 16V 10% X	Capacitor 1uF Ceramic	1.1.8.3.2	3	1,684e+8	C40, C38, C2	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1, Stress=1,041, Circuit Resistance=1
				CC0805 100nF 50V 10%	Capacitor 100nF Ceramic	1.1.8.3.3	3	2,153e+8	C37, C39, C1	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				R0805 10K 1% 0.125W	Resistor 10k	1.1.8.3.5	3	1,549e+9	R17-R19	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,06989, Stress=0,7168
				LM4140BCM-2.0	High Precision Voltage Reference	1.1.8.3.1	1	4,238e+9	IC7	40	Supplier given	Temperature=0,118
				AD7927BRUZ	8-Channel ADC	1.1.8.3.4	1	3,905e+10	IC1	40	Supplier	Temperature=0,04001
Sub-block - HV feedback		1.1.8.4	3,163e+7	CC0805 100nF 50V 10%	Capacitor 100nF Ceramic	1.1.8.4.2	6	2,153e+8	C43, C44, C154, C153, C152, C155	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				R0805 10K 1% 0.125W	Resistor 10k	1.1.8.4.3	3	1,549e+9	R20, R21, R1	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,06989, Stress=0,7168
				R0805 51K 1% 0.125W	Resistor 51k	1.1.8.4.1	1	2,949e+9	R145	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,03699, Stress=0,7113
				BAV199	Low-leakage double diode	1.1.8.4.4	1	1,181e+10	D1	40	Supplier given	Temperature=0,07627
				ADR130BUJZ	Precision Voltage Reference	1.1.8.4.6	1	3,944e+11	IC6	40	Supplier given	Temperature=0,006339



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - HV feedback		1.1.8.4	3,163e+7	AD8226	Rail-to-Rail Instrumental Amplifier	1.1.8.4.5	1	5,604e+11	SOIC	40	Supplier given	Temperature=0,004461
Schematic block		1.1.9	1,076e+6	Sub-block - FPGA filters	FPGA filters	1.1.9.4	1	3,161e+6	N/A	40	N/A	N/A
				Sub-block - FPGA external memory	FPGA external memory	1.1.9.2	1	3,701e+6		40	N/A	N/A
				Sub-block - FPGA chip	FPGA chip	1.1.9.1	1	6,562e+6	N/A	40	N/A	N/A
				Sub-block - FPGA reset	FPGA reset	1.1.9.3	1	8,504e+6	N/A	40	N/A	N/A
				Sub-block - FPGA oscillator	FPGA oscillator	1.1.9.5	1	1,372e+7	N/A	40	N/A	N/A
Sub-block - FPGA chip		1.1.9.1	6,562e+6	EP4CGX150CF23C7N	Altera Cyclone IV FPGA	1.1.9.1.1	1	6,562e+6	IC5	40	Supplier given	
Sub-block - FPGA external memory		1.1.9.2	3,701e+6	EPCS128SI16N	EPC Code chip	1.1.9.2.1	1	3,701e+6	IC2	40	Supplier given	Temperature=1
Sub-block - FPGA reset		1.1.9.3	8,504e+6	System Block-5-3-1	Jumper	1.1.9.3.1	1	0e+0		40	N/A	N/A
				System Block-5-3-2	Push button	1.1.9.3.8	1	1e+7		40	Pushbutton	Base Failure Rate=1E-07, Environment=1, Quality=1, Contact Configuration=1, Load Stress=1
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.9.3.4	1	2,153e+8	C148	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic CT	1.1.9.3.5	1	2,156e+8	C148	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - FPGA reset		1.1.9.3	8,504e+6	CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.9.3.7	1	2,652e+8	C147	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				CC0603 1000PF 100V 1	Capacitor 1000pF Ceramic	1.1.9.3.2	1	3,262e+8	C149	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,537, Stress=1, Circuit Resistance=1
				R0805 10K 1% 0.125W	Resistor 10k	1.1.9.3.6	1	1,549e+9	R96	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,06989, Stress=0,7168
				TPS3808G30DBVT	Programmable-Delay Supervisory Circuit	1.1.9.3.3	1	1,187e+12	RG3	40	Supplier given	Temperature=0,001203
Sub-block - FPGA filters		1.1.9.4	3,161e+6	Sub-block - 1.2V supply voltage	1.2V supply voltage	1.1.9.4.3	1	7,097e+6	N/A	40	N/A	N/A
				Sub-block - 3.3V supply voltage	3.3V supply voltage	1.1.9.4.1	1	8,785e+6	N/A	40	N/A	N/A
				Sub-block - 2.5V supply voltage	2.5V supply voltage	1.1.9.4.2	1	1,622e+7	N/A	40	N/A	N/A
Sub-block - 3.3V supply voltage		1.1.9.4.1	8,785e+6	MF-USMF005	Fuse	1.1.9.4.1.3	1	1e+8	F1	40	Supplier given	Base Failure Rate=1E-08, Environment=1
				CC1210 10uF 25V 10%	Capacitor 10uF Ceramic	1.1.9.4.1.1	6	1,226e+8	C58-C60, C66	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,011, Circuit Resistance=1
				R0805 100R 1% 0.125W	Resistor 100 ohm	1.1.9.4.1.6	1	1,859e+8	R38	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,3392, Stress=1,231



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - 3.3V supply voltage		1.1.9.4.1	8,785e+6	CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.9.4.1.2	7	2,153e+8	C55, C97, C63, C88, C48, C87	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.9.4.1.4	2	2,652e+8	C76, C94	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				R0805 24R 1% 0.125W	Resistor 24 ohm	1.1.9.4.1.8	1	6,031e+8	R35	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,166, Stress=0,7753
				R0805 2K 1% 0.125W	Resistor 2k	1.1.9.4.1.7	1	7,957e+8	R34	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1309, Stress=0,7448
				R0805 10K 1% 0.125W	Resistor 10k	1.1.9.4.1.5	5	1,549e+9	R33, R32, R31, R36, R37	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,06989, Stress=0,7168
Sub-block - 2.5V supply voltage		1.1.9.4.2	1,622e+7	CC1210 10uF 25V 10%	Capacitor 10uF Ceramic	1.1.9.4.2.9	1	1,233e+8		40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,005, Circuit Resistance=1
				CC1210 4.7uF 50V 10%	Capacitor 4.7uF Ceramic	1.1.9.4.2.2	1	1,523e+8	C10	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,149, Stress=1,001, Circuit Resistance=1
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.9.4.2.3	4	2,154e+8	C53, C83, C100	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - 2.5V supply voltage		1.1.9.4.2	1,622e+7	CC0402 4NF7 50V 10%	Capacitor 4.7nF Ceramic	1.1.9.4.2.6	1	2,306e+8	C61	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,7594, Stress=1,001, Circuit Resistance=1
				CC0402 22NF 16V 10%	Capacitor 22nF Ceramic	1.1.9.4.2.4	1	2,427e+8	N/A	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,7093, Stress=1,018, Circuit Resistance=1
				CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.9.4.2.5	1	2,652e+8	C102	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				CC0402 2NF2 50V 10%	Capacitor 2.2nF Ceramic	1.1.9.4.2.7	2	3,037e+8	C93, C70	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,5765, Stress=1,001, Circuit Resistance=1
				CC0402 2NF2 50V 10%	Capacitor 1nF Ceramic	1.1.9.4.2.8	1	3,037e+8	C50	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,5765, Stress=1,001, Circuit Resistance=1
				R0805 1K 1% 0.125W	Resistor 1k	1.1.9.4.2.10	3	7,487e+8	R41, R42, R39	40	Fixed, Film, Insulated, NE R	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,1382, Stress=0,7501
				N2510-6002RB	Connector 10 pin	1.1.9.4.2.11	1	1,449e+10	J4	0	Reflow Solder	Base Failure Rate=6,9E-11, Environment=1
				597D476X0050Z2T	Capacitor 47uF Tantalum	1.1.9.4.2.1	1	3,937e+10	C9	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=2,424, Stress=1, Circuit Resistance=0,66



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - 1.2V supply voltage		1.1.9.4.3	7,097e+6	CC1210 10uF 25V 10%	Capacitor 10uF Ceramic	1.1.9.4.3.7	2	1,238e+8	C19, C49	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,414, Stress=1,001, Circuit Resistance=1
				CC1210 4.7uF 50V 10%	Capacitor 4.7uF Ceramic	1.1.9.4.3.2	2	1,524e+8	C11, C67	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=1,149, Stress=1, Circuit Resistance=1
				CC0805 100nF 50V 10%	Capacitor 100nF Ceramic	1.1.9.4.3.3	15	2,155e+8	C64, C65, C62, C80-C82, C103, C52, C84, C71	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1, Circuit Resistance=1
				CC0402 4nF7 50V 10%	Capacitor 4.7nF Ceramic	1.1.9.4.3.5	2	2,307e+8	C98, C96	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,7594, Stress=1, Circuit Resistance=1
				CC0805 10nF 200V 10%	Capacitor 10nF Ceramic	1.1.9.4.3.4	6	2,652e+8	C104, C51	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				CC0402 2nF2 50V 10%	Capacitor 2.2nF Ceramic	1.1.9.4.3.6	2	3,039e+8	C98, C96	40	Ceramic, General, NE R	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,5765, Stress=1, Circuit Resistance=1
				597D476X0050Z2T	Capacitor 47uF Tantalum	1.1.9.4.3.1	1	3,937e+10	C105, C106	40	Tant Elect, Dry, E R	Base Failure Rate=4E-10, Environment=1, Quality=0,03, Temperature=1,323, Capacitance=2,424, Stress=1, Circuit Resistance=0,66



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
Reliability Responsibility: Vegard Joa Moseng (BI/BL)

Reliability Prediction - Mean Time To Failure

Prediction Number: 005
Date: 30.08.2013
Prediction Date (Orig.): 18.05.2013
Rev.: A
Standard used: MIL-HDBK-217F notice 2

Parent block type	Parent block name	Parent ID nr	Parent MTTF	Block type & Part nr	Sub-block & component	ID	X	MTTF	Sch.nr	Temp	Sub category	Pi Values
Sub-block - FPGA oscillator		1.1.9.5	1,372e+7	R0805 51R 1% 0.125W	Resistor 51Ω	1.1.9.5.4	4	8,485e+7		40	Fixed,Film, Insulated,NER	Base Failure Rate=3,7E-09, Environment=1, Quality=3, Temperature=1,161, Power=0,4402, Stress=2,077
				CC0805 100NF 50V 10%	Capacitor 100nF Ceramic	1.1.9.5.1	2	2,154e+8	C22, C168	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,8128, Stress=1,001, Circuit Resistance=1
				CC0805 10NF 200V 10%	Capacitor 10nF Ceramic	1.1.9.5.3	4	2,652e+8	C169, C170, C20, C21	40	Ceramic,General,NER	Base Failure Rate=9,9E-10, Environment=1, Quality=3, Temperature=1,922, Capacitance=0,6607, Stress=1, Circuit Resistance=1
				530FC125M000DG	Crystal Oscillator	1.1.9.5.2	1	5,18e+10	QZ2, QZ1	40	Supply	Temperature=0,03861



System: BLEAC
Sub-system: BLEDP
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.1.1.1	Sub-block - +5v	2.722e-8	0.05Ω Shunt - Open	Random failure	No voltage can pass out of the circuit breaker	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.1.2			0.05Ω Shunt - Short	Random failure	No current measurements -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.1.3			0.05Ω Shunt - Parameter Change	Random failure	Shunt tolerance is 1%, but if the parametric drift is > 10%, load measurement is out of the error threshold	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.1.4			Defective MAX4272	Random failure	No current measurements -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.1.5			1k Resistor - Open	Random failure	No voltage can pass to the Gate drive input -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.1.6			MOSFET - Short	Random failure	Voltage will pass directly, or in a limited way -> Lack of protection.	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.1.7			MOSFET - Open	Random failure	No voltage can pass out of the circuit breaker	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.1.8			100nF Capacitor, Gate on MOSFET - Short	Random failure	No current measurements -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.1.9			Filtering capacitors - Short	Random failure	+5V will pass through Capacitors -> Drained to Ground	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.2.1	Sub-block - Feedback	6.145e-9	0.025Ω Shunt - Open	Random failure	No voltage can pass out of the circuit breaker	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.2.2			0.025Ω Shunt - Short	Random failure	Current Shunt Monitors can't detect the current through Rsense -> No feedback on current levels -> No diagnostics	Maintenance - Erroneous diagnostics	2	1	1	2	Maintenance fix. Detectable, no special action is warranted.
1.1.1.2.3			0.025Ω Shunt - Parameter Change	Random failure	Parametric drift will cause measured current levels to be wrong -> Erroneous diagnostics	Maintenance - Erroneous diagnostics	2	1	2	4	Not detectable, but non critical. Can be added to a maintenance check.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.1.2.4	Sub-block - Feedback	6.145e-9	Current Shunt Monitor - Open	Random failure	Measured current can't be sent to the ADC -> No diagnostics	Maintenance - No diagnostics	2	1	1	2	Maintenance fix. Detectable, no special action is warranted.
1.1.1.2.5			10k Resistor - Open	Random failure	Measured current can't be sent to the ADC -> No diagnostics	Maintenance - No diagnostics	2	1	1	2	Detectable, no special action is warranted.
1.1.1.2.6			100k Resistor - Short	Random failure	Measured current signal will be drained to Ground -> Can't send information to the ADC -> No diagnostics	Maintenance - No diagnostics	2	1	1	2	Detectable, no special action is warranted.
1.1.1.2.7			100nF Capacitor - Short	Random failure	Measured current signal will be drained to Ground -> Can't send information to the ADC -> No diagnostics	Maintenance - No diagnostics	2	1	1	2	Detectable, no special action is warranted.
1.1.1.3.1	Sub-block - -5v	7.821e-9	0.2Ω Shunt - Parameter Change	Random failure	Shunt tolerance is 1%, but if the parametric drift is > 10%, load measurement is out of the error threshold	False dump - Loss of operation for 4 BLM's	3	1	2	6	Detectable, no special action is warranted.
1.1.1.3.10			Filtering capacitors - Short	Random failure	-5V will pass through Capacitors -> Drained to Ground	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.3.2			0.2Ω Shunt - Open	Random failure	No voltage can pass out of the circuit breaker	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.3.3			0.2Ω Shunt - Short	Random failure	No current measurements -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.3.4			MOSFET - Short	Overvoltage	Voltage will pass directly, or in a limited way -> Lack of protection.	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.3.5			MOSFET - Open	Random failure	No voltage can pass out of the circuit breaker	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.3.6			100Ω Resistor - Open	Random failure	No voltage can pass to the Gate drive input -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.1.3.7	Sub-block - -5v	7.821e-9	10nF Capacitor - Short	Random failure	-5V will pass to MOSFET Gate -> Continuous voltage output -> No protection	Maintenance - No protection on the -5V -> can cause damage in the BLEDP -> Need dual failure before its critical.	2	1	1	2	Detectable, no special action is warranted.
1.1.1.3.8			Defective MAX5901	Random failure	Internal error check -> IC will self diagnose an error condition. All errors -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.3.9			10k Resistor - Short		Fault condition for the MAX5901 -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.4.1	Sub-block - Powergood	7.762e-9	12k Resistor - Short	Random failure	Powergood signal is continuously high > Potentially wrong diagnostics on overcurrents -> Loss of retry function	Maintenance - Powergood continuously high will indicate good operation even with an error condition. No retry can be done if the system triggers on a false or temporary overvoltage	2	1	2	4	Not detectable in normal operation. Short is very unlikely, but a fix could be to split up the 12k resistor into two, making it single failure tolerant.
1.1.1.4.2			NPN-transistor - Open	Random failure	No powergood -> no enable -> no voltage output	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.4.3			NPN transistor - Short	Random failure	Shorts to Ground -> Loss of powergood signal -> no enable -> no voltage output	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.4.4			PNP-transistor - Open	Random failure	No powergood -> no enable -> no voltage output	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.4.5			PNP-transistor - Short	Random failure	Short to +5V -> Powergood signal is broken -> no powergood -> no voltage output	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.5.1	Sub-block - ON_CB	3.271e-9	3,3k Resistor - Short	Random failure	ON_CB (enable) drained to Ground -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.1.5.2	Sub-block - ON_CB	3.271e-9	Diode - Open	Random failure	ON_CB can't enable MAX5901 -> No voltage can pass through MOSFET on -5V output	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.5.3			100k Resistor - Open	Random failure	No enable for MAX5901 -> No voltage can pass through MOSFET on -5V output	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.5.4			NPN-transistors - Open	Random failure	No enable for MAX5901 or MAX4272 -> No voltage can pass through MOSFET -5V and +5V output	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.5.5			NPN-transistors - Short	Random failure	Enable will be driven to Ground or -5V -> No enable can pass	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.5.6			PNP-transistors - Open	Random failure	No enable for MAX5901 or MAX4272 -> No voltage can pass through MOSFET -5V and +5V output	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.5.7			PNP-transistors - Short	Random failure	Too high voltage on enable -> fault condition on hot-swap IC -> No voltage can pass through MOSFET	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.5.8			10k Resistor - Open -5V	Random failure	No pull function on transistor input -> Enable may not pass through the transistor	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.1.5.9			10k Resistor - Open +5V	Random failure	No enable for MAX5901 -> No voltage can pass through MOSFET on -5V output	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.2.1.1	Sub-block - Digital potentiometer	1.302e-8	1k Resistors - Open I2C	Random failure	No pull up function -> Bad I2C connection -> No or erroneous default threshold	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.1.2			1k Resistors - Short I2C	Random failure	I2C is set continuously high -> No I2C -> No default threshold	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.1.3			100Q Resistor - Open W1	Random failure	No voltage in on A1 and B1, for Dig.Pot Channel 1 -> No offset current	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.1.4	Sub-block - Digital potentiometer	1.302e-8	Digital potentiometer - Latch up	Power-up sequence (VMDD->V MSS->GND ->VA ->VB) is not followed.	Short due to a low-impedance path, causing disruption in functionality, or destruction due to overcurrents -> No remote calibration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.1.5			Digital potentiometer - Overvoltage	Overvoltage greater than VMDD - VMSS across A-B, W-B, or W-A	Destruction of Dig.Pot due to overvoltage -> No remote calibration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.10.1	Sub-block - Switch FDFC / DADC to Input	4.801e-9	FDFC to DADC switch - Open	Random failure	No signal can pass to the FDFC -> Loss of measurement	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.10.2			FDFC to DADC switch - Sticking	Random failure	Can't switch to the desired measuring method -> Loss of measurement	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.10.3			FDFC to DADC switch - Short	Random failure	FDFC signal will be drained to ground, or pass to the output when toggled off -> Erroneous measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.10.4			Filtering capacitor - Short	Random failure	Supply voltage will be drained to Ground -> Loss of measurement	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.11.1	Sub-block - Input switch	7.022e-9	Input switch - Open	Random failure	No output to either polarity branch in the FDFC -> Loss of measurement	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.11.2			Input switch - Sticking	Random failure	Wrong polarity branch in the FDFC -> Loss of measurement	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.11.3			Input switch - Short	Random failure	FDFC signal will be drained to ground, or pass to the output when toggled off -> Erroneous measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.11.4	Sub-block - Input switch	7.022e-9	Filtering capacitor - Short	Random failure	Supply voltage will be drained to Ground -> Loss of measurement	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.12.1	Sub-block - Fully diff. integrator	2.13e-8	100Ω Resistor - Open	Random failure	No signal can pass to the affected polarity branch in the FDFC -> No measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.12.10			Fully differential amplifier - Erroneous output from parameter change and leaks	Random failure	Wrong signal will pass to the comparators and the ADC -> Wrong measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.12.11			Fully differential amplifier - Short	Random failure	Signal will pass through, or the supply voltage will leak into the component/system and cause an erroneous output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.12.2			JEFT - Open	Random failure	No signal can pass to the affected polarity branch in the FDFC -> No measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.12.3			JEFT - Erroneous output from parameter change and leaks	Random failure	Measured input signal levels sent to the FDFC will be erroneous	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.12.4			JEFT - Short	Random failure	Signal will pass through, or the supply voltage will leak into the component/system and cause an erroneous output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.12.5			470Ω Resistor - Open	Random failure	No voltage division on the input which will cause the gain to be wrong -> Erroneous measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.12.6			470Ω Resistor - Parameter Change	Random failure	Resistance changes will cause the voltage division to be changed -> affecting the gain and therefore the output of the JFET	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.12.7	Sub-block - Fully diff. integrator	2.13e-8	100Ω Resistor - Open	Random failure	FDFC signal can't pass to the fully differential op amp in one of the polarity branches -> No measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.12.8			100pF Capacitor - Short	Random failure	FDFC signal will be drained to ground -> No measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.12.9			Fully differential amplifier - Open	Random failure	FDFC signal can't pass to the comparators nor the ADC -> No measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.13.1	Sub-block - Power supply for dig.pot	2.782e-8	Filtering capacitors - Short	Random failure	Supply voltage for the dig. pot. will be drained to Ground -> No functioning digital potentiometer	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.13.2			Levels converter - Open	Random failure	No supply voltage to the level converter that supplies the digital potentiometer -> No functioning digital potentiometer	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.13.3			Levels converter - Parameter Change	Random failure	Different voltage levels can cause the digital potentiometer to have incorrect supply voltage -> No functioning digital potentiometer	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.13.4			Levels converter - Short	Random failure	+5V can pass to the input of the digital potentiometer, causing it to malfunction -> No functioning potentiometer	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.14.1	Sub-block - Input voltage filtering	5.541e-9	1 uH Coil - Open	Random failure	+5 supply voltage can't pass to the input monitors	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.14.2			Filtering capacitors - Open	Random failure	+5 supply voltage can't pass to the input monitors	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.14.3			Filtering capacitors - Short	Random failure	+5V supply voltage is drained to Ground	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.15.1	Sub-block - Filter 6x capacitor	4.372e-8	Filter capacitors - Short Switch FDFC / DADC supply voltage	Random failure	Switch will be disabled, causing there to be no switching between the DADC and FDFC -> Wrong measurement method	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.15.2			Filter capacitors - Short Buffer amplifier supply voltage	Random failure	No supply voltage to the buffer amplifiers	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.16.1	Sub-block - Filter 4x capacitor	5.2e-8	Filter capacitors - Short Digital potentiometer supply voltage	Random failure	No 2.5V supply voltage to the digital potentiometer -> No functioning digital potentiometer	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.16.2			Filter capacitors - Short Saturation Monitor supply voltage	Random failure	Voltage to the saturation monitor is drained to Ground -> No saturation monitoring	Maintenance - Loss of protection	2	1	2	4	Maintenance fix. Not detectable, but not essential for safe operation.
1.1.2.16.3			Filter capacitors - Short Comparator supply voltage	Random failure	Comparators will not have their supply voltage -> No COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.16.4			Filter capacitors - Short Fully differential amplifier supply voltage	Random failure	Fully differential amplifier will not have a supply voltage -> No measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.17.1	Sub-block - Filter 2x capacitor	3.324e-8	Filter capacitors - Short Fully differential integrator supply voltage	Random failure	No supply voltage for the fully differential amplifier -> No measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.17.2			Filter capacitors - Short Flip flop supply voltage	Random failure	No supply voltage for the flip-flop -> Loss of flip-flop	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.2.1	Sub-block - Saturation monitoring	1.535e-8	100Ω Resistor - Open	Random failure	No stop signal can be sent to OR-gate from the comparator -> No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.10			470Ω Resistor - Open	Random failure	No reference voltage for saturation monitor -> No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.11			470Ω Resistor - Short	Random failure	No voltage divider -> Wrong input on the comparator -> Continuous fault condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.12			510Ω Resistor - Open	Random failure	No voltage can pass to saturation monitor -> No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.13			510Ω Resistor - Short	Random failure	No voltage divider -> Wrong input on the comparator -> Continuous fault condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.14			1uF Capacitor - Short	Random failure	Saturation monitor input voltage will be drained to Ground -> No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.15			Diode - Open	Random failure	No voltage can pass to saturation monitor -> No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.16			Diode - Short	Random failure	Short between the outputs on the fully differential op. amp -> No functioning DADC and FDFC	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.2			3,3k Resistor - Open	Random failure	No positive feedback -> No hysteresis -> No comparison threshold -> No stop signal on a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.3			Fully differential comparator - Short	Very low current levels in input	No comparator -> No saturation monitor -> Can't restore from a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.2.4	Sub-block - Saturation monitoring	1.535e-8	Fully differential comparator - Erroneous output and leakage	Random failure	Hysteresis will trigger a stop condition at the wrong threshold -> Continuous fault condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.5			Fully differential comparator - Open	Very low current levels in input	No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.6			10k Resistor - Open	Random failure	No voltage divider -> Wrong input on the comparator -> Continuous fault condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.7			10k Resistor - Short	Random failure	Saturation monitor input voltage will be drained to Ground -> No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.8			1k Resistor - Open	Random failure	No voltage divider -> Wrong input on the comparator -> Continuous fault condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.2.9			1k Resistor - Short	Random failure	Saturation monitor input voltage will be drained to Ground -> No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.3.1	Sub-block - Stop	1.096e-8	OR gate - Open	Random failure	No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.3.2			OR gate - Short	Random failure	Continuous stop signal to FPGA -> No operation of the Input Monitors	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.3.3			Filtering capacitors - Short	Random failure	No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.3.4			100Ω Resistor - Open	Random failure	No saturation monitor -> Can't restore a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.4.1	Sub-block - Switch FDFC / DADC to ADC	7.626e-10	1k Resistor - Short	Random failure	Output voltages from the double polarity integrator will negate each other -> Wrong signal out to ADC -> No DADC and FDFC function	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.4.2			FDFC to DADC switch - Open	Random failure	No signal from the double polarity integrator can pass to the ADC -> No DADC and FDFC function	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.4.3			FDFC to DADC switch - Short	Random failure	Short causes wrong voltages on the output of the switch -> No switching between DADC and FDFC	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.1	Sub-block - Buffer amplifier	5.498e-8	Op. Amp - Short	Very low current levels in input	No comparator -> No saturation monitor -> Can't restore from a faulty condition	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.10			Fully Differential Amplifier - Parameter Change	Random failure	Changes in the input bias voltage can cause there to be wrong measurements amplified -> Wrong signal sent to the ADC	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.11			Fully Differential Amplifier - Short	Random failure	Voltage passes through unchanged or changed wrongly -> Wrong measurement sent to ADC	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.12			24Ω Resistor - Open	Random failure	Signal can't pass through to one of the differential inputs on the ADC -> No ADC signal	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.13			Filtering capacitor - Short Vin	Random failure	Output signal from one of the differential outputs would be drained to Ground	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.14			Filtering capacitor - Short VOCM	Random failure	Short would cause the VOCM to be drained to Ground -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.2			Op. Amp - Parameter Change	Random failure	High input offset voltage -> Wrong measurements being sent to ADC	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.3			Op. Amp - Open	Random failure	No voltage can pass -> No signal to the ADC.	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.5.4	Sub-block - Buffer amplifier	5.498e-8	100Ω Resistor - Open Op. amp. output	Random failure	No signal from DADC or FDFC can pass to the ADC on one branch	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.5			100Ω Resistor - Open Diff. Amp. input	Random failure	No voltage can pass to Vin -> No amplification -> Signal will in stead go to ADC input directly	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.6			100Ω Resistor - Open Feedback	Random failure	Feedback can't be put to input -> No amplification -> Wrong signal sent to the ADC.	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.7			47pF Capacitor - Short Fully diff. amp	Random failure	Voltages on both inputs will be the same -> No differential output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.8			47pF Capacitor - Short Feedback loop	Random failure	Signal will also pass to the inverted output negating it partly -> Wrong signal being sent to the ADC	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.5.9			Fully Differential Amplifier - Open	Random failure	Signal can't pass through the amp to the ADC	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.6.1	Sub-block - Voltage reference generator	2.221e-8	Filtering capacitors - Short -5V	Random failure	-5V supply voltage will be drained to Ground -> No voltage reference for the fully. diff. comparators -> Erroneous threshold for the comparators -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.6.2			Linear regulator - Short	Random failure	-5V will pass to one of the differential inputs on the fully diff. comparators -> Erroneous threshold for comparators -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.6.3			Linear regulator - Parameter Change	Random failure	Change in output voltage will cause the threshold to be wrong -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.6.4			Linear regulator - Open	Random failure	No reference voltage can pass to one of the differential inputs of the comparators -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.6.5	Sub-block - Voltage reference generator	2.221e-8	Filtering - Short FB	Random failure	Output of the digital potentiometer is drained to Ground -> No control of voltage regulator output value -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.6.6			100Ω Resistor - Short A2	Random failure	Linear regulator output and thus comparator threshold will not be correct due to there being no calibration from the dig. pot. -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.6.7			Filtering capacitors - Short -2.5V	Random failure	Reference voltage will be drained to Ground -> No threshold in the comparators -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.1	Sub-block - Comparators	3.095e-8	Filter - Short + Input	Random failure	Reference voltage will be drained to Ground -> No threshold in the comparators -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.10			NAND - Open	Random failure	No status signal can be sent to the flip-flop -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.11			100Ω Resistor - Open	Random failure	No status signal can be sent to the flip-flop -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.12			1k Resistor - Short	Random failure	No status signal can be sent to the flip-flop -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.13			Filtering capacitors - Short	Random failure	No supply voltage to the NAND -> No signal sent to the flip-flop -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.2			Filter - Open + Input	Random failure	No reference voltage can pass to comparators -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.7.3	Sub-block - Comparators	3.095e-8	Comparator - Short	Random failure	Can cause either no output signal, or wrong output signal being transmitted to the COUNT outputs -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.4			Comparator - Parameter Change	Random failure	Value changes in the differential inputs will cause the output value to be incorrect -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.5			Comparator - Open	Random failure	No output can pass through -> No COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.6			100Ω Resistor - Open	Random failures	No voltage can pass to the negative differential input of the comparator -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.7			10k Resistor - Open	Random failure	Feedback is not sent to positive comparator input causing there to be no hysteresis and potential unwanted switching -> Wrong COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.8			270Ω Resistor - Open	Random failure	No comparator output signal can pass - No COUNT value	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.7.9			NAND - Short	Random failure	Short would cause either the COUNT outputs to be shorted, or the flip flop to give wrong turns	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.8.1	Sub-block - Flip-Flop	8.133e-9	Flip flop - Short	Random failure	Wrong signal can pass to the input switch -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.8.2			Flip flop - Open	Random failure	No signal can pass to the input switch from the flip flop -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.8.3			Flip flop - Erroneous state	Random failure	Wrong signal can pass to the input switch -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.8.4	Sub-block - Flip-Flop	8.133e-9	1k Resistor	Random failures	Causes the Preset and Clear to be continuously low -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.8.5			100Ω Resistor - Open Output	Random failure	No signal can pass to the input switch from the flip flop for one the outputs -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.8.6			N-channel MFET - Short	Random failure	Voltage will be drained to Ground, causing there to be continuous 0 or 1 depending if its PRESET or CLEAR -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.8.7			N-channel MFET - Open	Random failure	+5V used to set PRESET and CLEAR will be unable to go to Ground, causing the PRESET or CLEAR to be continuously high -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.8.8			N-channel MFET - Leakage	Random failure	Input signal from FPGA to PRE and CLR can either be drained to Ground or be passed to the +5V -> No PRESET or CLEAR -> No switching in branch -> Loss of differential integration	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.8.9			100Ω Resistor - Open FPGA PRE / CLR	Random failure	Input signal from FPGA to PRE and CLR can't pass one of the resistors	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.9.1	Sub-block - Offset current & det. input	9e-9	1G Resistor - Open	Random failure	No voltage out on W1, from Dig.Pot -> No offset current	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.2.9.2			1G Resistor - Short	Random failure	No current limiting from the voltage out on W1 -> Erroneous offset current	False dump - Loss of operation for 4 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.2.9.3			47Ω Resistor - Open	Random failure	Input monitoring signal can't pass -> No measurements -> Loss of detector	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.2.9.4	Sub-block - Offset current & det. input	9e-9	Input filter capacitors - Short	Random failure	Input monitoring signal can't pass -> No measurements -> Loss of detector	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.9.5			Input protection diode - Open	Random failure	Diode can not be used as input protection -> Overvoltages can damage system	Maintenance - Loss of protection	2	1	2	4	Maintenance fix. Requires a secondary fault to cause a problem. Not detectable, but non critical.
1.1.2.9.6			Input protection diode - Short	Random failure	Beam loss monitor measurements will be drained to Ground -> No measurements -> Loss of detector	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.9.7			3Ω Shunt - Open	Random failure	No current shunt level to the DADC and FDFC -> Erroneous measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.9.8			3Ω Shunt - Short	Random failure	No differential input to the DADC, and no shunt current measurements can be used in the FDFC -> Erroneous measurements	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.2.9.9			3Ω Shunt - Parameter Change	Random failure	Measured input signal levels sent to the DADC and FDFC will be erroneous Only if the value is drastically changed (over 10%).	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.1	Sub-block - ADC	7.656e-8	100nF Capacitor - Short	Random failure	Reference voltage for the ADC is drained to Ground -> No CNV range and no input being read -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.10			Rail-to-Rail I/O Amplifier - Input bias current VOCM	Very low current levels on input	Errors or failure will cause incorrect or no values to be sent to the FPGA -> Incorrect ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.11			Rail-to-Rail I/O Amplifier - Input offset voltage VOCM	Random failure	High input offset voltage will cause wrong measurements -> Wrong reference voltage -> Incorrect ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.12			10uF Capacitor - Short REF	Random failure	Reference voltage is drained to Ground -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.3.1.13	Sub-block - ADC	7.656e-8	10uF Capacitor - Open REF	Random failure	No low ESR, low ESL capacitor will cause wrong reference voltages -> Incorrect ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.14			10uF Capacitor - Short CAP1 & CAP2	Random failure	Lack of capacitor will cause failure to the ADC -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.15			10uF Capacitor - Open CAP1 & CAP2	Random failure	Reference voltage is drained to Ground -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.16			Filter capacitors VIO - Short	Random failure	I/O interface will not have 2.5V supply voltage causing no inputs or outputs -> No ADC outputs	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.17			Filter capacitors VDD2 - Short	Random failure	Lack of 2.5V power supply -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.18			Filter capacitor VDD1 - Short	Random failure	Lack of 5V power supply -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.19			Filter inductor - Open	Random failure	Lack of 2.5V power supply -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.2			Rail-to-Rail I/O Amplifier - Input bias current VREF	Very low current levels on input	Flows in internal impedances and produces unwanted voltages -> Shorts -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.3			Rail-to-Rail I/O Amplifier - Input offset voltage VREF	Random failure	High input offset voltage will cause wrong measurements -> Wrong reference voltage -> Incorrect ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.4			ADC - Erroneous or no output	No power signal or internal IC failure	Errors or failure will cause incorrect or no values to be sent to the FPGA -> Incorrect ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.5			100Ω Resistor - Short D	Random failure	No differential output is given due to short between the outputs -> Incorrect ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.3.1.6	Sub-block - ADC	7.656e-8	100Ω Resistor - Short DCO	Random failure	Positive and negative clock signal will be the same signal from the output of the ADC -> Incorrect ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.7			100Ω Resistor - Short CLK	Random failure	Positive and negative clock signal will be the same signal from the output of the ADC -> Incorrect ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.8			100Ω Resistor - Short CNV	Random failure	Wrong CNV edges will cause the voltage sample differences between IN+ and IN- to be measured incorrectly -> Incorrect ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.1.9			10k Resistor - Open	Random failure	En0 = 0 and En1 = 0 will cause the ADC to be in power-down mode -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.2.1	Sub-block - Voltage level converter	3.12e-8	Filter inductor - Open	Random failure	No +5V can pass, causing no +5V or +2.5V supply voltage -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.2.2			2200pF Capacitor - Open	Random failure	No +5V can pass, causing no +5V or +2.5V supply voltage -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.2.3			2200pF Capacitor - Short	Random failure	+5V drained to Ground, causing no +5V or +2.5V supply voltage -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.2.4			Filter capacitor 5V	Random failure	+5V drained to Ground, causing no +5V or +2.5V supply voltage -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.2.5			Linear regulator - Short	Random failure	5V will pass into the 2.5V inputs causing failure -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.2.6			Linear regulator - Open	Random failure	Lack of 2.5V power supply -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.2.7			10nF Capacitor - Short	Random failure	A short from the feedback to ground would cause the linear regulator to be unable to give an output -> No 2.5V supply -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.3.2.8	Sub-block - Voltage level converter	3.12e-8	Filter capacitor 2.5V	Random failure	+2.5V drained to Ground, causing no +2.5V supply voltage -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.3.1	Schematic block-1	2.444e-8	XFET voltage reference - Open	Random failure	No reference voltage can be generated for the ADC -> No reference voltage -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.3.2			XFET voltage reference - Short	Random failure	5V will pass through the XFET -> Wrong reference voltage -> Wrong ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.3.3.3			Filtering capacitors - Short	Random failure	No reference voltage -> No ADC output	False dump - Loss of operation for 1 BLM	3	1	1	3	Detectable, no special action is warranted.
1.1.4.1.1	Filters & Protection block-2	1.024e-7	Connector 26 pin - Open	Random failure	Lack of connection between the connector and the board will cause there to be either full or partly missing functionality -> No JTAG	Maintenance - No JTAG	2	1	1	2	Maintenance fix. JTAG is not essential for system safety. Detectable, no special action is warranted.
1.1.4.1.2			Connector 26 pin - Bad connection	Random failure	Lack of connection between the connector and the board will cause there to be either full or partly missing functionality -> No JTAG	Maintenance - No JTAG	2	1	1	2	Maintenance fix. JTAG is not essential for system safety. Detectable, no special action is warranted.
1.1.4.1.3			Connector 26 pin - Short	Random failure	A short will cause a connection between the JTAG I/O and/or the supply voltage -> No JTAG	Maintenance - No JTAG	2	1	1	2	Maintenance fix. JTAG is not essential for system safety. Detectable, no special action is warranted.
1.1.4.1.4			Fuse - Premature Open	Random failure	If the fuse opens it will cause there to be no input voltage to the JFET -> No JTAG	Maintenance - No JTAG	2	1	1	2	Maintenance checks.
1.1.4.1.5			ESD protection diode - Open	Random failure	No protection from ESD -> Lack of protection	Maintenance - Loss of protection	2	1	1	2	Maintenance fix. Opens up for ESD problems, but requires ESD to occur before it causes damage. Not detectable, but not essential for system safety. No special actions are warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.4.1.6	Filters & Protection block-2	1.024e-7	ESD protection diode - Short	Random failure	Testpoint voltage is drained to Ground -> No testpoint	Maintenance - No testpoints	2	1	2	4	Maintenance fix. Not essential for system safety. No special actions are warranted.
1.1.4.2.1	Filters & Protection block-3	5.038e-8	1k Chip Resistor - Open	Random failure	POS1 to POS4 can't be sent from the FPGA to the card connector -> Unable to give away position	Maintenance - No card positions	2	1	1	2	Maintenance - Non critical for operation
1.1.4.2.10			Backplane connector - Poor Contact or Intermittent Relay Status	Random failure	Bad connection through the connector from the backplane to the BLEDP card - Relay Status -> Inconsistent signal transferring -> Failure on bootup	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - Not implemented
1.1.4.2.11			Backplane connector - Poor Contact or Intermittent En_card	Random failure	Bad connection through the connector from the backplane to the BLEDP card - En_card -> Bad enable signal to card	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - Not implemented
1.1.4.2.12			Backplane connector - Poor Contact or Intermittent HV	Random failure	Bad connection through the connector from the backplane to the BLEDP card - HV -> Bad HV signal sent to backplane	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - Not implemented
1.1.4.2.13			Backplane connector - Poor Contact or Intermittent POS1 to POS4	Random failure	Bad connection through the connector from the backplane to the BLEDP card - POS1 to POS4 -> Bad positioning ID for the card	Maintenance - No card positions	2	1	1	2	False dump - Not implemented
1.1.4.2.14			Backplane connector - Poor Contact or Intermittent 48V input voltage	Random failure	Bad connection through the connector from the backplane to the BLEDP card - -> Non-continuous 48V to the card	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - No supply voltage to the BLEDP card. No special action warranted.
1.1.4.2.15			Coaxial connector - Open	Random failure	No connection to the backplane for the beam loss monitors -> No measurements from the beam loss monitors	False dump - Loss of operation for 1 BLM	3	1	1	3	False dump - Lack of a detector signal being sent through the BLEDP will cause a false dump / no beam permit. No special action warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.4.2.2	Filters & Protection block-3	5.038e-8	100nf Capacitor - Short	Random failure	POS1 to POS4 will be drained to Ground -> Unable to give away position	Maintenance - No card positions	2	1	1	2	Maintenance - Non critical for operation
1.1.4.2.3			Backplane connector - Open CMD_CH1 to CH8	Random failure	No connection through the connector from the backplane to the BLEDP card - CMD_CH1 to CH8 -> No signal sent to card on calibration mode	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - Not implemented
1.1.4.2.4			Backplane connector - Open Relay Status	Random failure	No connection through the connector from the backplane to the BLEDP card - Relay Status -> No signal to indicate Relay status	Maintenance - No relay status	2	1	1	2	False dump - Not implemented
1.1.4.2.5			Backplane connector - Open EN_card	Random failure	No connection through the connector from the backplane to the BLEDP card - EN_card -> No enable to card	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - Not implemented
1.1.4.2.6			Backplane connector - Open HV	Random failure	No connection through the connector from the backplane to the BLEDP card - HV -> No HV signal sent to backplane	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - Not implemented
1.1.4.2.7			Backplane connector - Open POS1 to POS4	Random failure	No connection through the connector from the backplane to the BLEDP card - POS1 to POS4 -> No positioning ID for the card	Maintenance - No card positions	2	1	1	2	Maintenance fix. Detectable and not essential for system safety. No special actions are warranted.
1.1.4.2.8			Backplane connector - Open 48V input voltage	Random failure	No connection through the connector from the backplane to the BLEDP card - 48V input voltage -> No 48V to the card	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - No supply voltage to the BLEDP card. No special action warranted.
1.1.4.2.9			Backplane connector - Poor Contact or Intermittent CMD_CH1 to CH8	Random failure	Bad connection through the connector from the backplane to the BLEDP card - CMD_CH1 to CH8 -> Bad signal sent to card on calibration mode	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - Not implemented



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.5.1.1	Sub-block - +48V Input voltage	6.458e-8	3.3k Resistor - Short	Random failure	DCDC enable will be drained to Ground -> Can't turn DC/DC 48V/5V converter on -> No 5V for the BLEDP	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.1.2			NPN-transistor - Open	Random failure	DCDC enable can't pass to DC/DC converter -> Can't turn DC/DC 48V/5V converter on -> No 5V for the BLEDP	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.1.3			NPN transistor - Short	Random failure	DCDC enable will either be drained to Ground -> Can't turn DC/DC 48V/5V converter on -> No 5V for the BLEDP DCDC enable will pass to DC/DC converter with no voltage division -> Incorrect enable voltage -> Can't turn DC/DC 48V/5V converter on -> No 5V for the BLEDP	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.1.4			DC/DC converter - Short	Random failure	DC/DC converter will have 48V output -> 48V in on the 5V supply line -> BLEDP shutdown 48V will be drained to Ground -> No 48V/5V conversion -> No 5V for BLEDP	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.1.5			DC/DC converter - Erroneous output	Random failure	DC/DC converter output gives out a wrong voltage -> Incorrect voltage in on 5V supply line -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.1.6			DC/DC converter - Open	Random failure	No 48V to 5V conversion can be made -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.1.7			Filtering capacitors - Short	Random failure	-5V and 5V will short -> No or wrong output	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.1.8			22uH Coil - Open	Random failure	5V will be unable to pass -> No 5V on output	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.5.2.1	Sub-block - 5V DC/DC	1.341e-6	2M Resistor - Short	Random failure	No voltage division for the gate voltage on the MOSFET -> MOSFET won't open -> No 48V input on DC/DC converter -> No 5V to BLEDP card -> BLEDP card shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.10			NPN-transistor - Open	Random failure	Enable can't be used to open the gate at the transistor -> No 48V/5V conversion -> No 5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.11			Filtering capacitors - Open DC/DC 5V	Random failure	Short between the negative and positive input on the DC/DC converter -> No 48V/5V conversion -> No 5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.12			Filtering capacitors - Open DC/DC 3.3V	Random failure	Short between the negative and positive input on the DC/DC converter -> No 48V/5V conversion -> No 5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.13			Coil - Open	Random failure	No 48V can pass to the DC/DC converter -> No 48V/5V conversion -> No 5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.2			2M Resistor - Open	Random failure	No voltage can pass to the gate on the MOSFET -> No 48V input on DC/DC converter -> No 5V to BLEDP card -> BLEDP card shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.3			100nF Capacitor - Short	Random failure	48V will pass to the gate on the MOSFET -> MOSFET won't open -> No 48V input on DC/DC converter -> No 5V to BLEDP card -> BLEDP card shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.5.2.4	Sub-block - 5V DC/DC	1.341e-6	MOSFET - Short	Random failure	MOSFET will have 48V on input -> MOSFET won't open -> No 48V/5V conversion -> No 5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.5			MOSFET - Open	Random failure	No 48V can pass to the DC/DC converter -> No 48V/5V conversion -> No 5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.6			10k Resistor - Open	Random failure	Enable can't be used to open the gate at the transistor -> No 48V/5V conversion -> No 5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.7			1uF Capacitor - Short	Random failure	Enable can't be used to open the gate at the transistor -> No 48V/5V conversion -> No 5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.8			10k Resistor - Short	Random failure	Enable can't be used to open the gate at the transistor -> No 48V/5V conversion -> No 5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.2.9			NPN-transistor - Short	Random failure	No voltage can pass to the gate on the MOSFET -> No 48V input on DC/DC converter -> No 5V to BLEDP card -> BLEDP card shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.3.1	Sub-block - 3.3V DC/DC	1.349e-6	Filtering capacitors - Short	Random failure	48V voltage will short with reference -> No 48V/3.3V conversion -> No 3.3V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.3.2			DC/DC converter - Short	Random failure	DC/DC converter will have 48V output -> 48V in on the 5V supply line -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.3.3			DC/DC converter - Erroneous output	Random failure	DC/DC converter output gives out a wrong voltage -> Incorrect voltage in on 5V supply line -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.5.3.4	Sub-block - 3.3V DC/DC	1.349e-6	DC/DC converter - Open	Random failure	No 48V/3.3V conversion -> No 3.3V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.3.5			Filtering capacitors - Short	Random failure	-3.3V and 3.3V will short -> No 3.3V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.3.6			22uH Coil - Open	Random failure	3.3V will be unable pass the coil -> No 3.3V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.4.1	Sub-block - Voltage converter	3.197e-8	Filtering capacitors - Short Voltage converter input	Random failure	3.3V will be drained to Ground -> No 3.3V/2.5V conversion -> No 2.5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.4.2			Voltage level converter - Short	Random failure	3.3V input voltage is drained to Ground -> No 3.3V/2.5V conversion -> No 2.5V to BLEDP card -> BLEDP shutdown 3.3V input voltage pass over the voltage level converter -> 3.3V on the 2.5V supply line -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.4.3			Voltage level converter - Erroneous output	Random failure	Wrong voltage level is converted -> No 2.5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.4.4			Voltage level converter - Open	Random failure	No 3.3V/2.5V conversion -> No 2.5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.4.5			Filtering capacitors - Short Output	Random failure	2.5V will be drained to Ground -> No 2.5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.4.6			22uH Coil - Open	Random failure	2.5V will be able to pass the coil -> No 2.5V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.5.5.1	Sub-block - Step down	7.288e-8	Filtering capacitors - Short Vin	Random failure	No voltage can pass to the Vin on the step down converter -> No 3.3V/1.2V conversion in the step down converter -> No 1.2V for the BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.10			Step down converter - Erroneous output	Random failure	Incorrect voltage on the 1.2V supply line -> FPGA won't function -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.11			Step down converter - Short	Random failure	3.3V will pass over the step down converter -> 3.3V on the 1.2V supply line -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.12			100nF Capacitor - Open	Random failure	Lack of a bootstrap capacitor between BOOT and PH -> Output will be switched off -> No 1.2V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.13			3.3uH Coil - Open	Random failure	Step down converter output voltage can't pass to the 1.2V supply line -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.14			100k Resistor - Open Vsense	Random failure	Lack of a Vsense -> COMP will be wrong because the internal voltage reference is wrong -> No 1.2V to the supply line -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.15			Filtering capacitors - Short	Random failure	Step down converter output will be drained to Ground -> No 1.2V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.16			22uH Coil - Open	Random failure	No voltage can pass from the step down converter to the circuit output -> No 1.2V to BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.2			100k Resistor - Open	Random failure	No enable for the step down converter -> No 3.3V/1.2V conversion -> No 1.2V for the BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.5.5.3	Sub-block - Step down	7.288e-8	100k Resistor - Short	Random failure	No voltage divider for the enable input on the step down converter -> No 3.3V/1.2V conversion -> No 1.2V for the BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.4			15nF Capacitor - Short Slow Start	Random failure	Lack of capacitor -> No slow start on the step down converter -> Unwanted inrush currents -> BLEDP circuit breakers clamping	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.5			390k Resistor - Open	Random failure	Switching frequency will be wrong -> Incorrect voltage level conversion -> No 1.2V for the BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.6			Frequency compensators - Open	Random failure	No frequency compensation -> Wrong switching thresholds -> Incorrect voltage level conversion -> No 1.2V for the BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.7			Frequency compensators - Short	Random failure	COMP voltage will be drained to Ground, causing there to be no error amplification -> No error detection -> Incorrect voltage level for the BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.8			100k Resistor - Open PWRGD	Random failure	No pull-up resistor for the PWRGD signal -> Floating output -> Potentially wrong diagnostics of step down converter status	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.5.5.9			Step down converter - Open	Random failure	No 3.3V/1.2V conversion -> No 1.2V for the BLEDP card -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.6.1.1	Sub-block: SFP connector	3.007e-6	Filter capacitors - Short	Random failure	Signal will be drained to Ground -> No signal can pass through the SFP connector -> No connection to the optical link	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.6.1.10			SFP connectors - Short	Random failure	Erroneous data will pass through to the optical link	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.6.1.2	Sub-block: SFP connector	3.007e-6	Filtering coils - Open	Random failure	Signal will be unable to pass to the SFP connector -> No connection to the optical link	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.6.1.3			10k Resistor - Open LOS	Random failures	SFP will not have a pull up resistor -> Can cause the LOS signal to be indicative of a below threshold signal -> No signal can pass through the SFP connector -> No connection to optical link	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.6.1.4			10k Resistor - Short LOS	Random failures	SFP will not have a pull up resistor -> Can cause the LOS signal to be indicative of a below threshold signal -> No signal can pass through the SFP connector -> No connection to optical link	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.6.1.5			10k Resistor - Open I2C	Random failures	No pull function for the I2C -> Can cause there to be erroneous outputs to the SFP connector -> Wrong data is sent over the optical link	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.6.1.6			10k Resistor - Open TX_FAULT	Random failures	SFP will not have a pull-up resistor -> Output signal will be floating -> Can indicate failure	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.6.1.7			10k Resistor - Open TX_FAULT	Random failures	SFP will not have a pull-up resistor -> Output signal will be floating -> Can indicate failure	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.6.1.8			SFP connectors - Open	Random failure	SFP signal will not be able to pass to the output -> Indicative of a failure	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.6.1.9			SFP connectors - Erroneous output	Random failure	Erroneous data will pass through to the optical link	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.7.1.1	Sub-block: Relay Activation	6.879e-8	1k Resistor - Open	Random failure	No activation signal can be sent from the FPGA to the BLEDP -> No "calibration mode" activated -> Failure on bootup	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - A lack of a command to set the BLEDP to calibration mode will cause the start algorithm to fail and thus remove beam permit. Only a problem in the start of a mission. Detectable, no special action warranted.
1.1.7.1.2			Diode - Open	Random failure	No clamping function for the calibration command -> No protection on input	Maintenance - Loss of protection	2	1	1	2	False dump - No clamping function can cause the signal to be out of range, which would damage the FPGA, or at least disable calibration. Detectable, no special action warranted.
1.1.7.1.3			Diode - Short	Random failure	3.3V passes through the diode and cancels out the relay signal -> No calibration -> Failure on bootup	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - A lack of a command to set the BLEDP to calibration mode will cause the start algorithm to fail and thus remove beam permit. Only a problem in the start of a mission. Detectable, no special action warranted.
1.1.7.1.4			100nF Capacitor - Short	Random failure	Activation signal to the BLEDP cards to get them activated in "calibration mode" will be drained to Ground -> Failure on bootup	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - A lack of a command to set the BLEDP to calibration mode will cause the start algorithm to fail and thus remove beam permit. Only a problem in the start of a mission. Detectable, no special action warranted.
1.1.7.2.1	Sub-system: Relay status	1.122e-8	100nF Capacitor - Short	Random failure	Relay status signal will be drained to Ground -> No relay status signal to indicate calibration mode -> Failure on bootup algorithm	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - A lack of a relay status signal to indicate the calibration mode of the BLEDP cards will cause the start algorithm to be broken and therefore no beam permit. Only a problem in the start of a mission. Detectable, no special action warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.7.2.2	Sub-system: Relay status	1.122e-8	10k Resistor - Open	Random failure	No relay status signal can be sent from the BLEDP to the FPGA -> Failure on bootup algorithm	False dump - Loss of operation for 8 BLM's	3	1	1	3	False dump - The lack of a relay status will cause the start up algorithm to be broken, and so no beam permit is given. Only a problem in the start of a mission. Detectable, no special action warranted.
1.1.7.2.3			Diode - Open	Random failure	No clamping function for the relay status signal -> No protection on relay status input	Maintenance - Loss of protection	2	1	1	2	False dump - The lack of a clamping can lead to a signal out of range being sent to the FPGA. Only a problem on the start of a mission. Detectable, no special action warranted.
1.1.7.2.4			Diode - Short	Random failure	3.3V passes through the diode and cancels out the relay status signal -> No relay status signal to indicate calibration mode -> Failure on bootup algorithm Relay activation signal will be drained to Ground -> No relay status signal to indicate calibration mode -> Failure on bootup	False dump - Loss of operation for 8 BLM's	3	1	1	3	
1.1.8.1.1	Sub-block: Serial Number Generator	1.021e-8	Serial Number Generator - Open	Random failure	Serial number generator can't generate a number sequence -> No serial number for the geo-location of the BLEDP cards	Maintenance - No card positions	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.1.2			Serial Number Generator - Erroneous output	Random failure	Serial number generator can't generate a valid number sequence -> No valid serial number for the geo-location of the BLEDP cards	Maintenance - No card positions	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.1.3			Serial Number Generator - Short	Random failure	No serial number generation - No geo-location of the BLEDP cards	Maintenance - No card positions	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.1.4			100uF Capacitor - Short	Random failure	Supply voltage for the serial number generator is drained to Ground -> No serial number for the geo-location of the BLEDP cards	Maintenance - No card positions	2	1	1	2	Solved in maintenance runs. Detectable.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.8.1.5	Sub-block: Serial Number Generator	1.021e-8	2k Resistor - Open	Random failure	Pull-up resistor will no longer work -> Possibility of floating output -> Wrong serial number generation for the geo-location of the BLEDP cards	Maintenance - No card positions	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.1.6			2k Resistor - Short	Random failure	3.3V will pass over the resistor -> Overvoltages on the output line of the sensor -> Erroneous signal is sent to the BLEAC	Maintenance - No card positions	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.2.1	Sub-block: Temp and humid. sensor	1.918e-9	SHT15 - Open	Random failure	Loss of temperature and humidity sensor -> No data is sent to the BLECU	Maintenance - No or incorrect temperature and humidity data	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.2.2			SHT15 - Erroneous output	Random failure	Erroneous outputs from the temperature sensor -> Wrong data is sent to the BLECU	Maintenance - No or incorrect temperature and humidity data	2	1	1	2	Solved in maintenance runs. Detectable if there are bigger temperature fluctuations.
1.1.8.2.3			SHT15 - Short	Random failure	3.3V will pass through the sensor and go directly to the BLECU -> Incorrect data retrieved by the BLECU 3.3V will pass through the sensor and go directly to Ground -> No data retrieved by the BLECU	Maintenance - No or incorrect temperature and humidity data	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.2.4			1k Resistor - Open	Random failure	Pull-up resistor will no longer work -> Possibility of floating output -> Wrong data is sent to the BLECU	Maintenance - No or incorrect temperature and humidity data	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.2.5			1k Resistor - Short	Random failure	3.3V will pass over the resistor -> Overvoltage on the output line of the sensor -> Erroneous signal is sent to the BLEAC	Maintenance - No or incorrect temperature and humidity data	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.3.1	Sub-block: ADC for housekeeping	3.519e-8	Filtering capacitors - Short Input		3.3V supply voltage and enable is drained to Ground -> No consistency check between the data in the PROM and the database -> Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.8.3.10	Sub-block: ADC for housekeeping	3.519e-8	10k Resistor - Short	Random failure	SCLK is drained to Ground -> No serial clock for accessing data and doing conversions in the ADC -> No ADC output value for consistency check -> Warning generated DIN is drained to Ground -> No data is written to ADC control register -> Wrong ADC output value for consistency check -> Warning generated ICS is drained to Ground -> No Chip Select means no framing of the serial data transfer -> Wrong ADC output value for consistency check -> Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.
1.1.8.3.11			Filtering capacitors - Short ADC VDD	Random failure	No voltage input for the ADC -> No consistency check -> Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.
1.1.8.3.2			Filtering capacitors - Short Output	Random failure	Vref is drained to ground -> No reference voltage level for the ADC -> No ADC for consistency check -> Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.
1.1.8.3.3			High Precision Voltage Reference - Open	Random failure	No vref is generated -> No reference voltage level for the ADC -> No ADC for consistency check -> Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.
1.1.8.3.4			High Precision Voltage Reference - Erroneous output	Random failure	Wrong vref is generated -> Wrong reference voltage level for the ADC -> No ADC for consistency check -> Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.
1.1.8.3.5			High Precision Voltage Reference - Short	Random failure	3.3V will pass to the vref -> Incorrect reference voltage to the ADC -> No ADC for consistency check -> Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
					3.3V will pass to Ground -> No vref is generated -> No ADC for consistency check -> Warning generated						
1.1.8.3.6	Sub-block: ADC for housekeeping	3.519e-8	8-bit ADC - Open	Random failure	No ADC for consistency check - Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.
1.1.8.3.7			8-bit ADC - Erroneous output	Random failure	Wrong ADC output -> Erroneous value for the consistency check - Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.
1.1.8.3.8			8-bit ADC - Short	Random failure	No or wrong value on ADC output -> No consistency check -> Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.
1.1.8.3.9			10k Resistor - Open	Random failure	No pull-down function can cause the SCLK to float -> Erroneous serial clock for accessing data and doing conversions in the ADC -> Wrong ADC output value for consistency check -> Warning generated No pull-down function can cause the DIN to float -> Data written to ADC control register is wrong -> Wrong ADC output value for consistency check -> Warning generated No pull-down function can cause the ICS to float -> No Chip Select means no framing of the serial data transfer -> Wrong ADC output value for consistency check -> Warning generated	Maintenance - No consistency check for PROM and database	2	1	1	2	No recovery after unexpected shutdown or watchdog triggering. Solved in maintenance runs. Detectable.
1.1.8.4.1	Sub-block: HV feedback	3.162e-8	51k Resistor - Short	Random failure	HV signal is drained to Ground -> No signal is sent to the ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.8.4.10	Sub-block: HV feedback	3.162e-8	Op. amp - Short	Random failure	Input signal is drained to Ground -> No HV value is generated Input signal will pass through -> Erroneous HV value is sent to the ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.11			100nF - Short Op. amp input voltages	Random failure	3.3V supply voltage is drained to Ground -> No operative op. amp -> No HV value is sent to ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.12			100nF - Short Op. amp REF	Random failure	1V reference voltage used to detect overvoltages is drained to Ground -> No HV value is sent to ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.13			100nF - Short Op. amp HV Value	Random failure	HV value signal on the op. amp. output is drained to Ground -> No data is sent to the ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.14			10k Resistor - Open	Random failure	HV value signal on the op. amp. output can't pass to the ADC -> No data is sent to the ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.15			100nF - Short Voltage reference generator	Random failure	3.3V supply voltage to the reference voltage generator is drained to Ground -> No voltage reference -> No HV value is sent to the ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.2			51k Resistor - Open	Random failure	No pull-up function for the HV input -> Floating input values to the Rail-to-Rail op. amp -> Potentially erroneous outputs	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.3			100nF Capacitor - Short		HV signal is drained to Ground -> No signal is sent to the ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.4			10k Resistor - Open		HV signal can't pass to the op. amp -> No HV signal output -> No signal sent to the ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.5			BAV199 - Open	Random failure	No overvoltage protection on op. amp. input	Maintenance - Loss of protection	2	1	1	2	No protection on input. Solved in maintenance runs. Detectable.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.8.4.6	Sub-block: HV feedback	3.162e-8	BAV199 - Short	Random failure	3.3V will pass to the HV signal, or the HV signal will be drained to Ground -> No signal sent to the ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.7			100nf Capacitor - Short	Random failure	HV signal is drained to Ground -> No signal is sent to the ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.8			Op. amp - Open	Random failure	No HV value can be generated -> No data sent to the ADC	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.8.4.9			Op. amp - Erroneous output	Random failure	HV signal output is wrong -> Loss of protection of overvoltages to the input interface	Maintenance - No or wrong HV Feedback value	2	1	1	2	Solved in maintenance runs. Detectable.
1.1.9.1.1	Sub-block - FPGA chip	1.524e-7	Single Event Upset		Loss of data -> Erroneous processing in FPGA -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.1.2			Single Event Functional Interrupt		Loss of data -> Erroneous processing in FPGA -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.1.3			Single Event Latch-up		Internal short in power lines -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.1.4			Single Event Gate Rupture		Destruction of the gate oxide in the presence of a high electric field -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.1.5			Single Event Burnout		Loss of FPGA due to a burn out -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.2.1	Sub-block - FPGA external memory	2.702e-7	EPC code chip - Open	Random failure	Chip won't be able to load code to the FPGA -> No FPGA working -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.2.2			EPC code chip - Erroneous output	Random failure	Error in code loaded to the FPGA -> FPGA will not work properly -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (B/BL)
FMEA Responsibility: Vegard Joa Moseng (B/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.9.2.3	Sub-block - FPGA external memory	2.702e-7	EPC code chip - Short	Random failure	Chip won't be able to load code to the FPGA -> No FPGA working -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.3.1	Sub-block - FPGA reset	1.176e-7	1000pF Capacitor - Short	Random failure	3.3V will be drained to Ground -> Voltage drops below threshold so !Reset is asserted -> BLEDP shutdown until voltage levels are OK	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.3.2			Programmable-Delay Supervisory Circuit - Short	Random failure	Voltage is below threshold so !Reset is asserted -> BLEDP shutdown until voltage levels are OK	Maintenance - No card positions	2	1	1	2	Maintenance fix. Detectable, no special action is warranted.
1.1.9.3.3			Programmable-Delay Supervisory Circuit - Erroneous output	Random failure	Inconsistent reset thresholds -> Lack of reset functionality	Maintenance - Inconsistent reset	2	1	1	2	Maintenance checks.
1.1.9.3.4			Programmable-Delay Supervisory Circuit - Open	Random failure	Permanent reset -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	2	3	Detectable, no special action is warranted.
1.1.9.3.5			10nF Capacitor - Short MR*	Random failure	Manual reset voltage will be drained to ground -> No manual reset	Maintenance - No manual reset	2	1	2	4	Maintenance checks.
1.1.9.3.6			10k Resistor - Short	Random failure	RESET does not have a pull-up resistor which helps attain voltages higher than VDD -> Reset will be on continuously -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.3.7			10k Resistor - Open	Random failure	RESET does not have a pull-up resistor which helps attain voltages higher than VDD -> Reset will be on continuously -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.3.8			100nF Capacitor - Short 3.3V supply voltage		3.3V supply voltage will be drained to Ground -> Permanent reset -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.



System: BLEAC
Sub-system: All
Circuit block: All
Design Responsibility: William Viganò (BI/BL)
FMEA Responsibility: Vegard Joa Moseng (BI/BL)

Failure mode and effects analysis

FMEA Number: 012
FMEA Date (Orig.): 27.02.2014
Date: 10.02.2014
Rev.: A

Failure mode ID	Sub-block	Sub-block failure rate	Failure mode	Causes for failure	Initial effect	End effects	Sev	Occ	Det	RPN	Recommended actions
1.1.9.4.1.1	Sub-block - 3.3V supply voltage	1.075e-7	Filtering capacitors - Short	Random failure	FPGA supply voltage is drained to Ground -> FPGA not operative -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.4.2.1	Sub-block - 2.5V supply voltage	6.06e-8	Filtering capacitors - Short	Random failure	FPGA supply voltage is drained to Ground -> FPGA not operative -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.4.3.1	Sub-block - 1.2V supply voltage	1.388e-7	Filtering capacitors - Short	Random failure	FPGA supply voltage is drained to Ground -> FPGA not operative -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.5.1	Sub-block - FPGA oscillator	7.291e-8	100nF Capacitor - Short	Random failure	2.5V supply voltage is drained to Ground -> No VDD for the crystal oscillator -> No clock for the FPGA -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.5.2			Crystal Oscillator - Short	Random failure	2.5V supply voltage is drained to Ground -> No VDD for the crystal oscillator -> No clock for the FPGA -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.5.3			Crystal Oscillator - EMI-induced failure	Random failure	Electromagnetic induction cause crystal oscillator to fail -> No clock for the FPGA -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.5.4			Crystal Oscillator - Open	Random failure	Loss of clock for the FPGA -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.5.5			10nF Capacitor - Open	Random failure	Clock can't pass the capacitor -> No clock for the FPGA -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.5.6			51ohm Resistor - Open	Random failure	Loss of pull-up resistor -> Inconsistent clock -> FPGA clock irregular -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.
1.1.9.5.7			51ohm Resistor - Open	Random failure	2.5V will pass to the clock transmission line -> Erroneous inputs on the FPGA clock input -> BLEDP shutdown	False dump - Loss of operation for 8 BLM's	3	1	1	3	Detectable, no special action is warranted.