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Evaluation of different readout systems with the FE-I4 based IBL stave

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List of used abbreviations

ATLAS	A Toroidal LHC ApparatuS
DAC	Digital Analog Converter
FE-I4	Front End I4
GR	Global Registers
IBL	Insertable B-Layer
ID	Inner Detector
LHC	Large Hadron Collider
PDR	Pixel Digital Region
RCE	Reconfigurable Cluster Element
ToT	Time over Threshold
YARR	Yet Another Rapid Readout

1. Introduction

The Large Hadron Collider (LHC) at CERN is probably the most well-known research project for high energy physics. It is the largest particle accelerator worldwide and used to study the properties of elementary particles and to search for new particles beyond the Standard Model in collision experiments.

One of the big detectors at the LHC is the ATLAS detector, whose purpose it is to measure the properties of the particles produced in a proton-proton collision as detailed as possible. One of the subsystems of the ATLAS detector is the Pixel detector, which is closest to the beam pipe where the collisions take place. The Pixel detector uses silicon sensors to detect charged particles. The charge signals produced by the sensors is processed by readout chips, which determine how much charge was deposited in the sensor. As this information is needed to determine the impulse of the detected particle, it is important to configure the chips properly so that a certain signal from a sensor leads to the same digital signal for all chips.

This tuning of the readout chips can be done with readout systems that are also used to read the data from the chips in an experimental run. This bachelor thesis deals with the tuning of the readout chip "FE-I4B" used in the innermost layer of the Pixel detector. Two different readout systems, YARR (Yet Another Rapid Readout) and RCE (Reconfigurable Cluster Element), are evaluated with regard to the FE-I4B tuning results.

Chapter 2 gives a more detailed overview about the ATLAS detector and the innermost detector layer of the Pixel detector, the Insertable B-Layer (IBL). A description of the structure and functions of the FE-I4B chips as well as a description of the tuning procedure are given in Chapter 3. The experimental setup and differences between the readout systems are described in Chapter 4 and the results of the tunings are discussed in Chapter 5.

2. Overview

2.1. The Large Hadron Collider

The LHC [1] is a part of CERN's acceleration complex and was put to operation in 2008. As the name suggests, the LHC accelerates protons or lead ions for high energy collision experiments. With its circumference of 27 km and maximum collision energy of 14 TeV for protons, it is the largest and most powerful accelerator worldwide.

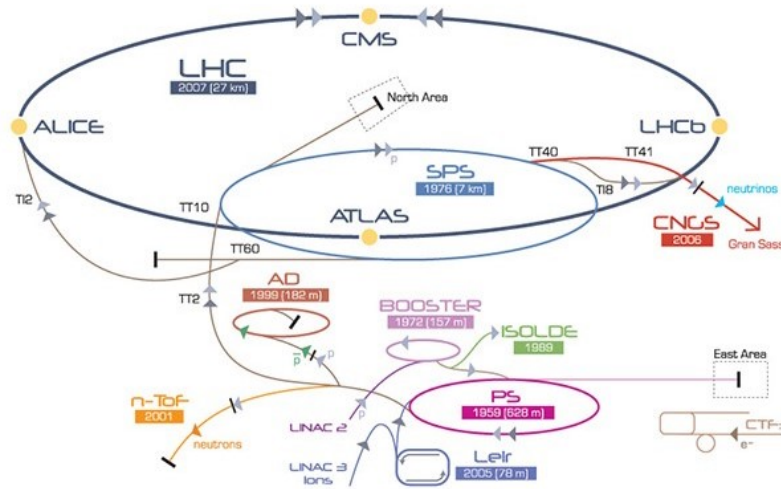


Figure 2.1.: Schematic representation of CERN's acceleration complex [2].

The LHC ring, shown in Figure 2.1 as a blue ring, consists of two beam pipes, in which counter-rotating particle beams are accelerated. Each beam consists of maximal 2556 [3] bunches, which travel at a distance of 25 ns. There are four collision points where the particle beams interact, which are represented by the yellow dots in Figure 2.1. The four big experiments, ALICE, ATLAS, CMS and LHCb are each located at one of the collision points.

ALICE (A Large Ion Collider Experiment) [4] measures lead ion collisions to study the properties of quark-gluon plasma. LHCb (Large Hadron Collider beauty) [5] focuses on interactions of particles which contain b-quarks to study the asymmetry between matter and antimatter in those interactions. ATLAS (A Toroidal LHC ApparatuS) [6] and CMS (Compact Muon Solenoid) [7] are general-purpose detectors, which study similar phenomena but differ in the technical detector design.

During the first period of data taking from 2010 to 2012, known as Run 1, the collaborations at LHC collected data at a proton-proton (pp) collision energy of 7 and 8 TeV. It was during this first operation period that ATLAS and CMS independently found evidence of the Higgs boson in their data. The LHC was shut down for two years and resumed data taking in 2015 with a pp collision energy of 13 TeV. This period of data taking, known as Run 2, will conclude in 2018. Afterwards, the LHC will be upgraded for Run 3 as an intermediate step on the way to the High-Luminosity

LHC (HL-LHC) project, which is scheduled to start in 2025. The current LHC was designed for a nominal luminosity of roughly $1.2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. This goal has been superseded by reaching regularly a luminosity of about $2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. HL-LHC is planned to run with a luminosity 5 to 7 times higher [8]. The upgrade for HL-LHC marks the ending of the "Phase 1" operation.

2.2. The ATLAS Experiment

The ATLAS detector [6] is one of the main particle detectors at the Large Hadron Collider at CERN. It measures pp collisions as well as heavy-ion collisions. The ATLAS detector was designed to search for the Standard Model Higgs boson but is not restricted to this task. The primary goal of finding the Higgs boson provided the framework of the detector design, as it demanded among others precise measurements of charged particle momenta, vertex identifications for flavour tagging and muon identification. The ATLAS experiment can also study Standard Model particles and search for beyond Standard Model physics in the TeV range.

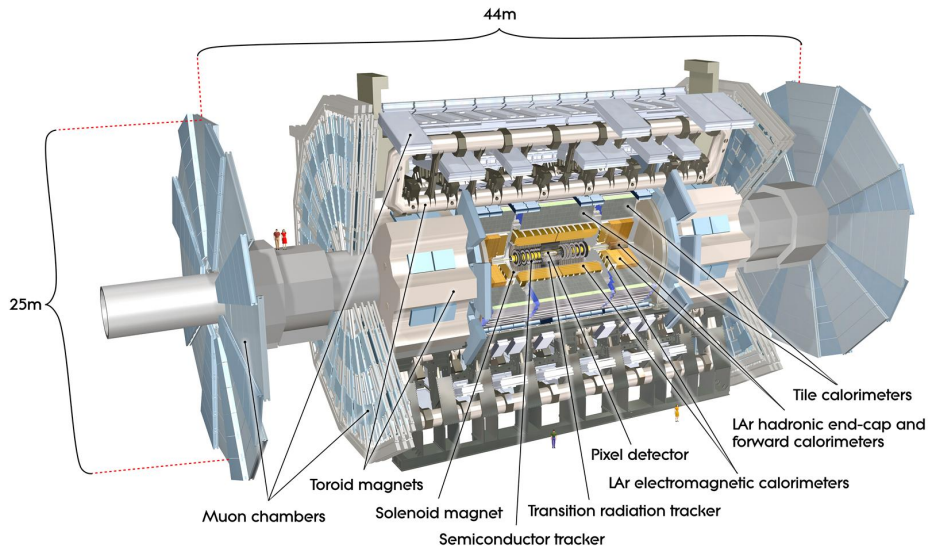


Figure 2.2.: Overview of the ATLAS detector [6]

The structure of the detector can be seen in Figure 2.2. Different detector layers are build around the beam pipe and can be divided in three main parts, the Inner Detector (ID), the calorimeters and the muon system.

The ID is a tracking system that contains three subdetectors, the Pixel detector, the Semiconductor tracker (SCT) and the Transition radiation tracker (TRT). Its purpose is to measure the momentum of charged particles and to detect the particle tracks in order to distinguish between primary and secondary vertices and to reconstruct the point of interaction. It is therefore immersed in a solenoidal magnetic field of 2 T, which deflects particles depending on their charge and momentum.

The ID is followed by the electromagnetic and hadronic calorimeters, which absorb and measure

the energy of electrons, photons and hadrons respectively. The muon spectrometer forms the outermost layer of the detector. It measures the muon tracks in a similar manner as the ID by deflecting the muons in a magnetic field produced by large superconducting toroid magnets.

2.3. The Insertable B-Layer

The Insertable B-Layer (IBL) [9] was added to the ATLAS detector during the first long shutdown of the LHC in 2013-2014 as an additional Pixel detector layer. The original Pixel detector was designed for a luminosity of $1 \times 10^{34} \text{ cm}^2 \text{ s}^{-1}$. The radiation damage occurring at higher luminosities, such as those reached in Run 2, causes inefficiencies in the tracking system.

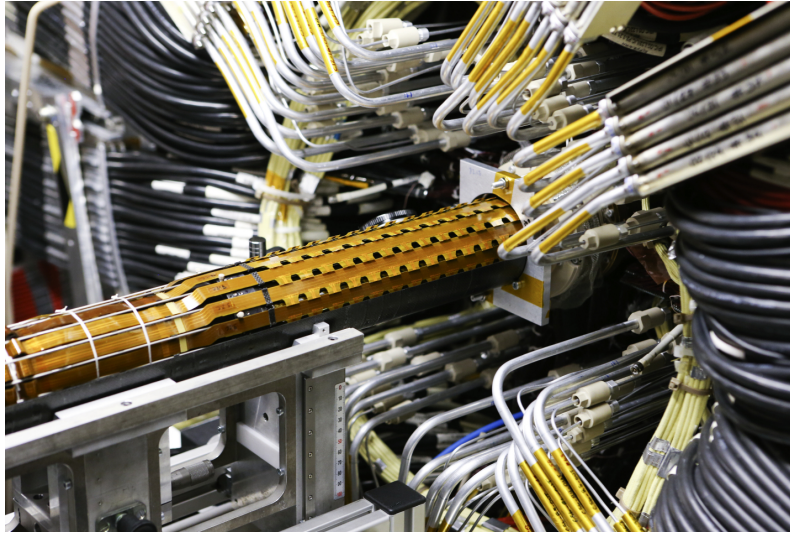


Figure 2.3.: Photography of the IBL being added to the ATLAS Pixel detector [10].

The IBL was installed between the original Pixel detector and a new smaller beam pipe to maintain a good tracking performance. Figure 2.3 shows how the IBL was inserted to the Pixel detector. It consists of 14 mechanical support structures referred to as staves, with each staff supporting 20 sensor modules together with the needed electrical services and cooling pipes.

A module consists of a silicon sensor and two readout chips called FE-I4B. Two different kinds of sensors are used, planar ones and 3D sensors. Consequentially, there are two kinds of modules. Planar modules consist of a planar sensor tile which is connected to two FE-I4B readout chips while 3D modules consist of two 3D sensor tiles each of which is connected to only one chip.

The planar sensor is an enhanced version of the ID's Pixel detector sensors. For example, the sensor's inactive edges have been reduced to increase the active area. The 3D sensor was newly developed for the IBL and is characterized by a high radiation hardness.

3. Components and Calibration of IBL Modules

3.1. The FE-I4B

The FE-I4B [11] is a readout chip designed for the IBL detector. In comparison to its predecessor, the FE-I3 used in the original Pixel detector, the FE-I4B has a higher radiation tolerance and better read-out efficiency at high luminosities. The size of the single pixels was also reduced from $50 \times 400 \mu\text{m}^2$ to $50 \times 250 \mu\text{m}^2$, effectively leading to a higher resolution for track reconstruction, specifically in the z-direction.

The FE-I4B contains 26880 pixels which are arranged in 80 columns and 336 rows. The columns are arranged in double column pairs, consisting of two analog columns with 336 pixels each and a digital double column in between, as shown in Figure 3.1.

As one can see in Figure 3.1, the double columns are further divided in 2×2 pixel regions, which means four analog pixels share one Pixel Digital Region (PDR).

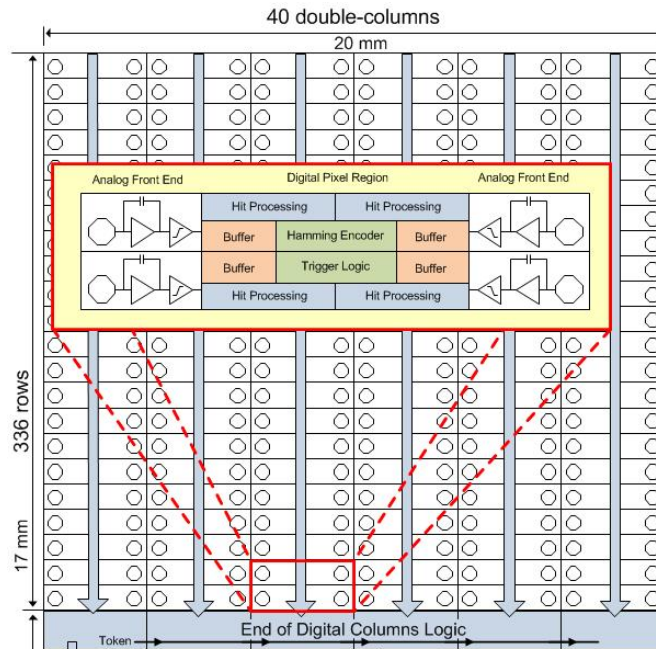


Figure 3.1.: Schematic representation of the FE-I4B layout. Each digital double column (blue) is embedded in two analog columns [11].

3.1.1. Analog Region

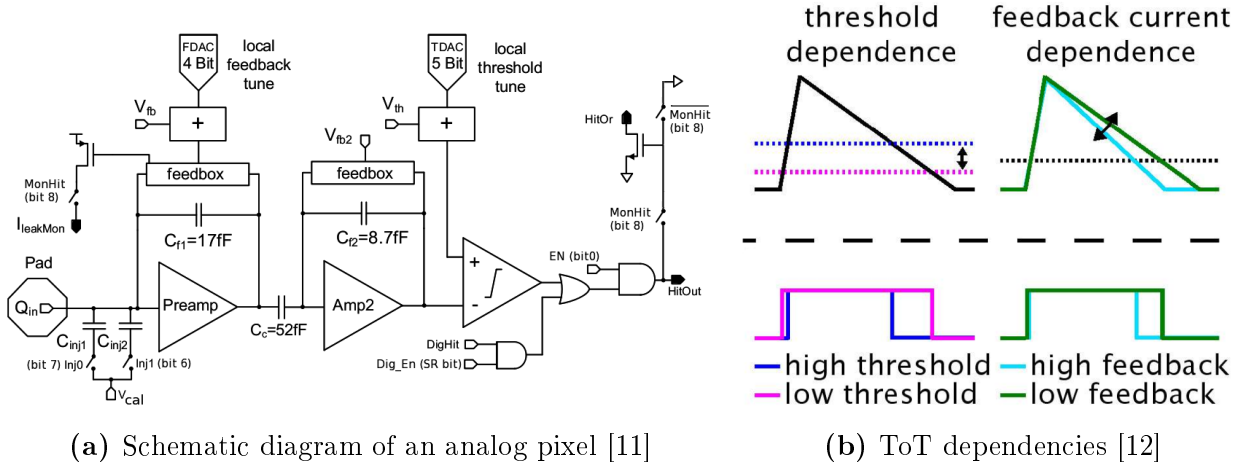


Figure 3.2.: Figure 3.2a shows a schematic diagram of an analog pixel. Figure 3.2b shows the changes in ToT depending on the threshold and feedback current.

The analog pixel contains two amplifiers, as shown in Figure 3.2a. The *Preamp* is used to alter the shape of the signal while the *Amp2*'s sole purpose is voltage amplification determined by the C_c/C_{f2} ratio. The V_{cal} input is used for analog calibration injections in an analog scan (cf. Section 3.2.2). This is done by switching the calibration voltage from baseline to ground level. The injection capacitors C_{inj1} and C_{inj2} translate the falling edge of the voltage in a negative charge injection.

When a negative charge, coming from the sensor connected at Q_{in} or from the calibration input V_{cal} respectively, is collected, the *Preamp* delivers a positive output pulse. The feedback current provided by the *feedback* adjusts the time needed to return to the baseline of the signal. Therefore, the *Fdac* register, which defines the feedback current, is used to adjust the Time over Threshold (ToT). The ToT describes the time the signal is higher than a certain threshold in units of 25 ns. The feedback current dependence of the ToT can be seen in Figure 3.2b. A high feedback current results in a steep falling edge of the signal and hence in a small ToT.

After being amplified by the *Amp2*, the signal is given to a comparator, whose threshold can be adjusted with the *Tdac* register. This threshold determines how strong a signal needs to be to be counted as a hit. Therefore, a high *Tdac* value leads to a high threshold. It can be seen in Figure 3.2b that a higher threshold results in a shorter ToT. The comparator output is passed on to the digital region described in the following.

3.1.2. Digital Region

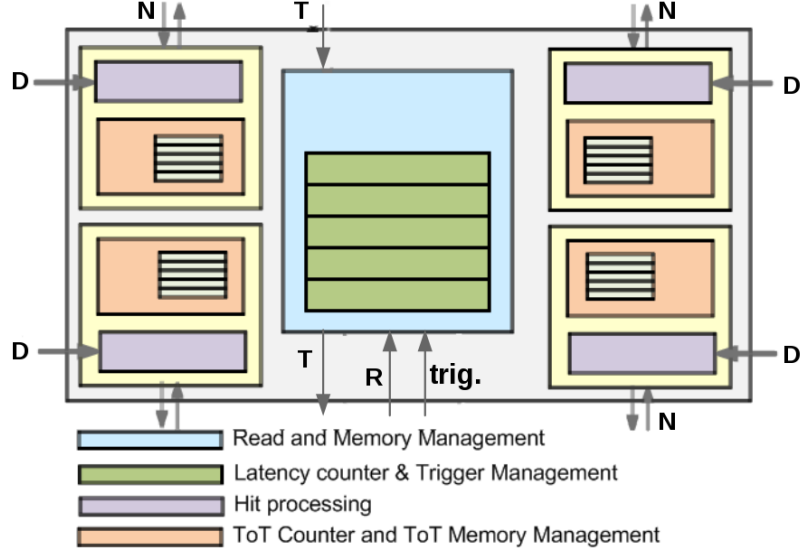


Figure 3.3.: Schematic diagram of the Pixel Digital Region [11].

A Pixel Digital Region (PDR) is shared by four analog pixels and works with a 40 MHz clock. This is the reason why the ToT is measured in units of 25 ns, which is the duration of one clock cycle. The discriminator input from the analog pixels is marked with a D in Figure 3.3. There is a 4-bit binary counter for each analog signal, so the ToT is measured individually for each analog pixel. The latency counter and trigger management are PDR specific, which means that the timestamp of a recorded event always belongs to the digital region.

There are 5 latency counters in the PDR, which means that up to 5 events can be stored temporarily. The ToT values of all 4 analog regions associated with the time of the hit arrival are stored in the ToT memory.

Once a counter is activated, the next one can be started in the next clock cycle. This means that the PDR has no own dead time and can record a hit that was detected from a second analog region while the first one is still counting the ToT of the previous event. The analog pixels of course have a dead time, as they cannot record a hit while their discriminator output is still high from a previous one. If a second hit arrives during that time, the ToT of the pixel is prolonged, which means that the second hit leads to a distortion of the signal of the first hit.

3.1.3. Chip Configuration

The configuration of the FE-I4B is stored in a master memory bank, called global registers (GR). The configuration parameters stored in the GR are needed to initialize the chip, to set analog biases and digital values and to control the different functions of the chip. For example, the V_{cal} input for analog calibration injections mentioned in Section 3.1.1 can be changed via the 'PlsrDAC'

register entry.

The configuration parameters are listed in a configuration file, whose format differs for the different readout systems. The configuration file always includes values for each GR entry and for the pixel specific configurations, such as the Fdac and Tdac described in Section 3.1.1. The tuning procedure described in Section 3.2 alters those parameters that regulate the threshold and ToT of the chip.

3.2. The Tuning Procedure

A tuning of a front end chip alters special configuration parameters to get a certain response from the chip. A minimum ionizing particle is expected to deposit on average $16000 e^-$ in the sensor connected to the chip and to result in a signal that stays over a threshold of $3000 e^-$ for about 250 ns, which equals a ToT value of 10 [13]. Therefore, the chips are usually tuned such that each pixel returns a ToT of 10 for an injected charge of $16000 e^-$ and a signal threshold of $3000 e^-$.

The tuning procedure of the FE-I4B is divided in different scans which are described in the following. The figures used in this section are taken from a tuning with YARR. This was done for the sake of clarity only. The described procedures are kept general and are applicable to both, RCE and YARR.

3.2.1. Mask Staging

The digital and analog signals are never injected to all pixels at the same time, as the injection circuit of the FE-I4B is not able to do so. Therefore, every scan has a mask staging process, which determines which pixels are to be enabled in which step. The mask staging could for example enable every 16th pixel in every column, which means that there would be 16 mask steps per scan to cover the whole chip.

Out of the enabled pixels the "double column loop" chooses double columns in which the signal gets injected at the same time. The double column loop could select every 4th double column, which would result in 420 pixels being scanned at the same time. The exact number of pixels enabled per mask stage depends on the readout system and the scan type but has no influence on the scan result.

3.2.2. Digital- and Analog Scan

A digital scan tests the response of the PDR. Therefore, the discriminator threshold is set to the maximum to exclude the analog region and an emulated signal is injected to the digital region multiple times. For a decent front end chip it is to be expected that all pixels see all injections. Pixels that do not count exactly as many hits as injected are disabled for the following scans.

An analog scan tests the response of the analog pixel region and is usually done right after a digital scan. A high charge is injected to the analog region multiple times and the number of reported hits is counted. In combination with the results of the digital scan it is possible to identify pixels with a failing analog region. Those pixels show a good response in the digital scan but have a low occupancy in the analog scan. Even for good quality FE-I4Bs it is common to observe a few pixels with a failing analog region.

The results of digital and analog scans are presented in form of an occupancy map as shown in Figure 3.4. Every cell in the map stands for one pixel of the FE-I4 chip and the colour indicates how many hits the pixel recorded. The blue cells in Figure 3.4b show dead pixels as they did not see any hits.

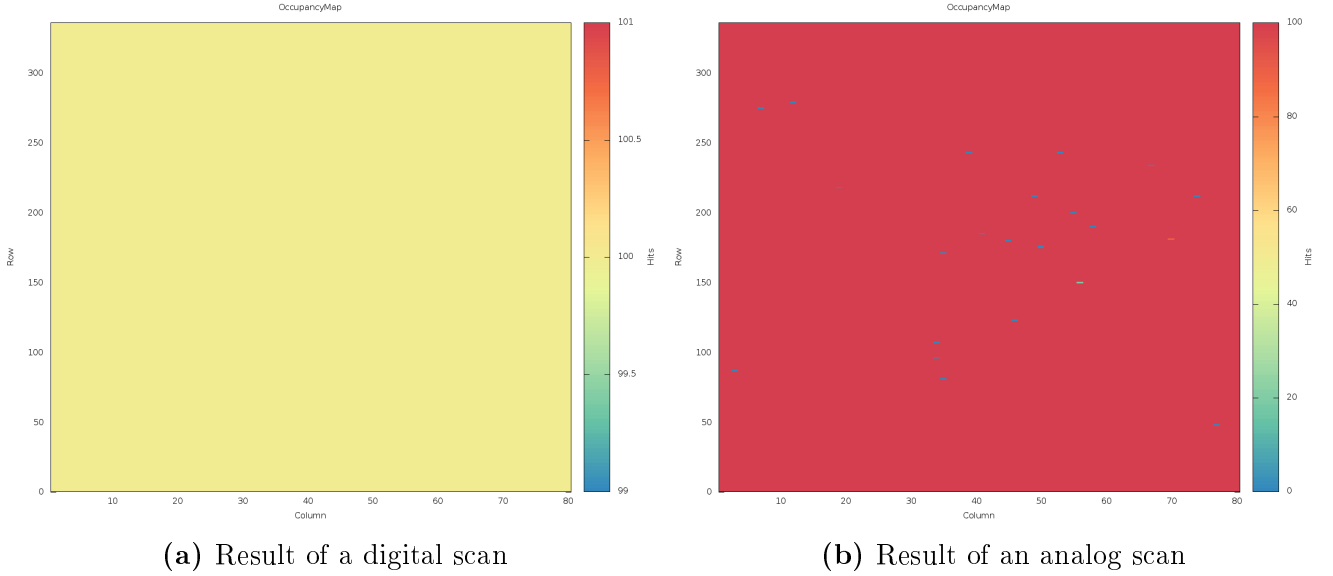


Figure 3.4.: Typical results of a digital scan and an analog scan with a FE-I4B chip. For both scans, 100 hits were injected.

3.2.3. ToT Scan

A ToT scan works similar to an analog scan, but it is used to test the *Preamp* setting (cf. Section 3.1.1). The defined target charge is injected multiple times in the analog region and the output signal is analysed with regard to the ToT of each pixel. An untuned chip usually shows a wide ToT distribution. As the result displayed by the readout systems is averaged over all injections, it is possible to get a non-integer ToT value, although the ToT is always an integer, giving the time in units of clock cycles. The readout systems also return the ToT sigma of each pixel, which is a scale for the stability of the pixel, as a high sigma indicates high fluctuations in the ToT response of a pixel.

3.2.4. Threshold Scan

A threshold scan consists of a series of analog scans with increasing injection charges. A pixel can only record a hit when the injected charge is above its threshold. The occupancy is measured for every charge, resulting in an "S-curve" for every pixel as seen in Figure 3.5. The pixel threshold is defined as the mean value of the S-curve, which is determined by fitting an error function to the curve.

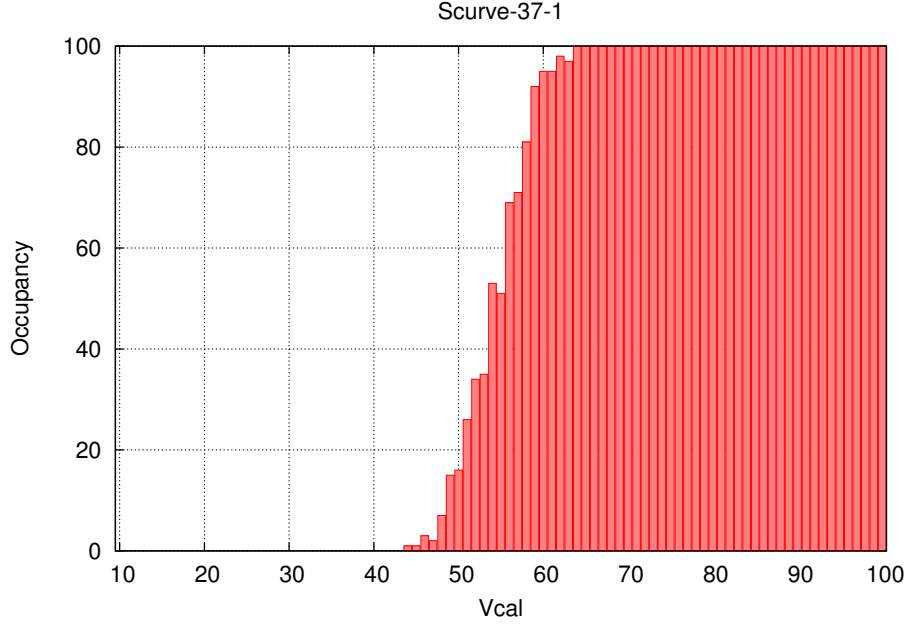


Figure 3.5.: Figure of an S-curve. The occupancy is plotted against the V_{cal} parameter.

As described in Section 3.1.1, the charge is injected by setting the V_{cal} voltage from baseline to ground. A higher baseline results in a steeper falling edge and in a higher injected charge. Therefore, the occupancy is plotted against V_{cal} in Figure 3.5.

The conversion of the V_{cal} voltage to the injected charge depends on which injection capacitor is used and is done automatically by the readout systems. The user specifies the wanted injection charge in e^- and the readout systems set the value of V_{cal} accordingly.

3.2.5. ToT Tuning

The ToT tuning procedure is split in two parts, the global and the pixel tuning. The global ToT value is defined by the configuration parameter 'PrmpVbpf', which regulates the feedback current of the *Preamp* amplifier for the whole chip. The parameter is an 8-bit variable and can therefore take on values between 0 and 255. A high value results in a short ToT (cf. Section 3.1.1). The global tuning sets the 'PrmpVbpf' parameter to the value that results in a mean ToT closest to the target value.

The pixel ToT tuning alters the in-pixel feedback current regulator, which is configured by the Fdac parameter. The Fdac has 4 bits and is stored for every pixel individually. The pixel ToT tuning sets the Fdac to the value that results in the desired ToT response of the respective pixel. After the global ToT tuning, the ToT of the front end chip should be calibrated to the target value with a rather large dispersion. The pixel ToT tuning does the fine tuning per pixel, so that the mean ToT distribution shows a clear focus on the integer target ToT value.

3.2.6. Threshold Tuning

The threshold tuning contains a global and a pixel specific tuning, similar to the ToT tuning. In both tunings, the target threshold is injected as charge and the occupancy is measured. The global threshold tuning alters the configuration parameter 'Vthin_fine' until the mean occupancy of the front end chip is as close to 50% as possible. This is done because an occupancy of 50% for a single pixel indicates that the mean value of the S-curve is centred on the target threshold. A higher occupancy indicates a threshold too low and a lower occupancy is a sign for a threshold too high. 'Vthin_fine' is an 8-bit variable and a higher value results in a higher threshold, although the scaling is non-linear [11].

As the occupancy is measured for each pixel individually, the occupancy of the whole chip can be displayed as a histogram only. After a successful global tuning, the occupancy should show a valley-like distribution as shown in Figure 3.6a because most pixels should have a threshold a little bit higher or lower than the target value.

The pixel specific threshold tuning is done with the Tdac register. For each pixel, a 5-bit Tdac value is tuned in the same way as for the global threshold tuning, by injecting the target charge and measuring the occupancy. After a successful pixel threshold tuning, the threshold of each pixel should be set to the target value which means that the occupancy distribution of the whole chip is centred around 50% as shown in Figure 3.6b.

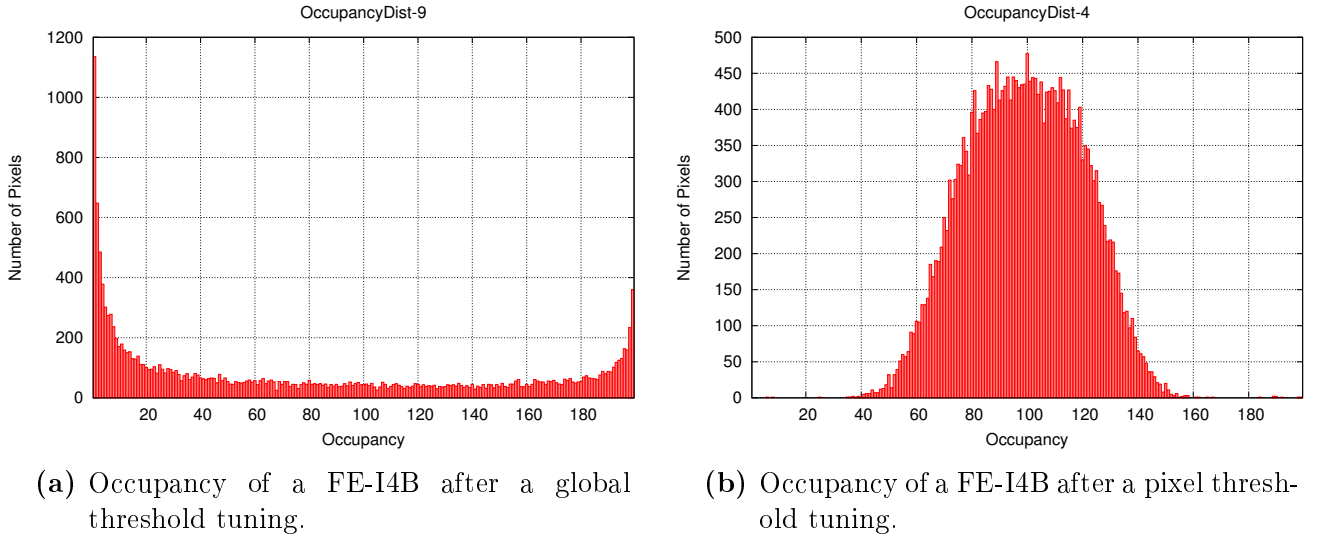


Figure 3.6.: Occupancy distributions of a FE-I4B after a global and after a pixel threshold tuning. 200 hits are injected in every pixel for both tunings, which means that an occupancy of 100 hits equals an occupancy of 50%.

4. Setup

4.1. The Stave

The measurements were done with an IBL stave that is not suitable for usage in the IBL as some modules are damaged. The stave is placed in a cooling box which is cooled down to 15°C with a water cooling. The chips themselves usually reach temperatures between 18°C and 20°C during operation but the temperature can go up to about 22°C on hot days as the box is not sealed perfectly and therefore influenced by the environmental temperature. The stave is divided in two halves, the A-side and the C-side, referring to the position of the according modules relative to the nominal interaction point in the center of the detector. There is no difference between the FE-I4Bs on the A-side and the C-side, therefore the position of a chip on the stave is used only to specify which chip was used for which measurement. A photography of the front end chips can be seen in Figure 4.1.

The tunings were done on the C-side of the stave with the first two module groups (M1 and M2). Module groups consist of two modules each and regulate the low voltage and high voltage supply of the respective modules.

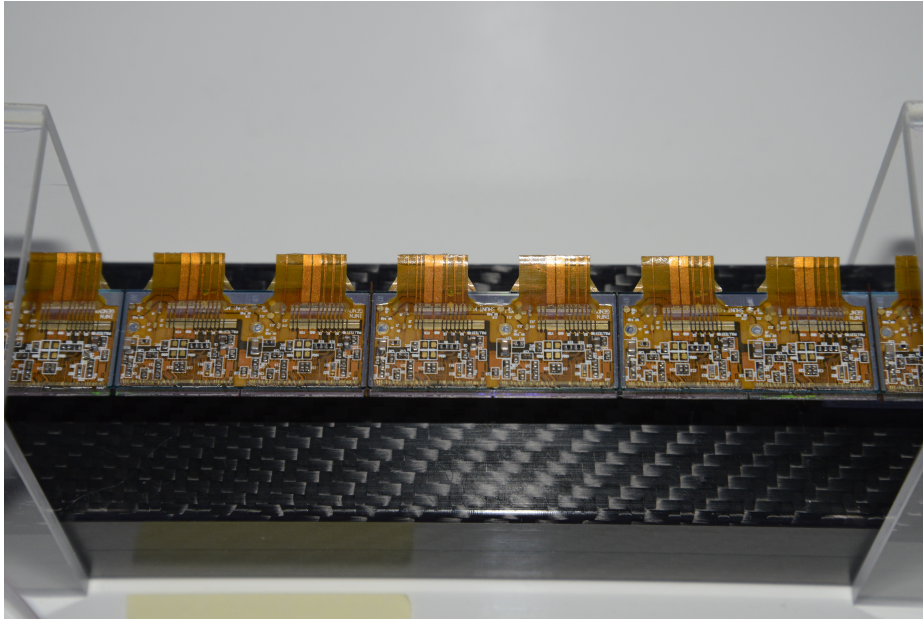


Figure 4.1.: Photography of a section of the IBL stave. The orange circuit board is a module flex with two FE-I4Bs mounted on top. Two chips are connected to one sensor tile on the bottom of the chips.

Table 4.1.: Overview of the used front end chips and ratings of the used modules.

FE-I4B	used	Module group	Module rating
C1-1	✓	M1	severe
C1-2	×		
C2-1	×		IBL
C2-2	×		
C3-1	✓	M2	IBL
C3-2	×		
C4-1	✓		IBL
C4-2	×		

Each side contains four module groups. The third module group (M3) of the C-side consumed too much power when connected to a high voltage source and the fourth module group (M4) provides 3D sensors, therefore the tunings were done with the first two module groups only. Before the actual tunings, digital and analog scans were done with RCE to check the response of the front end chips. Most chips occasionally returned failed digital scans and were not used for the tunings.

4.2. Tuning Procedure

For the tunings with RCE the same configuration file was used as starting point for all chips during all tunings. The configuration file was taken from earlier scans with the stave. All parameters which have a suggested value given in the FE-I4 Guide [11] were set accordingly. For the other parameters, the value present in the configuration file was used.

The same file was also used for tunings with YARR, but because the C1-1 chip showed analog issues (cf. Section 5.2.1) there were also tunings done with the YARR default configuration file. An overview of important configuration parameters and their values is given in Table A.1. After each tuning, five ToT scans and five threshold scans were made to get a better average value. Each scan averages the final outcome over 100 injections, which means that the results presented in Chapter 5 are averaged over 500 measurements each.

4.3. Differences between YARR and RCE

The tuning procedure for RCE is organized such that the global parameters get tuned before the pixel tuning starts [14]. At the beginning, the Fdacs are set to 7 and the Tdacs are set to 14. The tunings for the global threshold and ToT are repeated until the parameters do not change anymore. Then the tunings of the Fdac and Tdac values are done repeatedly until the mean value and dispersion of threshold and ToT remain the same.

YARR does one pixel threshold tuning before the final global ToT tuning and ends with a pixel threshold tuning instead of a pixel ToT tuning [15]. It also starts with all Fdacs set to 8 and all Tdacs set to 16. However, as the Fdacs can take on values between 0 and 15 and the Tdacs have values between 0 and 31, both readout systems start with Fdac and Tdac values in the middle of

the possible range. The tuning processes are presented in Table 4.2.

The scans with RCE were done with the "calibGUI", a graphical user interface which is used to load the chip configuration files and to select the target values and the scan. The scans with YARR were done with a command line interface and a tuning script, which calls the individual scans of a tuning procedure shown in Table 4.2 in the right order.

Table 4.2.: Overview of the tuning procedures of YARR and RCE. In the YARR procedure, each tuning is done once while the global and pixel tunings are done multiple times in the RCE procedure.

YARR	RCE
digital scan	digital scan
analog scan	analog scan
global threshold tuning	global threshold tuning
global ToT tuning	global ToT tuning
pixel threshold tuning	pixel threshold tuning
global ToT tuning	pixel ToT tuning
pixel ToT tuning	
pixel threshold tuning	

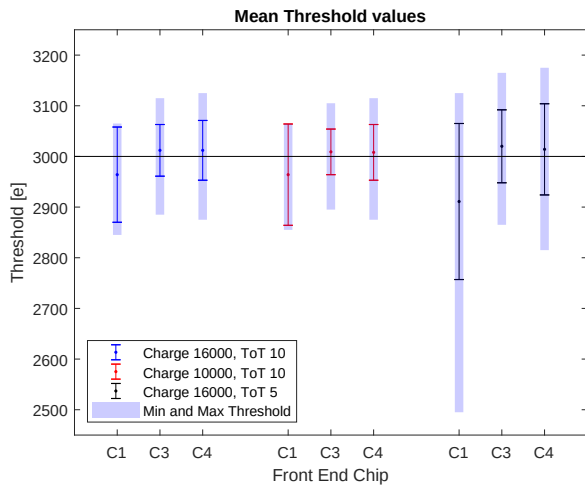
5. Results

The front end chips C1-1, C3-1 and C4-1 were tuned to different target values using RCE and YARR respectively. The results of the tunings are discussed in the following sections. In Section 5.1 and Section 5.2 the results of the tunings with RCE and YARR are analysed with special regards to those tunings that did not return the expected results. In Section 5.3 the results are compared to each other and the results of scans are presented that were done with one readout system using the tuned configuration file delivered by the other system. Section 5.4 finally shows the result of a source scan done with the front end chip C3-1 and a radioactive Sr-source.

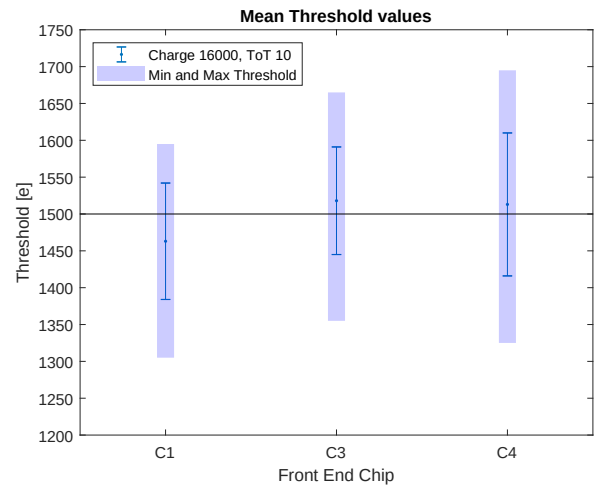
5.1. RCE

Threshold

The threshold tunings with RCE show consistent results. As one can see in Figure 5.1, the mean thresholds of the C3-1 and C4-1 chips are slightly too high in all tunes while the threshold of C1-1 is too low in all three cases. As this result is seen for all four tunings, one can assume that the larger deviation of the C1-1 chip is a chip specific issue. The global configuration parameters listed in Table A.2 also confirm this explanation, as the C3-1 and C4-1 chip ended up with exactly the same parameters for each tuning while C1-1 got higher values for the parameters.



(a) Mean threshold values after tunings with a target threshold of $3000 e^-$



(b) Mean threshold values after a tuning with a target threshold of $1500 e^-$

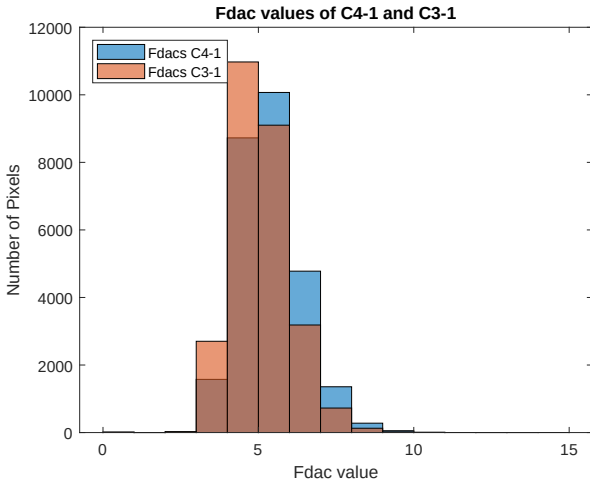
Figure 5.1.: Mean threshold values of the chips C1-1, C3-1 and C4-1 after tunings. The errorbars show the standard deviation while the boxes show the minimal and maximal value. The minimum and maximum are defined as the middle of the first and last bin in which at least 0.1% of all pixels are sorted.

As exemplarily shown in Figure 5.2 and Figure 5.3, the Fdac and Tdac settings for the C3-1 and C4-1 chips are also similar. Some differences are to be expected, as the tuning results are influenced by electronic noise, but it can be said that RCE reached very similar configurations for both chips.

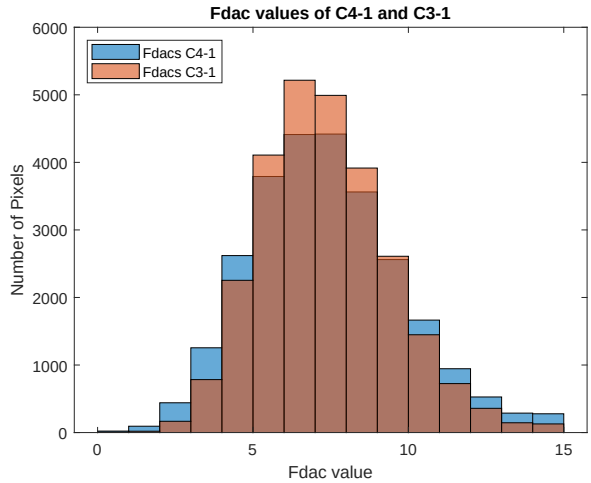
A possible explanation for the different result of the C1-1 chip is the condition of the module. The module of the chips C3-1 and C4-1 was rated IBL suitable while the module of the C1-1 chip was rated severe. It is possible that damages on the sensor influence the tuning, as the pixels of the sensor act as capacitors on the charge injection area of the analog circuit.

Another explanation for the result of the threshold tuning could be a problem with the threshold tuning itself. Therefore, a closer look was taken on the Tdac settings of the individual pixels. A higher Tdac value results in a higher threshold, therefore a correlation between a low Tdac value and a low threshold value is to be expected.

From Figure 5.4 it can be seen that the right half of the chip ended up with a higher Tdac setting but not with a higher deviation from the target threshold. Therefore, the high deviation is most likely not an issue within the threshold tuning as the deviation does not follow the pattern of the Tdac values. The most likely explanation is the electronic noise of the sensor connected to the chip. As mentioned above, the module of the chip was rated severe, which is a possible reason for the higher deviation seen for the C1-1 chip.

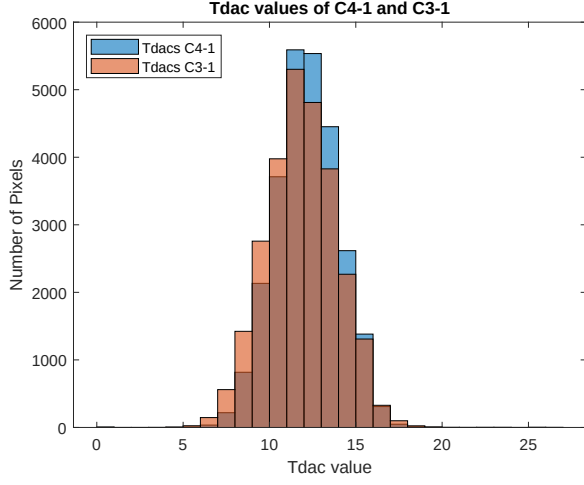


(a) Fdac values of C3-1 and C4-1 after a tuning to a ToT of 10

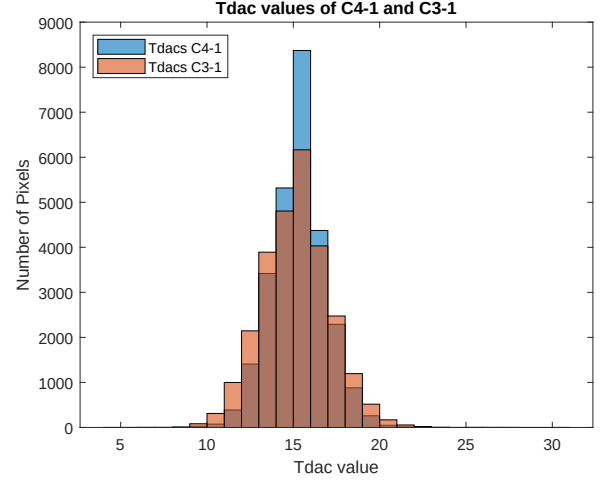


(b) Fdac values of C3-1 and C4-1 after a tuning to a ToT of 5

Figure 5.2.: Fdac values of C3-1 and C4-1 after tunings with different target ToTs. The target threshold was $3000 e^-$ and the injected charge $16000 e^-$ for all tunings.

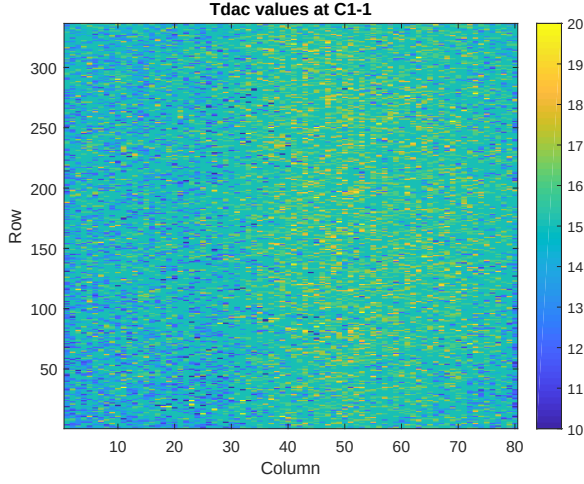


(a) Tdac values of C3-1 and C4-1 after a tuning to a ToT of 10

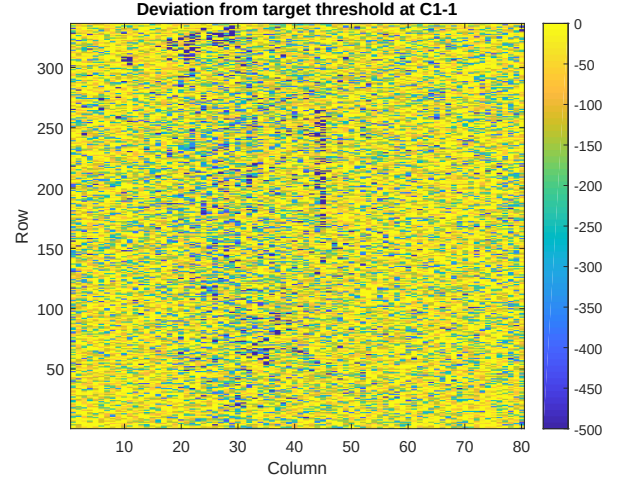


(b) Tdac values of C3-1 and C4-1 after a tuning to a ToT of 5

Figure 5.3.: Tdac values of C3-1 and C4-1 after tunings with different target ToTs. The target threshold was $3000 e^-$ and the injected charge $16000 e^-$ for all tunings.



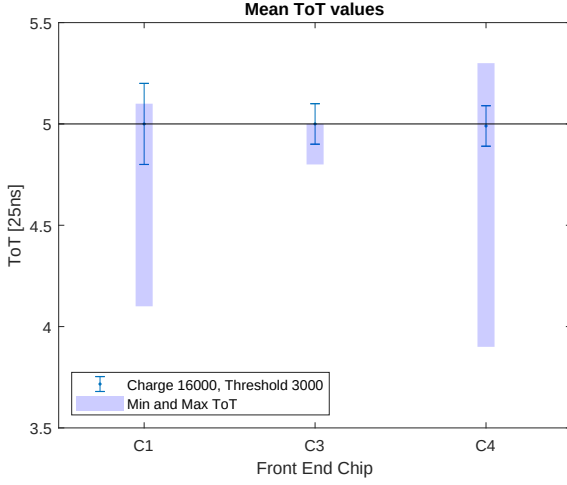
(a) Tdac setting at C1-1



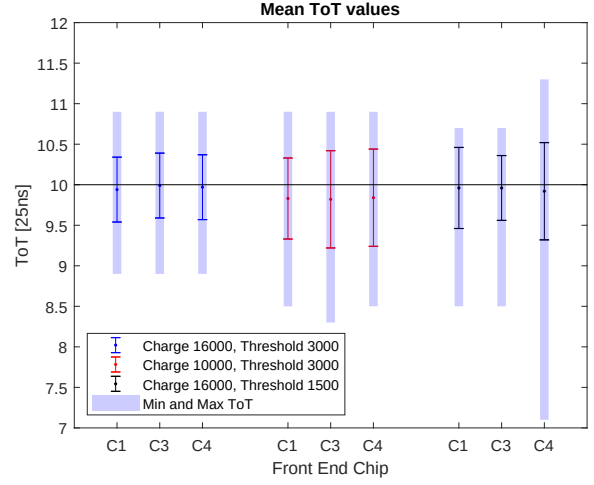
(b) Deviation from the target threshold at C1-1

Figure 5.4.: Figure 5.4a shows the Tdac setting of the C1-1 chip after a tuning to a threshold of $3000 e^-$ and a ToT of 5 with an injected charge of $16000 e^-$. Figure 5.4b shows the deviation from the target threshold after the tuning.

ToT



(a) Mean ToTs after a tuning with a target ToT of 5



(b) Mean ToTs after tunings with a target ToT of 10

Figure 5.5.: Mean ToT values of the chips C1-1, C3-1 and C4-1 after tunings. The errorbars show the standard deviation while the boxes show the minimal and maximal value. The minimum and maximum are defined as the middle of the first and last bin in which at least 0.1% of all pixels are sorted.

The ToT tunings presented in Figure 5.5 show the desired results. The mean ToT values listed in Table A.4 are non-integer values as they are averaged over 500 measurements. The ToT itself is an integer, therefore it can be said from the results that the ToT was successfully tuned to the target ToT with a standard deviation of less than one clock cycle for all target parameter combinations. The tuning with an injected charge of $10000 e^-$ resulted in a slightly lower mean ToT value as the tunings with an injected charge of $16000 e^-$. The histograms for the ToT values, one of which is presented in Figure 5.6, also show a rather high peak at a ToT value of 9. This can be explained by the "timewalk effect". A lower injection charge results in a lower signal amplitude and a less steep rising edge which in turn results in a reduced ToT. Therefore, the falling speed of the signal must be reduced in comparison with tunings at a higher injection charge to reach the same ToT. This can be done by lowering the value of the 'PrmpVbpf' parameter. However, as one can see in Table A.2 this parameter was already set to zero for the C3-1 and C4-1 chips for a tuning with $16000 e^-$ injected and cannot be decreased anymore. For the C1-1 chip the parameter was lowered from 32 to 0, therefore it is possible that an optimal value for the global parameter cannot be reached for an injected charge of $10000 e^-$ as the charge is too low. However, the pixel specific Fdac values were decreased as expected. Histograms which show the Fdac values depending on the injected charge can be found in Figure A.1.

The large maximal ToT deviation for the C4-1 chip at a target threshold of $1500 e^-$ and a target ToT of 10 with an injected charge of $16000 e^-$ seems to be uncorrelated to the tuning parameters. As depicted in Figure A.2, the large deviations are found for some pixels mostly at the upper right corner of the chip. However, the ToT deviation does not follow any pattern like the Fdac values

depicted in Figure 5.7a do.

What can be seen in Figure 5.7 is a correlation between the threshold deviation of a pixel and its Fdac value. This is to be expected, as the pixel ToT tuning is done after the pixel threshold tuning (cf. Table 4.2). When the threshold is too low, the signal needs to decrease faster in order to reach the same ToT response. Therefore, pixels with a lower threshold show a higher Fdac value. The pattern in the threshold deviation hints at problems with the pixel threshold tuning, but the Fdac values in combination with the ToT results of a mean ToT of 9.93 ± 0.6 show that the ToT pixel tuning was able to compensate for the results of the threshold tuning.

An observation from the evaluation of the YARR tuning results in Section 5.2.2 is that the configuration parameters 'FdacVbn' and 'TdacVbp' did not have the optimal values. YARR reached better tuning results with the setting 'FdacVbn'=30 and 'TdacVbp'=150 instead of 'FdacVbn'=50 and 'TdacVbp'=255. The latter was used in the tunings with RCE. Therefore, a tuning to a threshold of $3000 e^-$ and a ToT of 10 was done with the other values to see if RCE reaches better tuning results as well.

From the results presented in Table 5.1, it appears that tunings with RCE with the changed parameters return target values with a reduced standard deviation and mean values slightly further away from the target values. The differences in the mean values are negligibly small but the standard deviation of the threshold values is reduced by roughly 45% for both front end chips, suggesting that the values 'FdacVbn'=50 and 'TdacVbp'=255 taken from the FE-I4 Guide lead to a higher standard deviation than necessary.

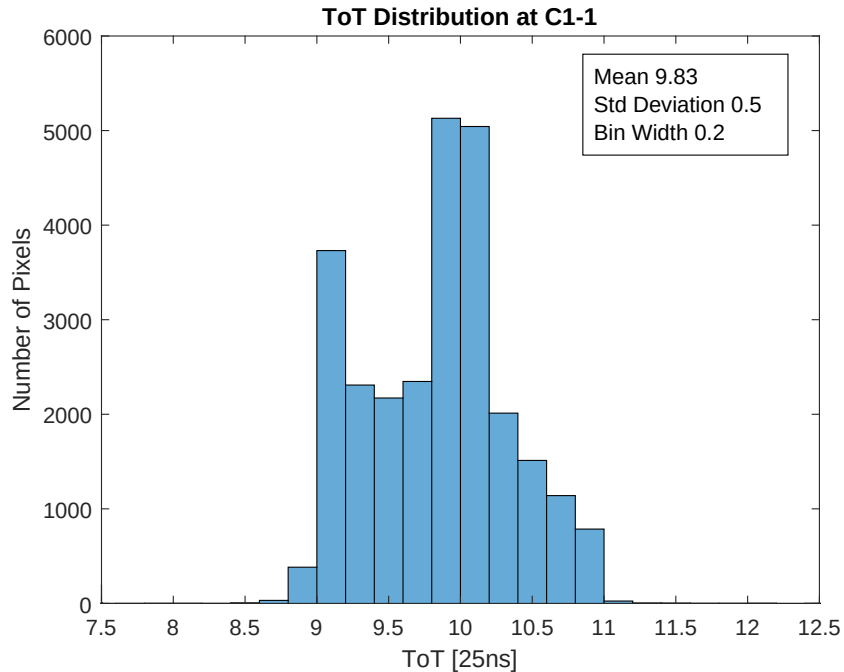
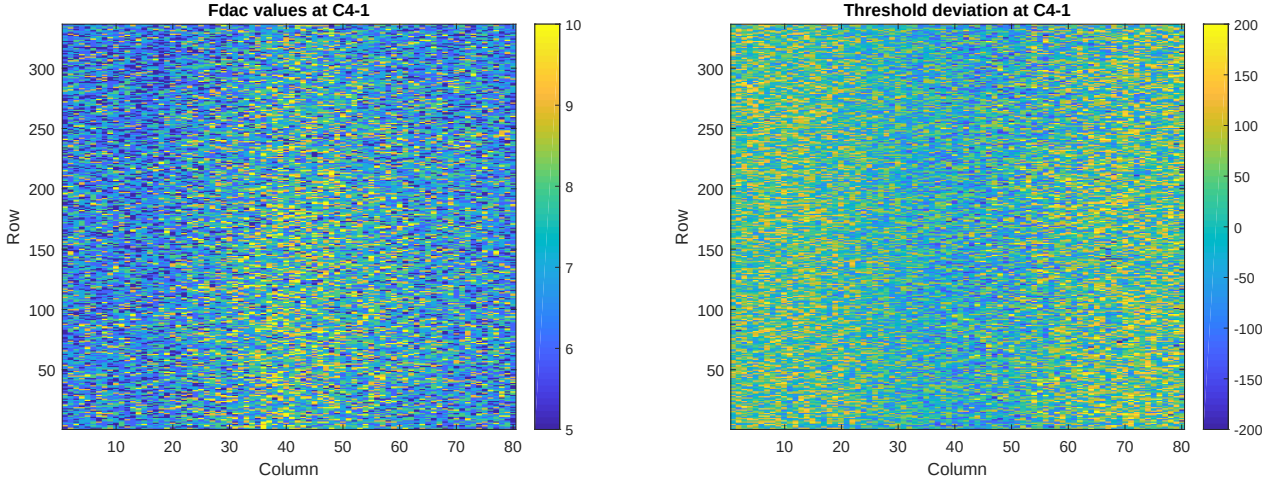


Figure 5.6.: Histogram of the ToT distribution at C1-1 after a tuning to a target threshold of $3000 e^-$ and a ToT of 10 with an injected charge of $10000 e^-$



(a) Fdac values at C4-1 after the tuning

(b) Deviation from the target threshold of 1500 e^- at C4-1 after the tuning

Figure 5.7.: Fdac values and threshold deviation at C4-1 after a tuning with a target threshold of 1500 e^- and a target ToT of 10 with an injected charge of 16000 e^- .

Table 5.1.: Tuning results of RCE with configuration file parameters 'FdacVbn'=30 and 'TdacVbp'=150. The tuning was done with a target threshold of 3000 e^- , a target ToT of 10 and an injected charge of 16000 e^- . The columns named 'old results' show the results of the first tunings with 'FdacVbn'=50 and 'TdacVbp'=255 for comparison.

Chip	changed parameters		old results	
	Threshold in e^-	mean ToT in 25 ns	Threshold in e^-	mean ToT in 25 ns
C3-1	3020 $\pm$ 35	9.94 $\pm$ 0.3	3012 $\pm$ 51	9.99 $\pm$ 0.4
C4-1	3028 $\pm$ 41	9.90 $\pm$ 0.3	3012 $\pm$ 59	9.97 $\pm$ 0.4

5.2. YARR

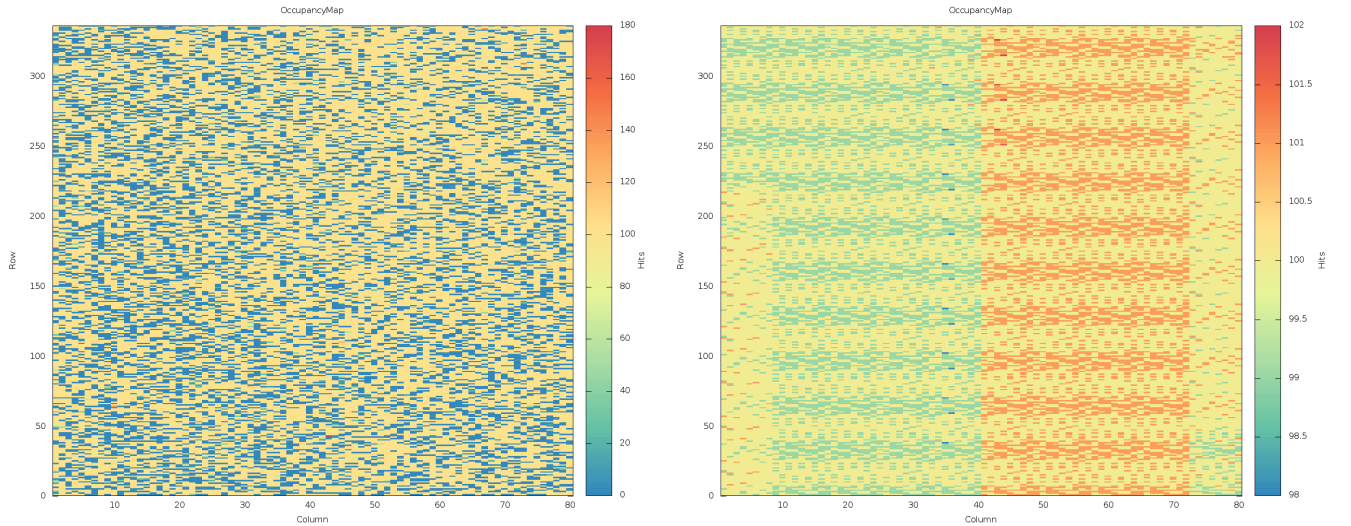
Contrary to the tunings with RCE, the tunings with YARR showed a strong dependency on the configuration files of the front end chips. Therefore, different configuration files were used for the tunings and the following discussion deals with the results obtained with the different configuration files separately. Section 5.2.1 describes the issues that occurred during the first scans, the following Section 5.2.2 and Section 5.2.3 present the results of the tunings done with the different configuration files.

5.2.1. Problems encountered

Failing digital and analog tests

The tunings with YARR showed results which made it necessary to change the tuning scripts, unlike the tunings with RCE discussed in Section 5.1. First of all, the FE-I4B C1-1 showed bad analog scans when configured with the standard configuration file that was used for all RCE tunings. The occupancy map of the scan can be seen in Figure 5.8a. Therefore it was necessary to switch to the YARR default configuration file. Nevertheless, tunings were also made with the standard configuration file for the other two chips C3-1 and C4-1.

Digital scans with more than one chip at a time produced an error pattern that suggests that some hits were assigned to the wrong pixels. The occupancy maps looked the same for all three chips, one of which can be seen in Figure 5.8b. Pixels on the left side of the chip recorded one hit less than injected while pixels on the right side recorded one more hit. Therefore, the scans were done separately for each chip.



(a) Occupancy map of an analog scan from the C1-1 chip with the standard configuration file. 100 hits were injected

(b) Occupancy map of a digital scan from the C4-1 chip. 100 hits were injected and the three chips C1-1, C3-1 and C4-1 were scanned simultaneously.

Figure 5.8.: Occupancy maps of failing digital and analog scans with YARR

Bugs

The first tunings with YARR showed unexpected results, as the ToT tuning did not work as intended. In a manual tuning procedure using the YARR scan console, the 'PrmpVbpf' parameter responsible for the global ToT setting was always tuned to a value of 1, regardless of the target ToT. Using the YARR tuning script resulted in a ToT of 14, which is the highest possible value. The reason for the latter problem was an issue with the tuning script. The script uses three target parameters, target threshold, target ToT and target charge. The individual scans only use two parameters each. The threshold tunings use the target threshold and target ToT as input arguments, while the ToT tunings use the target charge and the target ToT. The order in which the parameters are given to YARR is important, as the first input parameter is interpreted as the target threshold or charge respectively. For the ToT tunings, the parameters were taken in the wrong order by the tuning script, which resulted in YARR trying to tune the chip to a target ToT of 16000 with an injected charge of $10 e^-$. Changing the order in the tuning script solved the issue.

The other problem, which resulted in a 'PrmpVbpf' value of 1, was a bug in the Analysis script of YARR. The binary algorithm that should set the 'PrmpVbpf' parameter to the optimal value used a hard-coded target ToT value of 10. Therefore, the global threshold tuning always tuned the chip to a ToT of 10, ignoring the ToT specified by the user.

5.2.2. Standard configuration files

As explained in Section 5.2.1, the FE-I4B C1-1 showed a bad analog scan with the standard configuration file used for the RCE tunings. Therefore, the tunings with that configuration file were done for the chips C3-1 and C4-1 only. The standard configuration file uses the values suggested in the FE-I4 Guide [11] for the configuration parameters. The most important difference from the YARR default files are the values for the 'TdacVbp' and 'FdacVbn' parameter, as they have a great influence on the threshold and ToT tunings as will be shown below. An overview of the values of the configuration parameters can be found in Table A.1.

Threshold

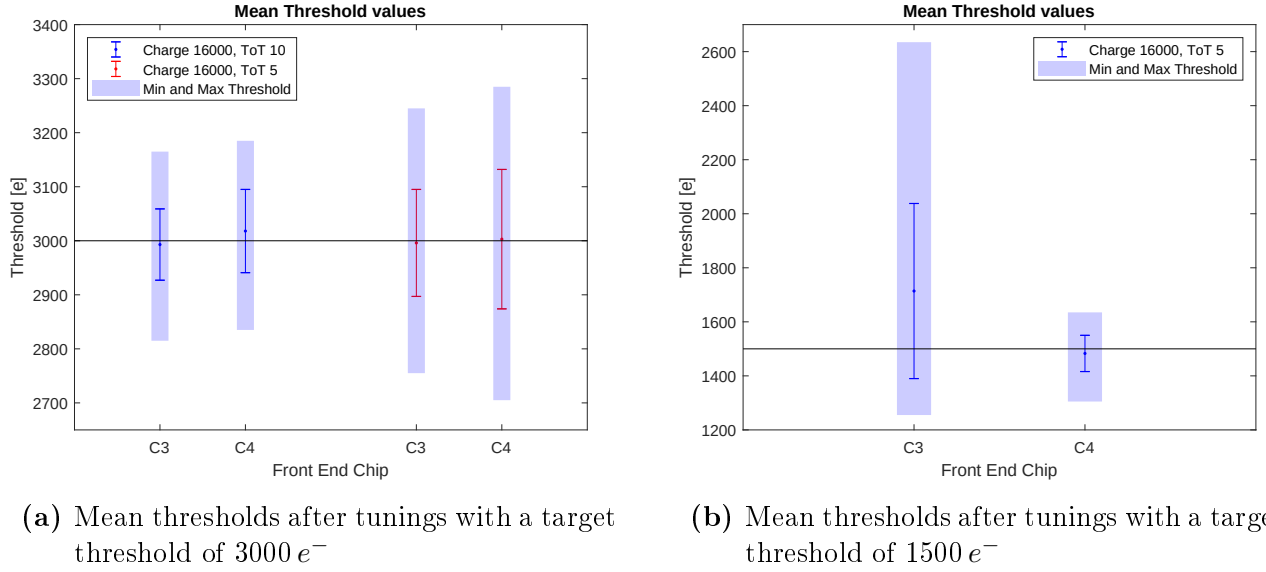


Figure 5.9.: Mean threshold values of the chips C3-1 and C4-1 after tunings with the standard configuration files. The errorbars show the standard deviation while the boxes show the minimal and maximal value. The minimum and maximum are defined as the middle of the first and last bin in which at least 0.1% of all pixels are sorted.

The tunings with a target threshold of $3000 e^-$ presented in Figure 5.9a show satisfying results. The largest deviation from the target value is the mean threshold of $3018 \pm 77 e^-$ for the C4-1 chip. The tunings with a target ToT of 5 show higher standard deviations and generally a wider range between the minimal and maximal threshold.

From Figure 5.9b it can be seen that the tuning to a threshold of $1500 e^-$ and a ToT of 5 did not result in the desired threshold for the C3-1 chip. The obtained threshold of $1714 \pm 324 e^-$ is too large and the values for the minimal and maximal threshold also show a clear shift towards higher thresholds. Plotting the mean threshold for each pixel individually as a kind of occupancy map (cf. Figure 5.11a) shows a region a little below the middle of the chip, where most pixels were tuned to a higher threshold. The Tdac map presented in Figure 5.11b also shows that the Tdacs were set to 31 for many pixels, which is the highest possible value.

The reason for this can be found in the occupancy map, which is created by YARR for every pixel threshold tuning. The occupancy map presented in Figure 5.10 shows how many hits every pixels recorded. A pixel tuned to the correct target threshold should see 50% of all hits. This equals an occupancy of 100 hits in Figure 5.10 as 200 hits are injected during the threshold tuning. Many pixels of the C3-1 chip did not see any hits and the position of these pixels corresponds to the pixels with the highest Tdac values in Figure 5.11b.

The occupancy map of the global threshold tuning (cf. Figure A.3a) shows that almost all pixels showed an occupancy of 0 hits after the tuning. This should result in YARR decreasing the pixel threshold, but the global parameter 'Vthin_fine' was set to the highest possible value as well as

many of the pixel specific Tdacs.

A conceivable explanation is that the algorithm producing the occupation map experienced problems due to the low threshold setting. The histogram for the occupancy distribution in Figure A.3b shows an occupancy of almost 200 hits for all pixels after the global tuning. This contradicts the occupancy map based on the very same scan result that shows an occupancy of 0 hits per pixel. A target threshold of $1500 e^-$ is a very low value and it is possible that the tuning is affected by the electronic noise. The chip probably saw too many hits to be processed properly. A tuning with the same chip to a target threshold of $2000 e^-$ and a target ToT of 5 showed much better results. As one can see in Figure 5.12, the mean target threshold is close to the target value, albeit the standard deviation is still quite high.

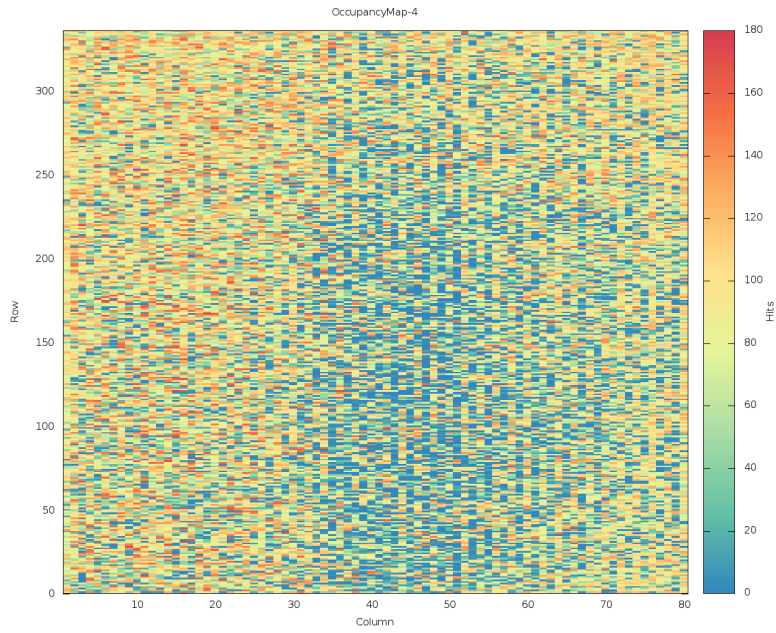
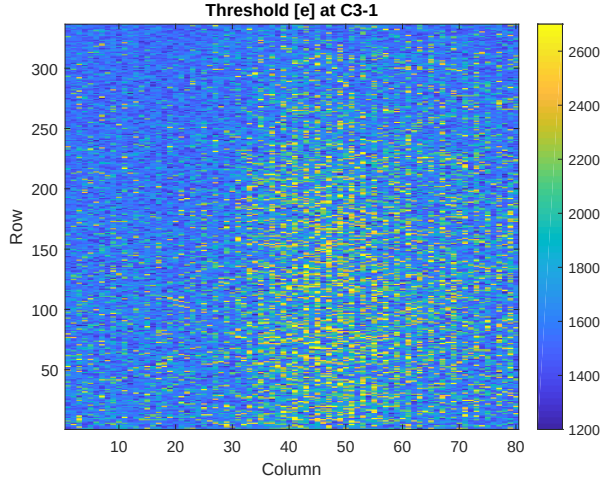
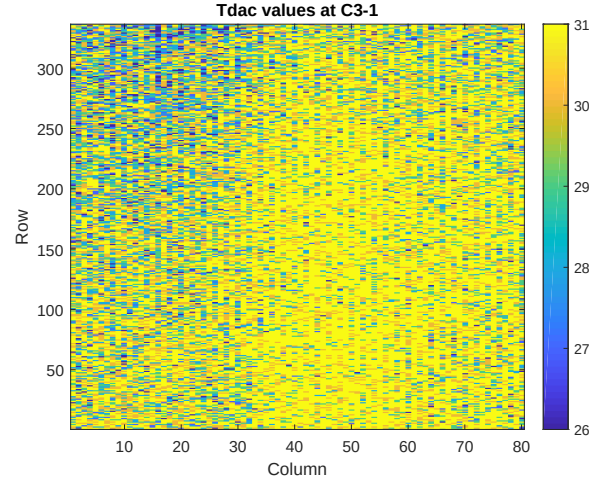


Figure 5.10.: Occupancy map after the final threshold tuning at C3-1. The chip was tuned to a target threshold of $1500 e^-$ and a target ToT of 5 with an injected charge of $16000 e^-$.

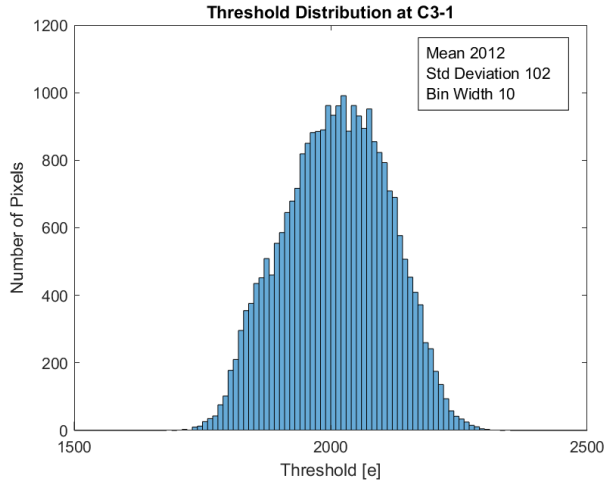


(a) Mean threshold values at C3-1

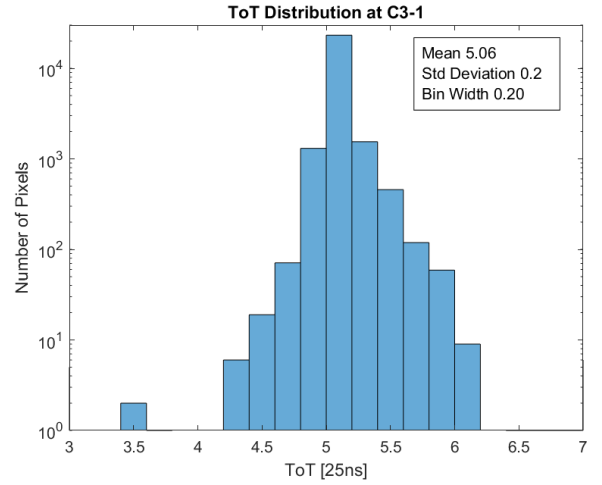


(b) Tdac values at C3-1

Figure 5.11.: Mean threshold values and Tdac values at C3-1 after a tuning to a target threshold of $1500 e^-$ and a target ToT of 5 with an injected charge of $16000 e^-$.



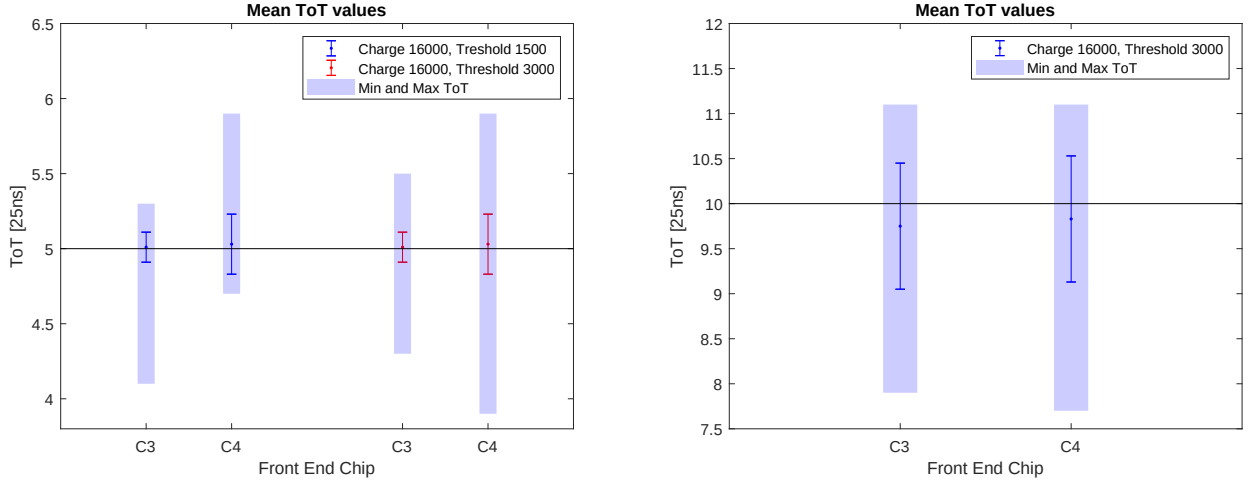
(a) Mean threshold at C3-1



(b) Mean ToT at C3-1

Figure 5.12.: Tuning results of C3-1 after a tuning with a target threshold of $2000 e^-$, a target ToT of 5 and an injected charge of $16000 e^-$. The histograms show the results of a single threshold scan or ToT respectively, which means that the results are averaged over 100 measurements.

ToT



(a) Mean ToTs after tunings with a target ToT of 5

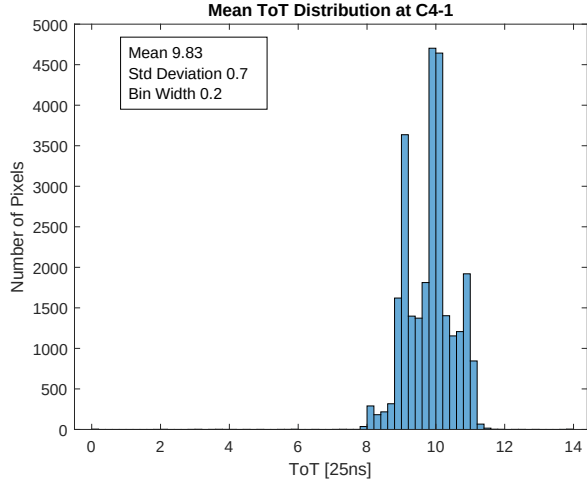
(b) Mean ToTs after tunings with a target ToT of 10

Figure 5.13.: Mean ToT values of the chips C3-1 and C4-1 after tunings with the standard configuration files. The errorbars show the standard deviation while the boxes show the minimal and maximal value. The minimum and maximum are defined as the middle of the first and last bin in which at least 0.1% of all pixels are sorted.

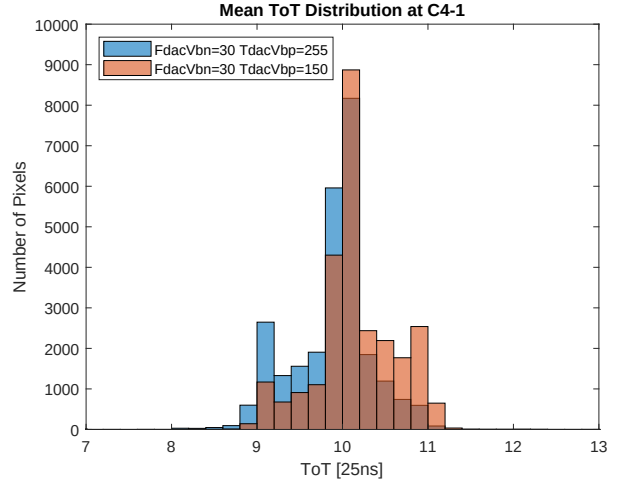
The tunings to a target ToT of 5 presented in Figure 5.13a show results similar to the tunings with RCE (cf. Figure 5.5), as the ToT reached after the tunings is centered on the target value with a deviation of less than one clock cycle. The tuning to a target ToT of 10 produced some unexpected peaks at a ToT value of 9 and 11 respectively, as one can see in Figure 5.14a. The higher peak at a ToT of 9 leads to the mean ToT beneath the target ToT of 10.

As a similar ToT distribution was reached after tuning with RCE with an injected charge of $10000 e^-$, some tunings were done with the C4-1 chip at higher injection charges. The result of the tunings, as one can see in Figure A.4 shows clearly that the undesired peaks at a ToT of 9 and 11 decrease considerably with an increasing injection charge. This result is to be expected, as the timewalk effect has a greater influence on tunings with a lower injection charge. However, an injected charge of $16000 e^-$ is a standard value and a decent tuning with this setting should be possible.

The peaks at a ToT of 9 and 11 did also not appear after the tuning with the YARR default configuration files, which hints at the setting of a configuration parameter as the cause of the result. Therefore, some tunings were made with the same target parameters and the standard configuration file, but for each tuning, one configuration parameter was altered. It turned out that the parameters 'FdacVbn' and 'TdacVbp' had the greatest impact on the results, as one can see in Figure 5.14b.



(a) Mean ToT at C4-1 after tunings with a target ToT of 10



(b) Mean ToT at C4-1 after tunings with a target ToT of 10 with varying configuration parameters

Figure 5.14.: Mean ToT values at C4-1 after tunings with varying configuration parameters 'FdacVbn' and 'TdacVbp'. The histograms in Figure 5.14b show the results of a single ToT scan respectively, which means that the results are averaged over 100 measurements.

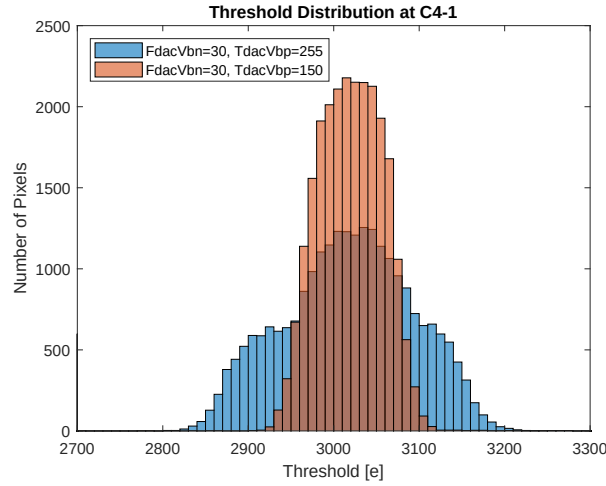


Figure 5.15.: Results of threshold tunings with C4-1 at different configuration parameters 'FdacVbn' and 'TdacVbp'. The tuning was done with a target threshold of $3000 e^-$ and a target ToT of 10 with an injected charge of $16000 e^-$.

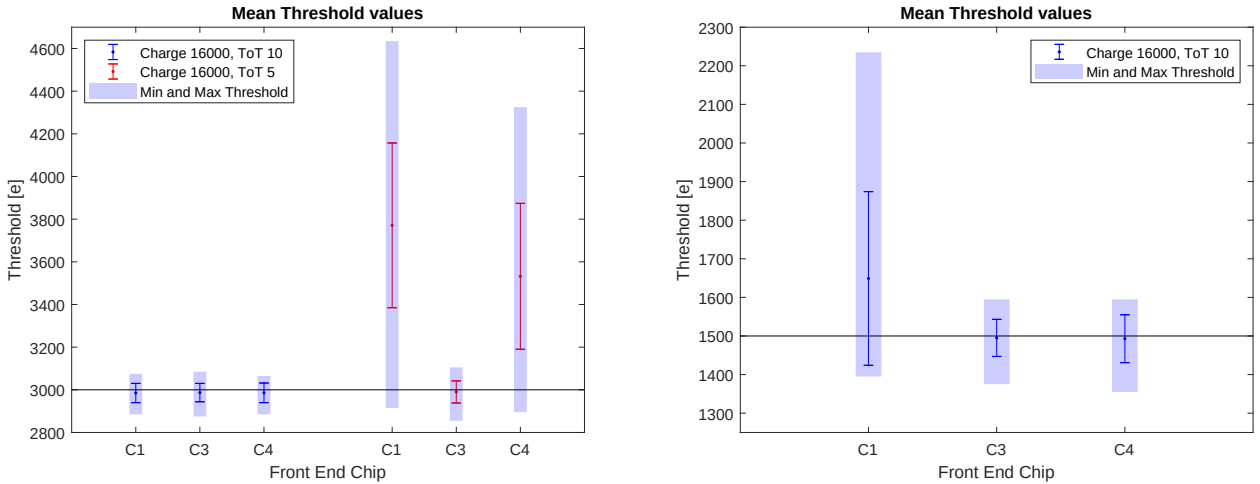
The parameters 'FdacVbn' and 'TdacVbp' set the step size for the least significant bit (LSB) of the pixel specific Fdac and Tdac registers. A high value means that the DAC can cover a wider signal range at the cost of a coarser step size. The standard configuration file uses the suggested values from the FE-I4 Guide [11] of 'FdacVbn' = 50 and 'TdacVbp' = 255. Changing the 'FdacVbn'

value to 30 showed significant improvements in the ToT distribution. Using the values suggested by the YARR default configuration files results in a higher peak at a ToT of 11, as one can see in Figure 5.14b. It appears that a lower 'TdacVbp' value results in a better threshold tuning (cf. Figure 5.15) but in a less precise ToT tuning. The results of this short test series suggest that a compromise between a precise ToT and a precise threshold must be found.

5.2.3. Default configuration files

As explained in Section 5.2.1, the FE-I4B C1-1 showed a bad analog scan with the configuration file used for the RCE tunings. Therefore, the tunings discussed in this section were done with the default configuration file from the YARR software in order to gain tuning results from all three front end chips for a comparison with the RCE results. The default configuration file uses other values for some of the configuration parameters. The most important differences are the altered values for the 'TdacVbp' and 'FdacVbn' parameter, as they have a great influence on the threshold and ToT tunings (cf. Section 5.2.2). An overview of the values of the configuration parameters can be found in Table A.1.

Threshold



(a) Mean thresholds after tunings with a target threshold of $3000 e^-$

(b) Mean thresholds after tunings with a target threshold of $1500 e^-$

Figure 5.16.: Mean threshold values of the chips C1-1, C3-1 and C4-1 after tunings with the YARR default configuration files. The errorbars show the standard deviation while the boxes show the minimal and maximal value. The minimum and maximum are defined as the middle of the first and last bin in which at least 0.1% of all pixels are sorted.

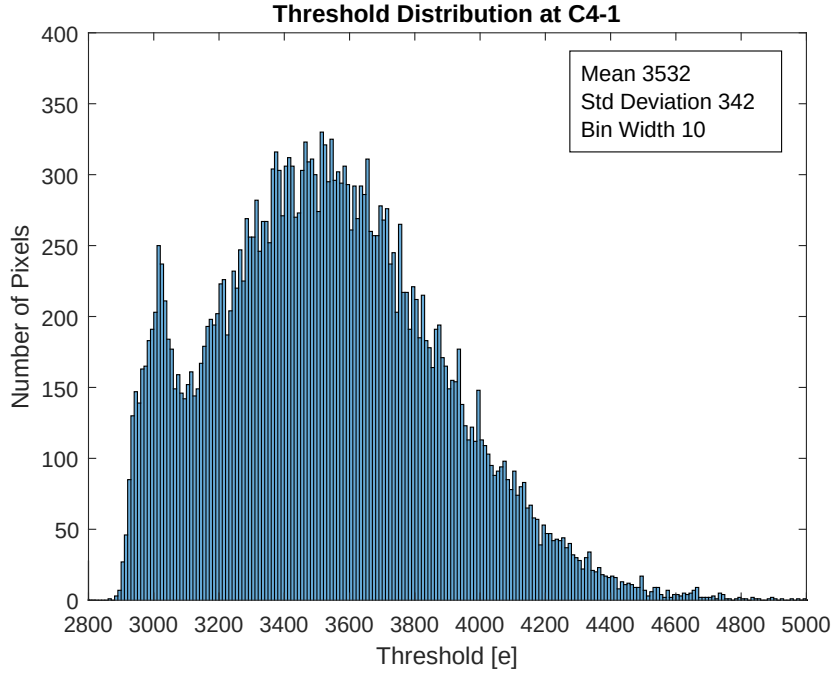


Figure 5.17.: Threshold distribution at C4-1 after a tuning to a target threshold of $3000 e^-$ with a target ToT of 5

As one can see from Figure 5.16a, the tuning to a threshold of $3000 e^-$ with a target ToT of 10 shows good results for the threshold, while the tuning with a target ToT of 5 did not result in the target threshold for the chips C1-1 and C4-1. The global parameter 'Vthin_fine' as well as the pixel specific Tdacs are set to very high values (cf. Figure A.5). As a consequence, the threshold of most pixels is set to a too high value, as the histogram in Figure 5.17 exemplarily shows.

It seems that YARR experienced problems with the threshold tuning for a low ToT. This is a rather unexpected result, as the YARR tuning procedure ends with a pixel threshold tuning and a threshold of $3000 e^-$ is not such a low value as that there should be serious problems due to the electronic noise. It is also counterintuitive that a steeper falling edge of the signal, produced by the low target ToT of 5, should result in pixels showing an occupancy higher than wanted during threshold scans.

The tuning of the C1-1 chip to a threshold of $1500 e^-$ showed the same problems described in Section 5.2.2 for the C3-1 chip. Almost all pixels recorded no hits after the final global threshold tuning and the Tdac values are mostly set to 31. However, this time a tuning to a threshold of $2000 e^-$ did not show a good result but rather a threshold distribution resembling the one seen in Figure 5.17.

Taking the results of the threshold tunings with RCE and YARR with the other configuration files into consideration, it appears that the YARR default configuration files are optimized for a tuning to a threshold of $3000 e^-$ and a ToT of 10 but do not always deliver good results for other parameter combinations. It has already been established that the condition of the C1-1 chip as well as the temperature are possible explanations for bad tuning results but the similarity between

the results of the three failed threshold tunings in combination with the results of the preceding tunings suggest that the reason is to be found in the configuration file.

ToT

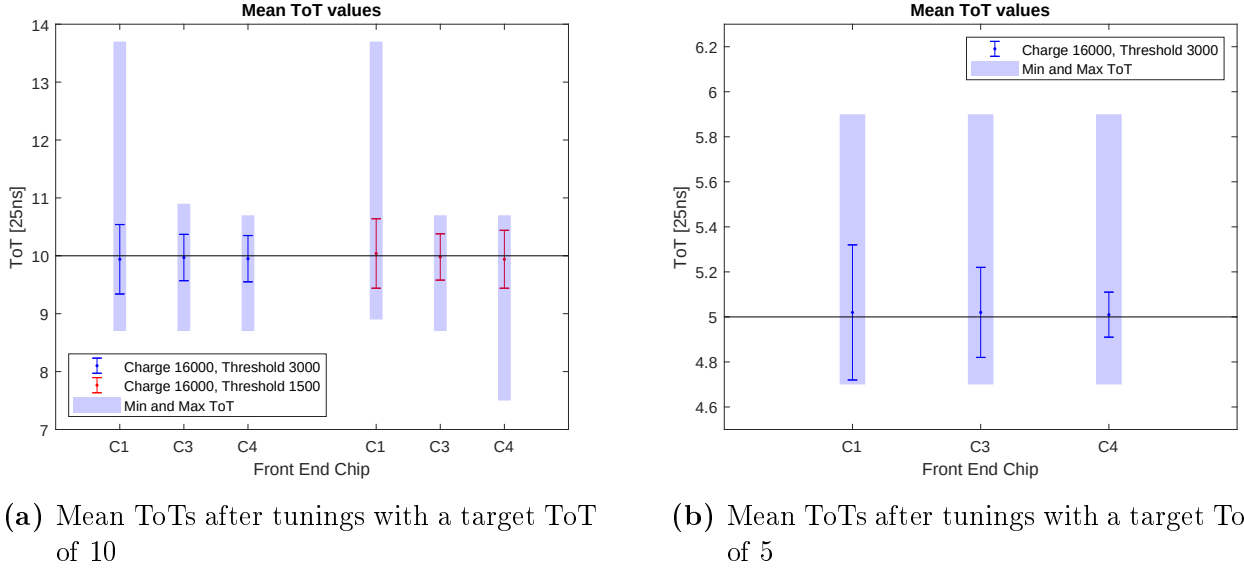


Figure 5.18.: Mean ToT values of the chips C1-1, C3-1 and C4-1 after tunings with the YARR default configuration files. The errorbars show the standard deviation while the boxes show the minimal and maximal value. The minimum and maximum are defined as the middle of the first and last bin in which at least 0.1% of all pixels are sorted.

One can see from Figure 5.18a that the tuning to a ToT of 10 was successful, as the standard deviation of the mean values is again lower than one clock cycle. The maximal deviation of the C4-1 chip from the tuning with a target threshold of $1500 e^-$ is a systematic error with one of the mask stages (cf. Figure A.6). For the C1-1 chip there are some pixels that were set to a very high threshold. These pixels are all located in the vicinity of pixels that showed a bad response in the analog scan (cf. Figure A.7), which suggests that this result can be traced back to damages in these pixel regions. On the other hand, the tunings with RCE (cf. Figure 5.5b) do not show these large deviations. As the tunings with YARR were done about seven weeks after the tunings with RCE, it cannot be said for certain if the deviation is caused by damages in the chip or by problems with YARR.

The tunings to a ToT of 5 presented in Figure 5.18b show very similar results. The results for the different front end chips only differ in the standard deviation, which is 0.1 clock cycles for the C4-1 chip, 0.2 cycles for C3-1 and 0.3 cycles for C1-1. As the standard deviations are only given with one digit behind the decimal point, the difference is a really small one and it can be said that the tuning was equally successful for all chips. This is especially remarkable as the threshold tunings showed varying degrees of success. The YARR tuning procedure ends with a

pixel threshold tuning (cf. Table 4.2) but it seems that the tuning is occasionally not able to adapt the threshold properly while the ToT tuning works as intended.

5.3. Comparison

The tuning results of RCE and YARR presented in the sections above are compared in the following. The YARR results are those from the tuning with the YARR default configuration files (cf. Section 5.2.3) as the C1-1 chip showed bad analog scans with the configuration file used for the RCE tunings. The most important difference between the configuration files are the values used for the 'FdacVbn' and 'TdacVbp' parameter, which can be found in Table A.1.

Table 5.2.: Comparison of the tuning results of YARR and RCE. The values in the first column are the target values in the following order: target threshold in e^- /target ToT in 25 ns. The tunings were done with an injected charge of $16000 e^-$. The error given for the threshold and ToT values is the standard deviation. The YARR results are those produced by tunings with the YARR default configuration file.

target values	Chip	YARR		RCE	
		Threshold in e^-	ToT in 25 ns	Threshold in e^-	ToT in 25 ns
3000/10	C1-1	2985±45	9.94±0.6	2964±94	9.94±0.4
	C3-1	2987±43	9.97±0.4	3012±51	9.99±0.4
	C4-1	2986±46	9.95±0.4	3012±59	9.97±0.4
3000/5	C1-1	3771±386	5.02±0.3	2911±154	5.00±0.2
	C3-1	2990±52	5.02±0.2	3020±72	5.00±0.1
	C4-1	3532±342	5.01±0.1	3014±90	4.99±0.1
1500/10	C1-1	1649±225	10.04±0.6	1463±79	9.96±0.5
	C3-1	1495±48	9.98±0.4	1518±73	9.96±0.4
	C4-1	1493±62	9.94±0.5	1513±97	9.93±0.6

What can be seen from Table 5.2 is that both YARR and RCE were able to tune the chips to the target ToT for all three tuning parameter combinations. The mean values differ from the target value in the second decimal digit and the standard deviations all lie between 0.1 and 0.6 clock cycles, with the largest difference between the YARR and RCE standard deviation being 0.2 clock cycles. For most measurements with both RCE and YARR, the C1-1 chip showed a higher standard deviation for the ToT values so this is probably a chip specific issue related to the bad condition of the module of the C1-1 chip (cf. Table 4.1).

The only noteworthy thing is the high maximal ToT value of the C1-1 chip after tunings with YARR to a ToT of 10 discussed in Section 5.2.3, as it cannot be said for certain whether it is caused by defects in the chip or problems with the tuning. All in all, it can be said that the readout systems both delivered satisfying results.

For the threshold tuning, it appears that RCE arrived at a wider distribution, resulting in a higher standard deviation. However, the exemplary tunings to a threshold of $3000 e^-$ and a ToT of 10 done with some configuration parameters changed (cf. Section 5.1) resulted in a threshold of

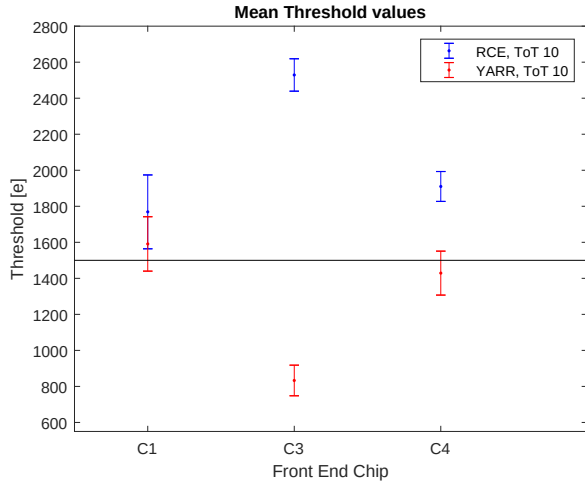
$3020 \pm 35 e^-$ for C3-1 and $3028 \pm 41 e^-$ for C4-1. As these standard deviations are on a par with the results produced by YARR, it cannot be said that RCE tunes more inaccurate than YARR but rather that the parameters suggested by the FE-I4 Guide [11] do not return optimal results for the threshold tuning.

From the global tuning parameters listed in Table A.2 and Table A.5 it appears that RCE delivers more continuous results. The C3-1 and C4-1 chips had the global tuning parameters set to the same value after each tuning with RCE while YARR always reached different settings for the two front end chips. Also, the deviation from the target threshold follows a clear pattern for the RCE results, namely that the threshold at C1-1 is too low while the thresholds at C3-1 and C4-1 are slightly too high. For the YARR results there is no such apparent pattern but it seems that YARR has difficulties tuning to specific target parameter combinations such as a target threshold of $3000 e^-$ and a target ToT of 5. However, a target ToT of 5 is a very low value not normally used for actual measurements.

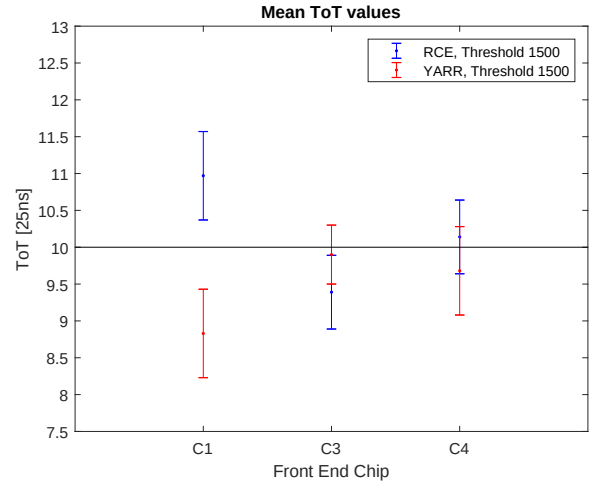
The tuning results of YARR also showed a greater dependency on the configuration file parameters. The C1-1 chip showed a bad analog response when configured with the configuration file used for the RCE scans and the C3-1 and C4-1 chip showed unwanted peaks in the ToT after a tuning with an injected charge of $16000 e^-$. RCE showed a comparable result after a tuning with an injected charge of $10000 e^-$ only, which means that YARR needed considerably higher charges to reach a proper tuning result with the configuration file used for the tunings with RCE.

All in all, it can be said that YARR and RCE reach equally good tuning results for the commonly used target values of a threshold of $3000 e$ and a ToT of 10, but RCE delivers better results for extremely low target values.

The results presented in the following were obtained by performing threshold and ToT scans with YARR and RCE using the configuration files that were tuned with the other readout system. As discussed above, YARR and RCE returned equally good tuning results but returned different values for the global configuration parameters. Therefore, the configuration files tuned to a target threshold of $1500 e^-$ and a target ToT of 10 were tested with the other readout system respectively to see if there are any changes in the threshold and ToT response. The results of the measurements are presented in Figure 5.19



(a) Results of the threshold scans



(b) Results of the ToT scans

Figure 5.19.: Results of threshold scans with YARR and RCE using the tuned configuration files of the other readout system. The used configuration files were tuned to a threshold of $1500 e^-$ and a ToT of 10 with an injected charge of $16000 e^-$.

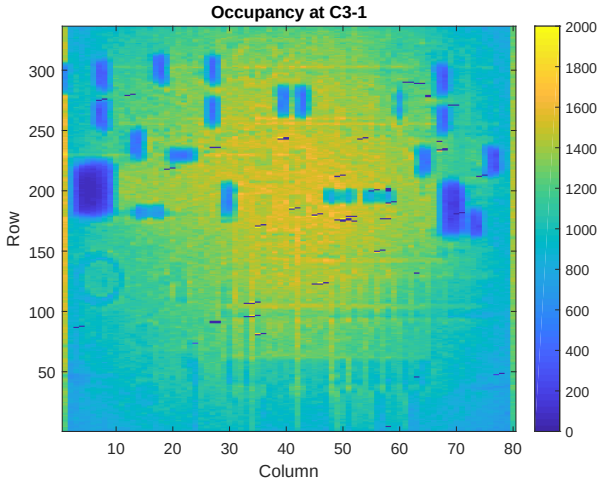
What can be seen from Figure 5.19a is that YARR reaches lower threshold values than RCE for all chips. Also, the deviation from the target value appears to be chip specific, as the distance between the results at C3-1 is larger than at C4-1, even though the difference between the values found for the parameter 'PrmpVbp' responsible for the global threshold setting is lower for C3-1 (cf. Table A.2 and Table A.5).

Interestingly, the ToT scans at C3-1 and C4-1 show rather good results as one can see in Figure 5.19b. For C1-1, YARR and RCE measure similar threshold values both above the target of $1500 e^-$ but the ToT values are about one clock cycle too high or low respectively. All in all it can be seen that the different results for the configuration parameters after tunings are caused by differences between the readout systems and are not simply two configurations that work equally well for both systems.

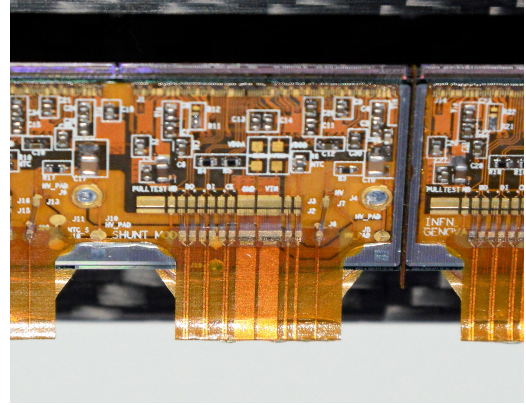
5.4. Source Scan

A source scan is a scan in which particles emitted from a radioactive source are detected. The chip is put into a selftrigger mode, which means that there is no external trigger that determines when the chip is read out but the pixels themselves send the trigger signal when a hit is recorded. Passive components of the FE-I4B can be made visible via a source scan, as regions of the sensor covered by these components see fewer hits or even no hits at all.

To perform the source scan, a Sr-source was placed right above the front end chip C3-1 with which the measurement was done. The scan was done with the RCE readout system and the configuration file that was tuned to a target threshold of $3000 e^-$ and a target ToT of 10 with an injected charge of $16000 e^-$. The chip was operated in the selftrigger mode for 600 s. The occupancy map showing how many hits the individual pixels recorded is presented in Figure 5.20a.



(a) Result of a source scan with a Sr-source at C3-1



(b) Photography of a FE-I4B

Figure 5.20.: Source scan result and an image of a FE-I4B.

It can be said that the source scan worked as intended. The single cells spread over the whole map and coloured dark blue in Figure 5.20a are dead pixels but the large blue areas in the upper half mark the position of electrical components on the module flex. As the sensor tile is underneath the front end chip shown in Figure 5.20b, the position of the components is mirrored in the occupancy map. The blue areas of the occupancy map, indicating that those pixels saw very few to no hits, match the positions of resistors and capacitors on the front end chip. It can also be seen that the source was not placed exactly over the centre of the chip, as the region where the most hits were recorded is above the middle. All in all, the structure of the FE-I4B and even the position of the radioactive source can be seen very clearly from the source scan result.

6. Conclusion

Generally speaking, the tunings with both readout systems showed satisfying results. Both YARR and RCE reached good values for a target threshold of $3000\text{ }e^-$ and a target ToT of 10 with an injected charge of $16000\text{ }e^-$, which is a parameter combination commonly used. RCE showed more stable results after tunings with very low target parameters, such as a threshold of $1500\text{ }e^-$ or a target ToT of 5. For these tunings, YARR occasionally returned threshold values more than $500\text{ }e^-$ above the target value.

Both readout systems occasionally returned threshold values that were not tuned properly to the target value while the ToT tunings still returned the target value. Especially for the low target threshold of $1500\text{ }e^-$, this is most likely an effect caused by electronic noise due to the rather high chip temperature of about 20°C . The tunings with the C1-1 chip also showed more inaccurate results than the tunings with the C3-1 and C4-1 chip, which can be explained by damages of the module of C1-1.

However, some deviations from the target values, as seen for the threshold values of C1-1 and C4-1 after a tuning to a target threshold of $3000\text{ }e^-$ and a target ToT of 5, are too similar to each other to be caused by environmental influences only. These deviations are more likely caused by the parameters in the configuration files, as different values for some parameters resulted in considerably different tuning results. YARR generally showed a higher dependency on the configuration files of the tuned chips than RCE. Therefore, it can not be said that YARR generally delivers more inaccurate results for the low target values but rather that YARR was not able to tune the used configuration files to the target values.

Both readout systems showed different tuning results when the configuration parameters 'FdacVbn' and 'TdacVbp' were altered. The parameters regulate the step size of the pixel specific discriminators which are used for the threshold and ToT tuning. From a short testing series with different values for these parameters, it appears as if a very low standard deviation of the threshold goes hand in hand with a higher standard deviation of the ToT. Therefore, one result is that the quality of the tuning results is influenced considerably by the configuration of the front end chips, albeit the influence was seen more clearly in the tunings with YARR.

The scans that were done with YARR and RCE using the tuned script of the other readout system showed that the final configurations of the front end chips differ between the systems. Scans with the tuned configuration file of the other system do not result in the target parameters the file was originally tuned to. This shows how YARR and RCE do not simply reach two different configurations that can be used universally but that there are general differences in the way the data is processed which demand different configurations of the front end chips.

A. Appendix

Setup

Table A.1.: Overview of global configuration parameters from the FE-I4B configuration files that are important for the performed tunings. The value in the 'value RCE' column is the value used for tunings with RCE and the 'value YARR' column contains the values from the YARR default configuration file. The descriptions are taken from the FE-I4 Guide [11].

Config Parameter	Description	Value RCE	Value YARR
PrmpVbpf	Adjustment of global ToT	Changes during global ToT tuning, starts at: 100	40
Vthin_Fine	Adjustment of the global threshold	Changes during global threshold tuning, starts at 230	
TdacVbp	Sets the step size of the in-pixel threshold tuning DAC	255	150
FdacVbn	Sets the step size of the in-pixel amplifier feedback current DAC	50	30

RCE

Table A.2.: Values of global configuration parameters after the tuning procedure. The values in the first row are the tuning parameters in the following order: target threshold in e^- /injected charge in e^- /target ToT in 25 ns.

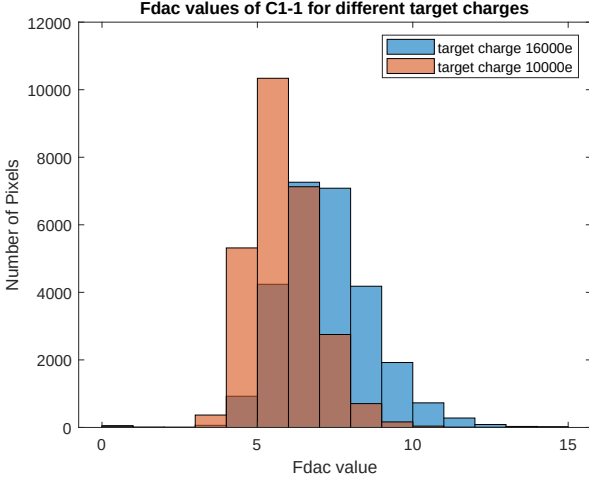
Chip	global parameter	3000/16000/10	3000/16000/5	1500/16000/10	3000/10000/10
C1-1	PrmpVbpf	32	196	72	0
	Vthin_fine	250	199	157	250
C3-1	PrmpVbpf	0	141	33	0
	Vthin_fine	189	136	110	190
C4-1	PrmpVbpf	0	141	33	0
	Vthin_fine	189	136	110	190

Table A.3.: Threshold values after tuning with RCE. The values in the first column are the tuning parameters in the following order: target threshold in e^- /injected charge in e^- /target ToT in 25 ns. The error given for the threshold is the standard deviation. The minimum and maximum is the middle of the outermost bins of the histograms in which 0.1% of all pixels were sorted.

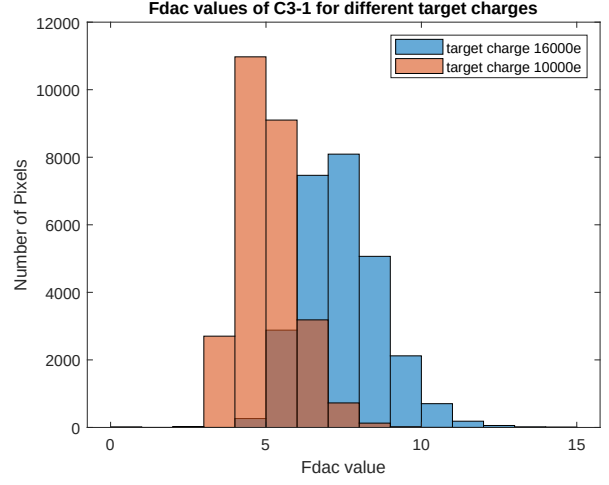
tuning parameters	Chip	Threshold in e^-	Minimum	Maximum
3000/16000/10	C1-1	2964 $\pm$ 94	2845	3065
	C3-1	3012 $\pm$ 51	2885	3115
	C4-1	3012 $\pm$ 59	2875	3125
3000/10000/10	C1-1	2964 $\pm$ 100	2855	3065
	C3-1	3009 $\pm$ 45	2895	3105
	C4-1	3008 $\pm$ 55	2875	3115
3000/16000/5	C1-1	2911 $\pm$ 154	2495	3125
	C3-1	3020 $\pm$ 72	2865	3165
	C4-1	3014 $\pm$ 90	2815	3175
1500/16000/10	C1-1	1463 $\pm$ 79	1305	1595
	C3-1	1518 $\pm$ 73	1355	1665
	C4-1	1513 $\pm$ 97	1325	1695

Table A.4.: ToT values after tuning with RCE. The values in the first column are the tuning parameters in the following order: target threshold in e^- /injected charge in e^- /target ToT in 25 ns. The error given for the ToT is the standard deviation. The minimum and maximum is the middle of the outermost bins of the histograms in which 0.1% of all pixels were sorted.

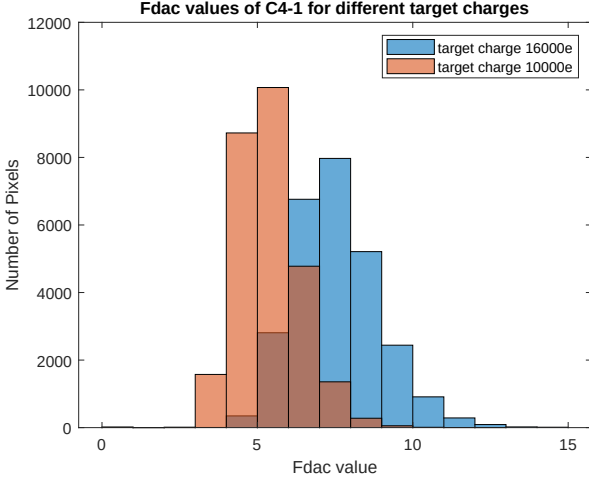
tuning parameters	Chip	mean ToT in 25 ns	Minimum	Maximum
3000/16000/10	C1-1	9.94 $\pm$ 0.4	8.9	10.9
	C3-1	9.99 $\pm$ 0.4	8.9	10.9
	C4-1	9.97 $\pm$ 0.4	8.9	10.9
3000/10000/10	C1-1	9.83 $\pm$ 0.5	8.5	10.9
	C3-1	9.82 $\pm$ 0.6	8.3	10.9
	C4-1	9.84 $\pm$ 0.6	8.5	10.9
1500/16000/10	C1-1	9.96 $\pm$ 0.5	8.5	10.7
	C3-1	9.96 $\pm$ 0.4	8.5	10.7
	C4-1	9.93 $\pm$ 0.6	7.1	11.3
3000/16000/5	C1-1	5.00 $\pm$ 0.2	4.1	5.1
	C3-1	5.00 $\pm$ 0.1	4.8	5.0
	C4-1	4.99 $\pm$ 0.1	3.9	5.3



(a) Fdac values of C1-1 after tunings with different injection charges.



(b) Fdac values of C3-1 after tunings different injection charges.



(c) Fdac values of C4-1 after tunings with different injection charges.

Figure A.1.: Fdac values of C1-1, C3-1 and C4-1 after tunings with different injection charges. The target threshold was $3000 e^-$ and the target ToT 10 for all tunings.

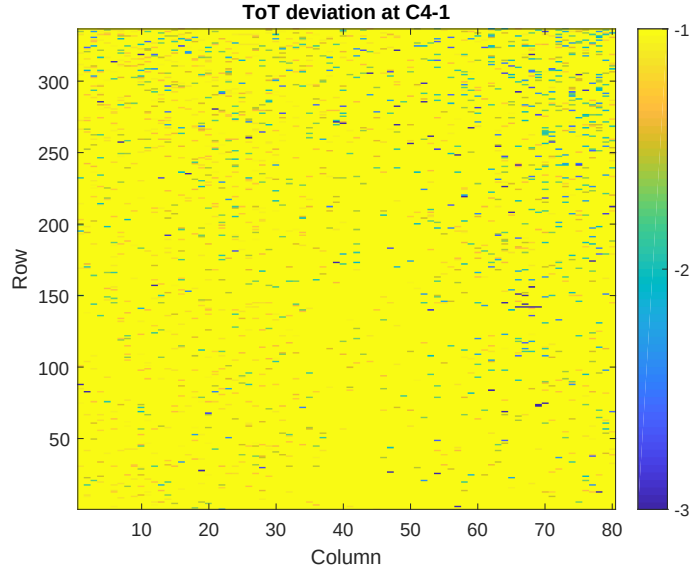


Figure A.2.: Deviation from the target ToT of 10 at C4-1 after a tuning to a target threshold of $1500 e^-$ with an injected charge of $16000 e^-$.

YARR

Table A.5.: Values of global configuration parameters after the tuning procedure. The tunings were all done with a target charge of $16000 e^-$. The values in the first row are the tuning parameters in the following order: target threshold in e^- /target ToT in 25 ns. 'std' means that the same configuration script as for RCE tunings was used while 'def' means that the YARR default configuration file was used.

Chip	global parameter	3000/10		3000/5		1500/5		1500/10	
		std	def	std	def	std	def	std	def
C1-1	PrmpVbpf	-	48	-	224	-	72	-	72
	Vthin_fine	-	165	-	243	-	175	-	175
C3-1	PrmpVbpf	1	28	120	208	160	48	160	48
	Vthin_fine	221	153	167	103	255	90	255	90
C4-1	PrmpVbpf	1	30	136	176	224	54	224	54
	Vthin_fine	255	177	187	255	82	100	82	100

Table A.6.: Values of global configuration parameters after tunings with different injection charges. The tunings were all done with the C4-1 chip and the standard configuration files. The number in the first row is the target charge, the target threshold was $3000 e^-$ and the target ToT 10.

	$20000 e^-$	$24000 e^-$
PrmpVbpf	16	40
Vthin_fine	241	227

Table A.7.: Threshold values after tuning with YARR using the standard configuration file. The values in the first column are the tuning parameters in the following order: target threshold in e^- /target ToT in 25 ns. The tunings were done with an injected charge of $16000 e^-$. The error given for the threshold is the standard deviation. The minimum and maximum is the middle of the outermost bins of the histograms in which 0.1% of all pixels were sorted.

tuning parameters	Chip	Threshold in e^-	Minimum	Maximum
3000/10	C3-1	2993 ± 66	2815	3165
	C4-1	3018 ± 77	2835	3185
3000/5	C3-1	2996 ± 99	2755	3245
	C4-1	3003 ± 129	2705	3285
1500/5	C3-1	1714 ± 324	1255	2635
	C4-1	1483 ± 67	1305	1635

Table A.8.: ToT values after tuning with YARR using the standard configuration file. The values in the first column are the tuning parameters in the following order: target threshold in e^- /target ToT in 25 ns. The tunings were done with an injected charge of $16000 e^-$. The error given for the threshold is the standard deviation. The minimum and maximum is the middle of the outermost bins of the histograms in which 0.1% of all pixels were sorted.

tuning parameters	Chip	Threshold in e^-	Minimum	Maximum
3000/10	C3-1	9.75 ± 0.7	7.9	11.1
	C4-1	9.83 ± 0.7	7.7	11.1
3000/5	C3-1	5.01 ± 0.1	4.3	5.5
	C4-1	5.03 ± 0.2	3.9	5.9
1500/5	C3-1	5.01 ± 0.1	4.1	5.3
	C4-1	5.03 ± 0.2	4.7	5.9

Table A.9.: Threshold values after tuning with YARR using the default configuration file. The values in the first column are the tuning parameters in the following order: target threshold in e^- /target ToT in 25 ns. The tunings were done with an injected charge of $16000 e^-$. The error given for the threshold is the standard deviation. The minimum and maximum is the middle of the outermost bins of the histograms in which 0.1% of all pixels were sorted.

tuning parameters	Chip	Threshold in e^-	Minimum	Maximum
3000/10	C1-1	2985 ± 45	2885	3075
	C3-1	2987 ± 43	2875	3085
	C4-1	2986 ± 46	2885	3065
3000/5	C1-1	3771 ± 386	2915	4635
	C3-1	2990 ± 52	2855	3105
	C4-1	3532 ± 342	2895	4325
1500/10	C1-1	1649 ± 225	1395	2235
	C3-1	1495 ± 48	1375	1595
	C4-1	1493 ± 62	1355	1595

Table A.10.: ToT values after tuning with YARR using the default configuration file. The values in the first column are the tuning parameters in the following order: target threshold in e^- /target ToT in 25 ns. The tunings were done with an injected charge of $16000 e^-$. The error given for the threshold is the standard deviation. The minimum and maximum is the middle of the outermost bins of the histograms in which 0.1% of all pixels were sorted.

tuning parameters	Chip	mean ToT in 25 ns	Minimum	Maximum
3000/10	C1-1	9.94 ± 0.6	8.7	13.7
	C3-1	9.97 ± 0.4	8.7	10.9
	C4-1	9.95 ± 0.4	8.7	10.7
3000/5	C1-1	5.02 ± 0.3	4.7	5.9
	C3-1	5.02 ± 0.2	4.7	5.9
	C4-1	5.01 ± 0.1	4.7	5.9
1500/10	C1-1	10.04 ± 0.6	8.9	13.7
	C3-1	9.98 ± 0.4	8.7	10.7
	C4-1	9.94 ± 0.5	7.5	10.7

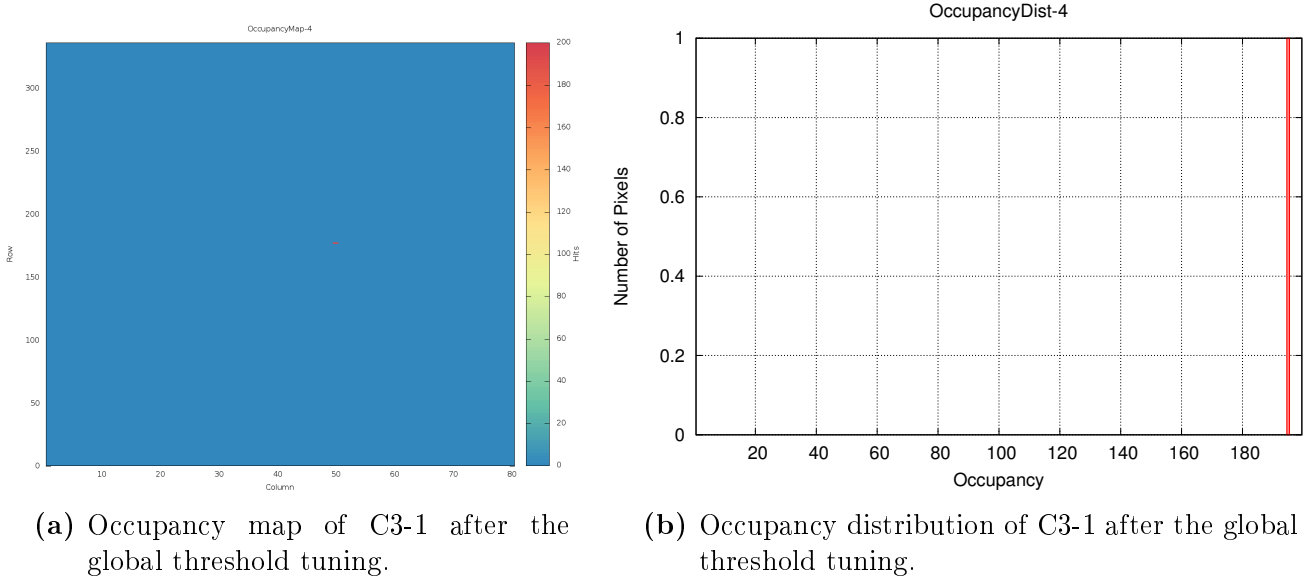


Figure A.3.: Occupancy map and distribution of C3-1 after the global threshold tuning. The tuning was done with a target threshold of $1500 e^-$ and a target ToT of 5 with an injected charge of $16000 e^-$.

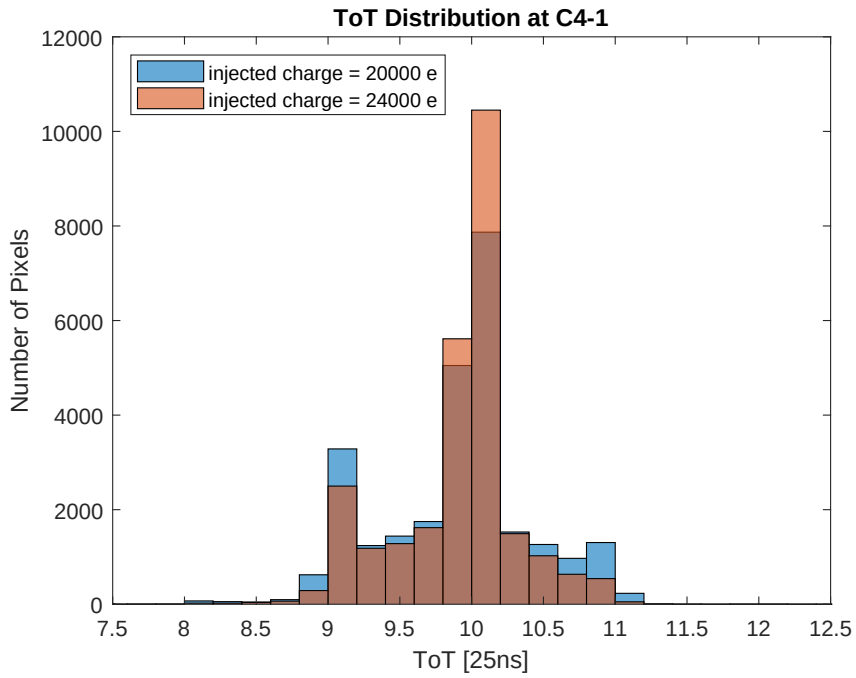
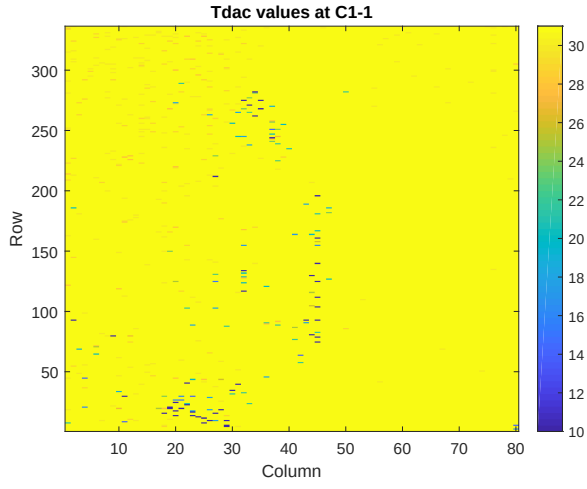
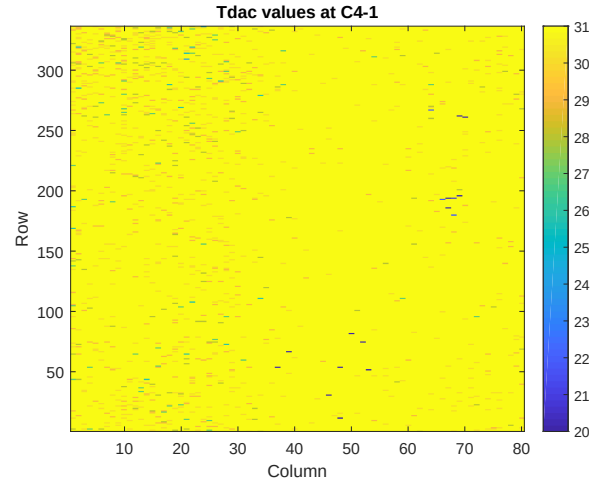


Figure A.4.: Results of ToT tunings with C4-1 at higher injection charges. The tunings were done with a target threshold of $3000 e^-$ and a target ToT of 10.



(a) Tdac setting at C1-1 after the tuning



(b) Tdac setting at C4-1 after the tuning

Figure A.5.: Tdac settings at C1-1 and C4-1 after the tuning with a target threshold of $3000 e^-$ and a target ToT of 5.

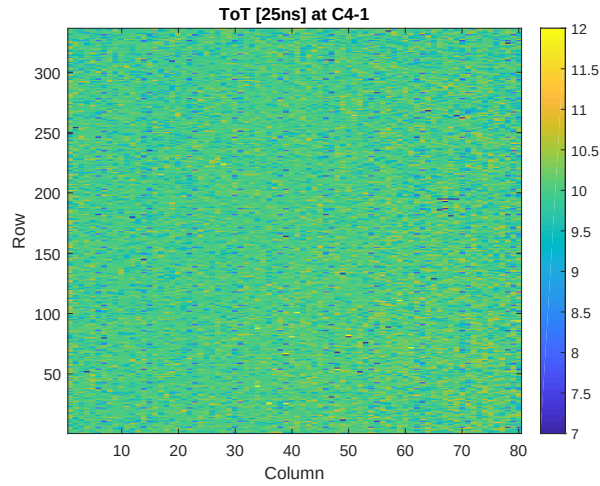
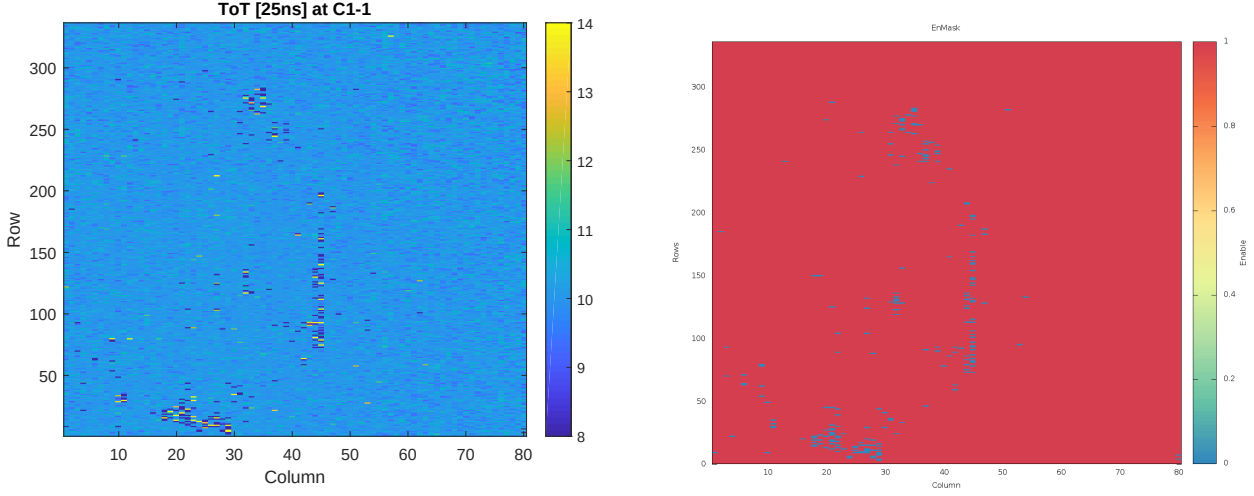


Figure A.6.: Per pixel results of a tuning to a ToT of 10 at C4-1 with a target threshold of $1500 e^-$ and an injected charge of $16000 e^-$



(a) Mean ToT at C1-1 after a tuning with a target threshold of $1500 e^-$ and a target ToT of 10.

(b) Enable Mask of C1-1. Pixels that are coloured blue showed a bad response and were disabled for further scans.

Figure A.7.: Mean ToT values and enable mask of C1-1

Comparison

Table A.11.: Threshold results from RCE. The scans were done with configuration files tuned by YARR to a target threshold of $1500 e^-$ and a target ToT of 10 with an injected charge of $16000 e^-$. The error given for the threshold is the standard deviation. The minimum and maximum is the middle of the outermost bins of the histograms in which 0.1% of all pixels were sorted.

Chip	Threshold in e^-	Minimum	Maximum
C1-1	1769 ± 205	1485	2275
C3-1	2529 ± 90	2325	2725
C4-1	1910 ± 83	1735	2075

Table A.12.: ToT results from RCE. The scans were done with configuration files tuned by YARR to a target threshold of $1500 e^-$ and a target ToT of 10 with an injected charge of $16000 e^-$. The error given for the ToT is the standard deviation. The minimum and maximum is the middle of the outermost bins of the histograms in which 0.1% of all pixels were sorted.

Chip	mean ToT in 25 ns	Minimum	Maximum
C1-1	10.97 ± 0.6	9.7	13.7
C3-1	9.39 ± 0.5	7.9	13.7
C4-1	10.14 ± 0.5	8.7	13.7

Table A.13.: Threshold results from YARR. The scans were done with configuration files tuned by RCE to a target threshold of $1500\,e^-$ and a target ToT of 10 with an injected charge of $16000\,e^-$. The error given for the threshold is the standard deviation. The minimum and maximum is the middle of the outermost bins of the histograms in which 0.1% of all pixels were sorted.

Chip	Threshold in e^-	Minimum	Maximum
C1-1	1591 ± 151	1405	1755
C3-1	833 ± 85	645	1015
C4-1	1429 ± 122	1215	1875

Table A.14.: ToT results from YARR. The scans were done with configuration files tuned by RCE to a target threshold of $1500\,e^-$ and a target ToT of 10 with an injected charge of $16000\,e^-$. The error given for the ToT is the standard deviation. The minimum and maximum is the middle of the outermost bins of the histograms in which 0.1% of all pixels were sorted.

Chip	mean ToT in 25 ns	Minimum	Maximum
C1-1	8.83 ± 0.6	7.5	13.7
C3-1	9.90 ± 0.4	8.5	10.7
C4-1	9.68 ± 0.6	7.7	11.3

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