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摘要

为了拓展新物理发现能力，欧洲核子中心的大型强子对撞机（LHC）计划于 2024 年进行一次主要升级。本博士论文的研究内容作为 LHC 上 ATLAS 实验的内层径迹探测器升级计划的一部分，目的在于研究一种新型单片式像素探测器。这种新型传感器基于高压/高阻 CMOS（HV/HR CMOS）工艺。相比较传统的复合式像素探测器，单片式探测器将会减少探测器物质质量（降低粒子多重散射），缩小像素尺寸（提高径迹重建精度）以及降低探测器成本（对于约 10m^2 的像素探测器，成本问题需要考虑）。

在 ATLAS HV/HR 合作组内，基于不同 HV/HR CMOS 工艺的多种原型传感器已被开发，比如 Global Foundry (GF) BCDlite 130 纳米工艺和 LFoundry (LF) 150 纳米工艺。为了获得不同 CMOS 工艺的相关电学特性以及粒子探测能力，已经通过三维计算机辅助设计（TCAD）模拟提取关键的电学参数，其中包括耗尽区分布、击穿电压、漏电流以及电容等。通过三维瞬态 TCAD 模拟，对传感器的电荷收集效率以及像素间电荷分享现象进行了详细研究。对于基于高阻衬底研发的原型传感器，传感器的保护环也通过二维 TCAD 模拟进行了优化设计。为了研究传感器因粒子辐照损伤而引起的性能变化，以上的 TCAD 模拟包括了非电离能损（NIEL）以及总电离剂量（TID）效应对传感器性能影响的研究。为了获得传感器在低温下的状态，传感器性能随温度的变化也通过 TCAD 模拟进行了研究。

同时我也参与了 HV/HR CMOS 原型芯片测试平台的研发。主要贡献在于 FPGA 固件的修改以及基于 C++ 和 python 的测试程序的编写。在 CPPM 组织并参与对 AMS 180 纳米，GF 130 纳米和 LF 150 纳米原型芯片的实验室电学性能表征测试。为研究 NIEL 和 TID 效应对不同原型芯片的影响，组织参与多次在 CERN 24 GeV 质子同步束流以及 X-射线放射源测试。前端放大器的线性以及信噪比通过外部测试脉冲进行了测试。甄别器的阈值可通过监测其输出信号进行调节。对原型芯片的测试主要集中在电子学和电荷收集部分的耐辐照强度方面。TID 对电子学的影响主要通过对前端放大器，甄别器以及模拟数据获取链的表征来研究：放大器输出幅度、甄别器阈值和噪声变化等等。NIEL 对衬底的影响主要通过对像素计数率、漏电流、 ^{55}Fe 和 ^{90}Sr 能谱等的测试来进行研究。HV/HR CMOS 传感器与 FE-I4（目前 ATLAS IBL 的像素读出芯片）的通信可以通过环氧树脂胶合来进行容性交流耦合。传感器与 FE-I4 的通信已通过 FE-I4 对传感器亚像素加权输出信号的读取进行测试。传感器的电子学占用率（occupancy）以及时间游走（time-walk）也通过 FE-I4 进行了测试。用于胶合的环氧树脂的均匀性以及厚度也通过 FE-I4 读取信号的幅度进行了研究。

除了参与 HV/HR CMOS 传感器的研究，同时也参与了对 FE-I4 GADC（generic ADC）的标定方法的研究并且进行了相关的验证测试。基于 ROOT 编写了一个简洁图形界面程序用来可视化标定过程以及结果。IBL 的所有 FE-I4 模块的 GADC 的标定数据已存储到 ATLAS IBL 的查找表中。

关键词：HL-LHC，ATLAS，硅像素探测器，高压/高阻 CMOS 传感器，耐辐照探测器，径迹探测器

Résumé

Prévue pour 2024, une série d'améliorations doit être apportée au grand collisionneur d'hadrons du CERN (LHC) de manière à élargir son potentiel de découverte de nouvelle physique. Cette thèse se situe dans la perspective des études d'amélioration du détecteur ATLAS dans ce nouvel environnement, et concerne une nouvelle technologie monolithique HV/HR CMOS qui pourrait être utilisée pour les détecteurs de traces centraux pixélisés. Cette technologie a le potentiel de permettre la réduction de l'épaisseur des détecteurs (réduction de la diffusion multiple), d'augmenter la granularité (plus de précision pour la reconstruction de traces...) ainsi que de réduire les coûts de production (un point particulièrement important dans le contexte d'un détecteur qui pourrait faire de l'ordre de 10 m^2).

Au sein de la collaboration HV/HR CMOS d'ATLAS, divers prototypes ont été développés en utilisant les technologies de différents partenaires industriels : GlobalFoundries (GF) BCDlite 130 nm et LFoundry (LF) 150 nm entre autres. Pour comprendre le comportement électrique et le potentiel de détection de ces technologies, des simulations 3D TCAD (Technology Computer Aided Design) ont été faites pour extraire le profil de la zone de déplétion, la tension de claquage, le courant de fuite ainsi que les valeurs capacitives des prototypes. Des simulations dynamiques 3D ont aussi été réalisées pour extraire l'efficacité de la collection de charge et le partage des charges générées dans le détecteur. Pour des prototypes de haute résistivité, la simulation 2D de l'implémentation des anneaux de garde a aussi été réalisée. Toutes ces simulations ont été faites en prenant en compte l'utilisation de ces détecteurs dans un contexte hautement radioactif, en introduisant les effets de dose totale (TID) ainsi que les effets de perte d'énergie non-ionisante (NIEL). L'effet de l'utilisation de ces technologies à basse température a aussi été évalué.

J'ai aussi contribué au développement de systèmes de tests pour les prototypes HV/HR CMOS, en modifiant des programmes FPGA et en écrivant des programmes de test en python et C++. J'ai organisé et participé à la caractérisation de prototypes AMS 180 nm, GF BCDLite 130 nm et LF 150 nm au CPPM, ainsi qu'à de multiples sessions de tests sous irradiation au CERN, sous rayon-X et aussi auprès du Synchrotron à Protons de 24 GeV, pour étudier les conséquences des effets TID et NIEL sur les prototypes. La linéarité et le rapport signal sur bruit ont pu être extraits en faisant des injections externes. L'uniformisation des seuils

des pixels a pu être réalisée. L'étude des effets TID sur l'électronique a été faite par caractérisation du préamplificateur, discriminateur et de la chaîne d'acquisition analogique : Mesure d'amplitude, d'évolution de seuil, de bruit, taux de SEU (Single Event Upset)... Les effets NIEL sur le silicium a été réalisée par étude de taux de comptage, évolution du courant de fuite, mesure de spectres ^{55}Fe et ^{90}Sr , etc... La possibilité de communication directe du prototype HV/HR CMOS par collage avec la puce FE-I4 (puce de lecture du la couche la plus interne du détecteur pixel d'ATLAS IBL) et transmission capacitive d'information a pu être démontrée, ainsi que le concept de sous-codage de pixels dans le prototype HV/HR CMOS avec décodage dans le FE-I4. Le taux d'occupation et le décalage temporel de plusieurs prototypes a aussi pu être mesuré de cette manière. Des questions de non-uniformité de collage (épaisseur de colle epoxy) ont aussi pu être abordées ainsi.

Outre ces études sur les détecteurs HV/HR CMOS, j'ai aussi pu contribuer au développement de procédures de calibration pour une section de diagnostic de la puce FE-I4, appelée GADC (Generic Analog-to-Digital Converter) et fait de nombreux tests en conséquence. J'ai développé une interface utilisateur basée sur ROOT pour visualiser les résultats de calibration, et extrait les données de calibration de tous les modules de l'IBL, la couche centrale pixélisée du détecteur ATLAS. Ces données font maintenant partie des tables de références du détecteur IBL actuellement en service dans ATLAS.

Mots clés : LHC Haute Luminosité, ATLAS, Détecteur pixel silicium, Technologie HV/HR CMOS, Détecteur tolérant aux radiations, Détecteur de traces

Abstract

A major upgrade to the Large Hadron Collider (LHC), scheduled for 2024 will be brought to the machine so as to extend its discovery potential. This PhD is part of the ATLAS program and aims at studying a new monolithic technology in the framework of the design of an upgraded ATLAS inner tracker. This new type of sensor is based on a HV/HR CMOS technology, which would potentially offer lower material budget (reduction of multiple scattering), reduced pixel pitch (increased precision for track reconstruction) and lower cost (a particularly important point for an approx. 10 m^2 detector) with respect to the traditional hybrid pixel detector concept.

Various prototypes have been developed using different HV/HR CMOS technologies from several industrial partners, within the ATLAS HV/HR collaboration, for instance Global Foundry (GF) BCDlite 130 nm and LFoundry (LF) 150 nm. In order to understand the electric behavior and the detection capabilities of these technologies, 3D Technology Computer Aided Design (TCAD) simulations have been performed to extract the depletion zone profile, the breakdown voltage, the leakage current as well as the capacitance of the prototypes. 3D transient simulations were also done in order to investigate the charge collection efficiency and charge sharing of the HV/HR CMOS pixels. For high resistivity substrate prototypes, a 2D guard-ring implementation was as well simulated. In order to explore the sensor performance degradation after irradiation, both Non-Ionizing Energy Loss (NIEL) and Total Ionizing Dose (TID) effects were taken into account when performing the above mentioned simulations. Temperature effects were also introduced in the DC simulations to understand the sensor behavior in a low temperature environment.

I have also participated in the test setup developments for the HV/HR CMOS prototypes. My main contributions concerned the modifications of the FPGA firmware and writing of test scripts using C++ and python. I have organized and participated in the laboratory characterizations for AMS 180 nm, GF 130 nm and LF 150 nm prototypes at CPPM, as well as in multiple test sessions of the devices under irradiation at CERN, either at the 24 GeV Proton Synchrotron irradiation center or at a high dose rate X-ray irradiation facility, to study the effects of NIEL and TID on the prototypes. The preamplifier linearity and signal-to-noise ratio were measured by using external test injections. The threshold tuning of the pixel matrix could be realized by using the monitor signal func-

tion of the discriminator. A main focus was the investigation of the irradiation hardness for both the electronics and the charge collection sensor. TID effect on the electronics could be performed by characterization of the pre-amplifier, discriminator and the overall analog acquisition chain : Amplitude measurement, threshold and noise evolution with respect to radiation, Single Event Upset rate, etc. . . NIEL effects on silicon were investigated by measuring the counting rate evolution with radiation, leakage current, ^{55}Fe or ^{90}Sr spectra, etc... The possibility of direct communication between the HV/HR CMOS sensor and the FE-I4 (the present readout IC of the innermost ATLAS pixel layer -IBL-) through simple gluing and capacitive coupling was also demonstrated, as well as the concept of sub-pixel encoding using weighted discriminator output in the HV/HR sensor followed by decoding in the FE-I4. The occupancy and time-walk of several prototypes were also measured through the FE-I4. Questions concerning the non-uniformity of the thickness of the epoxy glue used for the capacitive coupling between the sensor and the FE-I4 were also addressed in this way.

Beyond participating in the study of the HV/HR CMOS sensors, I have also contributed to calibration procedures of a diagnostic section of the FE-I4 called Generic Analog-to-Digital Converter (GADC) and performed the necessary corresponding measurements. I have developed a compact GUI to visualize the calibration results based on ROOT and extracted calibration constants for all the GADC of all IBL modules. This data is now part of the reference tables used for the IBL layer currently installed in the center of ATLAS.

Keywords : HL-LHC, ATLAS, Silicon pixel detector, HV/HR CMOS sensor, Radiation-hard detector, Tracking detector

Remerciements

Table des matières

Liste des figures	11
Liste des tableaux	18
Introduction	21
1 The LHC, ATLAS experiment and plans for upgrade	22
1.1 The Large Hadron Collider	22
1.2 The ATLAS experiment	24
1.2.1 Physics requirements	25
1.2.2 ATLAS layout	25
1.3 The ATLAS inner detector upgrade	35
2 Silicon properties and pixel sensor principles	39
2.1 Silicon physics and pn junction	39
2.1.1 Silicon properties	39
2.1.2 The pn-junction	47
2.2 Particles interaction with matter	51
2.3 Formation of signal in a sensor	53
2.4 Radiation effects	56
2.4.1 Bulk damage	57
2.4.2 Surface damage	62
3 ATLAS cylinder pixel detector technologies and HV/HR CMOS sensors	67
3.1 The hybrid pixel detector of ATLAS	67
3.1.1 Planar sensor for the initial ATLAS 3-layer pixel detector	68
3.1.2 Readout electronics	68
3.2 The IBL project	70
3.2.1 The IBL module	70
3.2.2 FE-I4 GADC calibration	77
3.3 HV/HR CMOS sensor	85
3.3.1 Smart diode array	85
3.3.2 HV2FEI4 prototype	87

4	TCAD simulation of HV/HR CMOS sensors	91
4.1	An introduction to TCAD simulation	91
4.1.1	Sentaurus Workbench	92
4.1.2	The Sentaurus Ligament and the Sentaurus Process	93
4.1.3	Sentaurus structure editor	93
4.1.4	Sentaurus mesh generation tools	95
4.1.5	Sentaurus device	95
4.1.6	Sentaurus visual	95
4.2	Physical models used for device simulation	96
4.2.1	Electrostatic potential and quasi-Fermi potential	96
4.2.2	Carrier transport	97
4.2.3	Mobility models	97
4.2.4	Generation-recombination	98
4.2.5	Traps and fixed charges	99
4.2.6	Radiation models	100
4.3	HV/HR sensor simulation	100
4.3.1	Type A technology simulation	101
4.3.2	Type B technology simulation	123
5	HV/HR CMOS detector test setup development and prototypes characterization	144
5.1	HV2FEI4 prototype introduction	144
5.1.1	HV/HR CMOS sensor	145
5.1.2	HV/HR CMOS sensor to FE-I4	149
5.1.3	HV2FEI4 test setup based on DE2	150
5.2	Characterization of HV/HR CMOS sensor prototypes	151
5.2.1	Characterizations of the AMS prototypes	151
5.2.2	GF prototype characterization	171
5.2.3	Characterization of LF CCPD prototypes	188
	Conclusion	214
	Bibliographie	215

Liste des figures

1.1	LHC accelerator complex	23
1.2	Integrated luminosity in 2011,2012 and 2015	24
1.3	Cut-away view of the ATLAS detector	26
1.4	ATLAS right-hand coordinate system	27
1.5	Cut-away view of the ATLAS ID	28
1.6	Side view of the pixel detector	29
1.7	Barrel pixel module schematic	29
1.8	Inner detector layout schematic	30
1.9	SCT modules	31
1.10	Cut-away view of the ATLAS calorimeter system	32
1.11	Cut-away view of the ATLAS muon spectrometer	33
1.12	Forward detectors of ATLAS	33
1.13	Trigger scheme of ATLAS	34
1.14	LHC upgrade schedule beyond LS1	35
1.15	HL-LHC radiation environment	37
1.16	The baseline layout of ITk	37
2.1	Intrinsic silicon	40
2.2	Silicon doping diagram	42
2.3	Thermal-equilibrium silicon generation and recombination diagram	42
2.4	Excess carrier generation and recombination diagram	43
2.5	Random movement of carriers with (right) and without (left) applied electric field	45
2.6	Carriers mobility vs. doping concentration	46
2.7	Resistivity vs. doping concentration. Phosphorous and boron doped silicon.	46
2.8	Carriers velocity vs. electric field in silicon	47
2.9	A conceptual view of pn junction	48
2.10	Energy band of a pn junction in thermal equilibrium	49
2.11	Junction capacitance vs. voltage	51
2.12	Critical electric field vs. doping concentration	51
2.13	Muon energy deposition in copper	52
2.14	Straggling functions in silicon of 500 MeV pions	53
2.15	Cross section of a sensor diagram	53

2.16	Weighting field and induced current for a pixel [37]	55
2.17	Electrode size for weighting potential calculation	55
2.18	Weighting potential	56
2.19	Displacement damage cross section in silicon	58
2.20	Diagram of point defects in n-type silicon	59
2.21	Effective doping concentration as a function of fluence	61
2.22	Diagram of energy band for a NMOS structure	62
2.23	Fraction of yield as a function of e-field in oxide	63
2.24	Diagram of E' center	64
2.25	Si/SiO_2 interface formation for different orientations	65
2.26	Diagram for P_b and P_{b0} centers	65
2.27	TID effect in STI	66
3.1	Schematic of a hybrid pixel detector	67
3.2	Schematic of ATLAS planar sensor	68
3.3	Schematic of the FE-I3 readout chip	69
3.4	Photograph of IBL installation	70
3.5	IBL layout in $r\Phi$ view	71
3.6	IBL double-chip modules size and picture	71
3.7	Comparison of the existing ATLAS pixel and the IBL pixel	72
3.8	3D sensor schematics	73
3.9	A comparison of the FE-I4 size and the FE-I3 size	74
3.10	FE-I4 functional diagram [82]	75
3.11	FE-I4 analog block schematic	76
3.12	Pixel digital region (PDR) diagram	76
3.13	Diagram of the GADC	77
3.14	The measured VDDA and GDAC output vs. VrefAnTune DAC	78
3.15	Scan of GADCout vs. PlsrDAC	79
3.16	The GADC output of the VDDA/2 vs. the VrefAnTune DAC	80
3.17	The GADC output of the PlsrDAC and fit result	80
3.18	VDDA variation with temperature	81
3.19	VDDA variation with power consumption	82
3.20	Calibration results depending on temperature	82
3.21	Calibration results depending on power consumption	83
3.22	LSB and pedestal distribution of ASSY data	84
3.23	LSB and pedestal distribution of FLEX data	84
3.24	HV CMOS sensor diagram	85
3.25	Simplified electronics schematic for the HV/HR CMOS sensor	86
3.26	The schematic of the preamplifier	87
3.27	The feedback loop of the preamplifier	88
3.28	The schematic of the discriminator	88
3.29	HV2FEI4 test assembly	89
3.30	A unit readout cell of the HV2FEI4 test assembly	89

4.1	A general TCAD simulation flow	91
4.2	Main panel of Sentaurus Workbench	92
4.3	Sentaurus Ligament overview	93
4.4	Main windows of Ligament Layout	94
4.5	A 3D structure in the Sde	94
4.6	A 3D HV/HR CMOS device as seen in the Sentaurus Visual GUI	96
4.7	TID simulation procedure	99
4.8	Heavy ion impinging process	100
4.9	Pixel layout in cadence	101
4.10	Pixel layout in sentaurus	102
4.11	3D simulation devices for the type A technology	102
4.12	Depletion of the standard pixel size for type A technology	103
4.13	Depleted depth vs. HV	104
4.14	Depletion of the intermediate pixel size for type A technology	104
4.15	Leakage current and capacitance of standard size pixels for type A technology	105
4.16	Leakage current and capacitance comparison between standard size and the intermediate size pixel	106
4.17	E-field distribution of the standard size pixel for the type A technology	106
4.18	E-field values in the Y-axis and Z-axis	107
4.19	MIPs induced current of the standard size pixels	108
4.20	MIPs induced current of the standard size and intermediate size pixels	108
4.21	Avalanche breakdown induced by MIPs	109
4.22	MIPs induced breakdown	109
4.23	Charge collection simulation region	110
4.24	Impinging position in the simulation region	110
4.25	MIPs responses with different impinging position in log scale (HV=-30V)	111
4.26	Collected charge within 5ns	111
4.27	MIPs responses with different impinging position with linear scale (HV=-30V)	112
4.28	Integrated collected charges (HV = -30V)	112
4.29	Electron current density variation in position 1	113
4.30	Hole current density variation in position 1	114
4.31	Electron current density variation in position 10	115
4.32	Hole current density variation in position 10	116
4.33	Charge collection profile with log scale (HV=-30V)	117
4.34	Leakage current vs. HV with NIEL effect for fluence of 0, 1×10^{14} , 1×10^{15} and $1 \times 10^{16} \text{ } n_{eq} \cdot \text{cm}^{-2}$	118
4.35	MIPs responses with NIEL effect for an impinging particle in position 1	119
4.36	Charge collection profile with NIEL effect	120
4.37	Leakage current with temperature effect	121
4.38	MIPs responses with temperature effect	122

4.39 The depletion region evaluations for the values of HV from -1 V to -100 V	123
4.40 Depleted depth vs. HV	124
4.41 Electric field distribution for type B technology	124
4.42 Leakage current vs. HV with NIEL effect	125
4.43 Leakage current at -6°C	126
4.44 DNW capacitance vs. HV (Type B VerA)	127
4.45 AC simulation structure	127
4.46 Total input capacitance vs. HV (LF VerA)	128
4.47 Transient simulation configuration and the collected charges	129
4.48 DNW responses for impinging particles (HV = -50 V)	129
4.49 Electron current density variation in position 1	130
4.50 Hole current density variation in position 1	131
4.51 Electron current density variation in position 10	132
4.52 Hole current density variation in position 10	133
4.53 Charge collection profile (LF VerA)	134
4.54 Charge collection at different temperatures	135
4.55 3D device for versionB simulation	135
4.56 Cut-plane of versionB doping	136
4.57 Leakage current vs. HV	136
4.58 Electric field of vesionB	137
4.59 LF CPIX V1 guardring layout	138
4.60 LF CPIX V1 simulation of the structure	138
4.61 The leakage currents of DNW-pixel and PW-pixel	139
4.62 The electric field distribution for both topside and backside biases.	139
4.63 Guard-ring simulation scenarios	140
4.64 The leakage currents for the DNW-pixel and for the PW-pixel for the top-side bias case	141
4.65 The leakage currents for the DNW-pixel and for the PW-pixel for the backside bias case	141
4.66 The electric field distribution of scenario (B)	142
4.67 The electric field distribution of scenario (C)	142
5.1 Picture of the layout of GF chip	145
5.2 Amplifier stage diagram of matrix pixel	146
5.3 Discriminator stage diagram of matrix pixel	146
5.4 Configuration diagram of the GF prototype	147
5.5 Structure of the six-pixel unit cell of the GF prototype	148
5.6 Row and column control bits	148
5.7 HV CMOS to FE-I4 diagram	149
5.8 Signal AC coupled to FE-I4	149
5.9 HVC MOS test setup diagram	150
5.10 A picture of the AMS V1 prototype	151

5.11 Responses of the preamplifier and discriminator of type A pixel to a 1 V external injection	152
5.12 Linearity of preamplifier (type A pixel)	152
5.13 Threshold and noise distributions for the matrix	153
5.14 Threshold and noise distributions of the type A and the type B pixels.	154
5.15 Threshold and noise distributions of the “right” and “left” pixels	154
5.16 Location map of the assemblies	155
5.17 The counting rate of preamplifier of AMS V1 as a function of the dose	156
5.18 CCPD2 responses for external injection after 3 weeks annealing	156
5.19 The snapshots of the preamplifier and discriminator responses in one PS spill	157
5.20 The layout of AMS V2	158
5.21 The responses of the preamplifier and discriminator for the rad-hard pixel	159
5.22 The responses of the preamplifier and discriminator for the normal pixel	159
5.23 The amplitude of the preamplifier of AMS V2 vs. the dose for two different pixels types	160
5.24 Threshold and noise for normal and rad-hard pixels	161
5.25 The leakage current as a function of dose	161
5.26 The layout of AMS V3	162
5.27 The amplitudes of the preamplifiers as a function of injection voltages	163
5.28 ^{55}Fe and ^{90}Sr signals detected by the “ATLAS-standard” pixel	163
5.29 ^{55}Fe and ^{90}Sr spectra of the “ATLAS-standard” pixel	164
5.30 ^{55}Fe and ^{90}Sr signals detected by the “CLIC” pixel	164
5.31 ^{55}Fe and ^{90}Sr spectra of the “CLIC” pixel	165
5.32 The layout of AMS V4	165
5.33 Responses of the “ATLAS-satandard” pixels with linear feedback transistor and amplitude encoding discriminator	166
5.34 Proton irradiation test setups for the AMS V4	167
5.35 Screenshot of preamplifier and discriminator responses in beam position	167
5.36 The amplitude and counting rate as a function of does for AMS V4	168
5.37 The amplitude of the preamplifiers of AMS V4 as a function of the dose	169
5.38 The 1 V injection and ^{55}Fe spectra taken by the pixel with ELT feedback transistor after 1 GRad X-ray irradiation	170
5.39 The snapshot and spectrum of ^{90}Sr of the pixel with ELT feedback transistor after 1 GRad X-ray irradiation	170
5.40 Leakage current variations with X-ray irradiation	171
5.41 The ^{90}Sr and ^{90}Sr signals detection of the GF prototype	172
5.42 Probe station platform	173
5.43 Probed GF V1 chip	173
5.44 Sin and Sout monitored by oscilloscope	173
5.45 Shift register scan for GF chips	174

5.46 Amplitude of matrix pixels vs. dose	174
5.47 Linearity of matrix pixel at different dose levels	175
5.48 The amplitudes of the “Along-pixel” and the “DNW-pixel”	175
5.49 Leakage current as a function of the dose	176
5.50 Test-DAC outputs at 800 and 1000 MRads	177
5.51 Pbias variation as a function of dose	177
5.52 The threshold and leakage current of the GF transistors as a function of dose	178
5.53 The correspondence between FE-I4 and GF chip	179
5.54 TDAC tuning to 1500 electrons for TH	179
5.55 FDAC tuning to "11" is equivalent to 20,000 electrons	180
5.56 FEI4 trigger diagram for the HV2FEI4 assembly test	180
5.57 FE-I4 occupancy with different Lvl1 trigger delays	181
5.58 FE-I4 lvl1 ID with different Lvl1 trigger delays	181
5.59 The GF HV2FEI4 assembly occupancy measurement	182
5.60 Timing and TOT distributions of the GF HV2FEI4 assembly	182
5.61 The Lvl1 ID distributions for 1V injections with different sensor thresholds.	183
5.62 The counting rate and lvl1 ID as a function of TH depending on the injections	183
5.63 TOT value depending on serial input capacitors	184
5.64 Unit readout cell of HV2FEI4 assembly	184
5.65 One pixel readout of unit cell	185
5.66 Sum signal of pixel “1”, “3”, “5”	185
5.67 Sum signal of pixel “2”, “4”, “6”	185
5.68 Summed signals of the 3 sub-pixels	186
5.69 TOT with weighted HV CMOS outputs	186
5.70 TOT vs. weighted HV CMOS output and external voltage injection	187
5.71 Hitting rate vs. TH	187
5.72 The threshold map and distribution before tuning	188
5.73 The threshold map and distribution after tuning	189
5.74 Local DAC map after threshold tuning	189
5.75 LF VA layout	189
5.76 LF VB layout	190
5.77 LF prototype floorplan	190
5.78 Placement of pixel flavors of VA and VB	191
5.79 LF CCPD guardring layout	191
5.80 LF CCPD VA analog scan	192
5.81 Threshold and noise distributions before tuning for ELT pixels before TDAC tuning, one pixel enabled mode.	193
5.82 Threshold and noise maps before tuning for ELT pixels before TDAC tuning, one pixel enabled mode.	193

5.83 Threshold and noise distributions after tuning for ELT pixels before TDAC tuning, one pixel enabled mode.	194
5.84 Threshold and noise maps after tuning for ELT pixels before TDAC tuning, one pixel enabled mode.	194
5.85 Threshold and noise distributions before tuning for Lin pixels before TDAC tuning, one pixel enabled mode.	195
5.86 Threshold and noise maps before tuning for Lin pixels before TDAC tuning, one pixel enabled mode.	195
5.87 Threshold and noise distributions after tuning for Lin pixels before TDAC tuning, one pixel enabled mode.	196
5.88 Threshold and noise maps after tuning for Lin pixels before TDAC tuning, one pixel enabled mode.	196
5.89 Threshold and noise distributions before tuning for ELT pixels before TDAC tuning, all pixels enabled mode.	197
5.90 Threshold and noise maps before tuning for ELT pixels before TDAC tuning, all pixels enabled mode.	197
5.91 Threshold and noise distributions after tuning for ELT pixels before TDAC tuning, all pixels enabled mode.	198
5.92 Threshold and noise maps after tuning for ELT pixels before TDAC tuning, all pixels enabled mode.	198
5.93 Threshold and noise distributions before tuning for Lin pixels before TDAC tuning, all pixels enabled mode.	199
5.94 Threshold and noise maps before tuning for Lin pixels before TDAC tuning, all pixels enabled mode.	199
5.95 Threshold and noise distributions after tuning for Lin pixels before TDAC tuning, all pixels enabled mode.	200
5.96 Threshold and noise maps after tuning for Lin pixels before TDAC tuning, all pixels enabled mode.	200
5.97 TDAC values comparison between one pixel enable and all pixel enable mode.	201
5.98 Leakage current variations with proton irradiation of the LF VA prototype	202
5.99 LF CCPD VA counting rate at room temperature as a function of TID	202
5.100(a) : TH as a function of dose. (b) : Noise as a function of dose.	203
5.101LF CCPD VA responses after annealing	203
5.102LF CCPD VA low temperature proton test setup	204
5.103Leakage current as a function of dose for both samples at $-20^{\circ}C$.	204
5.104Evaluation of the counting rate as a function of dose for both samples at $-20^{\circ}C$.	205
5.105Threshold as a function of dose for both samples at $-20^{\circ}C$ in 24 GeV protons irradiation environment.	206
5.106Noise as a function of dose for both samples at $-20^{\circ}C$	206
5.107Threshold and noise distributions for board 55 at 5 MRads, one pixel enabled mode.	207

5.108	Threshold and noise maps for board 55 at 5 MRads, one pixel enabled mode.	207
5.109	Threshold and noise distributions for board 55 at 100 MRads, one pixel enabled mode.	208
5.110	Threshold and noise maps for board 55 at 100 MRads, one pixel enabled mode.	208
5.111	Threshold and noise distributions for board 56 at 5 MRads, one pixel enabled mode.	209
5.112	Threshold and noise maps for board 56 at 5 MRads, one pixel enabled mode.	209
5.113	Threshold and noise distributions for board 56 at 100 MRads, one pixel enabled mode.	210
5.114	Threshold and noise maps for board 56 at 100 MRads, one pixel enabled mode.	210
5.115	CCPD VA threshold and noise variation as a function of dose.	211
5.116	CPIX reticles	211

Liste des tableaux

1.1	The design parameters of the LHC	22
1.2	Performance goals of the ATLAS detector. The unit for p_T and E are GeV.	26
1.3	Inner tracker active area and channel count	38
2.1	Radiation interaction characteristics	57
2.2	Hardness factor for two irradiation facilities	59
2.3	Characteristics of some defects in silicon	60
2.4	Ionizing conversion factor for various materials	63
3.1	GADC inputs	77
4.1	p-type silicon NIEL induced trap model	99
4.2	Leakage current considering NIEL effect (HV=-30V)	118
4.3	Collected charge taking into account NIEL effect for an impinging particle in position 1 (HV=-30V)	119
4.4	Charge collection profiles with NIEL effect (HV=-30V)	120
4.5	Leakage current with temperature effect (HV=-30V)	121
4.6	Leakage current with NIEL effect (HV=-50V)	125
4.7	Leakage current at $-6\text{ }^{\circ}\text{C}$ (HV=-50V)	126

4.8	Charge collection profiles with NIEL effect (HV=-50V)	134
5.1	List of HV/HR prototypes	144
5.2	Bias block of the GF prototype	147
5.3	Current consumption before and after X-ray irradiation	169
5.4	Transistor size	177
5.5	Leakage current at 100 MRads	205

Introduction

The Large Hadron Collider of the “Centre Européen de Recherche Nucléaire” (CERN, Geneva, Switzerland) is the flagship collider for high energy physics nowadays. It is the primary research apparatus allowing the extension of our knowledge of the infinitely small, as it allows the generation of particles in a higher energy regime with respect to previous generation colliders. ATLAS is one of four main detectors built on the LHC ring, with the goal of finding new particles, as for example the Standard Model Higgs boson, an essential ingredient to incorporate mass into the Standard Model of particles, or particles that would reveal a possible extension to the Standard Model (super-symmetry, new bosons. . .). In 2012, two years after the first proton-proton collisions, a new particle has been discovered at the LHC with a mass of $125.09 \pm 0.21(stat.) \pm 0.11(syst.) GeV$, its properties being compatible with those of a Higgs boson. Although this news has been received with great enthusiasm by the scientific international community, it also opens the path to deeper studies of this new particle and its decay modes.

To reach this goal, the LHC will gradually raise the collision energy of its protons in the coming years, which will enhance the production cross-section of the particles under study, and will also increase the luminosity of the machine. This will allow acquiring faster more statistics concerning the studied decay channels. This higher collision rate at a higher energy will directly translate into a higher number of particle tracks to treat per unit time, as well as higher received doses, in particular for the central detectors. For this challenging environment, new vertex detectors are under development, their main characteristics being a higher tolerance to radiation, light structures and improved granularity (to reduce multiple scattering and enhance particle trajectories reconstruction), and the possibility to cope with a higher number of particle hits per unit time.

A new pixel layer which was inserted in 2013 inside the initial 3-layer pixel detector operating in the heart of ATLAS. This cylindrical layer, the so-called IBL (which stands for “Insertable B-Layer”), is located about 3.7 cm away from the beams and should enhance ATLAS b-tagging and vertexing ability. It is based on a traditional hybrid pixel technology, with detection units bump-bonded through 20 μm diameter SnAg bumps to pixelated electronics units developed in a 130 nm CMOS process.

But the 130 nm CMOS technology is not adapted to the future environment of the innermost layers at an upgraded High Luminosity LHC. This technology

prevents the reduction of the pixel size well under $50 \times 250 \mu m^2$, which was the size chosen for the IBL pixels. Several R&D paths are followed to try and find a technology adapted to the needs of an upgraded ATLAS pixel detector : hybrid pixel using a smaller feature size IC (CMOS 65 nm), pixel based on 3D electronics and finally a new approach consisting in putting aside the standard hybrid pixel approach and targeting a monolithic pixel process. This technology integrates in a single layer the sensing part together with the electronics, which has for benefits a simplification of the module concept, a reduction of the costs, and allows designing smaller size pixels while having a rather strong signal and a high tolerance to radiation.

The research work presented here is part of this project and has for goal to study this new monolithic technology in the framework of the design of an upgraded ATLAS detector. The LHC, the ATLAS experiment and their foresee upgrades will be described in Chapter 1. In Chapter 2, the silicon physics and the pixel sensor operation concepts will be discussed. The initial ATLAS 3-layer pixel detector technologies, the insertable b-layer project and the principle of the HV/HR CMOS sensors will be introduced in Chapter 3. The conceptual simulations for the HV/HR CMOS sensors by using TCAD tools will be discussed in Chapter 4. Finally, the characterizations in particular with respect to radiation in a high radiation environment of several HV/HR CMOS prototypes will be given in Chapter 5.

1 The LHC, ATLAS experiment and plans for upgrade

1.1 The Large Hadron Collider

The Large Hadron Collider[1] (LHC) is the world's largest and most powerful particle accelerator. The LHC is a two-ring superconducting hadron accelerator and collider installed in the existing 26.7 km tunnel that was constructed between 1984 and 1989 for the CERN LEP[2] machine. The LEP tunnel has eight straight sections and eight arcs and lies between 45 m and 170 m below the surface on a plane inclined at 1.4% sloping towards the Léman lake. The LHC first started operation on 10 September 2008, and remains the latest addition to CERN's accelerator complex. The LHC design parameters are summarized in Table 1.1.

Parameter	Value	unit
Circumference	27	km
Beam energy	7	TeV
Dipole magnetic	8.3	T
Protons per bunch	1.15×10^{11}	
Bunches per beam	2808	
Nominal luminosity	1×10^{34}	$cm^{-2}s^{-1}$

Table 1.1 – The design parameters of the LHC

Acceleration of the protons take place in various stages of an accelerator complex as shown in Figure 1.1. When the protons have reached the intended collision energy, the two beams are made to collide head to head in the center of the four detectors (ALICE[3], ATLAS[4], CMS[5] and LHCb[6]) with an 8 TeV center-of-mass energy.

One of the goals of the LHC was to allow physicists to prove or disprove the existence of the theorized Higgs boson. It is a particle that gives mass to other particles and is part of the Standard Model (SM) in physics. Meanwhile, the LHC can also be used to explore the new particles predicted by extension of the

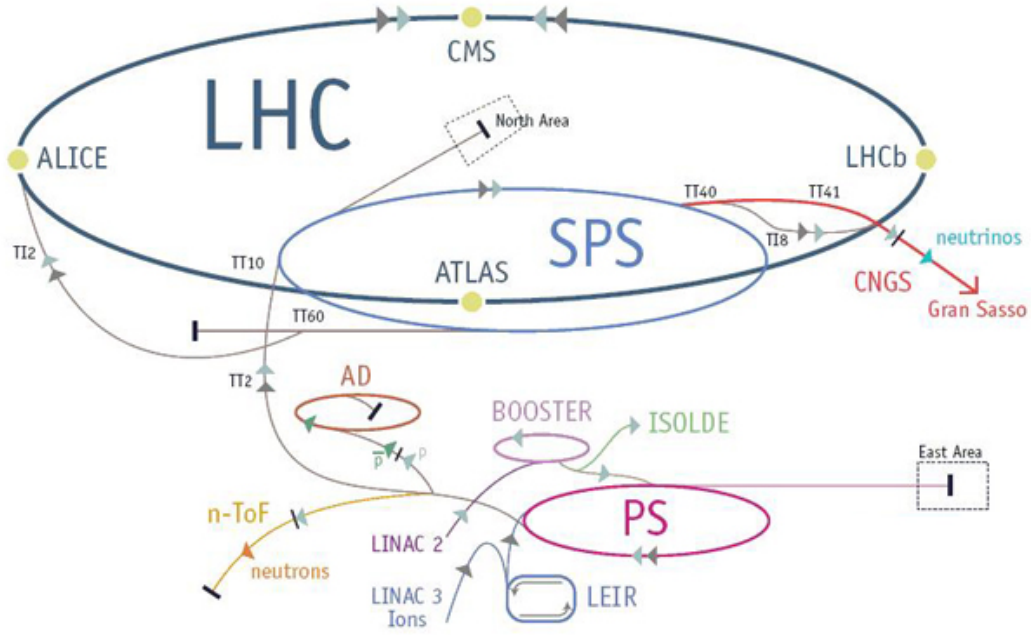


Figure 1.1 – LHC accelerator complex

SM physics for instance the supersymmetry. A main achievement of the ATLAS and CMS experiments at LHC was the confirmation of the evidence of a Higgs boson in 2013. The LHC is expected to address some of the unsolved questions of physics, advancing human understanding of physical law of nature.

A second key parameter of the collision, besides the collision energy, is the event rate, given by :

$$N_{event} = L \cdot \sigma_{event} \quad (1.1)$$

where σ_{event} is the cross section for the event under study and L the collision luminosity. The luminosity can be simply given by :

$$L = \frac{N^2 \cdot F}{t \cdot S_{eff}} \quad (1.2)$$

where N is the number of protons in a bunch, F the geometric luminosity reduction factor, t the time between bunches (25 ns) and S_{eff} the effective section of collision which depends on the cross section of the bunches. The factor F can be described by,

$$F = 1 / \sqrt{1 + \left(\frac{\sigma_s \phi}{\sigma_t} \right)^2} \quad (1.3)$$

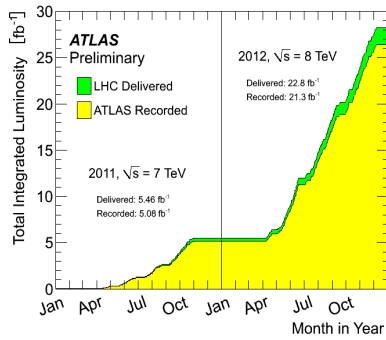
where σ_s is the longitudinal bunch length, σ_t the transverse bunch size in the plane of the crossing angle and ϕ the total crossing angle. F is around 0.95 for

the LHC. The formula for S_{eff} is given by :

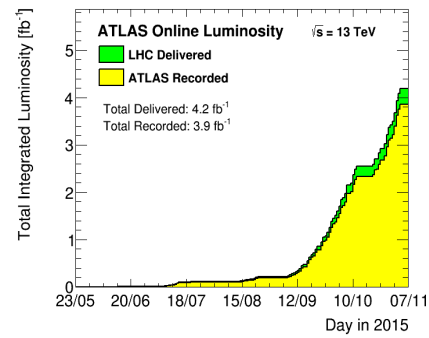
$$S_{eff} = 4 \cdot \pi \cdot \sigma^2 \quad (1.4)$$

with $\sigma = 16 \mu m$, the transversal size of the bunches at the interaction point in the detector. The bunches consist by design of 1.15×10^{11} protons, which results in the LHC designed luminosity of $10^{34} cm^{-2} \cdot s^{-1}$.

The LHC started data taking on November 23, 2009 at the energy of 450 GeV. The beam energy was then increased to 3.5 TeV (7 TeV center-of-mass energy) in 2010. In 2012, the collision energy reached 8 TeV. Figure 1.2a illustrates the



(a) Integrated luminosity in 2011 and 2012 [7]



(b) Integrated luminosity in 2015 [8]

Figure 1.2 – (a) : the integrated luminosity of the ATLAS in 2011 and 2012. (b) : the integrated luminosity of the ATLAS in 2015.

cumulative luminosity versus time delivered to ATLAS in green and recorded by ATLAS in yellow in 2011 and 2012. The LHC have started the RUN 2 period with 13 TeV collision energy in 2015, and the cumulative luminosity for 2015 is shown in Figure 1.2b.

1.2 The ATLAS experiment

The high interaction rates, the high radiation doses, the particle multiplicities and energies, as well as the requirements for precision measurements have set new standards for the design of particle detectors. Two general purpose detectors, ATLAS (A Toroidal LHC ApparatuS) and CMS (Compact Muon Solenoid), have been built for probing proton-proton (pp) and nucleus-nucleus (A-A) collisions[4]. We will focus on the ATLAS detector physics requirements as well as on its layout in Sections 1.2.1 and 1.2.2.

1.2.1 Physics requirements

With respect to previous generation colliders, the increased cross-sections and high luminosity will allow to perform high precision tests of QCD, electroweak interactions and flavour physics at the LHC. Searching for the Standard Model (SM) Higgs boson has been used as a benchmark to establish the performance of important sub-systems of ATLAS. The production and decay mechanisms of the Higgs boson, H , depends on its mass. The natural width of the Higgs is only a few MeV at low masses ($< 2m_Z$). Therefore, the observed width is defined by the instrumental resolution. New heavy gauge bosons W' and Z' could be inspected for masses up to ~ 6 TeV. In order to investigate their leptonic decays, the p_T -range of a few TeVs with high resolution charge identification and energy measurements are needed.

The nature of pp collisions imposes another difficulty. QCD jet production cross sections dominate over the rare processes mentioned above, requiring the identification of experimental signatures characteristic of the physics processes in question, such as E_T^{miss} or secondary vertices[9]. Identifying such final states for these rare processes requires a good particle-identification capabilities of the detector.

These physics goals can be turned to a set of general design criteria for the ATLAS detector :

- a) Fast, radiation hard electronics and sensors, and high granularity to reduce the overlapping events.
- b) High charged particle momentum resolution and reconstruction efficiency capability for the inner detector. Secondary vertices observation is needed for offline tagging of τ -leptons and b-jets.
- c) Large acceptance in pseudo-rapidity with almost full azimuthal angle coverage everywhere.
- d) High quality electron and photon measurements for electromagnetic calorimetry. Precision jets and missing transverse energy measurements for hadronic calorimetry.
- e) High momentum muon measurements.
- f) Efficient triggering on low transverse momentum objects with sufficient background rejection.

1.2.2 ATLAS layout

The ATLAS detector is a multi-purpose detector at the LHC. The overall schematic of the ATLAS experiment is shown in Figure 1.3. The dimensions of the detector are ~ 25 m in height and ~ 44 m in length. The overall weight of the detector is approximately 7000 tonnes. The main performance goals of this detector are listed in Table 1.2.

The ATLAS detector is a forward-backward symmetric instrument with respect

to the interaction point. Magnetic fields are required in order to identify charge sign and measure momentum. As a consequence, close to the interaction point, a solenoid provides 2 T for the inner detector. A barrel toroid and two end-cap toroids provide approximately 0.5 T and 1 T for the muon detectors, respectively. The ATLAS detector consists of an inner tracker, an electromagnetic calorimeter, a hadronic calorimeter, a muon spectrometer and forward detectors. These detector blocks as well as the trigger system will be introduced in this section.

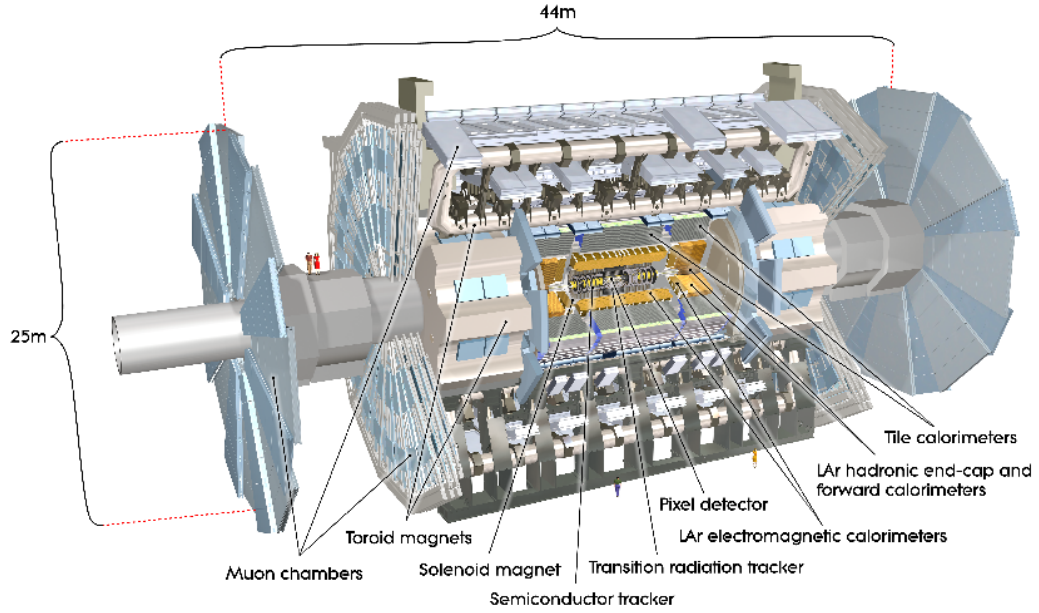


Figure 1.3 – Cut-away view of the ATLAS detector [4]

Detector component	Required resolution	η coverage	
		Measurement	Trigger
Tracking	$\sigma_{p_T}/p_T = 0.05\%p_T \oplus 1\%$	± 2.5	
EM calorimetry	$\sigma_E/E = 10\%/\sqrt{E} \oplus 0.7\%$	± 3.2	± 2.5
Hadronic calorimetry (jets)	$\sigma_E/E = 50\%/\sqrt{E} \oplus 3\%$	± 3.2	± 3.2
barrel and end-cap	$\sigma_E/E = 100\%/\sqrt{E} \oplus 10\%$	$3.1 < \eta < 4.9$	$3.1 < \eta < 4.9$
forward			
Muon spectrometer	$\sigma_{p_T}/p_T = 10\% \text{ at } p_T = 1 \text{ TeV}$	± 2.7	± 2.4

Table 1.2 – Performance goals of the ATLAS detector. The unit for p_T and E are GeV.

The ATLAS coordinate system is depicted in Figure 1.4. The origin of the coordinate is defined by the nominal collision point. The ATLAS coordinate system is a right-hand coordinate system with the z-axis along the beam direction and

the x-axis pointing towards the center of the LHC tunnel. The y-axis is tilted slightly with respect to vertical from the general tilt of the tunnel. The side-A is defined as the positive direction of the z-axis and the side-C is the negative direction of the z-axis. We use pseudorapidity to describe angles in the ATLAS. Pseudorapidity is defined as,

$$\eta = -\ln \tan\left(\frac{\theta}{2}\right) \quad (1.5)$$

where θ is the polar angle of the particle direction measured from the positive z-axis. The transverse momentum p_T , the transverse energy E_T , and the missing transverse energy E_T^{miss} are defined in the x-y plane.

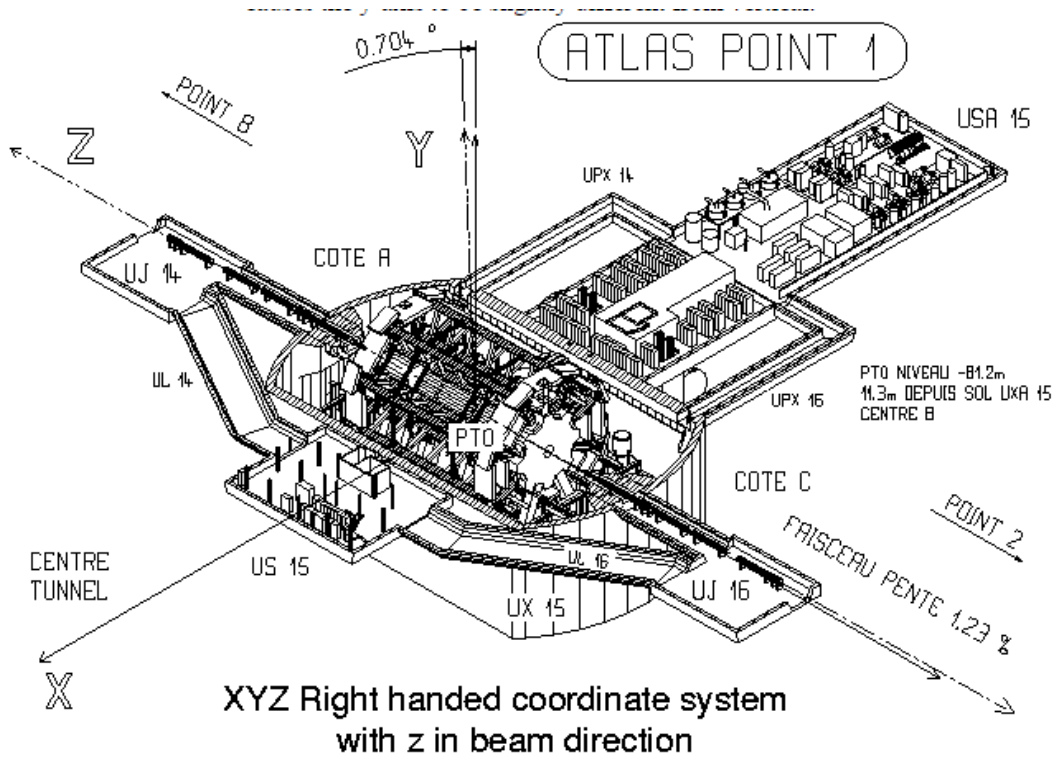


Figure 1.4 – ATLAS right-hand coordinate system

1.2.2.1 The inner tracker

The ATLAS inner detector (ID) is designed to provide hermetic and robust pattern recognition, excellent momentum resolution and both primary and secondary vertex measurements[4] for charged tracks above a given p_T threshold (nominally 0.5 GeV) and within the pseudorapidity range $|\eta| < 2.5$. The overall ID layout is shown in Figure 1.5. The ID has three independent but complementary sub-detectors. The inner most detector is the high resolution silicon pixel

detector. Then the semiconductor tracker (SCT) with silicon microstrip layers is implemented around the pixel detector. The outer layers of the ID is a combined tracking and electron identification detector, the transition radiation tracker (TRT).

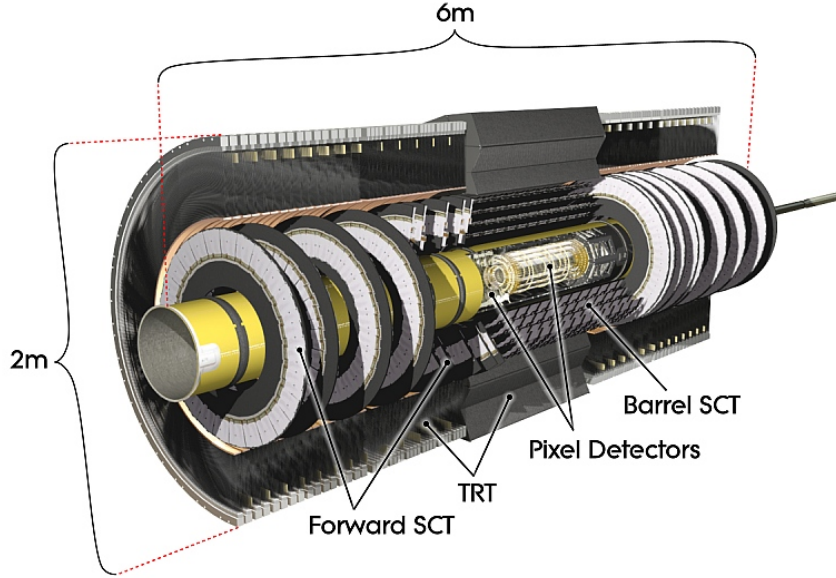


Figure 1.5 – Cut-away view of the ATLAS ID

The pixel detector

The pixel detector is the closest detector to the interaction point. Initially, the detector system consisted of three barrel layers at radii of ~ 5 cm, 9 cm, and 12 cm. On each side, three disks between radii 9 and 15 cm are implemented. A side view of the pixel detector is shown in Figure 1.6. In 2014, a new pixel layer was added inside the 3-layer pixel system, called insertable b-layer (IBL) [10], which will be described in Section 3.2.

The 3-layer pixel detector consists of 1744 modules (1456 modules in the barrels and 288 modules in the disks). A schematic view of a pixel module is shown in Figure 1.7. The pixel module consists of 16 front-end electronics chips, called FE-I3 [11], and a $250\ \mu\text{m}$ silicon sensor, connected together by bump bonding. On the top of the module, a flexible polyimide printed-circuit board (flex-hybrid) with a module control chip (MCC) glued to the flex-hybrid is mounted to support the electronics chips and sensor. Details of the pixel module concepts are described in Chapter 3.1.

The semiconductor tracker

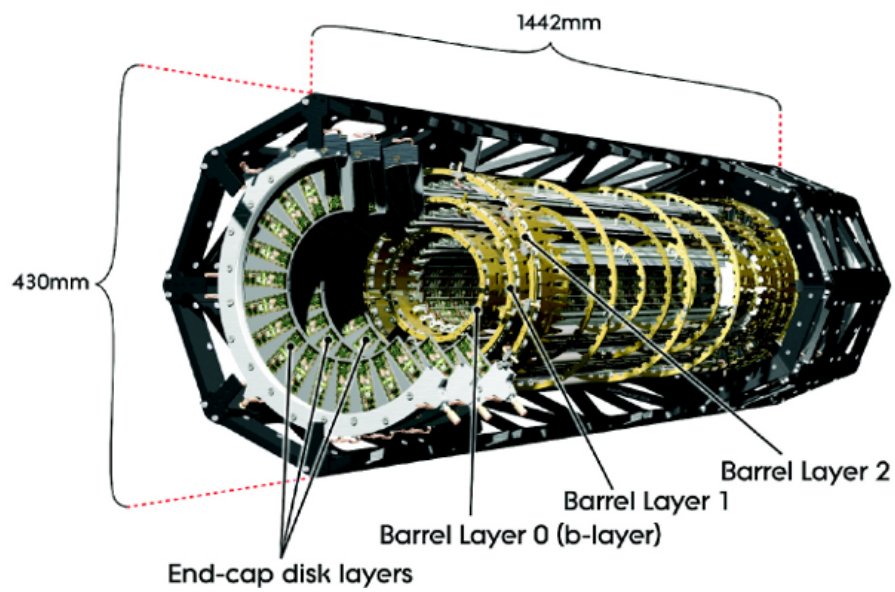


Figure 1.6 – Side view of the pixel detector

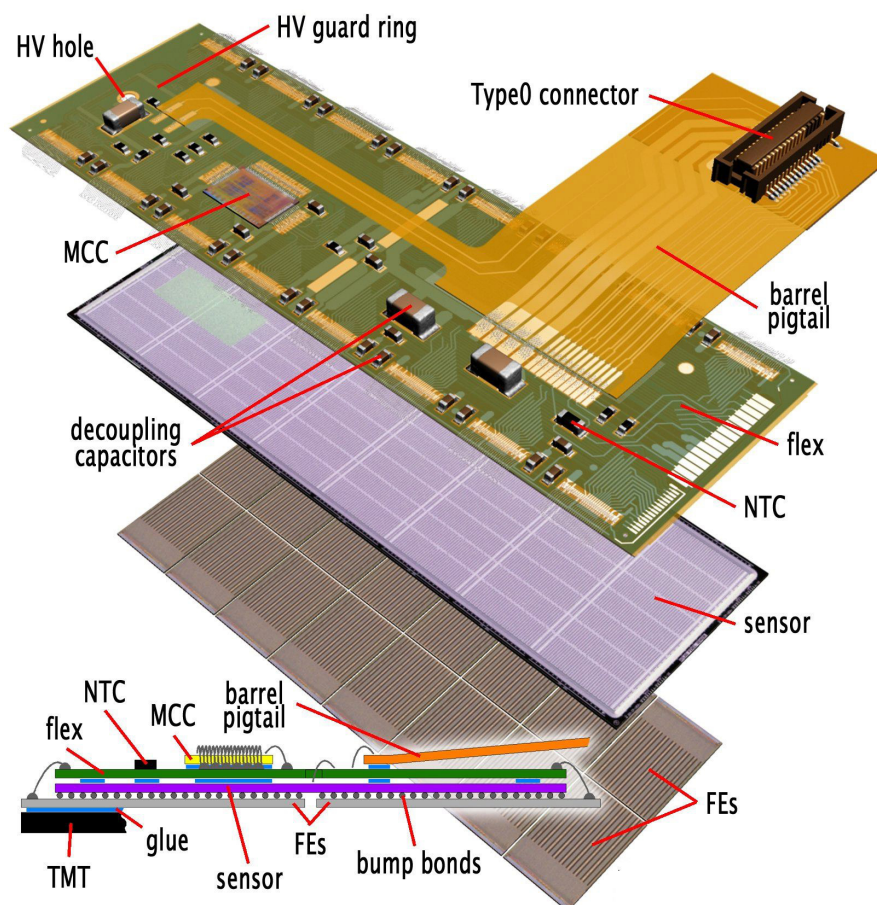


Figure 1.7 – Barrel pixel module schematic

The semiconductor tracker (SCT) surrounds the pixel detector, as shown in Figure 1.8. The SCT system consists of a barrel made of four cylinders and two endcaps each of nine disks [12] with 4088 modules.

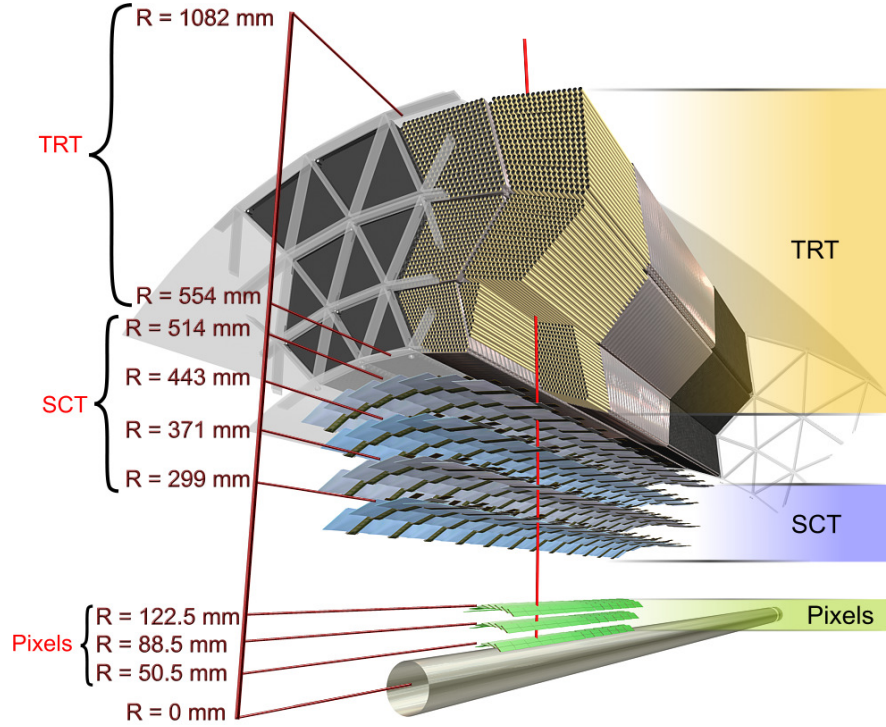


Figure 1.8 – Inner detector layout schematic

The four barrel layers consist of 2112 barrel SCT modules [12] and the strip size is $80\mu\text{m} \times 6\text{cm}$. A photograph and layout of a barrel SCT module is shown in Figure 1.9. 1976 modules of three different types make the endcaps. The end-cap modules are similar with the barrel modules but consist of three different sizes of tapered strips. The spatial resolution of the SCT modules has been measured in a test beam. At normal incidence, a combined spatial resolution of $\sim 16\mu\text{m}$ is measured in $R - \Phi$; the resolution is consistent with the binary readout of the two sensors with $80\mu\text{m}$ strips, including a small fraction of multiple hits [4].

The transition radiation tracker

The outermost layer of the ID is the transition radiation tracker (TRT) mounted between 55.4 cm and 108.2 cm radii with respect to the interaction point, as shown in Figure 1.8. The TRT is a polyimide drift (straw) tracker. Along with continuous tracking, the TRT provides electron identification capability through the detection of transition radiation X-ray photons [13]. Each straw is 4 mm of diameter with a $31\mu\text{m}$ tungsten anode wire placed in the center. The straw tube operates as a small proportional counter with the wall of the straw tube biased at

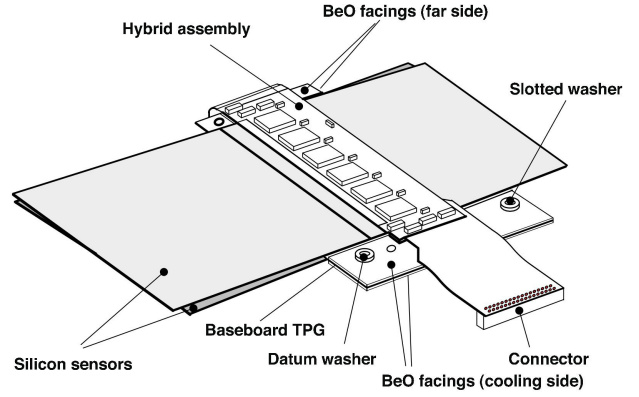
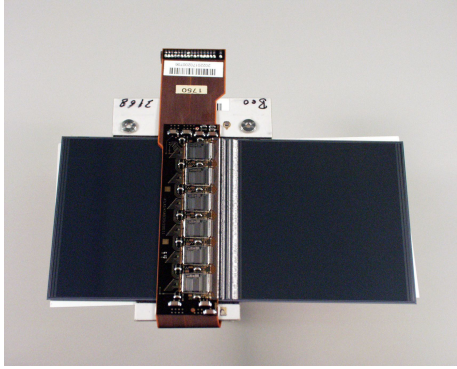


Figure 1.9 – Photograph (left) and drawing (right) of a barrel module, showing its components. The thermal pyrolytic graphite (TPG) base-board provides a high thermal conductivity path between the coolant and the sensors.

-1.5KV and the wire at ground. The barrel region consists of 52544 straw tubes of 1.5 m length and there are also 122 800 radial 0.4 m straws on each side of the end-cap.

1.2.2.2 The calorimeters

The ATLAS calorimeter system consists of an electromagnetic calorimeter [14] (EM) and a hadronic calorimeter [15], as shown in Figure 1.10. Over the η region matching that of the inner detector, the fine granularity of the EM calorimeter allows for accurate measurements of electrons and photons. The coarser granularity of the rest of the calorimeter is sufficient to satisfy the physics requirements for jet reconstruction and E_T^{miss} measurements [4]. The electromagnetic calorimeter is made of a liquid argon sampling calorimeter, and the endcaps of the hadronic calorimeter also uses liquid argon as the detection medium. The barrel volume of the hadronic calorimeter surrounding the EM calorimeter consists of iron tiles interleaved with scintillators to measure the charged particles from the induced fluorescence light. The calorimeter depth is an important design parameter. The calorimeters are not only providing good containment for electromagnetic and hadronic showers but also limit punch-through into the muon system. 11λ (interaction lengths) at $\eta = 0$ (including 1.3λ from the outer support) is sufficient to reduce punch-through well. Together with the large η coverage, good E_T^{miss} measurement is also ensured by this thickness, which is important for lots of physics signals and in particular for SUSY physics.

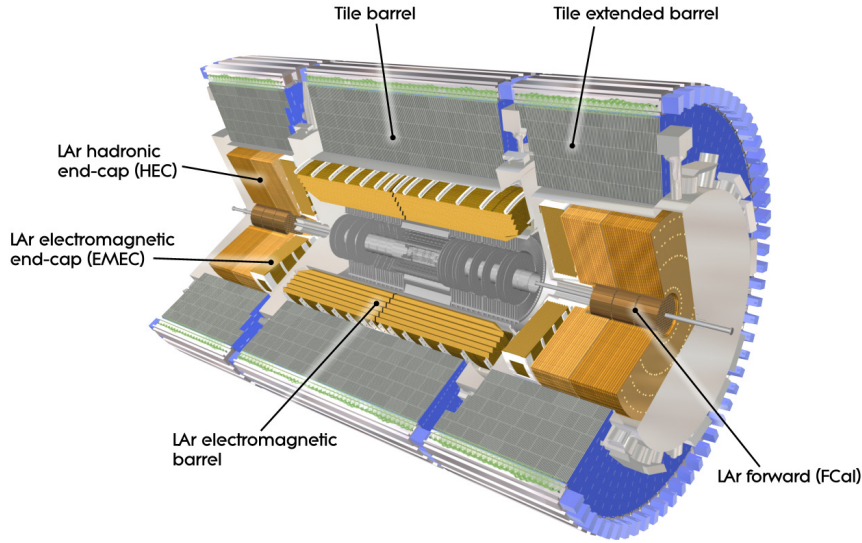


Figure 1.10 – Cut-away view of the ATLAS calorimeter system

1.2.2.3 The muon Spectrometer

The muon spectrometer [16] is the outermost detector of the ATLAS experiment. The spectrometer consists of four main chambers : monitored drift tubes (MDT), cathode strip chambers (CSC), resistive plate chambers (RPC), and thin gap chambers (TGC), as shown in Figure 1.11. It aims to measure high p_T muons with good precision independently of the inner detector. This information is an important information for the triggering system. In the barrel region, three cylindrical layers around the beam axis are used to measure the muons tracks, and in the endcap regions, three layers of chambers are installed perpendicular to the beam axis.

1.2.2.4 Forward detectors

The ATLAS forward regions are covered with three smaller detector systems [17], as shown in Figure 1.12. The LUCID (Luminosity measurement using Cerenkov Integrating Detector) is mounted at ± 17 m from the interaction point. It is the main online relative-luminosity monitor for ATLAS. Its main purpose is to detect the inelastic p-p scattering in the forward direction in order to measure the instantaneous luminosity and the integrated luminosity. The second detector is ALFA (Absolute Luminosity For ATLAS) located at ± 240 m from the interaction point to reach a sufficiently small angle. The absolute luminosity is monitored via elastic scattering at small angles by ALFA. The third detector is the Zero-Degree Calorimeter (ZDC). It plays a key role in determining the centrality of heavy-ion collisions and is located at ± 140 m from the interaction point. It detects the

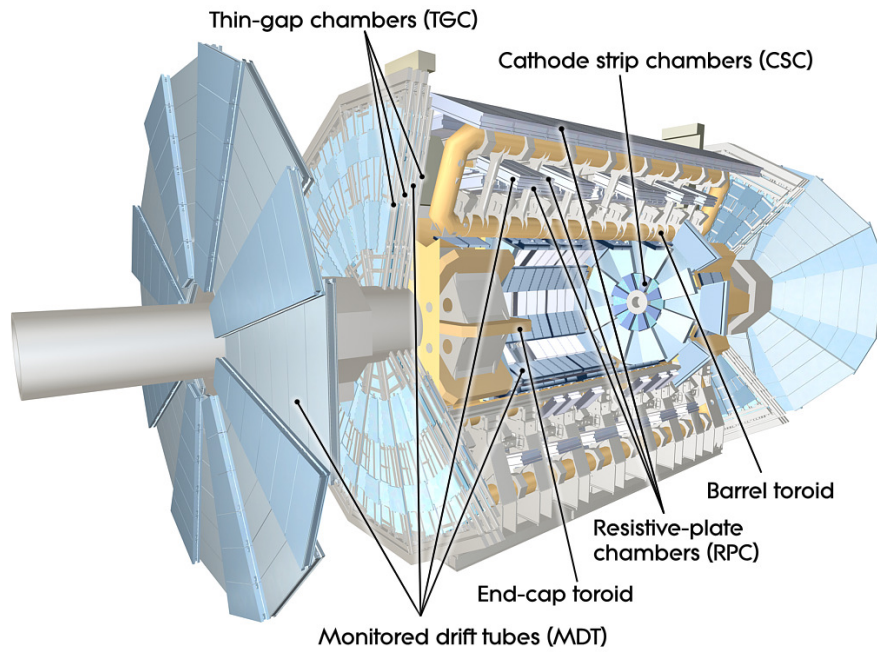


Figure 1.11 – Cut-away view of the ATLAS muon spectrometer

forward neutrons with $|\eta| > 8.3$ in heavy ion collisions.

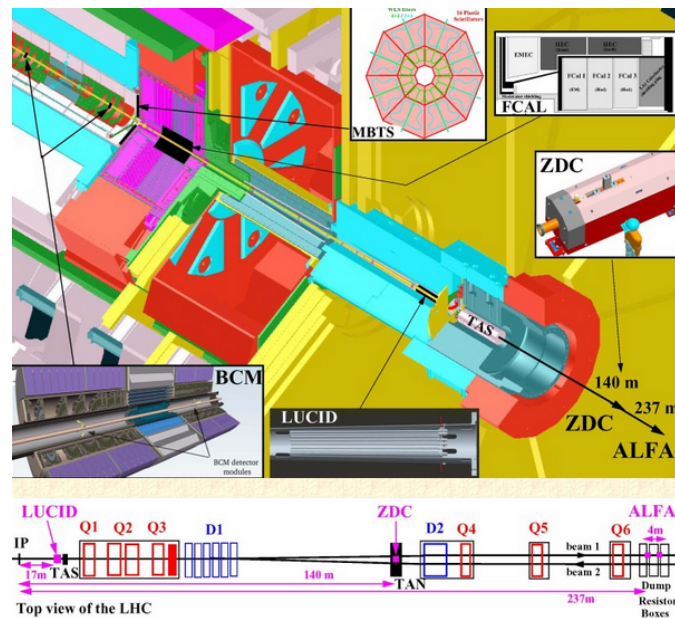


Figure 1.12 – Forward detectors of ATLAS

1.2.2.5 Trigger and data acquisition system

The bunch crossing of the LHC is 25 ns which results in a 40 MHz frequency collision rate. ATLAS real time recorded data exceeds by a large factor of its data storage capability. To reduce the data flow with minimal loss of physics events, ATLAS uses a three levels trigger system [18] as shown in Figure 1.13. The three

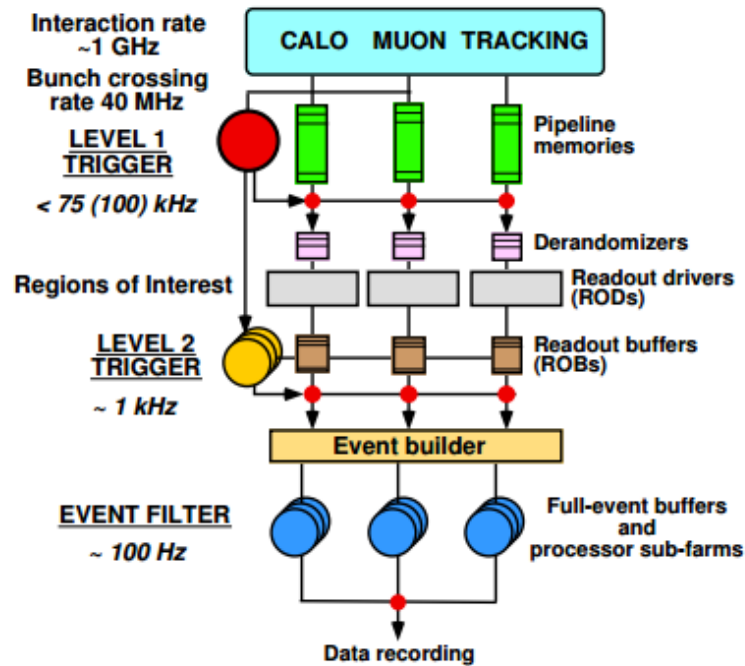


Figure 1.13 – Trigger scheme of ATLAS

trigger levels are L1, L2 and the event filter.

The level 1 trigger is a hardware based trigger using the information from the calorimeter and the muon system. It reduces the event rate from 40 MHz to 75 kHz, and has a latency of $2.5 \mu\text{s}$. It searches for high transverse-momentum muons, electrons, photons, jets, and τ leptons decaying into hadrons, as well as large missing and total transverse energy. In each event, the L1 trigger also defines one or more Region-of-Interest (RoI's), which are used by the high-level trigger subsequently.

The RoI information is used for the software level 2 trigger. The L2 trigger uses the all available detector data within the RoI's, and reduces the trigger rate to 1 kHz. The final step of the event selection is carried out by the event filter. It uses offline analysis procedures to reduce the event rate to roughly 200 Hz, which can then be recorded on tape.

1.3 The ATLAS inner detector upgrade

After the first successful years of running at the LHC, a new particle has been discovered in 2012 with a mass of $125.09 \pm 0.21(stat.) \pm 0.11(syst.) GeV$ [19], its properties being compatible with those of a SM Higgs boson. The LHC is now preparing to fully exploit the unprecedented physics opportunities offered by the exploration of a completely new energy domain to not only characterize the Higgs boson properties, but also to search for new resonances predicted in the SM. To reach this goal, the LHC will gradually raise its collision energy in the

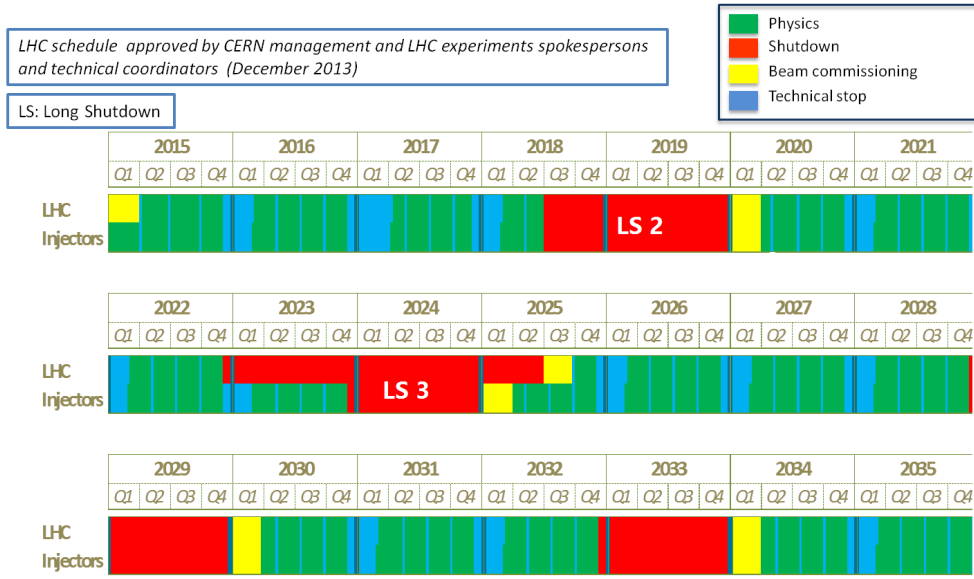


Figure 1.14 – LHC upgrade schedule beyond LS1

coming years, which will enhance the production cross section of the particles under study, and will also increase the luminosity of the machine. The ATLAS collaboration has decided to use the window of opportunity offered by the LHC long shutdowns (LS) to improve the equipment's detection performances by making gradual changes to the equipment suited for the new environment and improve the detector performance. A fourth pixel layer, called insertable b-layer (IBL) [20], has been inserted into the present 3-layer pixel tracker in LHC LS1. More details concerning the IBL will be discussed in Section 3.2. The LSs planned in the coming years are listed in Figure 1.14. In this section, only the upgrades concerning the inner detector are described.

LS1

The main upgrade during LS1 of the ATLAS detector has been the inner detector. The IBL was added to the present pixel detector between a new beam pipe

and the initial inner pixel layer (B-layer). The main motivations of this project are :

- a) Tracking and vertexing robustness : Irreparable failures of modules in the pixel layers in particular in the B-layer had appeared with time, which affected the tracking efficiency and b-tagging. The IBL improves the tracking robustness by providing a forth pixel data point and improves the b-tagging capability of ATLAS.
- b) Luminosity effects : The increasing luminosity after LS1 lead to higher hit rates. The IBL readout IC, called FE-I4, is developed with a new digital pixel architecture based on “4-Pixel Digital Region”. This will improve the detection capability in high hit rates condition.
- c) Improve the tracking precision : The IBL is mounted close to the interaction point and the pixel size was reduced compared with the present 3-layer pixel detector, which allows for more accurate primary vertexing and b tagging performance.

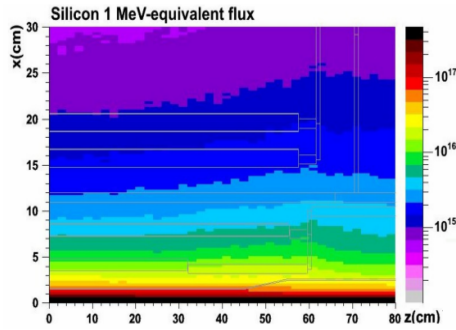
LS2

During the LS2, no upgrade of the pixel detector is at the present time foreseen. Nevertheless, it should be noted that the LS2 would give a good opportunity to intervene in case of an accident with the detector.

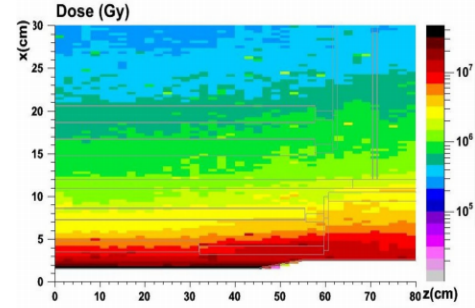
LS3

At the end of 2022, the LHC will have a major upgrade, called Phase II Upgrade. From 2024 on, the HL-LHC will provide unprecedented pp luminosities to ATLAS with a levelled instantaneous luminosity of $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, resulting in an additional integrated luminosity of around 2500 fb^{-1} over ten years [21]. The increased instantaneous luminosity at the HL-LHC results in an expected mean number of interactions per bunch crossing increasing from approximately 55 at $2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ to approximately 140 at $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ (assuming a bunch crossing time of 25 ns) [21]. By simulation, the predictions for the maximum 1 MeV-neq fluence and ionizing dose for 3000 fb^{-1} in the pixel system is $1.4 \times 10^{16} \text{ cm}^{-2}$ and 7.7 MRads at the center of the innermost barrel layer cite17, as shown in Figure 1.15a and Figure 1.15b.

The much harsher radiation and occupancy conditions of the HL-LHC requests a complete replacement of the present inner detector (ID). To withstand the HL-LHC environment, the new inner tracker (ITk) should have finer granularity, increased radiation hardness and reduced material budget. Based on these requirements, an all-silicon-detector tracker is proposed, with pixel sensors at the inner radii surrounded by microstrip sensors [22], as shown in Figure 1.16. The final layout of the ITk is not fixed yet. Several optimized layouts deriving from this baseline layout are under simulation. The pixel sizes of the new pixel



(a) 1 MeV neutron equivalent fluence



(b) TID

Figure 1.15 – (a) : The RZ-map of the 1 MeV neutron equivalent fluence. (b) : The RZ-map of the TID.

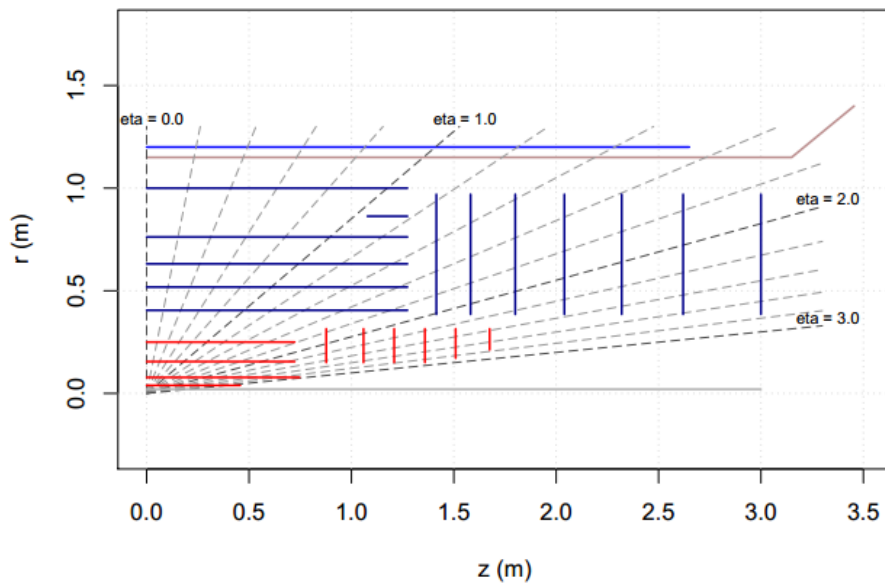


Figure 1.16 – The baseline layout of ITk

detector electronics is foreseen to be $25 \times 150 \mu\text{m}^2$ or $50 \times 50 \mu\text{m}^2$. The proposed all-silicon ITk could be covered by approximately 193 m^2 of strips and 10 m^2 of pixels. In this scheme, the ITk active area and channel count are listed in Table 1.3. The proposed ITk layout is mainly designed based on the optimized physics performance. In addition, it should consider the constraints from modularity, integration, cost, etc.

Detector	Silicon area [m^2]	Channels [10^6]
Pixel barrel	5.1	445
Pixel end-cap	3.1	193
Pixel total	8.2	638
Strip barrel	122	47
Strip end-cap	71	27
Strip total	193	74

Table 1.3 – Inner tracker active area and channel count

Presently, the inner pixel detector of the ATLAS tracker is foreseen to be made using a hybrid concept and has shown a relatively good radiation tolerance. But non-standard technologies used for the pixel detectors cause high construction cost, e.g. using of high resistivity FZ silicon and the bump-bonding for the hybrid pixels.

High-voltage particle detectors in commercial CMOS technologies are a detector family which allows implementation of low-cost, thin and radiation-tolerant detectors with high time resolutions [23]. The smaller pixel size that can be implemented in these technologies could improve the spatial resolution and two-track separation. The reduced thickness of the sensor would reduce the cluster size at high pseudorapidities, which would improve the resolution of tracks and the amount of data to be coped with.

ATLAS has started R&D on HV/HR CMOS detector since 2011. Several prototypes have already demonstrated positive results for radiation tolerance and efficiency. The concepts of the HV/HR sensors and specifications are described in Chapter 3. To understand the HV/HR technologies, prospect the detector behavior and optimize the design, a Technology Computer-Assisted Design (TCAD) simulation study is of great helpful. The details of the TCAD simulation methodology and results are described in Chapter 4. The characterizations of several HV/HR CMOS sensors are described in details in Chapter 5.

2 Silicon properties and pixel sensor principles

Usage of semiconductors for spectroscopic applications has started in the 1960s. In silicon, the ionization energy of an electron-hole (eh) pair is only 3.61 eV, which offers better energy resolution compared to the gas ionization energy of approximately 20 eV. In the late 1970s, semiconductor sensors became common as tracking devices in particle physics [24]. Some fundamental silicon physics relevant for tracking applications are briefly summarized in Section 2.1. The particle interaction properties with silicon are described in Section 2.2. The formation of signal in a sensor is discussed in Section 2.3. In Section 2.4, the radiation damages in silicon are explained in details, a phenomenon very relevant for the tracking detectors considered in this work.

2.1 Silicon physics and pn junction

2.1.1 Silicon properties

Pure semiconductors, also called intrinsic semiconductors, can be found in column IV of the periodic table of the elements. The most common elements are silicon and germanium for the semiconductor sensor productions. The current operating ATLAS pixel detector uses silicon as the sensing material, and it will be also the case for the future upgraded inner tracker. The silicon physics properties are hence introduced in this section.

2.1.1.1 Carrier concentration

Intrinsic silicon, has the same number of negative charge carriers (electrons) and positive charge carriers (holes). The number of electrons n can be calculated by the formula [25] :

$$n = \int_{E_C \equiv 0}^{E_{top}} N(E) F(E) dE \quad (2.1)$$

where E is the energy, E_C is the energy at the lower bound of the conduction band, arbitrarily set to zero, and E_{top} is the energy at the top of the conduction

band. The states density in the conduction band $N(E)$ can be calculated by [25] :

$$N(E) = 4\pi \left(\frac{2m_n^*}{h^2} \right)^{\frac{2}{3}} E^{\frac{1}{2}} \quad (2.2)$$

where m_n^* is the effective mass of the electrons and h is the Planck constant. The Fermi function is given by [26] :

$$F(E) = \frac{1}{1 + e^{\frac{E-E_F}{kT}}} \quad (2.3)$$

where E_F is the Fermi energy. The probability of occupying an electron is 1/2 at Fermi energy. For energies which are 3 kT below or above the Fermi energy, the function $F(E)$ (see expression (2.3)) can be approximated to :

$$F(E) \approx e^{-\frac{E-E_F}{kT}} \quad (2.4)$$

Hence the free electron and hole concentrations at temperature T can be calculated by :

$$n = 2 \left(\frac{2\pi m_n kT}{h^2} \right)^{\frac{3}{2}} e^{-\frac{E_C-E_F}{kT}} = N_C \cdot e^{-\frac{E_C-E_F}{kT}} \quad (2.5)$$

$$p = 2 \left(\frac{2\pi m_p kT}{h^2} \right)^{\frac{3}{2}} e^{-\frac{E_F-E_V}{kT}} = N_V \cdot e^{-\frac{E_F-E_V}{kT}} \quad (2.6)$$

where E_V is the upper bound of the valance band, N_C and N_V are called effective density of states in the conduction band and valence band with the values of $2.86 \times 10^{19} \text{ cm}^{-3}$ and $2.66 \times 10^{19} \text{ cm}^{-3}$ respectively [27]. The band diagram, state density, Fermi function and carrier concentration are illustrated in Figure 2.1. The electron and hole concentrations satisfy the relation [27] :

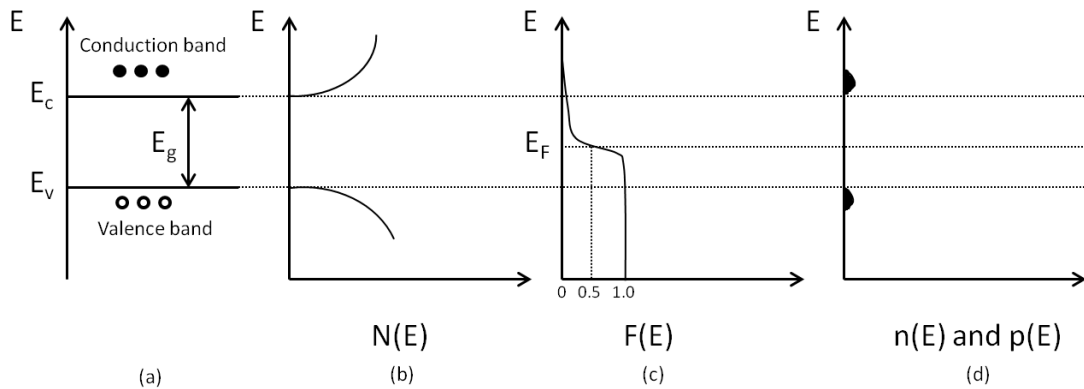


Figure 2.1 – Intrinsic silicon. (a) Band diagram. (b) density of states. (c) Fermi distribution function. (d) carrier density.

$$n \cdot p = n_i^2 = N_C N_V \cdot e^{\frac{-E_g}{kT}} \quad (2.7)$$

which is independent of the Fermi level and therefore also does not depend on the doping concentration. E_g is defined as the difference between the conduction band lower bound and valence band upper bound, and is called the energy gap. At $T=300$ K, the intrinsic carrier concentration is :

$$n_i = 1.45 \times 10^{10} \text{ cm}^{-3} \quad (2.8)$$

and the intrinsic Fermi level can be calculated by the formulas (2.5) and (2.6) :

$$E_{Fi} = \frac{E_C + E_V}{2} + \frac{3}{4} kT \ln\left(\frac{m_n^*}{m_p^*}\right) \approx \frac{E_C + E_V}{2} \quad (2.9)$$

As the second term in equation (2.9) is quantitatively only of the order of 0.01eV, the intrinsic Fermi level is very close to the middle of the band gap.

Intrinsic silicon can be doped with certain impurities to change its conductivity, and the properties of doped silicon depend on the doping materials. The elements used to dope silicon are either from the III group of the periodic table (e.g. boron) or from the V group (e.g. phosphorus, arsenic...). Boron has one electron less than silicon in its outermost shell. Therefore it is easy to trap a valence electron from the valence band of the silicon lattice, which produces a free hole. The boron is called an acceptor and the silicon doped by boron is defined as p-type. A similar situation happens when doping silicon with elements from the V group of the periodic table like phosphorus. Phosphorus has one electron more than silicon, and can easily release it as a free electron in the silicon lattice. Elements such as phosphorus are called donors and the silicon doped by phosphorus is defined as n-type. A sketch of the silicon lattices in these three cases (intrinsic, n-type and p-type) is shown in Figure 2.2. In crystalline intrinsic silicon, there are approximately $5 \times 10^{22} \text{ atoms/cm}^3$. A moderately doped silicon material (dopant concentration below 10^{18} cm^{-3}) is called “extrinsic silicon”. Doping concentrations above 10^{18} cm^{-3} are considered as “degenerate silicons” at room temperature. The property of “degenerate silicon” is more like a metal than a semiconductor.

The Fermi levels after donor and acceptor doping are shifted and can be calculated from the formulas (2.5) and (2.6) as :

$$E_F = E_i - kT \ln\left(\frac{N_A}{n_i}\right) \quad (2.10)$$

$$E_F = E_i + kT \ln\left(\frac{N_D}{n_i}\right) \quad (2.11)$$

where N_A is the acceptor concentration and N_D is the donor concentration. For n-type silicon, the electrons are called majority carriers and the holes are called

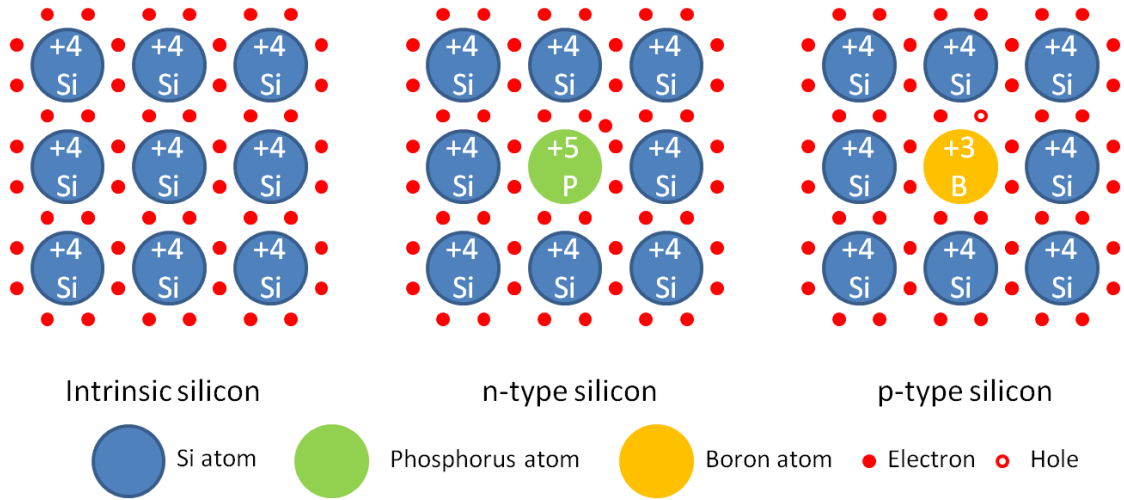


Figure 2.2 – Silicon doping diagram

minority carriers. For p-type silicon, the holes are called majority carriers and the electrons are called minority carriers.

2.1.1.2 Carrier generation and recombination

In silicon, carrier generation and recombination processes occur by which mobile charge carriers (electrons and holes) are created and eliminated, as sketched in Figure 2.3. On the left side of Figure 2.3, an electron leaves the valence band and goes to the conduction band leaving a hole below the valence band. On the right side of Figure 2.3, an electron of the conduction band goes to the valence band and recombines with a hole. In the thermal-equilibrium state, the electron and hole concentrations are independent of time, therefore the electrons and

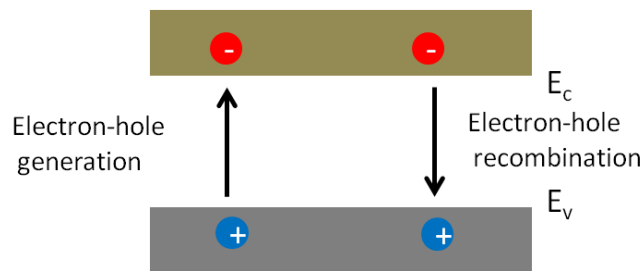


Figure 2.3 – Thermal-equilibrium silicon generation and recombination diagram

holes generation and recombination rates must be equal,

$$G_{n0} = G_{p0} = R_{n0} = R_{p0} \quad (2.12)$$

where G_{n0} is the electron generation rate, G_{p0} is the hole generation rate, R_{n0} is the electron recombination rate, and R_{p0} is the hole recombination rate.

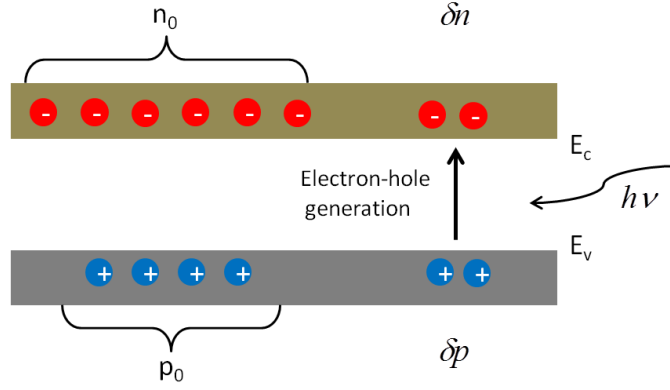


Figure 2.4 – Excess carrier generation and recombination diagram

When a silicon is excited by an external mechanism (e.g. radiation, photon pumping...), the concentrations of electron and hole are changed due to the non thermal-equilibrium condition. The electrons and holes generated by the external excitation are called excess carriers. The process is illustrated in the Figure 2.4. The excess electrons and holes are generated in pairs, $g'_n = g'_p$. Now the electron and hole concentrations are :

$$n = n_0 + \delta n \quad (2.13)$$

$$p = p_0 + \delta p \quad (2.14)$$

where n_0, p_0 are the intrinsic electron and intrinsic hole densities and $\delta n, \delta p$ are the excess electron and excess hole densities.

The excess electrons and holes also recombine in pairs, $R'_n = R'_p$. The direct band-to-band recombination is spontaneous in behavior, therefore the recombination rate is constant through time. The electron concentration variation rate is [28] :

$$\frac{dn(t)}{dt} = \beta[n_i^2 - n(t)p(t)] \quad (2.15)$$

where, $n(t) = n_0 + \delta n(t)$, $p(t) = p_0 + \delta p(t)$ and β is a proportional constant. The thermal equilibrium parameters n_0 and p_0 are time independent. For a p-type material ($n_0 \ll p_0$), in the low-level injection case, one can assume $\delta n(t) \ll p_0$. Then, the equation (2.15) changes to :

$$\frac{d(\delta n(t))}{dt} = -\beta p_0 \delta n(t) \quad (2.16)$$

The solution of equation 2.16 is an exponential decay from the initial excess carrier concentration :

$$\delta n(t) = \delta n(0)e^{-\beta p_0 t} = \delta n(0)e^{-\frac{t}{\tau_{n0}}} \quad (2.17)$$

where the minority lifetime is $\tau_{n0} = \frac{1}{\beta_{p0}}$. Therefore, the recombination rate of excess carriers for p-type silicon in the low-level injection case are :

$$R'_n = R'_p = R' = -\frac{d\delta n(t)}{dt} = \frac{\delta n(t)}{\tau_{n0}} \quad (2.18)$$

and for n-type silicon similarly :

$$R'_n = R'_p = R' = -\frac{d\delta p(t)}{dt} = \frac{\delta p(t)}{\tau_{p0}} \quad (2.19)$$

In the low-level injection case, the recombination is limited by the concentration of the minority carriers.

2.1.1.3 Carrier transport

The movement of free carriers driven by an electric field due to an external applied voltage can cause a current. This charge transport mechanism is called drift. The free carriers also move from high density regions to low density regions. The thermal energy and the random motion of carriers leads to this transport, which is called diffusion. The total current equals the sum of the drift and of the diffusion currents.

The drift current

Assuming the carriers move with the same average velocity, the current density, $\vec{J}$, can be written as :

$$\vec{J} = \rho \vec{v} \quad (2.20)$$

where the ρ is the charge density and the $\vec{v}$ is the velocity. For electrons and holes, the current density are :

$$\vec{J}_n = qn\vec{v} \quad (2.21)$$

$$\vec{J}_p = qp\vec{v} \quad (2.22)$$

where q is the electrical charge, n and p are the electron and hole density respectively.

In reality, the carriers do not follow straight paths along the electric field lines in silicon. The carrier velocity increases due to the external electric field, then the carriers collide with the silicon atoms with almost all kinetic energy loss. After the collision, the carriers are accelerated again and gain energy until the next collision with atoms. The carrier movement in silicon is described in Figure 2.5. Applying Newton's law to a hole in the silicon, we have :

$$\vec{F} = m_p^* \vec{a} = m_p^* \frac{d\langle \vec{v} \rangle}{dt} \quad (2.23)$$

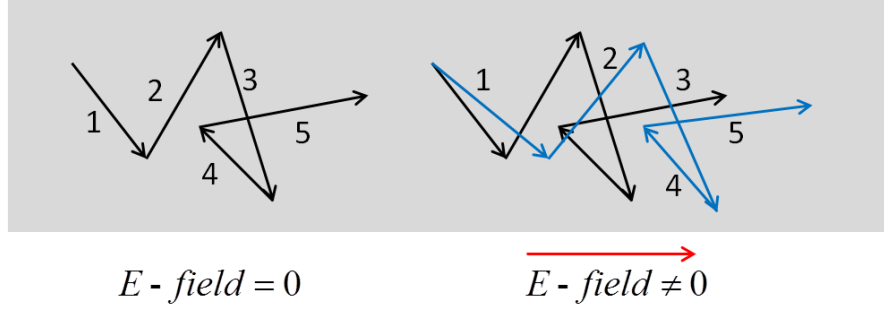


Figure 2.5 – Random movement of carriers with (right) and without (left) applied electric field

where $\langle \vec{v} \rangle$ is the hole average velocity and m_p^* is the effective mass of hole. The hole motion is caused by both the electrostatic force and the scattering force. Then the equation (2.23) can then be rewritten as :

$$\vec{F} = q\vec{\varepsilon} - \frac{m_p^* \langle \vec{v} \rangle}{\tau_c} \quad (2.24)$$

where ε is the applied electric field and τ_c is the average time between collisions. Combining these two equations yields the relation for the average hole velocity :

$$q\vec{\varepsilon} = m_p^* \frac{d \langle \vec{v} \rangle}{dt} + \frac{m_p^* \langle \vec{v} \rangle}{\tau_c} \quad (2.25)$$

Now just consider the hole has already accelerated and reached a steady average velocity. The hole velocity is proportional to the electric field and we can define the mobility as the velocity to field ratio :

$$\mu = \frac{\Delta |\vec{v}|}{|\vec{\varepsilon}|} = \frac{q\tau_c}{m_p^*} \quad (2.26)$$

Then, the drift current density for both electrons and holes can be described :

$$\vec{J}_n = -qn\mu_n\vec{\varepsilon} \quad (2.27)$$

$$\vec{J}_p = qp\mu_p\vec{\varepsilon} \quad (2.28)$$

Therefore, the total drift current in silicon can be written as :

$$\vec{J}_{drift} = \vec{J}_n + \vec{J}_p = q(\mu_n n + \mu_p p)\vec{E} = \sigma \vec{E} \quad (2.29)$$

where the σ is called conductivity with unit $(\Omega \cdot cm)^{-1}$. The conductivity depends on both the mobility and the doping concentration. The reciprocal of the conductivity, ρ , is named resistivity and the unit of resistivity is $\Omega \cdot cm$.

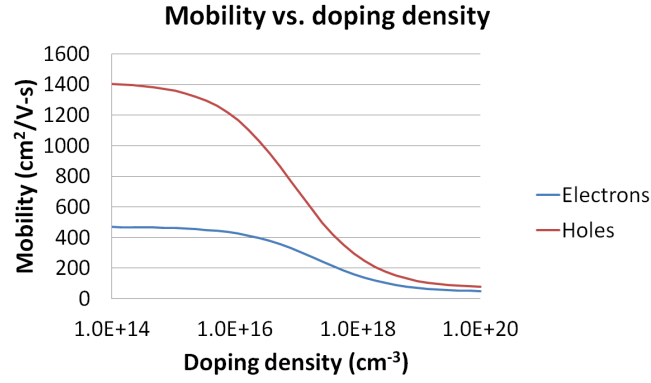


Figure 2.6 – Carriers mobility vs. doping concentration. Phosphorous and boron doped silicon.

The electron and hole mobilities have a similar dependence with respect to doping concentration. The mobility keeps almost constant at low doping concentrations (dopant concentration below 10^{15} cm^{-3}), whereas the mobility reduces at high doping concentrations due to impurity scattering. In addition, the mobility is different with different dopants. The electron and hole mobility variation with doping concentration is shown in Figure 2.6. The corresponding resistivity also depends on the doping concentration and is illuminated in Figure 2.7.

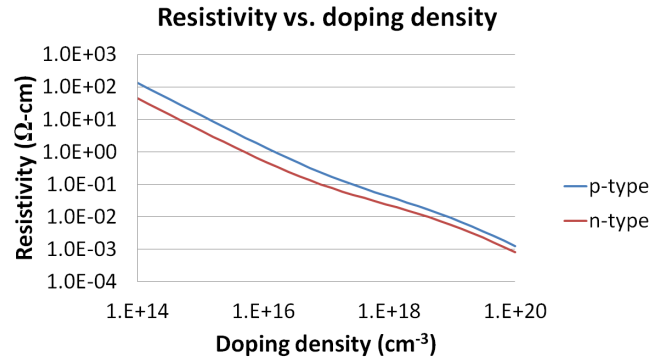


Figure 2.7 – Resistivity vs. doping concentration. Phosphorous and boron doped silicon.

The above discussion is based on the assumption that the mobility is independent of the electric field. Therefore the drift velocity is linearly proportional to the applied field. In reality, however, the linearity is not valid at high electric field and the velocity tends to saturate. This effect, also called mobility degradation, can be described by [29] :

$$\mu = \frac{v_s/E_c}{[1 + (E/E_c)^\beta]^\beta}, \quad (2.30)$$

The effect of velocity saturation as a function of electric field is shown in Figure 2.8. The low field mobility for intrinsic silicon at 300K is [30] :

$$\mu_n = 1415 \pm 46 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \quad (2.31)$$

$$\mu_p = 480 \pm 17 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \quad (2.32)$$

The electrons mobility is hence three times higher than the holes mobility, which causes the holes to be more easily trapped.

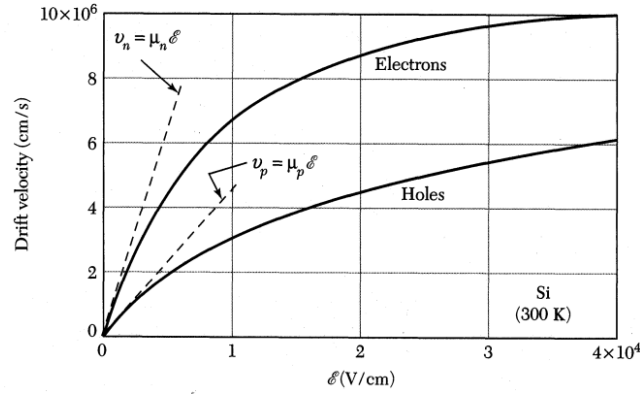


Figure 2.8 – Carriers velocity vs. electric field in silicon [31]

The diffusion current

The thermal energy leads to the carriers moving randomly, called carrier diffusion. But this random movement does not induce any net current unless a carrier gradient is present. In this case, the carriers diffuse from a high density region to a low density one. The diffusion current can be described by,

$$\vec{J}_{n,diffusion} = -D_n \vec{\nabla} n = \frac{kT}{q} \mu_n \vec{\nabla} n \quad (2.33)$$

$$\vec{J}_{p,diffusion} = D_p \vec{\nabla} p = \frac{kT}{q} \mu_p \vec{\nabla} p \quad (2.34)$$

where $\vec{\nabla} n$ and $\vec{\nabla} p$ are the gradients of the electron and hole concentrations.

2.1.2 The pn-junction

Two oppositely semiconductor regions form a pn-junction. In the domain of tracking detectors, the reverse biased pn-junction is often the basic sensor element.

2.1.2.1 Structure of the pn junction and thermal equilibrium

A pn-junction consists of one p-type region and one n-type region as shown in Figure 2.9. Let us assume a uniform doping concentration for both n-type and

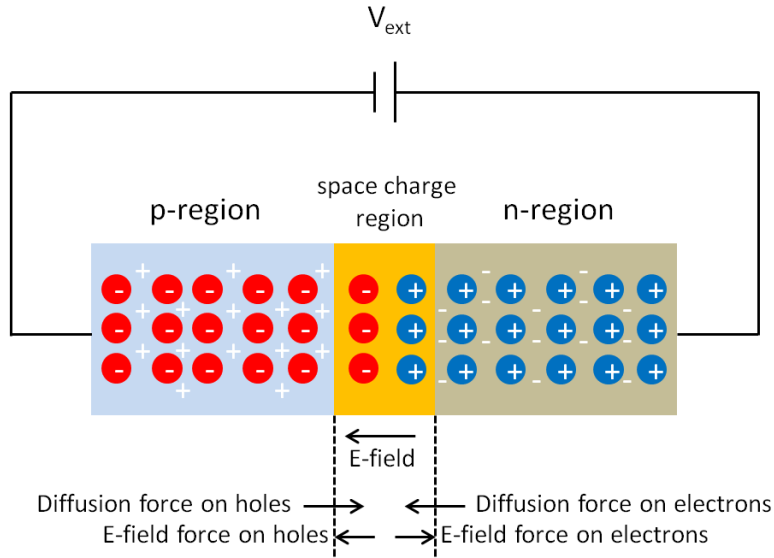


Figure 2.9 – A conceptual view of pn junction

p-type regions, and that the density variation at the interface is abrupt. In this case, we qualify the junction as an abrupt junction, and the interface is defined as metallurgical junction.

Let us consider the case where no external voltage is applied to the junction. The holes diffuse from the p-type region to the n-type region due to the carrier density difference, and the electrons diffuse in the other direction. The diffusion of the free carriers leaves the ionized charges around the metallurgical junction in which an electric field is induced. The electric field induces a drift of the carriers. The carriers diffusion process continues until the drift current equals the diffusion current, at which point the thermal equilibrium condition is reached. A zone without free carriers is hence created and it called the depletion zone (also called “space charge region”). In the thermal equilibrium situation, the system has only one constant Fermi level E_F , therefore the energy band is bended to adjust the Fermi level to a constant value, as shown in Figure 2.10. The electric field in the depletion region can be described by the so called built-in potential ϕ_i . The built-in potential for an abrupt junction can be calculated by the equation [24] :

$$\phi_i = \frac{kT}{e} \ln \left(\frac{n_{0,n} \cdot p_{0,p}}{n_i^2} \right) \approx \frac{kT}{e} \ln \left(\frac{N_D N_A}{n_i^2} \right) \quad (2.35)$$

where $n_{0,n}$ and $p_{0,p}$ are the electron and hole concentration in the n-type and p-type region respectively. In most cases, a complete ionization for donors and

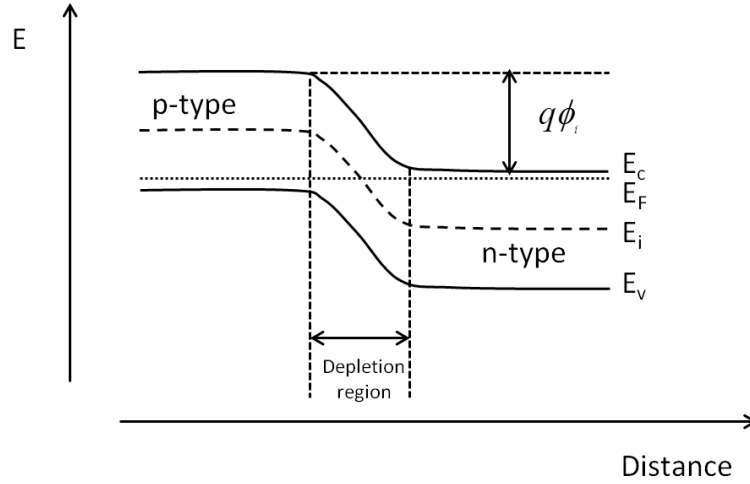


Figure 2.10 – Energy band of a pn junction in thermal equilibrium

acceptors can be assumed, therefore the electron and hole concentration can be substituted by the donor and acceptor doping concentration, N_D and N_A .

2.1.2.2 Reverse biased pn junction

The p-type region is typically connected to a low potential and the n-type to a high potential, in a configuration called reverse bias of pn-junction. Because of this bias, the holes in the p-type region are pulled away from the junction, and in the same way, the electrons are also repelled from the n-type side of the junction. This results in the increase of the size of the depletion zone. The depletion width and electric field in the depletion region can be calculated by solving the one dimensional Poisson equation. Taking the same abrupt junction mentioned hypothesis as before, the total depletion width is obtained by :

$$W = x_n + x_p = \sqrt{\frac{2\epsilon_0\epsilon_r}{e} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V + V_{bi})} \quad (2.36)$$

where V is the externally applied voltage.

In most cases, the sensor is formed by one heavily doped contact (e.g. $N_D = 10^{18} \text{ cm}^{-3}$) and one shallow doped substrate (e.g. $N_A = 10^{13} \text{ cm}^{-3}$). In this case, the depletion zone essentially grown in the p-type material and the depletion width can be approximated as :

$$W \approx x_p \approx \sqrt{\frac{2\epsilon_0\epsilon_r}{eN_A} V} \quad (2.37)$$

The maximum electric field occurs at the metallurgical junction, the value of

which can be calculated by :

$$E_{max} = \frac{2V}{W} \approx \sqrt{\left(\frac{2eN_A}{\varepsilon_0\varepsilon_r}\right)V} \quad (2.38)$$

In the reverse bias configuration, the leakage current derives from mainly two sources. One is the carriers diffusion from the undepleted region to the space charge region. The other one is the thermal generation-recombination centers at device surface and in the depletion region. The thermal generation dominates the leakage current per unit area in the space charge region and can be approximately described by :

$$J_{vol} = -e\frac{n_i}{\tau_g} \cdot (W - W_{V=0}) \approx -e\frac{n_i}{\tau_g} \sqrt{\frac{2\varepsilon_0\varepsilon_r}{eN_D}} V \quad (2.39)$$

where τ_g is the carrier lifetime, n_i is the intrinsic carrier concentration and $W_{V=0}$ is the initial depletion width without any external voltage applied.

The leakage current also depends on temperature due to the intrinsic carrier concentrations and the carrier lifetimes. The relation can be described by [24] :

$$J_{vol} \propto T^2 e^{-E_g(T)/2kT} \quad (2.40)$$

A useful rule of thumb for approximate estimation in practical case is that the volume current doubles when the temperature increase 8 K.

The capacitance per unit area of the pn junction can be modeled as two planar plates separated by the depleted region :

$$C(V) = \frac{\varepsilon_0\varepsilon_r}{W(V)} \approx \sqrt{\frac{\varepsilon_0\varepsilon_r e N_D}{2V}} \quad (2.41)$$

The capacitance is usually expressed as

$$\frac{1}{C^2} = \frac{2V}{\varepsilon_0\varepsilon_r e N_D} \quad (2.42)$$

A typical pn-junction capacitance characteristic is shown in Figure 2.11.

2.1.2.3 Breakdown voltage

If a very high voltage is applied to a pn junction, the breakdown of the junction occur. A junction breakdown is characterized by the rapid increase of the leakage current. The applied voltage leading to breakdown is referred to as the breakdown voltage. The breakdown is caused by two mechanisms : avalanche breakdown and Zener breakdown.

The Zener breakdown occurs through a tunneling mechanism in highly doped

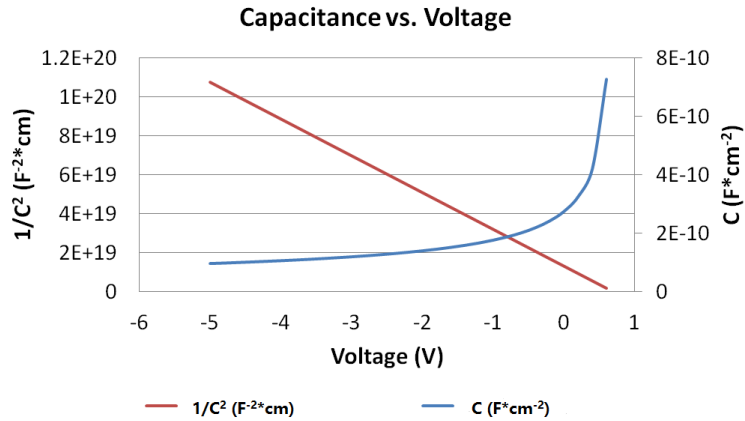


Figure 2.11 – Junction capacitance vs. voltage

pn junctions. The avalanche breakdown comes from the impact ionization of electron hole pairs at high electric field. When the applied voltage is so large that the free electrons gain very high velocities, these electrons then collide with the

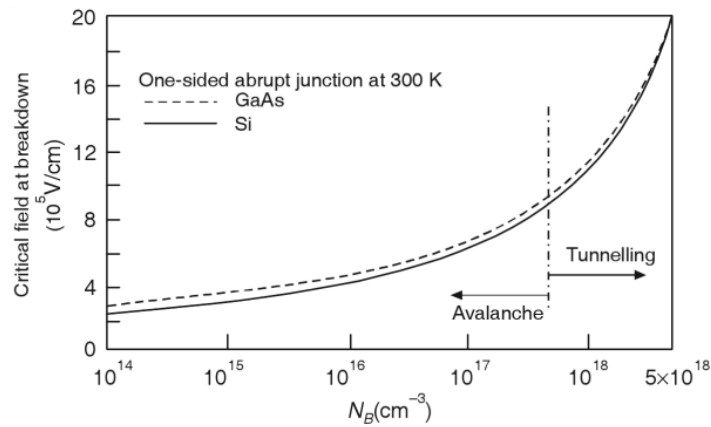


Figure 2.12 – Critical electric field vs. doping concentration [32]

silicon atoms and knock off more electrons. The free electrons lead to a rapid leakage current increase which can destroy the device. In most cases, the avalanche breakdown dominates the diode breakdown. The evaluation of the avalanche and the Zener breakdown critical electric field with the doping concentration is described in Figure 2.12.

2.2 Particles interaction with matter

A charged particle passing through a material (e.g. silicon) interacts with the lattice and loses in part its energy. The energy absorbed ionizes the silicon atom

and electron-hole pairs can then be detected as electrical signals. The charge deposition mechanism of charged particles heavier than electrons can be described by the Bethe-Bloch formula [33] :

$$-\left\langle \frac{dE}{dx} \right\rangle = \frac{4\pi r_e^2 m_e c^2 N_A z^2 Z}{A\beta^2} \times \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 + \dots \right] \quad (2.43)$$

where Z and A are the atomic and mass number of the material, N_A is the Avogadro constant, r_e is the classical electron radius (2.8 fm), z is the charge of the

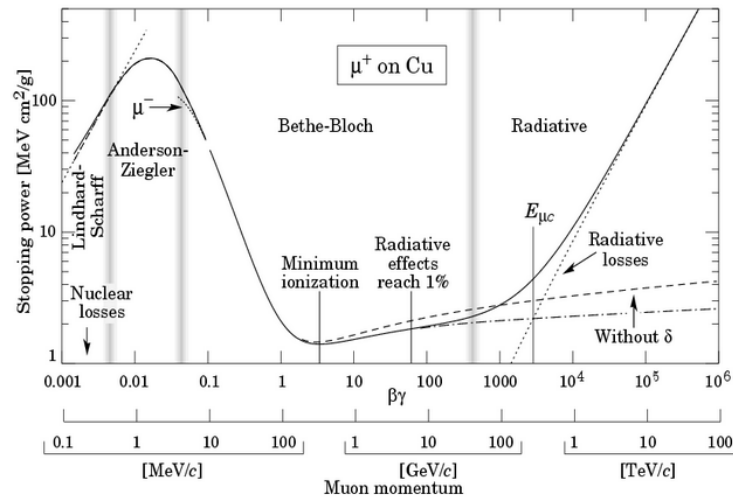


Figure 2.13 – Muon energy deposition in copper [34]

traversing particle in units of electron charge, $m_e c^2$ is the rest energy of the electron (0.511 MeV), β is the velocity of the traversing particle in units of the speed of light, γ is the Lorentz factor ($1/\sqrt{1-\beta^2}$), I is the mean excitation energy of the material (173 eV for silicon), and T_{max} is the maximum kinetic energy transfer to an electron.

As an example, the energy deposition in copper of muon is shown in Figure 2.13 as a function of the muon kinetic energy. For the low energy region (below $\beta\gamma$ value of 3), the β^2 -term is dominant and the stopping power decreases with increasing energy. A minimum stopping power is reached if $\beta\gamma \approx 3$. A particle with minimum energy deposition is called Minimum Ionizing Particle (MIP). For muon of momentum above the MIP's momentum, the stopping power increases weakly for increasing momentum due to the logarithmic term in equation (2.43). Most of the charged particles to be detected in contemporary high energy experiments can be approximated as MIPs.

In reality, the ionization process is subject to statistical fluctuations. The value calculated by equation (2.43) gives the average value of the so-called Landau distribution, an example of which is shown in Figure 2.14. For a thin sensor, the

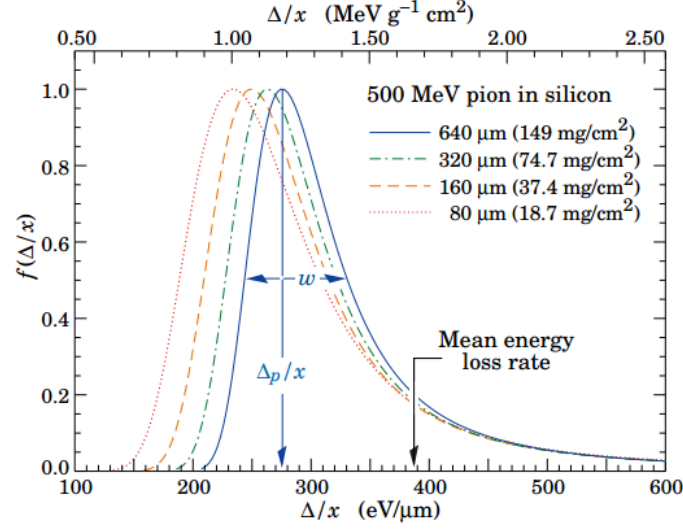


Figure 2.14 – Straggling functions in silicon of 500 MeV pions [35]

response varies around the peak of the distribution with a significant probability of signals belonging to a high energy deposition tail. This peak is called the Most Probable Value (MPV) of the distribution. The average value of the Landau distribution is higher than the MPV due to the tail caused by the so called δ -electron or knock-on electron. These δ -electrons are created by ionization that have enough energy to become ionizing particles themselves.

2.3 Formation of signal in a sensor

In this section, the basic sensor operation principles and the signal formation in a sensor are discussed.

Figure 2.15 shows a simple pixel sensor architecture in a n-type substrate. The

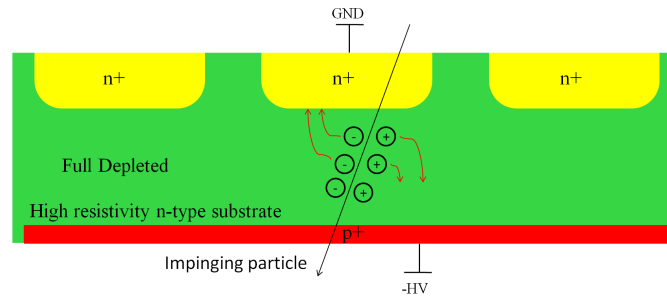


Figure 2.15 – Cross section of a sensor diagram

n^+ implantation on the topside forms the pixelated electrodes and are connected to ground. The uniform p^+ implantation on the backside forms the ohmic

contact and is biased at negative HV. If the HV is strong enough, a full depleted region might be formed due to the reverse biasing of the pn junction. The ionized electrons coming from an impinging particle drift towards the top-side and the holes drift towards the back-side driven by the buildup electric fields in the depletion region. The induced signals in the top-side segmented electrodes are then transmitted to a specific readout chip.

2.3.0.4 Leakage current and capacitance in a sensor

A description of the leakage current has already been introduced in Section 2.1.2.2 and it can be approximately described by Equation 2.39. The depletion depth and pixel capacitance between the pixel electrode and the back-plane depend on the substrate doping and can be calculated by equations 2.37 and 2.41. For the capacitance, one should also consider the capacitance to the neighbor pixels, especially for large edge rectangle pixel layout. The sum of all the inter pixel capacitances is approximately proportional to the perimeter of the pixel and the capacitance also comes from the gap size between the active regions. A signal collected by one pixel can couple in part to the neighbor pixels by these inter-pixel capacitors. This phenomenon is called cross-talk and should as much as possible be avoided.

2.3.0.5 Signal formation

The electron hole pairs generated by ionization drift to the corresponding electrodes due to the electric fields. As soon as the charges start to drift, they start to induce a signal at the electrodes. The instantaneous current induced on an electrode by a moving electron can be expressed by Ramo's theorem [36] :

$$i = e \vec{E}_e \cdot \vec{v} \quad (2.44)$$

where e is the charge, $\vec{v}$ is the drift velocity and E_e is called the weighting field. The weighting field is different from the electric field which is introduced by the applied voltage. To determine the weight field, the electrode under consideration is applied 1 V and the other electrodes are connected to 0 V. A weighting field diagram is illustrated in Figure 2.16. The induced charge, Q , in the time interval $[t_1, t_2]$ from position $\vec{x}_1$ to $\vec{x}_2$ can be integrated over the collection time :

$$Q = \int_{t_1}^{t_2} i(t) dt = e(\Phi_w(\vec{x}_1) - \Phi_w(\vec{x}_2)) \quad (2.45)$$

where Φ_w is the weighting potential. The weighting potential distribution will change significantly for different electrode sizes and wafer thicknesses. Figure 2.17 shows an example one-dimension pixel size of "a" and in this scenario, the po-

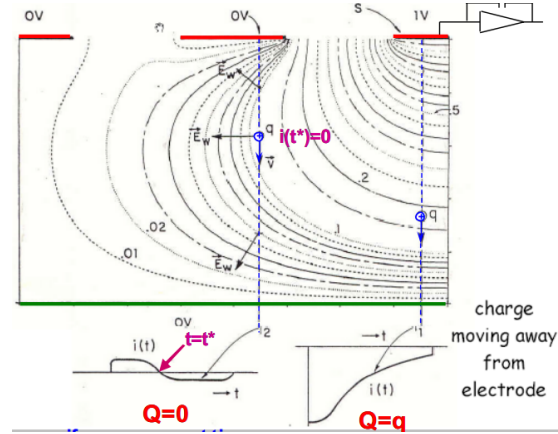


Figure 2.16 – Weighting field and induced current for a pixel [37]

tential can be obtained by [24] :

$$\Phi_w = \frac{1}{\pi} \frac{\sin(\pi y) \cdot \sinh(\pi \frac{a}{2})}{\cosh(\pi x) \cos(\pi x) \cdot \cosh(\pi \frac{a}{2})} \quad (2.46)$$

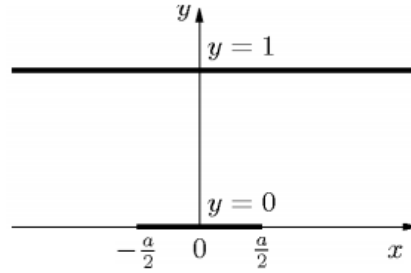


Figure 2.17 – Electrode size for weighting potential calculation

As an example, Figure 2.18 shows the weighting potential with different electrode sizes. Figure 2.18a illustrates the potential with two infinite parallel plates. In this case, the potential varies along one dimension, and the almost equivalent potential indicates that the movement of electrons and holes (assumed in the middle of the sensor) induce the same fraction of signal for an electrode. Figure 2.18b and c show the weighting potential distribution for the electrode/wafer-thickness ratio of 1/3 and 1/10 respectively. One can see that most of the signal is induced when the charges are close to the back-side pixelated electrode, and the charges drifting towards the top-side do not contribute significantly to the signal. For a heavily irradiated silicon sensor, assuming a uniform trapping probability in the substrate, most of the induced signal is lost when the ionized charge is trapped before drifting to the region close to the electrode. Therefore the charge collection efficiency is quite sensitive to the traps induced

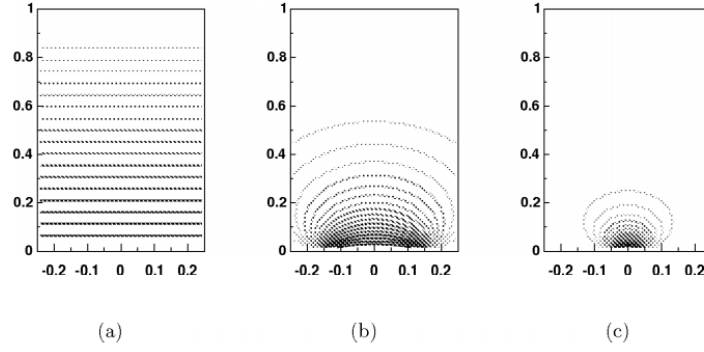


Figure 2.18 – Weighting potential

by irradiation in the case of small pixel pads in comparison to large electrode pads.

2.3.0.6 Spatial resolution

The spatial resolution is determined by the segmentation pitch, the charge sharing with neighbor pixels, the threshold of the readout electronic and how the signals are then being treated in the electronics (binary readout, analog readout, etc...). Here for simplicity of the description only the pixel pitch is considered to describe the detector spatial resolution principle. Let us assume the sensor is read out binarily, the hit probability is uniform and the hit position is between $-\frac{d}{2}$ and $\frac{d}{2}$ (with pixel pitch equals to d). To calculate the resolution, the first step is to normalize the probability distribution function f :

$$\int_{-\frac{d}{2}}^{\frac{d}{2}} f(x) dx = 1 \quad (2.47)$$

which gives $f = \frac{1}{d}$. Then, the resolution can be given by :

$$\sigma = \sqrt{\frac{1}{d} \int_{-\frac{d}{2}}^{\frac{d}{2}} x^2 dx} = \frac{d}{\sqrt{12}} \approx 0.28 \cdot d \quad (2.48)$$

Of course, implementing an analog readout can improve the spatial resolution with specific algorithms, for instance a simple center-of-gravity of the induced charge distribution or the use of an η -function [38].

2.4 Radiation effects

In a silicon sensor, the radiation damage in silicon are divided into bulk and surface defects. The bulk damage is caused by the displacement of crystal atoms.

The surface defect consists of the fixed charge which accumulate in oxide and of the interface traps which build up at the silicon oxide interface. Both types of defects can lead to an increase of the leakage current, an increase of the full depletion voltage, and charge trapping.

2.4.1 Bulk damage

Bulk damage is induced by interaction of the incident particles with the nuclei of the silicon lattice atoms. This kind of energy loss is called Non-Ionizing Energy Loss (NIEL). The energy transferred in the interaction is [39] :

$$\Delta E = 4 \frac{m_p M_{Si}}{(m_p + M_{Si})^2} \sin^2\left(\frac{\vartheta}{2}\right) \cdot E_P \quad (2.49)$$

where m_p and E_P are the mass and energy of primary particle, M_{Si} is the mass of silicon atom, and ϑ is the scattering angle. The displacement of the silicon atom will occur if the energy transferred to the silicon atom is high enough to displace the atom from its initial position in the lattice. The atom is then called primary knock-on atom. A minimum recoil energy E_d of ~ 25 eV [40] is required in order to remove a silicon atom from its lattice position. Electrons need at least 260 keV to provide such a recoil energy in a collision, while protons and neutrons only need 190 eV because of their higher masses. When high energy particles such as protons pass through a silicon sensor, they collide with silicon atoms and remove them from their initial lattice positions, which generate interstitial atoms and vacancies. These defects introduce extra energy levels in the band gap. If the recoil energy of the primary knock-on atom is larger than 130 keV, they can remove other atoms locally, which causes a cluster of defects. According to simulations, these clusters have an inner diameter of about 10 nm surrounded by an about 200 nm wide area with a lower defect density [41]. The interaction characteristics of some important impinging particles and the silicon knock-on atoms are summarized in Table 2.1.

Particle	Interaction	T_{max} [eV]	T_{av} [eV]	E_{min} [eV] (point)	E_{min} [eV] (cluster)
Electron	Coulomb scattering	155	46	260000	4600000
Proton	Coulomb and nuclear scattering	13370	210	190	15000
Neutron	Elastic nuclear scattering	133900	50000	190	15000
Si^+	Coulomb scattering	1000000	265	25	2000

Table 2.1 – Radiation interaction characteristics [33]. The radiation energy is 1 MeV. T_{max} is the maximum possible recoil energy. T_{av} is the average recoil energy. E_{min} is the minimum energy for the generation of a point defect or a cluster defect.

Based on the NIEL hypothesis [42], the displacement damage cross section is

described by [43] :

$$D(E_p) = \sum_i \sigma_i(E_p) \int_{E_{Rmin}}^{E_{Rmax}} f_i(E_p, E_R) P(E_R) dE_R \quad (2.50)$$

where the sum considers all the possible interactions, E_R is the energy of the recoiling nucleus, the function f_i describes the distribution of the recoil atom, and the function $P(E_R)$ [44] is the Lindhard partition function of the energy loss in non ionizing processes. The total displacement damage per volume is

$$T_{dam} = N \cdot t_{exp} \int_0^\infty \varphi(E_p) D(E_p) dE_p \quad (2.51)$$

where t_{exp} is the exposure time, $\varphi(E_p)$ is the differential particle flux, and N is the number of silicon atoms per unit volume. The displacement damage cross section of various particles is plotted in Figure 2.19. 1 MeV neutron is usually used as

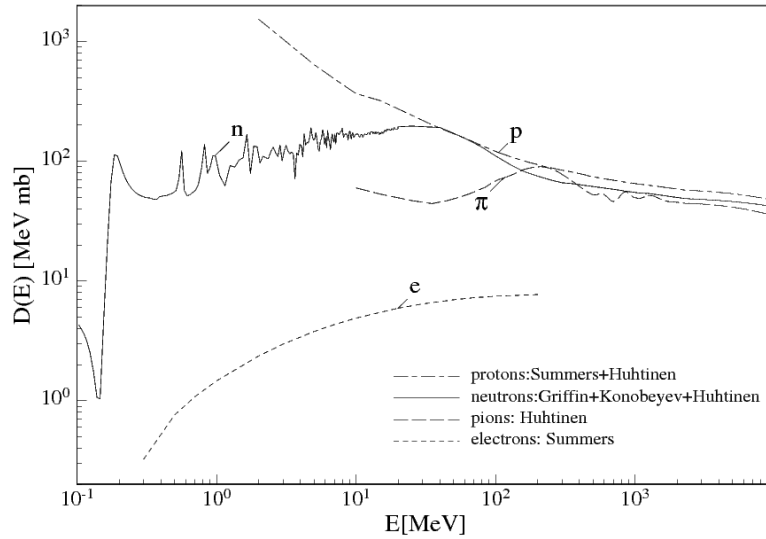


Figure 2.19 – Displacement damage cross section in silicon [45, 46, 47, 48]

the reference particle. The 1 MeV equivalent neutron fluence for an arbitrary particle is :

$$\Phi_{eq}^{1MeV} = k \Phi_{mea} \quad (2.52)$$

where k is called the hardness parameter and defined as :

$$k = \frac{1}{D_n(1MeV)} \frac{\int_{E_{min}}^{E_{max}} \varphi(E_p) D(E_p) dE_p}{\int_{E_{min}}^{E_{max}} \varphi(E_p) d(E_p)} \quad (2.53)$$

The k factor for 1MeV neutron is defined as 1 and the corresponding value of $D(1MeV)$ is 95 MeV mb. The k factor values are listed in Table 2.2 for two irra-

diation facilities which are commonly used in our project.

Source	Particle	Hardness factor
CERN PS	protons, 24GeV	0.5
Ljubljana	Neutron fission spectrum	0.75

Table 2.2 – Hardness factor for two irradiation facilities

Some example point defects are illustrated in Figure 2.20 for n-type silicon. Silicon interstitials and vacancies, as primary defects, are still mobile and not stable at room temperature. Part of these defects will anneal either by an inter-

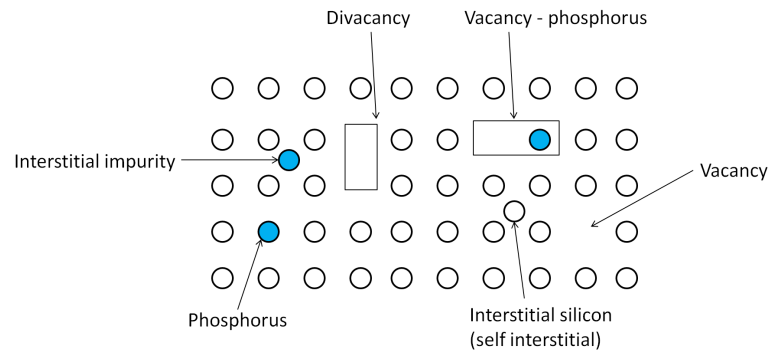


Figure 2.20 – Diagram of point defects in n-type silicon

stitial filling a vacancy or by diffusing out of the surface [33]. But the primary defects can also interact with other defects and therefore form new defect states which become then immobile at room temperature.

The formation of defects complexes is complicated and not fully understood in semiconductors. Furthermore, the silicon wafer production technology also plays an important role in the defects types, e.g. oxygen and carbon interstitials. A part of defect complexes we known is given in Table 2.3.

Here the E-center defect (vacancy-phosphorus complex) formation is discussed as an example as it has its importance in our devices. The donor, phosphorus, is captured by a vacancy right next to it, and forms a new defect complex. The new defect complex may have a different charge state, and change the previous donor charge state from positive to neutral in the space charge region. This phenomenon is called donor removal.

As discussed above, the radiation defects can introduce additional charge states, therefore they are able to change the effective doping concentration. Space-Charge Sign Inversion (SCSI) is predicted and then observed by experiments, and it can be explained by the donor removal and the acceptor state creation during the irradiation. It describes a phenomenon in which the space-charge sign changes from negative to positive with increasing radiation fluence for a n-type

Defect	Charge state	Energy level
interstitial	I^-	$E_C - 0.39$
	I^0	
	I^+	$E_V + 0.4$
vacancy	V^{--}	$E_C - 0.09$
	V^-	$E_C - 0.4$
	V^0	
	V^+	$E_V + 0.05$
	V^{++}	$E_V + 0.13$
divacancy	V_2^{--}	$E_C - 0.23$
	V_2^-	$E_C - 0.39$
	V_2^0	
	V_2^+	$E_V + 0.21$
A-center	$(V - O)^-$	$E_C - 0.18$
	$(V - O)^0$	
E-center	$(V - P)^-$	$E_C - 0.44$
	$(V - P)^0$	
boron interstitial	B_I^-	$E_C - 0.45$
	B_I^0	
	B_I^+	$E_V + 0.12$
vacancy boron	$(V - B)^0$	
	$(V - B)^+$	$E_V + 0.45$

Table 2.3 – Characteristics of some defects in silicon [33, 49]

silicon, as shown in Figure 2.21. The material effective doping density decreases

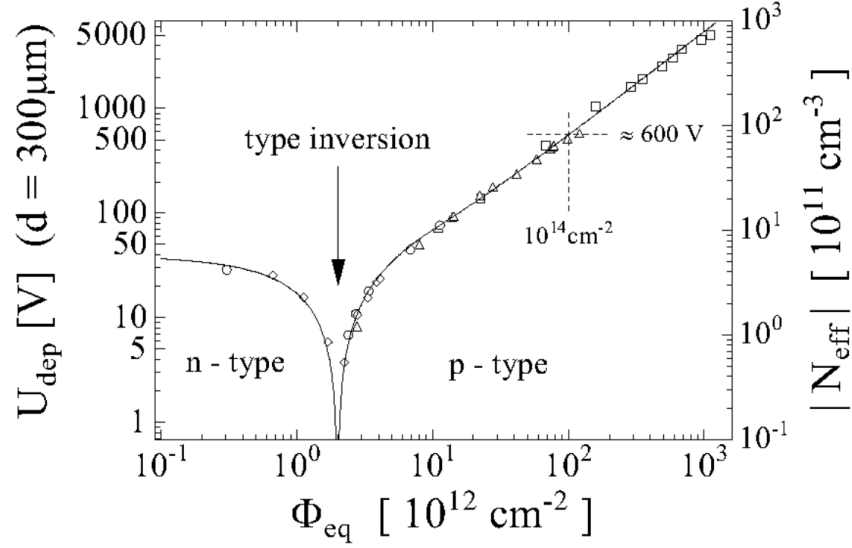


Figure 2.21 – Effective doping concentration as a function of 1 MeV neutron equivalent fluence for n-type silicon [50]

with fluence until the fluence up to the order of $2 \sim 5 \cdot 10^{12} \text{ cm}^{-2}$ is reached. At this point, the material becomes intrinsic. Above this value, type inversion is observed, and the doping changes to effectively p-type and eventually rises linearly with fluence [51, 52].

The radiation defects introduce energy levels in the band gap, which play roles as generation-recombination centers. The additional energy levels decrease the generation life time τ_g , therefore increase the volume generation current I_{vol} as a function of fluence :

$$\frac{\Delta I_{vol}}{V} = \alpha \Phi \quad (2.54)$$

where V is the biasing voltage, Φ is the radiation fluence, and α is defined as leakage current constant. The life time variation can be described as [50] :

$$\frac{1}{\tau_g} = \frac{1}{\tau_{(g,0)}} + k_\tau \Phi \quad (2.55)$$

where $\tau_{(g,0)}$ is the generation life time before irradiation. The relationship between α and k_τ is :

$$\alpha = q n_i k_\tau \quad (2.56)$$

Radiation induced defects behave also as trapping centers. Most of the trapping centers are unoccupied due to the lack of free carriers in the space-charge region. The traps can hold some signal charges longer than the charge collection

time, therefore reduce the Charge Collection Efficiency (CCE). The trap models will be discussed in Chapter 4.2.5.

2.4.2 Surface damage

In silicon sensor (as in silicon CMOS process), the surface region is also sensitive to the ionizing radiation. The ionizing particles passing through the silicon dioxide produce defects both in the oxide and on the silicon-oxide surface, called total-ionizing-does (TID) effect. The initial exploration of TID degradation in MOS devices has been carried out at the Naval Research Laboratory (NRL) in 1964 [53] and much effort in this field has been done since then [54]. The TID effect should be investigated for the HV/HR CMOS sensors due to the implemented CMOS electronics inside the pixel.

In this section, the TID effect in a MOS device is discussed. Figure 2.22 shows the energy band diagram and the basic processes occurring in the Si/SiO_2 for a NMOS device with positive biasing at gate. Many publications [59, 56, 57, 58]

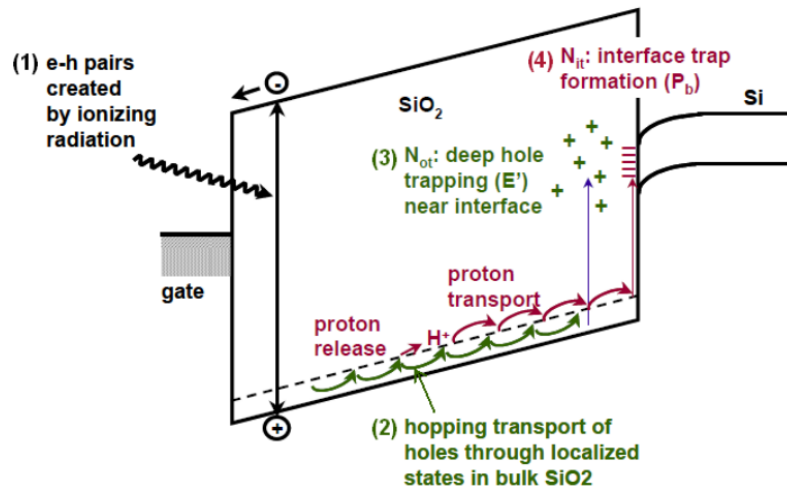


Figure 2.22 – Diagram of energy band for a NMOS structure [55]. (1) basic ionizing processe, (2) hole transport (3) hole trapping and (4) interface trap defects.

have described these processes in details. In this section, these four processes are summarized briefly.

The ionizing impinging particles, e.g. X-ray, Co-60 electrons, protons, deposit part of their energy and thereby generate electron hole pairs. The derived unit of TID in the International System of Units (SI) is gray, denoted as Gy, with $1\text{ Gy} = 1\text{ J/Kg}$. The unit "rad" (radiation absorbed dose) is more conventionally used in the high energy physics domain with the relation $1\text{ rad} = 100\text{ erg/g} =$

$6.24 \times 10^{13} \text{ eV/g} = 0.01 \text{ Gy}$. The required energy to generate one electron hole pair in the SiO_2 , E_p , is $17 \pm 1 \text{ eV}$ [60]. The generated pair density is described by a conversion factor g_0 and given by :

$$g_0 \left[\frac{e-h \text{ pairs}}{\text{cm}^3 \cdot \text{rad}} \right] = 100 \left[\frac{\text{erg}}{\text{g}} \right] \left[\frac{1}{\text{rad}} \right] \cdot \frac{1}{1.3 \times 10^{-12}} \left[\frac{\text{eV}}{\text{erg}} \right] \cdot \frac{1}{E_p} \left[\frac{\text{ehps}}{\text{eV}} \right] \cdot \rho \left[\frac{\text{g}}{\text{cm}^3} \right] \quad (2.57)$$

The conversion factors for various materials are listed in Table 2.4 [60]. In SiO_2 ,

Material	E_p [eV]	Density [g/cm ³]	g_0 [ephs/cm ³ · rad]
Silicon	3.6	2.328	4×10^{13}
GaAs	~ 4.8	5.32	7.6×10^{12}
SiO_2	17	2.2	8.1×10^{12}

Table 2.4 – Ionizing conversion factor for various materials

the conversion factor is $8.1 \times 10^{12} \text{ cm}^{-3} \text{ rad}^{-1}$.

It can first be noted that a fraction of the generated electron hole pairs recombine right away. They do not contribute to the building of the long time defects in the SiO_2 and at the interface. In SiO_2 , the electron mobility is approximately $20 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ [61] at room temperature, whereas the hole mobility is between 10^{-4} and $10^{-11} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ [62] depending on temperature and electric field. Therefore the electrons are swept out of the oxide quickly whereas

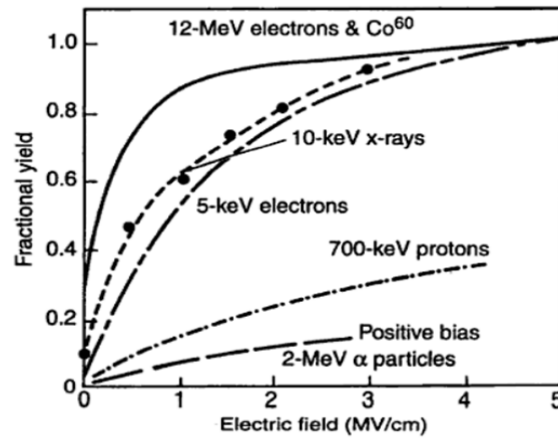


Figure 2.23 – Fraction of yield from initial recombination as a function of electric field in oxide depending on radiation type [63]

the holes stay in the SiO_2 much longer. The electron mobility determines the initial recombination fraction and the fraction of holes that remains. The holes are relatively immobile and thereby can survive from the initial recombination.

Depending on the polarity of the NMOS structure, the surviving holes that do not recombine in SiO_2 are transported towards the Si/ SiO_2 interface resulting in a long time TID effect. Because the hole mobility is proportional to the electric field, the fraction of holes surviving the initial recombination depends on the electric field in the SiO_2 . The so-called fractional yield is shown in Figure 2.23 as a function of electric field for a few impinging particles. The hole fractional yield can be approximated empirically by [64] :

$$f_y(E_{ox}) = \left(\frac{|E_{ox}|}{|E_{ox}| + E} \right)^m \quad (2.58)$$

where E_{ox} is the electric field of oxide. For X-ray irradiation, $E = 1.35$ MV/cm and $m = 0.9$.

Within few nanometers from the Si/ SiO_2 interface on the SiO_2 side, oxygen vacancies have been formed due to incomplete oxidation during the material processing. These oxygen vacancies introduce deep-level hole trapping centers, called E' center [65], formed by two silicon atoms joined by a weak strained Si-Si bond with a missing oxygen atom, as shown in Figure 2.24. Part of the holes

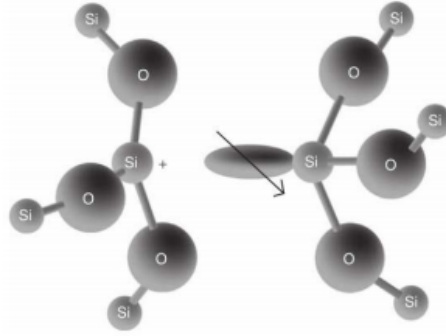


Figure 2.24 – Diagram of E' center [66]

drifting to the interface can be captured by the E' center, and therefore form a positive charge region near the interface. This process can be expressed as :



where T_{ox} is the trapping center, p is the hole, and T_{ox}^+ is the positive trapping center that is fixed due to the deep energy level. This positive trapping, however, can be neutralized by capturing an electron as expressed :



The fixed charge density can be approximately calculated by the function [67],

$$N_{ot} = g_0 \cdot D \cdot f_y(E_{ox}) \cdot f_{ot} \quad (2.61)$$

where D is the total dose, g_0 is the conversion factor, $f_y(E_{ox})$ is the hole fractional yield and f_{ot} is an empirical factor which depends on the oxide thickness and the oxide growth technological process [68]. A saturation of the fixed charge buildup has been observed due to the limited semi-permanent traps in the SiO_2 . The oxide growth quality influences the saturation value significantly. A typical value of N_{ot} for high quality thermal grown oxide is $3 \times 10^{12} \text{ cm}^{-2}$ [69].

The second long time component related to the TID is the production of interface traps at the Si/SiO_2 interface after hole hopping transport. Unlike the fixed oxide charge N_{ot} , the energy levels of the interface traps are localized in the band gap and contribute to the surface current generation. Figure 2.25 shows the Si/SiO_2 interface formation for different orientations. The interface traps are also denoted as P_b [70] and P_{b0} [65, 71] centers, consisting of Si bonds that dangle into the oxide, for $\langle 111 \rangle$ and $\langle 100 \rangle$ silicon wafers respectively, as shown in Figure 2.26. These trap states can be filled by electron or hole, and

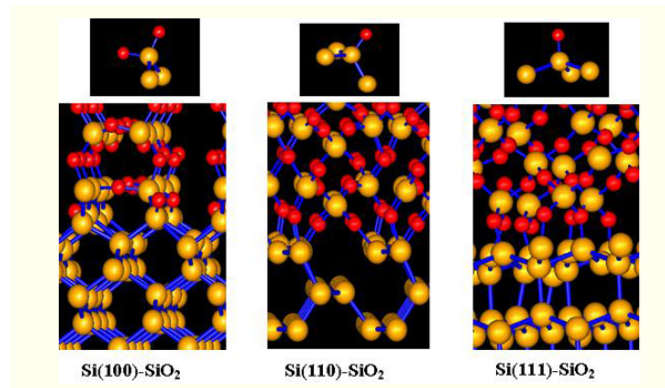


Figure 2.25 – Si/SiO_2 interface formation for different orientations

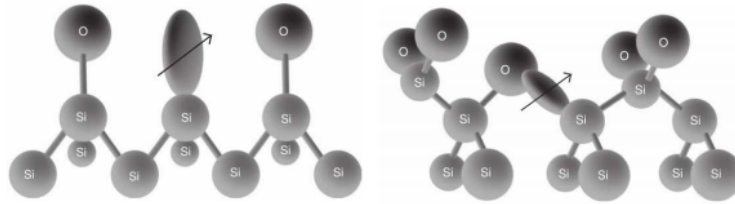


Figure 2.26 – Diagram for P_b and P_{b0} centers [66]

these processes can be expressed by :





Most of the dangling-bond defects have been passivated by the annealing step after the oxide generation, and do not lead to trap electrons and holes. However, molecular hydrogen (H_2) is introduced intentionally and unintentionally during the oxide growth process [72]. The holes transporting to the interface have possibility to interact with the hydrogenated oxygen vacancies, which can release protons and this process can be described by :



The passivated P_b centers in the annealing can then be broken by the protons (break the hydrogenated silicon bonds SiH), and create the dangling silicon bonds. These process can be expressed by :



The interface traps density, N_{it} , can be described empirically as [73] :

$$N_{it} = a_{it} \cdot D^{b_{it}} \quad (2.68)$$

where D is the dose value, and a_{it} and b_{it} are fitting parameters which should be tuned for specific technologies. The parameterization of the interface trap density is discussed in Chapter 4.2.5.

In sub-micron technologies, for instance 65 nm technology, the reduced gate oxide thickness has improved the radiation hardness due to annealing coming from quantum tunneling. However, the few hundreds nanometers Shallow Trench Isolation (STI) field oxides are still subject to TID effects, as shown in Figure 2.27, and in smaller scale technologies they influence the post-radiation device characteristics (much effort has been performed in the ATLAS RD53 [74] collaboration [75]).

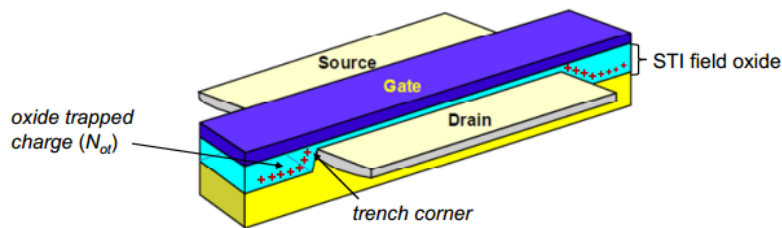


Figure 2.27 – TID effect in STI [76]

3 ATLAS cylinder pixel detector technologies and HV/HR CMOS sensors

The layout of the ATLAS experiment has been introduced in Section 1.2.2. In this section, we will focus on the ATLAS the hybrid pixel detector technologies and its 2014 upgrade, the IBL. We will introduce the FE-I4, the readout IC for the IBL, and focus on the Generic ADC block as well as its calibration. The HV/HR CMOS sensor operation concepts and the HV/HR CMOS prototype architecture will then be introduced.

3.1 The hybrid pixel detector of ATLAS

The ATLAS pixel detector consists of three cylinder layers with end-caps. It uses a so-called “hybrid pixel” technology which consists of a layer of sensing material (usually in silicon) connected by indium bump-bonding technology [77] to an electronics chip for readout. The sensor is used for charged particles detec-

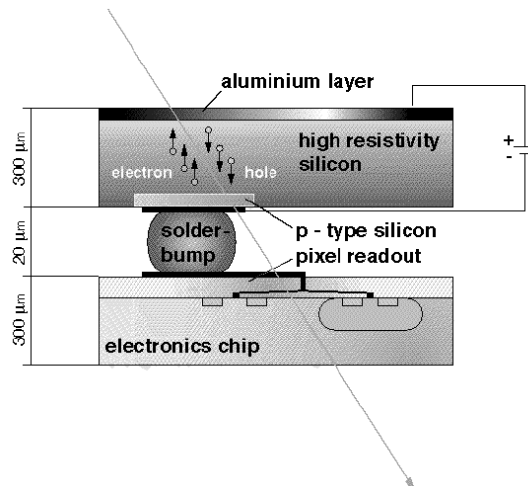


Figure 3.1 – Schematic of a hybrid pixel detector

tion, and the electronics treats the signals recorded in the sensor. The schematic of a hybrid pixel detector is shown in Figure 3.1. In Section 3.1.1, an introduction to planar sensor for the ATLAS initial 3-layer pixel system is discussed. The dedicated read out chip, called FE-I3 [11], is also introduced in Section 3.1.2.

3.1.1 Planar sensor for the initial ATLAS 3-layer pixel detector

The ATLAS pixel sensor is made of an array of diodes implemented on a high resistivity n-type substrate, as shown in Figure 3.2. The sensor thickness is $256 \pm$

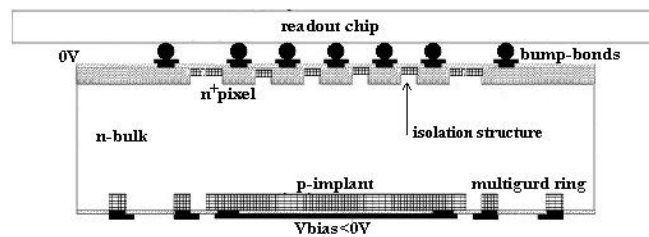


Figure 3.2 – Schematic of ATLAS planar sensor

$3\mu m$. For each sensor tile, the 47232 pixel implants are arranged in 144 columns and 328 rows [78], which amounts to 41984 pixels of size $400 \times 50 \mu m^2$ and 5248 pixels of size $600 \times 50 \mu m^2$. Oxygen impurities have been introduced in the bulk to increase tolerance of the silicon against bulk damage caused by charged hadrons [79]. Full depletion is obtained with few tens of volts biasing before irradiation. As discussed in Section 2.1.5, the full depletion voltage needs to be rise and the leakage current increases with the accumulated radiation dose throughout the detector lifetime.

3.1.2 Readout electronics

When a particle goes through the sensor, it creates eh pairs by ionization. The electrons are collected thanks to the biasing of the sensor through the bump bonds, and the corresponding signal is transferred to a readout ASIC. Three versions of the readout chip were produced (FE-I1, FE-I2 and FE-I3). The final version used in the experiment is FE-I3, which was fabricated in a commercial $0.25 \mu m$ CMOS process with radiation tolerant layout. Each chip contains 2880 pixels with $400 \times 50 \mu m^2$ pitch arranged in an 18×160 matrix. The chip schematic is shown in Figure 3.3. Each pixel cell contains an analog block in which the signal from the sensor is amplified by a charge sensitive preamplifier and compared to a programmable threshold by a discriminator. The digital readout part which follows this analog block transfers the hit information with pixel address, hit leading edge time stamp, and trailing edge time stamp to the buffers at the

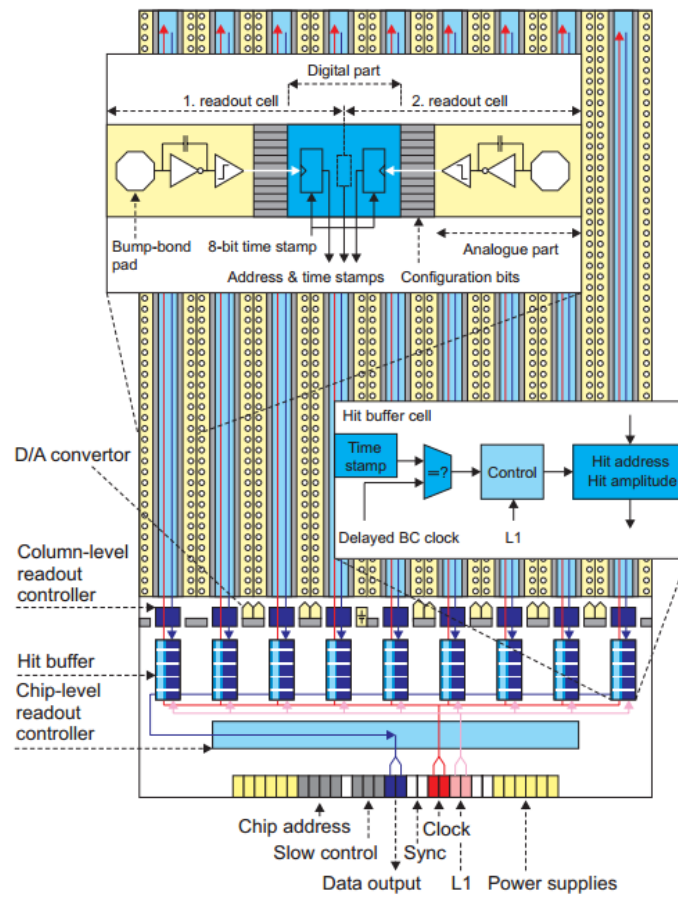


Figure 3.3 – Schematic of the FE-I3 readout chip with its main functional blocks highlighted (not to scale) [11]

chip periphery. A Time-Over-Threshold (TOT) information is extracted from the leading and the trailing edge time stamps and this information is proportional to the charges collected in the sensor. More information about this IC can be found in [11].

3.2 The IBL project

During the year 2014, ATLAS was under the Phase-0 upgrade. In the center of the initial ATLAS 3-layer pixel detector, a new layer was inserted together with a new beam pipe of reduced radius (from 36 mm initially to 29 mm) : this project was called the IBL. The project motivation has been described in Chapter 1. The IBL module is discussed in Section 3.2.1 and the calibration of the GADC for the FE-I4, the new IBL pixel readout ASIC, is described in details in Section 3.2.2 as this is part of my research work. Figure 3.4 shows a picture

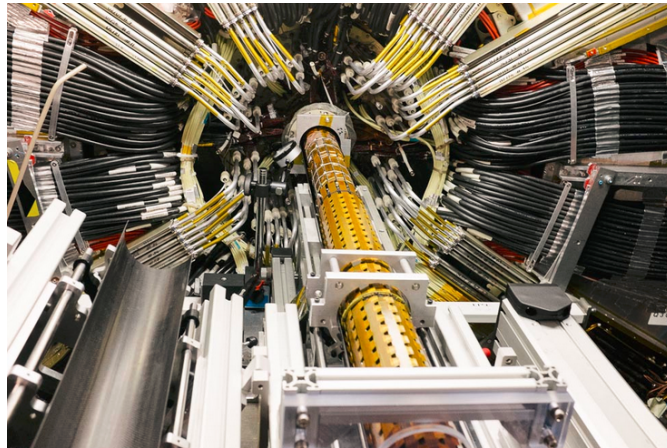


Figure 3.4 – Photograph of IBL installation

of the IBL during the installation taken from the side of the opened up ATLAS detector. The stave arrangement is shown in Figure 3.5. The IBL consists of 14 staves surrounding the beam pipe. Each stave consists of a mechanism structure, cooling pile, service, sensors and 32 FE-I4 chips. Each one or two FE-I4 chip(s) and a sensor are the base elements of a module. The modules are described in next section.

3.2.1 The IBL module

The IBL module is based on the new readout integrated circuit, FE-I4. Two kinds of modules were designed for the IBL. In each stave, the central 12 modules use planar sensors, whereas the outer 4 modules use 3D sensors. A sketch of the planar double-chip module size and an assembly are shown in Figure 3.6.

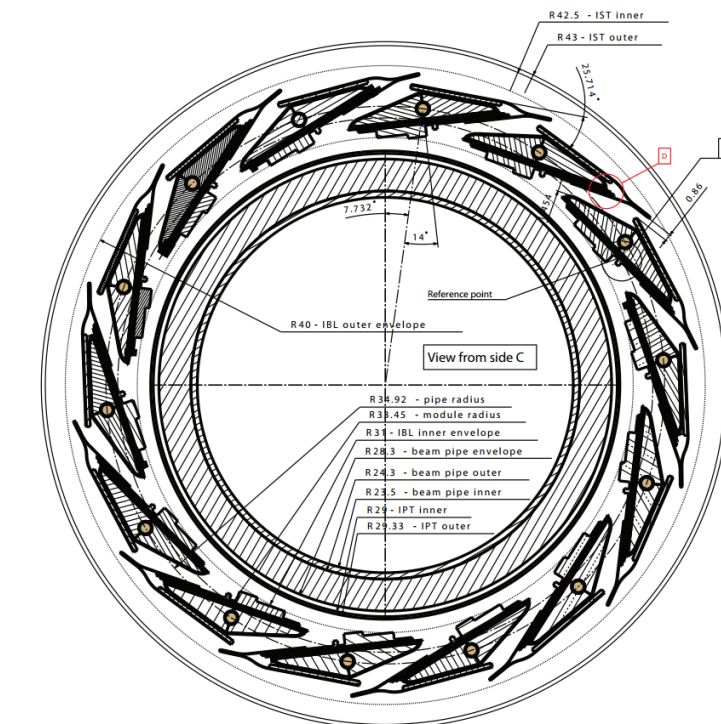
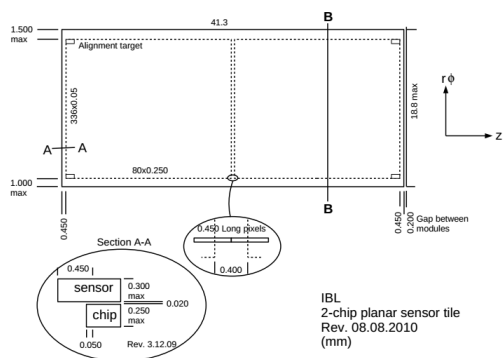
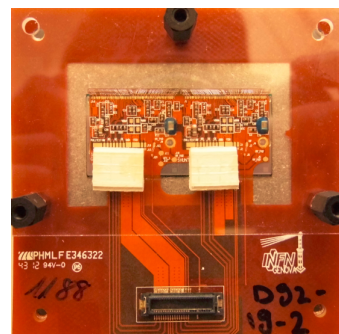


Figure 3.5 – IBL layout in $r\Phi$ view



(a) The IBL double-chip module [80]



(b) A picture of the IBL double-chip module

Figure 3.6 – (a) : A sketch of the IBL double-chip modules. (b) : A photo of the IBL double-chip modules.

3.2.1.1 Planar sensor

The IBL planar sensors use an n-in-n design on diffusion oxygenated float-zone (DOFZ) silicon wafers fabricated by CiS [81]. The wafer thickness is $200\mu m$ with $2 - 5 k\Omega \cdot cm$ resistivity. The sensor layout is very similar to the previous 3-layer

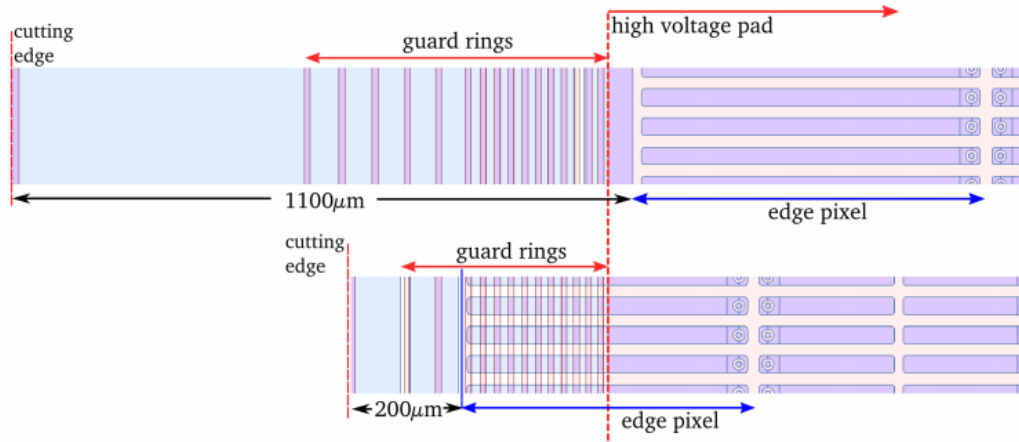


Figure 3.7 – Comparison of the edge region of the initial ATLAS 3-layer pixel sensor and of the IBL pixel sensor with slim edge [82]

ATLAS pixel sensor layout [78] with a reduced pitch of $250\mu m \times 50\mu m$ to match the new pixel electronics size. A new feature of this design is the slim edge to reduce the inactive edge region, as shown in Figure 3.7. The edge pixels are enlarged to $500\mu m \times 50\mu m$ to accommodate the region between two FE-I4 chips. The floating guard rings generate potential drop via punch through effect from high voltage to ground in order to reduce the leakage current due to the edge defects.

3.2.1.2 3D sensor

3D sensors have also been used in the IBL for the 4 outermost modules at the extremities of each stave. They have faster charge collection time and improved radiation hardness compared to planar sensor. The 3D sensor fabrication used a combination of two well established industrial technologies : MEMS (Micro-Electro-Mechanical Systems) and VLSI (Very-Large-Scale Integration) [82]. 3D sensors were manufactured in 4 inches float zone (FZ) p-type high resistivity wafer by two foundaries, CNM [83] and FBK [84]. The wafer thickness is $(230 \pm 20)\mu m$.

A sketch of the sensor cross sections for the two foundaries is shown in Figure 3.8. The charge carriers drift towards the electrodes parallel to the sensor surface with a typical distance between the electrodes of $50\mu m$. Compared with

planar sensor, the distance of charge collection can be several times shorter and the full depletion voltage is also smaller. Both kinds of sensors are similar, and

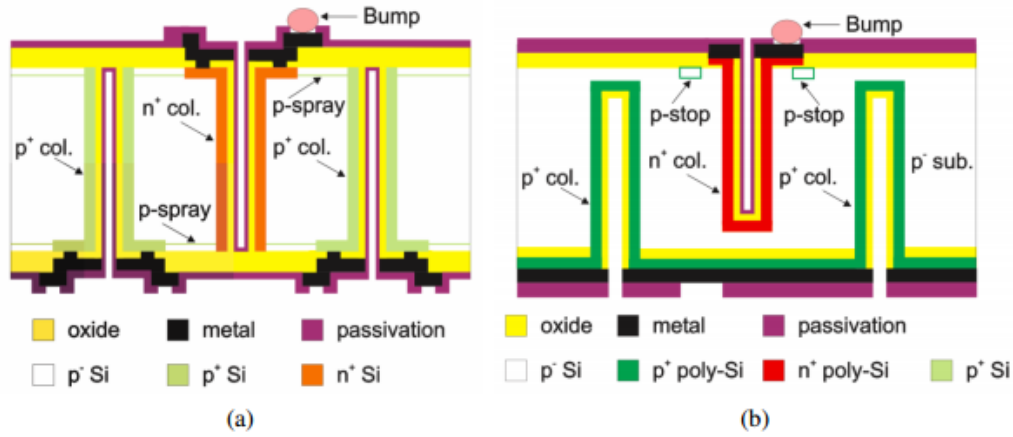


Figure 3.8 – 3D sensor schematics for the FBK (left) and CNM (right) processes [82]

the main difference is the depth of the electrode columns. The columns cross completely the substrate in the FBK process, whereas the columns stop at a short distance from the surface in the CNM process. Another difference is the pixel isolation implementation. Double sided p-spray implantation is used for FBK and p-stop implantation is chosen for the CNM.

3.2.1.3 The FE-I4 readout IC

The previous readout IC, FE-I3, could not withstand the expected occupancy and radiation dose at the reduced radius where the IBL is mounted. Therefore a new readout IC was developed for the IBL, called FE-I4 [85]. The FE-I4 size is $20.2 \text{ mm} \times 18.8 \text{ mm}$. It contains 26 880 pixels arranged in 80 columns and 336 rows with $250 \mu\text{m} \times 50 \mu\text{m}$ pitch. A photographic comparison between FE-I4 and FE-I3 is shown in Figure 3.9 to scale. It is manufactured in a 130 nm CMOS technology using thin gate oxide transistors in order to improve radiation hardness.

A functional diagram of the FE-I4 is shown in Figure 3.10. The FE-I4 pixel array is arranged in double-columns, which are further divided into 2×2 pixel regions. Each region contains 4 identical analog pixels, followed by a discriminator, and one shared memory and logic block called Pixel Digital Region (PDR) [86]. A physical event is measured by the discriminator firing time encoded with the Time Over Threshold (TOT) with 4-bit resolution in counts of a 40 MHz clock. The firing times of all discriminators can be recorded in the chips for a programmable latency interval of up to 255 clocks. Within this time interval,

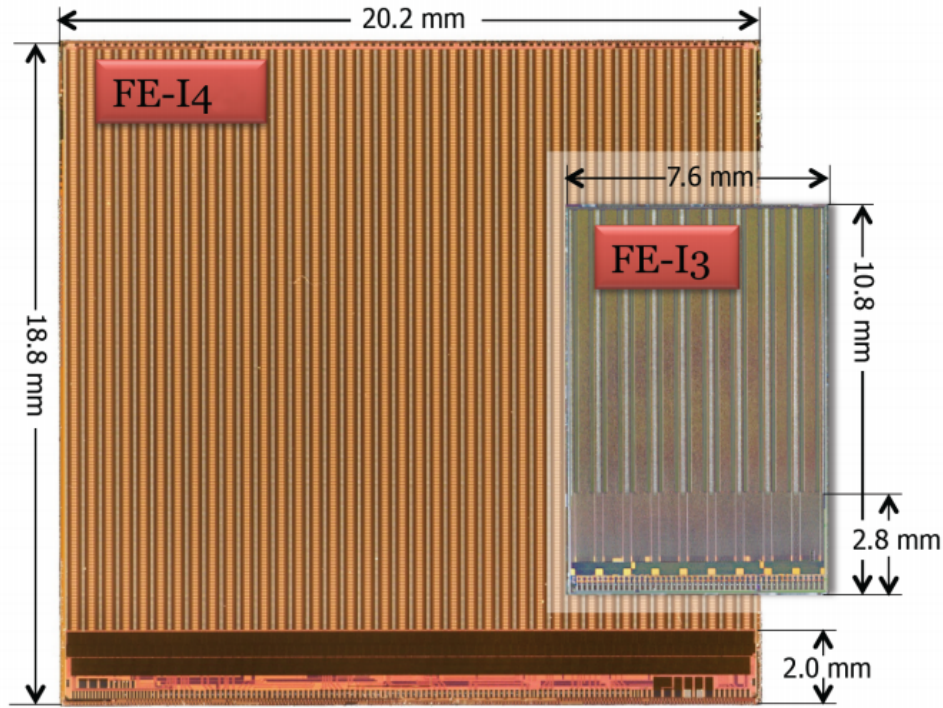


Figure 3.9 – A comparison of the FE-I4 size and the FE-I3 size

the information can be read out via the serial LVDS output if an external trigger arrives.

Each synchronized discriminator output is further processed by applying a digital cut on the TOT. Hits smaller than a certain TOT (programmable between 1 and 3 clock periods) are classified as “small hits” and those larger as “large hits” [86]. The hits that do not go over the threshold in the correct trigger window, but cross the threshold just after the trigger window, are classified as “late hits”.

The analog part of each pixel consists of a two-stage amplifier followed by a discriminator, which is shown schematically in Figure 3.11. The preamplifier is AC coupled to the second amplifier. The feedback currents of the 2 stages can be tuned respectively by V_{fb} and V_{fb2} . A 4-bit local feedback tuning DAC, FDAC, is implemented for the preamplifier. The FDAC allows to find adjustment for the shaping time of amplifier which affects the ToT length for a specific injected charge. Two capacitors are implemented for analog test signal injection. The capacitances by design are 1.95 fF and 3.90 fF respectively. The two capacitors can be connected in parallel resulting in a designed capacitance of 5.85 fF. A digital test signal injected after the discriminator output can be fed directly to the column-parallel wired-OR circuit (HitOR). This function is designed for test purposes.

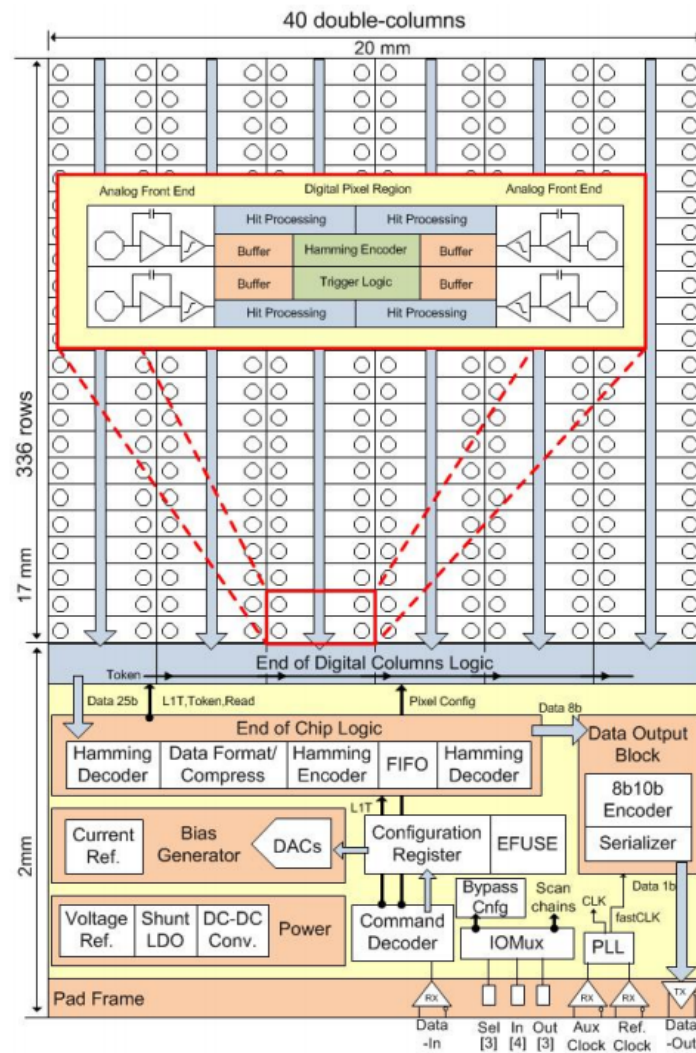


Figure 3.10 – FE-I4 functional diagram [82]

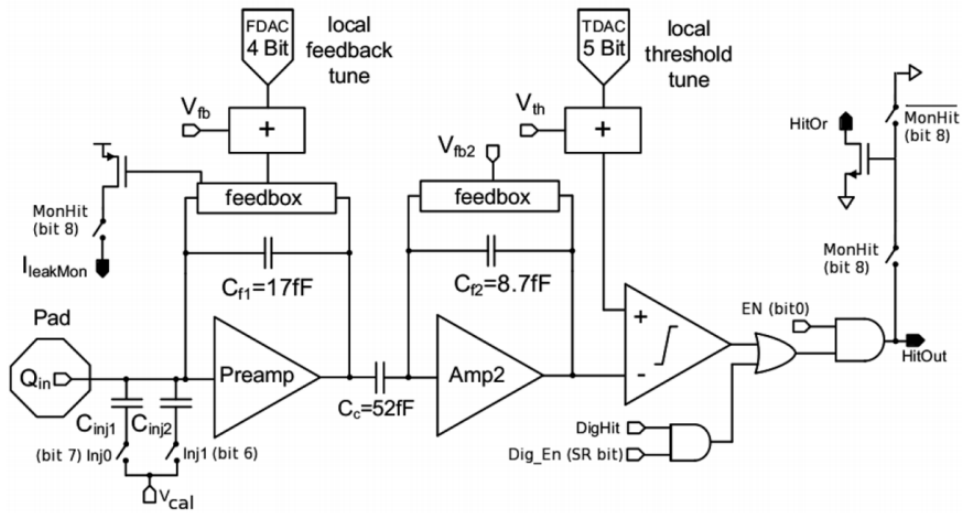


Figure 3.11 – FE-I4 analog block schematic

The 80 columns are arranged in 40 Digital Double Columns (DDC) connected together via the End of Double Column Logic (EODCL). Each DDC contains 168 Pixel Digital Regions (PDR). Four pixel discriminator outputs are transferred to one PDR. The functional blocks of a PDR is shown in Figure 3.12. The

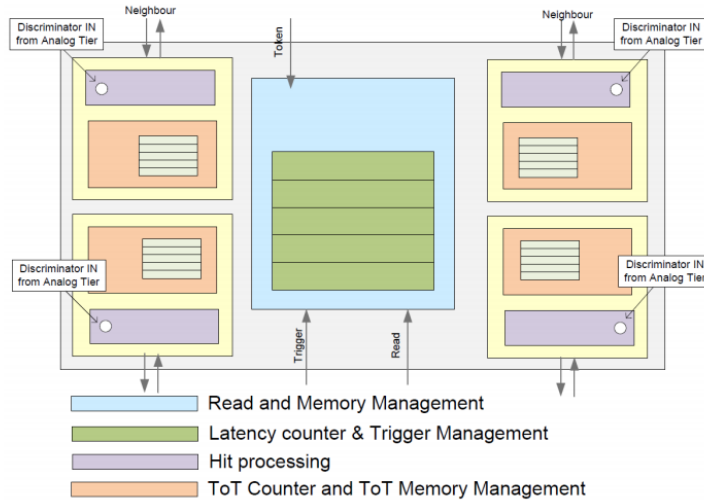


Figure 3.12 – Pixel digital region (PDR) diagram

PDR contains five latency counters, however, each pixel have independent ToT counters. Once a hit occurs within the 4-pixel group, the PDR allocates the first unallocated latency counter to start counting. The hit information will be transferred to the EODCL if a Level-1 trigger arrives in time, after the user defined

Level-1 trigger latency.

3.2.2 FE-I4 GADC calibration

In order to monitor and test the FE-I4, a Generic ADC (GADC) is implemented in the periphery of the FE-I4. The GADC is a general purpose 10 bit Analog to Digital Converter (ADC). It consists of two main blocks : an input analog multiplexer to select the input, followed by a 10 bit Successive Approximation Register (SAR) ADC, as shown in Figure 3.13.

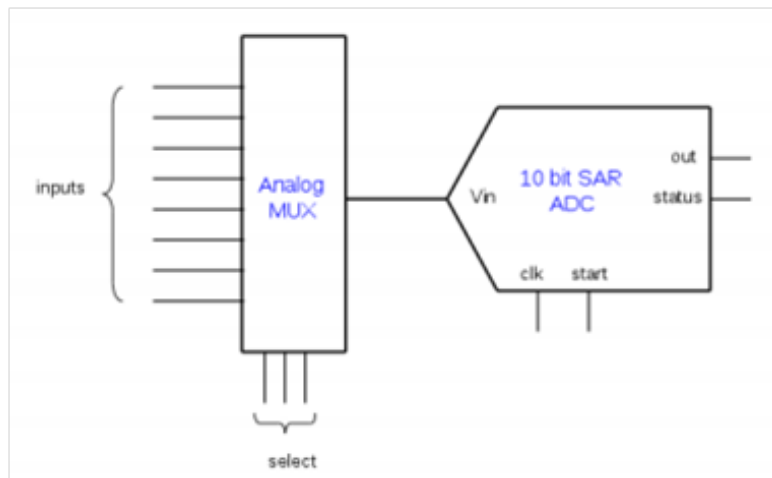


Figure 3.13 – Diagram of the GADC

The GADC has 8 inputs as listed in Table 3.1. The GADC needs a reference voltage to operate. The GADC must be calibrated in order to compensate for its intrinsic offset and also for the reference voltage dependence to the temperature. Therefore it is mandatory to set up the following calibration procedure in order

GADC Select Code	Input signal
0	Temperature sensor
1	GADC reference voltage for testing
2	Analog ground for testing
3	Analog MUX output
4	Analog regulator current sense
5	10 bit DAC output (input to the calibration voltage pulser)
6	Half of regulated analog voltage
7	Ileak leakage current bus into 90 kΩ or 10 kΩ, depending on range bit (ILR)

Table 3.1 – GADC inputs

to get a 1 mV designed precision in the measurements. Such precision is necessary for the temperature monitor resolution of 2 °C. The basis of this calibration

procedure is the precise measurement of the VDDA voltage of the chip. Indeed one of the eight GADC inputs being exactly the half of VDDA, this input is used to calibrate the GADC with this known absolute voltage.

The first step is the investigation of the VDDA voltage variation with the DAC, VrefAnTune. The function of the VrefAnTune DAC is the adjustment of the analog ShuLDO voltage. The scan of VDDA versus VrefAnTune is shown in Figure 3.14a. The FE-I4 nominal VDDA voltage is 1.4 V. The VrefAnTune value is therefore de-

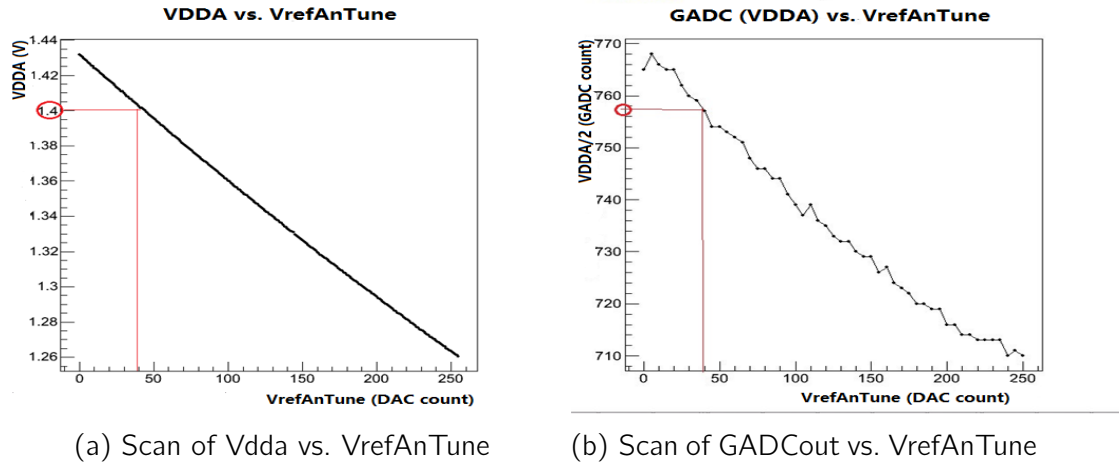


Figure 3.14 – (a) The VDDA values measured by a multi-meter as a function of the VrefAnTune DAC value. (b) The GADC output as a function of the VrefAnTune DAC value.

termined corresponding to $VDDA = 1.4$ V. One of the GADC inputs is $VDDA/2$. Therefore a GADC output of half VDDA can be measured with different VrefAnTune value. The scan of GADC out versus VrefAnTune is plotted in Figure 3.14b and the GADC count corresponding to half the VDDA voltage (700 mV) is obtained from this scan.

The other GADC input is the pulser voltage. The scan of GADC out versus PlsrDAC can be performed as shown in Figure 3.15, where the PlsrDAC is used to change the calibration injection voltage value. Assuming the pulse generator has no offset, the PlsrDAC LSB (least significant bit) can be calculated directly by dividing the $VDDA/2$ voltage by the corresponding PlsrDAC value. Then, one fits this curve with a linear function resulting in two fitting parameters, p_0 and p_1 . The parameter p_0 is the pedestal (offset) of the GADC and the LSB of the GADC can be calculated by the formula :

$$LSB_{GADC} = \frac{LSB_{PlsrDAC}}{p_1} \quad (3.1)$$

Now the GADC output can be calibrated with the value of the LSB and its pedes-

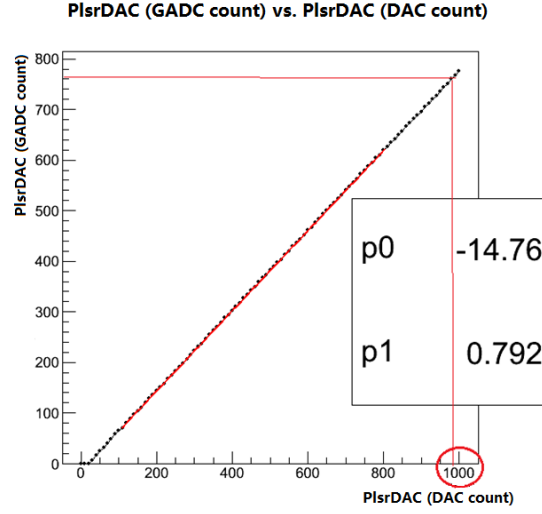


Figure 3.15 – Scan of GADCout vs. PlsrDAC

tal. An example for a GADC output value of half VDDA is given by :

$$V_{VDDA/2} = (GADC_{out} - pedestal) \times LSB \quad (3.2)$$

To verify the hypothesis of PlsrDAC offset, two FE-I4 modules which have positive GADC offsets are investigated. The GADC out difference between GNDA and PulserDAC=0 is only 2 ADC counts, which results in 0.2% error. Therefore this offset can be neglected.

A few issues exist with the above discussed calibration procedure. The first issue is the noise of the GADC output. The GADC output has large fluctuation with respect to the value of the VrefAnTune, as shown for a sample in Figure 3.16a, which influences the precision of the searching of the half VDDA GADC output value.

In order to improve the calibration precision, a quadratic polynomial fit is performed for this curve, using a "robust" [87] fitting method with robustness value set to 0.75, as shown in Figure 3.16b. This so called robust method means the dataset has outliers and the outliers are partially removed. A robustness factor of 0.75 means at least 75% data points are used as good points.

The second issue derives from the GADC out versus PlsrDAC plot. Some pulser outputs are stuck to a specific value as shown in Figure 3.17a. To improve the fitting precision, the stuck points are removed first then the linear fitting is performed as shown in fig 3.17b.

The above mentioned calibration algorithm is based on the precise measurement of VDDA. Unfortunately, the shunt regulator output of FE-I4 is subject to temperature. Five chips were tested at different temperature, which were all tuned to 1.4 V at room temperature (20 °C). The VDDA voltage variation with

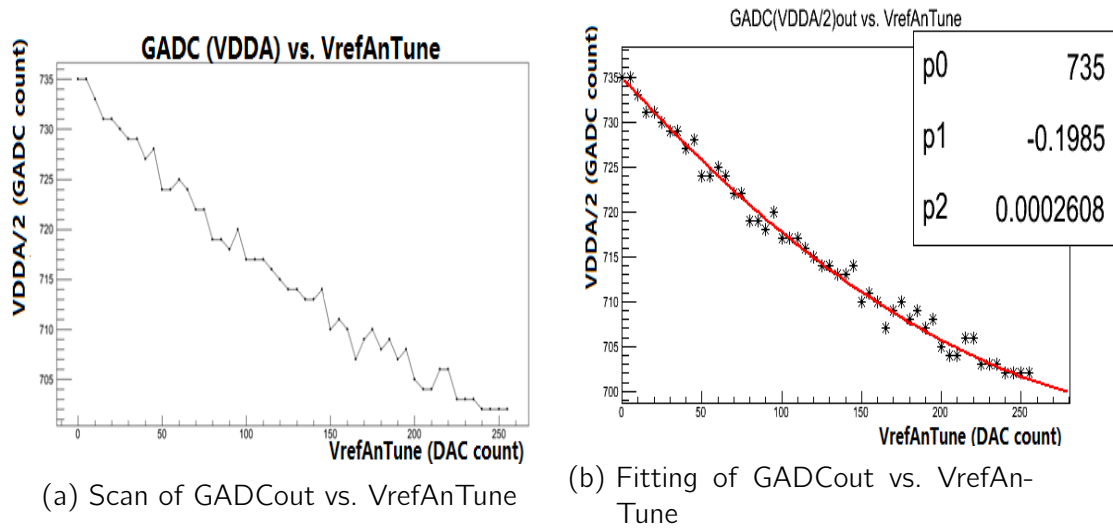


Figure 3.16 – (a) The GADC output of the VDDA/2 as a function of the VrefAnTune DAC value. (b) Fit performed with the robustness value set to 0.75.

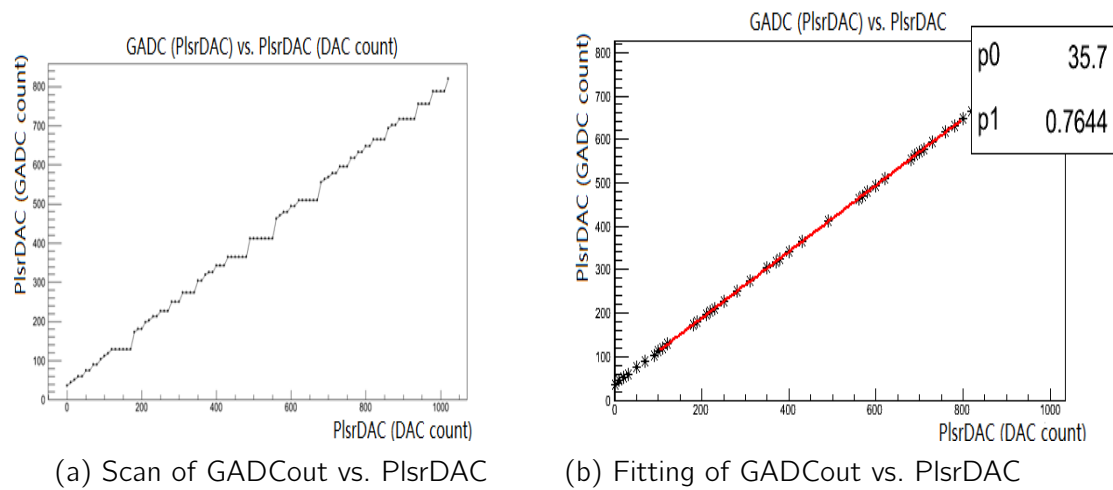


Figure 3.17 – (a) The GADC output of the PlsrDAC as a function of the PlsrDAC DAC value. (b) Fit performed with the stuck data points removed.

respect to temperature for these five samples is plotted in Figure 3.18. The VDDA

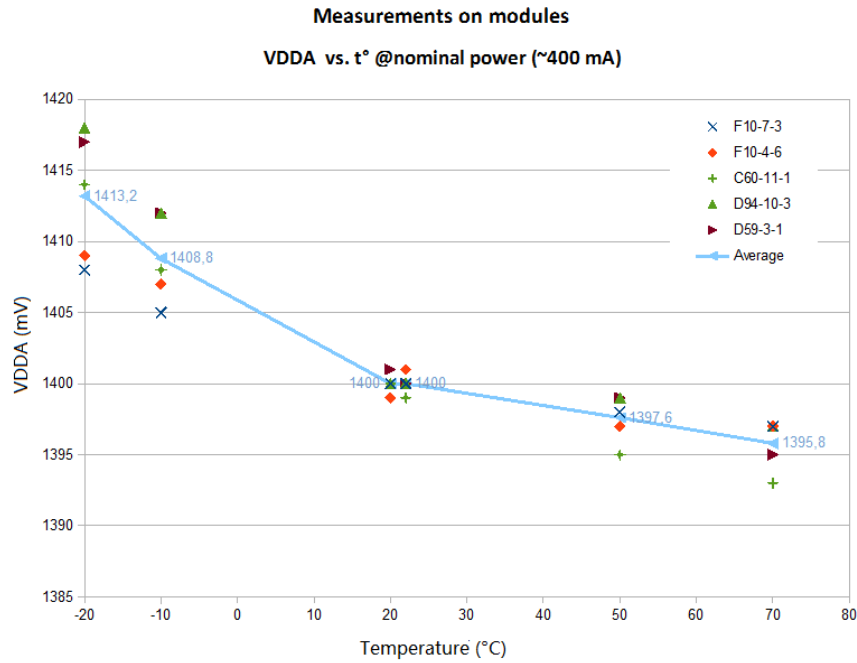


Figure 3.18 – VDDA variation with temperature

voltage of FE-I4 modules can not be measured when they are mounted on the detector, and as seen, the VDDA increases with reduced temperature. Therefore the voltage variation of VDDA with temperature must be considered. For the FE-I4 chips tested, the variations of the VDDA for temperature is very similar, so a correction factor function of temperature can be introduced to improve the calibration precision.

Actually the VDDA voltage depends not only on the temperature, but also on the power consumption (analog and digital current), as shown in Figure 3.19. At the nominal power consumption, the VDDA voltage is tuned to 1.4 V. Then few relevant register values are changed to decrease the power consumption. The VDDA voltage increases with decreasing power at first, peaking at 230 mA of total current, then decreases with the reducing power consumption. Like the temperature dependence, the variation behavior of each individual chip is also quite similar, therefore a correction factor depending on power consumption can be introduced to improve the calibration precision.

To verify the above mentioned calibration algorithm, few modules were calibrated in different temperature and power consumption conditions. Figure 3.20a shows the calibration results with different temperatures. The VDDA voltage measured by a multimeter is drawn in blue color. The GADC out calculated with the first basic calibration algorithm, using a fixed value of $VDDA = 1.4$

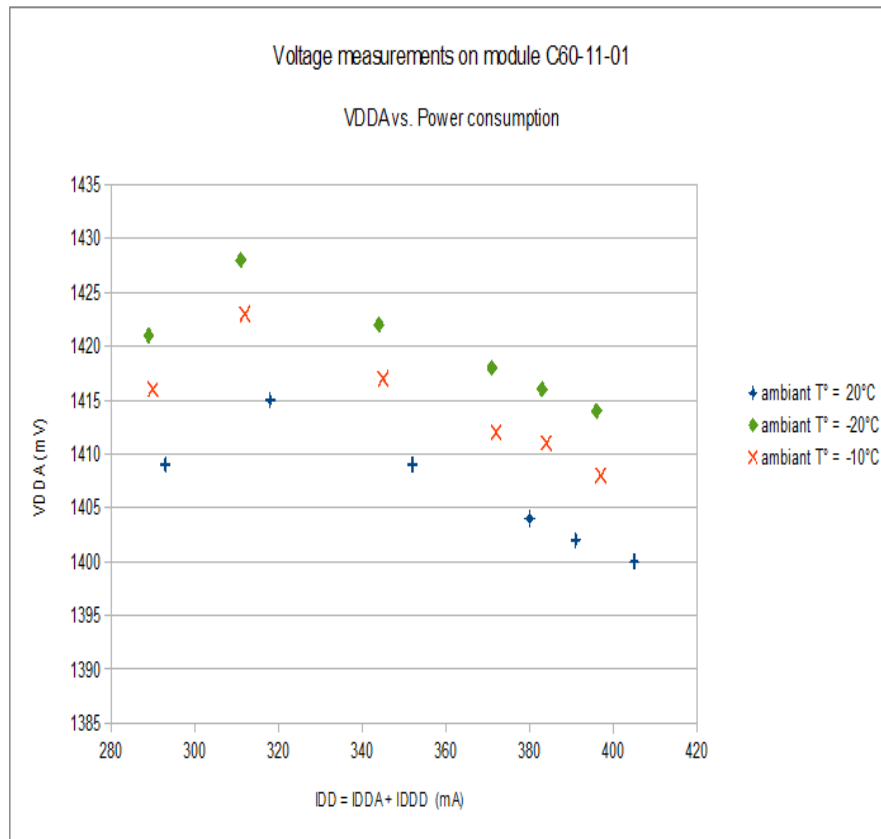


Figure 3.19 – VDDA variation with power consumption

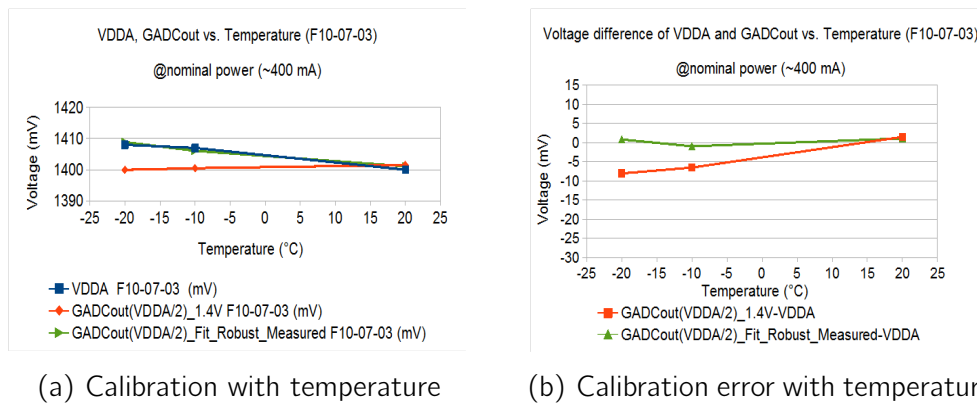


Figure 3.20 – Calibration results depending on temperature. (a) Measured VDDA and the VDDA values calculated by the calibrated GADC. (b) The errors between measurements and calibrated readout.

V, is drawn in red color. The results using this basic algorithm has large deviations compared with measured VDDA voltages. The green curve is the results obtained using the robust calibration algorithm, which means : using measured VDDA instead of 1.4 V, "robust" fitting of GADC out vs. VrefAnTune scan and stuck points removed of GADC out vs. PlsrDAC scan. After the calibration with this new algorithm, the error between the GADC output and the measured VDDA voltage is less than $\pm 0.8\%$ in the temperature range $-20\text{ }^{\circ}\text{C}$ to $20\text{ }^{\circ}\text{C}$. The errors are shown in Figure 3.20b.

The power consumption dependence is also explored with the same methodology. The calibration results are shown in Figure 3.21a, and the error is shown in Figure 3.21b. The error is less than $\pm 1.3\%$ in the current consumption range 293 mA to 409 mA.

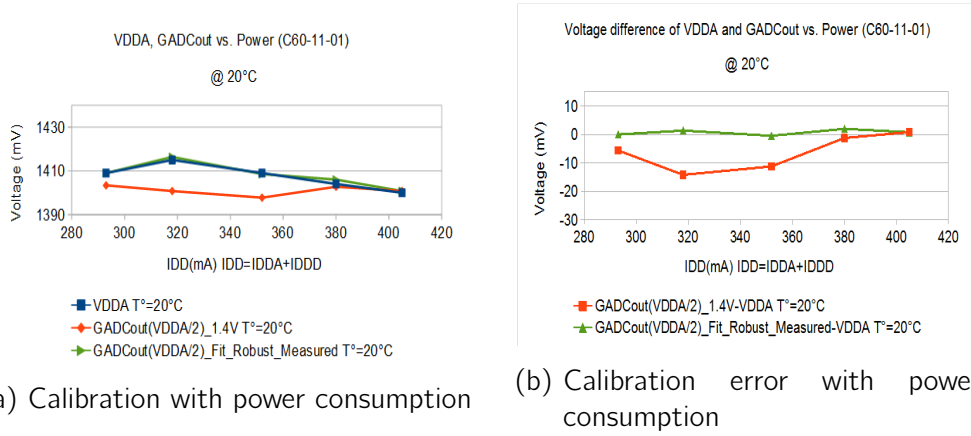


Figure 3.21 – Calibration results depending on power consumption. (a) Measured VDDA and the VDDA values calculated by the calibrated GADC. (b) The errors between measurements and calibrated readout.

The more sophisticated calibration algorithm is hence validated by the VDDA measurements. All the IBL modules were tested and the corresponding scans for the GADC calibration were recorded in the database. Two types of data can be used for the calibration. One is the so called ASSY data, which is the test results at $10\text{ }^{\circ}\text{C}$. The other one is the so called FLEX data, which is tested from $-5\text{ }^{\circ}\text{C}$ to $-10\text{ }^{\circ}\text{C}$. The LSB and offset distribution of all ASSY data are shown in Figure 3.22. The mean LSB of ASSY data is 0.9809 mV with 0.078 RMS.

Figure 3.23 shows the LSB and offset of FLEX data. The mean LSB of ASSY data is 0.9697 mV with 0.069 RMS. A lookup table (LUT) was created for all IBL modules, which contains the module ID, the LSB and the offset for the GADC. This LUT is integrated into the IBL software framework.

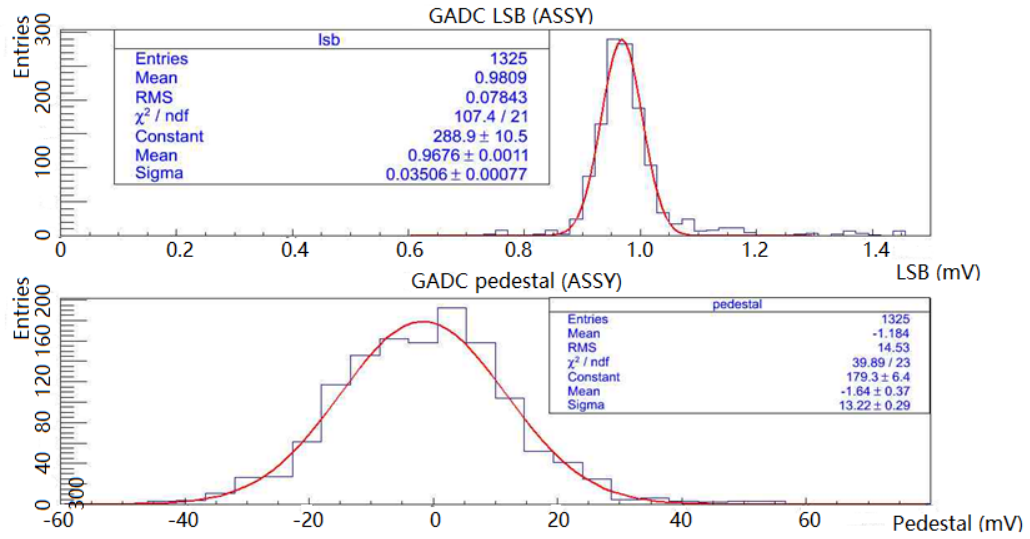


Figure 3.22 – LSB and pedestal distribution of ASSY data

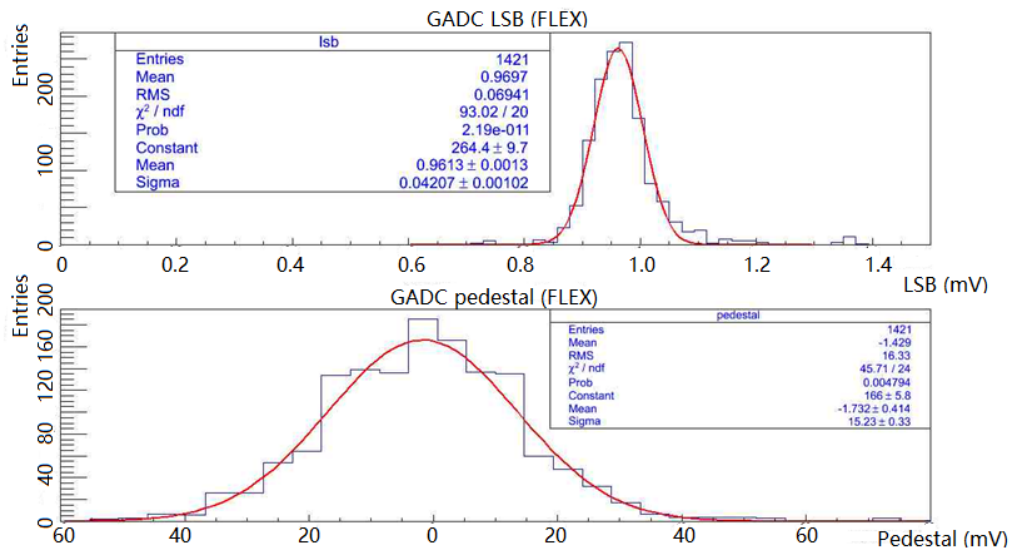


Figure 3.23 – LSB and pedestal distribution of FLEX data

3.3 HV/HR CMOS sensor

As discussed in Section 1.3, the HV/HR CMOS sensors would be a potential solution for the ATLAS ITk. The HV/HR CMOS sensor concepts and the HV2FEI4 assembly will be introduced in this section.

3.3.1 Smart diode array

A sensor which is developed based on a triple-well structure is discussed here as an example. It is to be noted that following in this section is a description of the electronics for the LFoundry prototype which we will encounter again in Section 5.2.3. The triple-well process allows to implement the full CMOS electronics, while isolating the sensitive electronics from the high voltage charge collection part. The charge collection diode is formed by a lightly doped DNW (Deep N-Well) and the substrate. The depletion width is proportional to the square root of the voltage difference of the pn-junction and the substrate resistivity. Therefore

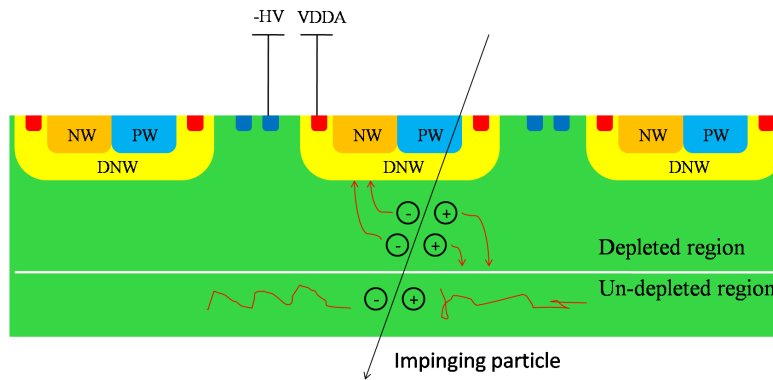


Figure 3.24 – HV CMOS sensor diagram. A relative large depleted region can be obtained due to the high voltage difference between the DNW and the substrate, and due to the usage of a high resistivity. This results in a high charge collection efficiency despite the high radiation levels.

one can gain a relatively large depleted area by applying a high voltage and/or using a high resistivity substrate. In the case of the HV/HR CMOS sensor, the DNW is typically connected to VDDA (power supply for analog electronics) and the p-type substrate is biased with high voltage. The electron-hole pairs generated by ionization caused by charged particles passing through the depleted region are separated and quickly collected by drift towards the electrodes due to the electric field in the space charge regions. The fast charge collection time reduces the charge loss particularly after irradiation with respect to the traditional Monolithic Active Pixel Sensors (MAPS) in which the charge is mainly collected by diffusion. The breakdown voltage is strongly technology dependent

and also influenced by the pn-junction geometry. For the HV/HR CMOS sensor, depending on the different processes and wafer resistivities, a depletion depth range from $10\ \mu\text{m}$ to $120\ \mu\text{m}$ can be obtained, which corresponds to a collected charge range from around 800 to around 9600 electrons for a Minimum Ionizing Particle (MIP). A sketch of an HV/HR CMOS sensor is shown in Figure 3.24.

The readout electronics is placed inside the DNW. A simplified schematic of the electronics is shown in Figure 3.25. The sensor signal is amplified by a charge

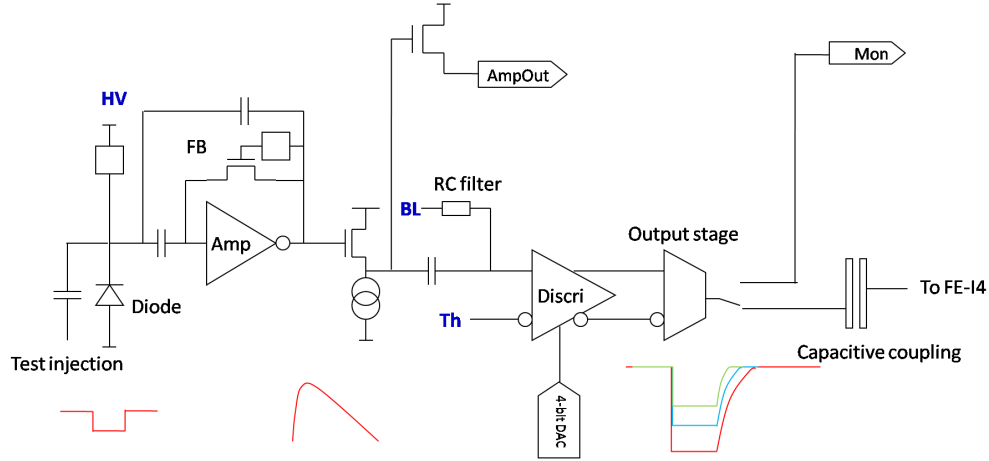


Figure 3.25 – Simplified electronics schematic. A typical HV-CMOS electronics chain for one pixel consists of a charge sensitive preamplifier, a source follower, an RC filter, a discriminator and a weighted output stage.

sensitive amplifier, which converts the current pulse to a voltage signal via an integral feedback circuit. The output of the amplifier is brought to a discriminator via a source follower and compared with an external controlled threshold. A four bit threshold tuning DAC (Digital-to-Analog Converter) is designed in order to provide fine adjustment of the threshold in each pixel. The output of the discriminator is connected to an output stage, which can generate weighted output voltages for sub-pixel encoding.

The substrate is biased with a high resistance element which is typically realized by using a PMOS transistor working in diode mode. The high resistance assures that most of the charges flow to the feedback loop of the preamplifier. The transistor level schematics of the preamplifier and the feedback loop are shown in Figure 3.26 and 3.27. The preamplifier is a single ended folded cascode amplifier. A separated power supply rail, called VDD_{Apre} , is designed for biasing of the preamplifier in order to avoid the noise injection from the VDD_{A} power line to this sensitive element. The preamplifier can be disabled and enabled by an “enable” analog switch, and the biasing current can be adjusted by the voltage of V_N . The preamplifier load and the polarization of the cascode transistor can be set by tuning the voltage of the $V_{N\text{Load}}$ and the V_{casc} .

The DC feedback is implemented with an approximately constant discharge

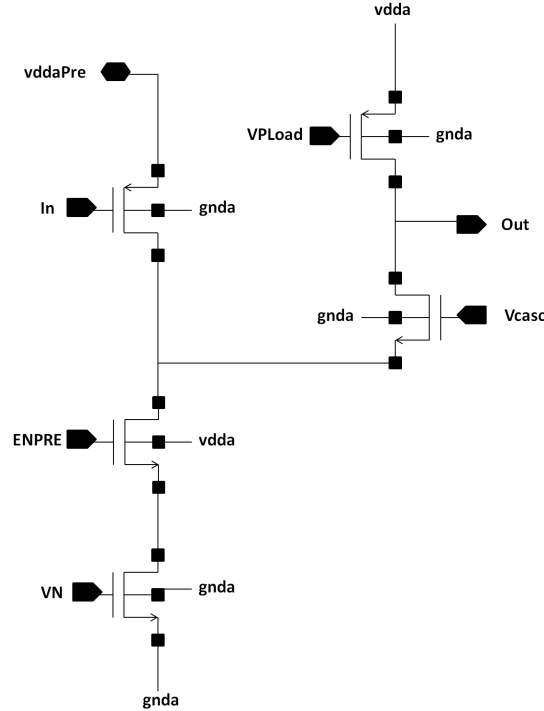


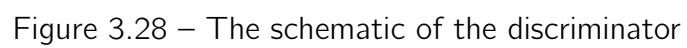
Figure 3.26 – The schematic of the preamplifier

current circuit as shown in Figure 3.27. The feedback loop used for charge integration consists of a resistive element and a capacitor connected in parallel, which converts the inout current pulse to a voltage output. The discharge current can be tuned by changing the voltage of the VPFB.

The output of the preamplifier is followed by a source follower (SF) which is used as a low-pass filter in order to reduce the noise. The signal is then AC coupled to the discriminator. A well defined reference DC point is set for this input signal via the external voltage BL (see Figure 3.25). The discriminator is made of a fully differential operational amplifier. A typically 300 mV higher voltage than VDDA is applied to the load transistors of the differential amplifier in order to compensate the voltage drop (could limit the output dynamic range) due to the diode-connected transistors. The threshold dispersion introduced from the transistor mismatch can be tuned by the 4-bit DAC on the ITUNE node. The output of the discriminator is sent to an output stage which can generate weighted output pulse height for sub-pixel encoding.

3.3.2 HV2FEI4 prototype

To early 2016, several HVCMOS prototype sensors have already been produced in 350 nm and 180 nm HV Austria MicroSystems (AMS) [88], GlobalFoundries (GF) 130 nm BCDlite [89], LF 150 nm [90] and ESPROS 150 nm [91] tech-



nologies, etc... The above mentioned prototypes are compatible with the FE-I4 chip, which is the readout ASIC developed for the ATLAS IBL project described above in this chapter. The sensor can be coupled with FE-I4 capacitively using liquid fluid epoxy glue, as shown in Figure 3.29, and the assembly is then called HV2FEI4. The prototypes have different pixel matrices but have the same individual pixel pitch, $125 \times 33 \mu m^2$.

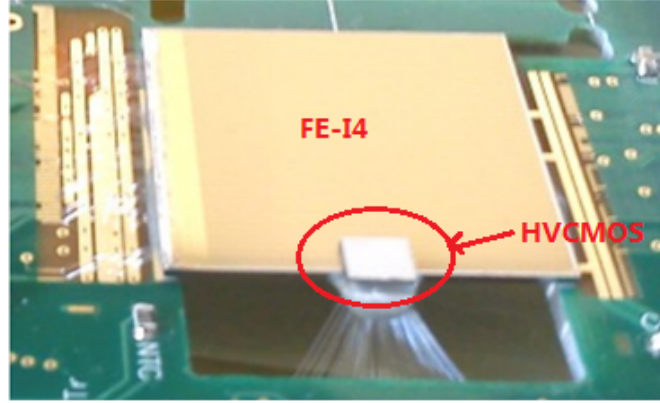


Figure 3.29 – HV2FEI4 test assembly. The AMS 180 nm HV CMOS sensor is glued onto FE-I4 face to face using epoxy glue with below $5 \mu m$ thickness ensuring good AC transmission.

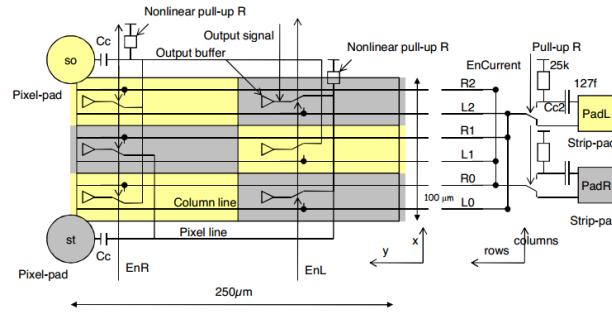


Figure 3.30 – A unit readout cell of the HV2FEI4 test assembly. The sensor configuration. Six sensor pixels with chess box placement are connected to two individual FE-I4 pixels via pixel pads (st and so). The sensor output that is transmitted to FE-I4 is pulled up by a transistor (acting as a nonlinear resistor). The sensor output also can be monitored through a test pad with a $20 \text{ k}\Omega$ pull-up resistor. The pixels can be also connected together column by column to be used as a strip chip with output signals PadL and PadR.

Therefore, to fit to the FE-I4's pixel size $250 \times 50 \mu m^2$, six sensor pixels are matched to two FE-I4 pixels. As shown in Figure 3.30, the six pixels in a unit cell

are connected three by three to two FEI4 pixels in a triangular configuration. The three pixels connected to the same FE-I4 pixel can later be distinguished downstream thanks to the different weighted output amplitudes generated at the output of the HVCMOS electronic chain. Sub-pixel decoding can improve the spatial resolution compared to using solely the standard FE-I4 pitch. The sensor output signal is capacitively coupled to the FE-I4, then converted inside the FE-I4 to digital Time-Over-Threshold (TOT) information with a hit time stamp.

Further discussion of the HV/HR CMOS sensor and the HV2FEI4 assembly can be found in Section [5.1](#).

4 TCAD simulation of HV/HR CMOS sensors

Technology Computer Aided Design (TCAD) refers to the use of computer simulations to develop and optimize semiconductor processing technologies and devices [92]. The TCAD simulation software simulates the semiconductor physics processes by solving some specific equations that will be described in Section 4.2. with finite element method. In this chapter, the TCAD software called Sentaurus is used for the simulation of several variations of the HV/HR CMOS in various technologies. The Sentaurus [92] is a suite of TCAD tools which simulates the fabrication, operation and reliability of semiconductor devices. TCAD simulation tools and procedures are briefly introduced in Section 4.1. The necessary physical models as well as the radiation models specific to our applications are discussed in Section 4.2. Simulation results are then given in Section 4.3.

4.1 An introduction to TCAD simulation

The Sentaurus simulators use physical models to represent the wafer fabrication steps and device operation, thereby allowing the exploration and optimi-

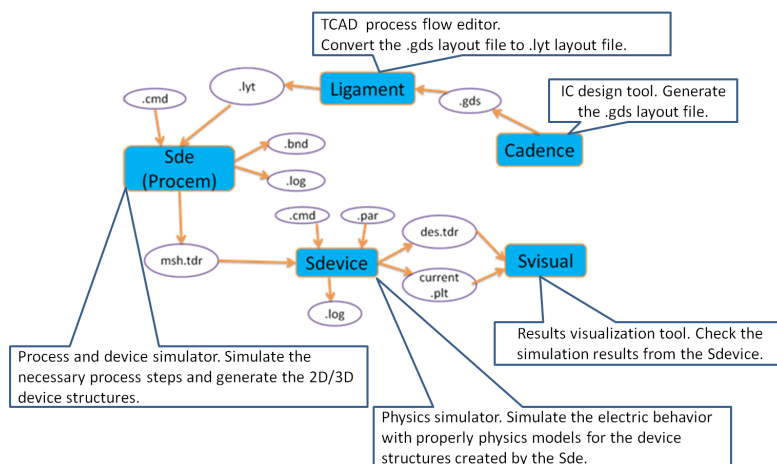


Figure 4.1 – A general TCAD simulation flow

zation of new semiconductor devices [93]. The Sentaurus TCAD tools can be combined into complete simulation flows to simulate in 2-D and 3-D. A very generic simulation flow for HVCMOS sensor simulation is shown in Figure 4.1. A so called .gds layout is drawn in the Cadence IC design tool, then this layout file is converted to a TCAD readable file called .lyt file by the Ligament. A so called .cmd file which declares the process procedures and mesh information together with the .lyt file are read by the Sde. Then, the Sde generates the .bnd file that has the device geometry parameters, the log file that includes the common software running information and the msh.tdr file which contains both the geometry, doping and mesh parameters. The msh.tdr file is sent to the Sdevice to make physical simulations. A .cmd is also needed for the Sdevice to define the electrodes, physical models and solving strategies. A so called .par might be need if one need to modify the default physical model parameters in Sdevice. Normally the Sdevice generates two kind of results : des.tdr and current.plt. The des.tdr file saves all the simulation results with spacial information, and the current.plt file saves the current and capacitance results. All the above mentioned simulation items can be managed in the Sentaurus Workbench, which will be introduced below.

4.1.1 Sentaurus Workbench

Sentaurus Workbench [94] is a framework that is a graphic user interface (GUI) designed for simplifying the usage of the various tools. One of the main

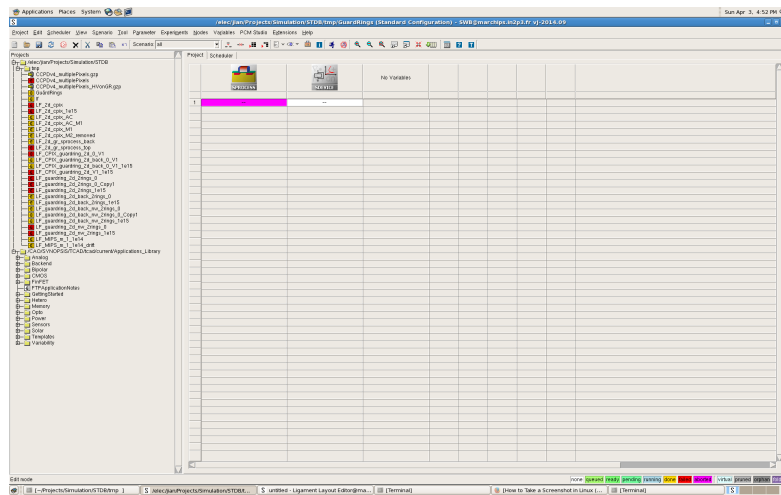


Figure 4.2 – Main panel of Sentaurus Workbench

advantages over a traditional simulation session is the possibility of parameterizing input files to run simulation groups automatically, as shown in Figure 4.2. This function of Workbench is useful for a multi-project platform manipulation. Much effort has been devoted on investigation and development of HV CMOS

sensors with different technologies and geometries. In order to shorten the simulation time for different prototypes, a multi-project platform development is inevitable.

4.1.2 The Sentaurus Ligament and the Sentaurus Process

Sentaurus Process is a complete and highly flexible, multidimensional, process modeling environment [93]. The input files for process simulations can be written entirely by the user or generated using the tool of Ligament. Ligament is a package which provides a convenient interface for process simulation, which is independent of the particular process simulator and simulation dimension. The Ligament operation flow is shown in Figure 4.3.

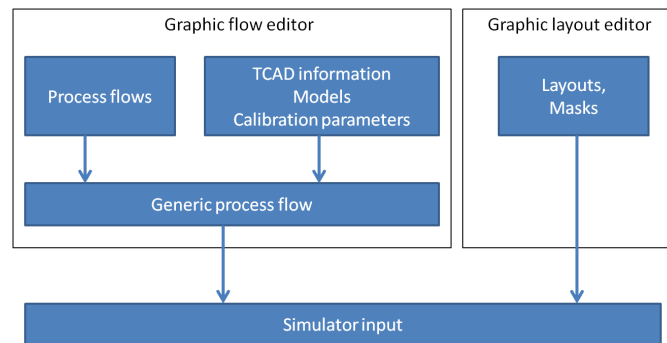


Figure 4.3 – Sentaurus Ligament overview

The Ligament Flow Editor is the graphical representation of a Ligament file. It is a GUI that can visualize and manage the corresponding process simulation commands. The Ligament Layout Editor can manage multiple types of file, for example, layout files and command files. The Ligament Layout supports the CIF and GDSII file formats. The best way to manage the masks we needed is to draw the layout in an IC design tool such as Cadence IC and then to export the GDS file into the Ligament Layout Editor. As for IC layout, Cadence was found easier to handle than Sentaurus. Figure 4.4 shows the main window of the Ligament Layout Editor. The simulation region can be defined and the layers needed can be activated, and saved as ISE-DF format file for simulation.

4.1.3 Sentaurus structure editor

In the Sentaurus Structure Editor (Sde) [95], structures are generated or edited interactively using a GUI. Doping profiles and meshing strategies can also be defined interactively. A 3D structure created in the Sde is shown in Figure 4.5. Alternatively, the Sde can also work in a batch mode. In batch mode, one can create a device using scripts. This option is useful for creating parameterized

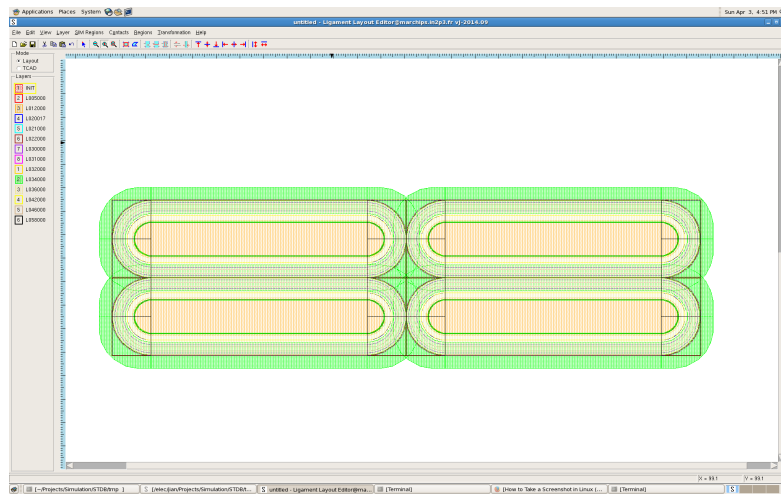


Figure 4.4 – Main windows of Ligament Layout

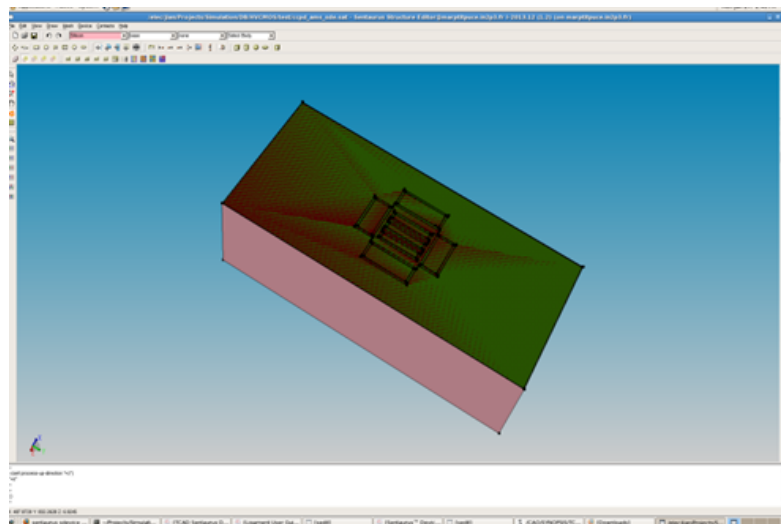


Figure 4.5 – A 3D structure in the Sde

device structures particularly the complex and large 3D devices. The Sde can run in a process emulation mode, and the module is called process emulation (Procem). The process steps such as etching, diffusion and implantation can be simulated in the Procem.

4.1.4 Sentaurus mesh generation tools

Mesh Generation Tools is a suite of tools that produce finite-element meshes for use in applications such as semiconductor device simulation, process simulation and electromagnetic simulation [96].

The choice of mesh strategies is case dependent. For the devices for which the main surfaces are not straight (e.g. round corners, trapezoid structures, etc...), the Noffset3D mode can offer a better mesh productions. However, for a device that the main surfaces are straight, as the case for the HV/HR CMOS sensors, the usage of the Sentaurus Mesh can obtain easier doping control and minimize the number of mesh cells.

The mesh density should also be optimized in different simulation cases. For example, one should choose a fine mesh size, few tens of nanometers, close to the junction area for the breakdown simulation in order to gain a precise result. For the transient simulations, the region which surrounds the impinging particle track should also be meshed with few hundreds of nanometers to obtain an accurate charge generation.

4.1.5 Sentaurus device

Sentaurus Device is a multidimensional, electro thermal, mixed-mode device and circuit simulator for one-dimensional, two-dimensional, and three-dimensional semiconductor devices [97]. Various physical models and numeric methods can be chosen in the Sentaurus Device. The physical models should be chosen properly and some default parameters, for instance the lifetime of the free carriers in substrate, should also be tuned for a specific simulation in order to obtain precise simulation results and save computing time. The physical models for HV/HR CMOS sensor simulations are briefly described in Section 4.2.

4.1.6 Sentaurus visual

The 1D, 2D or 3D simulation results generated from the Sentaurus Device can be visualized by the Sentaurus Visual tool [98]. It can display the I-V curve, C-V curve, doping profile, electric field distribution, electron and hole densities, etc... An snapshot of a 3D HV/HR CMOS sensor device opened in the Sentaurus Visual is shown in Figure 4.6.

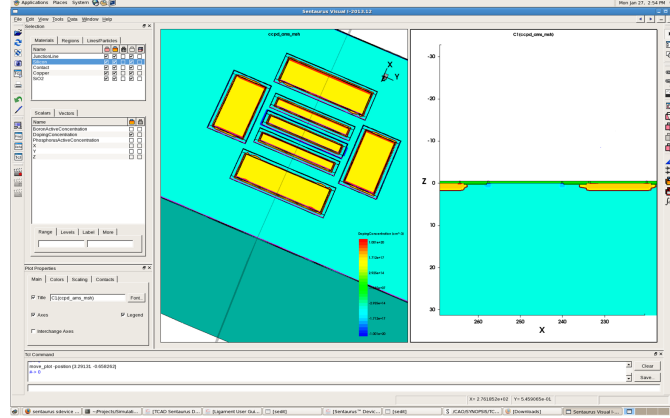


Figure 4.6 – A 3D HV/HR CMOS device as seen in the Sentaurus Visual GUI

4.2 Physical models used for device simulation

In this section, the main physical models, such as the parameterization of electrostatic potential, mobility, carrier transport and particularly the implementation of radiation effect in silicon, which are needed in the sensor simulations are briefly discussed.

4.2.1 Electrostatic potential and quasi-Fermi potential

The mobile charges (holes and electrons) and immobile charges (ionized dopants and traps) in semiconductors determine the electrostatic potential. The electrostatic potential Φ can be found by solving the Poisson equation,

$$\vec{\nabla} \cdot (\epsilon \vec{\nabla} \Phi + \vec{P}) = -q(p - n + N_D - N_A) - \rho_{trap} \quad (4.1)$$

where ϵ is the electrical permittivity, $\vec{P}$ is the ferroelectric polarization, q is the elementary electronic charge, n and p are the electron and hole concentration respectively, N_D and N_A are ionized concentration of donors and acceptors, and ρ_{trap} is the charge concentration introduced by traps and fix charges.

A constant quasi-Fermi potential can describe the electron and hole densities in equilibrium state, when all electrodes of a device are set to the same voltage. The electron and hole concentration can be calculated with Fermi-Dirac statistics :

$$n = N_C \frac{1}{1 + e^{\left(\frac{E_{F,n} - E_C}{kT}\right)}} \quad (4.2)$$

$$p = N_V \frac{1}{1 + e^{\left(\frac{E_V - E_{F,p}}{kT}\right)}} \quad (4.3)$$

where N_C and N_V are the effective density of states, $E_{F,n} = -q\Phi_n$ and $E_{F,p} =$

$-q\Phi_p$ are the quasi-Fermi energies for electrons and holes respectively, and Φ_n and Φ_p are electron and hole quasi-Fermi potential.

In the case when the carrier concentration is smaller than $10 \times 10^{18} \text{ cm}^{-3}$, $E_{F,n} - E_C \gg kT$ and $E_V - E_{F,p} \gg kT$ hold in expressions (4.2) and (4.3). Therefore, the electron and hole concentration can be calculated with the Boltzmann statistics,

$$n = N_C \exp\left(\frac{E_{F,n} - E_C}{kT}\right) \quad (4.4)$$

$$p = N_V \exp\left(\frac{E_V - E_{F,p}}{kT}\right) \quad (4.5)$$

4.2.2 Carrier transport

Several carrier transport models can be chosen for different devices. For the HV/HR CMOS sensors, they can be treated as low-power density with long active region devices. In this case, the carrier transport behavior can be described with the drift-diffusion model. The drift and diffusion current densities have been discussed in Section 2.1.1.3. The carrier transport can hence be simulated by solving the current continuity equations :

$$\vec{J}_n = qn\mu_n\vec{\varepsilon} + \frac{kT}{q}\mu_n\vec{\nabla}n \quad (4.6)$$

$$\vec{J}_p = qp\mu_p\vec{\varepsilon} + \frac{kT}{q}\mu_p\vec{\nabla}p \quad (4.7)$$

where q is electrical charge, T is the temperature, k is the Boltzmann constant, n and p are electron and hole concentrations, μ_n and μ_p are electron and hole mobilities respectively.

4.2.3 Mobility models

The simplest mobility simulation model only considers the phonon scattering. Therefore it only depends on the lattice temperature T :

$$\mu_{const} = \mu_L \left(\frac{T}{300K}\right)^{-\xi} \quad (4.8)$$

where μ_L is the mobility due to the substrate phonon scattering, and ξ is an exponent factor which is different for electron and hole.

Actually for doped materials, the carrier mobility is degraded due to the scattering on the charged impurity ions. Therefore doping-dependent mobility model should be taken into account. Moreover, the high transverse electric field (e.g. the channel region of a MOSFET) near the semiconductor-insulator interface causes an interaction of the carriers with the interface, which results in a carrier

mobility degradation. As discussed in Section 2.1.1.3, the mobility is no longer proportional to the electric field in high electric fields. The high electric field saturation effect should also be considered in the diode simulation.

4.2.4 Generation-recombination

The basic generation-recombination mechanism was described in Section 2.1.1.2. In silicon, an important recombination process is caused by the deep defect levels in the band gap, which is called Shockley-Read-Hall (SRH) recombination as the theory was first derived by Shockly and Read [99] and then by Hall [100]. It can be expressed by :

$$R_{SRH}^{net} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \quad (4.9)$$

with :

$$n_1 = n_{i,eff} \exp\left(\frac{E_{trap}}{kT}\right) \quad (4.10)$$

and :

$$p_1 = n_{i,eff} \exp\left(\frac{-E_{trap}}{kT}\right) \quad (4.11)$$

where E_{trap} is the difference between the defect level and intrinsic level, $n_{i,eff}$ is the effective intrinsic concentration. The lifetime τ_n and τ_p are modeled as functions of doping, electric field and temperature.

As described in Section 2.1.2.2, avalanche breakdown might occur in the high electric field region (space charge region) in a reverse biased diode. The charge multiplication occurs when the high electric field region is larger than the mean free path between two impacts. The electron-hole pair generation through avalanche process (impact ionization) can be expressed as :

$$G_{ii} = \alpha_n n v_n + \alpha_p p v_p \quad (4.12)$$

where α is the reciprocal of the mean free path labeled ionization coefficient. The junction breakdown can be simulated by inspecting the ionization integrals :

$$I_n = \int_0^W \alpha_n(x) e^{-\int_x^W (\alpha_n(x') - \alpha_p(x')) dx'} dx \quad (4.13)$$

and

$$I_p = \int_0^W \alpha_p(x) e^{-\int_0^x (\alpha_p(x') - \alpha_n(x')) dx'} dx \quad (4.14)$$

where W is the depletion width. The integrations are performed along electric field lines through the depletion zone. The avalanche breakdown occurs if the ionization integral equals one.

4.2.5 Traps and fixed charges

The physical processes of both the NIEL and TID effects are discussed in details in Section 2.4. In this section, the parameterized trap models that can be implemented in simulation due to these effect are described.

A number of bulk damage models have been extrapolated from irradiation experiments in recent years [101, 102, 103]. To simulate the displacement defects, few discrete trap levels can be implemented into the forbidden gap. The model I have used for the HV/HR CMOS sensor simulations shown in this Section is summarized in Table 4.1.

Table 4.1 – p-type silicon NIEL induced trap model [104]

Type	Energy(eV)	$\sigma_e(\text{cm}^2)$	$\sigma_h(\text{cm}^2)$	$\eta(\text{cm}^{-1})$
Acceptor	Ec -0.42	9.5×10^{-15}	9.5×10^{-14}	1.613
Acceptor	Ec -0.46	5×10^{-15}	5×10^{-14}	0.9
Donor	Ec +0.36	3.23×10^{-13}	3.23×10^{-14}	0.9

The TID effect simulation procedure is shown in Figure 4.7. The first step is to

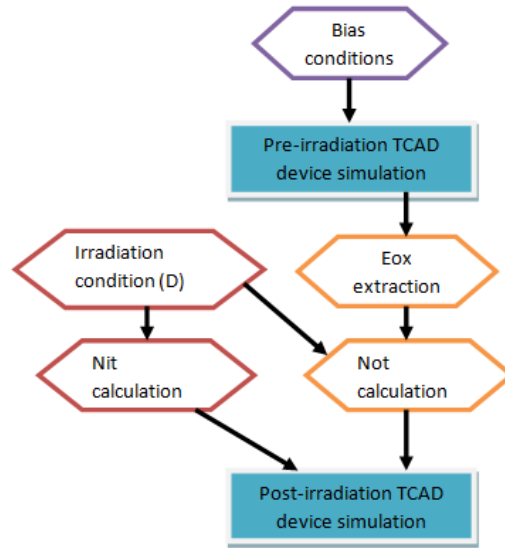


Figure 4.7 – TID simulation procedure

extract the electric field profile of the SiO_2 under a given bias. For the HV/HR CMOS sensor, the Shallow Trench Isolation (STI) region that stands between the DNW and the P-Well should be simulated carefully. Although Sentaurus can give a continuous distribution electric field, it is impossible to implement traps and fixed charges continuously. In order to obtain a precise simulation result, the STI

region needs to be split into several blocks. Constant N_{it} and N_{ot} values are used in each block with respect to their electric field values.

4.2.6 Radiation models

To obtain the charge collection efficiency, a transient simulation should be performed. A heavy ion model can be used for the simulation of MIPs. A simple

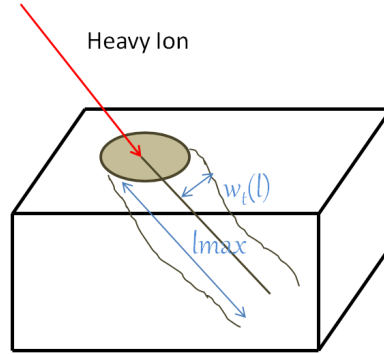


Figure 4.8 – Heavy ion impinging process

heavy ion impinging process is for example shown in Figure 4.8. The charge generation rate caused by the heavy ion is computed by :

$$G(l, w, t) = G_{LET}(l)R(w, l)T(t) \quad (4.15)$$

where $R(w, l)$ and $T(t)$ are functions describing the spatial and temporal variations of the generation rate. $R(w, l)$ is defined as $R(w, l) = e^{-\frac{w}{w_t(l)}}$, where w is the radius from the track and w_t is the characteristic distance (can be a function of l) that can be set by user. $G_{LET}(l)$ is the linear energy transfer generation density and its unit is $pairs/cm^3$. The linear energy transfer (LET) generate density $G_{LET}(l)$ is given by :

$$G_{LET}(l) = a_1 + a_2l + a_3e^{a_4l} + k' [c_1(c_2 + c_3l)^{c_4} + LET_f(l)] \quad (4.16)$$

where $a_1, a_2, a_3, a_4, k', c_1, c_2, c_3$ and c_4 are carrier generation coefficients. There are two options for the units of LET_f : $pairs/cm^3$ (default) or $pC/\mu m$. The LET_f , for MIPs, is around $80 \text{ ehps}/\mu m$, which corresponds to $1.28 \times 10^{-5} pC/\mu m$. The carriers generation is only activated within the range of l_{max} .

4.3 HV/HR sensor simulation

In this section, the simulation procedures and results are described in details. These simulations include the leakage current, breakdown voltage, capacitance,

transient behavior and irradiation simulations. The TCAD numerical simulation is quite time and computing resources consuming, in particular for 3D simulations. Nevertheless, in order to obtain more precise simulation results, most of the simulations discussed below are performed using 3D simulations.

4.3.1 Type A technology simulation

The type A technology is a 130 nm BCD (Bipolar-CMOS-LDMOS) process, which allows to have bipolar, CMOS and LDMOS implementation on the same wafer. It is based on a epi-layer, grown upon a low or a high resistivity substrate.

4.3.1.1 The simulated device

Taking into account the simulation time as well as limitation capabilities of the simulation tool, only a 4-pixel array was simulated. The pixel layout is shown in Figure 4.9. It was drawn in Cadence IC 615.

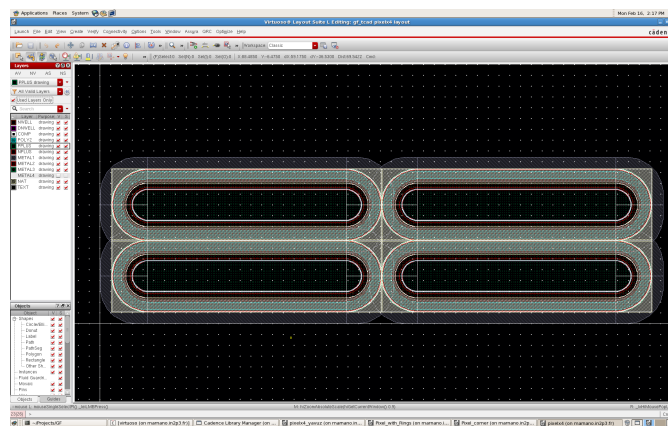


Figure 4.9 – Pixel layout in cadence

The GDS file generated by Cadence can not be read by the Sentaurus tool directly. It needs to be converted to a “.tdr” file in Sentaure Ligament, as shown in Figure 4.10. The necessary layers can be defined and chosen for the device generation.

Two different pixel sizes (different DNW sizes with same pixel pitch), later referred as “standard” and “intermediate” pixel sizes, are simulated in order to investigate the detector capacitance and charge collection mechanism. The 3D devices of standard and intermediate pixels generated by the Sentaurus Procm are shown in Figure 4.11a and 4.11b respectively together with the used mesh.

To simulate the low doping substrate, the resistivity of substrate was defined as $1 \text{ k}\Omega \cdot \text{cm}$.

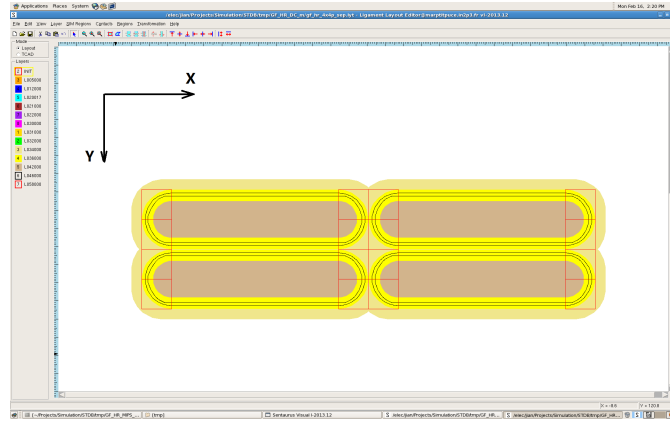
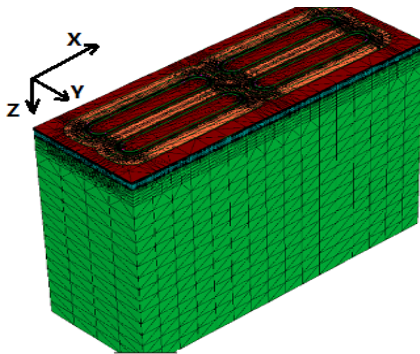
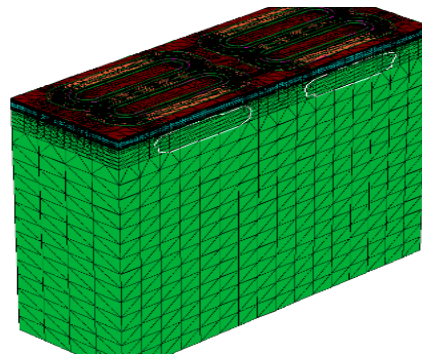


Figure 4.10 – Pixel layout in sentaurus



(a) 3D device of standard size pixel



(b) 3D device of standard size pixel

Figure 4.11 – (a) A 4-pixel array with standard pixel size of $33 \times 125 \mu m^2$. (b) A 4-pixel array with intermediate pixel size of $33 \times 80 \mu m^2$.

4.3.1.2 Depletion zone comparison

Compared with low resistivity substrate, a bigger depleted area can be reached for $1\text{ k}\Omega \cdot \text{cm}$. It is obvious that the depleted region using this rather high resistivity substrate will be larger than few more heavily doped substrate. Below a comparison of the depleted zone formed for the stand size pixel and intermediate size pixel is given.

Standard size pixel

The cut planes of the depleted region at a high voltage (HV) value if -30 V along the X and the Y axis are shown in Figure 4.12a and 4.12b. The edge of

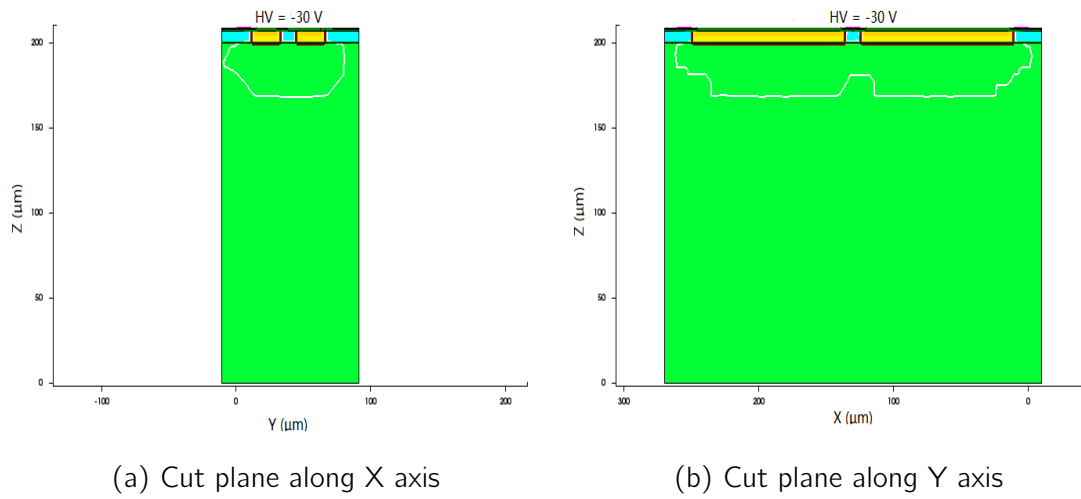


Figure 4.12 – Depletion of the standard pixel size. The depleted region generated in the high resistivity substrate instead of in the epi-layer due to relatively heavier doping. Smaller depleted depth observed in the region between DNWs.

depleted region is highlighted with a white curve. The DNW gaps are $13\mu\text{m}$ and $13\mu\text{m} - 33\mu\text{m}$ (round corner as shown in Figure 4.10) along X-axis and Y-axis. A weaker depleted area is found between two pixels as shown in Figure 4.12b due to a larger DNW gap along the X-axis. The depleted depth as a function of the substrate biasing voltage is shown Figure 4.13. A depletion depth of $45\mu\text{m}$ can be obtained when the HV is -30 V.

Intermediate size pixel

The cut planes of the depleted region for the intermediate size pixel in the same simulation conditions as in the standard size pixel case are shown in Figure 4.14a and 4.14b. The DNW gap along the Y-axis has the same value as in the standard size pixel. The DNW gap along the X-axis is extended from $13\mu\text{m}$ to

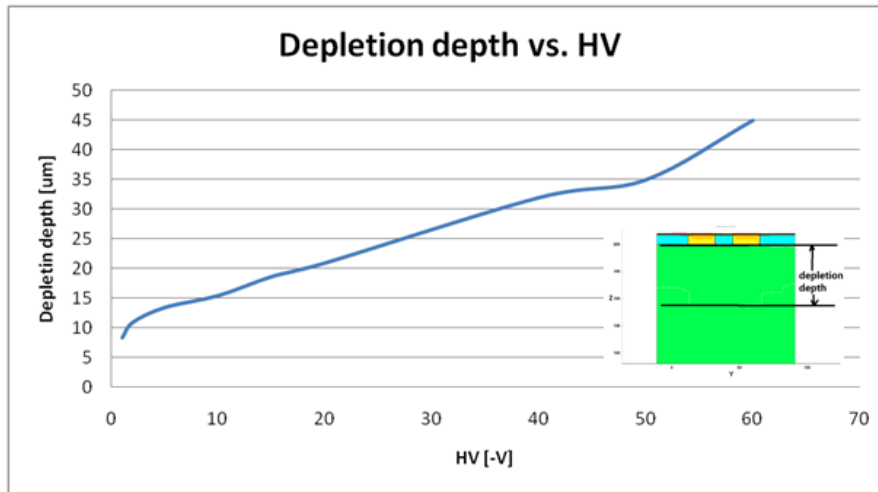


Figure 4.13 – Depleted depth vs. HV

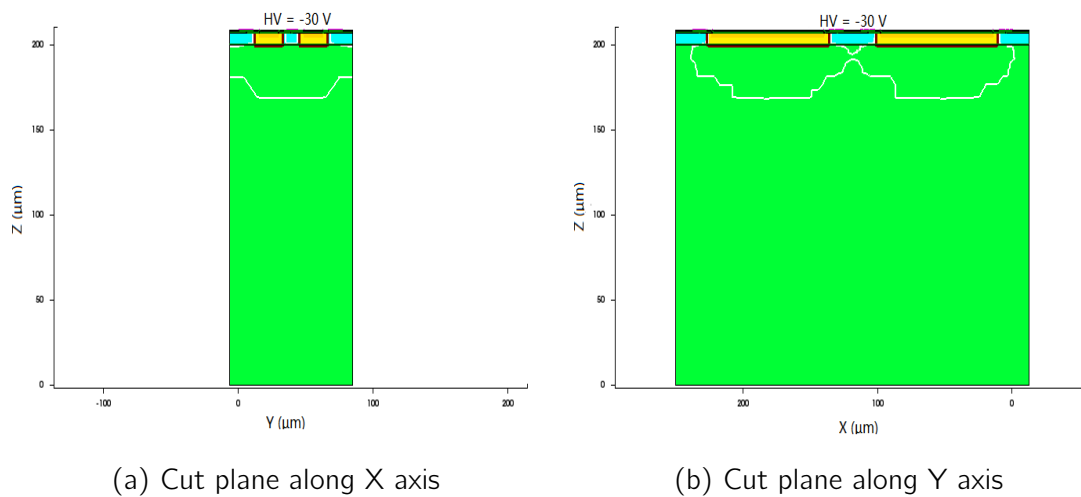


Figure 4.14 – Depletion of the intermediate pixel size. Much smaller depleted depth observed in the region between DNWs due to the extended DNW gap with respect to the standard pixel size.

33 μm . Most of the region beneath the DNW gap along the X-axis is un-depleted due to bigger DNW gap compared with the standard size pixel.

4.3.1.3 Comparison of leakage current and capacitance for standard and intermediate size pixel

The leakage current of the standard size pixel as a function of the HV bias is shown in Figure 4.15a. The leakage current increases with increasing high voltage, and is $\sim 9.1 pA$ when the HV is -30V. The simulation shows that the sensor would breakdown if the HV is lower than -70 V. The DNW capacitance variation

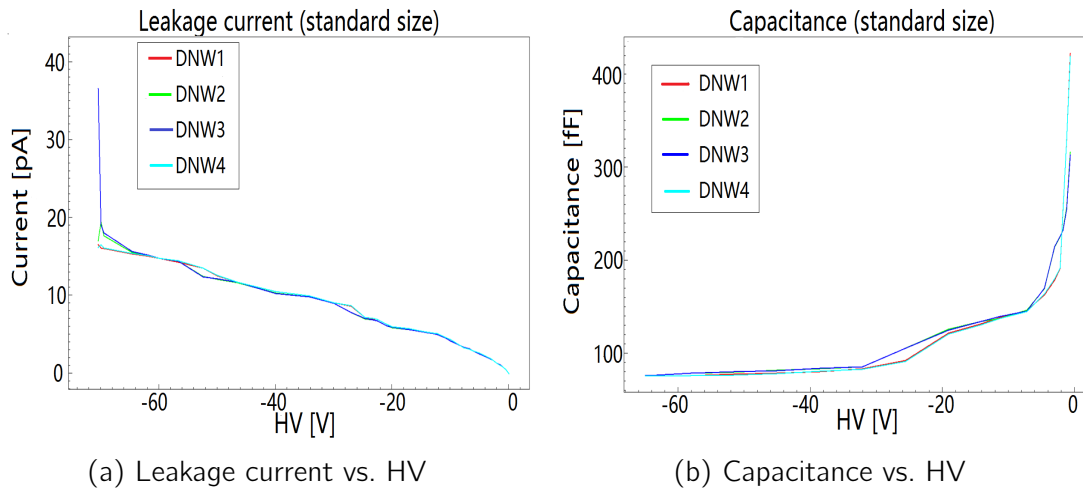


Figure 4.15 – (a) Leakage current of four standard size pixels as a function of HV. (b) Capacitance of four standard size pixels as a function of HV.

with HV of standard size pixel is shown in Figure 4.15b. The capacitance reduces when the absolute value of the HV is increased, and is $\sim 85 fF$ when the HV is -30 V.

The leakage current and capacitance comparison between standard and intermediate size pixels are shown in Figure 4.16a and 4.16b. For the same benchmark -30 V HV value, the leakage current reduces from $\sim 9.1 pA$ for the standard size pixel to $\sim 7.4 pA$ for the intermediate pixel, and the capacitance reduces from $\sim 85 fF$ to $\sim 72 fF$.

4.3.1.4 Electric field and potential for standard size pixel

The electric field and potential distributions are important to understand the avalanche breakdown and charge collection mechanism. The cut plane of the electric field distribution and corresponding field vector are shown in Figure 4.17a and 4.17b respectively. One can see that a high electric field exists near the lateral junction area in epi-layer. The cut lines of the electric field along Y and

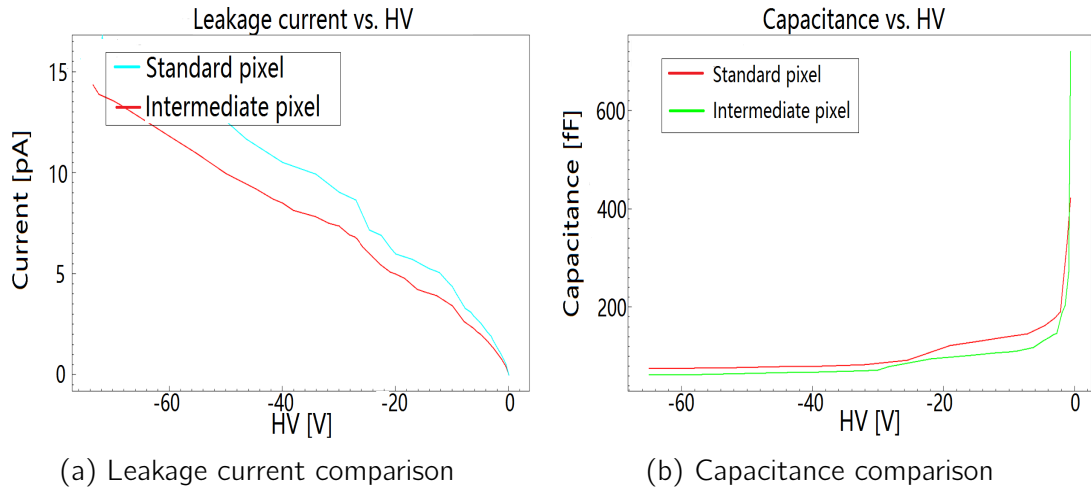
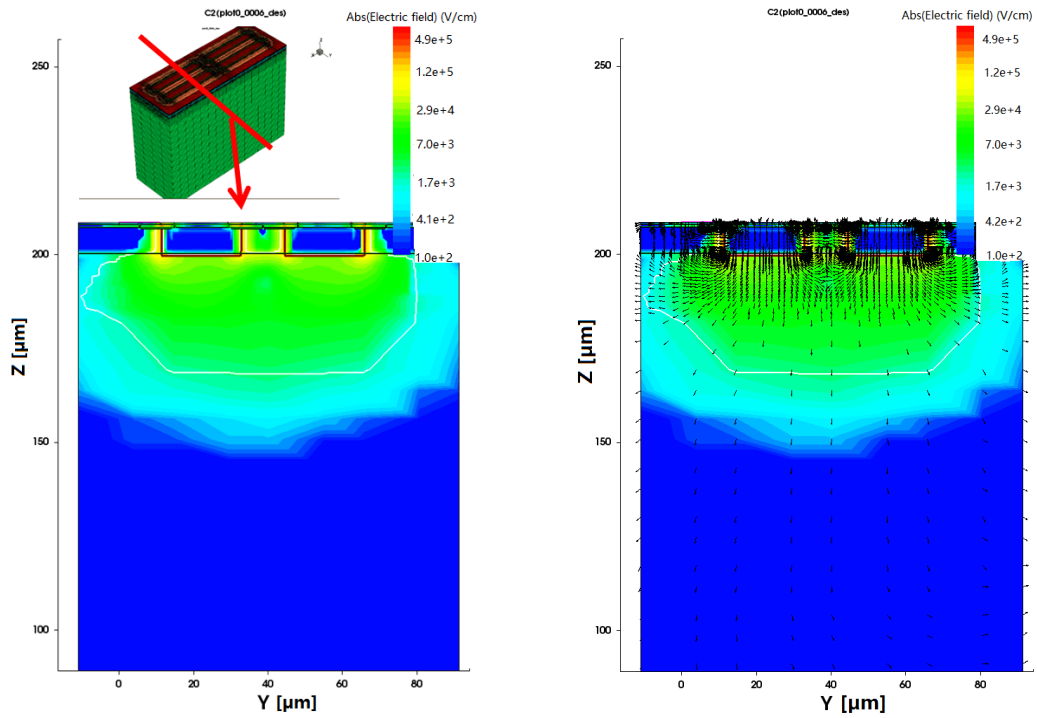


Figure 4.16 – (a) Capacitance comparison between the standard size pixel and the intermediate size pixel. (b) The capacitance comparison between the standard size pixel and intermediate size pixel.



(a) Electric field distribution (HV=-30V) (b) Electric vector (HV=-30V)

Figure 4.17 – The high electric field in the lateral junction area is due to the heavier doping in the epi-layer and dominates the breakdown voltage.

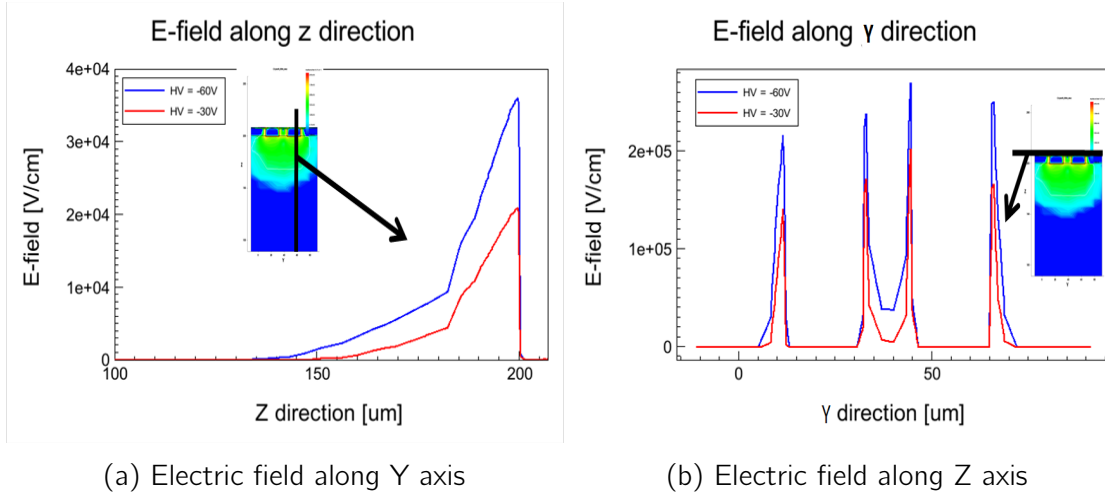


Figure 4.18 – The electric field of the junction between the DNW and epi-layer is much higher than at the junction between the DNW and the substrate.

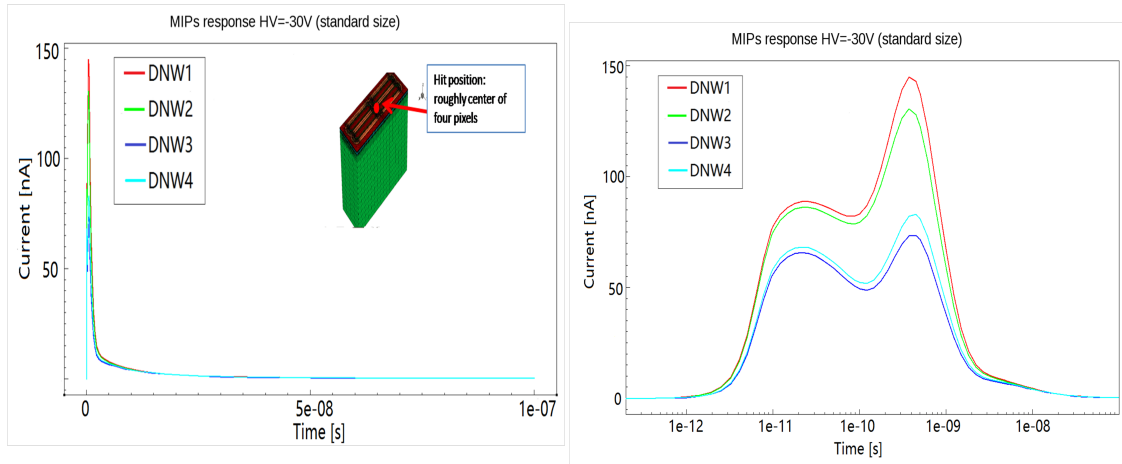
Z directions are shown in Figure 4.18a and 4.18b. The depleted region forms a high electric field so that the generated charges by charged particles can be quickly collected by drift. As shown in Figure 4.18a, the electric field reaches the critical values of approximately $2 \times 10^5 \text{ V/cm}$ near the junction edges when the high voltage is $\sim 60\text{V}$, which will cause the avalanche breakdown. The high doping regions in the epi-layer limit the maximum voltage which can be applied to the substrate.

4.3.1.5 Transient

As discussed in Section 4.2.6, the signal of MIPs can be simulated as a heavy ion particle signal in Sentaurus. In this section, the electron hole pair generation rate is set to $80/\mu\text{m}$. The direction is perpendicular to the device surface. Figure 4.19a and 4.19b show the responses of four pixels in terms of current recorded when the particle hits roughly in the center of the device. As seen in Figure 4.19b, the signals consists of two peak. The first fast peak, recorded within approximately 30 ps, is induced by the charges generated very close to the substrate contacts. The charges drifting from the depleted area form the second main peak, the collection of which comes at approximately 400 ps.

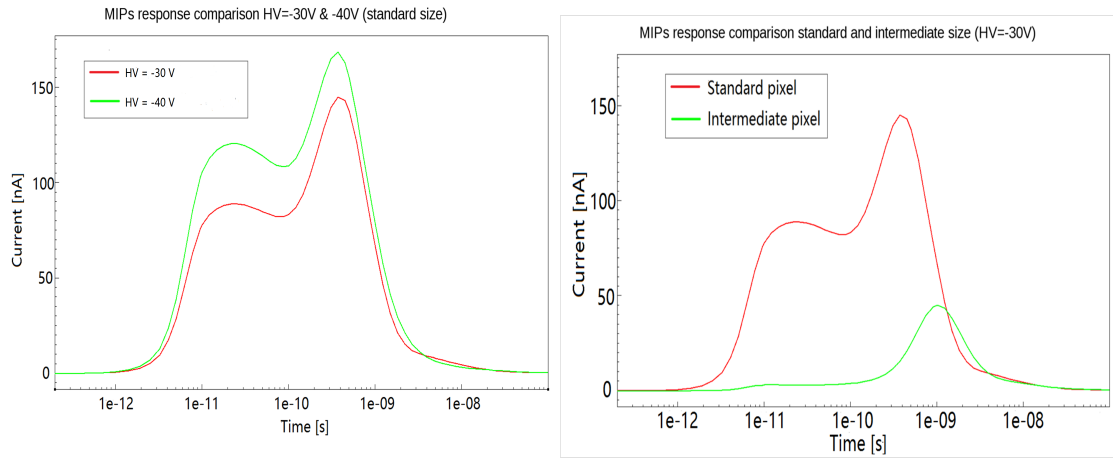
The collected charges improves $\sim 12\%$ when the substrate voltage changes from -30 V to -40 V, as shown in Figure 4.20a. However, the charge collection efficiency of intermediate size pixel reduces by 28% compared with standard size pixel as shown in Figure 4.20b.

If the electric field is close to the critical value, the MIPs induced charges will be accelerated and cause the avalanche breakdown. The breakdown occurs after



(a) MIPs responses of four pixels (linear scale) (b) MIPs responses of four pixels (log scale)

Figure 4.19 – The impinging position is in the middle along the x-axis but shifted by $1 \mu\text{m}$ in the direction towards the two pixels (DNW3 and DNW4).



(a) MIPs responses with different HV values (standard size) (b) MIPs responses comparison (HV= - 30V)

Figure 4.20 – (a) MIPs induced current as a function of time depending on HV values. More charges are collected with increasing HV value. (b) MIPs induced current as a function of time for the standard size pixel and the intermediate pixel. Lower collected charges for the intermediate size pixel due to the smaller depleted area.

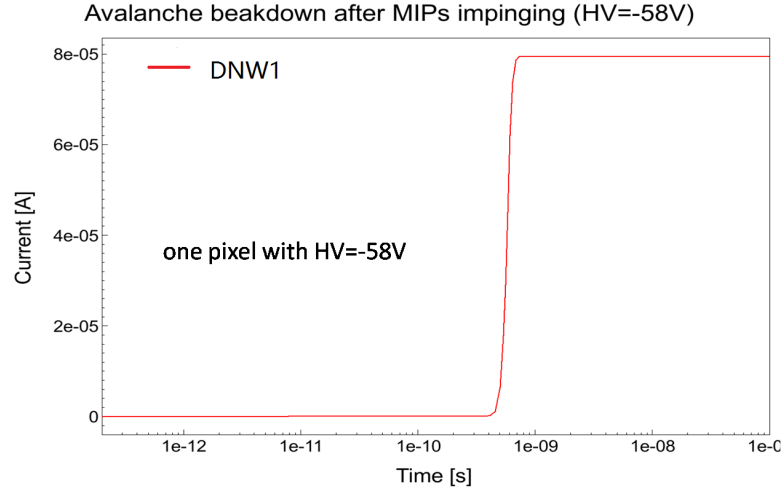


Figure 4.21 – Avalanche breakdown induced by MIPs

few hundred ps as shown in Figure 4.21. If we compare the current density between a HV induced breakdown (Figure 4.22b) and no induced breakdown with lower absolute HV value (Figure 4.22a), one can see that the breakdown initializes from the lateral junction region and forms a current path under the oxides. In order to investigate the charge collection and charge sharing behavior,

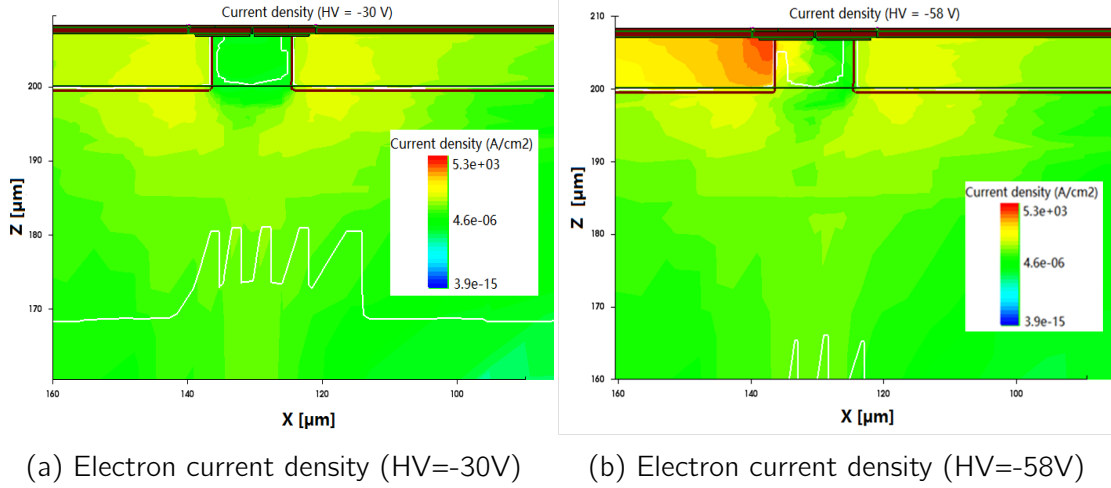


Figure 4.22 – The MIPs induced charges would induce the breakdown close to the junction region when the sensor is biased close to the breakdown voltage.

a quarter of a single pixel region is selected to perform the transient simulations with various particle impinging positions (see Figure 4.23).

Ten different impinging positions are simulated. The positions are detailed in Figure 4.24.

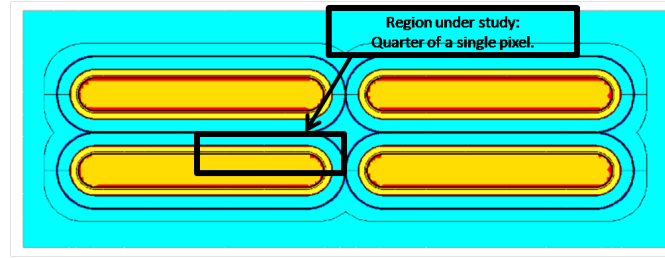


Figure 4.23 – Charge collection simulation region

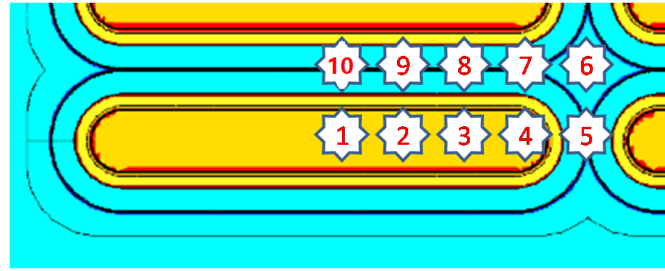


Figure 4.24 – Impinging position in the simulation region

The responses measured via the DNW are shown in Figure 4.25. The charges generated through MIPs that impinge inside DNW are totally collected by one pixel (for instance case of positions 1, 2 and 3). The charges are shared by two to four pixels when the MIPs hit the border regions, such as positions 4 to 10.

The charges collected within 5 ns by the pixel under study with different impinging positions are given in Figure 4.26. Around 4400 collected electrons can be expected for this technology when the substrate voltage is -30 V (a typical bias voltage value before irradiation). From a half to three quarter of the charges will be shared with adjacent pixels where the impinging position is on the side of the DNW.

The induced current as a function of time and the corresponding integrated charges are shown in Figures 4.27 and 4.28 respectively. Most of the charges can be collected within 5 ns and 90% charges can be collected within approximately 25 ns. The charges collected after 5 ns come mainly from diffusion instead of drift.

The electron and hole current density variations for a particle hitting the sensor in position 1 are shown in Figure 4.29 and 4.30 as a function of time. The electrons drift towards the DNW and are collected. The holes are pushed out of the depleted region towards the bottom side.

The electron and hole current density variations for a particle hitting the sensor in position 10 are shown in Figures 4.31 and 4.32. One can see that the charges are shared by the two adjacent pixels obviously.

To understand the contribution of the charges coming from drift and from diffusion respectively, charge generation is only activated in the depleted and in

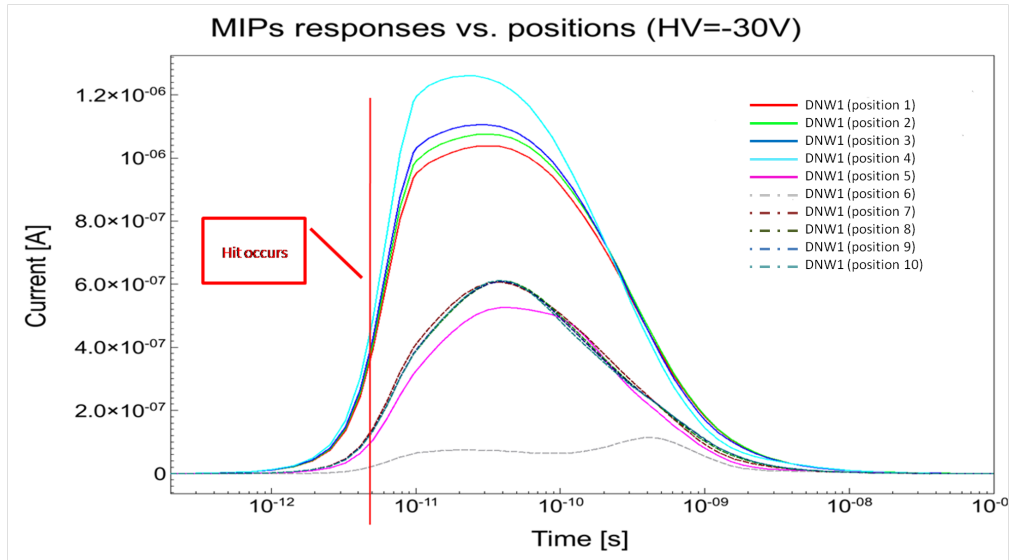


Figure 4.25 – MIPs responses with different impinging position in log scale (HV=-30V)

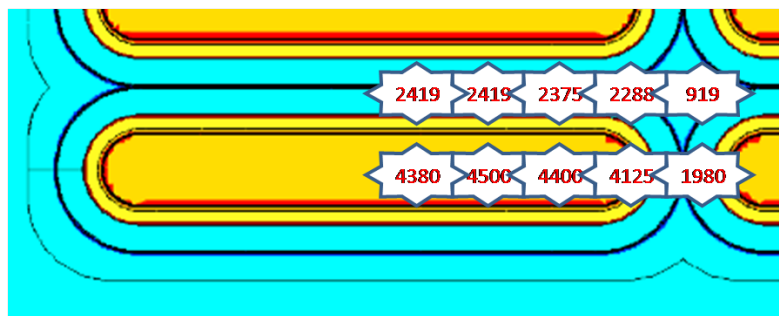


Figure 4.26 – Collected charge within 5ns

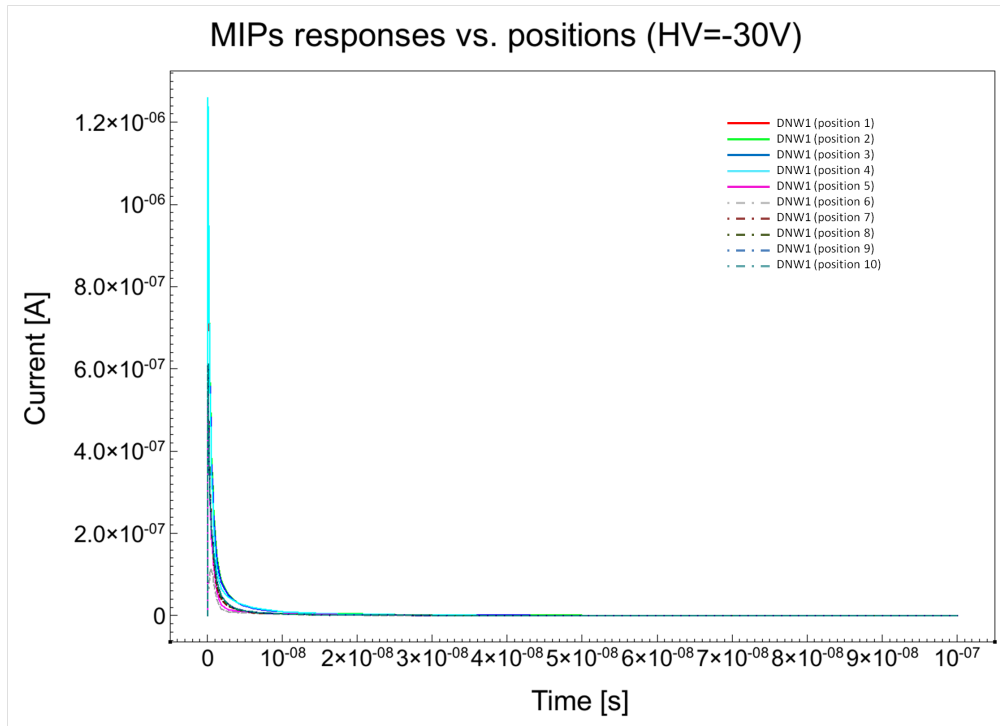


Figure 4.27 – MIPs responses with different impinging position with linear scale (HV=-30V)

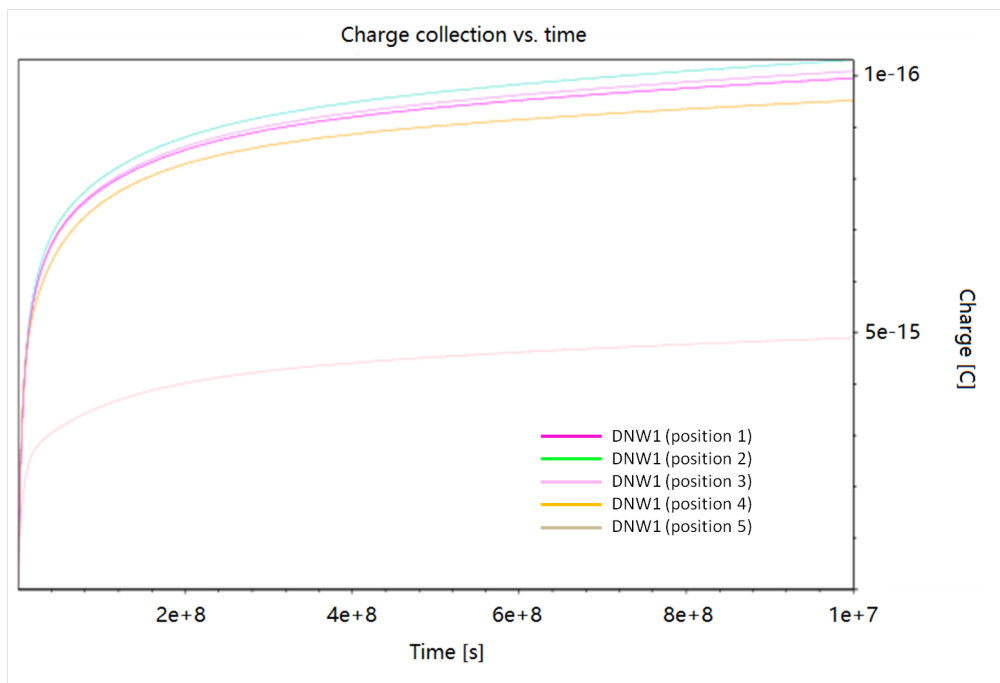


Figure 4.28 – Integrated collected charges (HV = -30V)

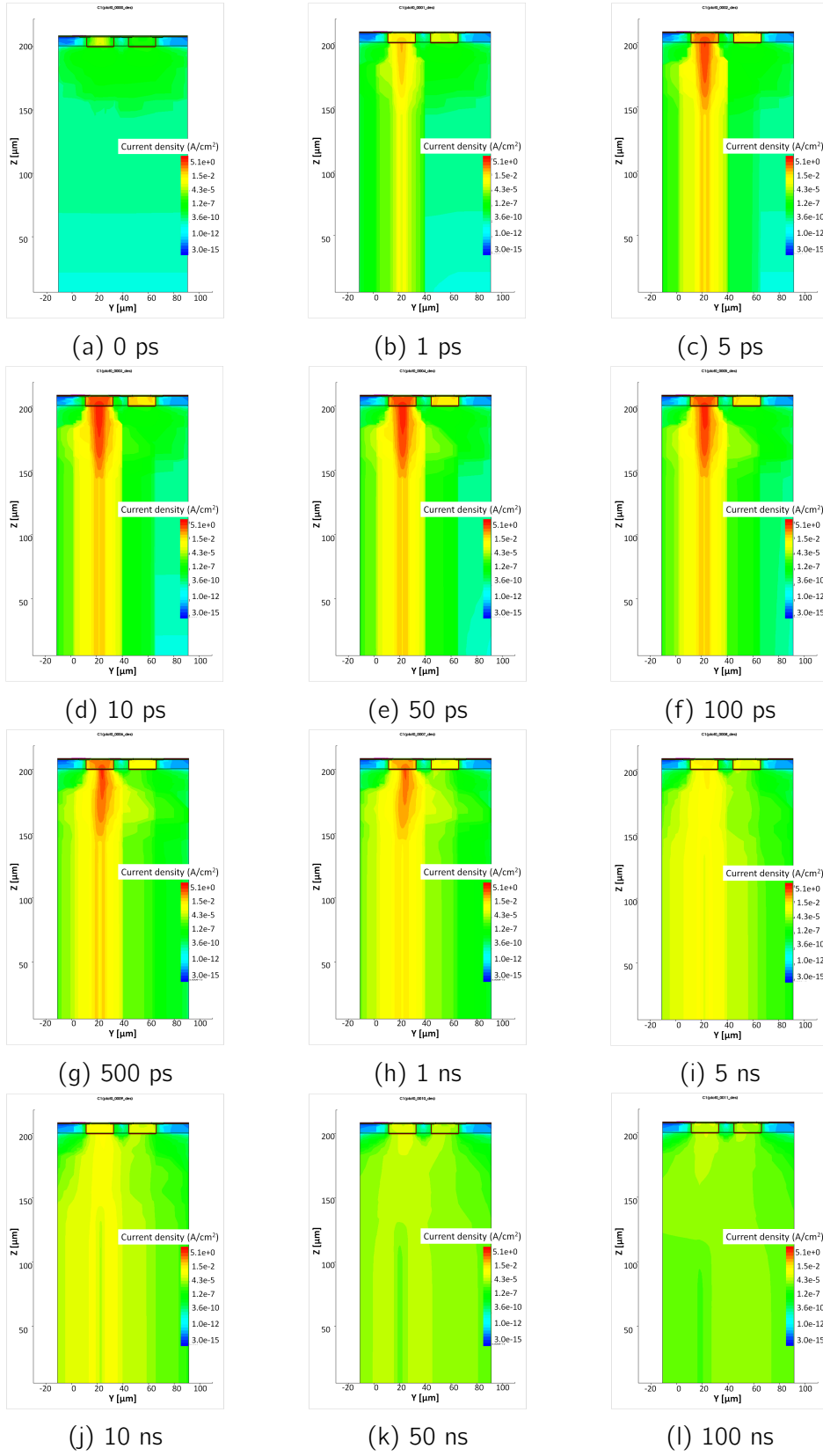


Figure 4.29 – Electron current density variation in position 1

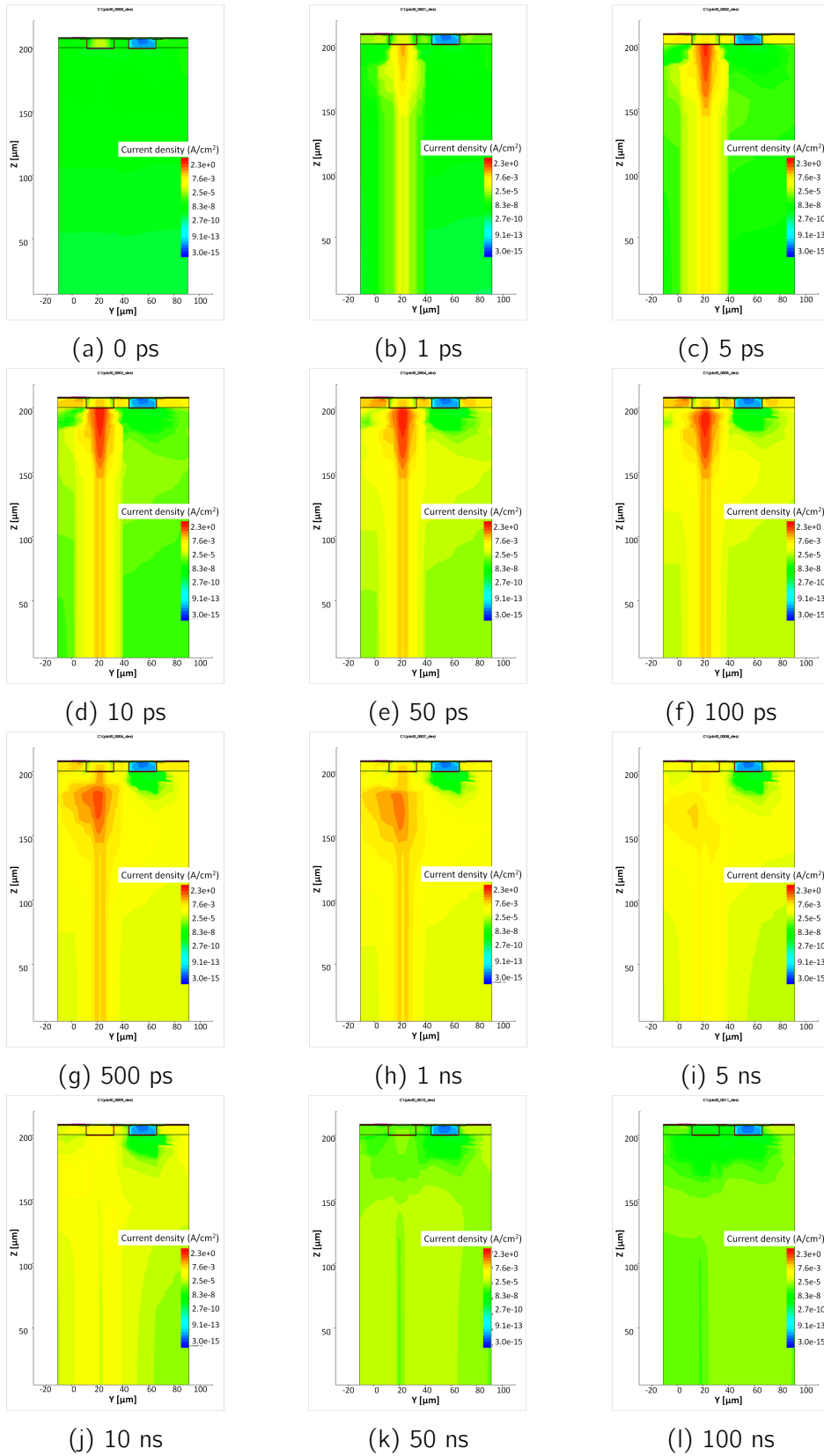


Figure 4.30 – Hole current density variation in position 1

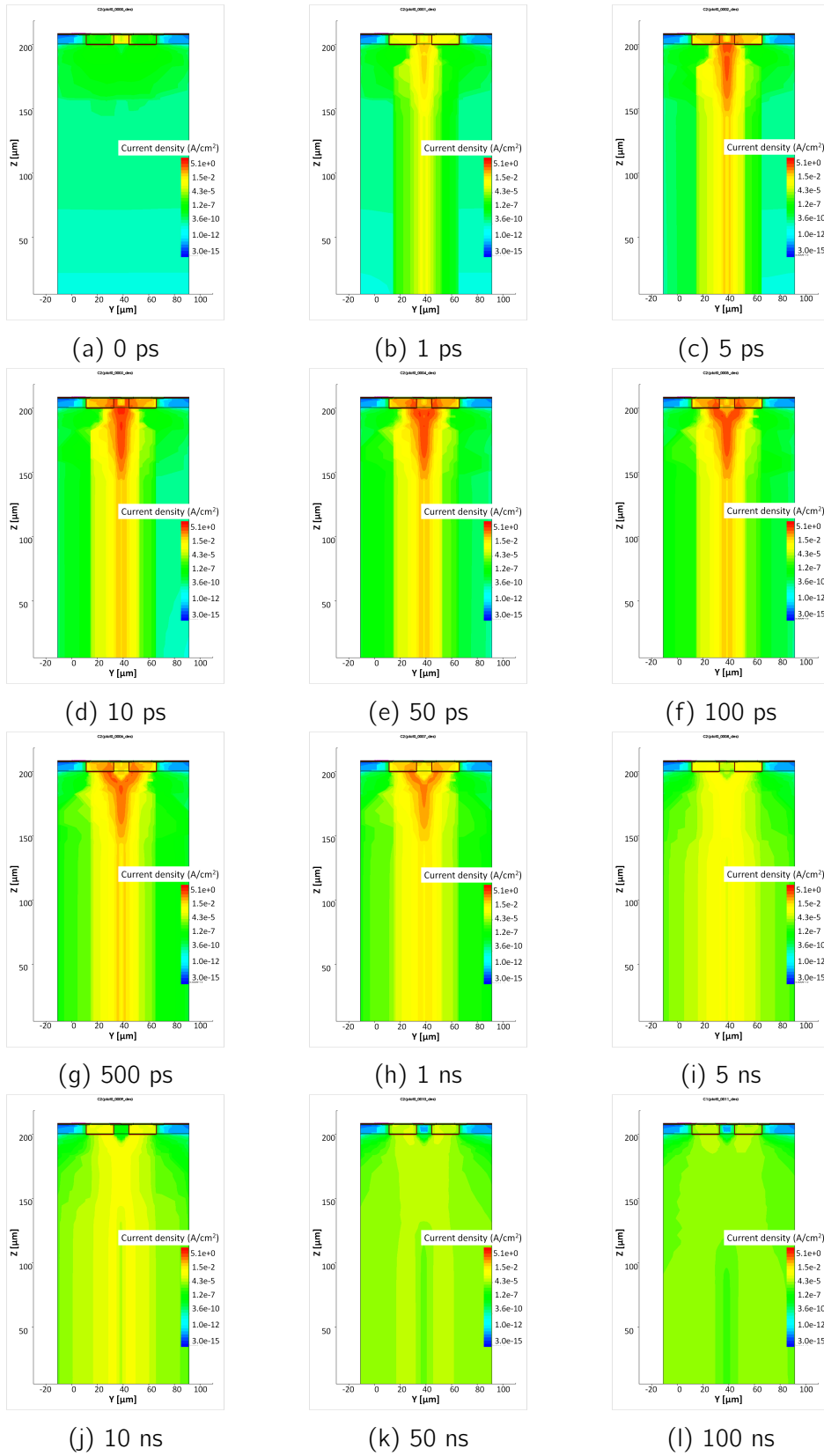


Figure 4.31 – Electron current density variation in position 10

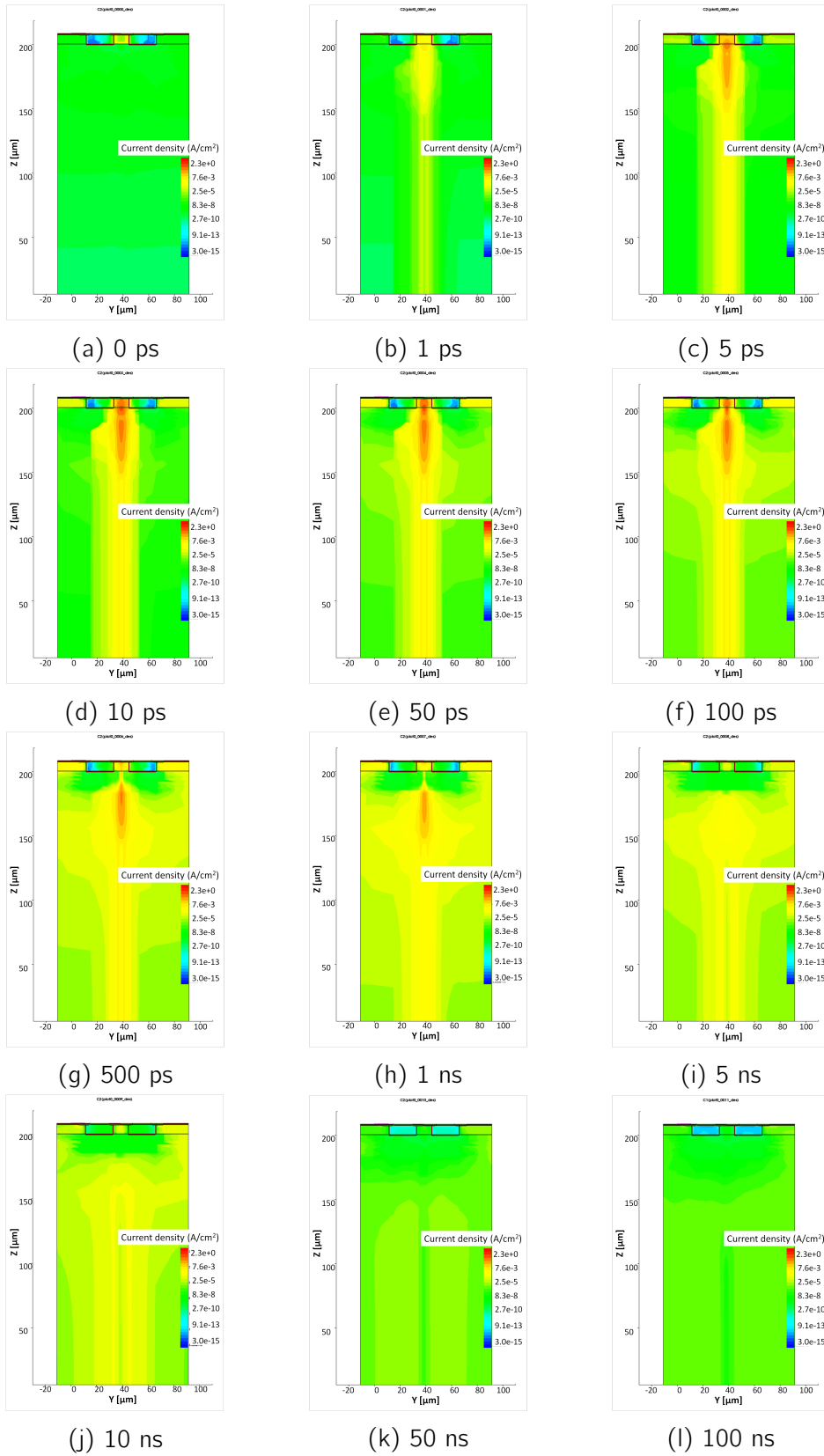


Figure 4.32 – Hole current density variation in position 10

the un-depleted regions respectively. The charge collection profile is shown in Figure 4.33. The charges collected by drift account for 3250 electrons, for a par-

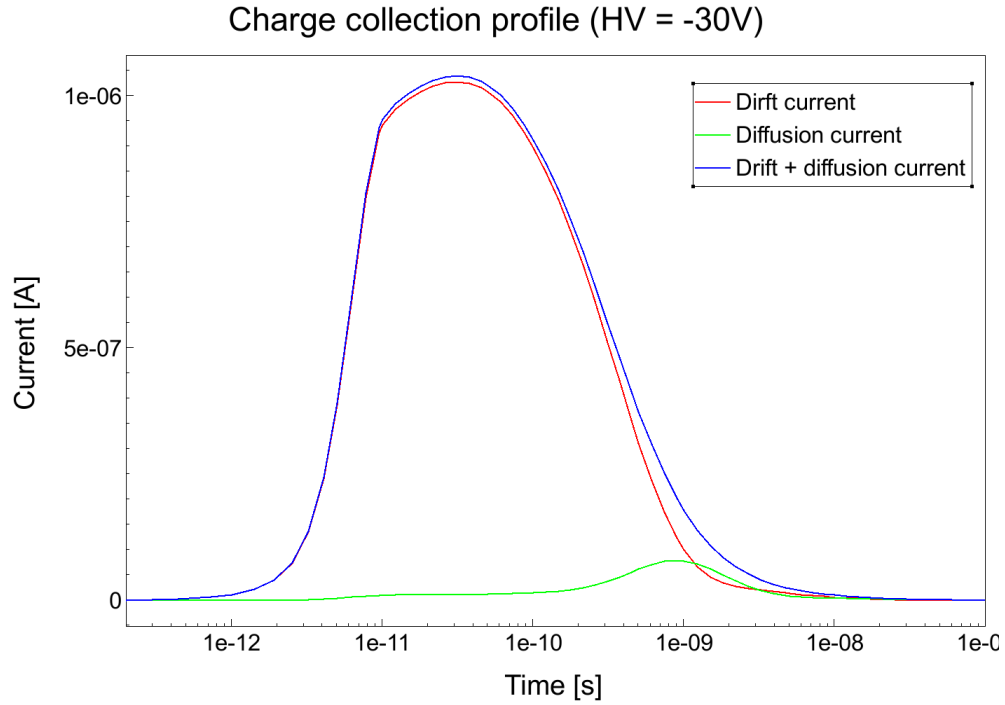


Figure 4.33 – Charge collection profile with log scale (HV=-30V)

ticle impinging position 1, 74% of the total collected charge and with a collection time peaking at 40 ps. The charges collected by diffusion account for 1125 electrons, 26% of the total collected charges and peaking at 1 ns. This diffusion peak is induced by the charges close to the depletion edges. The diffusion process finishes in few hundred nanoseconds.

4.3.1.6 NIEL effect

As discussed in Section 2.4.1, the charge collection in the sensor is significantly affected due to the traps induced by the bulk damage. The induced traps also increase the leakage current dramatically. The bulk damage effect implementation methodology in the simulation has been described in Section 4.2.5.

The leakage current variations with different fluences are shown in Figure 4.34. The leakage current values (HV = -30 V) are listed in Table 4.2 for few NIEL values ; typically of what could be found for the inner layers at the HL-LHC.

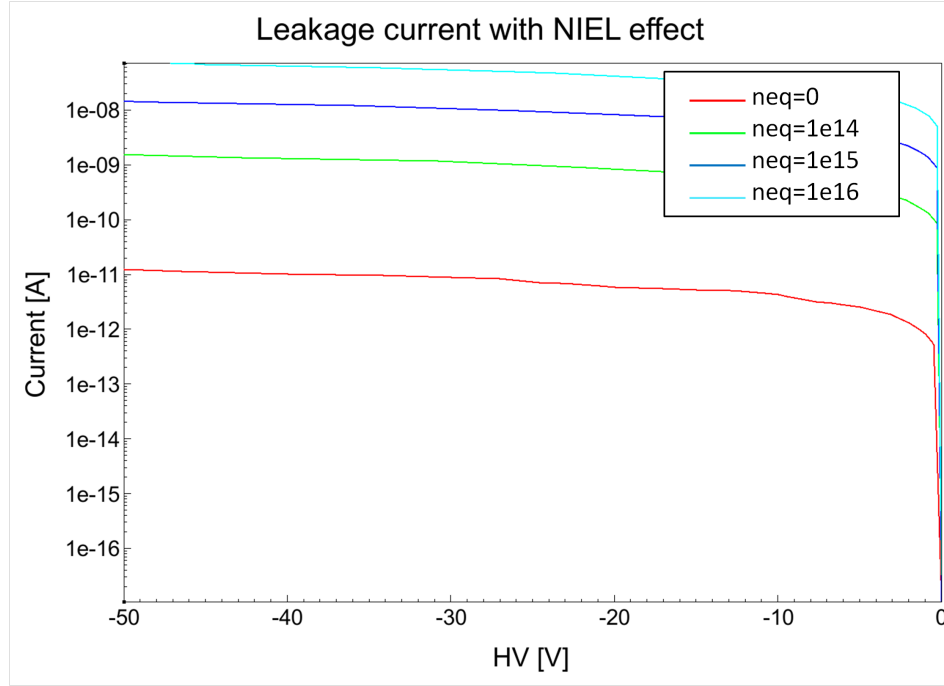


Figure 4.34 – Leakage current vs. HV with NIEL effect for fluence of 0, 1×10^{14} , 1×10^{15} and $1 \times 10^{16} \text{ n}_{eq} \cdot \text{cm}^{-2}$

Table 4.2 – Leakage current considering NIEL effect (HV=-30V)

Fluence ($n_{eq} \cdot \text{cm}^{-2}$)	Current (A)
0	9.1×10^{-12}
1×10^{14}	1.2×10^{-9}
1×10^{15}	1.1×10^{-8}
1×10^{16}	5.6×10^{-8}

The collected charge for an impinging MIP at position 1 is shown in Figure 4.35 for different NIEL values. The charge collection efficiency decreases with increasing irradiation fluence. The collected charges within 5 ns are listed in Table 4.3.

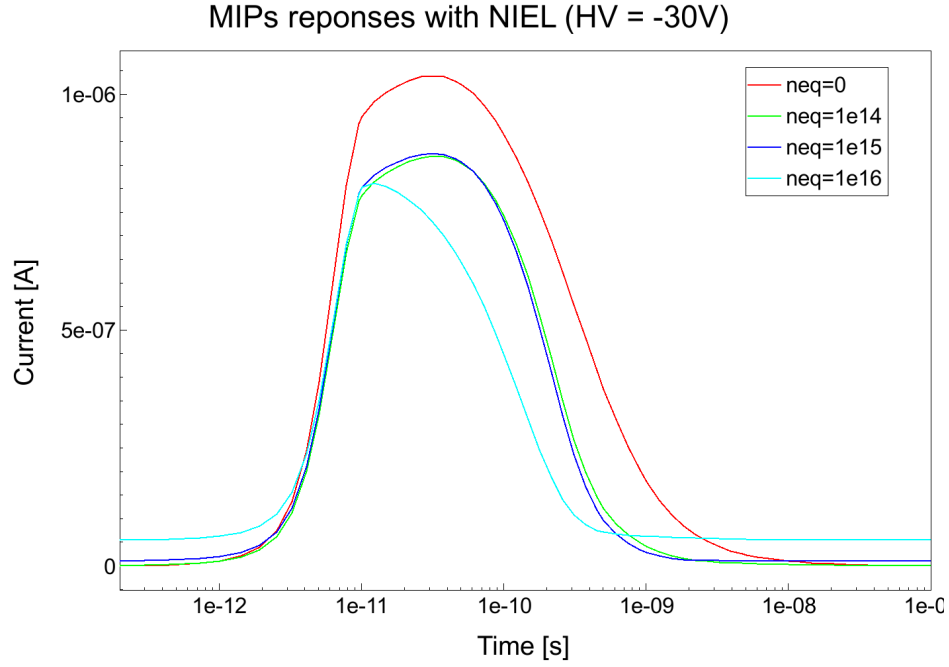


Figure 4.35 – MIPs responses with NIEL effect for an impinging particle in position 1

Table 4.3 – Collected charge taking into account NIEL effect for an impinging particle in position 1 (HV=-30V)

Fluence ($n_{eq} \cdot cm^{-2}$)	Charge (e-)
0	4380
1×10^{14}	1837
1×10^{15}	1437
1×10^{16}	918

The charge collection profiles are also simulated in order to investigate the NIEL effect on the carrier transportation. The profiles are shown in Figure 4.36 for several fluences. The charge contributions, collected within 5 ns, coming from

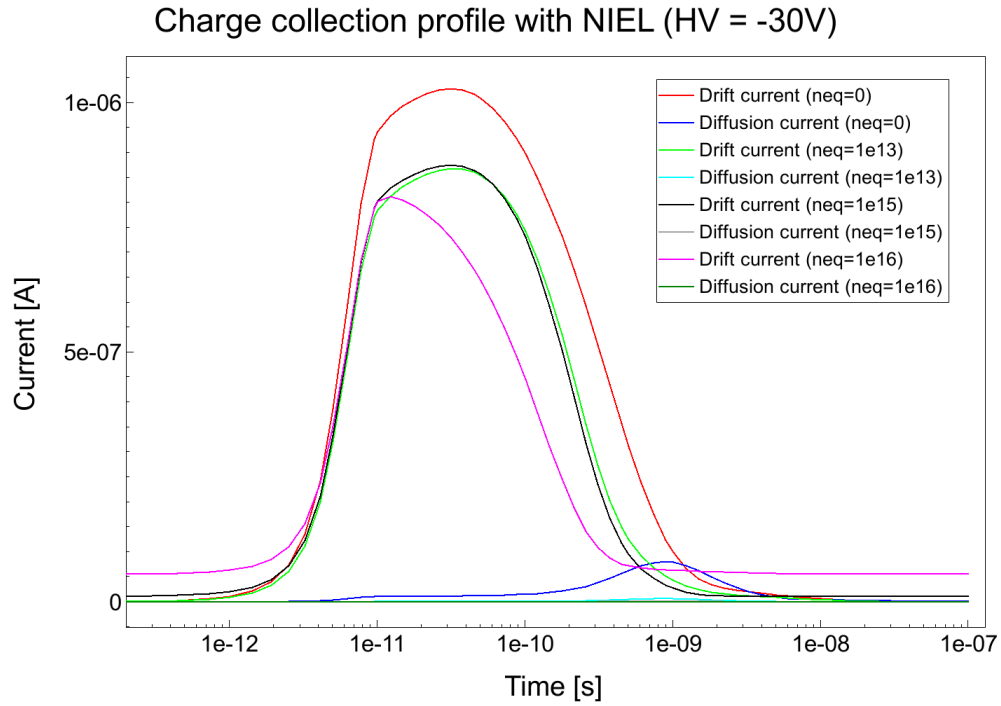


Figure 4.36 – Charge collection profile with NIEL effect

drift and diffusion respectively are detailed in Table 4.4. One can see that 90% of the diffusion charge is lost at the rather low fluence of $1 \times 10^{13} \text{ } n_{eq} \cdot \text{cm}^{-2}$. After the fluence of $1 \times 10^{16} \text{ } n_{eq} \cdot \text{cm}^{-2}$, there is no more diffusion charge collected.

Table 4.4 – Charge collection profiles with NIEL effect (HV=-30V)

Fluence ($n_{eq} \cdot \text{cm}^{-2}$)	Drift charge (e-)	Diffusion charge (e-)	Total charge (e-)
0	3250	1130	4380
1×10^{13}	1981	81	2062
1×10^{15}	1125	31	1156
1×10^{16}	918	0	918

4.3.1.7 Temperature effect

As discussed in Sections 2.1.1.2 and 2.1.1.3, the carrier mobility and the generation-recombination process depend on the lattice temperature, and influence the leakage current and charge collection behavior. In this section, only the lattice temperature variation is taken into account. The carrier temperature effect is neglected.

The leakage current variation as a function of the HV and at a lower temperature of $-6\text{ }^{\circ}\text{C}$ temperature at different irradiation fluences is shown in Figure 4.37.

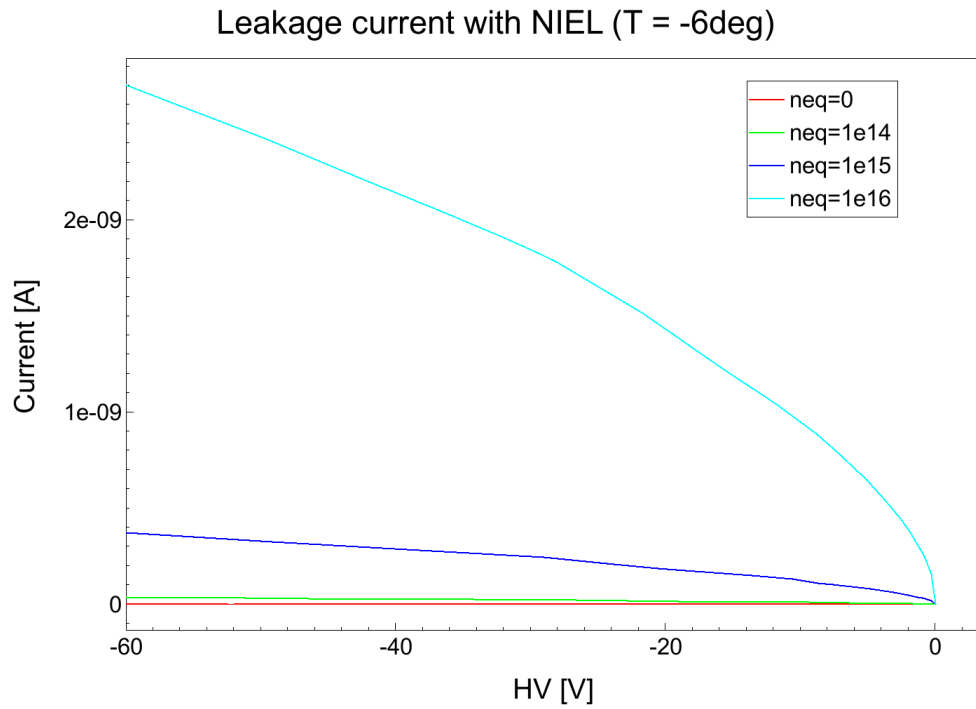


Figure 4.37 – Leakage current with temperature effect

A leakage current variation comparison for different temperatures is shown in Table 4.5. At $-6\text{ }^{\circ}\text{C}$, compared with room temperature results, the leakage

Fluence ($n_{eq} \cdot \text{cm}^{-2}$)	Current at $27\text{ }^{\circ}\text{C}$ (A)	Current at $-6\text{ }^{\circ}\text{C}$ (A)
0	9.1×10^{-12}	3.5×10^{-13}
1×10^{14}	1.2×10^{-9}	2.4×10^{-11}
1×10^{15}	1.1×10^{-8}	2.5×10^{-10}
1×10^{16}	5.6×10^{-8}	1.8×10^{-9}

current decreases roughly by a factor of 30.

The MIP responses for an impinging particle in position 1 at different temperatures are shown in Figure 4.38. With increased carrier lifetime and lower

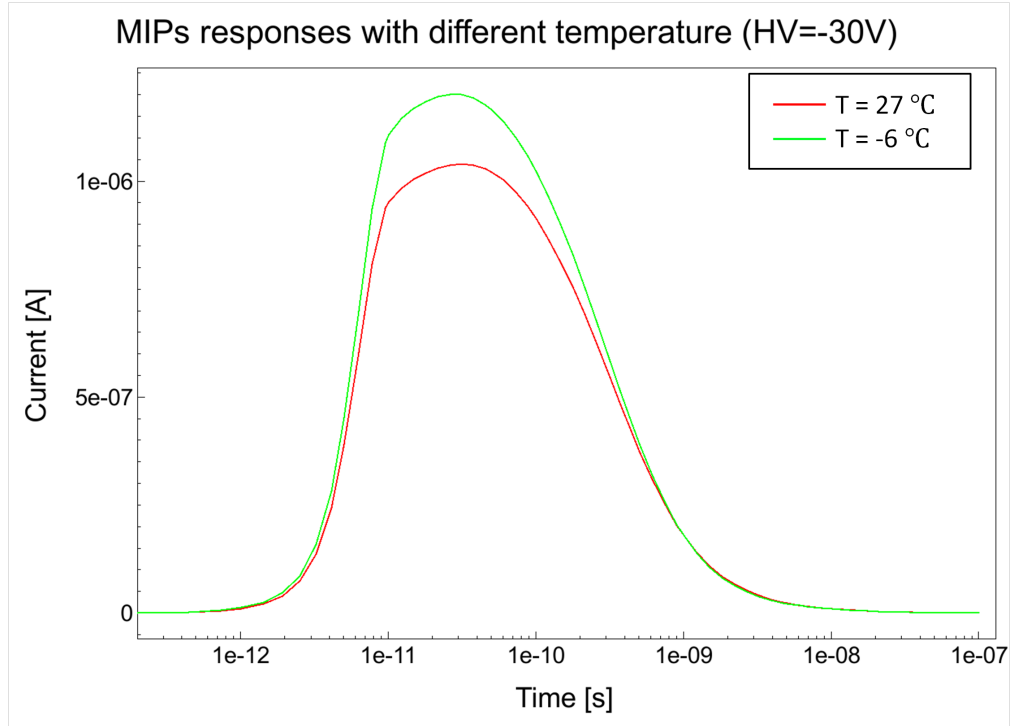


Figure 4.38 – MIPs responses with temperature effect

generation-recombination rate, the collected charges increases only by $\sim 1\%$ at $-6\text{ }^{\circ}\text{C}$. Although there is no significant improvement for the charge collection efficiency, the reduced leakage current would have great help for the reduction of the electronics noise.

4.3.2 Type B technology simulation

The type B technology is a 150 nm CMOS process on high resistivity (typically $2k\Omega \cdot cm$) p-type substrate. The TCAD simulation procedures are similar to what has been done for the type A technology. In this section, the DC, AC and transient simulation results will be shown and the charge collection behavior with NIEL and temperature effects will also be discussed.

4.3.2.1 Depleted region

The HV is applied to the substrate from the top-side (the side of the electronics implementation). The depleted regions with different biasing voltages are shown in Figures 4.39a and 4.39b. One can see here the depletion region increasing as a function of the HV. The depleted depth as a function of HV is shown in

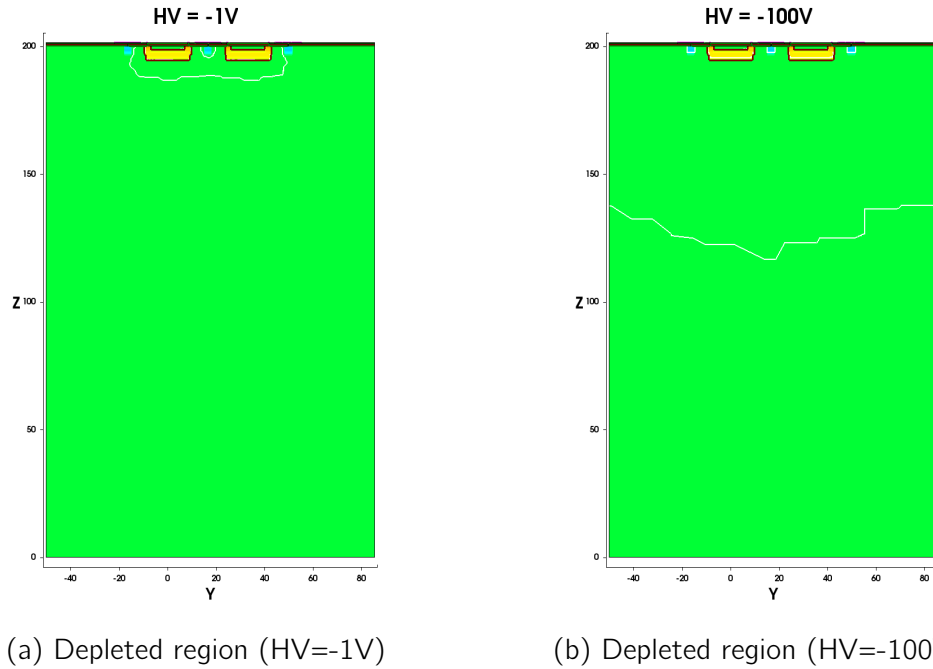


Figure 4.39 – The depletion region evaluations for the values of HV from -1 V to -100 V.

Figure 4.40. $57\mu m$ and $72\mu m$ depleted depth can be obtained when the HV are -50 and -100 V respectively.

4.3.2.2 Electric field

The cut planes of the electric field distribution and corresponding field vectors are shown in Figure 4.41a and 4.41b respectively. The highest electric fields occur in the metallurgical junction regions close to the silicon and oxide interfaces.

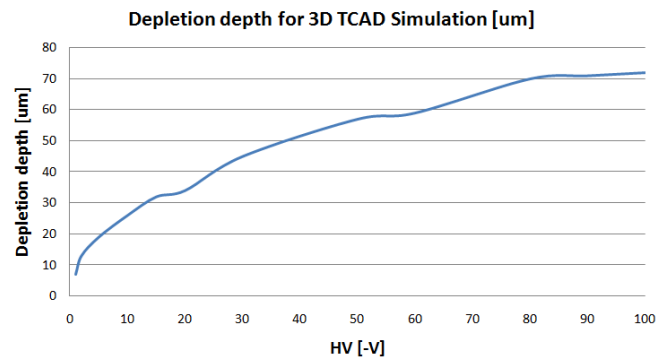
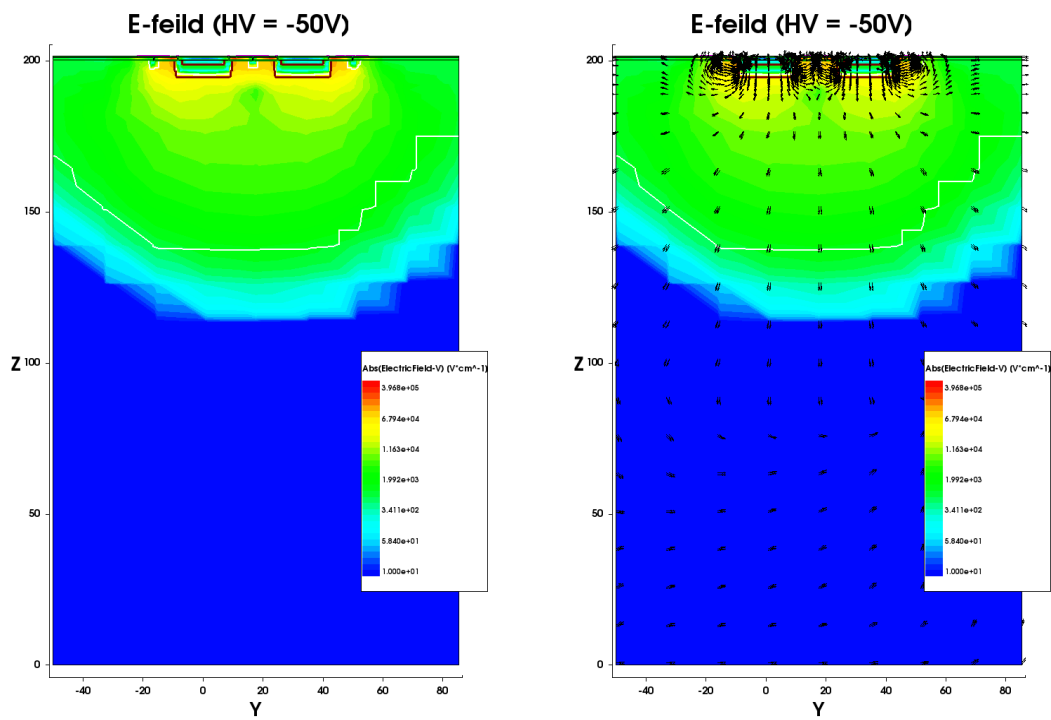


Figure 4.40 – Depleted depth vs. HV



(a) Electric field distribution

(b) Electric field vector

Figure 4.41 – The electric field distribution and the field vector (HV = -50 V).

This high field region would dominate the breakdown voltage. An extended gap between the DNW and PWell pixel guard-ring could reduce the electric field value and increase the breakdown voltage. We will see later that this is a solution which was simulated and chosen the the CPIX V2 prototype in Section 4.3.2.6.

4.3.2.3 Leakage current and capacitance

The leakage current of one pixel as a function of bias voltages with various neutron equivalent fluences are shown in Figure 4.42. The breakdown voltage is around -106 V before irradiation. The leakage current increases with increasing irradiation fluences. The values of the leakage current when the high voltage is -50 V are listed in Table 4.6. In comparison with a low resistivity substrate, the leakage current increases significantly due to the larger depleted areas.

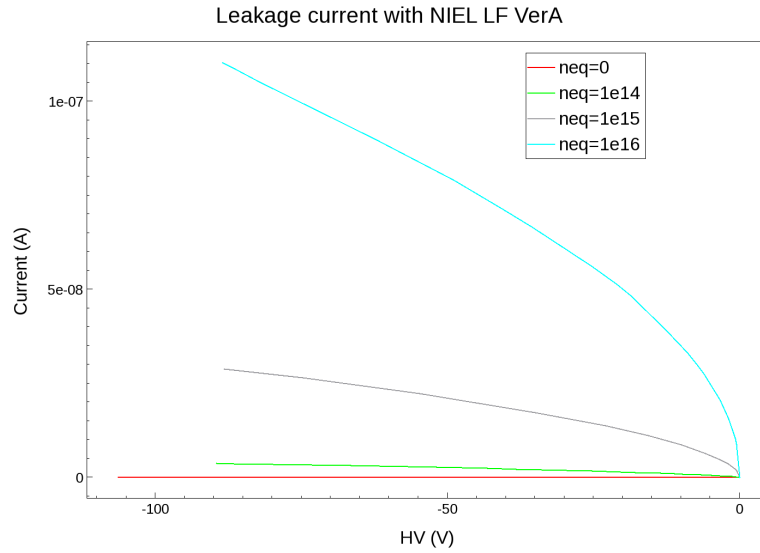


Figure 4.42 – Leakage current vs. HV with NIEL effect

Table 4.6 – Leakage current with NIEL effect (HV=-50V)

Fluence ($n_{eq} \cdot cm^{-2}$)	Current (A)
0	2.1×10^{-11}
1×10^{14}	2.6×10^{-9}
1×10^{15}	2.1×10^{-8}
1×10^{16}	8.0×10^{-8}

Reduced leakage current is expected when the temperature is decreased. The leakage current at $-6\text{ }^{\circ}\text{C}$ is shown in Figure 4.43, and the currents at HV = -50 V are given in Table 4.7.

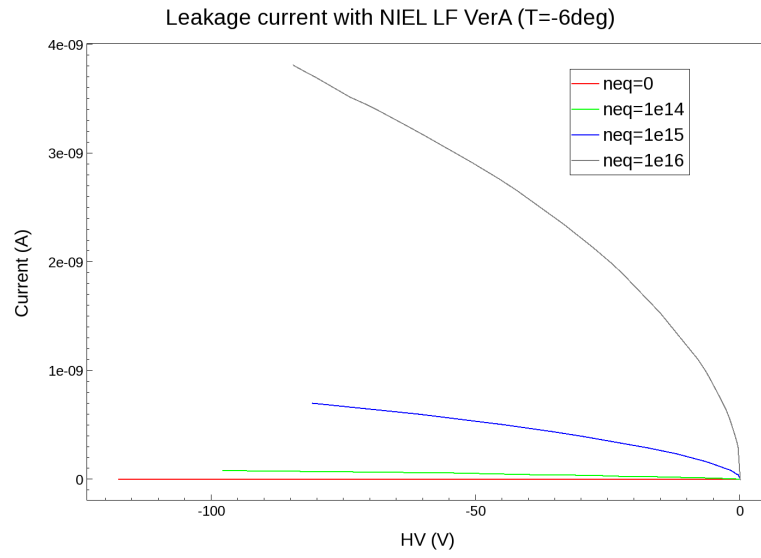


Figure 4.43 – Leakage current at $-6\text{ }^{\circ}\text{C}$

Table 4.7 – Leakage current at $-6\text{ }^{\circ}\text{C}$ (HV=-50V)

Fluence ($n_{eq} \cdot cm^{-2}$)	Current (A)
0	8.3×10^{-13}
1×10^{14}	5.7×10^{-11}
1×10^{15}	5.4×10^{-10}
1×10^{16}	2.9×10^{-9}

The capacitance of the DNW as a function of the HV is shown in Figure 4.44. For one pixel the DNW capacitance is roughly 44 fF when the HV is -50 V.

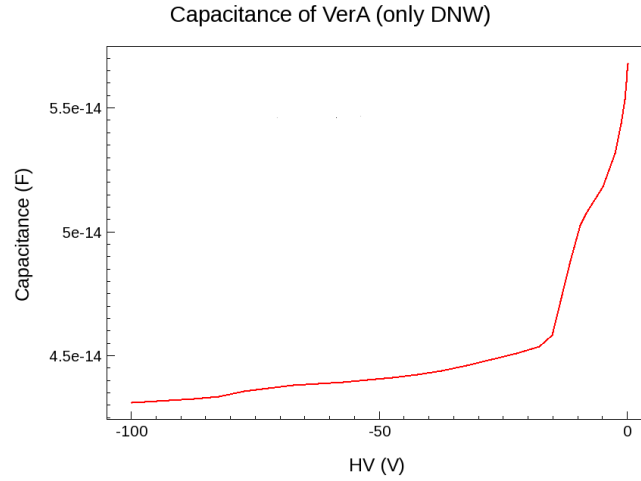


Figure 4.44 – DNW capacitance vs. HV (Type B VerA)

In order to gain insight into the precise input capacitance of this kind of pixel geometry, the NWell, NISO, PWell and PSUB layers inside one pixel are implemented into the simulation. The top view and cut-plane of the simulated device are shown in Figure 4.45a and 4.45b.

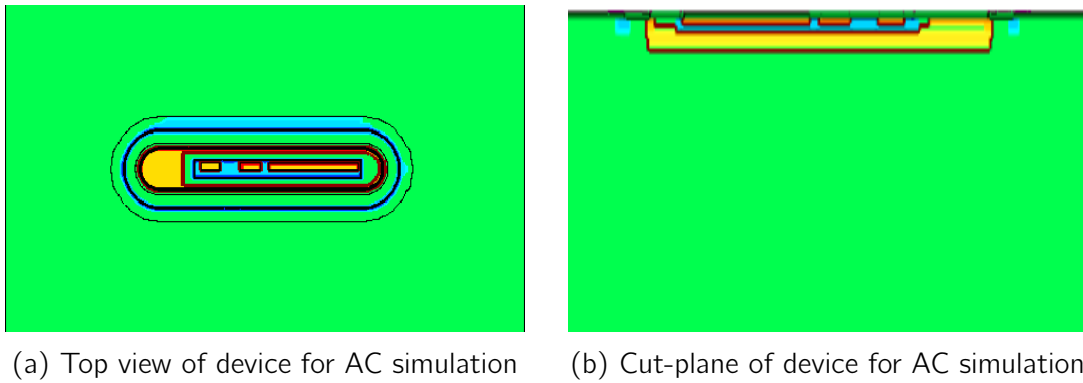


Figure 4.45 – The top view and the cut-plane of the simulation structure for the AC simulation.

The total input capacitance is shown in Figure 4.46 as a function of the HV. The input capacitance increases to roughly 200 fF taking in account the PWells and NWells inside pixel.

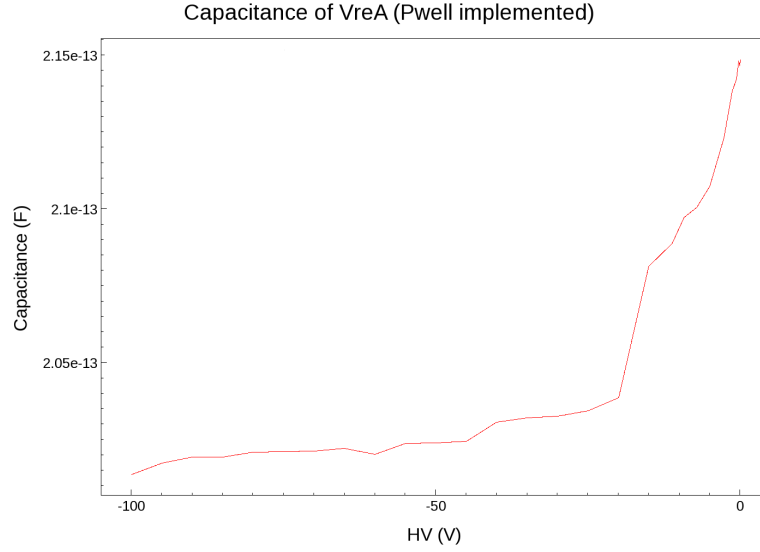


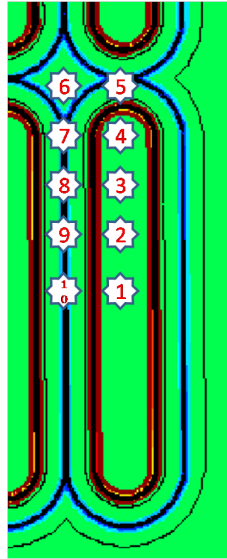
Figure 4.46 – Total input capacitance vs. HV (LF VerA)

4.3.2.4 Transient simulations

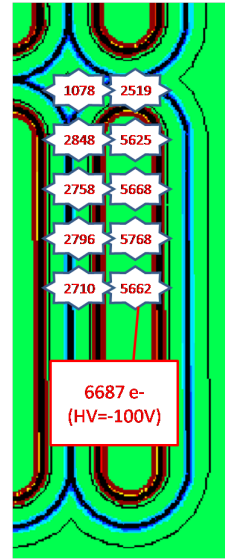
Transient simulations were also performed for the Type B technology to investigate the charge collection. The particle impinging positions and corresponding charge collections within 5 ns ($HV = -50$ V) for one specific pixel are shown in Figure 4.47a and 4.47b.

The charges in the border regions are shared between neighbor pixels. Improved charge collection can be obtained with increased high voltage due to the enlarged depleted region, as shown in Figure 4.47b.

The transient current evolution for ten different particle hit positions is shown in Figure 4.48 as a function of collection time. Most of the charges generated by the impinging particle can be collected within 5 ns. The rest of the charges mainly come from diffusion. To visualize the charge collection process, the electron and hole current densities for two hit positions 1 and 10 are shown from Figure 4.49 to Figure 4.52.



(a) Particle impinging positions



(b) Collected charges within 5 ns (HV=-50V)

Figure 4.47 – The particles impinging positions and the collected charges in the first 5 ns.

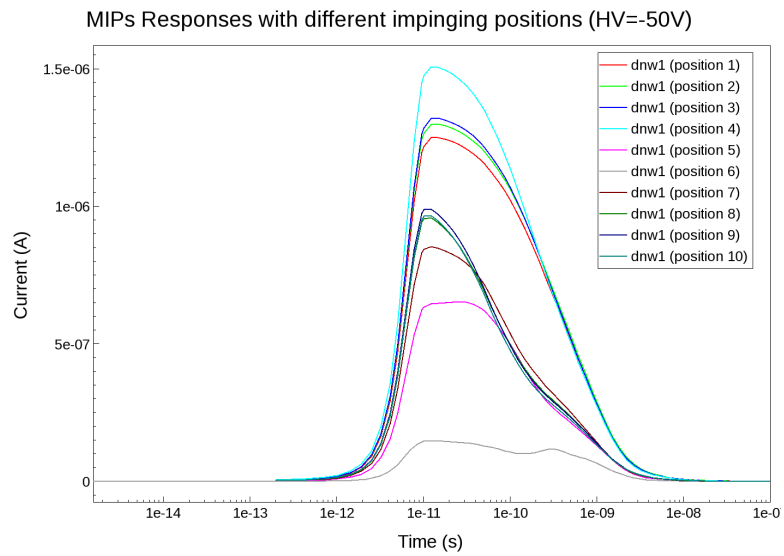


Figure 4.48 – DNW responses for impinging particles (HV = -50 V)

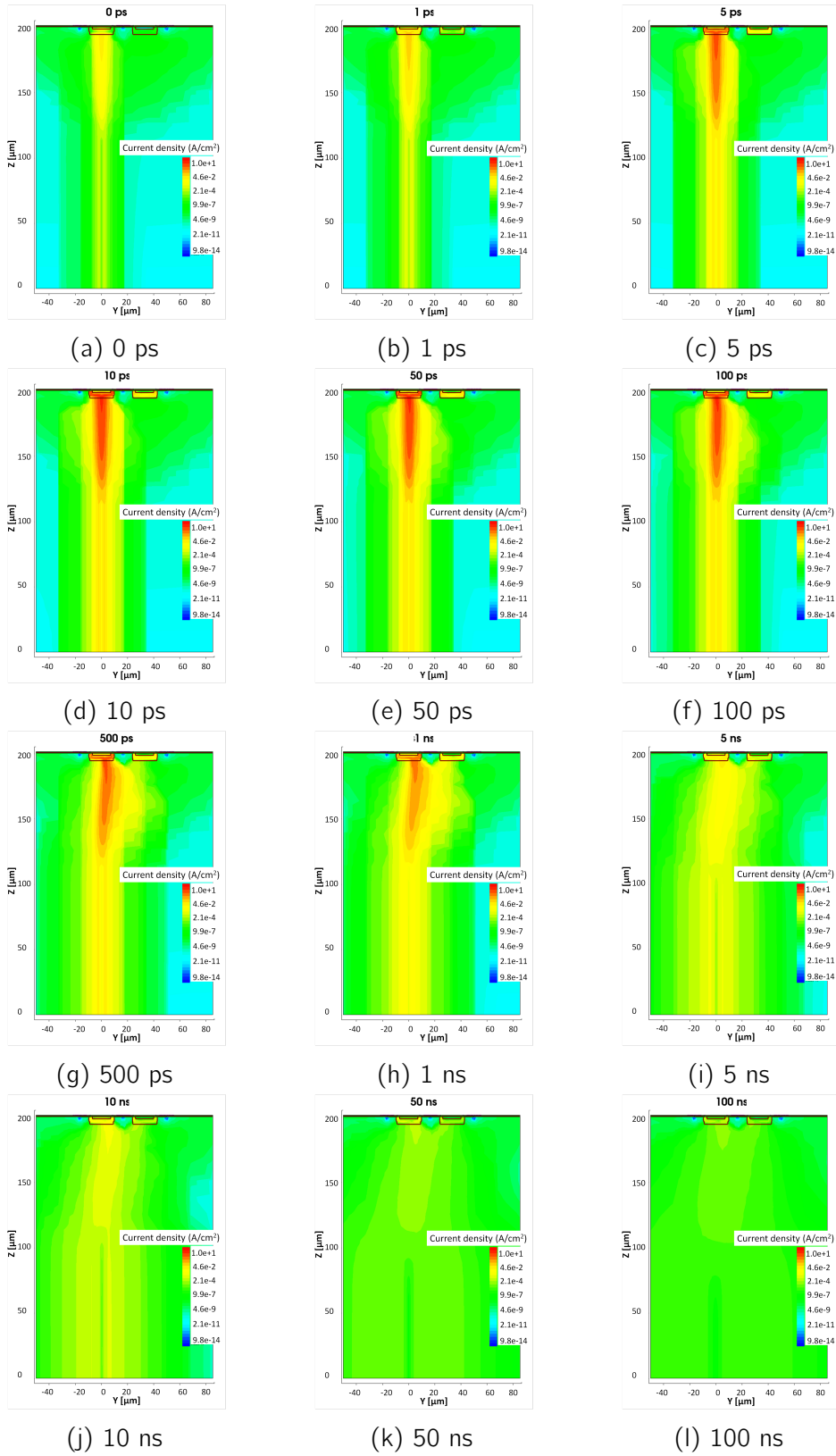


Figure 4.49 – Electron current density variation in position 1

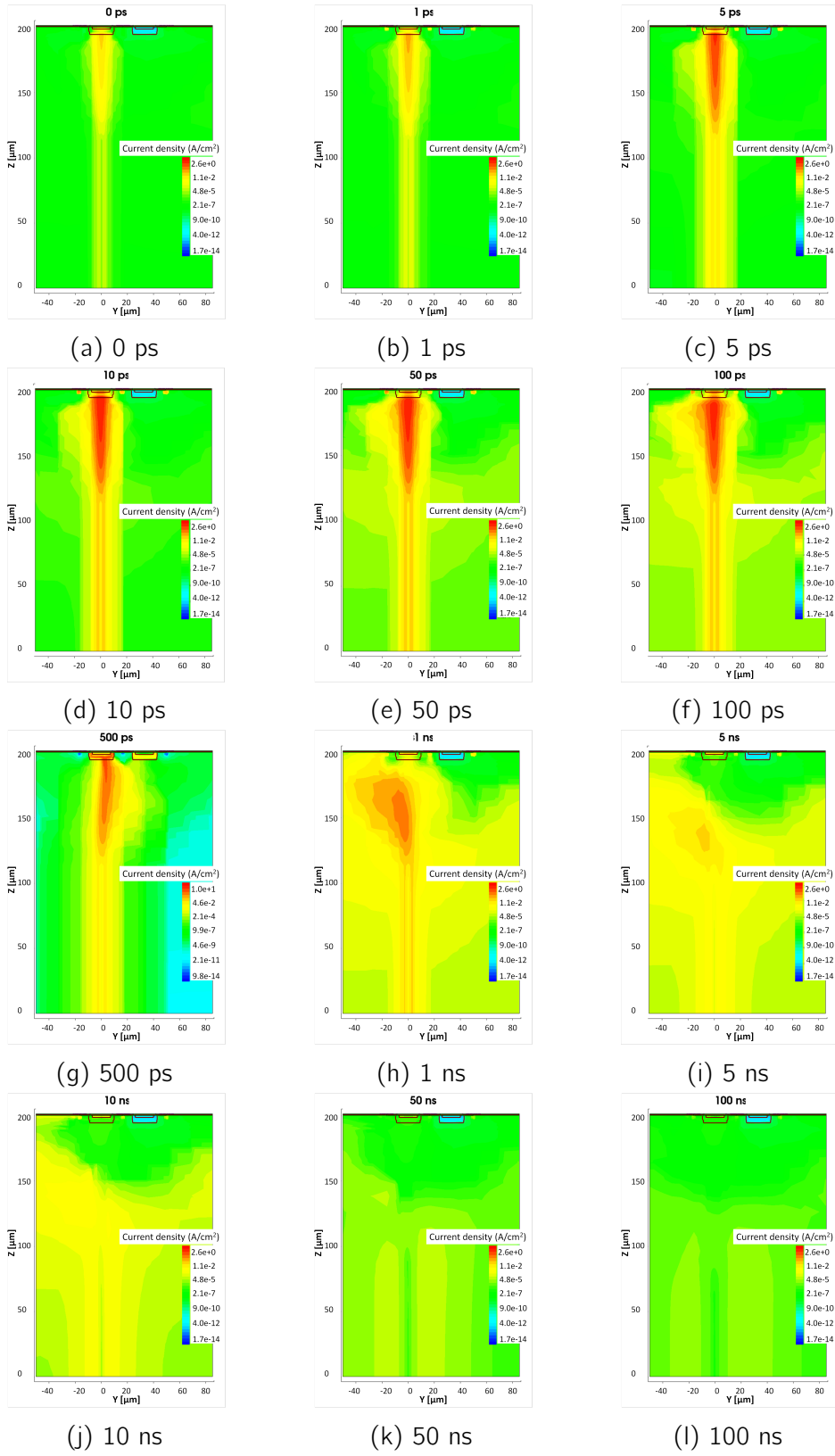


Figure 4.50 – Hole current density variation in position 1

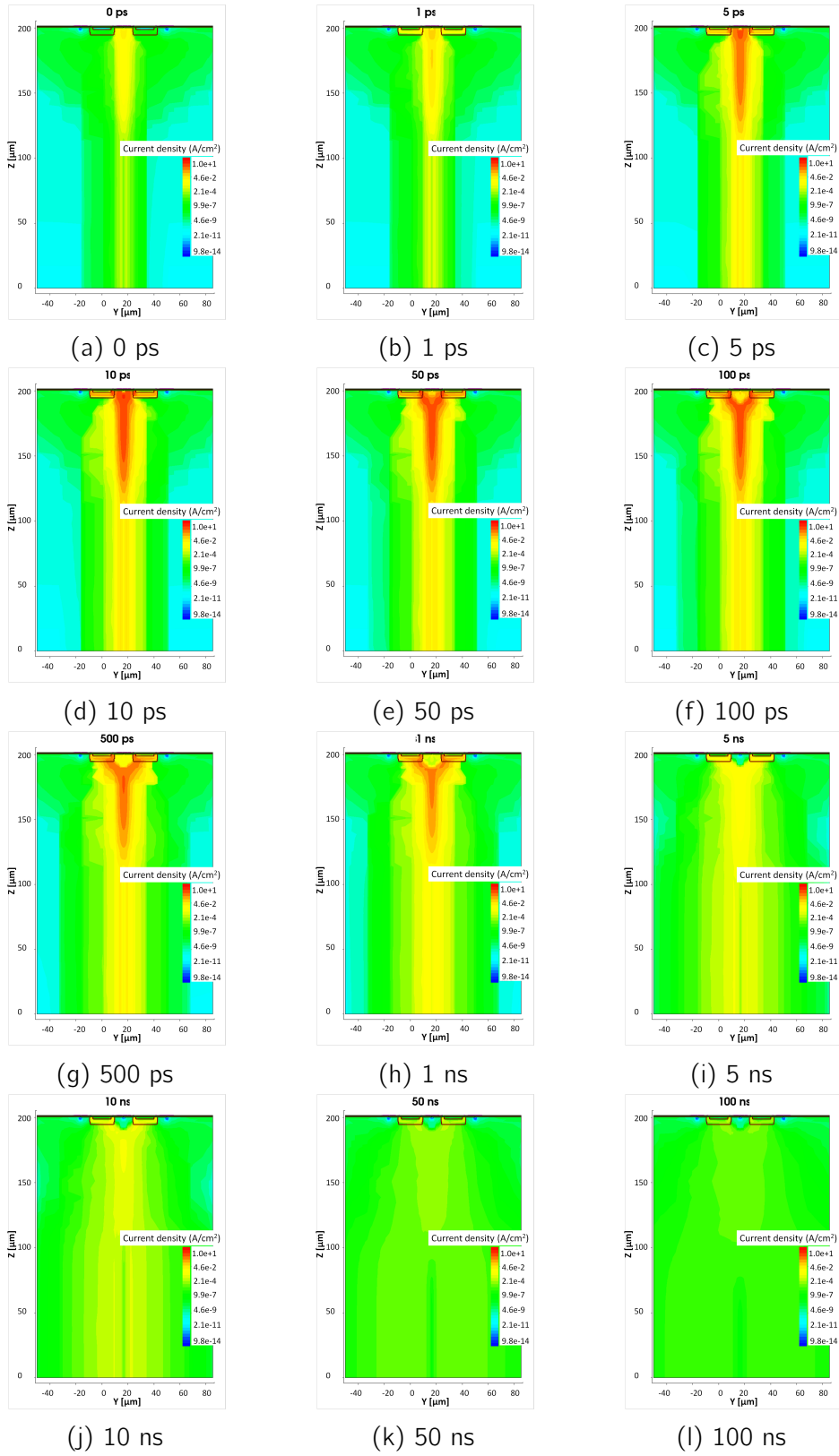


Figure 4.51 – Electron current density variation in position 10

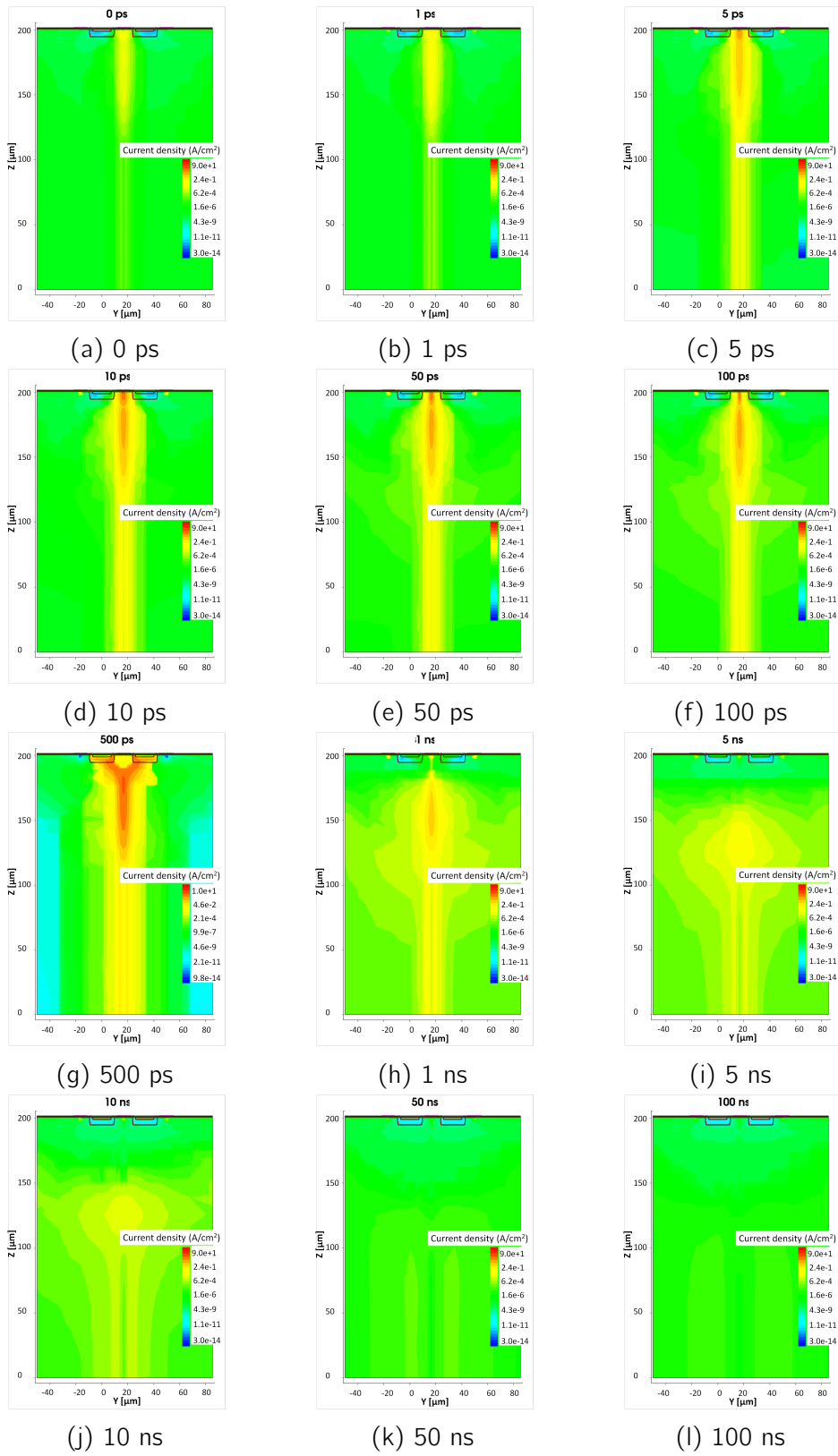


Figure 4.52 – Hole current density variation in position 10

In order to explore the contributions of the collected charge coming respectively from drift and from diffusion, the charge generation is activated only in the depleted region and in the un-depleted region respectively. The DNW responses (hit in position 1 in Figure 4.47a) from drift and diffusion charges are shown in Figure 4.53. The charges collected by drift account for almost 85% of the total

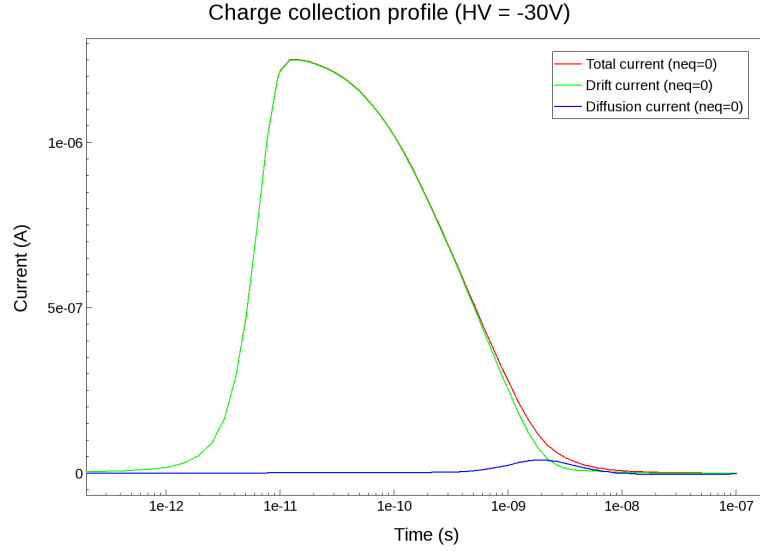


Figure 4.53 – Charge collection profile (LF VerA)

collected charge. As can be seen in Table 4.8, the quantity of collected charge reduces to almost half after the radiation fluence of $1 \times 10^{15} \text{ } n_{eq} \cdot \text{cm}^{-2}$ with respect to its initial value. At the fluence of $1 \times 10^{16} \text{ } n_{eq} \cdot \text{cm}^{-2}$, still the collected charges are above 1000 electrons.

Table 4.8 – Charge collection profiles with NIEL effect (HV=-50V)

Fluence ($n_{eq} \cdot \text{cm}^{-2}$)	Drift charge (e-)	Diffusion charge (e-)	Total charge (e-)
0	4812	850	5702
1×10^{14}	4507	491	4998
1×10^{15}	2536	188	2724
1×10^{16}	1081	0	1081

The DNW response for room temperature and $-6 \text{ } ^\circ\text{C}$ is shown in Figure 4.54. The collected charges increase by 2% when the temperature reduces from $27 \text{ } ^\circ\text{C}$ to $-6 \text{ } ^\circ\text{C}$ due to the longer carrier lifetime and the lower generation recombination rate. This is no big help for the charge collection but the reduced leakage current will decrease the noise significantly.

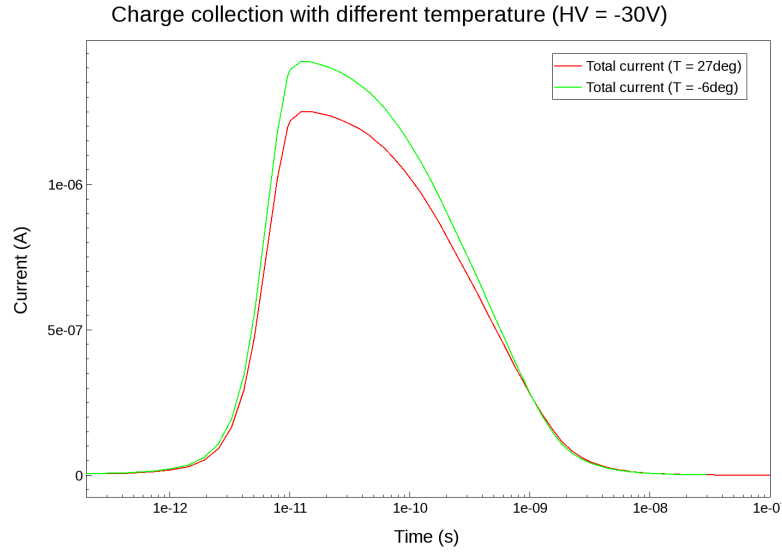


Figure 4.54 – Charge collection at different temperatures

4.3.2.5 Breakdown simulation of Version B geometry

In this section, a new sensor geometry, called versionB, is simulated. In this layout, the charge collection diode is separated from the electronics in order to reduce the input capacitance. The 3D simulation of the device is shown in Figure 4.55. The cut plane of the doping for this sensor is shown in Figure 4.56.

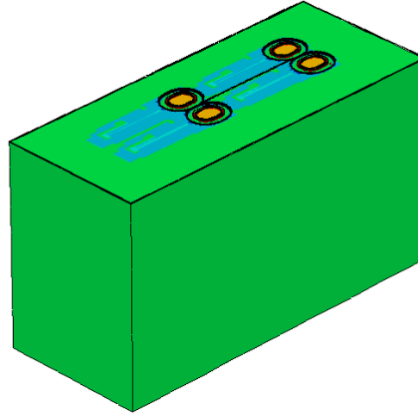


Figure 4.55 – 3D device for versionB simulation

The DNW is connected to +HV and the PW is for electronics implementation.

The leakage current is shown in Figure 4.57 as a function of HV. The breakdown voltage is roughly 38 V which is lower than the versionA due to the existence of a voltage difference between the DNW and the PW. The electric field



Figure 4.56 – Cut-plane of versionB doping

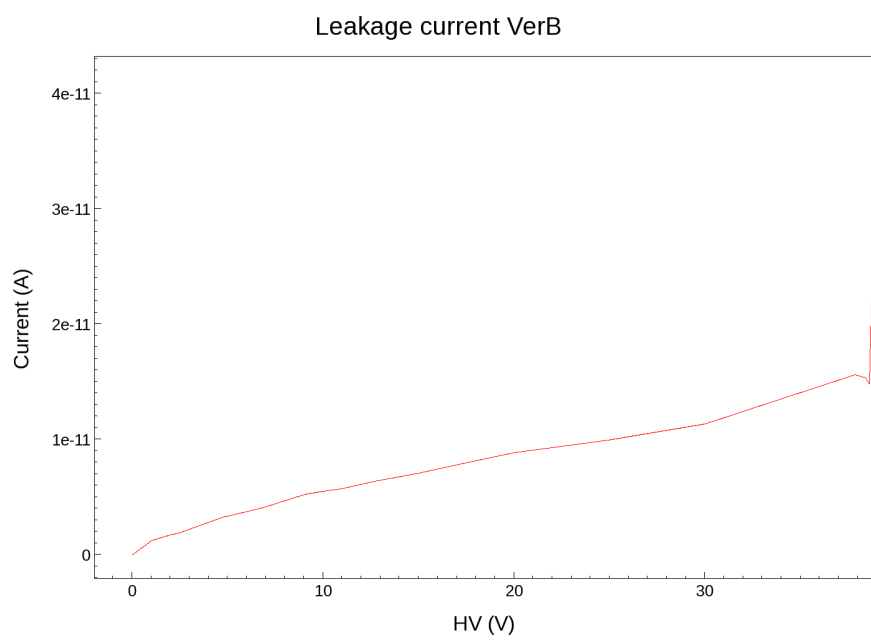


Figure 4.57 – Leakage current vs. HV

distribution is shown in Figure 4.58. The maximum electric field occurs in the junction region formed by the DNW and the PW, and dominates the breakdown voltage due to the relatively heavy doping.

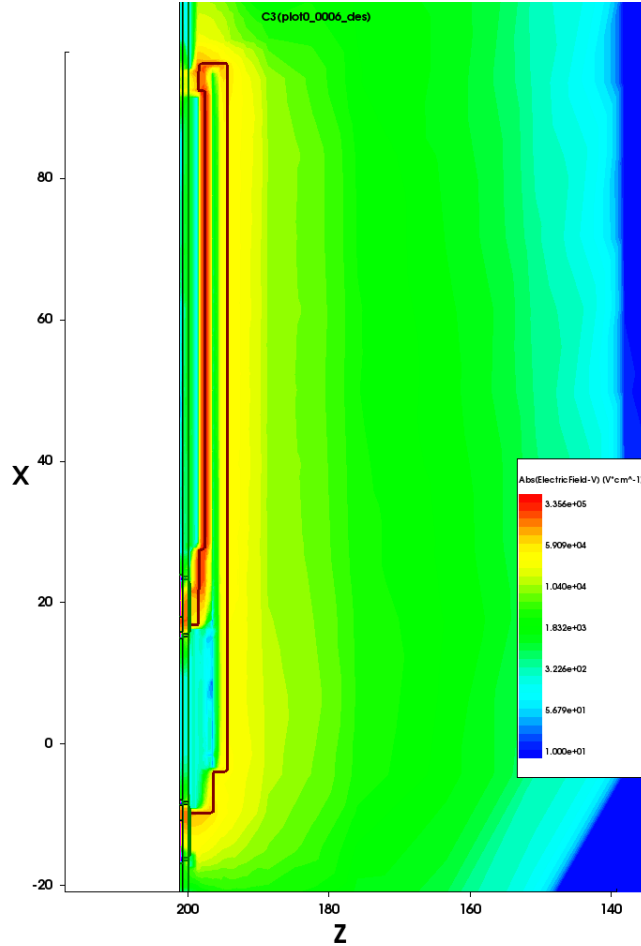


Figure 4.58 – Electric field of vesionB

4.3.2.6 Simulation of guard-rings

From the characterizations of CCPD prototypes (will be discussed in Section 5.2.3), the guard-ring layout can be optimized in order to increase the breakdown voltage and reduce the inactive area. Two large size demonstrators are being designed early 2016 using this technology named : CPIX V1 and V2. Both chips have the same pixel size as the FE-I4 pixel to demonstrate the sensor performance for ATLAS upgrade. For the guard-rings, the CPIX V1 will use a conservative strategy with the guard-rings having exact the same size as for the earlier CCPD prototypes, as sketched in Figure 4.59, but the CPIX V2 was optimized to reduce inactive area following the studies described below.

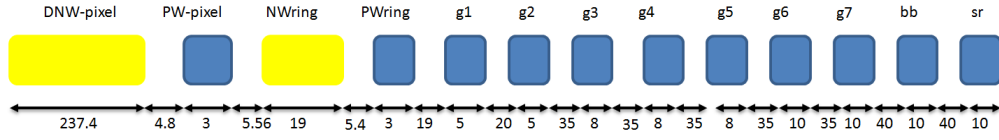


Figure 4.59 – LF CPIX V1 guardring layout

The pixel region as implemented in the simulation is shown in Figure 4.60. Fixed charge and interface traps were implemented in the STI. The NIEL effects were also taken into account in the bulk. In simulation, the current recorded by the DNW-pixel and by the NWring were measured. For the top-side and back-side

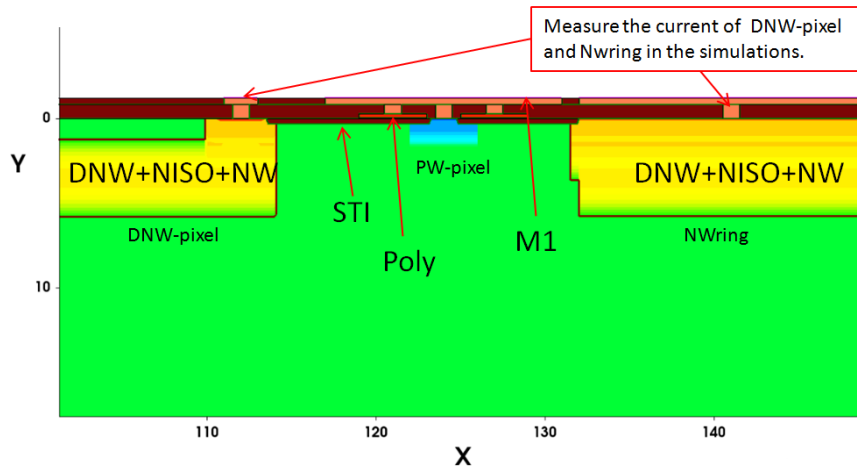


Figure 4.60 – LF CPIX V1 simulation of the structure

biasing cases, the sensor thickness were set to $30\mu m$ and $100\mu m$ respectively. For the top-side bias, the PW-pixel, bb (backbias) and sr (seal-ring) were connected to - HV, DNW-pixel and NWring to VDDA and the remaining guard-rings were floating. For the backside bias, the backplane was biased with - HV, the DNW-pixel and NWring were connected to VDDA and the remaining guard-rings were floating.

The leakage current recorded in the DNW-pixel and in the NWring before and after irradiation are shown in Figure 4.61. One can see that the DNW-pixel dominates the breakdown for both before and after irradiation. After irradiation, the breakdown voltage increases from 90 V to 105 V in the simulation. The breakdown and leakage current are not significantly different in the top-side and in the back-side bias cases.

The depleted regions and electric field distributions (at HV = -100 V) of the top-side bias and of the back-side bias are shown in Figure 4.62. Along the x axis, the distance between the depleted edge and the cutting edge is around $300\mu m$. This means that a guard-ring reduction is possible, which can reduce the inactive

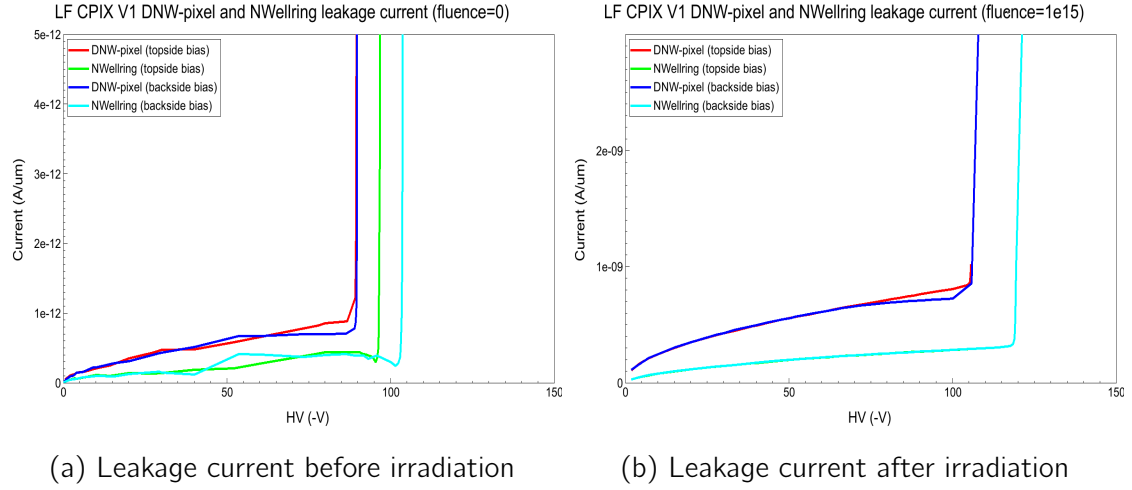


Figure 4.61 – The leakage currents of DNW-pixel and PW-pixel for both top-side and back-side biases. (a) : Before irradiation. (b) : After a fluence of $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$.

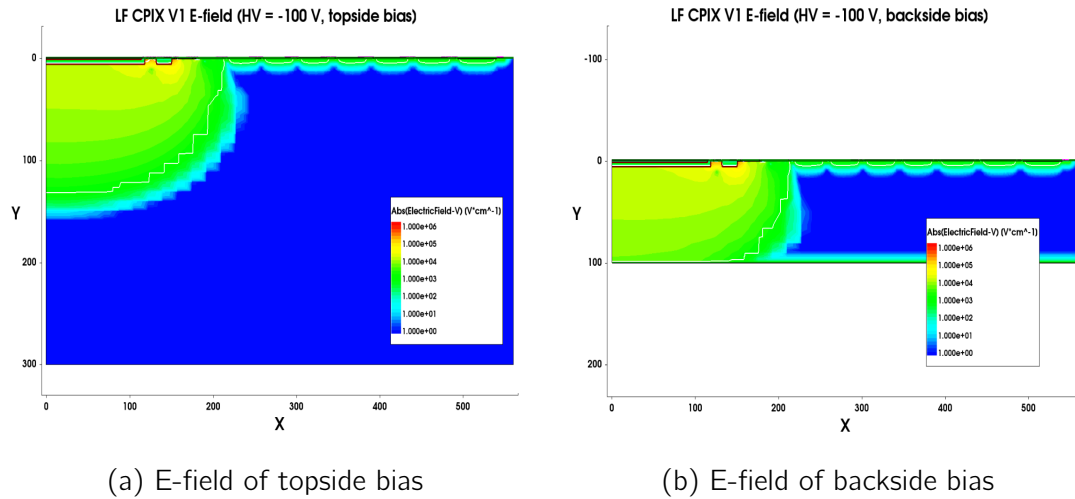


Figure 4.62 – The electric field distribution for both topside and backside biases.

region.

Compared with CPIX V1, the guard-rings of V2 have been modified to increase the breakdown voltage and reduce the dead region. Three scenarios were simulated. The parameters of these three guard-ring layouts are shown in Figure 4.63. Scenario (A) has the same size as CPIX V1 except for the distance between the DNW-pixel and the PW-pixel. In scenario (B), the NWellring was shrunk to in-

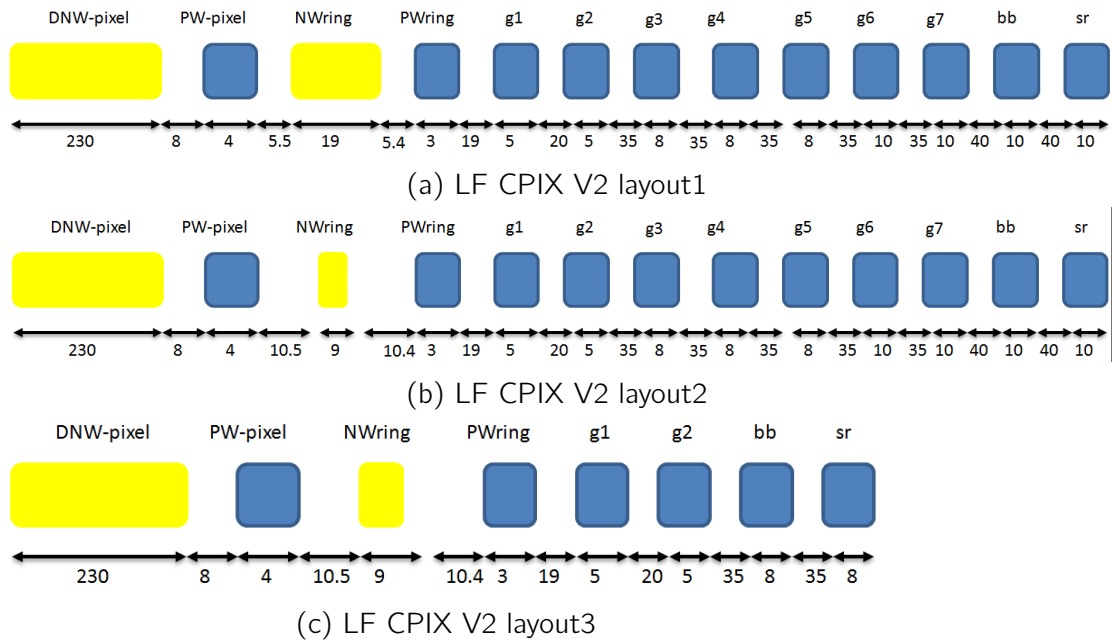


Figure 4.63 – Three guard-ring scenarios. (A) :Default : The same size as LF CPIX V1 except for the distance between DNW-pixel and PW-pixel. (B) : Shrunk NWring : Increase of the distance between NWring and its neighbor PWs to improve the breakdown voltage. (C) : Shrunk NWring + reduced guard-rings : To reduce the inactive area.

crease the breakdown voltage. Scenario (C) keeps the same NWellring but the outer five guardrings are removed to reduce the inactive region.

The leakage currents of the DNW-pixel and of the NWellring for top-side and back-side bias cases are shown in Figures 4.64 and 4.65. One can see the NWellring limits the breakdown voltage for scenario (A) and the breakdown voltage is around 100 V. The breakdown voltage increases to roughly 150 V by shrinking the NWellring for scenario (B). For scenario (C), there is no significant difference after guard-rings removal compared with scenario (B). After irradiation, the breakdown voltage increases from 150 V to 170 V for both scenario (B) and (C).

The depletion regions and electric field distributions for scenario (B) and (C) are shown in Figure 4.66 and 4.67. For scenario (C), one can see that the distance between the end of the depletion area and the cutting edge is roughly

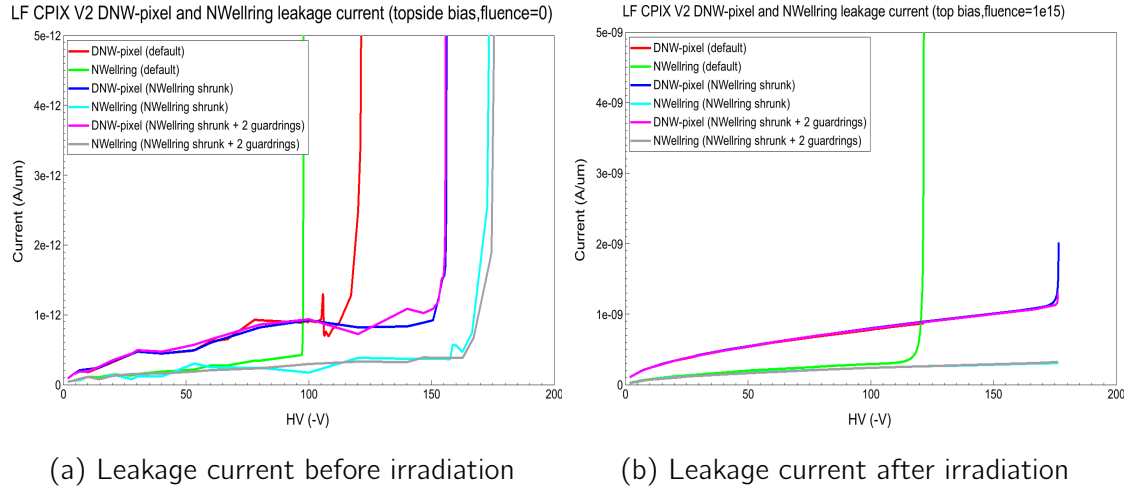


Figure 4.64 – The leakage currents for the DNW-pixel and for the PW-pixel for the top-side bias case. (a) : Before irradiation. (b) : After a fluence of $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$.

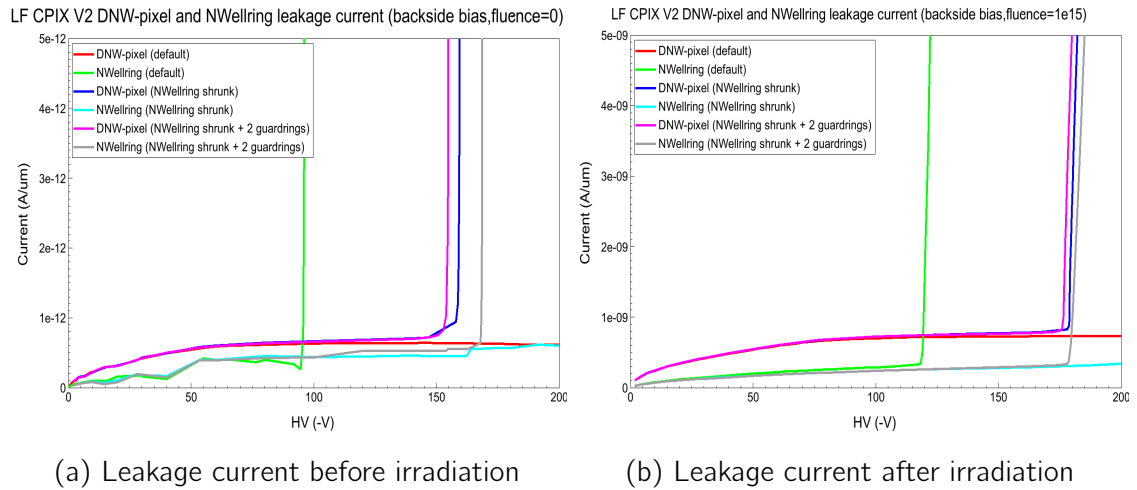
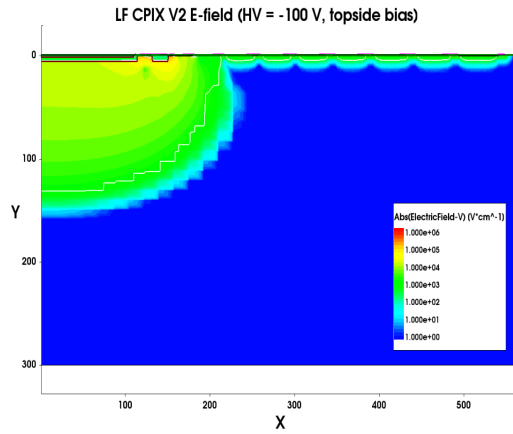
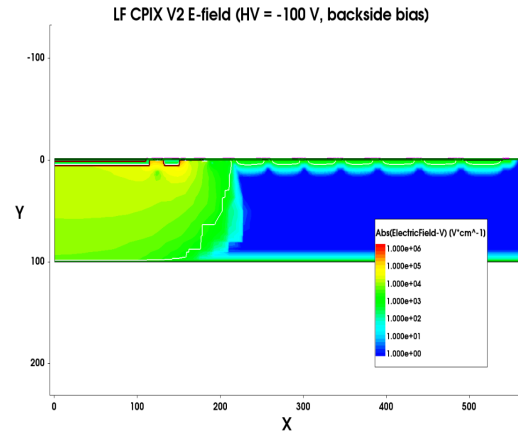


Figure 4.65 – The leakage currents for the DNW-pixel and for the PW-pixel for the backside bias case. (a) : Before irradiation. (b) : After a fluence of $1 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$.

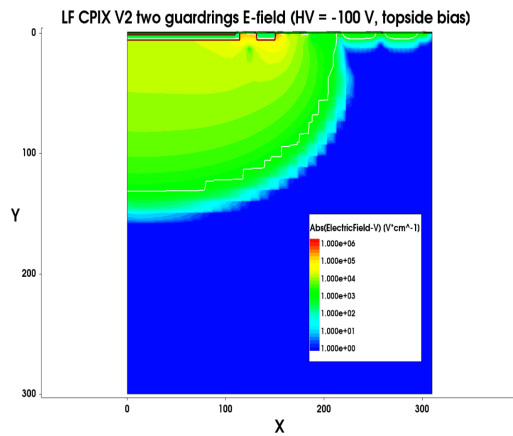


(a) E-field of top-side bias

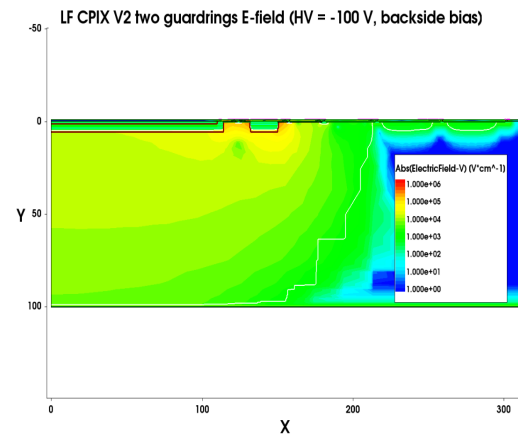


(b) E-field of back-side bias

Figure 4.66 – The electric field distribution of scenario (B) for both top-side and back-side biases.



(a) E-field of top-side bias



(b) E-field of backside bias

Figure 4.67 – The electric field distribution of scenario (C) for both top-side and back-side biases.

100 μm when the high voltage is - 100 V. Eventually the guard-rings of the V2 was designed based on the scenario (C). Two additional floating guard-rings were added in order to leave enough safety region between the depletion area and the cutting edge. Both increased breakdown voltage and improved charge collection efficiency are expected for the V2.

5 HV/HR CMOS detector test setup development and prototypes characterization

As briefly introduced in Chapter 3, the development of HV/HR CMOS sensor is dedicated to the ATLAS Phase-II upgrade, which would potentially be carried out around 2022. Several prototypes in various technologies have been developed and characterized. Much effort has been done in order to improve the detection efficiency and radiation hardness. The typical architecture of HV/HR CMOS sensors is described in details in this chapter. Then, the test setup developed based on DE2 board is also introduced. The sensor characterization results in laboratory test, proton irradiation test and X-ray irradiation test are illustrated in the end of this chapter.

5.1 HV2FEI4 prototype introduction

The first HV CMOS sensor prototype was developed and characterized by the ATLAS HV CMOS collaboration in 2012. This chip was fabricated with AMS 0.18 μm HV technology, and is called AMS V1. Three successive versions with the same technology were developed with some specific modifications in order to improve the radiation hardness and signal to noise ratio (SNR). They are called AMS V2, AMS V3 and AMS V4 respectively in this dissertation. Some characterizations of the AMS prototypes can be found in [105, 106, 107, 108, 109]. In

Table 5.1 – List of HV/HR prototypes

Chip	Technology	Substrate	Comment
AMS V1	AMS 0.18 μm HV	$\sim 15 \Omega \cdot \text{cm}$	characterized
AMS V2	AMS 0.18 μm HV	$\sim 15 \Omega \cdot \text{cm}$	characterized
AMS V3	AMS 0.18 μm HV	$\sim 15 \Omega \cdot \text{cm}$	characterized
AMS V4	AMS 0.18 μm HV	$\sim 15 \Omega \cdot \text{cm}$	characterized
GF	GF BCDlite 130 nm	$\sim 10 \Omega \cdot \text{cm}$	characterized
LF	LF 150 nm	$\sim 2 k\Omega \cdot \text{cm}$	under characterization

parallel, a prototype in GF 130 nm BCDlite [108] technology was also designed in 2013. A first prototype with high resistivity was designed using LF 150 nm technology in 2014, and is being characterized in 2016. Some design and test results can be seen in [110, 111]. A large demonstrator ($1\text{ cm} \times 1\text{ cm}$) that has the same size size as FE-I4 was designed in LF 150 nm technology and submitted in March of 2016. A partial list of prototypes developed by the ATLAS collaboration is given in Table 5.1.

5.1.1 HV/HR CMOS sensor

Here the layout architecture and electronic blocks of the GF prototype is described as an example. The chip size is 3 mm by 3 mm and contains 14×78 pixels in the main matrix. The top level layout is shown in Figure 5.1. The first six triple-column (18 columns) are implemented with cap pixels, which means a serial capacitor is implemented before the connection to the metal plate. As shown

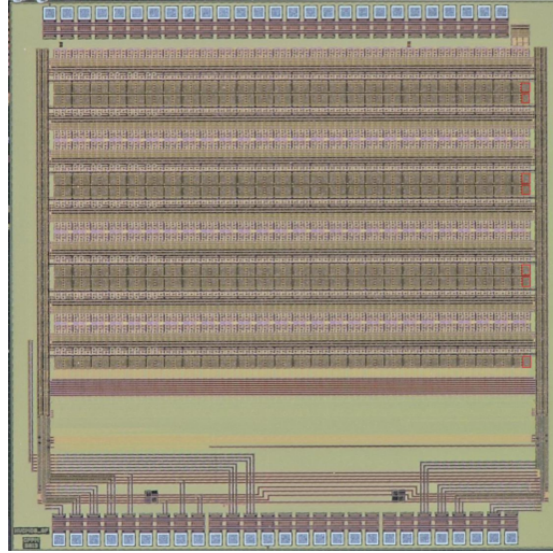


Figure 5.1 – Picture of the layout of GF chip

in Figure 5.2 and 5.3, each pixel in the matrix consists of a charge sensitive preamplifier, a discriminator and a local tuning DAC for the threshold adjustment.

The amplifier stage diagram is shown in Figure 5.2. The charge collecting Deep N-Well (DNW) is biased by the DNW bias cell. The bias DAC VNBias is for the tuning of the resistance value of the biasing resistor. A separate preamplifier power rail vddaPRE is implemented to suppress the noise which would be coming from the main VDDA power line. The bias DAC VN determines the current of the preamplifier. VNLoad is for the polarization of the preamplifier load. Vcasc is used for the polarization of the cascode stage. The VNFB is for the tuning of the

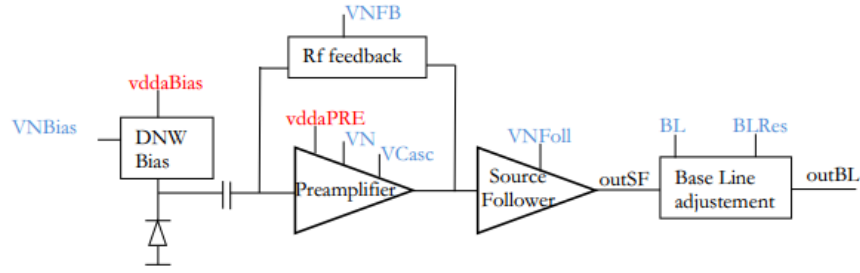


Figure 5.2 – Amplifier stage diagram of matrix pixel

feedback time constant to adjust the signal return to baseline time. The preamplifier is followed by a source follower which is biased by the DAC VNFoll. The base line (BL) voltage, the reference potential for the discriminator, is defined by an external power supply. A BL adjustment is implemented between source follower and discriminator. Its function is to adjust the BL voltage and form a RC filter. The BLRes DAC can tune the resistance of the RC filter.

The discriminator stage is shown in Figure 5.3. The threshold voltage is set

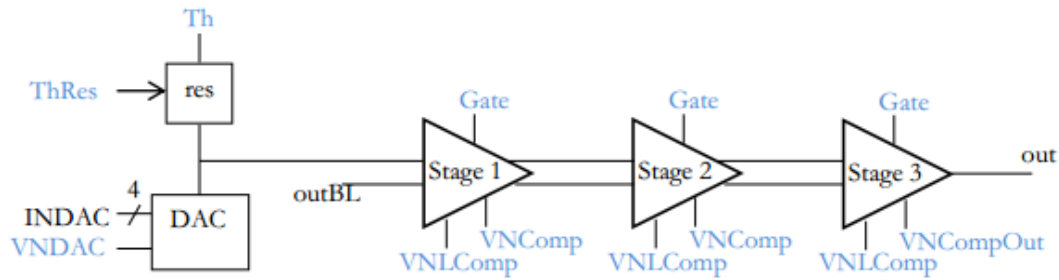


Figure 5.3 – Discriminator stage diagram of matrix pixel

globally by an external polarization “TH” and can be adjusted in each pixel individually by a four-bit DAC, TDAC, inside the pixel. The VNDAC tunes the LSB of the local DAC and ThRes acts as a resistance to allow a fine tuning of the global threshold voltage. To compensate the voltage drop of the diode-connected transistors in the discriminator stage, the gate of these kinds of transistors are polarized typically 200 mV - 300 mV higher than VDDA. The VNCOut0,1 and 3 control the amplitude of the output of discriminator.

The pixels are configured via a shift register which transmits the bias block values, TDAC values and pixel control information to the pixels. The configuration chain is described in Figure 5.4. The bias block consists of 15 six-bit DACs and another test DAC. The function of the DACs are summarized in Table 5.2.

The pixels in matrix are arranged by six-pixel unit cell, as shown in Figure 5.5. Each structure consisting of six sensor pixels with chess box placement is connected to two individual FE-I4 pixels via pixel pads called st and so in Figure 5.5. The

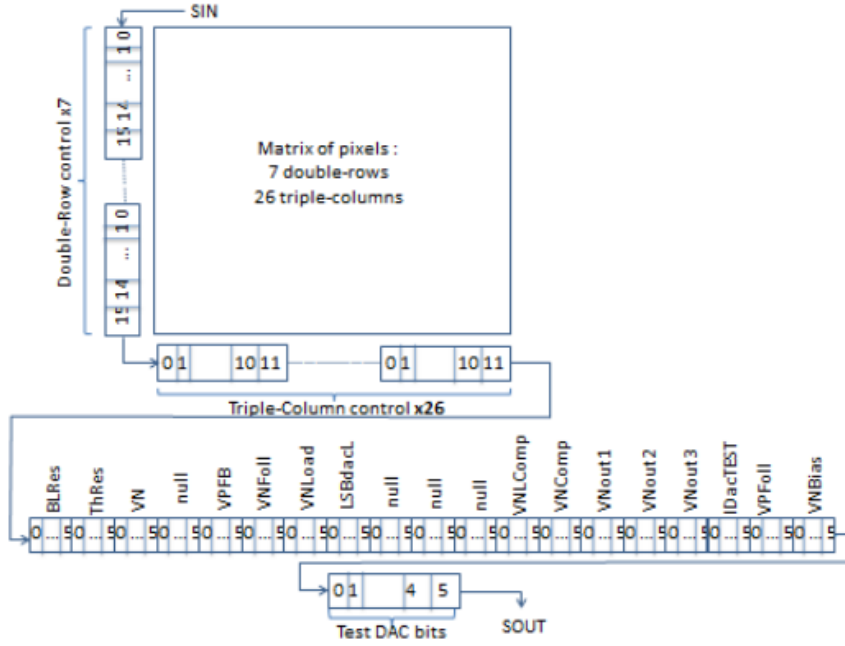


Figure 5.4 – Configuration diagram of the GF prototype

Table 5.2 – Bias block of the GF prototype

DACG	Name	Function	Typical value
1	BLRes	Resistance of the filter	17
2	ThRes	Resistance for the fine tuning of TH	
3	VN	Bias current of preamplifier	23
4	NULL		
5	VNFB	Feedback resistance	6
6	VNFoll	Bias current of source follower	6
7	VNLoad	Bias of the preamplifier load	18
8	VNDAC	LSB of the local DAC	6
9	NULL		
10	NULL		
11	NULL		
12	VNComp	Bias current of the first two stages of discriminator	11
13	VNLComp	Dissymmetry of the discriminator output	6
14	VNCOut0	Output amplitude of pixel 1	30
15	VNCOut1	Output amplitude of pixel 2	30
16	VNCOut2	Output amplitude of pixel 3	30
17	IDACTest		
18	VPFoll		
19	VNBias	Bias current of the DNW biasing cell	

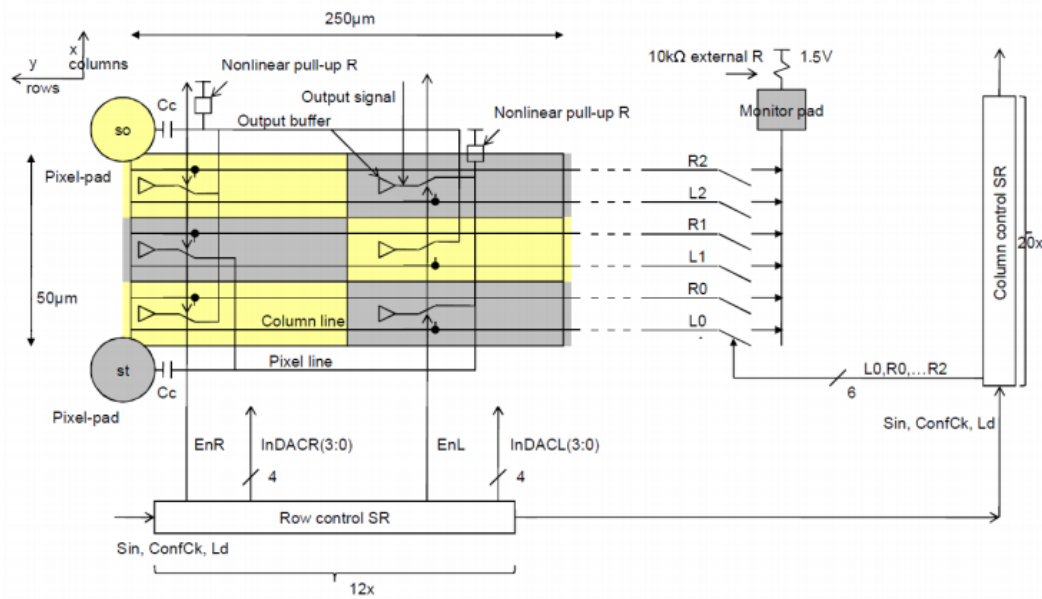


Figure 5.5 – Structure of the six-pixel unit cell of the GF prototype

sensor output that is transmitted to FE-I4 is pulled up by a transistor (acting as a nonlinear resistor). The sensor output can also be monitored via a test pad with a 20 kΩ pull-up resistor. The pixels can also be connected together by column to be used as a pixelated strip chip with output signals PadL and PadR. There are 16 bits for every double-row control and 12 bits for every triple-column control as shown in Figure 5.4. A detailed row and column control unit cell is shown in Figure 5.6.

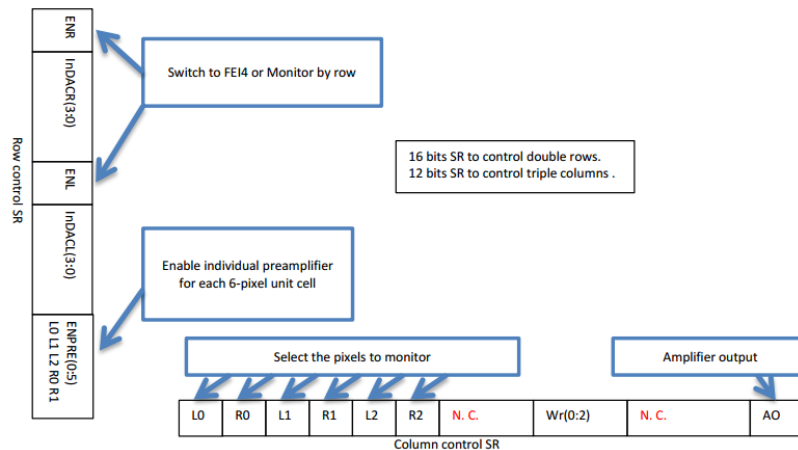


Figure 5.6 – Row and column control bits

In order to investigate the pixel behavior in more details, two special pixels outside of the matrix were designed on the top region of the chip. They are

called "DNW-pixel" and "Alone-pixel". The "Alone-pixel" has the same footprint as the pixels used in the matrix, but contains only the preamplifier part (no discriminator). The "DNW-pixel" also has the same footprint as the pixels used in the matrix, but it is made of a sensor without electronics inside the DNW, together with an additional preamplifier beside the sensor. In addition, six test transistors (three NMOS and three PMOS) with different sizes were designed stand-alone to investigate the transistor radiation hardness.

5.1.2 HV/HR CMOS sensor to FE-I4

The output signal of the HV/HR CMOS sensor can be read out by AC coupling to a specific electronics, as shown in Figure 5.7. At this moment, this sensor is compatible with the IC we have available, the FE-I4. The weighted discriminator

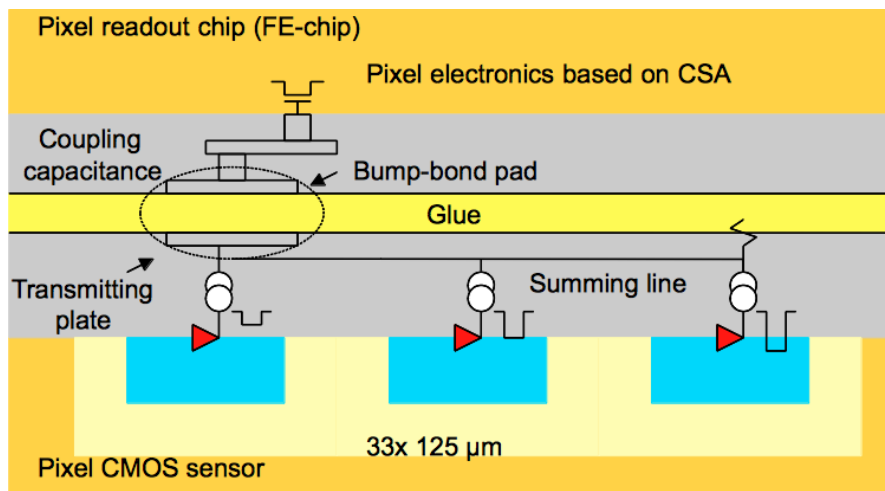


Figure 5.7 – HV CMOS to FE-I4 diagram

signal of the sensor is transmitted to the FE-I4 where the signal height can be encoded with TOT codes, as sketched in Figure 5.8. The three subpixels which are connected to the same FE-I4 pixel can be distinguished by these weighted discriminator signals.

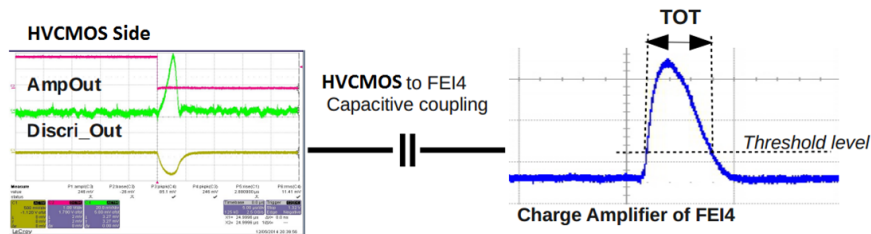


Figure 5.8 – Signal AC coupled to FE-I4

5.1.3 HV2FEI4 test setup based on DE2

To characterize the standalone sensors and the HV2FEI4 prototypes, a test setup was developed based on the Altera DE2 board at CPPM. A typical setup construction to test a standalone sensor in PS proton irradiation is schematized in Figure 5.9.

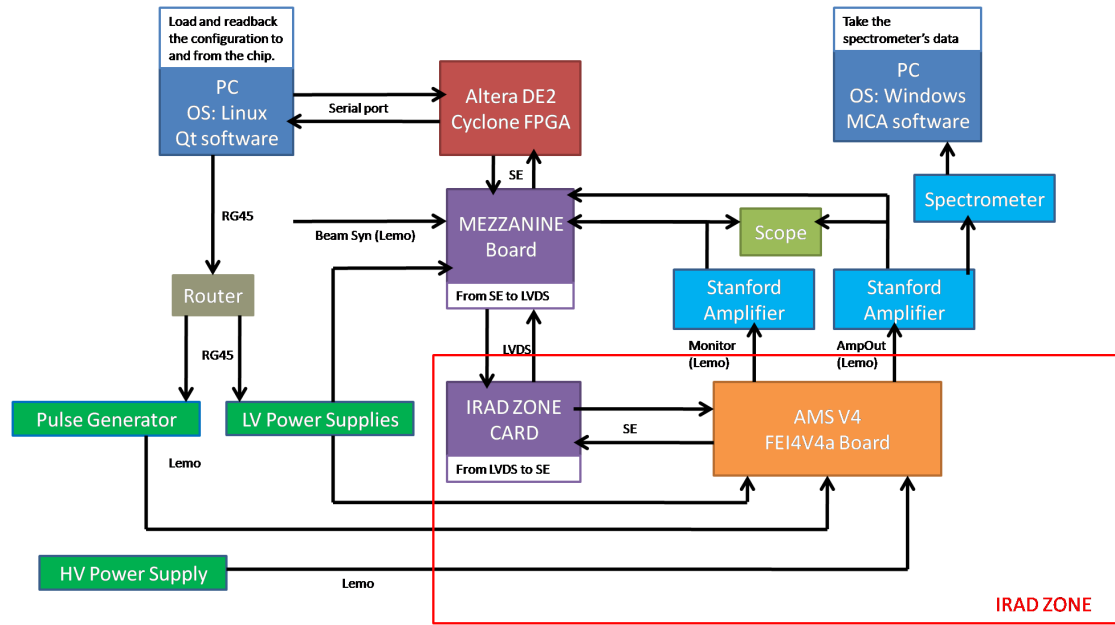


Figure 5.9 – HVCMOS test setup diagram

The firmware and Nios [112] software were developed and implemented into Field-programmable gate array (FPGA) to achieve the functionality of the sensor configuration and readback. A dedicated software written in the Qt [113] framework was developed as GUI for the data loading to the sensor. The DE2 board (in red in Figure 5.9) is followed by a so called MEZZANINE board, which converts the single ended (SE) signal to LVDS in order to suppress the signal distortion experienced with single cable transmission. The MEZZANINE board also receives the Beam Synchronization from the PS trigger system as well as the preamplifier and discriminator signals from the sensor. The MEZZANINE board is then followed by the IRRAD ZONE CARD. The CARD converts the LVDS to SE again, and sends the data to the Device Under Test (DUT) board (in orange in Figure 5.9). The DUT board carries the sensor and only needs to have passive components to avoid the degradation of the components with irradiation.

For the HV2FEI4 setup, an FE-I4 test suite developed within the ATLAS pixel collaboration is merged into the above mentioned setup to control the FEI4 and read the corresponding data out.

5.2 Characterization of HV/HR CMOS sensor prototypes

In this section, the test results of several prototypes for both standalone chips and HV2FEI4 assemblies are discussed. For AMS V1, both laboratory test and PS 24 GeV proton irradiation test were performed. AMS V2 was characterized in both the laboratory and under an X-ray heavy irradiation source. For AMS V3, only laboratory testing was performed at CPPM. AMS V4 was tested in the laboratory and irradiated both in the PS proton beam and with an X-ray source. For GF, the standalone chip was tested at lab and irradiated with X-ray and the HV2FEI4 assemble was investigated at laboratory.

5.2.1 Characterizations of the AMS prototypes

In this section, the test results of several iterations of the AMS prototypes are discussed, focusing on stand-alone characterization.

5.2.1.1 AMS V1 characterization

The AMS V1 chip was the first prototype developed for the ATLAS ITK project. A photograph of the AMS V1 prototype is shown in Figure 5.10. It consists of 60 columns and 24 rows. The pixels between column 3 and 5, called type B, are

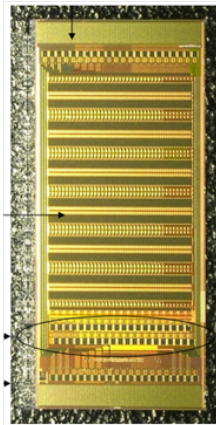


Figure 5.10 – A picture of the AMS V1 prototype

implemented with much simpler electronics than the other pixels in order to reduce the noise and improve the radiation hardness. The remaining pixels in the matrix are called type A. The chip was first characterized before irradiation. Both the preamplifier and discriminator have good response with external test injection, as shown in Figure 5.11. In Figure 5.11, the green pulse is the preamplifier

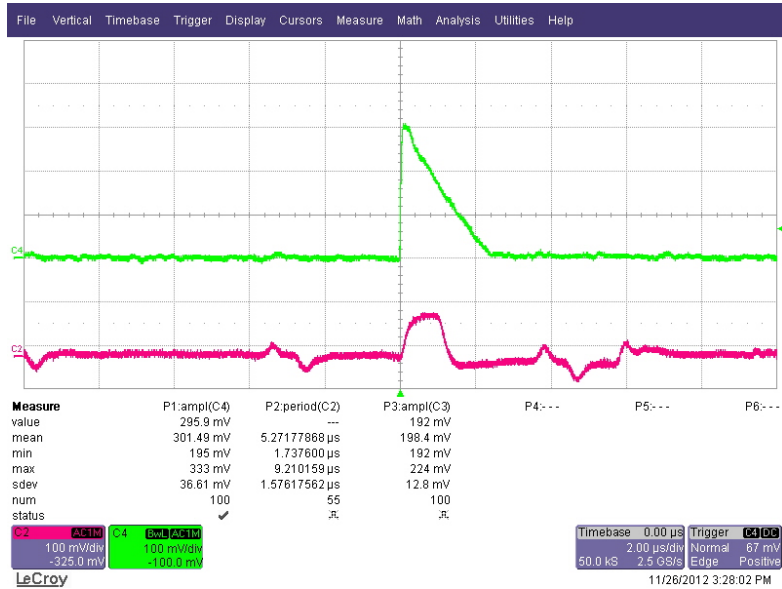


Figure 5.11 – Responses of the preamplifier and discriminator of type A pixel to a 1 V external injection

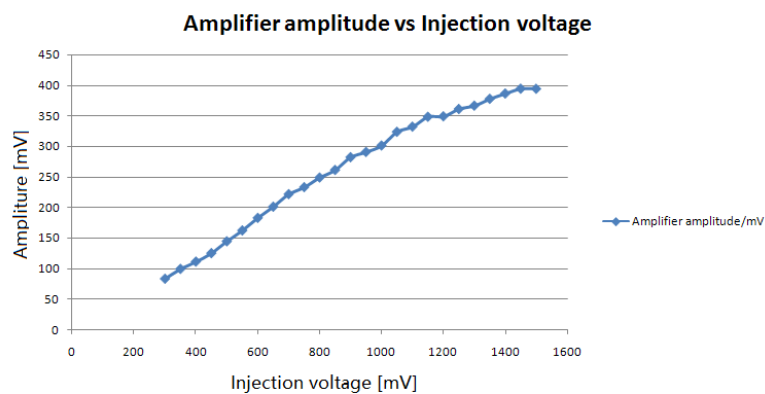


Figure 5.12 – Linearity of preamplifier (type A pixel)

output to 1 V external injection and the pink signal is the corresponding inverted output of the discriminator. The linearity of the preamplifier is also shown in Figure 5.12.

To get the value of the local threshold and local pixel noise, an analog scan was performed for all pixels. The BL voltage, which sets the baseline, and the TH voltage, which sets the global threshold, were set to 0.85 V and 0.90 V respectively. Figure 5.13 shows the threshold and noise map for the full matrix. The

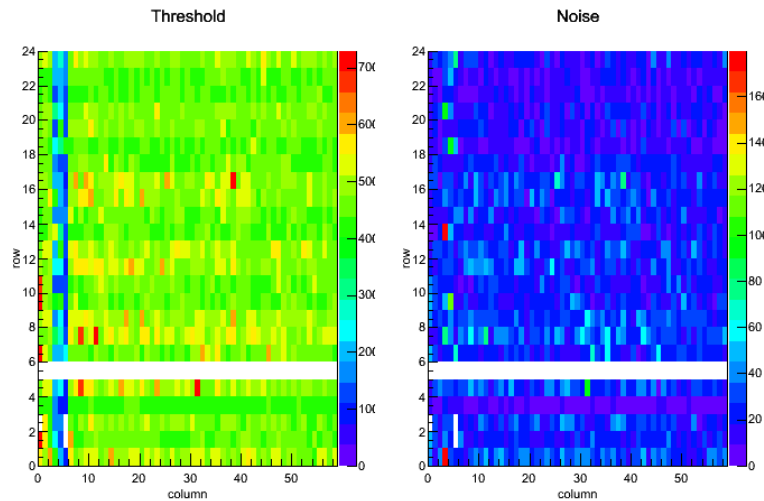


Figure 5.13 – Threshold and noise distributions for the matrix

threshold and noise distributions of type A and type B pixels are shown in Figure 5.14 separately. The type B pixels' threshold is approximately a factor two lower compared with the threshold of the type A pixels, and the noise is higher.

As mentioned in Section 5.1, every double-row of sensor are separately read out via the top metal plate, which are named “Right pixels” and “Left pixels”. The threshold and noise distributions of the “Right pixels” and the “Left pixels” of the type A pixels are shown in Figure 5.15. One can see that the left pixels have lower dispersion, and have lower noise than the right pixels. It is suspected that the higher noise of the “left pixels” is caused by the fact that the readout routes are closer to the capacitive readout pads compared to the “Right pixels”.

To verify the behavior of the chips under radiation, five AMS V1 chips were irradiated with 24 GeV proton beam at CERN PS in two irradiation periods. First, a batch with three chips were irradiated to 435 MRad at room temperature in a first irradiation period. The chips were mounted on a movable table which can be controlled remotely, as sketched in Figure 5.16. The three chips were numbered CCPD2, CCPD4 and CCPD5. Two chips were unresponsive after the installation, and only CCPD2 can be configured and monitored. In practice, the assemblies were moved to the beam center during irradiation and moved to a so-called park position, 10 cm away from the beam center, for measurements at each planned

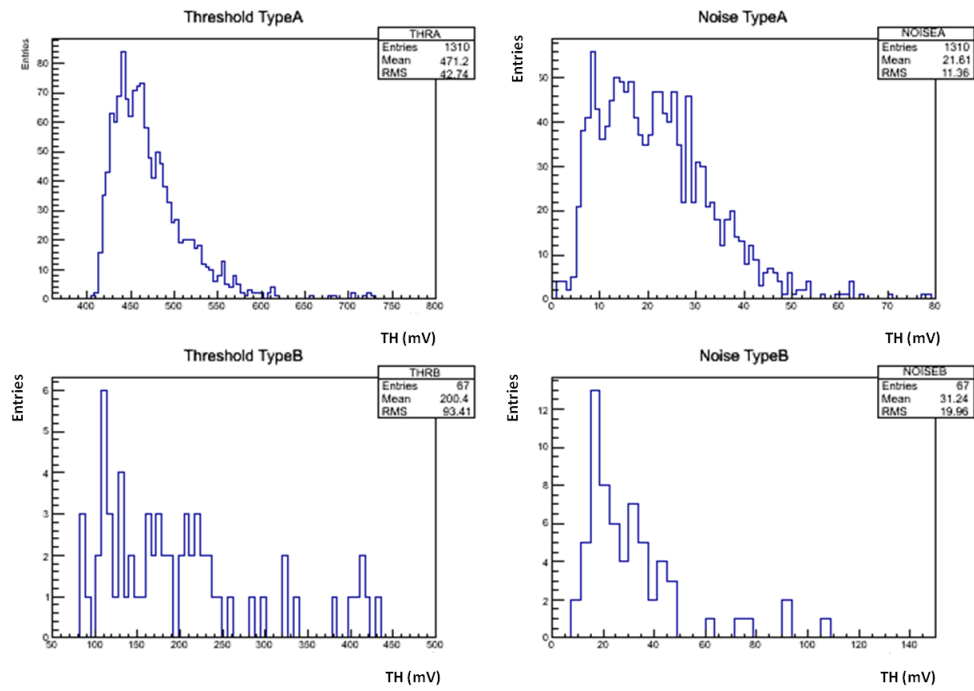


Figure 5.14 – Threshold and noise distributions of the type A and the type B pixels.

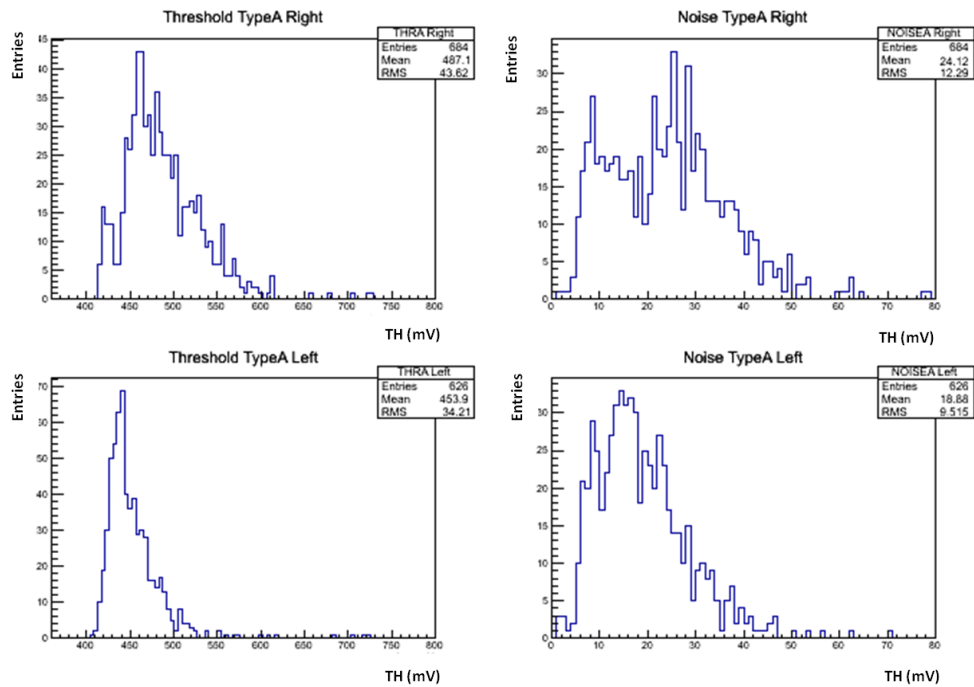


Figure 5.15 – Threshold and noise distributions of the "right" and "left" pixels

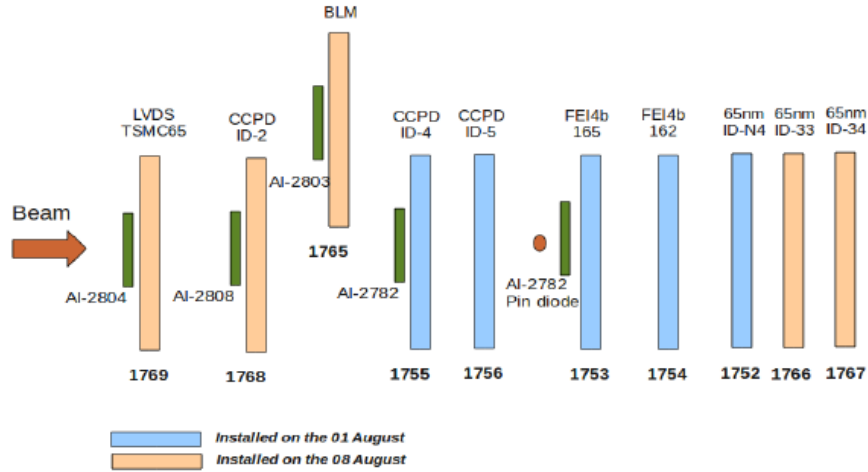


Figure 5.16 – Location map of the assemblies

dose level. The discriminator was unresponsive at 0.5 MRads. The preamplifier counting rate for the proton beam halo in the park position was explored at each irradiation step, which reflects the sensor detection capability for the charged particles. It was the first time that we studied this kind of prototype. The counting rate was not recorded at the beginning and was measured only after 100 MRads. The gain of the preamplifier can be changed by a 6-bit tuning DAC in the chip. This tuning DAC can adjust the resistance of the load transistor in the output stage of the preamplifier, and two sets of tuning were chosen : low gain and high modes. The preamplifier started to malfunction at 160 MRads in the high gain mode, but it was responsive up to 435 MRads in the low gain mode, as shown in Figure 5.17. In high gain mode, both the reduced amplitude of the preamplifier and the damage to the sensor bulk led to the decrease in the counting rate. The large fluctuations that can be seen in Figure 5.17 were due to the few days annealing which was performed in order to partially recover the sensor in high gain mode. In low gain mode, the amplitude of the preamplifier was high enough for the counting rate measurement, and the reduced counting rate was mainly caused by the bulk damages.

After three weeks room temperature annealing, both the preamplifier and discriminator signals could be measured again with some specific tuning, as shown in Figure 5.18.

After this first irradiation period, two new chips, numbered CCPD8 and CCPD9, were mounted on the table. The CCPD8 and CCPD9 were irradiated at -8°C to approximately 86 MRads. The preamplifier and discriminator were unresponsive quite early (440 kRads and 550 kRads for each sample respectively) and could not be recovered by tuning the corresponding bias DACs. After 550 kRads TID and 24 hours 28°C annealing, the preamplifier was responsive with degraded

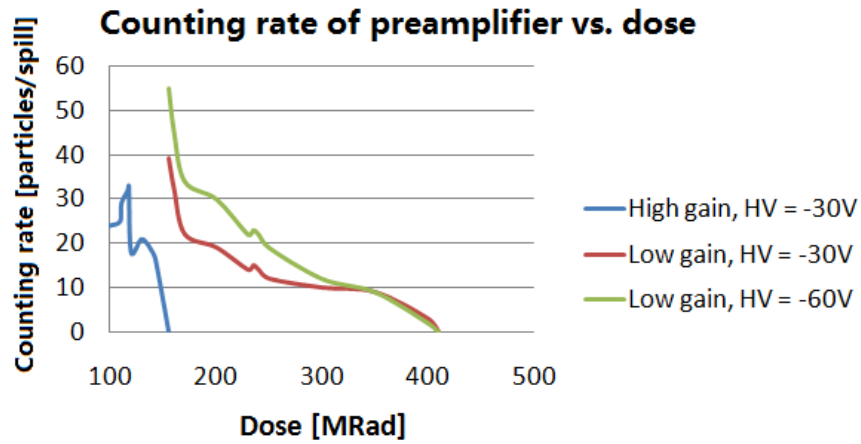


Figure 5.17 – The counting rate of preamplifier of AMS V1 as a function of the dose. The counting of one PS spill was measured in the so-called park position (10 cm away from the beam center).

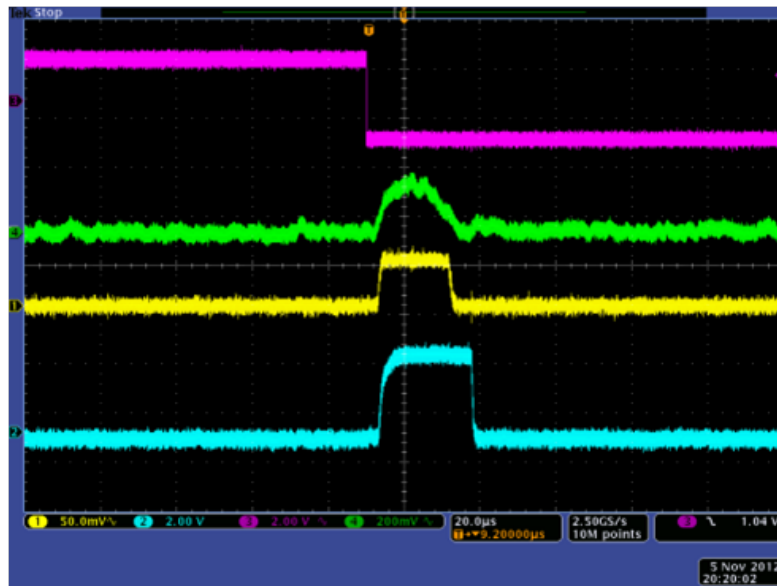
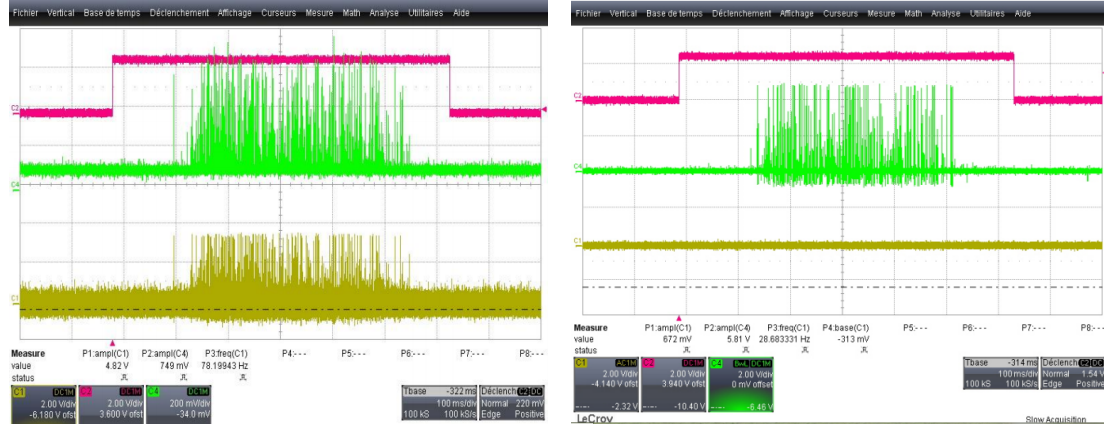


Figure 5.18 – CCPD2 responses for external injection after 3 weeks annealing. Pink : injection pules. Green : the response of the preamplifier. Yellow : the response of the discriminator. Blue : the response of the discriminator after a comparator board.

amplitude, but the discriminator had still no output signal. The preamplifier and discriminator responses of CCPD9 in one PS spill at 0 MRad and 70 MRads are shown in Figure 5.19a and 5.19b. After 86 MRads, the preamplifiers for both chips were still responsive and had counting from the PS beam halo.



(a) The preamplifier and discriminator signals in one PS spill (0 MRad) (b) The preamplifier and discriminator signals in one PS spill (70 MRad)

Figure 5.19 – The snapshots of the preamplifier and discriminator responses in one PS spill. Preamplifier is in green and discriminator is in yellow. The data acquisition gate is shown in red. (a) : Preamplifier and discriminator responses at 0 MRad. (b) : Preamplifier and discriminator responses at 70 MRad.

5.2.1.2 AMS V2 characterization

The AMS V1 prototype was designed with standard linear transistors with no consideration concerning its capability to cope with high radiation dose. According to the characterizations of AMS V1, some specific modifications were carried out to the design of the AMS V2 prototype in order to improve its radiation hardness, for instance the implementation of Enclosed Layout Transistors (ELTs). A snapshot of the layout of V2 is shown in Figure 5.20. As shown in Figure 5.20, the preamplifiers of the pixels in the first four triple-columns were made entirely of ELTs, and are called rad-hard pixels. The middle 12 triple-columns are the so called normal pixels, which means ELTs were used for the critical regions in the preamplifier and the remaining transistors were implemented with linear type. The pixels in the last 4 triple-columns were similar to the type B pixels of AMS V1 with no usage of the ELTs ; they are called simple pixels.

In order to verify the ionizing damage in the oxide and the oxide-silicon interface, the chip was irradiated with 10 keV X-ray source to 862 MRads at CERN. The dose rate was set to 103 kRad/min. Two kinds of pixels, normal and rad-hard, were monitored to investigate the TID effect. The electronics of normal

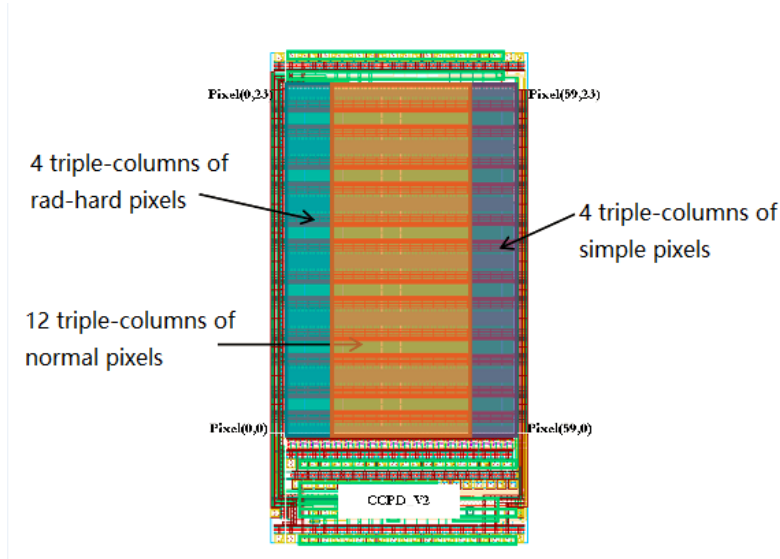


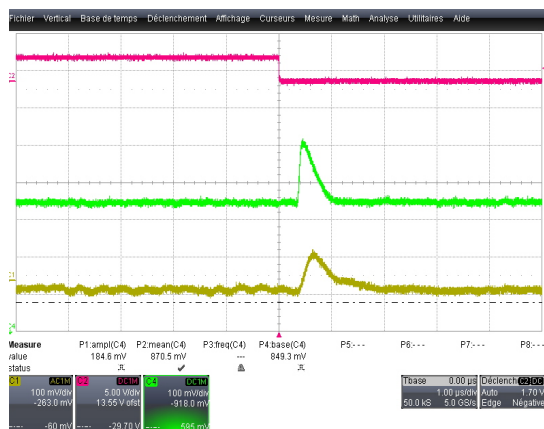
Figure 5.20 – The layout of AMS V2

pixel was designed with linear transistors, and the rad-hard pixel means that some ELT transistors were implemented in the preamplifier. It could be shown in preliminary test that both two kinds of pixels were behaving correctly before irradiation. The preamplifier and discriminator responses (before irradiation) of a rad-hard pixel to an external 1 V test injection and to a ^{90}Sr source are shown in Figure 5.21a and 5.21b. In the same way, the responses of a normal pixel are shown in Figure 5.22a and 5.22b.

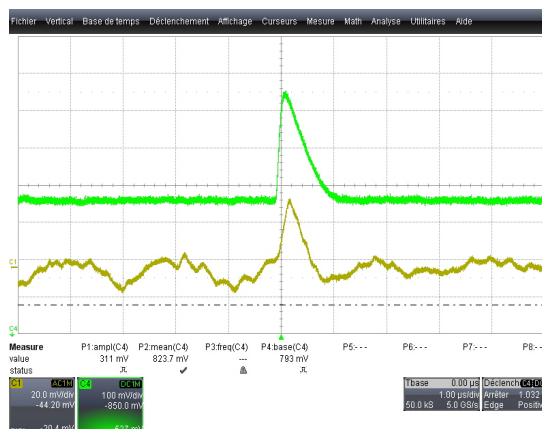
At each irradiation step, the amplitudes of rad-hard and normal pixels' preamplifier were measured. The amplitude decreases with increasing dose level but is still responsive at 862 MRads, as shown in Figure 5.23. Compared with the proton test of AMS V1, the electronics of AMS V2 is more radiation hard. To recover the output of the preamplifier, two hours of 70 °C annealing was performed at each irradiation step. The amplitudes of the normal pixel and the rad-hard pixel reduce to 11% and 28% after 862 MRads compared with their initial amplitudes. The amplitudes can be recovered to 50% and 90% of their initial values by tuning the corresponding bias currents. The rad-hard pixel show better radiation hardness as expected.

The threshold scans of these two pixels were performed by using external test injections in order to measure the threshold and noise variations, as shown in Figure 5.24. One hundred test pulses were applied to the pixel at each scan step via a test capacitor, as shown in Figure 3.25. The threshold and noise can be extracted by fitting the scan curves with the error function,

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^{\frac{x-n}{\sigma}} e^{-t^2} dt \quad (5.1)$$

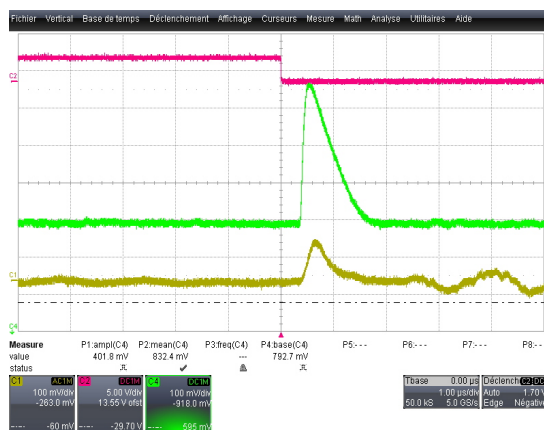


(a) 1V injection responses

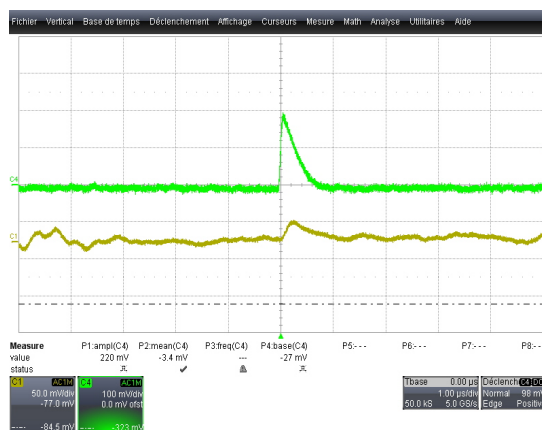


(b) ^{90}Sr responses

Figure 5.21 – The responses of the preamplifier and discriminator for the rad-hard pixel. The preamplifier output signal is in green and the inverted discriminator output signal is in yellow. (a) : 1V injection responses of rad-hard pixel before irradiation. (b) : ^{90}Sr responses of rad-hard pixel before irradiation.



(a) 1V injection responses



(b) ^{90}Sr responses

Figure 5.22 – The responses of the preamplifier and discriminator for the normal pixel. The preamplifier output signal is in green and the inverted discriminator output signal is in yellow. (a) : 1V injection responses of normal pixel before irradiation. (b) : ^{90}Sr responses of normal pixel before irradiation.

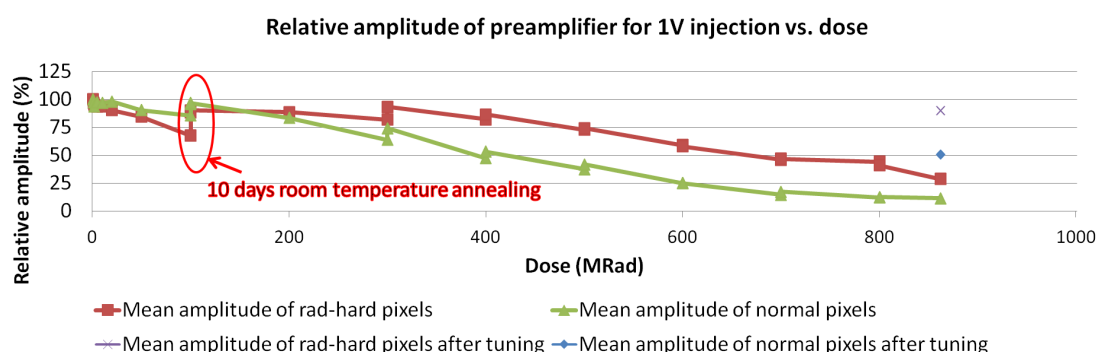


Figure 5.23 – The amplitude of the preamplifier of AMS V2 as a function of the dose for two different pixels types. A 10 days room temperature annealing was carried out due to a suspension of the X-ray source at 100 MRads. Then the chip was irradiated to 862 MRads.

where x is the recorded hits at each scan step, n is the threshold and σ is the noise. By comparing the Figure 5.24a to 5.24b, one can see that the ELT pixel kept a rather stable noise level.

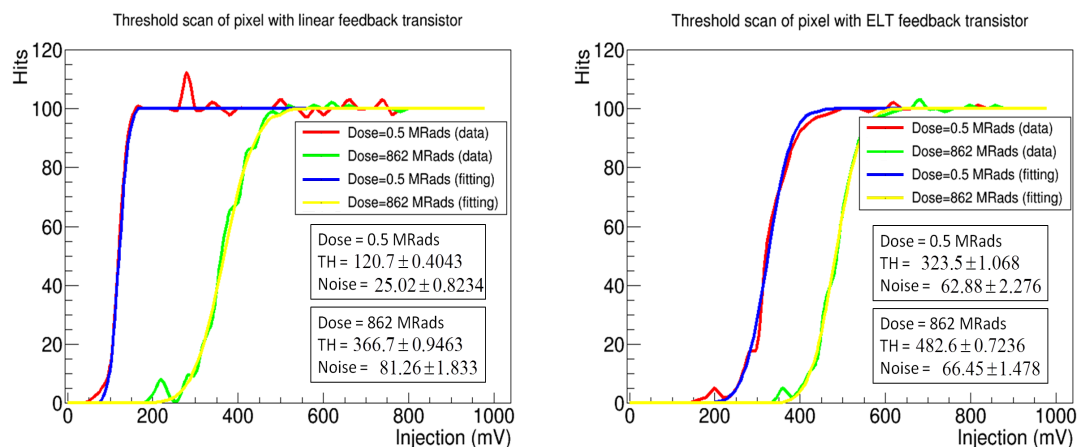
The leakage current between the DNW and the substrate was also measured after each dose step, as shown in Figure 5.25. After each dose step, a two hours high temperature annealing was applied (accelerated annealing procedure). The leakage current decreased strongly after each 70°C annealing procedure. This is because the high temperature enhances the interface traps recovery. Before irradiation, the leakage current is ~ 1 nA and it increases to ~ 590 nA at 862 MRads after the last two hours 70°C annealing step. The increased leakage current after the highest dose could be coped with by the preamplifier but it would increase the noise.

5.2.1.3 AMS V3 characterization

The AMS V3 prototype was implemented with three kinds of pixels. The matrix consists of two triple-columns made of “ATLAS-standard” pixels, two quadruple-columns made of “new type” pixels and 64 columns of “CLIC” (Compact Linear Collider) pixels, as shown in Figure 5.26.

The “ATLAS-standard” pixels have the same electronics architecture as AMS V2 normal pixels. The preamplifier are made entirely of ELTs and linear long feedback transistor for higher gain and lower noise. The “new type” of pixels are implemented with separated electronics and charge collection diode, and the sub-pixel size is then reduced to $25\ \mu\text{m} \times 125\ \mu\text{m}$. The “CLIC” type pixels are dedicated to the CLIC experiment with a compact preamplifier structures and no discriminator in the pixel; the pixel size is $25\ \mu\text{m} \times 25\ \mu\text{m}$.

Laboratory test has been performed at CPPM for AMS V3. “ATLAS-standard” and “CLIC” pixels were tested. The linearity of both two kinds of pixels was mea-



(a) Threshold scan of pixel with linear feed- (b) TH scan of pixel with ELT feedback transistor

Figure 5.24 – The data were fitted with error function to extract the threshold and noise for each pixel. (a) The threshold of pixel with linear feedback transistor changed from 121 mV to 367 mV, and the noise increased from 25 mV to 81 mV. (b) The threshold of pixel with ELT feedback transistor changed from 324 mV to 483 mV, and the noise increased from 63 mV to 66 mV.

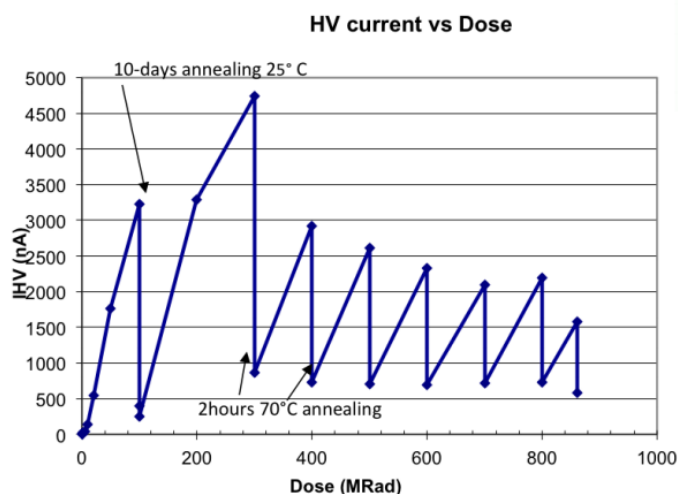


Figure 5.25 – The leakage current as a function of dose

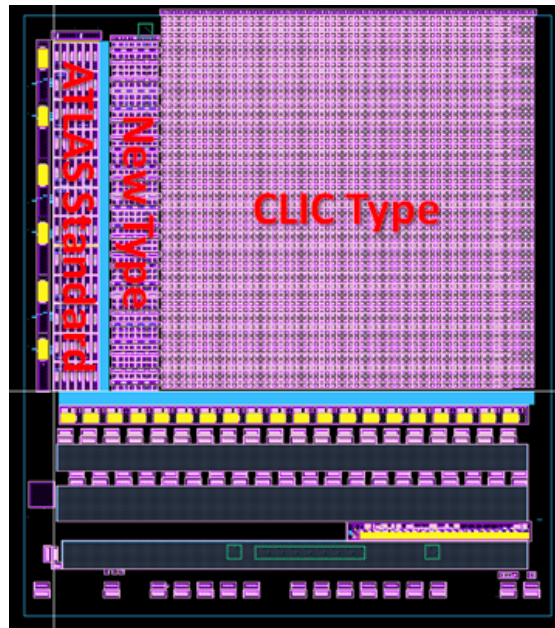


Figure 5.26 – The layout of AMS V3

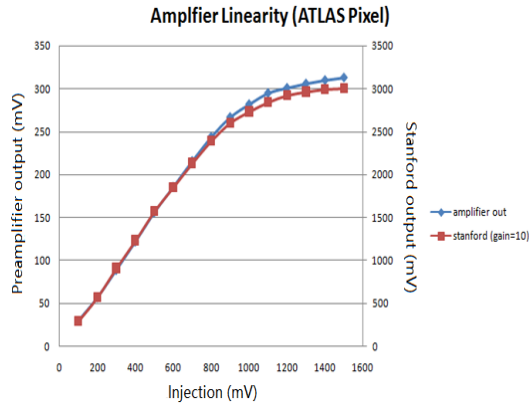
sured with external injection, as shown in Figure 5.27a and 5.27b. The preamplifier of the ATLAS pixels saturates when the injection voltage reaches over ~ 800 mV. The linearity of CLIC pixels is quite good up to 1.5 V.

The ^{55}Fe and ^{90}Sr source responses of ATLAS pixel are shown in Figure 5.28a and 5.28b, and the corresponding spectra acquired using a spectrometer are shown in Figure 5.29a and 5.29b.

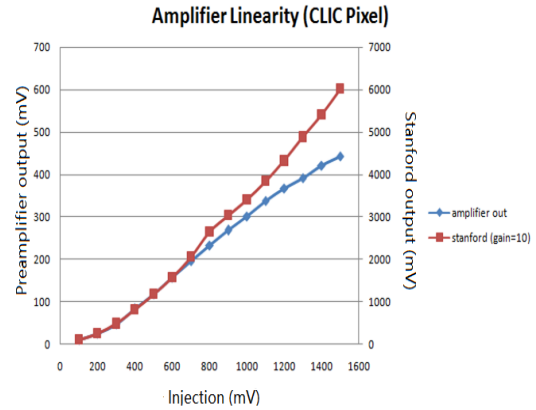
The ENC of the “ATLAS-standard” pixel is ~ 70 electrons. The K-alpha peak of ^{55}Fe was observed but the K-beta peak was concealed due to the relatively high noise. The high noise source was identified ; it derives from one of the ELT of the preamplifier, which in consequence has been modified in the next version of the chip. For the ^{90}Sr detection, it is difficult to separate the landau peak from the background.

The ^{55}Fe and ^{90}Sr responses of the “CLIC” pixel are shown in Figure 5.30a and 5.30b, and the corresponding spectra acquired using a spectrometer are shown in Figure 5.31a and 5.31b.

The ENC of the “CLIC” pixel is only ~ 35 electrons, due in part to the smaller pixel size and in part to the simpler implemented electronics. Thanks to this low noise, the two ^{55}Fe peaks are now separated. A bump with energy around 1900 electrons was observed in the ^{90}Sr spectrum and the value of the bump peak was independent of the substrate bias voltage. This bump comes from the non MIP-like particles and would be removed with a scintillator trigger.

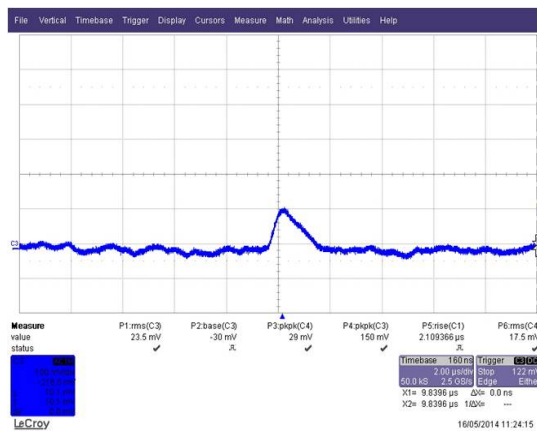


(a) Linearity of ATLAS type pixel

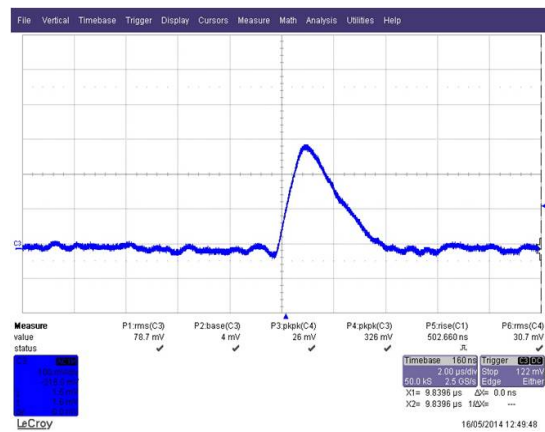


(b) Linearity of CLIC type pixel

Figure 5.27 – The amplitudes of the preamplifiers as a function of injection voltages. (a) : Response of the “ATLAS-standard” pixel. (b) : Response of the “CLIC” pixel.

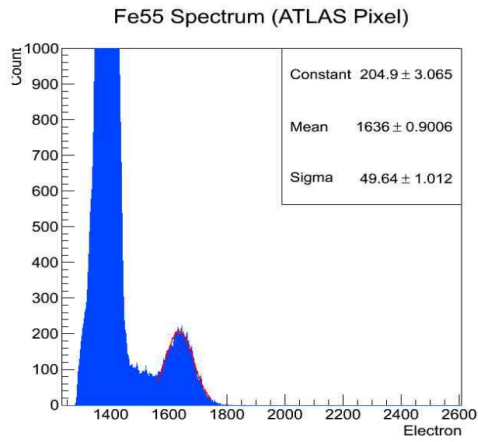


(a) ^{55}Fe signal

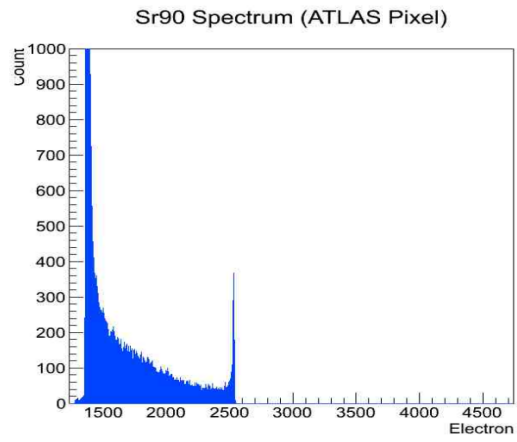


(b) ^{90}Sr signal

Figure 5.28 – ^{55}Fe and ^{90}Sr signals detected by the “ATLAS-standard” pixel.

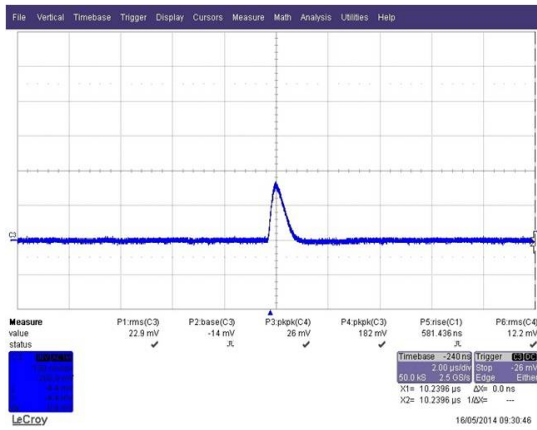


(a) ^{55}Fe spectrum

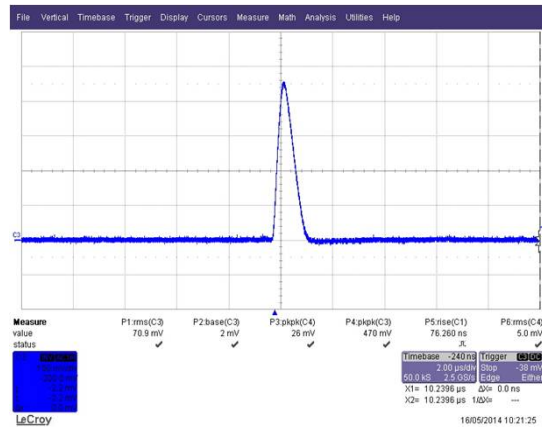


(b) ^{90}Sr spectrum

Figure 5.29 – ^{55}Fe and ^{90}Sr spectra of the “ATLAS-standard” pixel.



(a) ^{55}Fe signal



(b) ^{90}Sr signal

Figure 5.30 – ^{55}Fe and ^{90}Sr signals detected by the “CLIC” pixel.

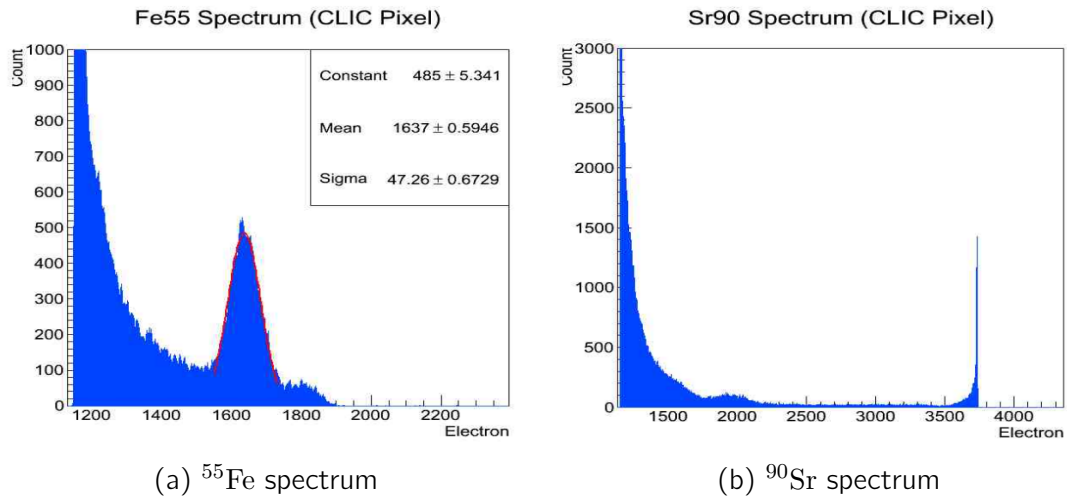


Figure 5.31 – ^{55}Fe and ^{90}Sr spectra of the “CLIC” pixel.

5.2.1.4 AMS V4 characterization

Some modifications were brought to the AMS V3 prototype to improve the SNR and its radiation hardness resulting in a new chip version : AMS V4. This chip was also made of three kinds of pixels as was the case for the AMS V3, as shown in Figure 5.32 : “CLIC”, “new type” and “ATLAS-standard” pixels.

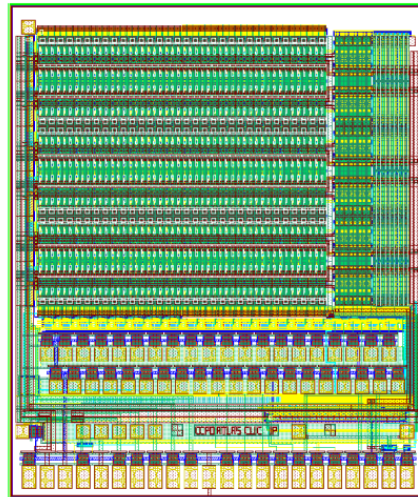


Figure 5.32 – The layout of AMS V4

Three pixel flavors were implemented for the “ATLAS-standard” pixels. The first pixel flavor was designed with an ELT feedback and the second pixel flavor with a linear feedback transistor. The third pixel flavor was also designed with a linear feedback transistor but with a time encoding discriminator. The discriminators for the first and the second pixel flavors were amplitude encoding.

The “ATLAS-satandard” pixels with linear feedback transistor and amplitude encoding discriminator were characterized before irradiation. The ENC of the preamplifier is ~ 25 electrons. Both the preamplifier and the discriminator behaved correctly and their responses to an external 1 V injection are shown in Figure 5.33a. The output signals from the preamplifier to ^{55}Fe and ^{90}Sr sources are also shown in Figure 5.33b.

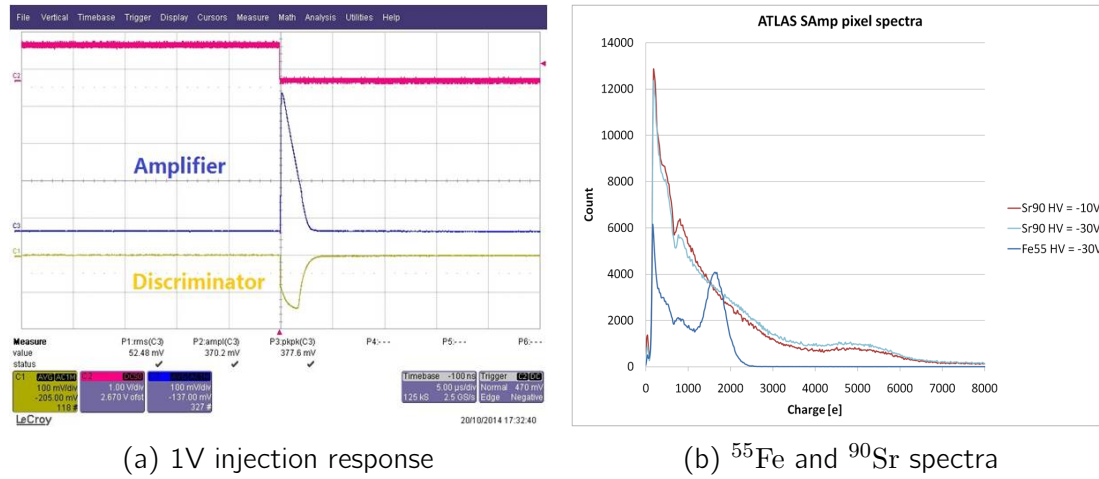
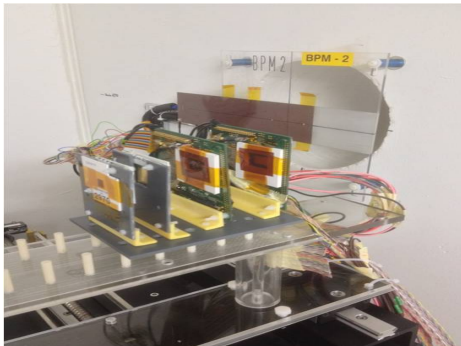


Figure 5.33 – Responses of the “ATLAS-standard” pixels with linear feedback transistor and amplitude encoding discriminator.

In order to verify the radiation hardness of AMS V4 for both NIEL and TID effects, the AMS V4 prototypes were irradiated with PS 24 GeV protons and X-ray source (110 kRad/min) at CERN in December 2014. Four samples, two AMS V4 chips and two TSMC 65 nm chips, were installed on the table in the irradiation zone, as shown in Figure 5.34a. The samples were controlled by the PCs in the control room via 20 m flat cable and lemo cables. Fig 5.34b shows the test setup installed in the PS control room.

The samples were irradiated to 560 MRads with 24 GeV protons. One “ATLAS-standard” pixel with ELT feedback transistor and one “ATLAS-standard” pixel with linear feedback transistor were monitored during the proton irradiation. The preamplifier and discriminator responses of the pixel with linear feedback transistor (between 4.75 MRads and 4.9 MRads) to one PS spill in the beam position is shown in Figure 5.35. The electronics was responsive for the external 1.2 V test injections after 560 MRads depicted a predicted degradation as shown in Figure 5.36a. The counting rate of particles for the sensor was also studied by using the same method as discussed in Chapter 5.2.1.1. The decreased counting rates shown in Figure 5.36b reveal that the depleted region was reduced at high irradiation dose.

The chip was also irradiated to 1 GRad by using a ~ 10 keV X-ray source. The current consumption variations before and after irradiation are listed in



(a) Samples mounted on the irradiation table (b) AMS V4 test setup in control room

Figure 5.34 – Proton irradiation test setups for the AMS V4. (a) : Samples on the irradiation table. (b) : Instruments in the control room.

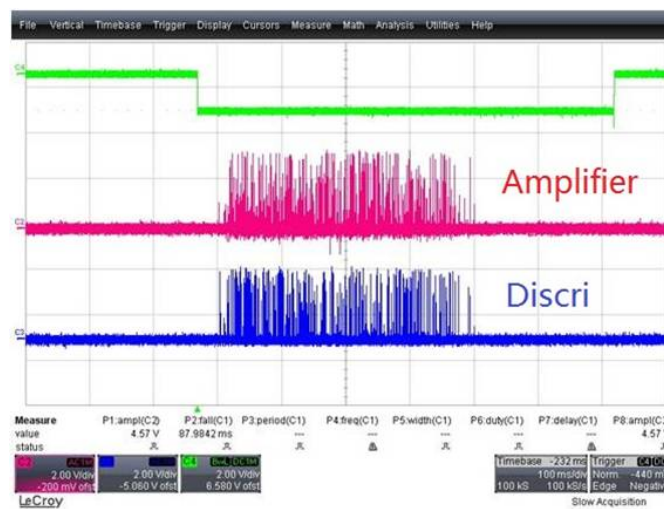
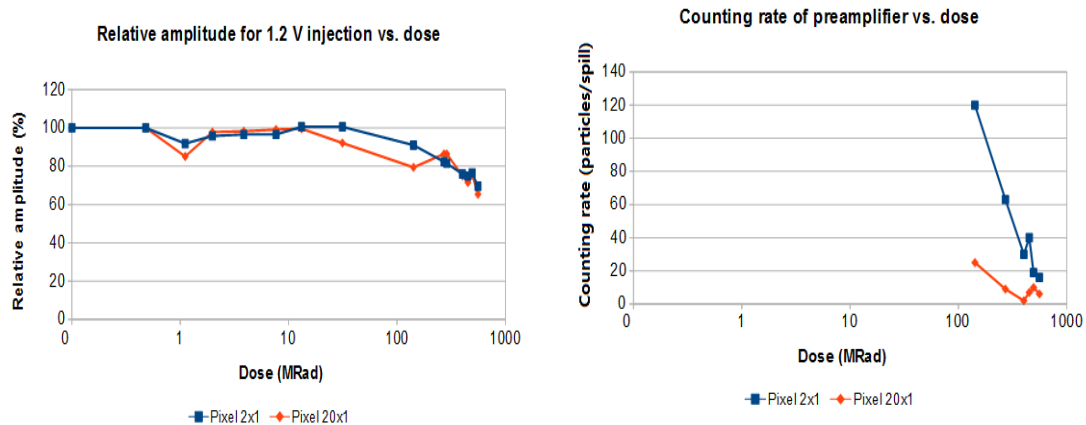


Figure 5.35 – Screenshot of preamplifier and discriminator responses in beam position



(a) The amplitude as a function of the dose (b) The counting rate as a function of the dose

Figure 5.36 – The response of the preamplifier was monitored during the proton irradiation to 560 MRads (HV = -60 V). (a) The amplitudes were measured by applying the external 1.2 V test pulses to the preamplifier. The amplitudes of pixels with linear feedback and ELT transistors lost 27% and 25% respectively compared with initial values. (b) The counting rates were not measured at the beginning of the irradiation due to a malfunction of our test setup. They were begun to be investigated after 110 MRads and exhibited a strong decrease due to the bulk damages after proton irradiation.

Table 5.3. Two different pixels were monitored during irradiation : pixel 2x1

	Voltage [V]	Current at 0 MRad (mA)	Current at 1 GRad (mA)
Idda	1.8	12	7
Issa	1.5	3	1
Iddd	1.8	1	0
Ihv	-60	0	0.001

and pixel 20x1. The pixel 2x1 was implemented with a linear feedback transistor and the pixel 20x1 with an ELT. The preamplifiers of both pixels were responsive after 1 GRad. By tuning the corresponding DACs, the amplitude of pixel 2x1 and pixel 20x1 can be recovered to 90% and 60% respectively, as shown in Figure 5.37. The amplitudes were normalized to the values before irradiation.

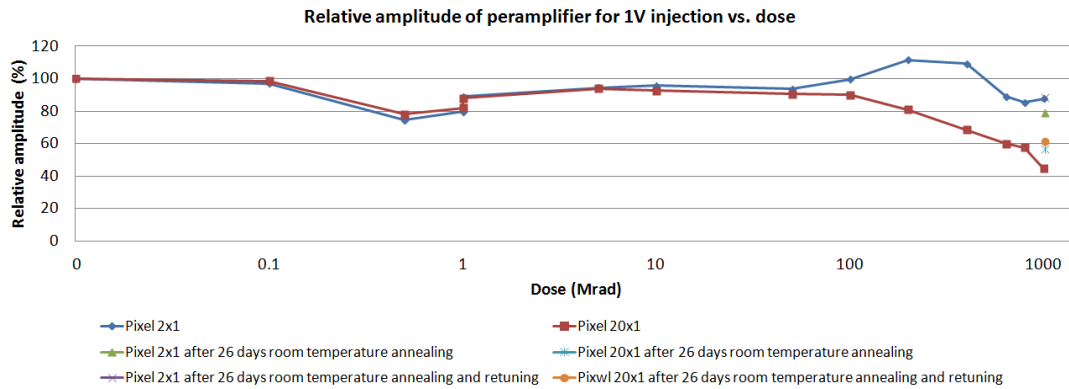
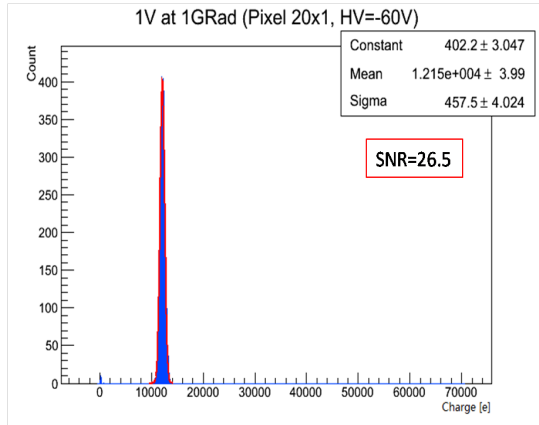


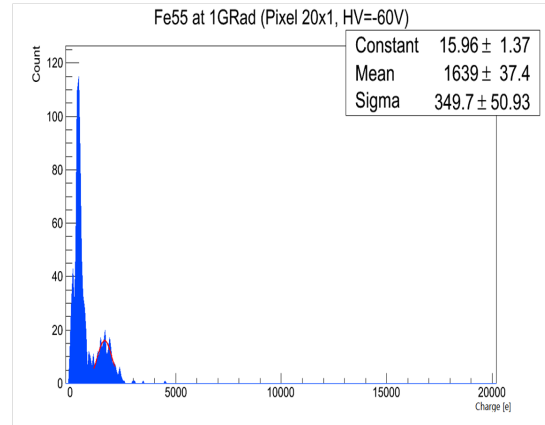
Figure 5.37 – The amplitude of the preamplifiers of AMS V4 as a function of the dose. The results after 26 days room temperature annealing and tuning were also included at 1 GRad in the plot.

The pixel 2x1 became quite noisy after 200 MRads, and the signals of ^{55}Fe and ^{90}Sr were submerged in the background. The pixel 20x1 kept a very low and stable noise level, and the SNR (signal-to-noise ratio) was reduced from 60.3 to 27.5 after 1 GRad irradiation. The 1 V injection spectrum is shown in Figure 5.38a. Therefore, both the ^{55}Fe and ^{90}Sr spectra can be obtained for pixel 20x1 thanks to the lower noise, even with lower preamplifier amplitude, as shown in Figure 5.38b and 5.39b. The MPV measured is of 1426 ± 29 electrons. The ^{90}Sr response at 1 GRads of preamplifier and discriminator taken by oscilloscope is shown in Figure 5.39a. It is the first time that both ^{55}Fe and ^{90}Sr spectra were observed at 1 GRad X ray irradiation for the AMS HV CMOS prototype.

Some modifications of the pixel guard-rings have been made for the AMS V4 to reduce the leakage current. The leakage current as a function of HV is plotted for two different doses in Figure 5.40a. The leakage current recorded as a function

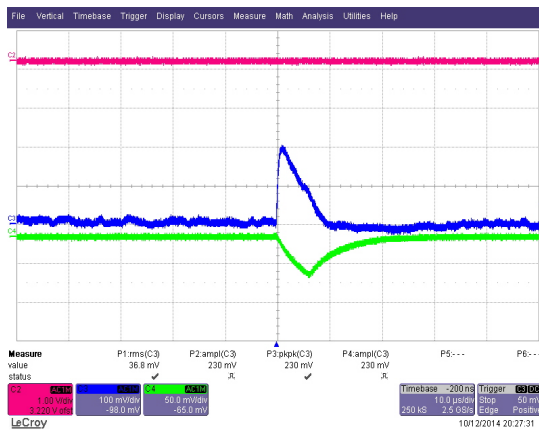


(a) 1 V injection spectrum

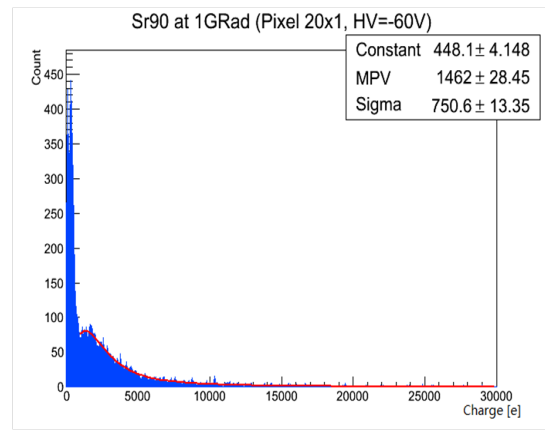


(b) ^{55}Fe spectrum

Figure 5.38 – The 1 V injection and ^{55}Fe spectra taken by the pixel with ELT feedback transistor after 1 GRad X-ray irradiation.



(a) Screenshot of ^{90}Sr response



(b) ^{90}Sr spectrum

Figure 5.39 – (a) : the ^{90}Sr source response. The preamplifier signal is in blue and the discriminator output signal is in green. (b) : the spectrum of ^{90}Sr .

of the dose is shown in Figure 5.40b. The current saturated after ~ 800 MRads and has reduced to about 380 nA after 26 days room temperature annealing. After 1 GRad, the average leakage current per pixel is 1.54 nA (without 70°C annealing during the whole irradiation period). This should be compared to the leakage current per pixel recorded for the AMS V2, which was 1.53 nA at 862 MRads, but for which two hours 70°C annealing was applied at each irradiation step.

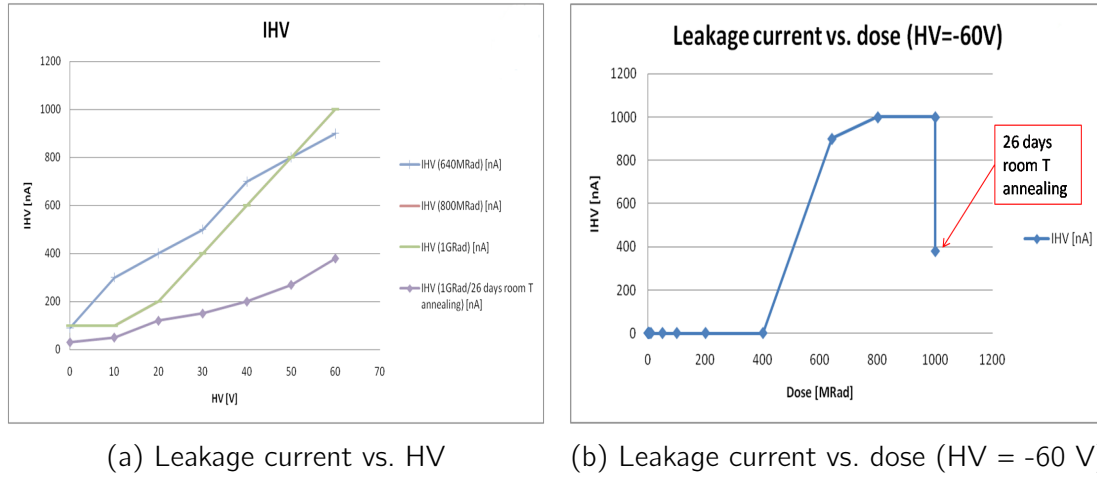


Figure 5.40 – (a) : Leakage current as function of HV depending on dose. (b) : Leakage current as a function of dose when the HV voltage value is -60 V.

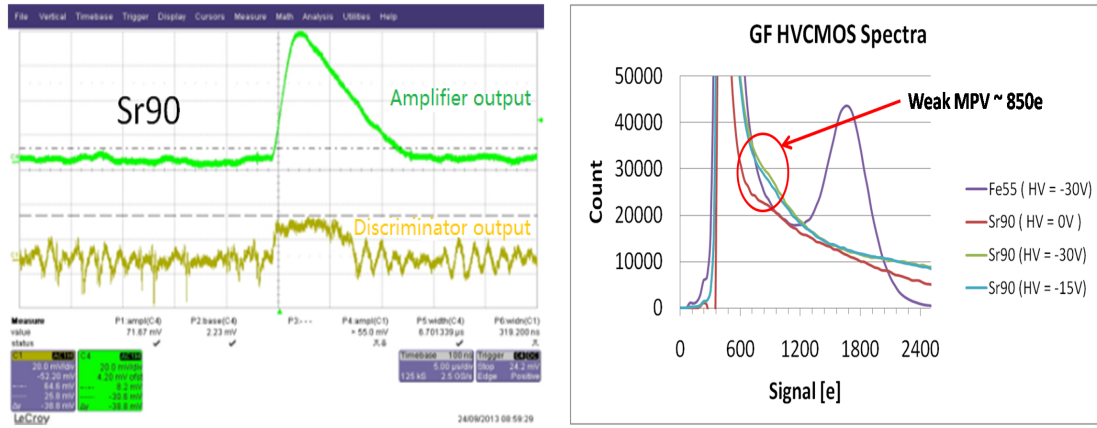
After three iterations of the AMS prototypes, many modifications have been brought to the latest prototype AMS V4 in terms of both the electronics and the charge collection part. Much effort has been done for the preamplifier in order to improve the radiation hardness and reduce the noise, such as implementation of the ELTs in radiation sensitive blocks and keeping linear transistors in the biasing stage to reduce the noise generation. Wider pixel guard-rings also suppressed the leakage current generation. These above mentioned modification results in better radiation hardness for both electronics and charge sensing, as discussed in this section.

5.2.2 GF prototype characterization

5.2.2.1 GF standalone prototype characterization

The prototype GF has been introduced in Section 5.1. It was developed in GF 130 nm BCDlite technology. The sensor was tested before and after X-ray irradiation. The chip works well with -30 V biasing. The preamplifier noise is ~ 50 electrons. The preamplifier and discriminator outputs under a ^{90}Sr source irradiation observed by oscilloscope are shown in Figure 5.41a. The spectra measu-

rement results from both ^{55}Fe and ^{90}Sr (measured by a spectrometer) are shown in Figure 5.41b. The sensor could detect the ^{55}Fe source signal but show low efficiency for ^{90}Sr detection due to some design defects. These defects have been identified and could be fixed in a next submission. The weak MPV (concealed by the noise) is ~ 850 electrons before irradiation at -30 V biasing. Compared with the AMS HV CMOS prototypes, the MPV of GF chip is half of AMS serials, which roughly agrees with the depletion behaviors of these two chips according to the different substrate resistivity and biasing.



(a) Amplifier and comparator signals of ^{90}Sr (b) Spectra of HVC MOS GF amplifier output

Figure 5.41 – (a) : The amplifier and discriminator signals of ^{90}Sr are taken with an oscilloscope. (b) : Weak MIPs detection efficiency is due to the small depletion region and some minor design defects.

Due to a design flaw, the chip can be correctly configured only if the VDDA (typically 1.5 V) is reduced, for instance between 0.9V and 1.4V. A specific function dedicated to probe station testing was integrated into the setup in order to qualify the chips and obtain the best configuration VDDA voltage. The chip is powered, loaded and readout through external probes and a probe card. The probe station platform and the probed chip are shown in Figure 5.42 and 5.43.

In the GF chip, the configuration shift register (SR) consists of 114 bits of bias block, 112 bits for row control and 312 bits for column control. The input SR bits and output bits (Sin and Sout) are stored and compared bit by bit via FIFO blocks that were instantiated in an FPGA. The loading frequency is set to 2.5 KHz. The real time monitoring signals by oscilloscope is shown in Figure 5.44.

For each chip, the VDDA was swept from 0.7 V to 1.5 V in order to find the region that has no configuration errors. Two typical scan results, good and bad, are shown in Figure 5.45a and 5.45b. For the good chip, a wide zero error VDDA region (0.9 V - 1.3 V) is allowed to configure the chip. However, there is no zero error VDDA value region in Figure 5.45b, which is identified as bad chip.

The matrix was irradiated in an X-ray source to 300 MRads at CERN. The

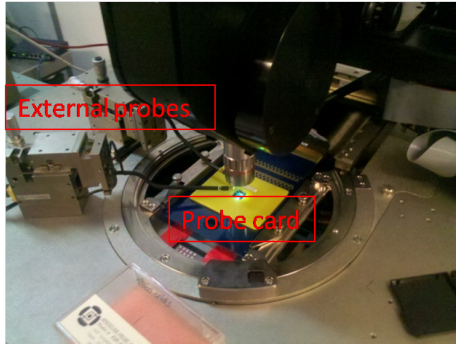


Figure 5.42 – Probe station platform

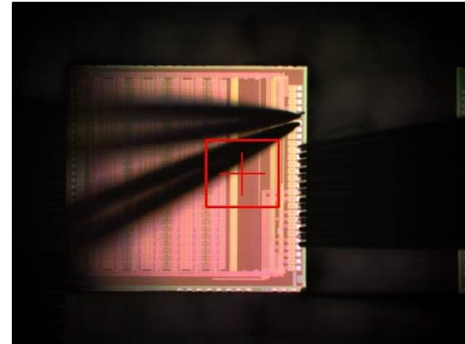


Figure 5.43 – Probed GF V1 chip

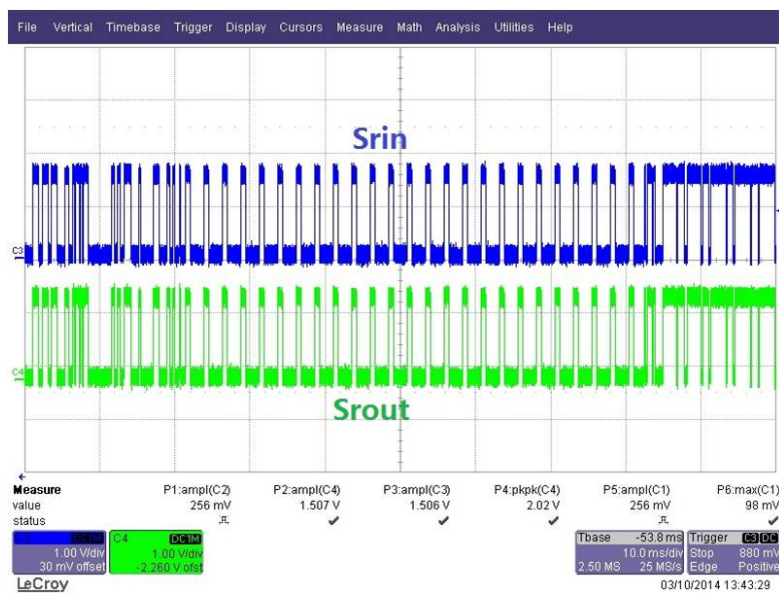


Figure 5.44 – Sin and Sout monitored by oscilloscope

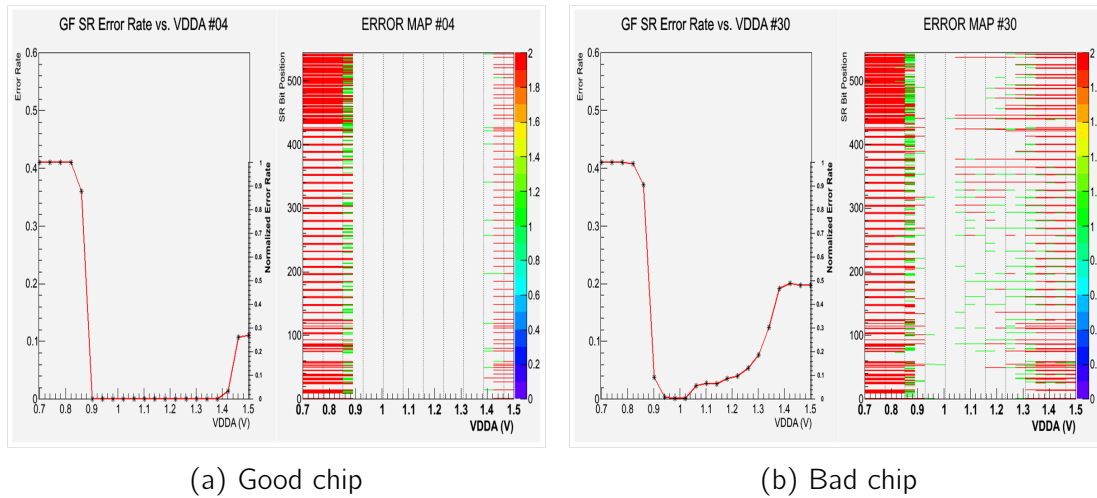


Figure 5.45 – (a) : A good chip identified by the SR scan. (b) : A bad chip identified by the SR scan.

pixels work fine at 0 MRad, but the cascode transistor inside the preamplifier of each pixels in the matrix is not able to deal with the radiations effects over 200 MRads. The preamplifier's amplitude with 1 V test injection of 26 pixels was measured after each irradiation step, as shown in Figure 5.46. All pixels were unresponsive after 200 MRads. The linearity of the pixels in the second column

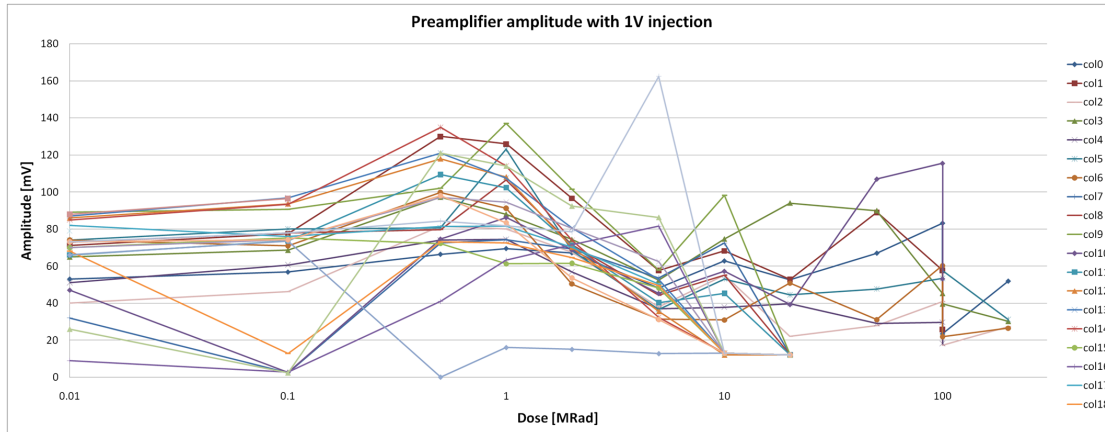


Figure 5.46 – Amplitude of matrix pixels vs. dose

was measured with different test injection. The pixel has fine linearity up to 100 MRads but there is indication that the data loading to the chip has erratic errors, as shown in Figure 5.47.

More tests could be performed thanks to the two special pixels "DNW-pixel" and "Alone-pixel" located outside of the matrix, which are not subject to these minor defects.

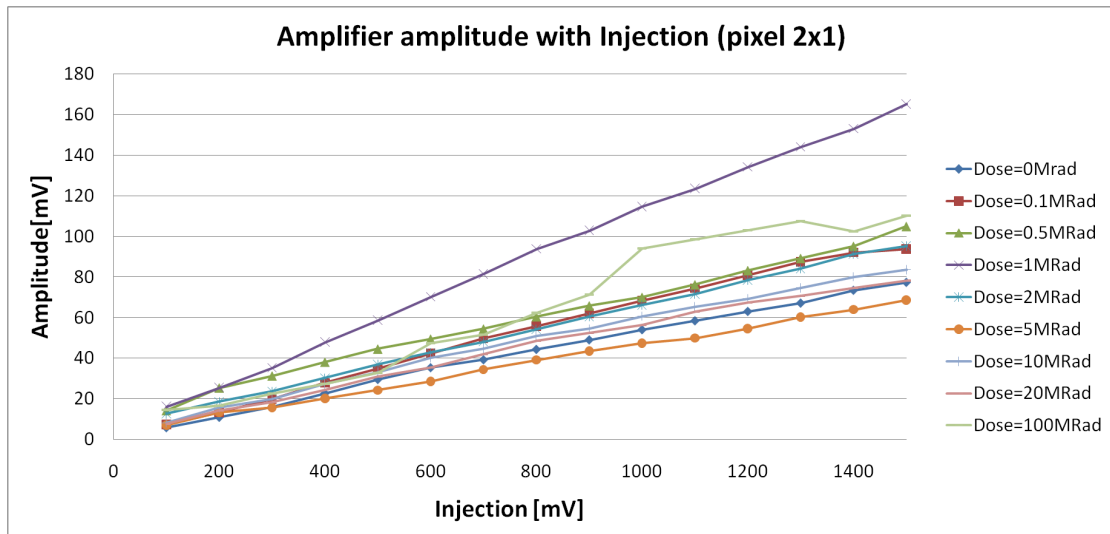
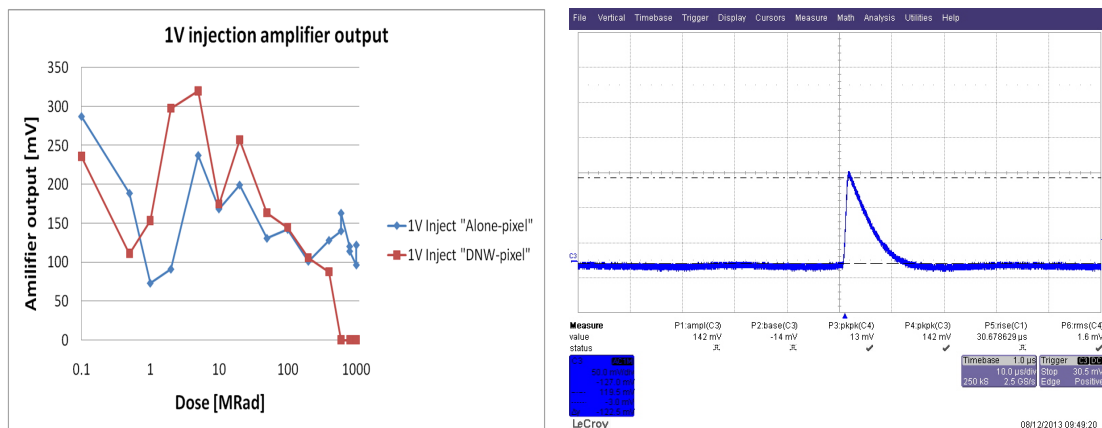
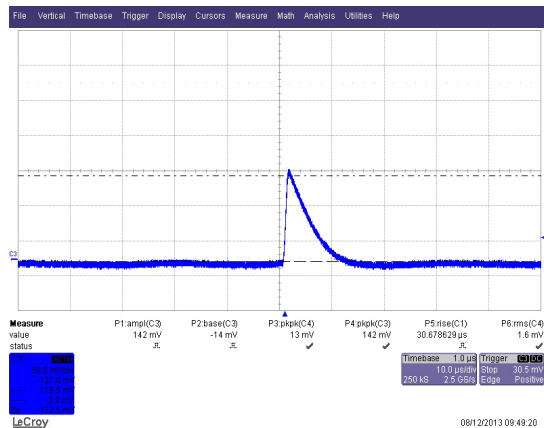


Figure 5.47 – Linearity of matrix pixel at different dose levels



(a) Preamplifier output vs. the dose



(b) ^{90}Sr response of the "Alone-pixel"

Figure 5.48 – (a) : The amplitudes of the “Along-pixel” and the “DNW-pixel” as a function of dose. (b) : The output signal of the preamplifier of the “Alone-pixel” for ^{90}Sr source.

These two special pixels were irradiated to 1 GRad. As shown in Figure 5.48a, the "Alone-pixel" could detect external test 1V injection after a dose as high as 1

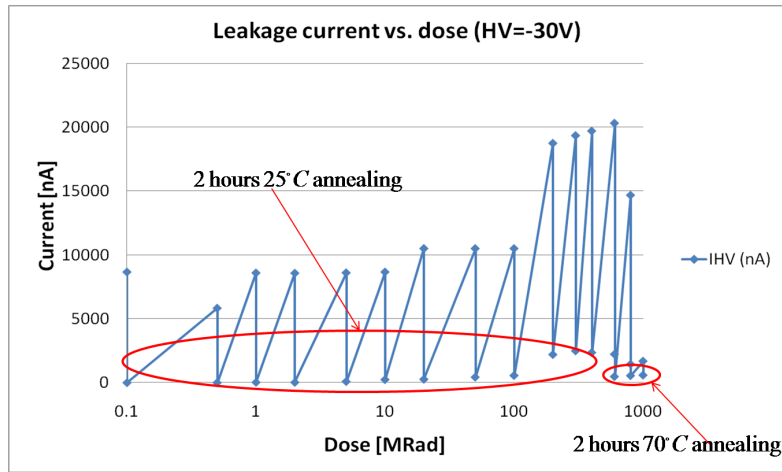


Figure 5.49 – Leakage current as a function of the dose

GRad and the screenshot of the response to a ^{90}Sr signal is shown in Figure 5.48b after this dose. The leakage current increases to $20\text{ }\mu\text{A}$ at 1 GRad, but the chip recovers after two hours of accelerated annealing at 70°C , and the current goes back to 500 nA , as shown in Figure 5.49.

A 6-bit DAC similar to the DACs used to bias all analog stages was implemented for test purpose. The outputs of the test DAC were measured after 800 MRads, as shown in Figure 5.50. The output slopes change slightly compared to its behavior pre-irradiation, but some periodical jumps reveal that some bits are stuck to bit "1", and indicate that TID affects the DAC operation conditions at transistor level.

The inner current reference was also monitored by measuring the equivalent voltage converted by a resistor implemented inside the chip. Its variation with irradiation is shown in Figure 5.51 and good radiation hardness could be demonstrated.

Three kinds of transistors were designed to test the radiation hardness of the technology. The transistor sizes are listed in Table 5.4. Some transistors were unfortunately unresponsive before irradiation, and we tested only the Mini_NMOS, Narrow_NMOS, ELT_NMOS and ELT_PMOS.

The leakage current and threshold voltage variations with irradiation are shown in Fig 5.52a and 5.52b. All transistors show good radiation hardness, in particular the ELT_NMOS transistor. We can note that a big increase in leakage current and decrease in threshold voltage occurs for the Mini_NMOS transistor after 2 hours of 70°C annealing. We think that at this stage, this transistor was lost for a reason unrelated to radiation damage and plan further exploration in the future.

As discussed above, both the special test pixel and the single test transistors showed good radiation tolerance as high as 1 GRad X-ray dose though the matrix

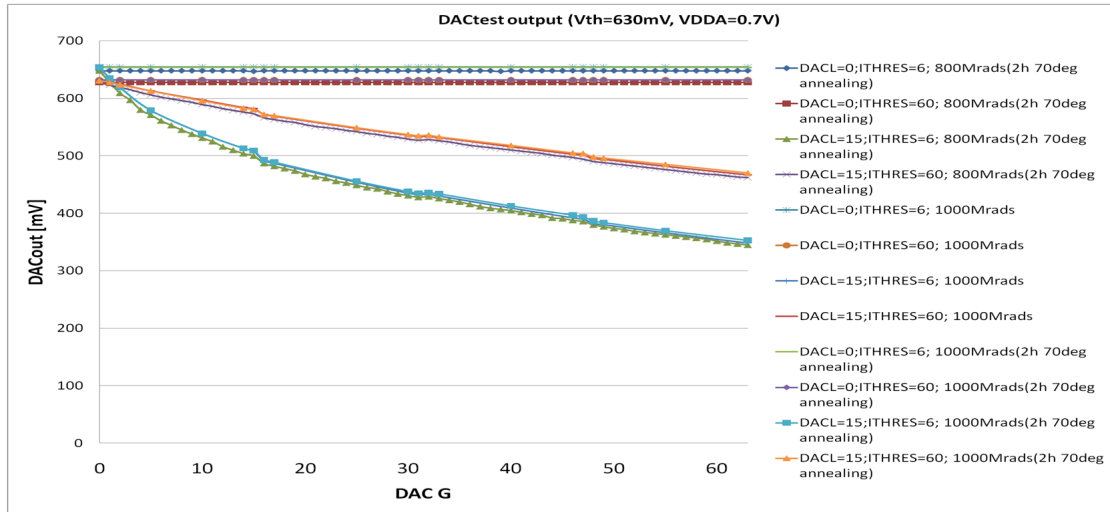


Figure 5.50 – Test-DAC outputs at 800 and 1000 MRads

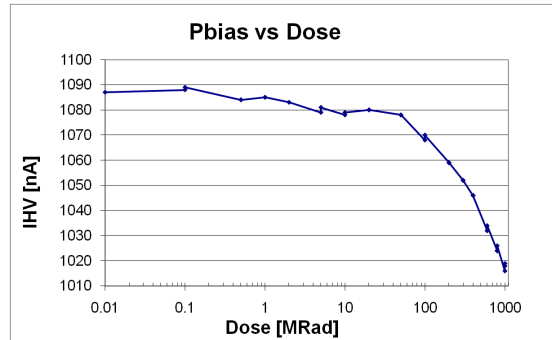
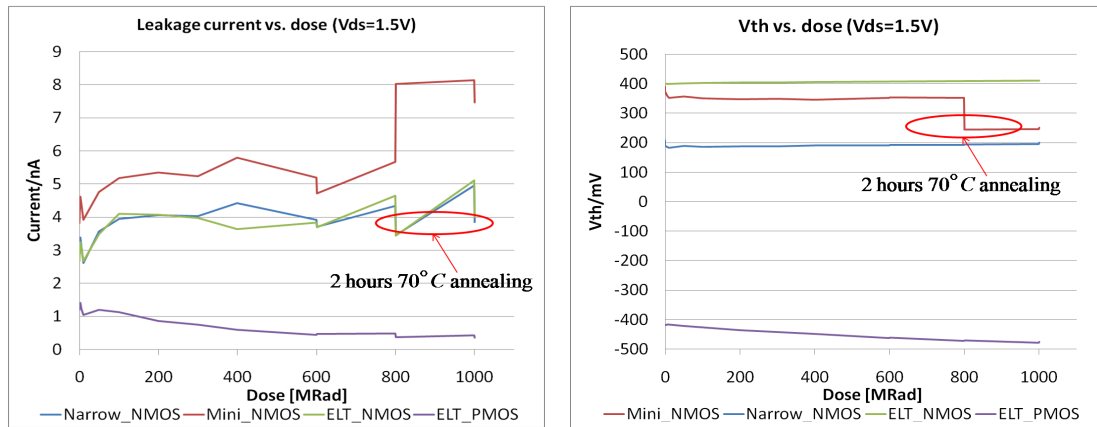


Figure 5.51 – Pbias variation as a function of dose

Table 5.4 – Transistor size

Transistor	Type	Width/Length
Mini_NMOS	NMOS	50nm/130nm
Narrow_NMOS	NMOS	200n/15 μ m
ELT_NMOS	NMOS	2.64 μ m/160nm
Mini_PMOS	PMOS	50nm/130nm
Narrow_PMOS	PMOS	200n/15 μ m
ELT_PMOS	PMOS	2.64 μ m/160nm



(a) Leakage current as a function of the dose (b) Threshold as a function of the dose

Figure 5.52 – The relatively small variations of the leakage current and of the threshold voltage show that the technology is quite radiation hard, up to 1 GRad radiation dose.

pixel has some minor design defects for the output buffer. A low MIPS detection efficiency was found for this prototype due to both the small depleted area and the weak output buffer. An improved detection efficiency is expected by using a high resistivity substrate which would be offered for this technology.

5.2.2.2 GF HV2FEI4 assembly characterization

The GF prototypes are compatible with the FE-I4 chip, and it can be coupled with FE-I4 capacitively using liquid fluid epoxy glue. This assembly is then called HV2FEI4. To demonstrate the functionality of the HV2FEI4 assembly, some tests were performed where charge is injected in the HV CMOS sensor and the hits are recorded by the FE-I4. The match map between the FE-I4 and the GF chip is shown in Figure 5.53. As mentioned in Section 5.1.1, the first 6 triple columns (the first 18 columns) of GF are implemented with serial capacitors before the output metal plates. The remaining pixels are directly connected to metal plates. For simplicity, the sensor row number will be written as 0, 1, 2, ..., 13 instead of the original 0R, 0L, 1L, ..., 7R.

Before the characterization of HV2FEI4 assembly, the first step is to tune the FE-I4 to a proper operation status for HV CMOS sensor measurement. For GF prototype, the FE-I4 threshold was tuned to 1500 electrons (TDAC tuning) and the TOT code "11" is equivalent to 20,000 electrons (FDAC tuning). The TDAC and FDAC tuning results are shown in Figure 5.54 and 5.55.

An external trigger method is used for HV2FEI4 measurements. The timing diagram is shown in Figure 5.56. A proper delay should be set in order to match the FE-I4 internal clock.

The HisDiscCnfg register of the FE-I4 is set to 0. In this case, the effective

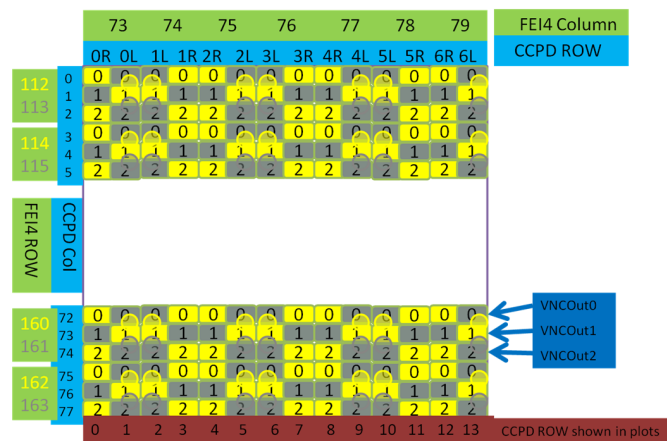


Figure 5.53 – The correspondence between FE-I4 and GF chip

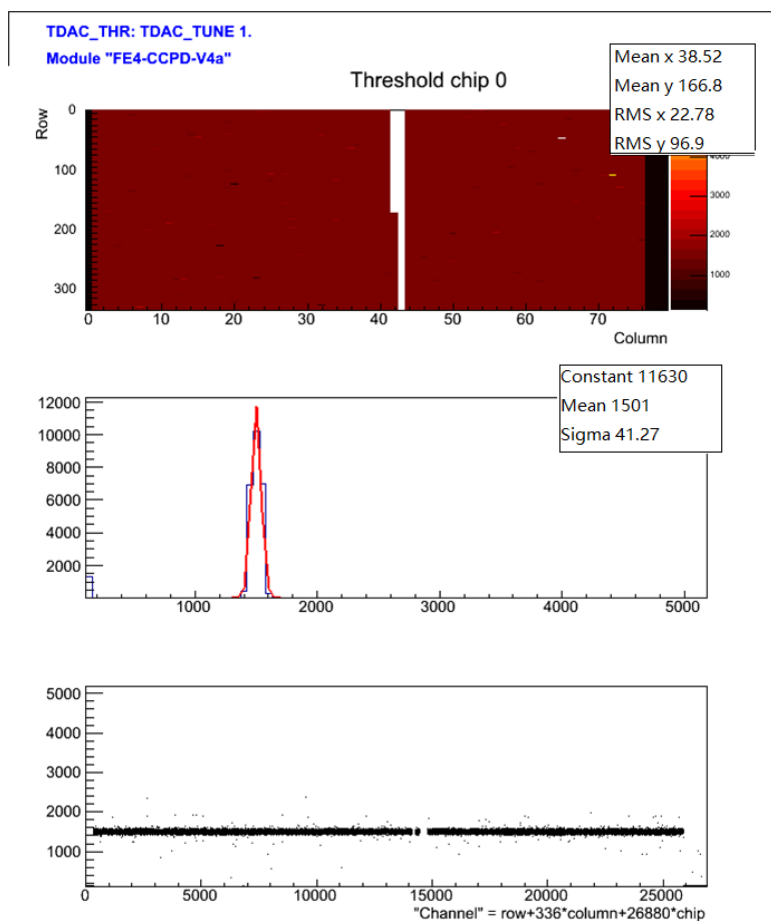


Figure 5.54 – TDAC tuning to 1500 electrons for TH.

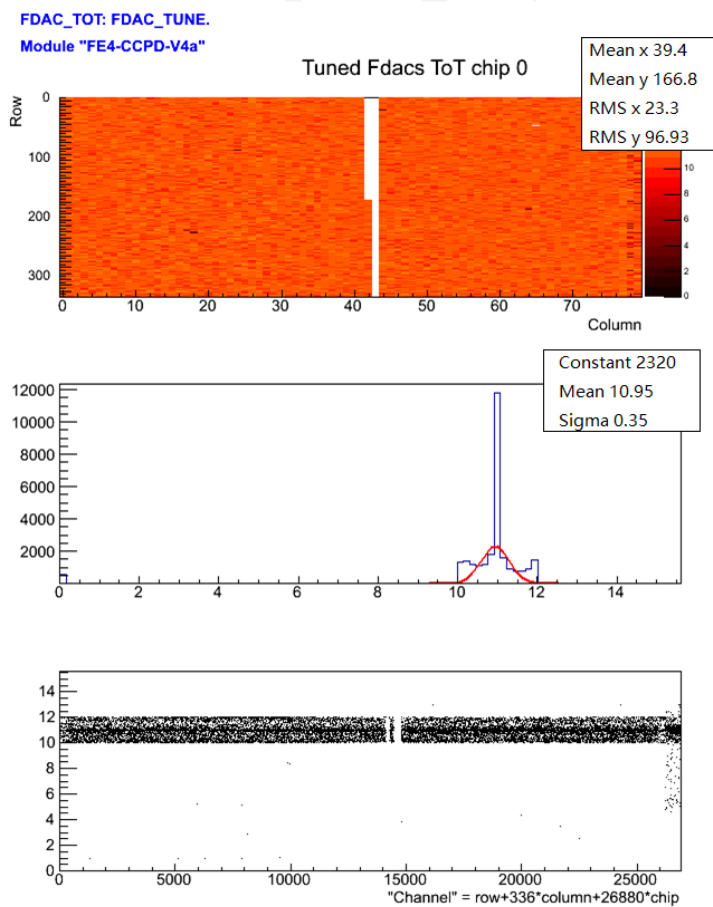


Figure 5.55 – FDAC tuning to "11" is equivalent to 20,000 electrons.

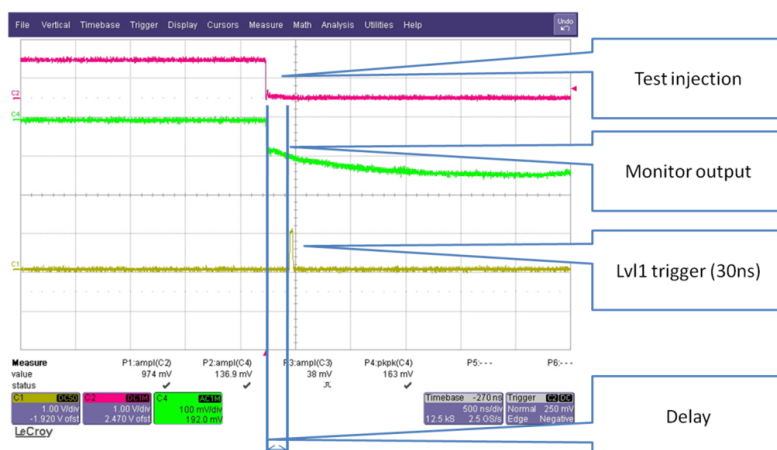


Figure 5.56 – FEI4 trigger diagram for the HV2FEI4 assembly test. The red pulse is the test injection. The discriminator output signal is in green. The FE-I4 Lvl1 trigger is shown in yellow.

range of the TOT is from 0 to 13 and no hits should be classified as small hits (TOT value is 14). Therefore ToT code 14 should never occur. However, the

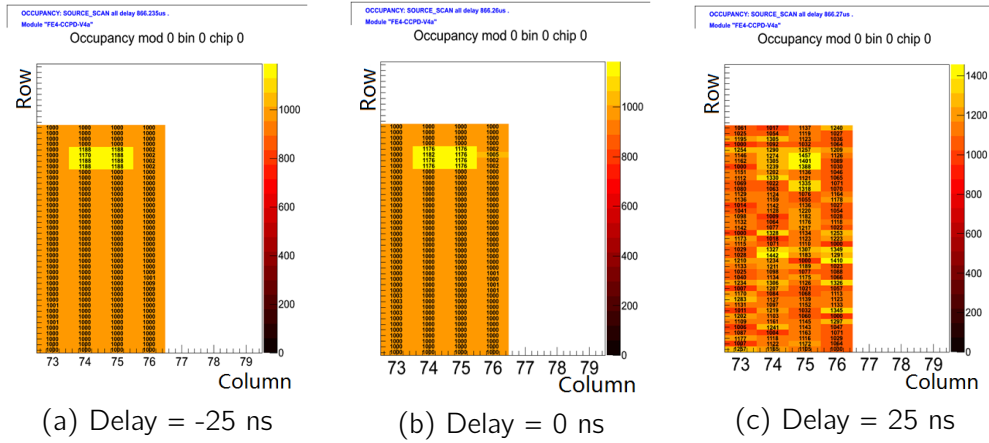


Figure 5.57 – FE-I4 occupancy with different Lvl1 trigger delays

association logic in the pixel region will create duplicated hits with TOT code 14 when HitDiscCfg=0 (this is a feature of how the FE-I4 pixel logic works). These duplicated hits should be ignored. The FE-I4B will automatically ignore them by setting SmallHitErase=1. This switch was included as an independent control for debugging purposes, but for normal operation SmallHitErase should always be set to the logical negative of HitDiscCfg. Figure 5.57 and 5.58 show the occupancy counts and their corresponding lvl1 trigger ID (1000 times external injection) with different trigger delays. One can see that if the trigger does not match the FE-I4 clock, the hits within one bunch crossing are recorded as in two bunch crossings and cause over counting issues, as shown in Figure 5.57c and 5.58c.

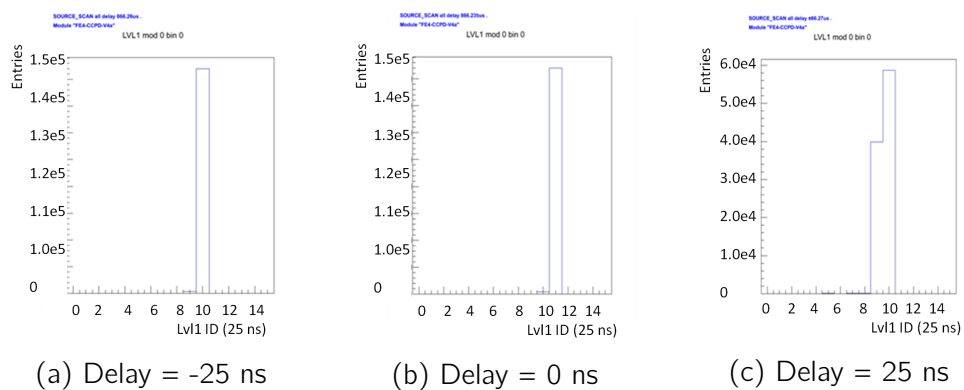


Figure 5.58 – FE-I4 Lvl1 ID with different Lvl1 trigger delays

The FE-I4 occupancy map and counting distribution when doing a 1000 external 1V injections in each HVCMOS pixel are shown in Figure 5.59a and 5.59b

(setting : BL = 0.65V, TH = 0.68V and VNCO_{0,1,2} = 60,60,60). This demonstrates good communication between the HVCMOS sensor glued to the FE-I4 and the FE-I4 chip itself, using this AC coupling method.

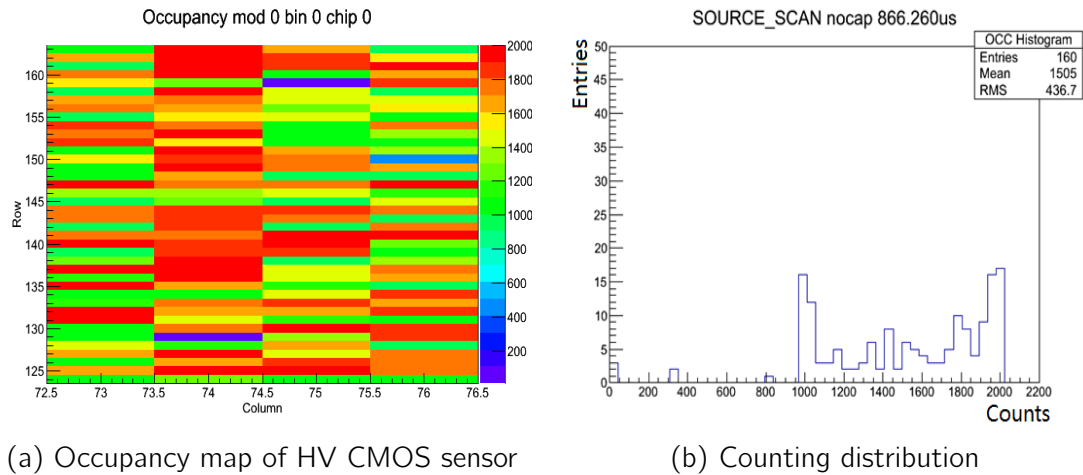


Figure 5.59 – (a) : The occupancy of 1000 times injection shows the sensor is able to communicate with FE-I4. But the over counting indicates the time-walk is larger than one bunch crossing. (b) : The distribution of the pixel counting.

The 1000 external injections result in the counting range from 200 to 2000 for the matrix pixels, as shown in Fig 5.60. The sensor outputs Lvl1 ID measured by the FE-I4 is distributed in three bunch-crossings as shown in Figure 5.60a and the ToT distribution is shown in Figure 5.60b (ToT code 14 means "late hit"). Once a hit is recorded after the correct bunch crossing (25ns) window, it will

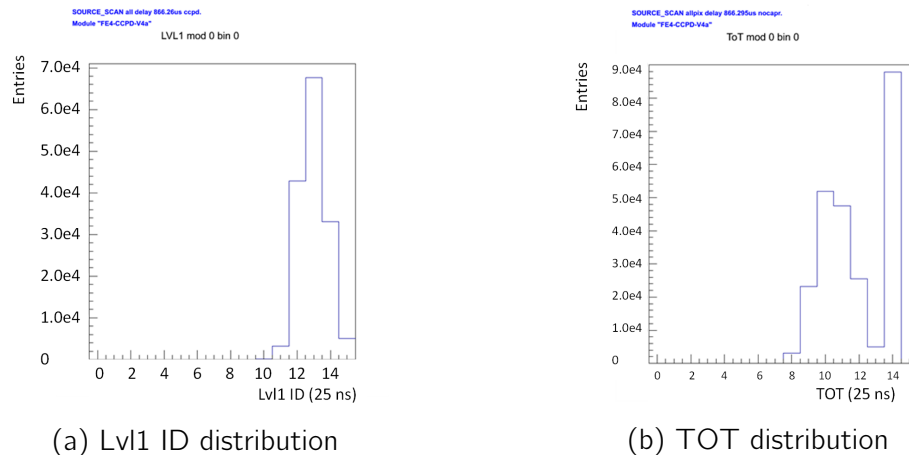


Figure 5.60 – (a) : The Lvl1 ID (25 ns unit) distribution of the assembly. (b) : TOT distribution of the assembly.

be classified as a "late hit". The "late hits" are duplicated in the FE-I4, therefore leads to the over counting. The over counting indicates that the time-walk is larger than one bunch crossing. We can measure the signal delay by tuning the threshold of the HVCMOS sensor with different injection charges. The Lvl1 ID shifts of 1 V external injection with different sensor TH are shown in Figure 5.61. This measurement gives the time-walk information. The preliminary measured

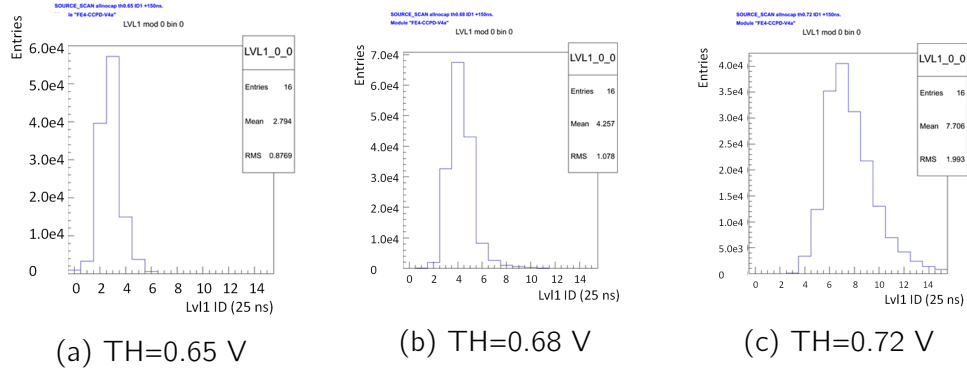


Figure 5.61 – The Lvl1 ID distributions for 1V injections with different sensor thresholds.

time walk is 29 ns with 20 mV above the base line (charge range from 918 to 4594 electrons), as shown in Figure 5.62a.

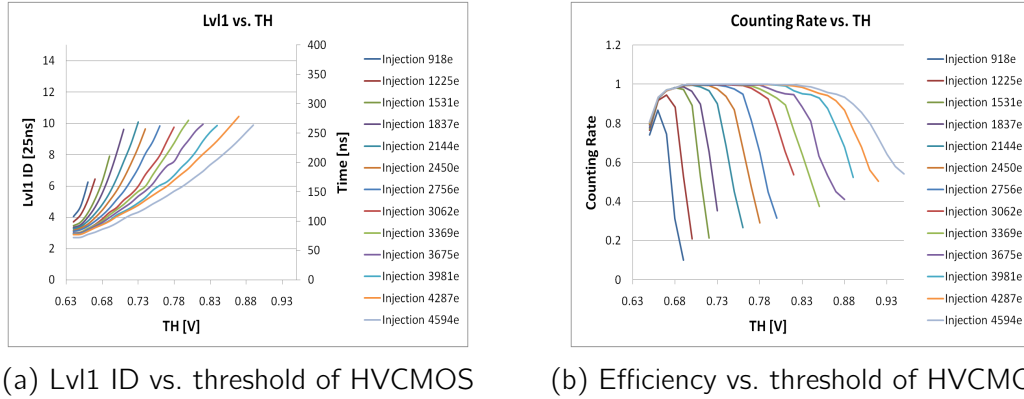


Figure 5.62 – (a) : The Lvl1 ID indicates the delay of the signal. (b) : The counting rate is measured by tuning TH with different injections. The shape of amplifier's output can be reconstructed by tuning the TH.

The counting rates with different TH and injection voltage were measured, as shown in Figure 5.62b. An efficiency of 100% before threshold tuning can be reached when the input electrons are 1837 electrons, as shown in Figure 5.62b. After threshold tuning, we expect that this 100% detection efficiency will be reached with lower signal.

The TOT values of sensor pixels with and without serial capacitors (implemented before readout plates) were measured as shown in Figure 5.63a and 5.63b. The serial capacitor value was of 153 fF. The coupling capacitance is ~ 65 fF,

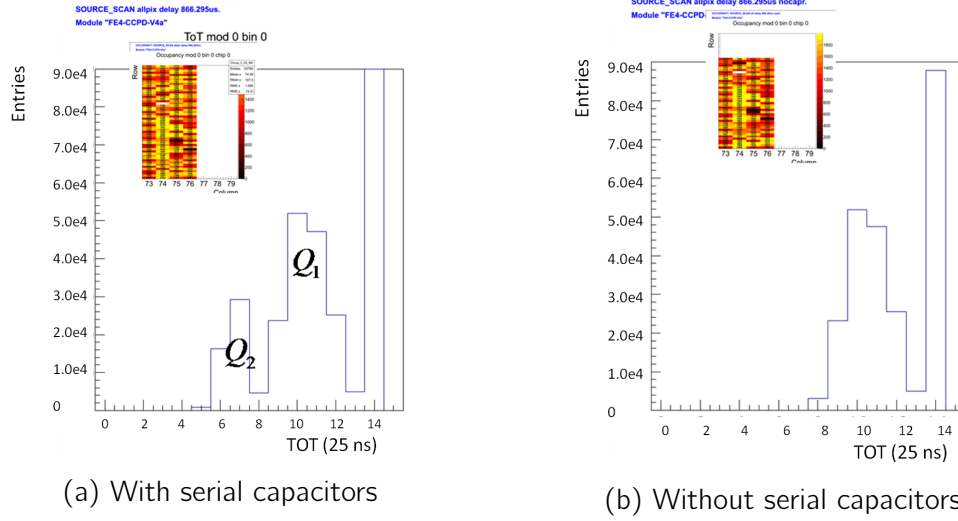


Figure 5.63 – (a) : TOT value of pixels with serial capacitors. (b) : TOT value of pixels without serial capacitors.

which is calculated through the two TOT peaks in Figure 5.63a. Therefore, we can extract the glue thickness from the coupling capacitance : $\sim 1 \mu m$.

A unit readout cell is schematized in Figure 5.64. The three yellow GF sensor

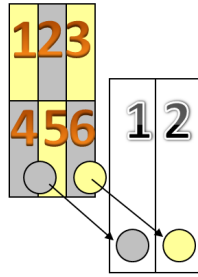
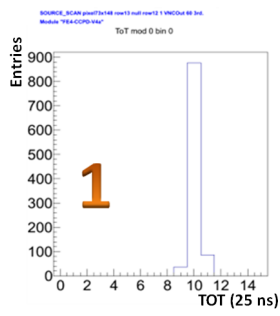


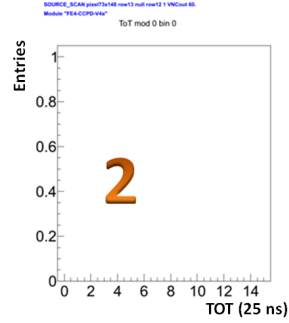
Figure 5.64 – Unit readout cell of HV2FEI4 assembly

pixels “1”, “3” and “5” are readout by FE-I4 pixel “1” and the remaining three grey pixels are readout by FE-I4 pixel “2”.

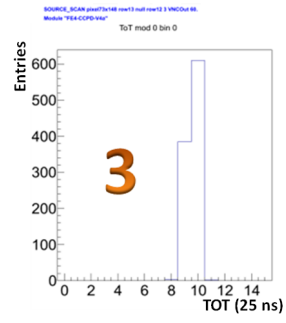
In order to investigate the crosstalk between the sensor and the FE-I4, the TOT value was recorded by the FE-I4 pixel “1” when only one GF sensor pixel was enabled in the unit cell. The 1 V injection TOT results are shown in Figure 5.65. The sub-pixels can be read out by the FE-I4 correctly. The sum signals of three sub-pixels of “1”, “3”, “5” and “2”, “4”, “6” were also measured by FE-I4 pixel “1”. The results is shown in Figure 5.68a and 5.68b.



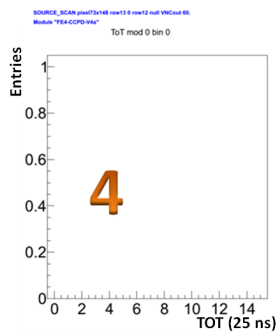
(a) ToT value of pixel "1"



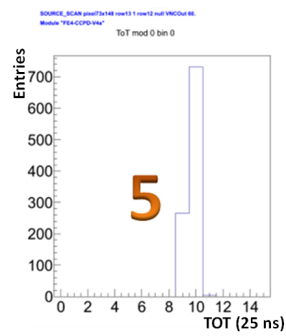
(b) ToT value of pixel "2"



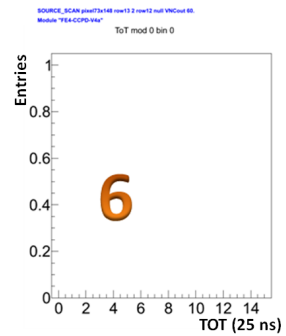
(c) ToT value of pixel "3"



(d) ToT value of pixel "4"



(e) ToT value of pixel "5"



(f) ToT value of pixel "6"

Figure 5.65 – One pixel readout of unit cell

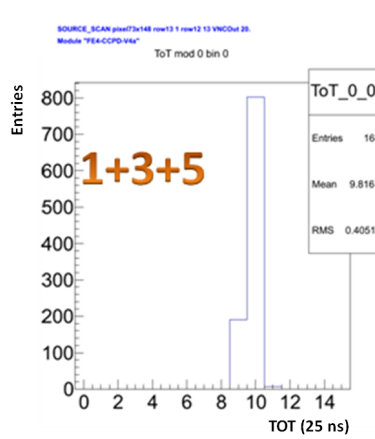


Figure 5.66 – Sum signal of pixel "1", "3", "5"

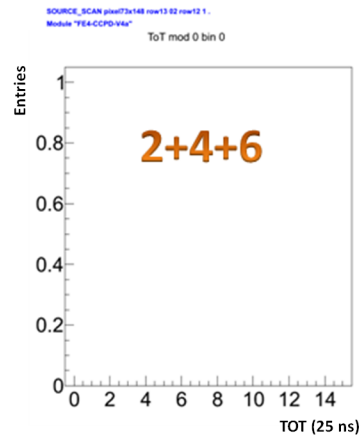
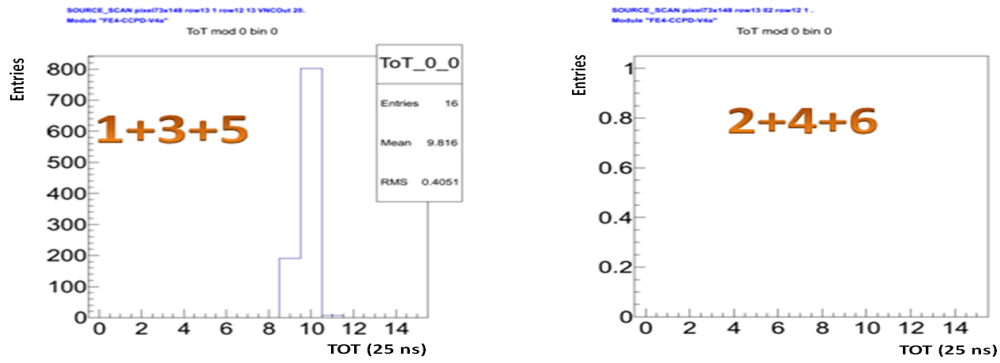


Figure 5.67 – Sum signal of pixel "2", "4", "6"



(a) Pixel "1", "3" and "5"

(b) Pixel "2", "4" and "6"

Figure 5.68 – (a) : Summed signals of the pixel "1", "3" and "5" measured by the FE-I4. (b) : Summed signals of the pixel "2", "4" and "6" measured by the FE-I4.

No signal for the pixel "2", "4" and "6" were observed by the FE-I4 pixel "1", which indicates there is no crosstalk and the gluing has fine alignment between sensor and FE-I4.

Figure 5.69 shows the TOT codes of three grey sub-pixels' with weighted output amplitudes. One can see there that the FE-I4 can distinguish the three sub-

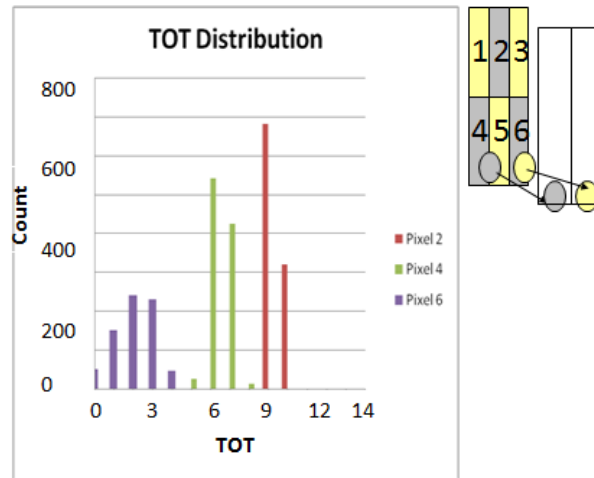


Figure 5.69 – TOT with weighted HV CMOS outputs. The three grey sensor pixels are connected to a single FE-I4 pixel and distinguished by weighted outputs.

pixels. The output of few pixels with different VNCOut codes, using a 6 bits DAC to tune the weighted output amplitude, are shown in Figure 5.70a. The output amplitude saturates when VNCOut are higher than 20. The saturation value corresponds to approximately 20000e converted by the TOT/Injection plot,

recorded with direct charge injection into the FE-I4, which can be found in Figure 5.70b.

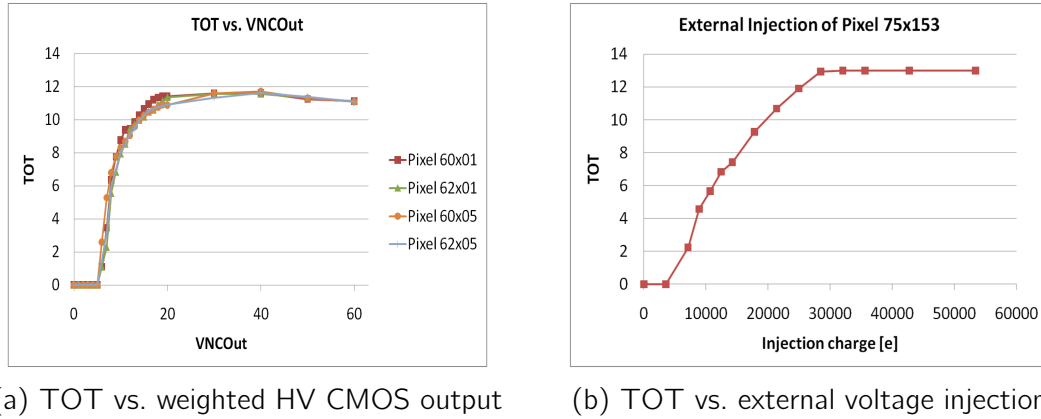


Figure 5.70 – (a) : A sweep of the 6-bit DAC "VNCOut" (controlling the weighted comparator output) is performed to explore the output linearity of the comparator. (b) : Direct injection to the FE-I4 with specific charges is performed to calibrate the TOT, which can be used for the calculation of comparator amplitude.

In order to achieve the best detection efficiency, a so-called threshold tuning based on noise method was performed. The first step consists in sweeping the threshold of the sensor with a fix test injection voltage. A hit rate as a function of threshold can be obtained, as shown in Figure 5.71. A 100% hit threshold value

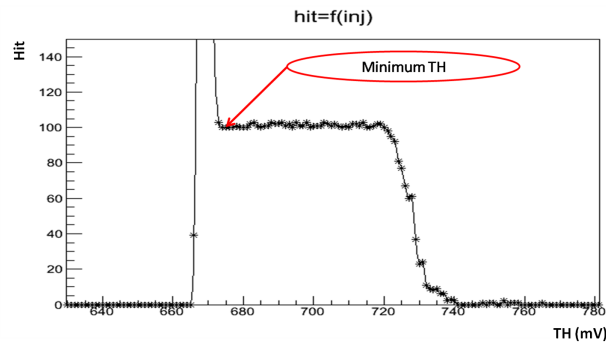


Figure 5.71 – Hitting rate vs. TH

can be found just after the baseline noise in Figure 5.71, which is identified as the minimum threshold. Then, one can tune the 4-bit local DAC to adjust the threshold. As this procedure is quite time consuming, a threshold scan for the half matrix of the GF chip was performed with local DAC at 7. The threshold map and distribution are shown in Figure 5.72a and 5.72b. In order to improve the uniformity of the threshold of individual pixels, a threshold tuning program

was integrated into the test software. Figure 5.73a and 5.73b show the threshold map and distribution after tuning where we can see the significant improvement in the threshold uniformity post-tuning. The local DAC values after threshold tuning are shown in Figure 5.74.

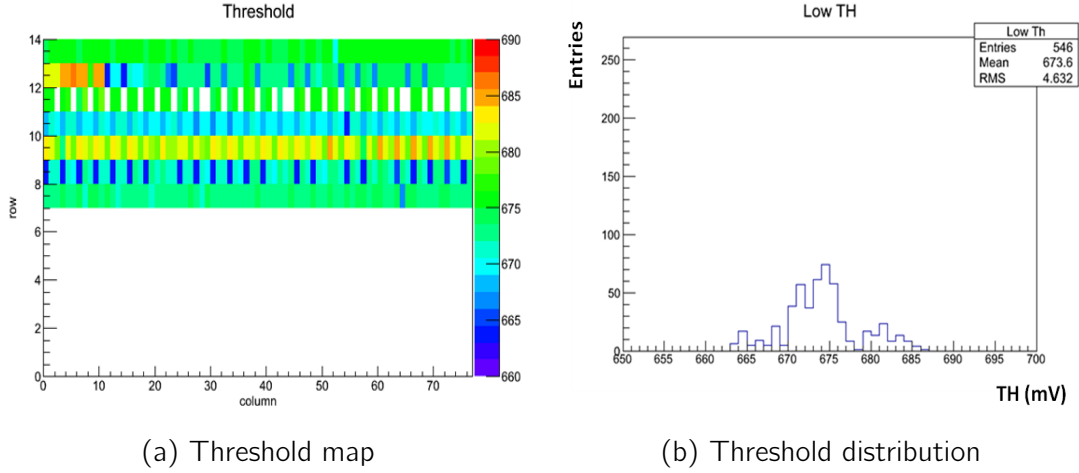


Figure 5.72 – (a) : The threshold map before tuning. The pixels which have no output signals are shown in white. The pixels are controlled horizontally row by row and vertically in triple-column structure. We can see the threshold differences periodically possibly due to the transistor mismatch and parasitic capacitance from the layout.(b) : The threshold distribution before tuning.

A good communication between the GF prototype and the FE-I4 has been demonstrated for the HV2FEI4 assembly. The sensor pixels with weighted output were distinguished by the FE-I4, which could offer better spacial resolution with respect to the current ATLAS planar sensors. A time-walk of approximately 29 ns and a epoxy glue thickness of about 1 μm were measured for this assembly.

5.2.3 Characterization of LF CCPD prototypes

The LF technology is a 150 nm technology with optionally high resistivity (HR) ($1 - 3k \Omega \cdot cm$) wafer and deep-wells. Two kinds of prototypes are designed with different charge collection diodes, which are labeled as version A (VA) and version B (VB). The layout of VA and VB are schematized in Figure 5.75 and 5.76.

As shown in Figure 5.75, the electronics is isolated from the HV ring by the Deep N-Well (DNW) in VA layout. The internal Pwell and Nwell are also isolated from the substrate by using the specific isolation layers. Therefore, a negative HV can be applied via the HV ring surrounding the DNW.

Another structure is chosen for the VB as the electronics of the VB is not isolated from the DNW. The diode can be positively biased through the DNW.

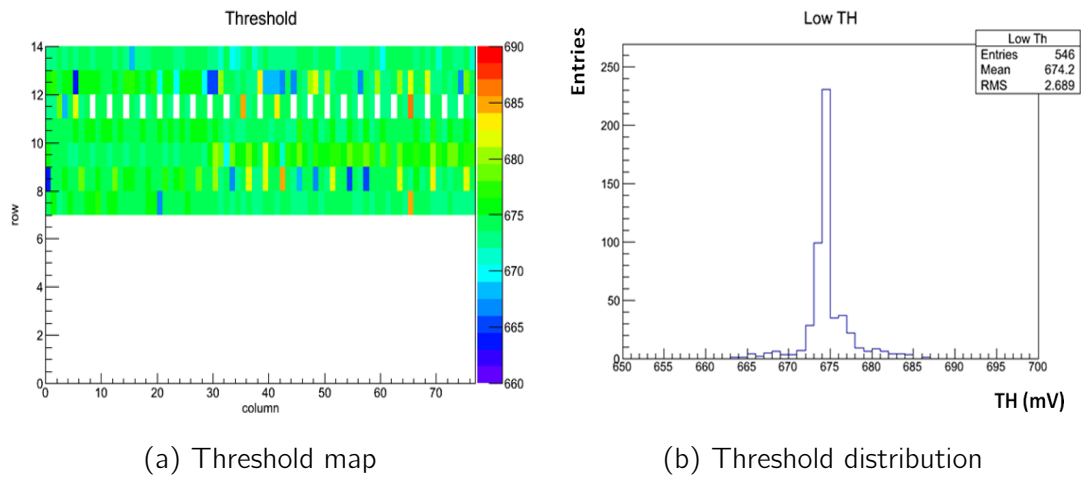


Figure 5.73 – (a) : The threshold map after tuning. (b) : The threshold distribution after tuning.

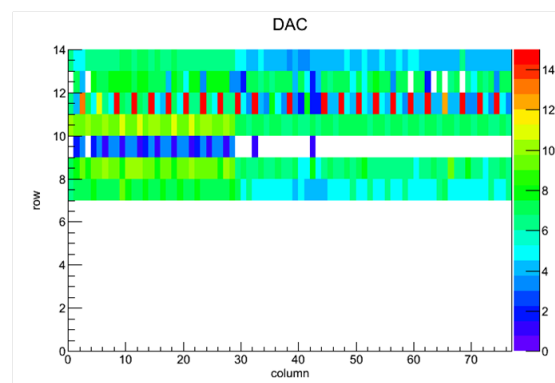


Figure 5.74 – Local DAC map after threshold tuning. The DAC value of “0” is drawn in white.

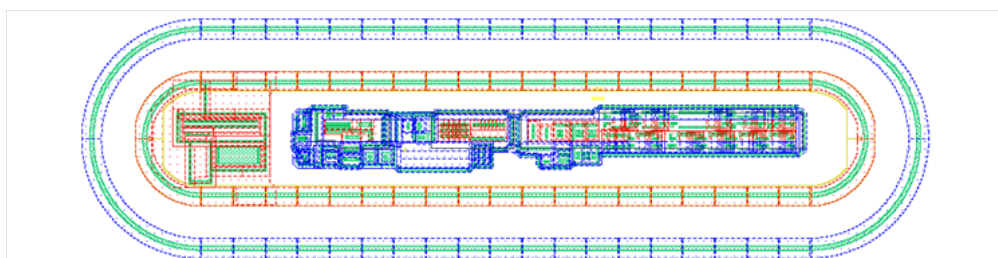


Figure 5.75 – LF VA layout

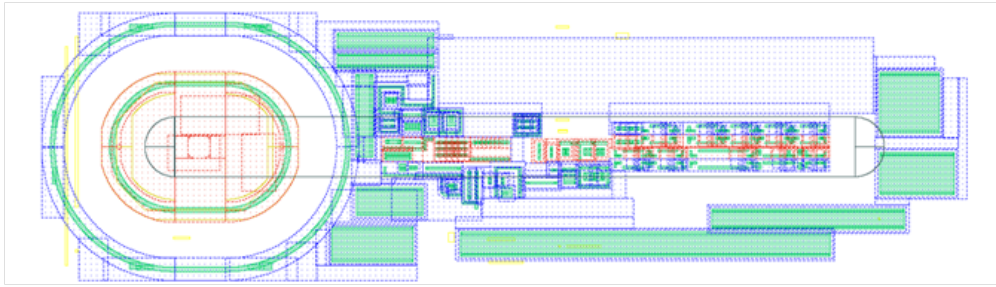


Figure 5.76 – LF VB layout

The prototype floorplan is shown in Figure 5.77. The chip size is 5 mm by 5 mm. The pixel matrix consists of 24 rows and 144 columns resulting in 3456 pixels. The pixel size is also $33 \times 125 \mu m^2$ identical to the AMS and the GF pixel size. A “BiasBlock” cell with eleven 6-bit DACs to generate all the polarizations of the pixel and one additional test DAC are located at the bottom of the chip. A “DigitalMatrix” cell to activate and select pixels is also in the chip periphery. An end of row cell designed for buffered signals transmission and row selection is located at the side of the chip. Some NMOS and PMOS test transistors and a test analogue buffer are implemented in the top of VA. Different flavors of test diodes are implemented in the top of VB.

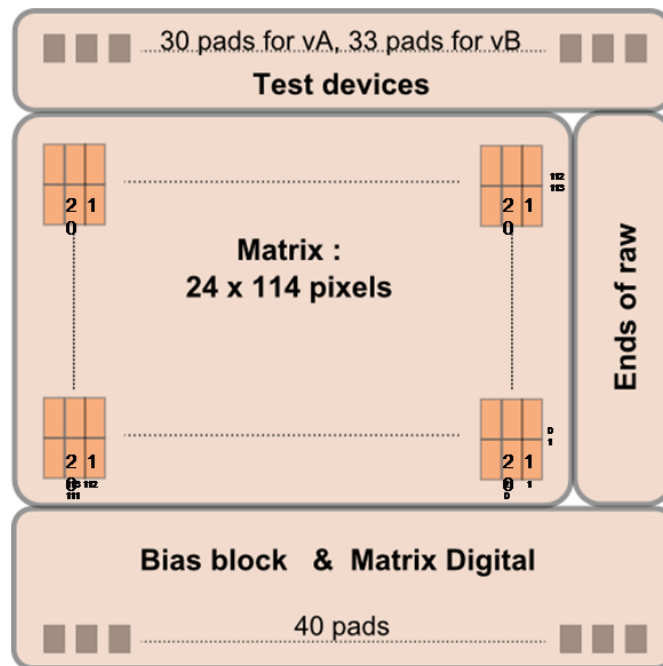


Figure 5.77 – LF prototype floorplan

Each pixel VA or VB is composed of a preamplifier which is AC coupled with the DNwell diode, a source follower and a comparator. For VA, 3 pixel flavors

have been implemented with different preamplifier feedback transistors. The VB chip has 3 flavors of feedback transistors as well. For VB, two different HV bias circuit are designed (via a diode or via a poly resistor). In addition, the VB pixels are separated in two groups with different PSUB layer implementations. The various pixel flavors for both VA and VB are illustrated in Figure 5.78.

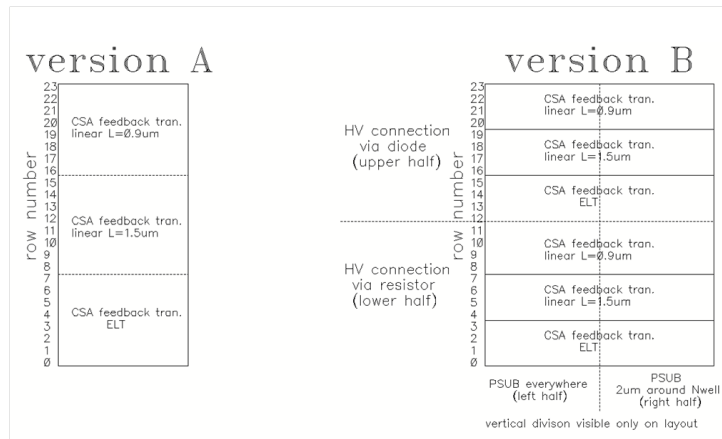


Figure 5.78 – Placement of pixel flavors of VA and VB

The guard-rings were designed for these prototype, as sketched in Figure 5.79, to smooth on the voltage drop from the pixels to the cutting edge and control the depleted region close to the cutting edge.

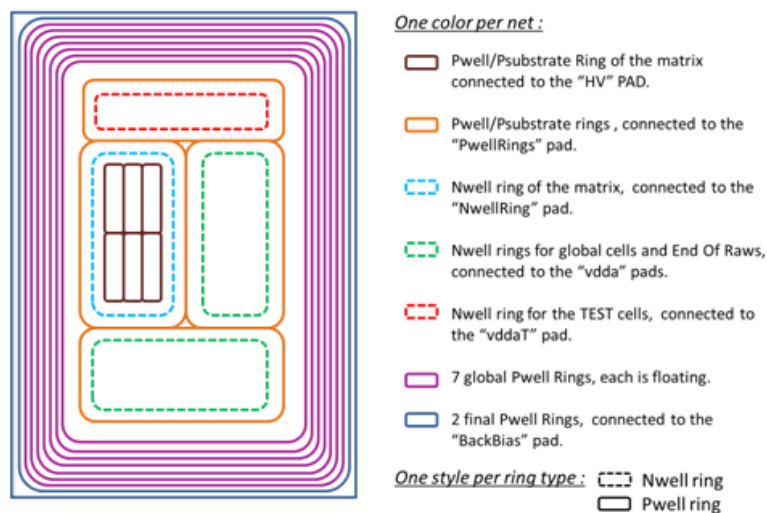


Figure 5.79 – LF CCPD guardring layout

The CCPD VA was carefully studied due to its higher breakdown voltage compared with VB. The higher breakdown voltage results in a larger depleted region

and better charge collection efficiency. A full matrix threshold scan was performed to investigate the electronics performance. The test pulses were applied to the input of preamplifier via a test capacitor that converts the voltage signal to a current pulse. The threshold scan results are shown in Figure 5.80. One can see a very large dispersion for the threshold which range from approximately 2000 to 7000 electrons.

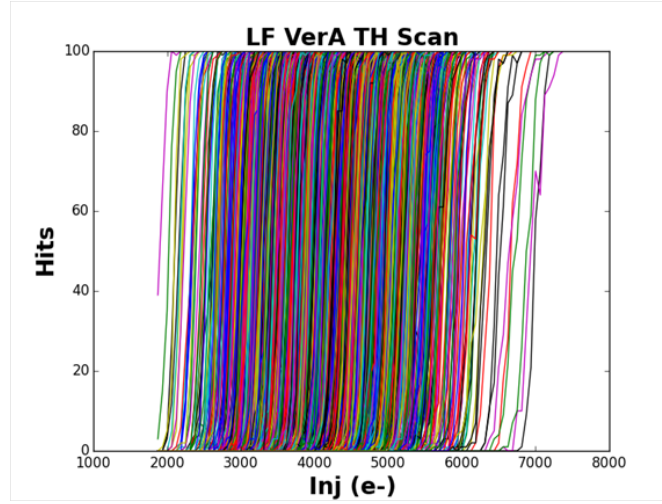


Figure 5.80 – LF CCPD VA analog scan

As shown in Figure 5.78, the matrix of VA consists of three flavors of pixels with different feedback transistors. The pixels with ELT in their feedback have significant different performance compared to the linear ones. Therefore, the pixels are divided into two separated parts, that we call here ELT pixels and LIN pixels, for the full matrix threshold scan. The threshold scan was performed initially with TDAC = 7 (the middle value of the dynamic range). Only the pixel under study was enabled during the threshold scan. The remaining pixels were disabled by setting the biasing current of preamplifier to 0 nA. The threshold and noise distributions as well as the maps of ELT pixels extracted from the threshold scan are shown in Figure 5.81 and 5.82. In order to reduce the dispersion of the threshold, the TDAC values were tuned for each pixel individually. The tuned threshold and noise distributions as well as maps of ELT pixels are shown in Figure 5.83 and 5.84. Reduced dispersion was observed as we expected. However, there are still many pixels which can not be tuned close to the target value due to the large initial dispersion.

Similar results were obtained for the LIN pixels, as shown from Figure 5.85 to 5.88.

Threshold scans were also performed enabling all preamplifiers for the matrix. The threshold and noise distributions and maps for the ELT pixels before and after tuning are shown from Figure 5.89 to 5.92 respectively. Figure 5.93 to 5.96 show the threshold scan and tuning results of LIN pixels. Compared to the single

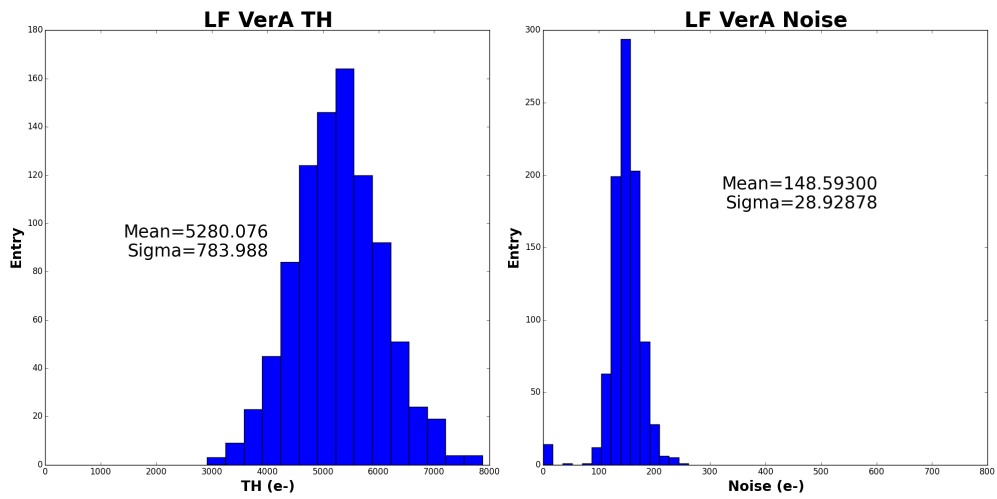


Figure 5.81 – Threshold and noise distributions before tuning for ELT pixels before TDAC tuning, one pixel enabled mode.

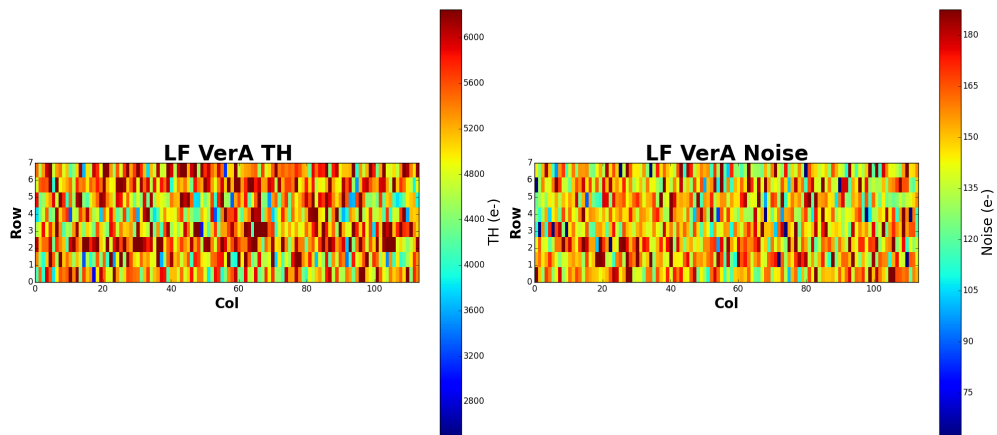


Figure 5.82 – Threshold and noise maps before tuning for ELT pixels before TDAC tuning, one pixel enabled mode.

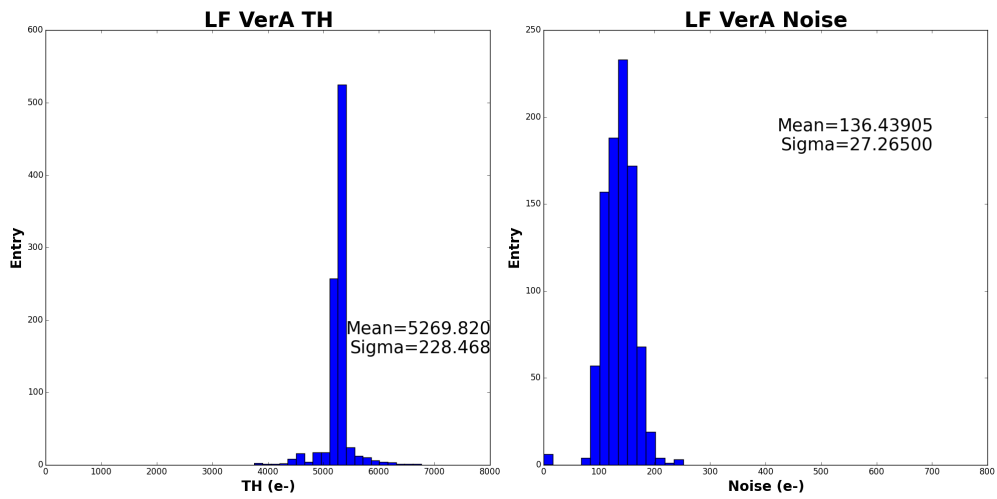


Figure 5.83 – Threshold and noise distributions after tuning for ELT pixels before TDAC tuning, one pixel enabled mode.

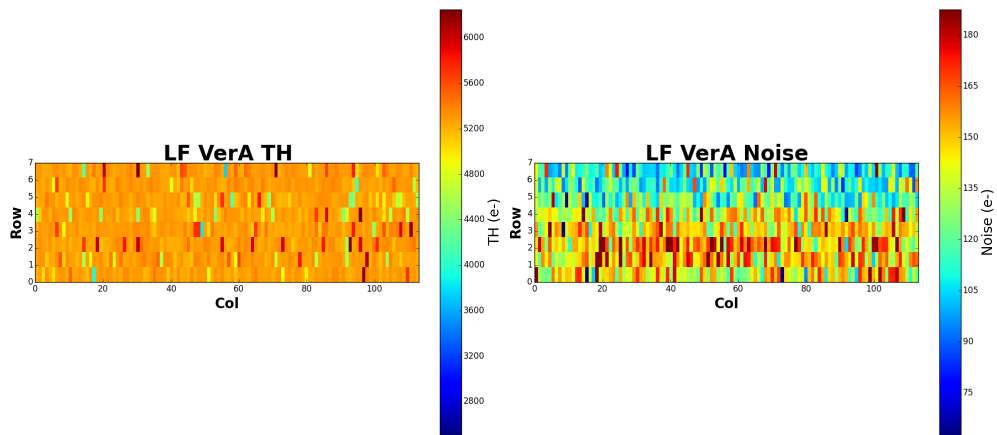


Figure 5.84 – Threshold and noise maps after tuning for ELT pixels before TDAC tuning, one pixel enabled mode.

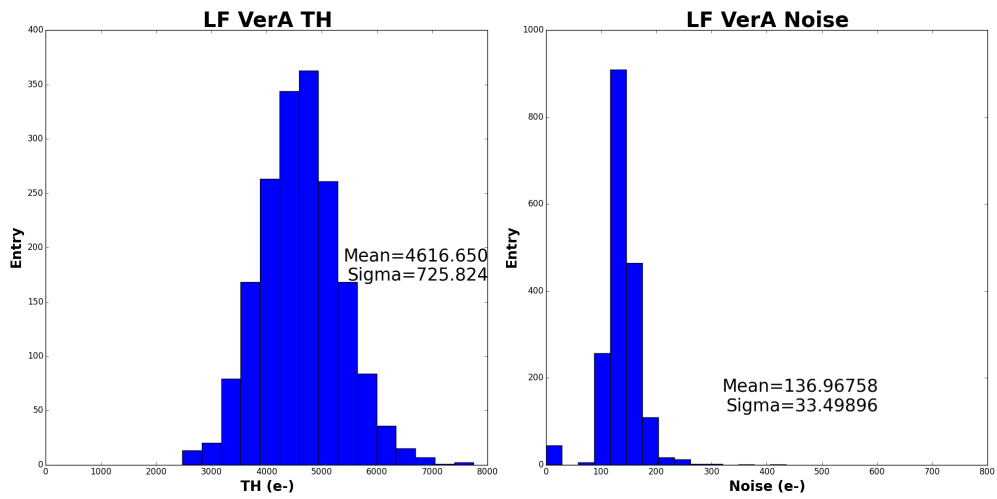


Figure 5.85 – Threshold and noise distributions before tuning for Lin pixels before TDAC tuning, one pixel enabled mode.

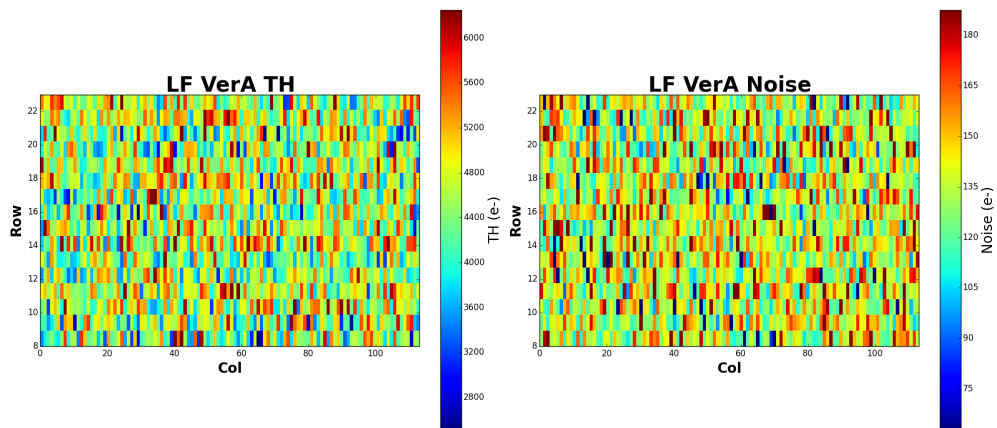


Figure 5.86 – Threshold and noise maps before tuning for Lin pixels before TDAC tuning, one pixel enabled mode.

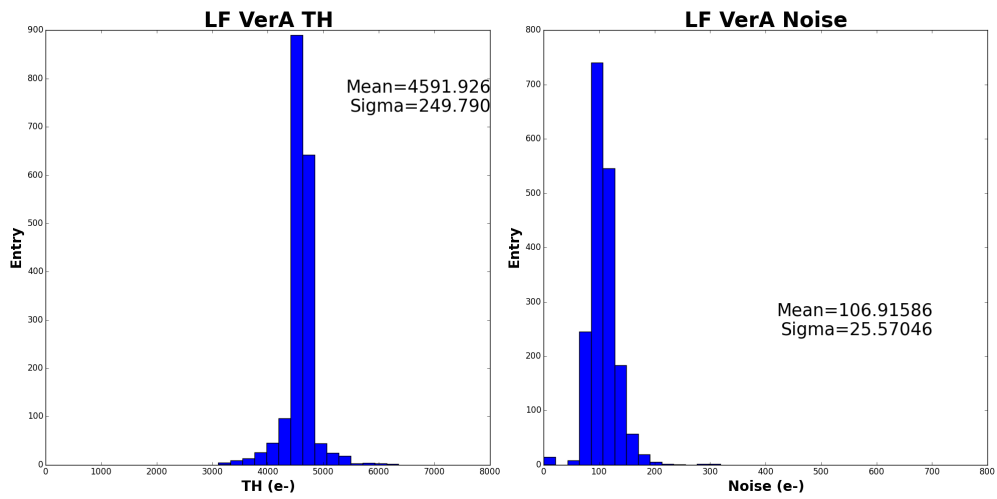


Figure 5.87 – Threshold and noise distributions after tuning for Lin pixels before TDAC tuning, one pixel enabled mode.

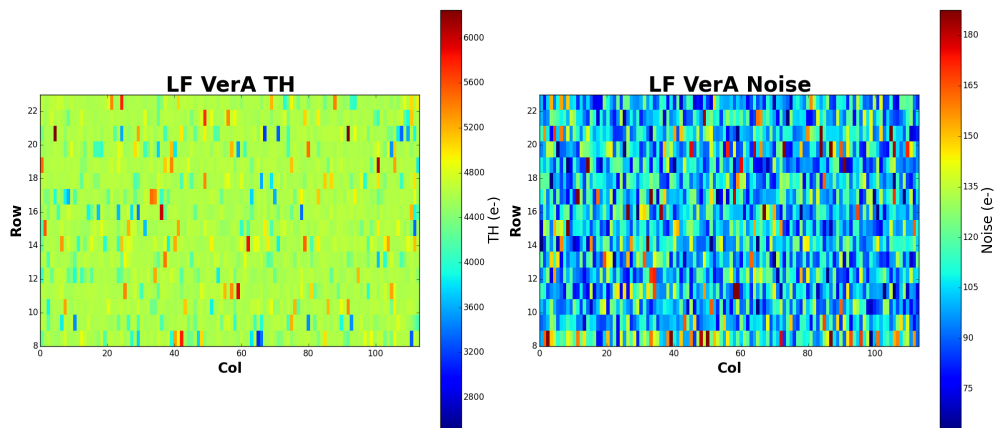


Figure 5.88 – Threshold and noise maps after tuning for Lin pixels before TDAC tuning, one pixel enabled mode.

pixel enabled mode, one can see that the all pixel enabled mode results in a more uniform tuning. The threshold deviation for the ELT pixel reduces from 1074 to 158 electrons, and for the LIN pixels, it reduces from 1218 to 178 electrons. The electronics noise is roughly 130 electrons for the VA pixels.

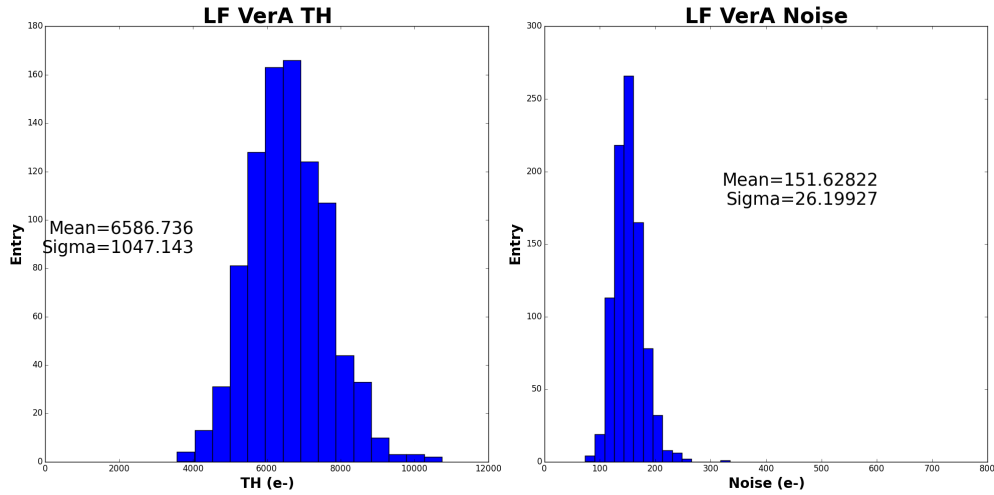


Figure 5.89 – Threshold and noise distributions before tuning for ELT pixels before TDAC tuning, all pixels enabled mode.

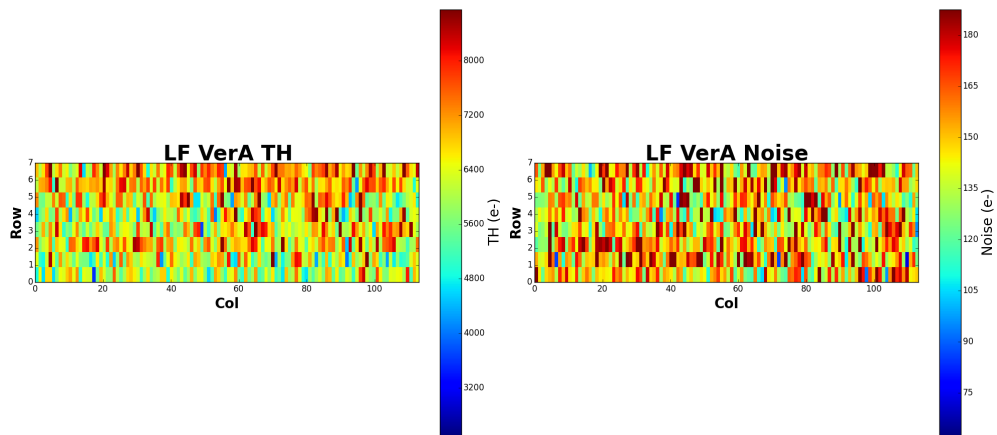


Figure 5.90 – Threshold and noise maps before tuning for ELT pixels before TDAC tuning, all pixels enabled mode.

The TDAC maps after tuning in one pixel enabled and in all pixels enabled mode are shown in Figure 5.97 to visualize the difference of chip working conditions. The more uniform tuning results reached in all pixels enabled mode reveals that the power distribution for individual pixel in the one pixel enabled

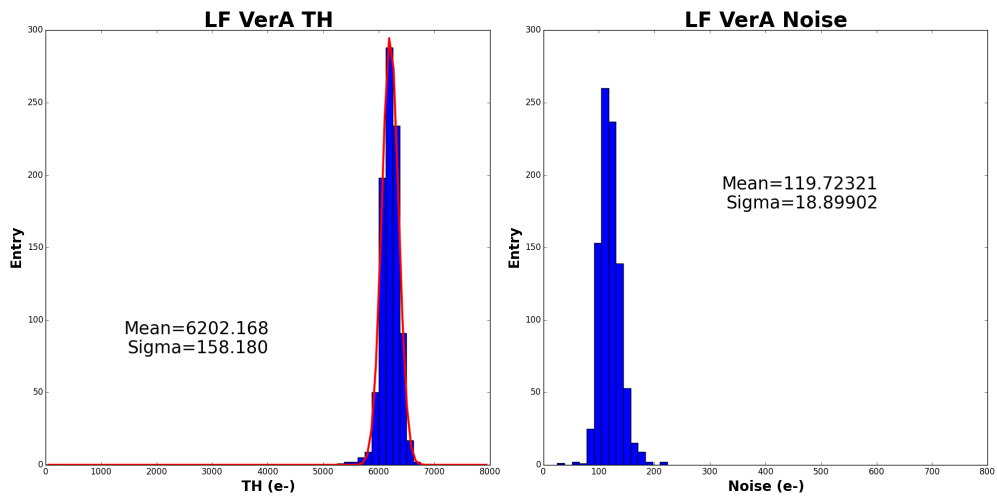


Figure 5.91 – Threshold and noise distributions after tuning for ELT pixels before TDAC tuning, all pixels enabled mode.

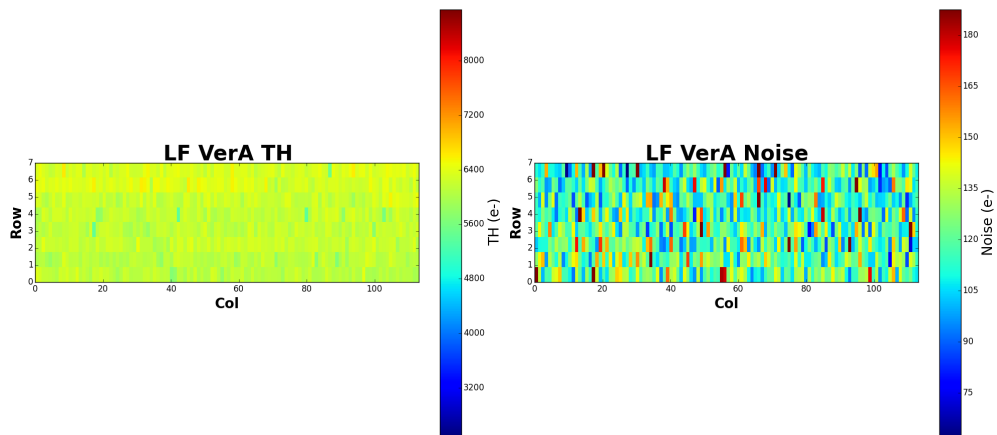


Figure 5.92 – Threshold and noise maps after tuning for ELT pixels before TDAC tuning, all pixels enabled mode.

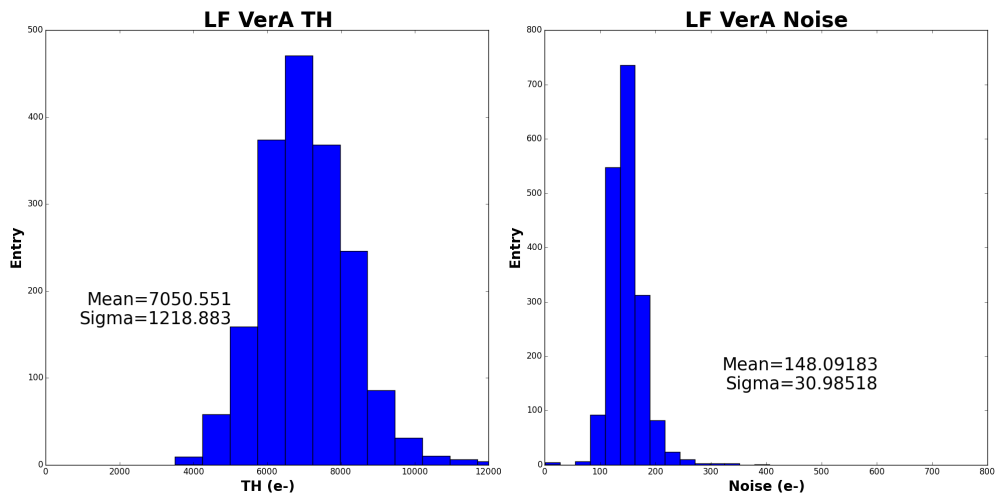


Figure 5.93 – Threshold and noise distributions before tuning for Lin pixels before TDAC tuning, all pixels enabled mode.

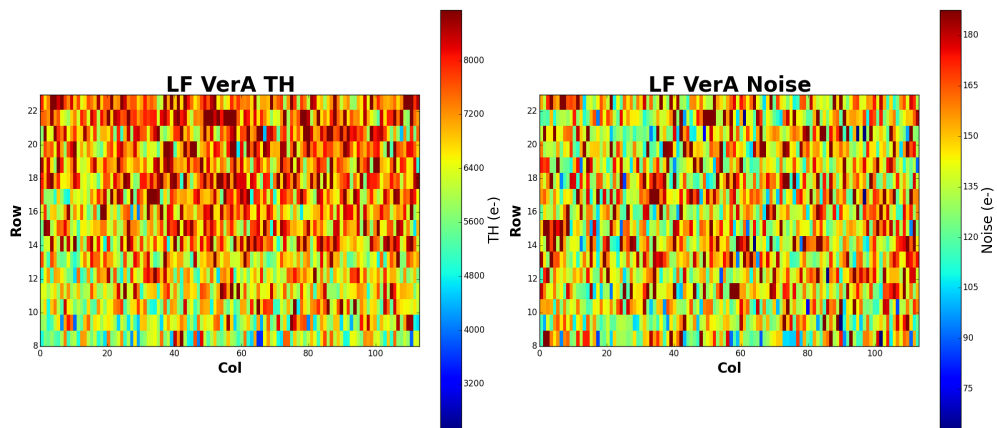


Figure 5.94 – Threshold and noise maps before tuning for Lin pixels before TDAC tuning, all pixels enabled mode.

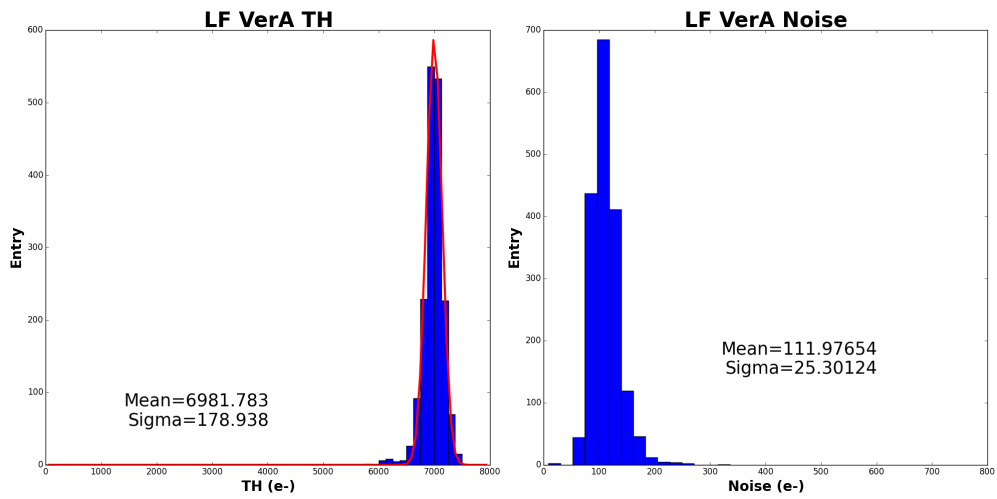


Figure 5.95 – Threshold and noise distributions after tuning for Lin pixels before TDAC tuning, all pixels enabled mode.

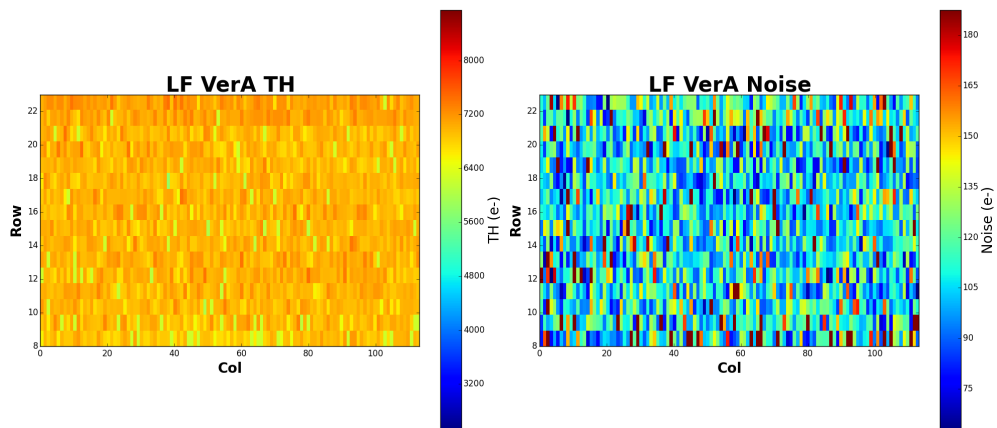


Figure 5.96 – Threshold and noise maps after tuning for Lin pixels before TDAC tuning, all pixels enabled mode.

mode might be unbalanced. One should pay attention to the power distribution particularly for a future large matrix.

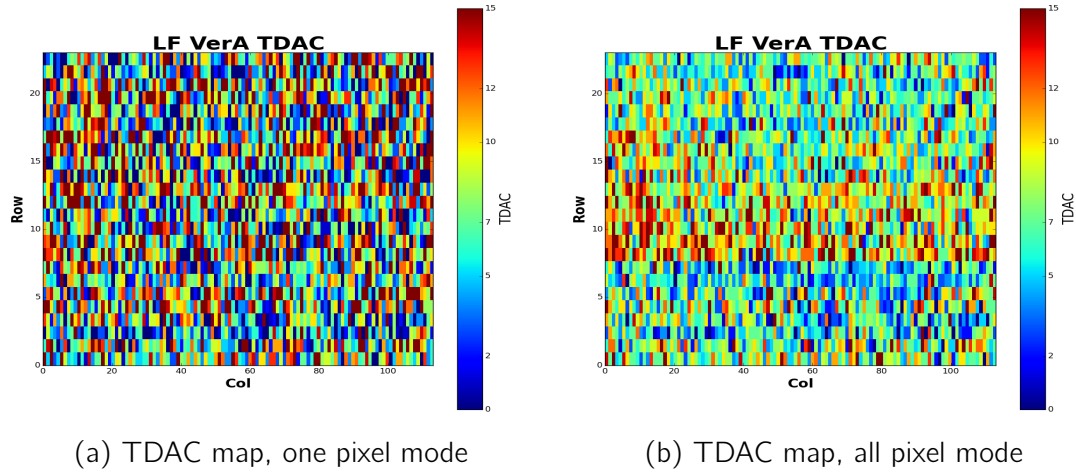
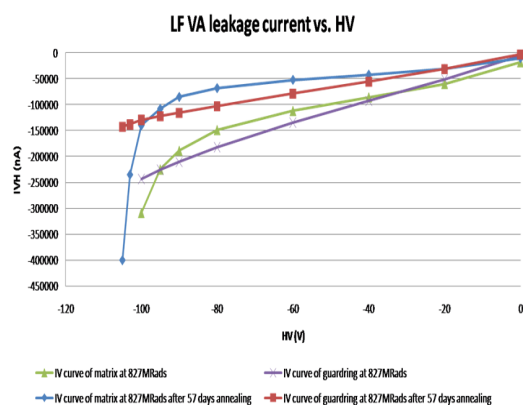


Figure 5.97 – TDAC values comparison between one pixel enable and all pixel enable mode.

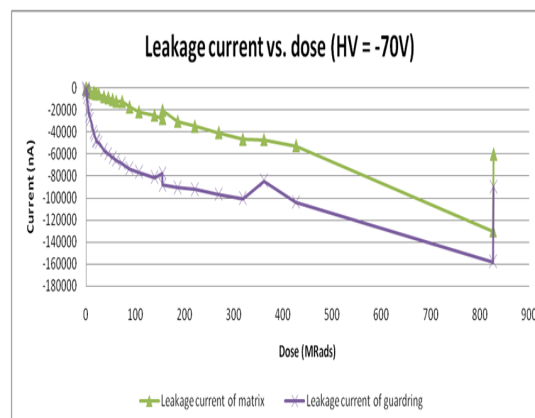
In order to investigate the radiation hardness of the LF technology, VA samples were irradiated with 24 GeV protons at room temperature up to a TID of 827 MRads. The leakage current of the matrix and of the guard-ring were measured during irradiation. The leakage currents as a function of voltage at the final dose and 57 days room temperature annealing are shown in Figure 5.98a. The breakdown voltage increased from 76 V pre-irradiation to 100 V after 827 MRads. The leakage current variations with dose for the matrix and the guard-ring at HV = -70 V are shown in Figure 5.98b. The leakage current of the matrix increased to $\sim 128 \mu A$ (47 nA/pixel) after 827 MRads, but reduced to $\sim 60 \mu A$ (22 nA/pixel) after 57 days room temperature annealing.

During the irradiation, the discriminator outputs were monitored. Six pixels (two pixels for each flavor) were measured. The first two L0.9 pixels were unresponsive after 100 MRads. Therefore, we have changed to two other L0.9 pixels after 100 MRads. Figure 5.99 shows the counting rate as a function of dose. The counting rate reduced by a factor of 10 after around 5 MRads. The dramatic drop in the counting rate is thought to be essentially due to the loss of diffusion charges as indicated by the TCAD simulations in Section 4.3.2.4 and by the test beam results. This mechanism should be investigated further.

A threshold scan was also performed during irradiation for the pixels under study. The threshold and noise extracted from the threshold scan are shown in Figure 5.100. The threshold of the pixels with ELT feedback increases with increasing dose level. The threshold of pixels with linear transistors keeps stable. The shift of threshold can be adjusted by TDAC. The noise increased by approximately a factor of 2 after 827 MRads.



(a) Leakage current vs. HV



(b) Leakage current vs. dose

Figure 5.98 – (a) : The leakage current of the matrix and of the guard-ring as a function of the high voltage. The leakage currents reduced after annealing as we expected. (b) : The leakage current of the matrix and of the guard-ring as a function of the dose.

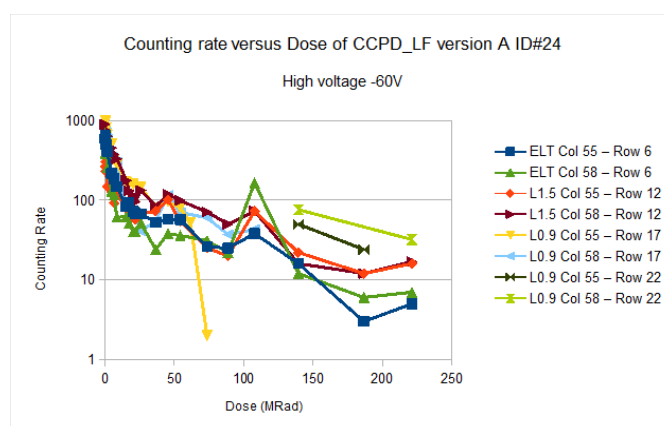


Figure 5.99 – LF CCPD VA counting rate at room temperature as a function of TID

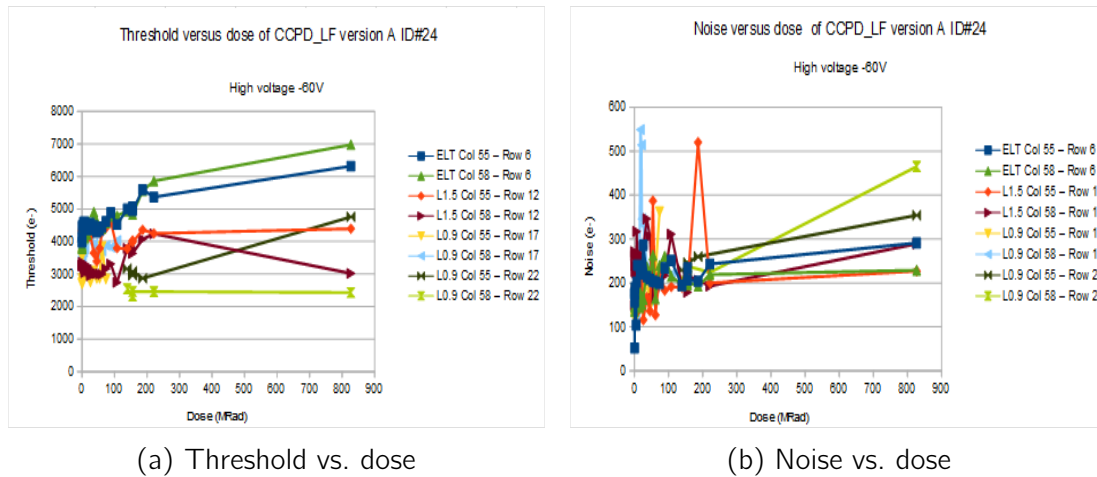


Figure 5.100 – (a) : TH as a function of dose. (b) : Noise as a function of dose.

After 220 MRads, all pixels were unresponsive but had normal power consumption and sensor leakage current. This malfunction was caused by the damaged comparator board which did not cope with the high dose recorded in the irradiation zone. After 57 days room temperature annealing, the preamplifier and discriminator signals were measured directly on the DUT board through oscilloscope, as shown in Figure 5.101. Both the preamplifier and the discriminator are responsive after 57 days room temperature annealing once the total dose of 827 MRads was recorded, but the amplitudes have strongly degraded with respect to pre-irradiation behavior. The discriminator amplitude is roughly 20 mV, whereas it is around 500 mV before irradiation. The degradation is probably due to the analog buffer inside the chip, which was too weakly designed with respect to radiation.

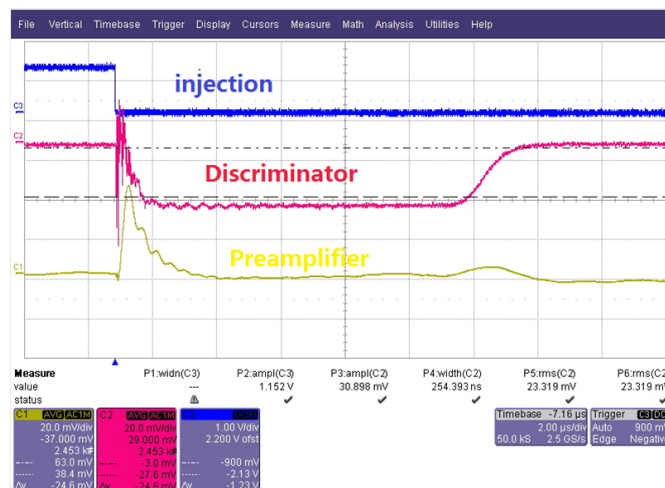


Figure 5.101 – LF CCPD VA responses after annealing

Two LF CCPD VA samples (back-side process, $100\ \mu\text{m}$ thickness) were irradiated with 24 GeV protons at $-20\ ^\circ\text{C}$ to 100 MRads in order to explore the temperature effects for radiation damage. The two samples were mounted on the lid of cold box. The boards were tilted to 4° with respect to the horizontal direction in order to have a uniform dose rate for the rather large chips, as shown in Figure 5.102. During irradiation, the high voltage was applied from the top-side.

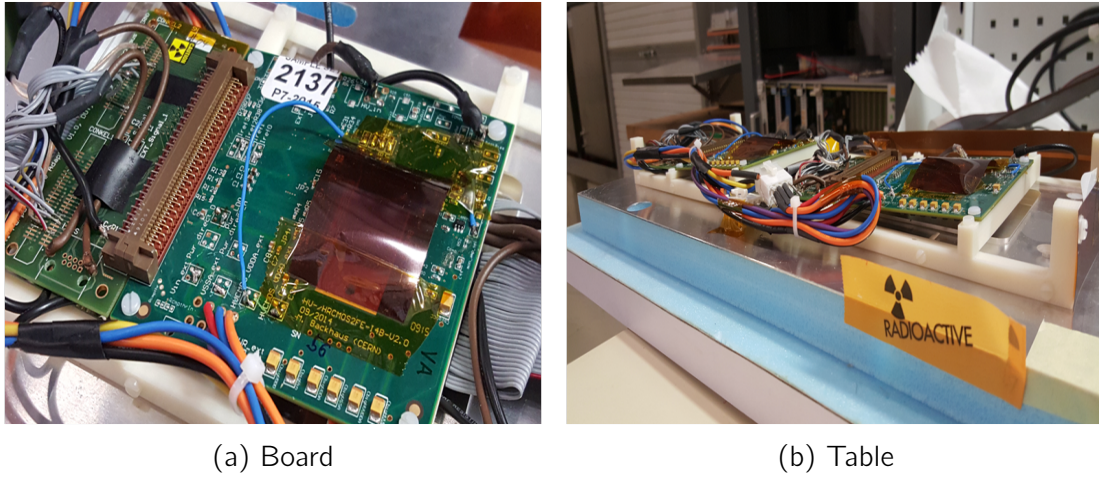


Figure 5.102 – LF CCPD VA low temperature proton test setup

The leakage currents of the matrix and of the guard-ring as a function of dose for both two samples are shown in Figure 5.103. Both two chips show similar

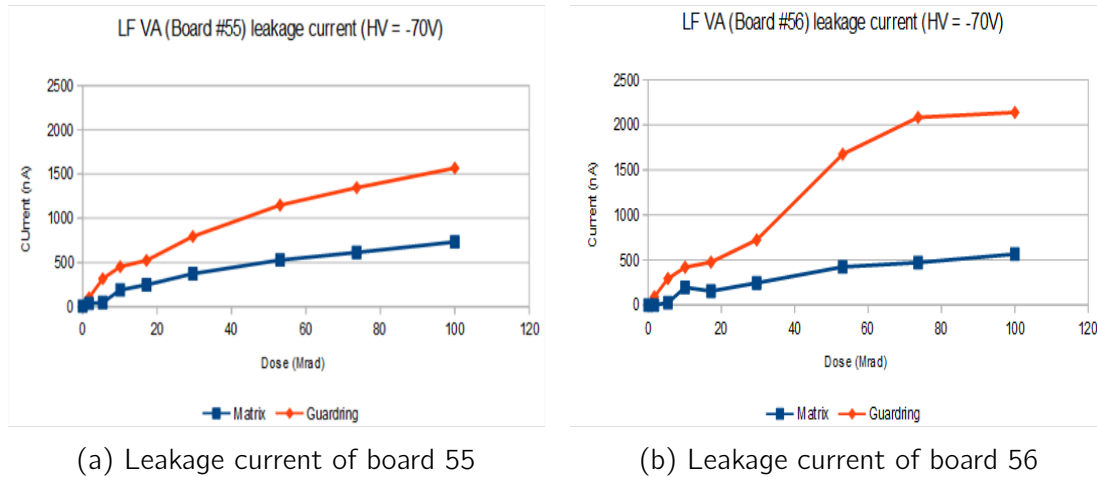


Figure 5.103 – Leakage current as a function of dose for both samples at $-20\ ^\circ\text{C}$.

leakage current degradation profile as a function of the integrated dose. The comparison of the leakage current between room temperature and $-20\ ^\circ\text{C}$ is also shown in Table 5.5.

Table 5.5 – Leakage current at 100 MRads

Board	24 (room temperature)	55 (-20°C)	56 (-20°C)
Matrix current (nA)	21430	732	565
Guardring current (nA)	76390	1568	2138

The counting rate variations for both samples as a function of dose are shown in Figure 5.104. Both two chips show very similar behavior and also correlated with room temperature results. A strong reduction of the counting rate is seen

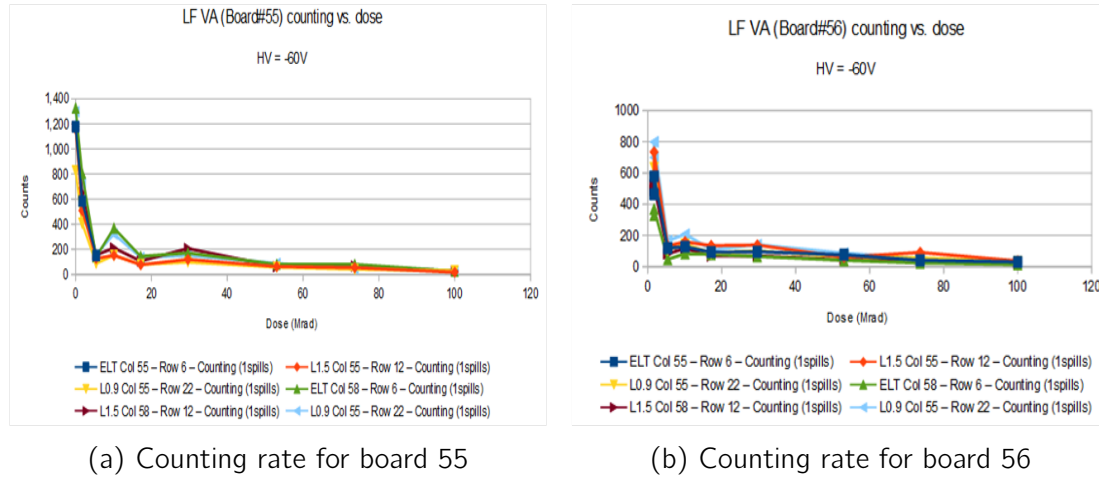


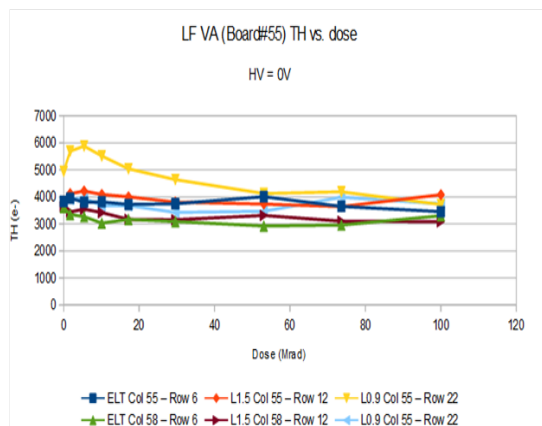
Figure 5.104 – Evaluation of the counting rate as a function of dose for both samples at -20°C .

after approximately 5 MRads. Then the counting rate rather steadily decreases until the final 100 MRads dose is reached. The samples were moved to the so-called park position (15 cm away from the beam center) to detect the particles from the beam halo. Therefore the impinging particles had small angles with respect to the chip surface. Many charges ionized by the impinging particles located near the monitored pixel could be collected by diffusion when the sensor was not irradiated. However, approximately 43% diffusion charges were lost due to the bulk damages when the fluence is $1 \times 10^{14} \text{ n}_{eq} \cdot \text{cm}^{-2}$ as shown in Table 4.8. This could explain the counting rate reduction before 5 MRads.

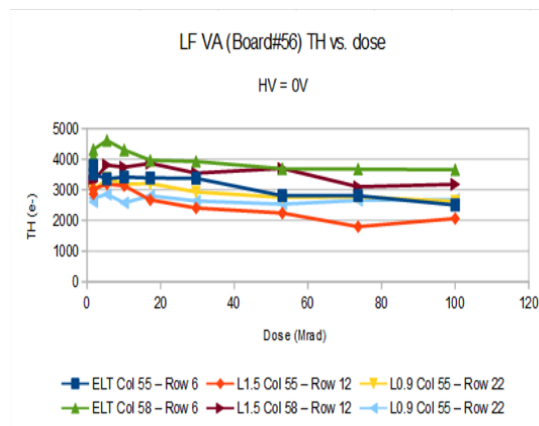
The threshold and noise as a function of the recorded dose are shown in Figure 5.105 and 5.106 for both two samples. The thresholds do not have significant variations up to 100 MRads for both samples and the noises are also rather stable at an average 160 electrons for both chips.

The threshold scan for the matrix was performed for both chips after each irradiation step. The threshold, noise distribution and maps at 5 MRads and 100 MRads for these two chips are shown from Figure 5.107 to 5.114.

In both cases, the threshold and noise reduced after 100 MRads. The average

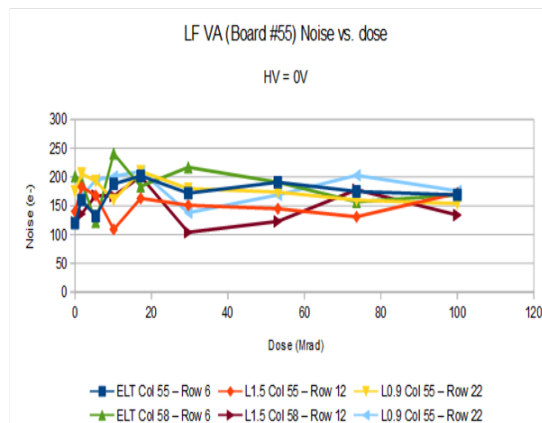


(a) Threshold of board 55

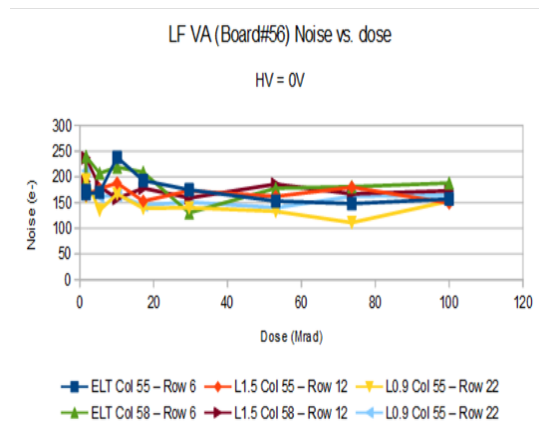


(b) Threshold of board 56

Figure 5.105 – Threshold as a function of dose for both samples at $-20\text{ }^{\circ}\text{C}$ in 24 GeV protons irradiation environment.



(a) Noise of board 55



(b) Noise of board 56

Figure 5.106 – Noise as a function of dose for both samples at $-20\text{ }^{\circ}\text{C}$ in 24 GeV protons irradiation environment.

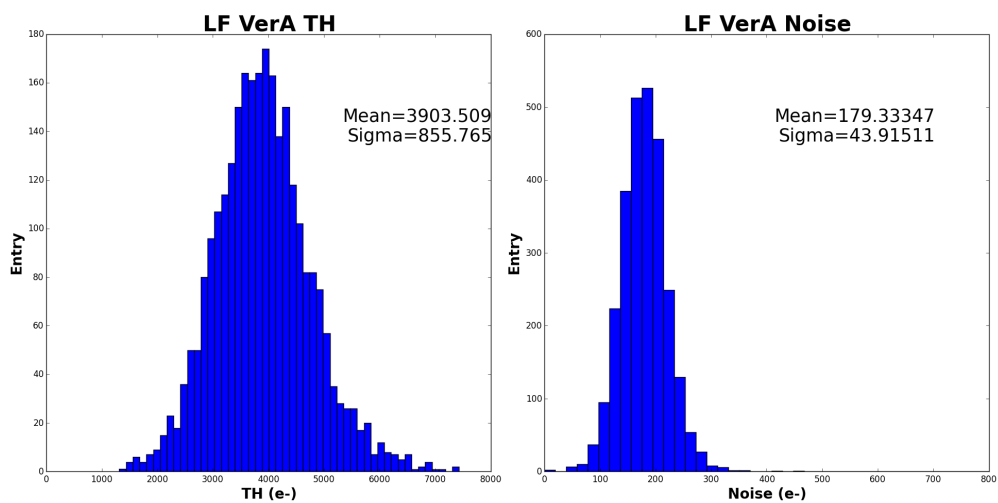


Figure 5.107 – Threshold and noise distributions for board 55 at 5 MRads, one pixel enabled mode.

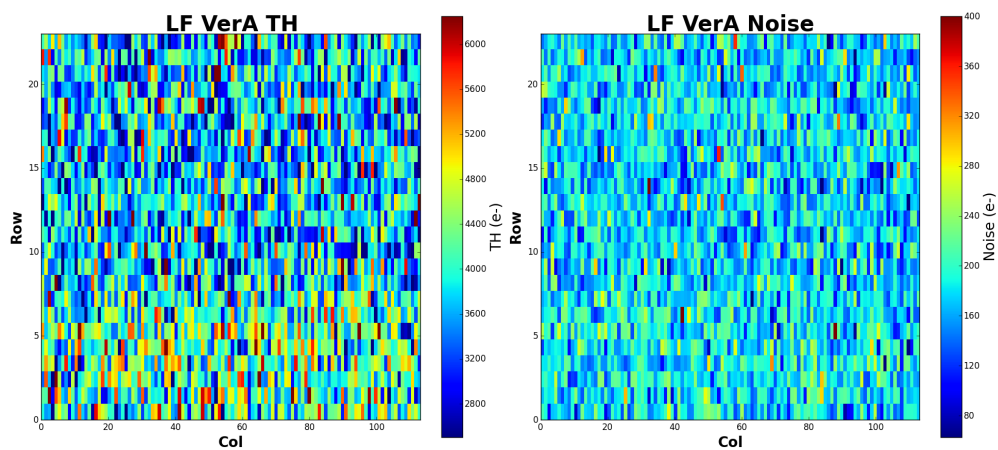


Figure 5.108 – Threshold and noise maps for board 55 at 5 MRads, one pixel enabled mode.

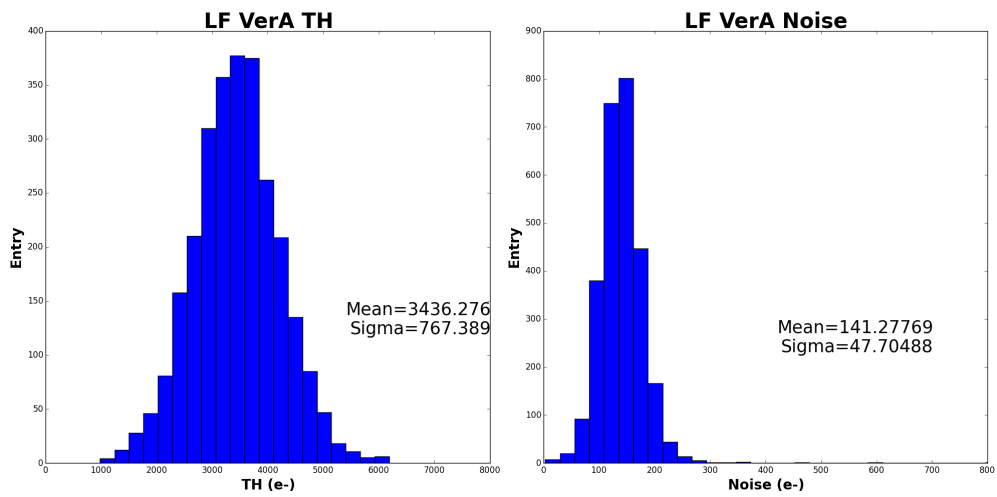


Figure 5.109 – Threshold and noise distributions for board 55 at 100 MRads, one pixel enabled mode.

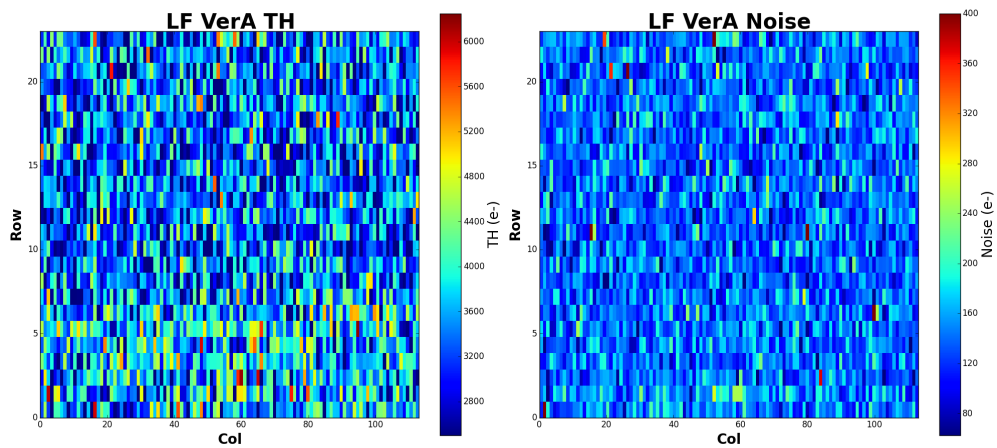


Figure 5.110 – Threshold and noise maps for board 55 at 100 MRads, one pixel enabled mode.

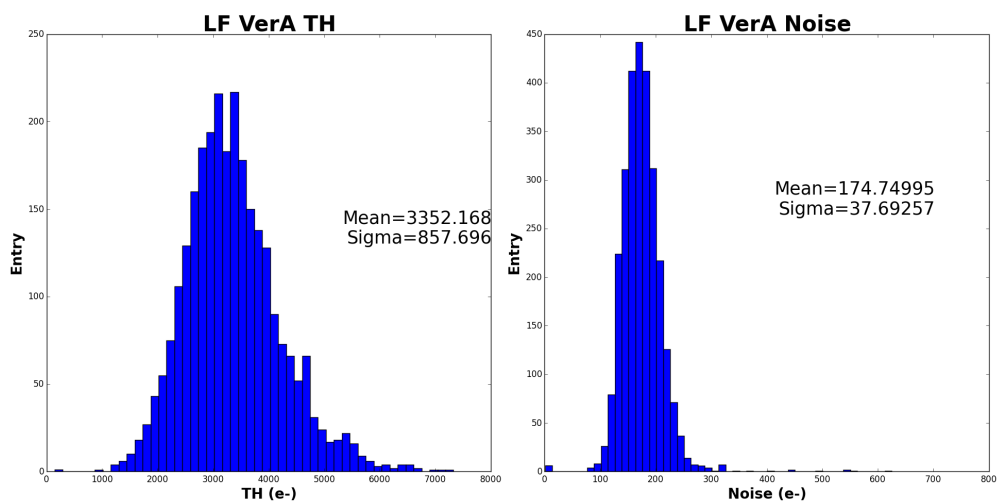


Figure 5.111 – Threshold and noise distributions for board 56 at 5 MRads, one pixel enabled mode.

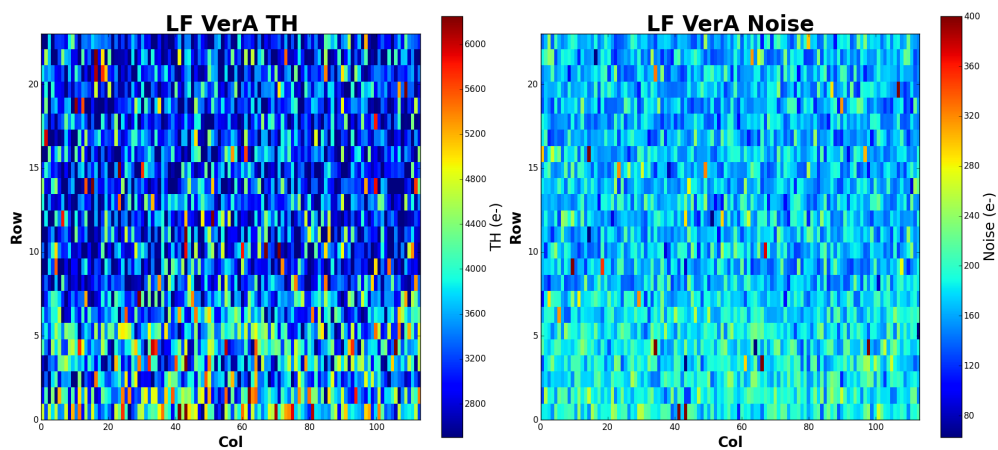


Figure 5.112 – Threshold and noise maps for board 56 at 5 MRads, one pixel enabled mode.

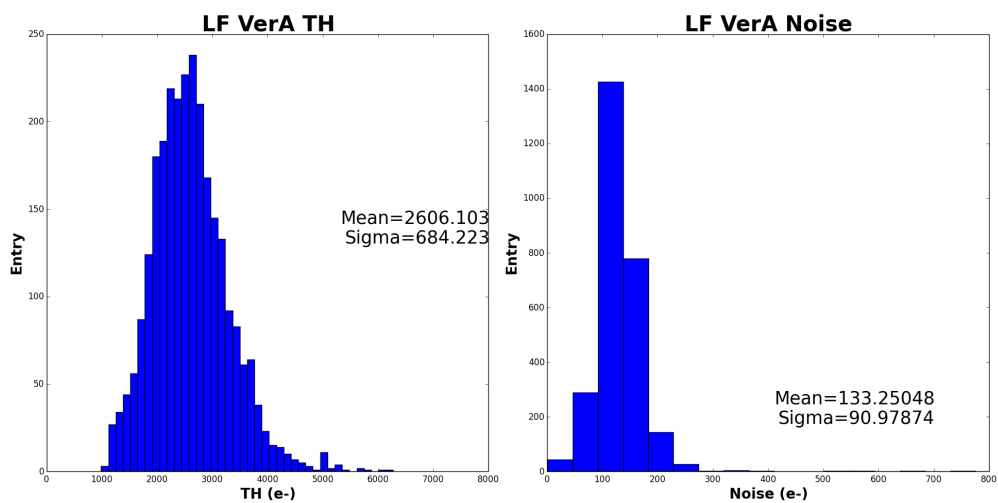


Figure 5.113 – Threshold and noise distributions for board 56 at 100 MRads, one pixel enabled mode.

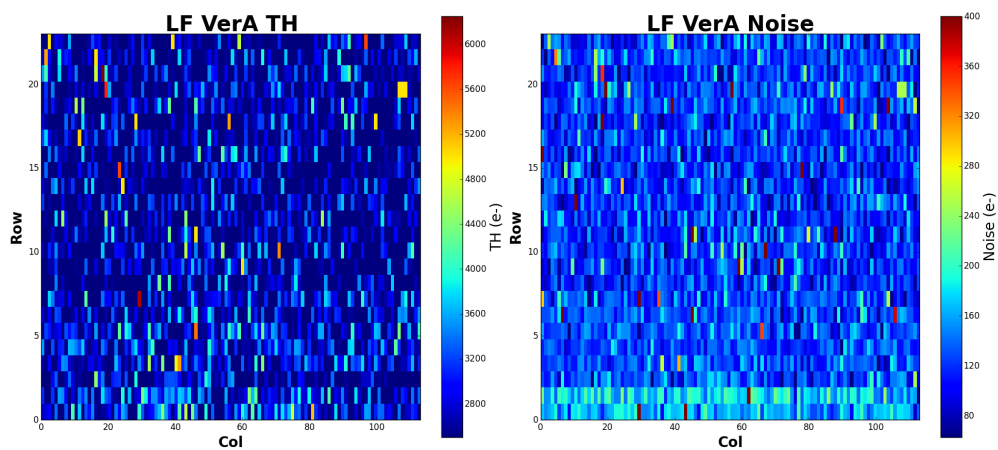


Figure 5.114 – Threshold and noise maps for board 56 at 100 MRads, one pixel enabled mode.

threshold and noise variations as a function of the dose for both chips are summarized in Figure 5.115. After 100 MRads, the threshold reduced by 13% and

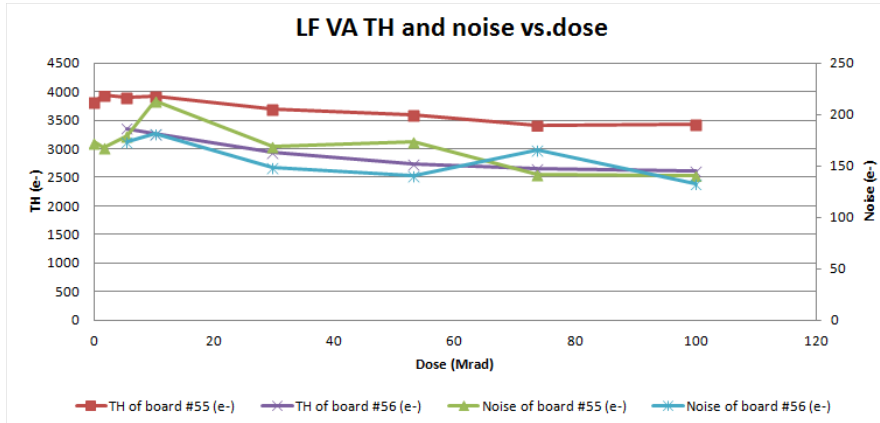


Figure 5.115 – LF CCPD VA threshold and noise variation as a function of dose.

the noise reduced by 18% compared with the initial values at -20°C . The reduced threshold and noise is probably due to a change in input sensor capacitance affected by the irradiation. This behavior needs to be carefully investigated in the future irradiation campaigns.

A new large demonstrator LF CPIX using LF 150 nm technology has been submitted in March of 2016. The reticles of this submission is shown in Figure 5.116. Two matrix versions, V1 and V2, and one test structure were designed in this

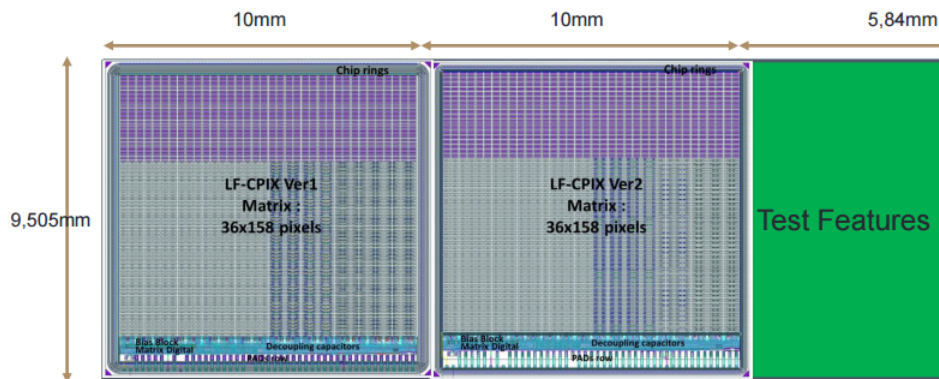


Figure 5.116 – LF CPIX reticles

submission. The V1 and V2 have the same electronics inside the pixels. The pixel size is the same as the FE-I4, $50\text{ }\mu\text{m} \times 250\text{ }\mu\text{m}$. The matrix consists of three pixel flavors : “passive”, “digital” and “analog” pixel. Only the charge collection sensor was implemented for the “passive” pixel. The “digital” pixel has a similar electronics but some modifications have been brought to this version with respect to the previous prototypes which have been discussed in Section 5.2.3. The

“analog” pixel has only a preamplifier implemented in the pixel. A new guard-ring strategy was used in V2 to increase the breakdown voltage and reduce the inactive region. Improved electronics performance and better charge collection efficiency are expected.

Conclusion

In this PhD thesis research work, TCAD simulations for the GF BCDlite 130 nm and LF 150 nm technologies have been performed. For the sensor pixel structure, 3D TCAD simulations have been carried out to investigate the depletion, breakdown voltage, leakage current, capacitance as well as the charge collection behaviors for both two kinds of technologies. 2D guard-rings simulations were also performed for the high resistivity substrate prototypes in order to increase the breakdown voltage and reduce the inactive areas. For these kinds of radiation hard HV/HR CMOS prototypes, both the NIEL and TID effects were included in the simulations. The simulations can predict and reproduce some of the characterization results, for instance the breakdown voltage, charge collection efficiency, etc. However, some of the simulations cannot agree with the measurements for the p-type substrate prototypes particularly after heavy irradiation, such as the enlarged depleted region at specific irradiation dose ranges (results from the edge-TCT measurements). More efforts should be performed to explore and tune the corresponding physics models.

Test setup developments and characterizations of the HV/HR CMOS prototypes were also part of this thesis. The data acquisition programs, in particular dedicated to the proton test beams, X-ray sources and threshold tuning, have been implemented into various test setups. Several HV/HR CMOS prototypes developed in three HV/HR technologies, AMS 0.18 μm HV, GF BCDlite 130 nm and LF 150 nm, have been characterized. Four versions of AMS prototypes have been characterized. The AMS V4, the latest version, can detect both the ^{55}Fe and the ^{90}Sr signals after 1 GRad X-ray irradiation. Both the preamplifier and the discriminator were responsive up to 560 MRads 24 GeV proton irradiation. Compared to the previous three AMS prototypes, the ELTs implementation in the critical region for the preamplifier and the modified pixel guard-rings for the AMS V4 have shown better radiation tolerance in terms of the amplitude of the preamplifier, the electronics noise and the sensor leakage current. One GF prototype has also been tested. The GF prototype showed a good radiation hardness behavior up to 1 GRad X-ray irradiation, but a low MIP detection efficiency due to not enough depleted region and some minor design defects. Improved detection efficiency is expected by using high resistivity (HR) substrate and modified designs in the future. The GF HV2FEI4 assembly also showed good communication between the sensor and the FE-I4. The sub pixels have been successfully

decoded by the FE-I4 which results in a better spatial resolution with respect to the current ATLAS planar sensor. The epoxy glue thickness that was used for AC coupling was also extracted for the GF HV2FEI4 assembly. Two versions of the LF prototypes are being characterized. They are the first two prototypes using high resistivity substrate. The samples were irradiated to 827 MRads at room temperature and to 100 MRads at $-20\text{ }^{\circ}\text{C}$. Lower leakage current was observed as expected at $-20\text{ }^{\circ}\text{C}$. The electronics was responsive and there was no significant variation after these doses. Efficiency tests using test beam telescope and LF HV2FEI4 assembly tests will continue to be performed. A large threshold dispersion was observed for the matrix through the threshold scan. This problem has been identified and has been corrected for the next CPIX demonstrator submission in March 2016. Some modifications have been brought to this CPIX demonstrator with respect to the characterizations of the LF prototypes, and an improved electronics performance and better charge collection efficiency are expected. Such large size matrix, approximately $1\text{ cm} \times 1\text{ cm}$, could be a demonstrator for the technology which could be used in the pixel detectors for the future ATLAS ITk.

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