

Diese Arbeit wurde vorgelegt am I. Physikalischen Institut B

Optimization Studies and Development of Test Procedures for Service Hybrids of CMS Silicon Modules at HL-LHC

Masterarbeit in Physik

von

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vorgelegt der

Fakultät für Mathematik, Informatik
und Naturwissenschaften der RWTH Aachen

im Oktober 2018

angefertigt bei

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1 Motivation

The CMS¹ experiment is one of the four major experiments at the world's largest particle accelerator LHC². It is located at the French-Swiss border close to Geneva. The CMS detector is capable to detect and record the products of the LHC's proton-proton collisions with a centre-of-mass energy of up to 13 TeV. The products' path of flight, energy, charge, and momentum are reconstructed. The detector contributed greatly to the discovery of the Higgs boson in 2012, one of the last missing pieces in the standard model of particle physics [1, 2].

To constantly enable new studies and improve the performance, the LHC is upgraded in multiple stages. A long shutdown (2013 to 2014) and an extended technical stop at the end of 2016 have already concluded. Two more long shutdowns will follow, which will last from 2019 to 2020 and from 2024 to 2026. These will result in an increase of the number of colliding particles as well as the centre-of-mass energy. The experiments will be upgraded in parallel to match the increasing requirements.

The studies presented in this Master's thesis were conducted in the course of the Phase-2 tracker upgrade of the CMS detector, which is scheduled to be conclude at the end of the third long shutdown in 2026. This upgrade covers the replacement of the full silicon tracker, which is made up of the pixel detector and the outer tracker. An operation of the current tracker after 2026 would lead to severe data losses, e.g. due to radiation damage. An increase in resolution, acceptance, and a smaller material budget are also foreseen. In addition, tracker information will contribute to the Level-1 trigger in the future. Due to the increase in collision rate inside the detector, the tracker needs improvements in radiation tolerance and event discrimination.

For this task, the so-called 2S and PS modules were developed for the outer tracker. These carry not a single silicon sensor, like the current tracker modules, but either two strip sensors or a macro-pixel and a strip sensor with a few millimetre spacing. This enables the recognition of particles with a high transverse momentum already on the level of the module's readout electronics. This information can be utilized by the Level-1 trigger. Service hybrids are responsible for the electrical power distribution and the module's data communication. The I. Physikalisches Institut B of the RWTH Aachen University is driving the development of the service hybrids. Major components are two-staged DC-DC converters and a serializer-deserializer ASIC. The use of DC-DC converters, which reduce the supply voltage for the module electronics, is necessary to keep losses on the supply cables low. The room for supply cables is limited and the amount of material inside the tracking volume needs to be reduced.

The DC-DC converters' efficiency and noise properties depend critically on the choice of their main inductor. The inductor of choice is a toroidal air-core coil with an inductance of about 100 nH, which geometric parameters and material have been explored in the course of this thesis. The functionality of each tracker module relies on a fully functional service hybrid. With a total of roughly 13,300 modules needed for the outer tracker upgrade, testing of all service hybrids becomes a major task during module production. An appropriate infrastructure for testing needs to be developed. A first prototype of a test board for the 2S service hybrids has been commissioned in my studies.

¹Compact Muon Solenoid

²Large Hadron Collider

After a short introduction to the CMS experiment at the LHC and to the scheduled upgrades, the module designs will be presented. In particular, I will introduce the service hybrids and their respective tasks for both module types. One of the two main chapters is concerned with the development of toroidal coils for the service hybrids' DC-DC converters. This includes simulations and measurements of coil parameters of inductor prototypes. Measurements with a converter evaluation board, which test the converter's characteristics in dependence of the main inductor's parameters, will also be presented. The second main chapter includes the commissioning of test board prototypes for a 2S service hybrid test system. The layout and operation of the test board will be discussed. In addition, measurements, that prove the functionality of the layout will be presented. A graphical user interface and a cooling system will be described.

2 Introduction

2.1 CMS experiment at the LHC

The LHC is a particle accelerator at the European Organization for Nuclear Research CERN¹ near Geneva in Switzerland. The accelerator, buried roughly 100 metres deep in-between Lake Geneva, the Jura Mountains and Cessy (France), provides protons (or by choice lead nuclei) for collisions. It is housed inside a 27 kilometre long tunnel. Previously, the tunnel contained the Large Electron Collider (LEP). The LHC supplies four major experiments. The ATLAS² and the CMS experiment consist of multi purpose detectors. They have a wide range of study. The two smaller experiments LHCb³ and ALICE⁴ have a tighter field of study. LHCb concentrates on the study of bottom quarks and ALICE on heavy ion physics. The collider is the last station in a series of pre-accelerators. The linear accelerator LINAC2 accelerates the protons to an energy of 50 MeV. The next stages are the BOOSTER synchrotron (1.4 GeV), the proton synchrotron (26 GeV), and the super proton synchrotron (SPS, 450 GeV). The last step is the acceleration in the LHC to currently 6.5 TeV.

This thesis is concerned with the CMS experiment [3]. The structure is sketched in Figure 2.1. The experiment uses a right-handed coordinate system, with the origin at the nominal interaction point. The x -axis points to the centre of the LHC ring, while the y -axis points to the top, orthogonal to the ring's plane. The z -axis points counter-clockwise along the beam. The polar angle θ is measured from the positive z -axis and the azimuthal angle ϕ in the x - y -plane. The pseudorapidity η is defined as $\eta = -\ln[\tan(\frac{\theta}{2})]$, where θ is the polar angle in radians.

The main feature of the CMS experiment is a 13 m long, six metres wide superconducting solenoid. It consists of four layers of niobium-titanium windings with a total mass of 220 t and a working temperature of 1.8 K. Inside the solenoid, it produces a homogeneous magnetic field of 3.8 T. The tracks of charged particles are bend when they travel through the magnetic field and in this way their momentum can be determined. The magnet is embedded in an iron return yoke with integrated muon chambers. The muon system consists of three types of different gas-filled detectors. Drift tubes (DT) and resistive plate chambers (RPC) are used in the barrel region (the medium part of the detector, extending concentric and parallel to the beam axis). RPCs are also present in the endcaps (closing the barrel and orthogonal to the beam axis) together with cathode strip chambers (CSC). The in total 1,400 muon detectors make up an area of 25,000 m². The tracking system and the calorimeters for energy measurements are located inside the solenoid. In the barrel region, the innermost part ('inner tracker') consists of four layers of silicon pixel modules followed by layers of silicon strip modules ('outer tracker'). In the endcap region, three layers of pixel modules and three plus nine layers of strip modules are present. Some strip modules are placed back-to-back and have a stereo angle of about 100 mrad. This allows a coarse measurement of the z and r coordinate in the barrel and endcap respectively. The electromagnetic calorimeter (ECAL) is attached further outward. It is made up of lead-tungsten crystals. Their

¹Conseil Européen pour la Recherche Nucléaire

²A Toroidal LHC ApparatuS

³Large Hadron Collider beauty

⁴A Large Ion Collider Experiment

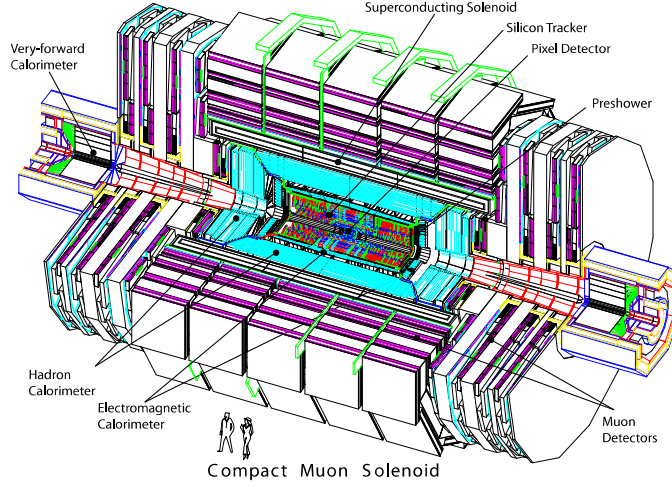


Figure 2.1: Schematic drawing of the CMS detector [3].

produced scintillator light is measured with avalanche photodiodes in the barrel and vacuum photo triodes in the endcap. The deposited energy can be calculated from the measured light. Last follows the hadronic calorimeter (HCAL). It consists of 14 layers of brass absorbers and 16 layers of plastic scintillator tiles. Their signal is transmitted via wavelength shifting and later optical fibres to optical decoder units and finally to hybrid photodiodes. An additional hadronic calorimeter (Hadron Forward, HF) is placed in beam direction behind the muon chambers. It consists of quartz fibres embedded in iron plates. Here the energy is determined via Cherenkov light. During collisions, the calorimeters and muon systems supply information to the Level-1 trigger, which features a trigger rate of about 100 kHz and 3.2 μ s latency. A computer cluster based high-level trigger makes a decision on recording an event. At the design luminosity, this is the case with a frequency of about 1000 Hz.

2.1.1 High-luminosity LHC

The LHC started operation in 2009. Data taking started with Run-1 from 2010 to 2012. With a centre-of-mass energy ($\sqrt{s}$) of 7 TeV, 45 pb^{-1} of integrated luminosity were recorded in 2010 and 6.1 fb^{-1} in 2011. In 2012 the centre-of-mass energy was increased to 8 TeV and 23.3 fb^{-1} of data were taken. After a multi-year long shut down (LS1), the LHC resumed operation with Run-2 and a centre-of-mass energy of 13 TeV, recording 4.2 fb^{-1} in 2015, 40.8 fb^{-1} in 2016, and 49.8 fb^{-1} in 2017. The instantaneous luminosity reached levels of around $2.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, doubling the design luminosity of $1.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. At the end of 2018 the LHC will be closed down during LS2 for two more years until it resumes operation in 2021 with Run-3. It is planned to continue to run until 2024, recording 300 fb^{-1} in the process. During LS3 (planned to last from 2024 to 2026) the accelerator infrastructure will be improved in order to achieve unprecedented luminosity levels. The project is titled HL-LHC for, High-luminosity LHC. A detailed time line can be found in Figure 2.2. Envisioned operational performance numbers are 5.0 to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ instantaneous luminosity, resulting in up to 300 fb^{-1} of data per year and a total of 3000 to 4000 fb^{-1} of data for the full accelerator lifetime. Collisions will occur with 25 ns spacing at $\sqrt{s}$ of 14 TeV. To reach such high luminosity, new radiation tolerant Nb_3Sn quadrupole magnets, resulting in a lower β^* (betatron amplitude at the interaction point) and

crab cavities, to achieve head-on bunch collisions, will be installed at the interaction points. The higher luminosity comes at the cost of a higher number of simultaneous collisions (pileup) during one bunch crossing. The maximum number of pileup events was about 80 during the 2017 run and is expected to rise to 140 at $5.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ instantaneous luminosity, or even 200 at the peak instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. The total ionizing dose after 3000 fb^{-1} will reach a 1 MeV neutron equivalent fluence of up to $2.3 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$, resulting in a challenging environment for all detector components [4].

To cope with the higher requirements, the CMS experiment is upgraded as well. Although the muon chambers themselves do not need to change, the DTs' and CSCs' front-end electronics will be replaced. This will improve radiation tolerance, readout speed, and general performance. In the forward region, the RCPs will be improved and new chambers with gas electron multipliers will be installed. The main goal is to enhance triggering, create redundancy, and higher reconstruction performance and acceptance.

In the barrel, the ECAL is improved to be operated at lower temperatures and equipped with new front-end electronics. These will allow the Level-1 trigger to use single crystal information. In the barrel HCAL, the hybrid diodes will be replaced with silicon photodiodes prior to LS3. During LS3, the calorimeter in the endcaps will be exchanged with a new combined electromagnetic and hadronic sampling calorimeter. It will be mainly composed of silicon pad sensors, accompanied by plastic scintillator tiles, which are read out by silicon photomultipliers. They are used in the outer parts of the hadronic section.



Figure 2.2: Overview of the time line for the HL-LHC upgrade [5].

2.2 Tracker upgrade

The original pixel detector has been replaced at the end of 2016. Currently installed are the Phase-1 pixel detector and the Phase-0 strip tracker. During their operation, radiation damage accumulates, resulting in a growing number of malfunctioning modules. To ensure proper data taking and to keep pace with the growing demands of the HL-LHC, the full tracker of the CMS experiment needs to be replaced during LS3. This so-called Phase-2 upgrade needs to fulfill the following requirements:

- The current tracker has been designed for 500 fb^{-1} of integrated luminosity. After the upgrade, all components must withstand a radiation dose corresponding to their position

in the detector and an integrated luminosity of 3000 fb^{-1} . The tracking volume will be kept at a temperature of -20°C . All components need to be continuously operational under these conditions.

- Layout and resolution have been optimized for a maximal number of 20 to 30 pileup events and an instantaneous luminosity of $1.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. These need to be improved to deal with a maximal number of 140 to 200 pileup events (at 5.0 to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ instantaneous luminosity, respectively). Track separation and pattern recognition need to be improved, too. Therefore, the outer (inner) tracker channels' occupancy needs to stay in the order of one percent (one per mill).
- To improve the performance and physics capability of the Level-1 trigger, tracking information is required to be incorporated. For this purpose, a higher data transmission bandwidth and data latency on the module side are required. The trigger bandwidth will rise from 100 to 750 kHz and the latency from 3.2 to 12.5 μs .
- For better calorimeter resolution and track finding, the amount of material inside the tracking volume needs to be reduced. In terms of radiation length the current maximal value depending on η of $1.4 X_0$ will decrease to about 0.8.
- The acceptance of the tracker improves up to $|\eta| = 4$, while it currently reaches a coverage of the pseudorapidity of up to 2.4 [4].

To meet these requirements, the tracker layout in Figure 2.3 was developed. The tracker is still divided into the inner and outer part. The inner part is composed of four layers of pixel modules in the barrel and twelve layers in the end caps. Pixel modules marked in green have two readout chips and yellow modules have four readout chips. The outer part hosts two kinds of modules, which carry two back-to-back sensors, the pixel-strip modules (PS, blue) and strip-strip modules (2S, red). Sketches of both modules are shown in Figure 2.4. In contrast to the Phase-0 outer tracker, the modules' two sensors do not yield a stereo angle. They are in fact parallel, in order to obtain on-module transverse momentum (p_T) information about traversing particles, which can be used for the Level-1 trigger. Particles with a high p_T only have a small curvature in the magnetic field of the detector. From the correlation between hits in the bottom and top sensor, high and low p_T particles can be distinguished. Figure 2.5 illustrates the concept. A particle hitting the first sensor opens a few strips wide window in the second sensor's readout electronics. If the particle has a high p_T , it will only bend slightly in the gap between the sensors. It will produce a hit inside the strip window. In this case, both hits will be forwarded as partial track ('stub') to the Level-1 trigger.

If the event is considered relevant after the combination of all stubs, calorimeter entries, and the information from the muon system, all tracker hits, also those failing the p_T requirement, will be read out. The concept is optimized for the detection of tracks of particles with a p_T of two or more GeV, which will be sent out at bunch crossing frequency (40 MHz).

The first three layers of the barrel are made up of PS modules, which have a macro-pixel sensor on the back side and a strip sensor on the top side. Depending on their position in the detector, the sensor spacing is 1.6, 2.6, or 4 mm. The outer three barrel layers are equipped with 2S modules with two strip sensors at a distance of 1.8 or 4 mm. The five endcaps are disk-like structures with PS modules for $200 \text{ mm} < r < 600 \text{ mm}$ and 2S modules for the outer part. Parts of the PS barrel layers need to be tilted in order to decrease geometric inefficiencies at large particle incident angles, while simultaneously using a small number of modules and little material. The main parameters of both module types are summarized in Table 2.1, which is extracted from the Technical Design Report (TDR) [4].

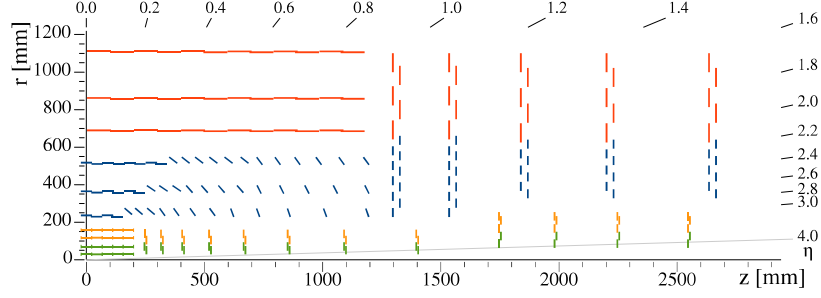


Figure 2.3: Sketch of a quarter of the CMS tracker design, which is foreseen for the Phase-2 tracker upgrade, in the r - z view. Pixel modules are shown in green and yellow, PS modules in blue and 2S modules are red. Part of the PS modules in the barrel are tilted to improve the geometric acceptance of the p_T approach, while simultaneously using a small number of modules and materials [4].

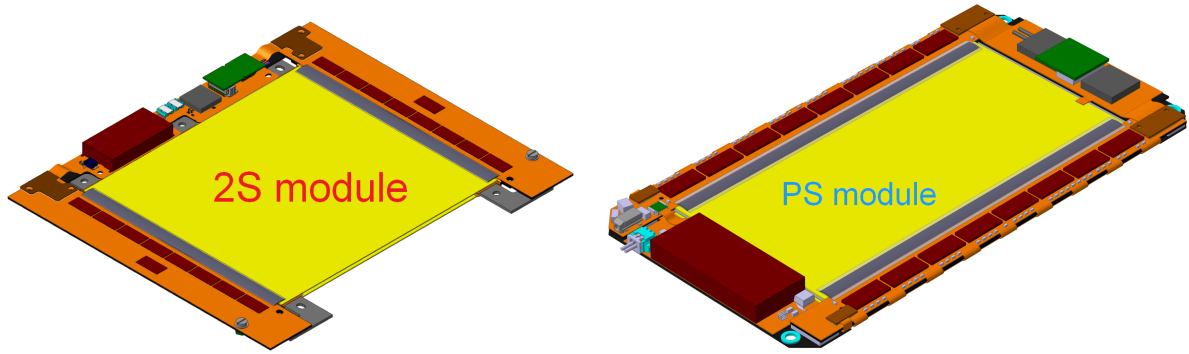


Figure 2.4: Sketch of a 2S (left) and PS (right) module for the CMS Phase-2 outer tracker. The 2S module hosts two strip sensors. The PS module hosts a macro-pixel sensor and a strip sensor [4].

2S module	PS module
$\sim 2 \times 90 \text{ cm}^2$ active area	$\sim 2 \times 45 \text{ cm}^2$ active area
2×1016 strips: $\sim 5 \text{ cm} \times 90 \mu\text{m}$	2×960 strips: $\sim 2.4 \text{ cm} \times 100 \mu\text{m}$
2×1016 strips: $\sim 5 \text{ cm} \times 90 \mu\text{m}$	32×960 macro-pixels: $\sim 1.5 \text{ mm} \times 100 \mu\text{m}$
Front-end power $\sim 5 \text{ W}$	Front-end power $\sim 8 \text{ W}$
Sensor power (-20°C) $\sim 1.0 \text{ W}$	Sensor power (-20°C) $\sim 1.4 \text{ W}$

Table 2.1: Main parameters of the 2S and PS module for the CMS Phase-2 outer tracker upgrade [4].

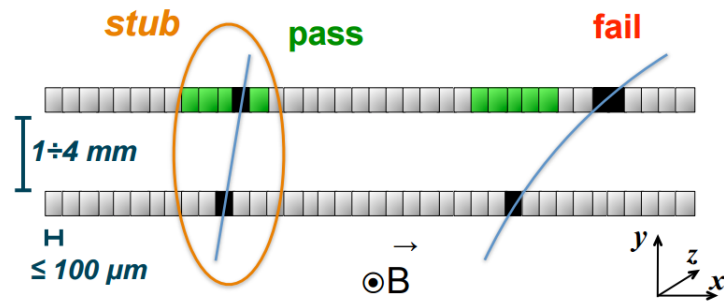


Figure 2.5: Illustration of the p_T module concept. Particles with low- p_T fail to hit a correlation window in closely spaced sensors. The green channels show the strips that need to be hit in order to form a ‘stub’ [6].

3 Service hybrids

Detailed information on the entire upgrade project and all its components can be found in the Technical Design Report [4]. Only the aspects necessary for this thesis will be discussed here. The topic of this thesis covers the service hybrids for the 2S and PS modules. Although the module design is quite different for both module types, due to the different sensors, the task of the service hybrids is largely the same. The design allows each module to operate independently. No additional panels for data or power aggregation are required inside the experimental volume.

3.1 2S module

A 2S module is composed of three main structures, as shown in Figure 3.1. The two silicon sensors (1) each have 2×1016 strips with a length of 5 cm and $90 \mu\text{m}$ pitch. The sensors are glued to supports made of an aluminium/carbon fibre composite. The strip length amounts to only half of the sensor length. Therefore, each half of the sensor is read out by the electronics on a separate front-end (FE) hybrid (2) at opposite sides of the module. However, one FE hybrid reads out the top and bottom sensors' half simultaneously in order to find stubs. This is achieved by wire-bonding the top sensor strips to the upper side of the FE hybrids and the bottom sensor strips to a flexible fold-over on the hybrids back side. The FE hybrids are laminated to a carbon fibre reinforced polymer (CFRP) stiffener. The service hybrid (3) is placed between both FE hybrids on one module side. It is responsible for the optical data transmission between module and back-end, the serialization of both FE hybrids' data streams, provides power for all readout and data transmission components, and filters and distributes the high voltage. The service hybrid is made up of a four-layer, high density, and flexible Kapton PCB, that is glued to a $500 \mu\text{m}$ thick carbon fibre stiffener. All of the carbon fibre based materials were chosen because of their high thermal conductivity in plane and their coefficients of thermal expansion, which are well matched to silicon.

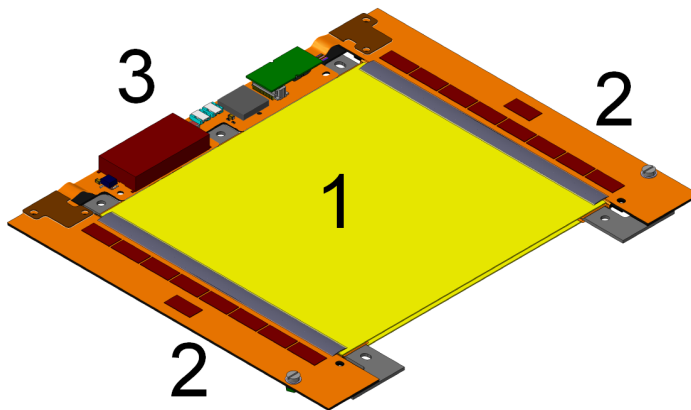


Figure 3.1: Sketch of a 2S module. Central features are the two silicon sensors (1), which are read out by the two front-end hybrids (2). The service hybrid (3) is placed at one side of the sensors, between the two front-end hybrids [6].

During collisions at the LHC, charged particles are produced amongst other remnants. When they pass through the high voltage depleted silicon sensors, they produce electron-hole pairs. In the 2S module, the induced charge is measured by the FE ASIC CBC¹. Eight CBC ASICs are placed on each FE hybrid. Their data are buffered, aggregated, and formatted by the CIC² ASIC. It acts as the FE hybrid's data hub to the service hybrid. The service hybrid covers all connections coming from and going to the counting room. The data of both FE hybrids are serialized via the LpGBT³ ASIC, which is placed on the service hybrid and also sends/receives data to/from the VTRx+⁴. The VTRx+ is an optoelectrical transceiver. It is connected to the counting room electronics via optical fibres. The LpGBT is also the module's I²C⁵ master and is therefore responsible for controlling, monitoring, and configuration of the FE ASICs. It contains monitoring features, like voltage and temperature measurement capabilities, too.

The numerous components on the modules need different supply voltages. The LpGBT, the CIC, the VTRx+, and the CBC have a nominal supply voltage of positive 1.25 V. The VTRx+ needs in addition positive 2.55 V. Both voltages are provided by a two-staged DC-DC conversion scheme, which is illustrated on the left in Figure 3.4. A DC voltage of around 11 V is applied to the 2S module. Two DC-DC converter ASICs, the bPOL12V⁶ and the bPOL2V5⁷, provide the desired 2.55 V and 1.25 V. The process is two-staged since the bPOL12V provides the input voltage for the bPOL2V5. The voltage conversion is necessary to allow a higher voltage on the supply cables. The available cable space is limited and the voltage drop along the cables goes linearly with the supply current, which drops linearly with a higher supply voltage. The power lost on the supply cable depends on the square of the current. Section 3.3 covers the DC-DC conversion in detail. The entire circuit associated with the DC-DC converters is summarized under the term low voltage (LV) circuit.

The negative sensor bias voltage is of the order of several hundred Volts and therefore referred to as the high voltage (HV). The HV filters and the connections to apply the voltage to the sensors are located on the bottom side of the service hybrid to save space on the top side. The part of the flexible PCB, which contains the HV circuit, is folded around the stiffener.

Figure 3.2 illustrates in more detail the entire module connectivity. The connections to the back-end enter the service hybrid on the right side. The connections are the LV power and the incoming and outgoing optical fibre (the HV connection is not shown). The 12 V LV is reduced by the DC-DC converters to 2.55 and 1.25 V and provided to the active components. The VTRx+ translates the optical data to electrical data, which are provided to the LpGBT, and vice versa. The LpGBT can configure the CBC, the CIC, and the VTRx+ via I²C. Its slow-control circuit can send hard-reset signals to the CBC and CIC, measure the RSSI voltage⁸ of the VTRx+, measure the power-good signals of the DC-DC converters, and can provide a current source to facilitate the use of a resistance temperature sensor. The RSSI voltage is a measure of the optical transmitter power and can be used for monitoring. The LpGBT also provides the 320 MHz clock and provides the 320 Mb/s trigger input stream for the CBC and CIC ASICs. Two different data streams are used by the module. The so-called DAQ stream⁹ contains the hit cluster data of all

¹CMS Binary Chip

²Concentrator Integrated Circuit

³Low power GigaBit Transceiver. It uses a lower input voltage than its precursor, the GBTx, and consumes less electric power.

⁴Versatile TRansceiver plus

⁵Inter-Integrated Circuit

⁶buck Point Of Load converter, 12.0 V input voltage

⁷buck Point Of Load converter, 2.5 V input voltage

⁸Received Signal Strength Indication

⁹marked with L1 in Figure 3.2

of the module’s CBCs. It is concentrated and provided by the CIC when it receives an L1-accept trigger signal. The stream uses one data line at 320 Mb/s (or 640 Mb/s in some cases, depending on module position and hence occupancy). This stream is asynchronous across detector modules. The second, so-called TRIG, stream¹⁰ is also aggregated from the CBCs to the CIC and contains up to 32 stubs across 8 bunch crossings. The TRIG stream is synchronous across the detector. It uses five lines at 320 Mb/s (or 640 Mb/s). The resulting data rate from the LpGBT to the VTRx+ for the serialized data of both FE hybrids is 5.12 Gb/s (10.24 Gb/s).

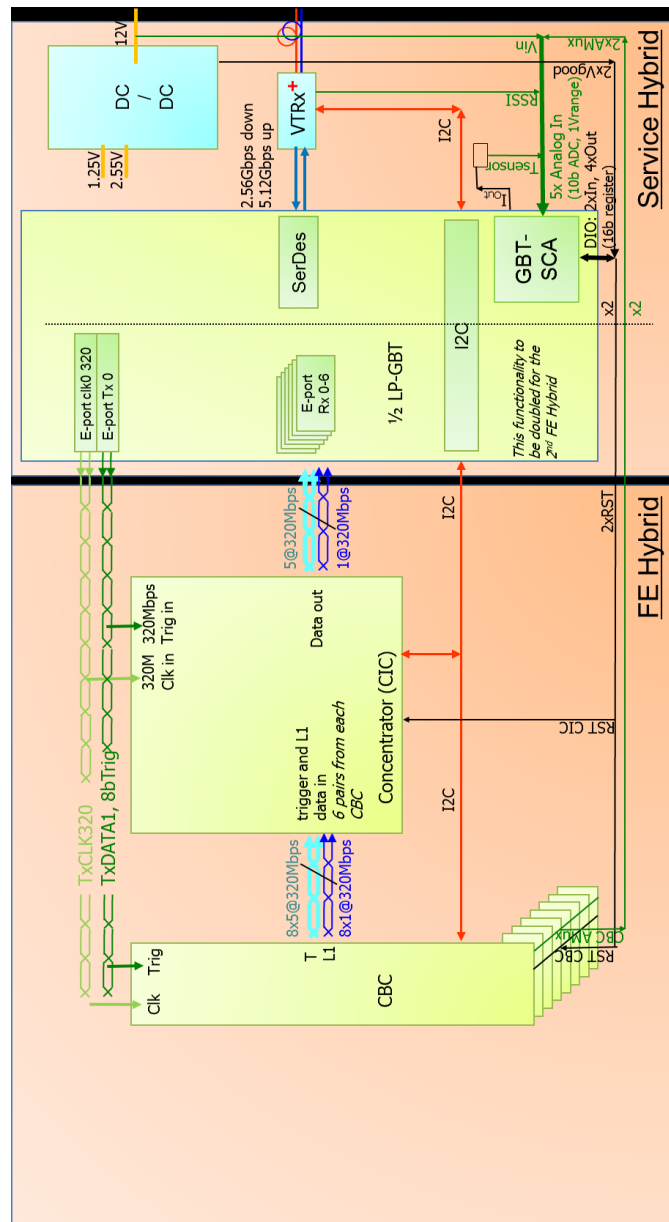


Figure 3.2: Overview of the 2S module communication [7].

¹⁰marked with T in Figure 3.2

3.2 PS module

An exploded-view drawing of the PS module is shown in Figure 3.3. The module has a CFRP baseplate, which is covered with a Kapton layer and directly attached to the macro-pixel sensor. The sensor has 32×960 macro-pixels with a size of $1.5 \text{ mm} \times 100 \mu\text{m}$. The surface of the pixelated sensor is covered with two rows of Macro-Pixel ASICs (MPAs). The MPAs read out the pixels. Two spacers couple the macro-pixel sensor thermally and mechanically to the strip sensor. The sensors has 2×960 strips with a length of 2.4 cm and $100 \mu\text{m}$ pitch. The strips are connected via wire bonds to the FE hybrids. They are placed on the long sides of the module and host eight Short-Strip ASICs (SSAs) to read out the strip sensor. The hybrids are manufactured in the same technology as the 2S FE hybrids and also contain a CIC. Since the PS module has only half the width of a 2S module, its service hybrid is split into two halves, a power and an opto hybrid. They are placed on opposite ends of the module. To improve the readability, in the following I will use the term service hybrid only for the 2S hybrid unless explicitly stated otherwise. The PS hybrids will be called opto and power hybrid. The opto hybrid hosts a LpGBT and a VTRx+. The CIC aggregates the data of the MPAs and SSAs and forwards it to the LpGBT. The serialized data are supplied to the back-end via the optical connection of the VTRx+. The distribution of signals from the back-end is analogue to the 2S case (Figure A.1 of the Appendix).

The power hybrid of the PS module uses two bPOL2V5 in the second stage, because 1.0 V is needed here in addition for the digital domain of the ASICs. The lower voltage is used to save power. The PS powering scheme is shown on the right in Figure 3.4. The HV circuit is not placed on the power hybrid. Instead, it is placed on one of the FE hybrids.

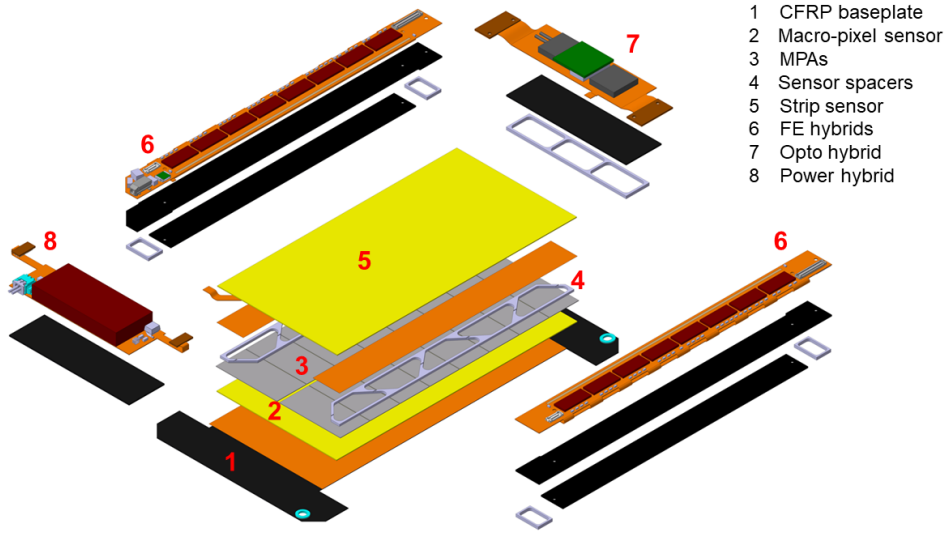


Figure 3.3: Exploded-view drawing of a PS module. Central features are the macro-pixel sensor (2) and the strip sensor (5). Not labelled are additional Kapton isolations and hybrid stiffeners [6].

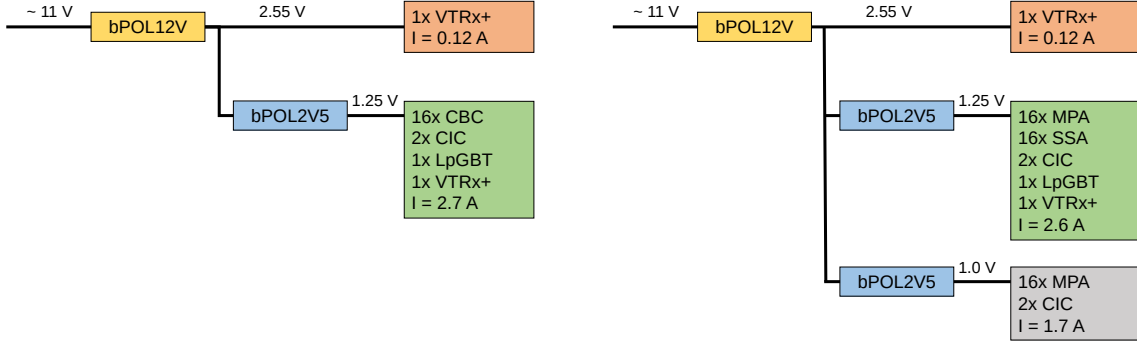


Figure 3.4: Sketch of the two-staged powering scheme used for the 2S (left) and PS (right) modules. The nominal voltages and total expected currents are indicated (based on [4]).

3.3 DC-DC converters

A major part of this thesis deals with the behaviour of the service hybrid's DC-DC converters. These are so-called step-down buck converters that transform a direct current to a lower voltage level. Only the basic working principal is discussed. The DC-DC converter's core components are two transistors (T1 and T2), a coil L and two capacitors to smoothen the input and output voltage. The coil L is the main inductor of the DC-DC converter. The components are arranged according to the simplified schematics in Figure 3.5. It also illustrates the two different circuit configurations, which result when the transistors are switched alternately. In phase a), during the period t_{on} , the transistor T1 is conductive and T2 non-conductive. The voltage source V_{in} supplies the main inductor L . The coil's inductance generates a magnetic field and delays the current flow to the load R_{load} .

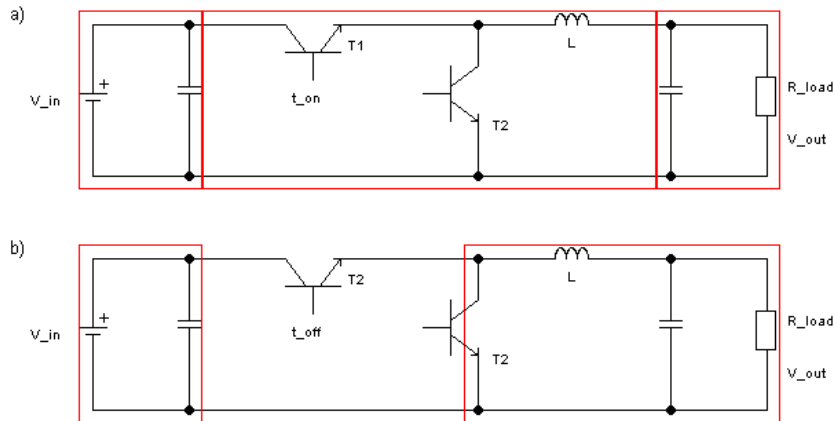


Figure 3.5: Circuit diagram of the general working principal of a DC-DC converter. The closed circuits during the phases a) and b) are marked in red [8].

In phase b), during t_{off} , the situation is reversed. Transistor T1 is non-conductive and T2 conductive. The coil's magnetic field reduces and keeps the current flow up. If the switching period is much smaller than the time constant of the LC circuit, the coil is never fully saturated or depleted. In this case, one can assume that the influence of the coil on the current flow is linear. Under this assumption, the output current is a direct current with a triangular modulation. The voltage V_{out} is reduced in comparison to V_{in} . Figure 3.6 demonstrates the behaviour of current, voltage and transistor states for a loss-less DC-DC converter. The green curve in the lower graph indicates during which phase each of the two transistors is conductive. The brown graph on top shows the mentioned triangular modulation of the output current during both phases and its variation between I_{max} and I_{min} . On the graph in the middle, the blue curve represents the voltage applied to the coil L ($V_{\text{in,L}}$). It is supplied by the voltage source to the transistors. The red curve represents the voltage caused by the inductance V_L . Both voltages are square voltages. According to the law of inductance, V_L corresponds to the variation on the coil current I_L :

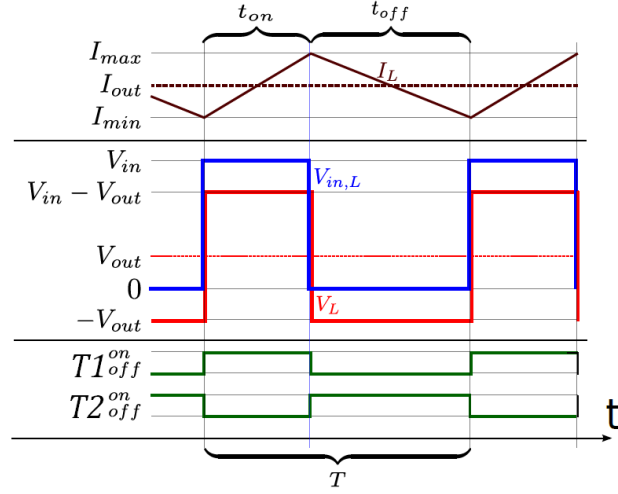


Figure 3.6: Time dependent current and voltage behaviour of a loss-less step-down DC-DC converter [9]. A detailed description is given in the text.

$$V_L = -L \frac{dI_L}{dt} . \quad (3.1)$$

Integration over t_{on} and t_{off} yields

$$\frac{V_{\text{in}} - V_{\text{out}}}{L} t_{\text{on}} - \frac{V_{\text{out}}}{L} t_{\text{off}} = 0 , \quad (3.2)$$

which can be solved for V_{out} :

$$V_{\text{out}} = \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off}}} V_{\text{in}} . \quad (3.3)$$

With the help of the period $T = t_{\text{on}} + t_{\text{off}}$, the switching frequency $f = 1/T$, and the duty cycle $D = t_{\text{on}}/T$ this ratio is often expressed as

$$V_{\text{out}} = \frac{t_{\text{on}}}{T} V_{\text{in}} = t_{\text{on}} f V_{\text{in}} = D V_{\text{in}} . \quad (3.4)$$

The difference between the blue and red curve is the constant output voltage V_{out} .

Instead of the two capacitors, real converters use so-called pi filters, which are placed on the input and output side of the circuit (not shown in the simplified schematics). They are made of a smaller coil in-between two capacitors and serve as a low-pass filter. They are necessary to reduce the high-frequency noise, which occurs in real converters due to the switching processes. Their frequencies are normally higher harmonics of the converter's switching frequency.

3.4 Generation 3 of the 2S service hybrid

The development of the service hybrids started at CERN and was moved to the I. Physikalisches Institut B of the RWTH Aachen University in November 2015. So far, three generations of prototypes have been produced. The LpGBT, the VTRx+, and both DC-DC converter ASICs are still under development at CERN. They are partially replaced by their predecessors. The two-staged DC-DC conversion scheme was implemented in the first generation for the first time. The radiation hard FEAST2 [10] was used instead of the bPOL12V, and a commercial DC-DC converter (LTC3412A [11]) instead of the bPOL2V5. Connectors for tests with the VTRx (the precursor of the VTRx+) and the HV circuit had also been implemented. A detailed series of tests [8] has been carried out to characterise the prototype.

A second generation was used to test a different layout of the pi filters. The goal was a reduction of the DC-DC converter noise.

The third and most recent generation uses the same LV layout as generation 1. A major milestone is the implementation of the GBTx and GBT-SCA¹¹. Together, they have a similar range of functionality as the LpGBT. This enables the first time usage of the readout chain *FE hybrid - service hybrid - optical connection to the back-end* [12]. In addition, two different kinds of connectors for the link between FE hybrid and service hybrid have been implemented and tested. They already provide all pins that will be needed in the final application. It was decided to use connectors instead of wire bonds. Wire bonds can compensate limited precision in the assembly process, but they introduce difficulties when it comes to hybrid testing. A picture of the service hybrid can be found in Figure 3.7. In this figure, the DC-DC converters are placed on the left half of the hybrid. The DC-DC converters main inductances are mounted above the DC-DC converters' chips. The fold-over with the HV circuit is visible on the backside underneath the DC-DC converters. The right part of the hybrid was increased in comparison to the final layout, to fit the GBTx and GBT-SCA, which have a larger footprint than the LpGBT. The connector for the VTRx+ will also be smaller than the connector for the VTRx, which is present on the service hybrid prototype. The 1.8 and 4 mm versions of the service hybrid differ only in a different length of the unglued flexible connection between the main hybrid stiffener and the connector stiffeners. The FE hybrid connectors are placed underneath these stiffeners on both sides of the hybrid. The DC-DC converters will be shielded with a 150 µm aluminium shield to avoid the coupling of electromagnetic radiation to the sensors and FE hybrid electronics. It was removed in Figure 3.7 to show the LV circuit.

Since the GBTx and GBT-SCA need a supply voltage of 1.5 V, the output of the second DC-DC converter stage has been adjusted accordingly. A diode (Schottky Barrier Diode NSR20 F30 NXT5G) has been added close to each FE hybrid connector. It reduces the output voltage so that the CBCs on the FE hybrid prototypes can be supplied with an appropriate voltage of 1.25 V.

¹¹GBT Slow Control ASIC

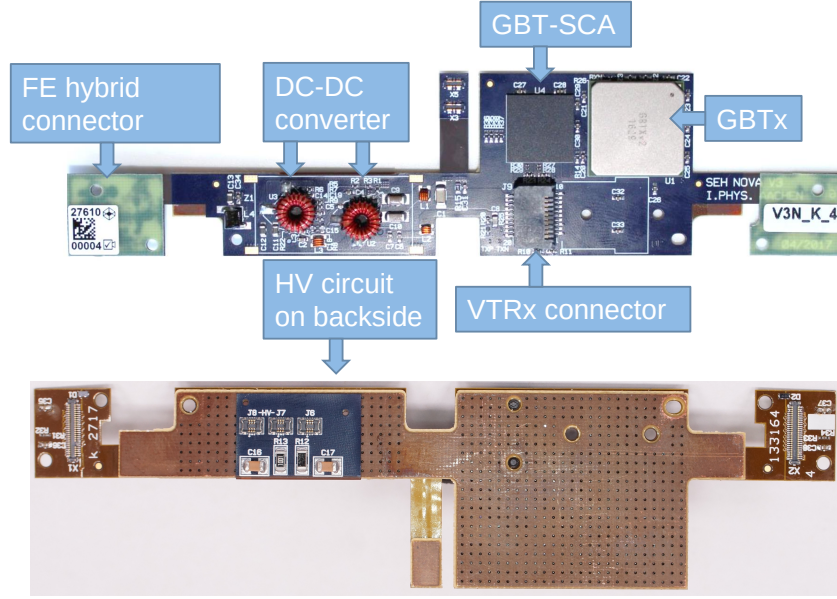


Figure 3.7: Picture of the front (top) and back side (bottom) of a 2S service hybrid. The prototype is from the third generation. The most important features are labelled. The DC-DC converters' shield is not attached.

3.5 PS power hybrid

Currently, the RWTH Aachen University is also responsible for the design of the PS power hybrid. As already mentioned, it hosts three DC-DC converters, one bPOL12V, with a nominal input voltage of around 11 V, and two bPOL2V5. The powering scheme is shown in Figure 3.4. The DC-DC converters provide 2.55 V in the first stage and 1.25 V and 1.0 V in the second stage. The layout of the first prototype is shown in Figure 3.8. It will be the first prototype, which is equipped with prototypes of the actual bPOL2V5 converters. The bPOL12V is still replaced with a FEAST2. All three voltages need to be routed on and through the FE hybrids in order to reach the opto hybrid on the opposite module side. Long flex tails, that wrap around the FE hybrids outside edge, carry the connectors. The placement of all off-chip components is challenging due to the small size of the hybrid. The hybrid has only a thin stiffener, as it is supposed to be attached directly to the baseplate of the PS module to improve thermal coupling. A 150 μm aluminium shield covers the DC-DC converters to protect the sensors and readout electronics from in-coupling noise. The variants for the three different module thicknesses differ only in the length of the flex tails. There is no design yet for the PS opto hybrid as it is largely influenced by the experiences gained with generation 3 of the service hybrid prototypes.

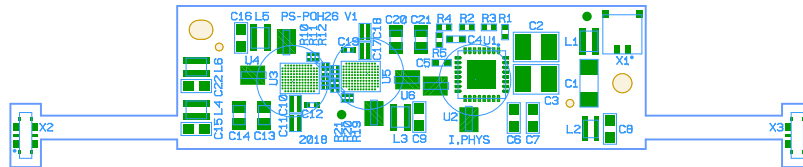


Figure 3.8: Layout of the PS power hybrid prototype. It hosts three DC-DC converters, which provide 2.55, 1.25 and 1 V.

4 Coil development

While the layout of the service hybrid PCB is designed by the RWTH Aachen, the DC-DC converter ASICs are designed at CERN. The chip designers provide information on typical applications and the additionally required SMD¹ components. However, the placing and sizing of all off-chip components fall under the responsibility of the PCB designers. The main inductor is part of these considerations, too. In the past years, the Aachen group has worked mainly with the FEAST2 converter. Both, the 2S service hybrid prototype and the Phase-1 pixel DC-DC converter modules, which were built by the RWTH Aachen, use the FEAST2 [13]. The main inductors used in both cases are shown in Figure 4.1. They are toroidal coils with about 25 windings and with an inductance of roughly 220 nH (service hybrid) and 430 nH (pixel module). Since the high magnetic field in the tracking volume would saturate all ferromagnetic materials, it is sufficient to use a material for the core, which electromagnetic permeability is similar to air. These coil types are called ‘air-core’ coils. The coil inductance can be adjusted to the converter’s switching frequency. As will be shown later, alternating currents (ΔI_L) are proportional to $1/Lf$. While the FEAST2 on the pixel module switches at 1.5 MHz, the service hybrid FEAST2 switches at 2 MHz. The latter is at the end of the recommended range of performance. One of the two newly developed DC-DC converter ASICs for the Phase-2 hybrids is the bPOL2V5. Its switching frequency can range from 4 to 10 MHz and, therefore, air-core inductors of 40-100 nH can be used [14]. So far, the chip designers used only solenoid coils for testing. Air-core solenoids are readily available off the shelf with almost any desired inductance and resistance. In the past, a number of studies showed advantages of toroidal coils over solenoids in terms of electromagnetic radiation [15]. There is little need for small air-core toroidal inductors outside physics experiments, so they need to be custom-made.

Two functional coil properties are considered. The coil resistance has a great influence on the DC-DC converter efficiency and therefore on the module’s power consumption and heat production. The coil inductance influences the noise, which is produced by the DC-DC converter. A high inductance usually reduces the noise, but increases the resistance and lowers the efficiency. To keep the resistance small, while increasing the inductance, the wire material or the wire cross-section can be adjusted. This has an impact on the material budget consumption of the DC-DC converter.

Theoretical predictions and finite element simulations are performed to find start parameters for inductor prototyping. The simulations are compared to measurements of hand-made prototypes. Further studies probe characteristics of the bPOL2V5 converter with different toroidal inductors and compare those to the default solenoid inductor. Finally, a recommendation is made for a suitable inductor for the assembly of power hybrid prototypes.

¹Surface-Mounted Device



Figure 4.1: Main inductors of the 2S service hybrid DC-DC converter (middle) and the Phase-1 pixel DC-DC modules (right). Left, a 1 Euro Cent coin for scale [8].

4.1 Theoretical prediction and simulation

In order to find a reasonable set of parameters to start coil prototyping, a theoretical model is considered [16]. The goal is a toroidal coil with an inductance of roughly 100 nH. A toroidal coil with a rectangular cross-section, the height h , and the inner and outer radii r_i and r_o (Figure 4.2) is assumed. In general the inductance L of a coil is given by

$$L = \frac{N\Phi}{I} ,$$

with N , the number of windings of the coil, Φ , the magnetic flux, and I , the current flowing through the coil. With Ampère's law

$$\oint \vec{H} ds = I$$

one can deduce, since the magnitude of the magnetic field $\vec{H}$ is constant for a toroid at a given radius r due to symmetry:

$$|\vec{H}|2\pi r = IN \Rightarrow |\vec{H}_{(r)}| = \frac{IN}{2\pi r} .$$

For the magnetic flux $\vec{B}$ holds with the magnetic permeability μ

$$\Phi = \int_{r_i}^{r_o} h|\vec{B}|dr = h\mu \frac{IN}{2\pi} \int_{r_i}^{r_o} \frac{dr}{r} .$$

Thus, the inductance of a toroid is derived:

$$L = N^2\mu \frac{h}{2\pi} \ln \frac{r_o}{r_i} . \quad (4.1)$$

For a solenoid coil with cross-section A and length l a similar calculation yields:

$$L_{\text{solenoid}} = N^2\mu \frac{A}{l} .$$

A solenoid's inductance becomes smaller when the coil becomes longer. Forming a solenoid into a ring (or toroid) stretches at least part of the coil. This results in a smaller inductance. The last two equations already yield that a toroidal coil always needs more windings or a bigger cross-section than a solenoid with the same inductance. The DC resistance of a toroid with length l , made up of a wire with radius r_w , and a material with electric resistivity ρ $\left[\frac{\Omega \cdot \text{mm}^2}{\text{m}} \right]$ can be approximated to

$$R_{DC} = \rho \frac{l}{A} = \frac{2N(h + r_o - r_i + 2r_w)\rho}{\pi r_w^2} .$$

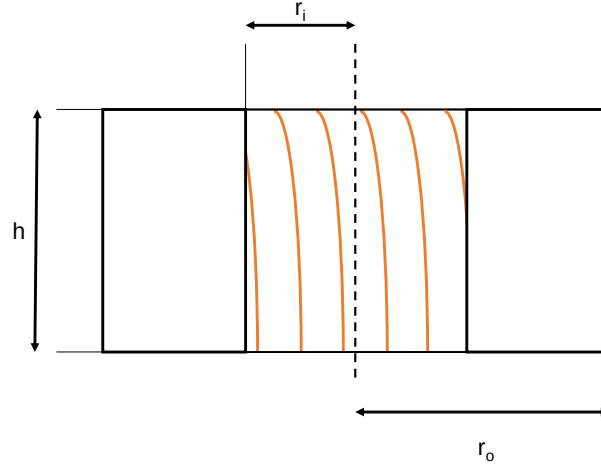


Figure 4.2: Cross-section of the coil design that is used for the theoretical description of the toroid inductor. The orange lines illustrate coil windings.

The term $2r_w$ in the wire length takes into account that r_o and r_i are measured to the centre of the wire.

In a first step, the theoretical predictions are compared to a finite element simulation of a toroidal coil. Later these results will be compared to measurements with prototype coils. *COMSOL Multiphysics 5.2* and its *AC/DC Module* are used for the simulation [17, 18]. An exemplary coil is shown in Figure 4.3. In this model, the parameters N , h , r_i , r_o , and r_w can be chosen freely. The coil volume is declared a ‘coil domain’ with a defined current flow through the surface marked in green. The simulation returns the resistance and inductance of the coil. Three parameters are explored. The number of windings, since theory predicts it to have the strongest influence, r_o , and h . All other parameters remain fixed. The standard values are summarized in Table 4.1 and only one parameter per time is varied. The height h is limited by the maximum height of the hybrid, the inner radius r_i remains fixed to ensure non-intersecting wire elements even for a high number of windings. The results are presented in Figure 4.4. On the left are the comparisons of the inductance and on the right the comparisons of the resistance. Qualitatively, the finite element simulation is always in agreement with the theory prediction. The inductance rises with the square of the number of windings and linearly with the height and the outer radius. The deviations regarding the resistance are remarkably small, despite the differences in the detailed coil geometry. The differences in geometry include the curved sections and the angles of the windings. However, there is an offset of more than 20 nH between every pair of inductance values. The simulation predicts higher inductance values. The difference reduces for a higher number of windings and an increasing outer radius. For a small number of windings, the windings themselves are further apart from each other and are quite distorted. This results in a greater effective cross-section and is not accounted for in the theory’s derivation of the inductance.

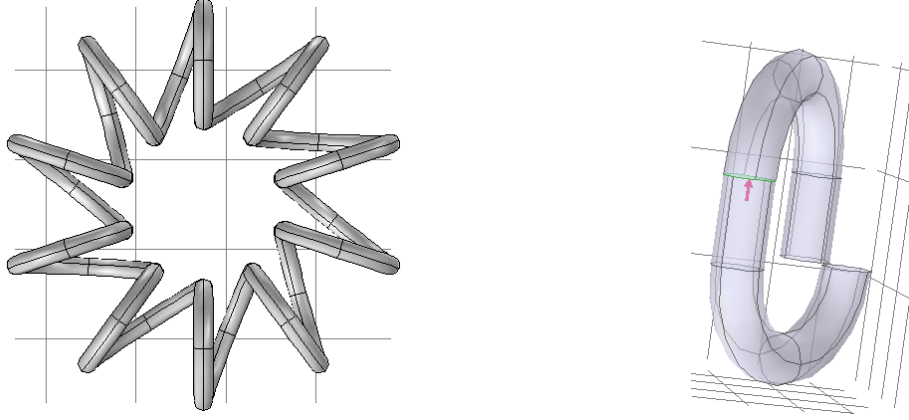


Figure 4.3: On the left, an exemplary coil for the *COMSOL* simulation is shown. The right picture shows the geometry of a single winding and the surface, where the coil is excited (green). The parameter h is given by the full height of the coil and r_o and r_i are defined as in Figure 4.2 above.

Number of windings	12
Height	3.1 mm
Outer radius	3.55 mm
Inner radius	1.5 mm
Wire radius	0.1136 mm
Wire material	copper
ρ	$1.667 \cdot 10^{-2} \text{ } \Omega \cdot \text{mm}^3/\text{m}$

Table 4.1: Standard parameters used to simulate inductance and resistance of the coils. They are motivated by the size of toroidal coils currently used for the DC-DC converters of the 2S service hybrid prototypes.

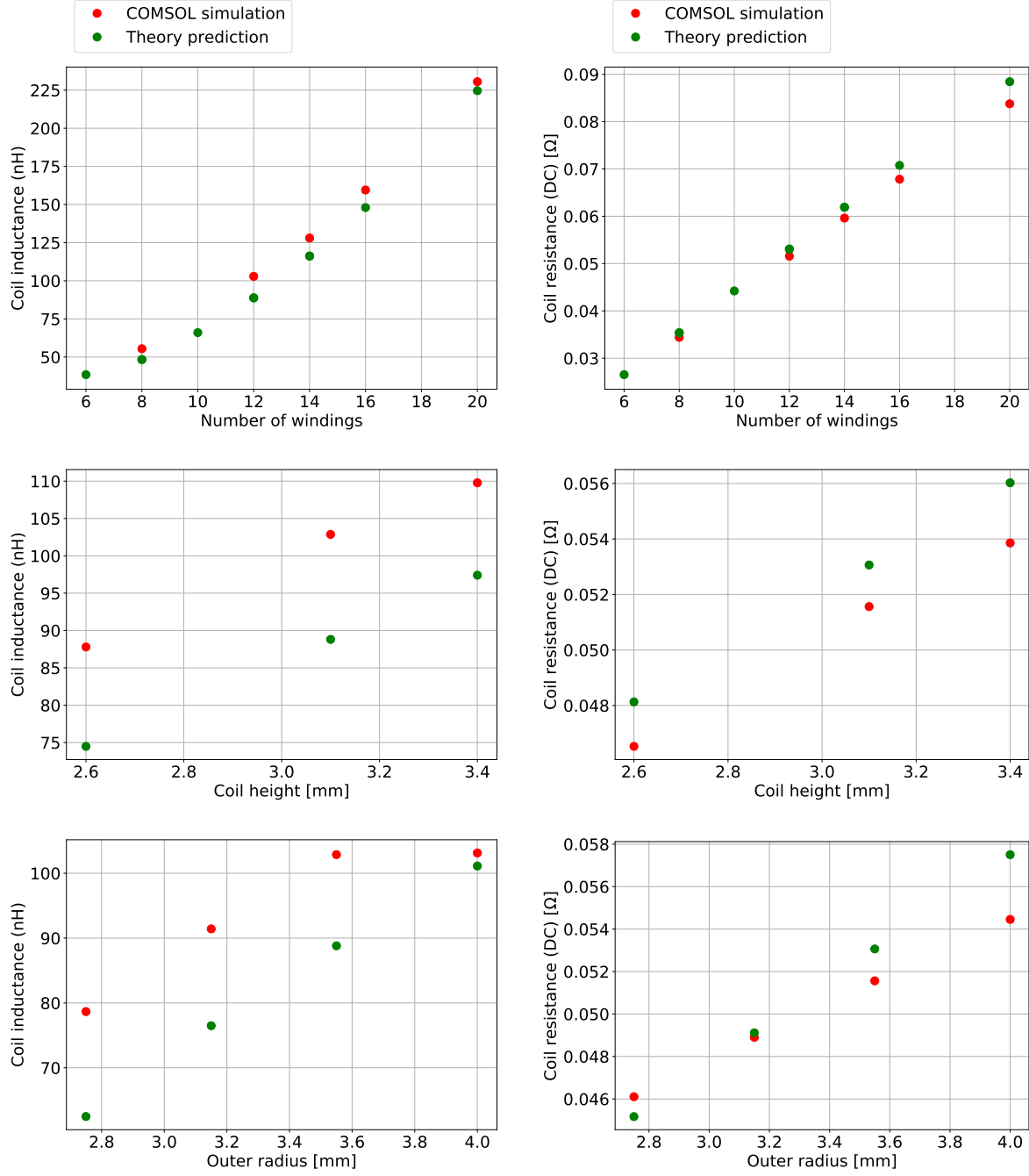


Figure 4.4: Results of the simulation and theoretical prediction of a toroid's inductance (left) and resistance (right). The examined parameters are, from top to bottom, number of windings N , coil height h , and outer radius r_o .

4.2 Characterisation of coils

The predictions give a starting point for a reasonable set of coil parameters. In order to test those, a variety of coils is wound by hand. 3D-printed polycarbonate rings are used as cores. They are printed according to Figure 4.5. An octagonal shape is chosen over the rectangular one for easier winding. The rings' size is of the order of the printer resolution. Therefore, their precision is limited. A variety of enamelled copper wires with different cross-sections are available for prototyping. As the standard wire a copper-clad aluminium (CCA) wire with 15 vol-% copper and an active diameter of 0.28 mm is chosen. CCA is the preferred material choice for the main DC-DC converter inductor of the Phase-2 upgrade, because it uses less material inside the tracking volume while ensuring low resistance.

While the skin effect is not relevant for the direct current component of the current inside the coil, it has to be considered for the alternating current component. At the bPOL2V5's switching frequency of 4 MHz the skin depth δ of copper is about 24 μm . The outer copper coverage of the CCA wire is about 11 μm thick. The simulation and theory predictions were conducted with a thinner full copper equivalent (about 227 μm diameter) of the CCA15 wire with respect to direct current resistance per unit length. Due to the skin effect, the current density of the alternating current component is concentrated near the wire surface, where the copper cladding of the CCA and a smaller resistance is present. The wire's alternating current resistance, therefore, suffers a smaller increase than the direct current resistance, when the wire material is changed from copper to CCA.

Figure 4.6 shows three different kinds of main inductors. The leftmost is a solenoid that is used as the default option on a bPOL2V5 evaluation board, which has been designed at CERN. The coil in the middle is a toroid, which is used on the 2S service hybrid prototypes and inspired the prototyping effort. The toroid on the right was made by hand using a 3D printed core. All different ring sizes used for prototyping are summarized in Table 4.2.

4.2.1 Inductance and resistance measurements

The measurements of the inductance and resistance of the hand-made coils are performed with a Keysight E4980A Precision LCR Meter [19, 20] and a 16047A Test Fixture [21], which are shown in Figure 4.8. The device measures the impedance Z , the phase of the impedance θ , and the series resistance R . All quantities, except the series resistance, depend on the test frequency. An

h [mm]	r_o [mm]	r_i [mm]
2.6	2.75	1.5
2.6	3.15	1.5
2.6	3.55	1.5
3.1	2.75	1.5
3.1	3.15	1.5
3.1	3.55	1.5
3.1	4.00	1.5
3.4	3.55	1.5

Table 4.2: Summary table of the core sizes that were produced for coil prototyping.

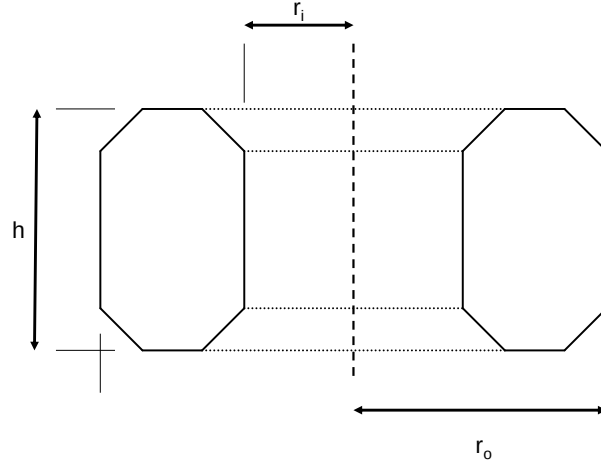


Figure 4.5: Sketch of the cross-section of a toroid core. The cores are 3D-printed and used for coil prototyping.



Figure 4.6: Picture of three different kinds of main inductors. On the left a 100 nH solenoid used as the default option on the bPOL2V5 evaluation board (Section 4.3). In the middle, a 220 nH toroid, which is used on the 2S service hybrid prototypes. On the right, a 100 nH custom made toroid. On the far left a 1 Euro Cent coil is given for scale.

important quantity is also the reactance X . The four quantities are connected by the equations

$$Z = R + jX \quad (4.2)$$

$$|Z| = \sqrt{R^2 + X^2} \quad (4.3)$$

$$\theta = \arctan\left(\frac{|X|}{R}\right) . \quad (4.4)$$

The test frequency f and the inductance L can be used to represent the reactance

$$X = 2\pi fL .$$

All measurements use the series equivalent circuit mode (Figure 4.7). For low inductance values, the reactance is small, too. So the series resistance component R_S is more significant than the parallel resistance component R_P . Since L is directly linked to the reactance, L is in general independent of the circuit model, unlike for example the quality factor $Q = |X|/R$, which is

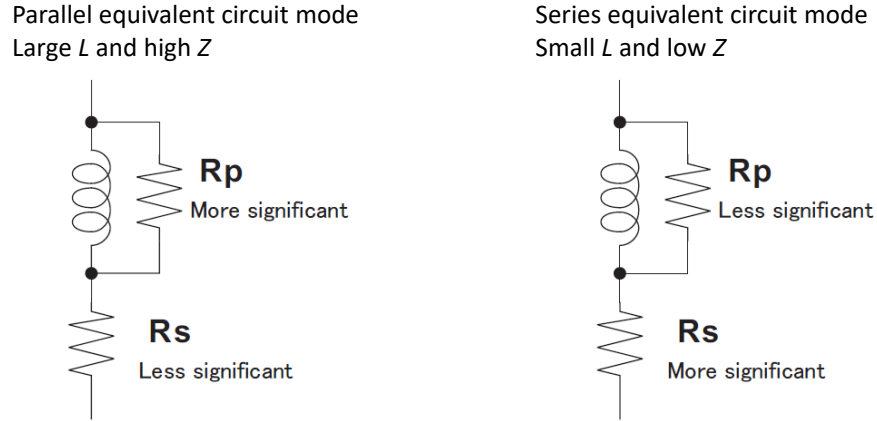


Figure 4.7: Equivalent circuit diagram of the series and parallel equivalent circuit mode of the LCR meter [20].



Figure 4.8: Picture of the LCR meter that is used for coil characterisation. A coil is attached to the test fixture.

the ratio of the energy stored in an oscillating resonator to the energy dissipated per cycle by damping processes. The manufacturer suggests the series circuit mode for an impedance below $10\ \Omega$ [20].

In order to measure resistance and inductance of a coil, the wire ends are stripped off the insulation and soldered to gold plated contacts. The coils can be attached to the fixture with the contacts, as shown in Figure 4.9. The coils are small compared to the fixture and the contacts. The contacts ensure a tight hold inside the fixture and a low unwanted resistance. It is important to keep the surplus wire, that is necessary for the soldering, as short as possible. Moreover, the contacts should be placed as close as possible to each other inside the fixture to avoid additional inductance due to the loop formed by the surplus wire. The inductance is measured for frequencies between 100 Hz and 2 MHz. The available LCR meter does not allow higher frequencies, e.g. the bPOL2V5 switching frequency of 4 MHz. Short and open corrections for the used fixture are applied. They correct the characteristics of the fixture and are applied automatically after two calibration procedures with a low impedance connection inside the fixture (short corrections) and measuring the bare fixture (open corrections).

A series of typical inductance measurements is shown in Figure 4.10. For this plot, the rings with $h = 3.1\text{ mm}$ and $r_o = 3.55\text{ mm}$ have been equipped with 6 to 20 windings. All inductors show the same basic behaviour. The inductance rises from 100 Hz to 1000 Hz by 30-40 nH and forms



Figure 4.9: Picture of the LCR meter test fixture with an attached coil (left). On the right, a custom made toroid. Gold plated contacts have been soldered to the ends.

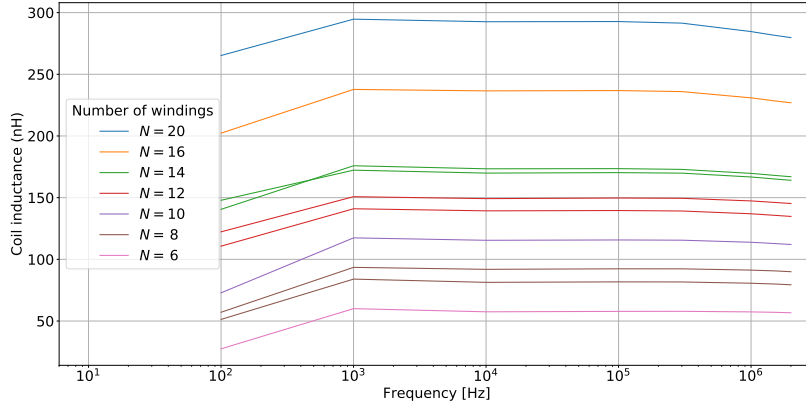


Figure 4.10: Inductance versus frequency measurement for different numbers of coil windings. All toroids have the same geometry.

a plateau after that. Clearly, the inductance rises with the number of windings. Some numbers of windings are present multiple times. These are multiple coils with the same properties and are used to estimate the uncertainties. The variations between these pairs are smaller than the differences to the adjacent number of windings. The greatest difference between two coils of the same kind times a factor of 1/2 is taken as uncertainty. It amounts to roughly 5 nH. The series resistance R is independent of the frequency f as illustrated by Figure 4.11. The expected increase of the resistance with increasing number of windings is observed. The uncertainties are approximated to be $2 \text{ m}\Omega$, due to the contacts and differences observed between congeneric coils. To compare the measurements to the simulation and theory prediction, the inductance value for $f = 2 \text{ MHz}$ is used. It is closest to the desired application. The results are given in Figure 4.12. The left plots show the inductance studies. While they qualitatively agree with the simulation and the theory, a discrepancy to the simulation of a 30-40 nH positive offset is observed. This offset stands in no relation to the same sized increase observed in the measurements in Figure 4.10, which is caused by the breakdown of the used circuit model at low frequencies. Two explanations for the offset in Figure 4.12 are possible. Firstly, both predictions assume a fully closed coil and ignore the surplus wire and the connectors. The connection forms a single-loop coil, which causes its own inductance. Tests with short wires without a core delivered inductance values of the order of 20 nH. Secondly, the winding process by hand is not perfect. The size of a winding is systematically bigger than in the models, leading to higher inductance values. If we assume

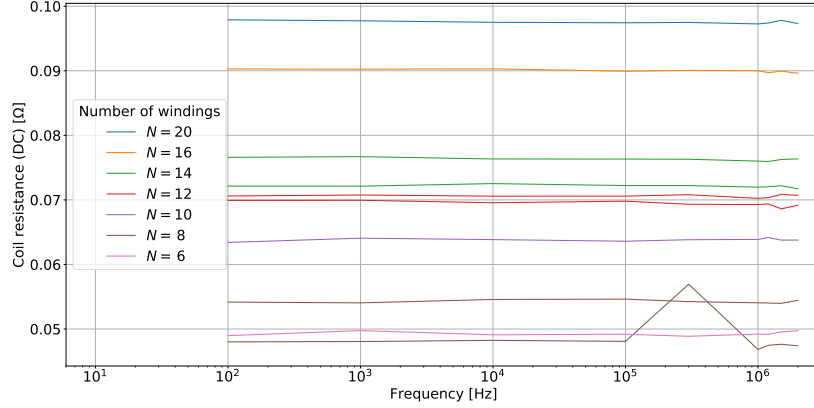


Figure 4.11: Resistance versus frequency measurement for different numbers of coil windings. All toroids have the same geometry.

the windings to be larger in each direction by 0.1 mm, we obtain an increase in inductance by a factor k of

$$k = \frac{h' \ln \frac{r_o'}{r_i'}}{h \ln \frac{r_o}{r_i}} = \frac{3.3 \text{ mm} \ln \frac{3.65 \text{ mm}}{1.4 \text{ mm}}}{3.1 \text{ mm} \ln \frac{3.55 \text{ mm}}{1.5 \text{ mm}}} = 1.18 .$$

As indicated in the top left plot, fitting a quadratic function without the linear term to the data (since theory predicts $L \propto N^2$) delivers a curve that intersects the y-axis at 45 nH. The parameter of the quadratic term (Equ. 4.1) is about 0.625 nH. The theory value of 0.534 nH yields a factor k of 1.17. This is in good agreement with a hypothesis of a coil with a bigger cross-section and an offset due to the connection wires. However, the fitted offset is higher than expected of the measurements of short wires without the core. The theory description is not valid for small numbers of windings.

An offset is also observed when looking at the coil resistance. It can be fully explained by the additional resistance of the surplus wire and the connectors. With short wire pieces soldered to connectors and measured on the LCR meter, the offset is determined to be about 18 mΩ. When this correction is applied, predictions and measurement are in very good agreement (black markers in Figure 4.12). The resistance shows the expected linear increase for all parameters. Measurements and predictions show that the easiest way to adjust a coil's inductance is to adjust the number of windings. The other values contribute linearly at best and require the adaptation of the core. Therefore, further studies will use the standard core parameters but a different number of windings. With this geometry, a toroidal inductor with ten windings comes closest to the inductance of the default 100 nH solenoid used by the bPOL2V5 chip designers. This is confirmed by the study shown in Figure 4.13. While toroid A is made of the CCA15 wire, toroid B is made of a full copper wire with a diameter of 0.45 mm. Both toroids show good agreement in terms of inductance with the solenoid.

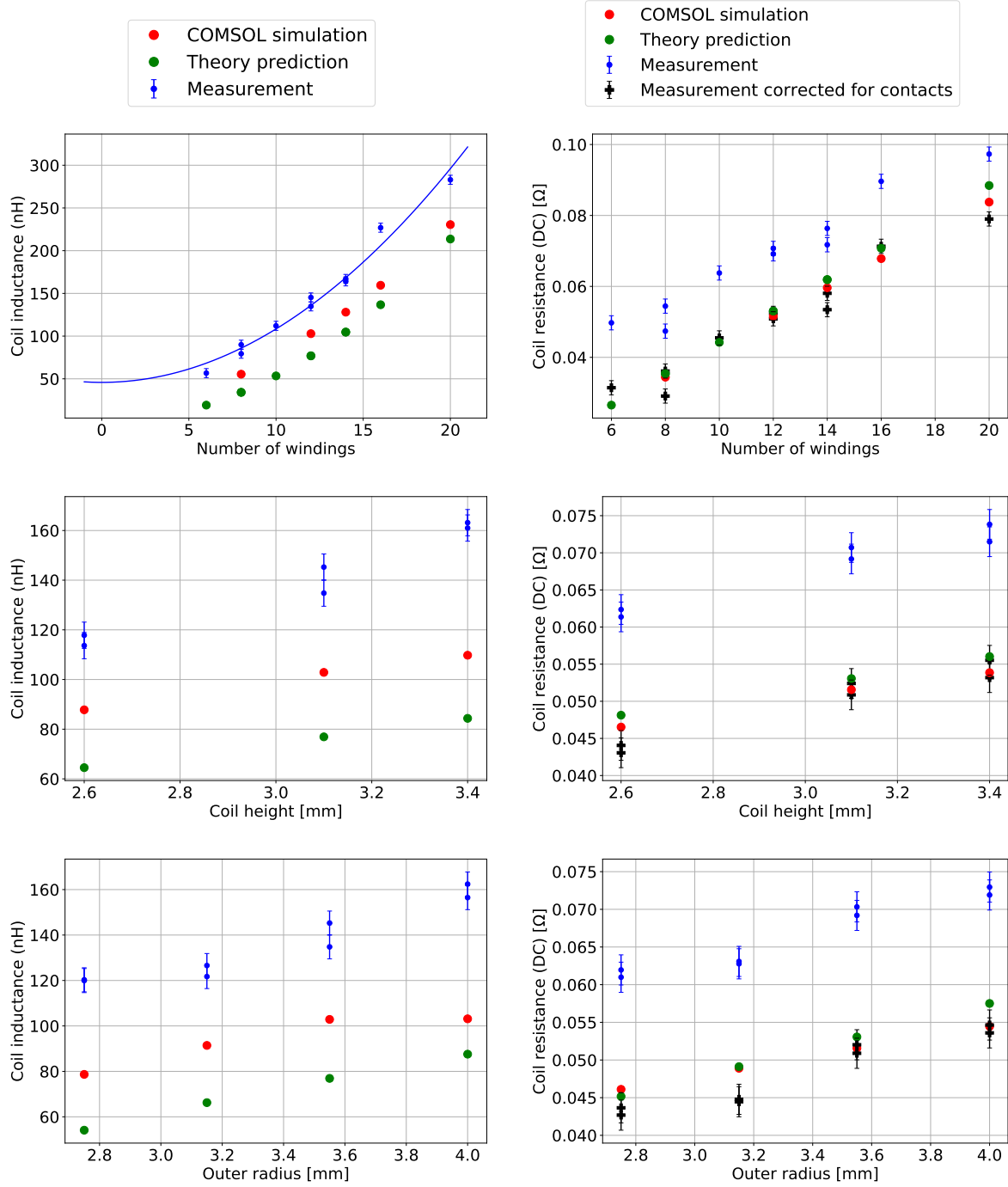


Figure 4.12: Measurement results of the inductance (left) and resistance (right) of toroidal inductor prototypes. The examined parameters are, from top to bottom, number of windings N , coil height h , and outer radius r_o . The results are compared to the simulation and the theory prediction.

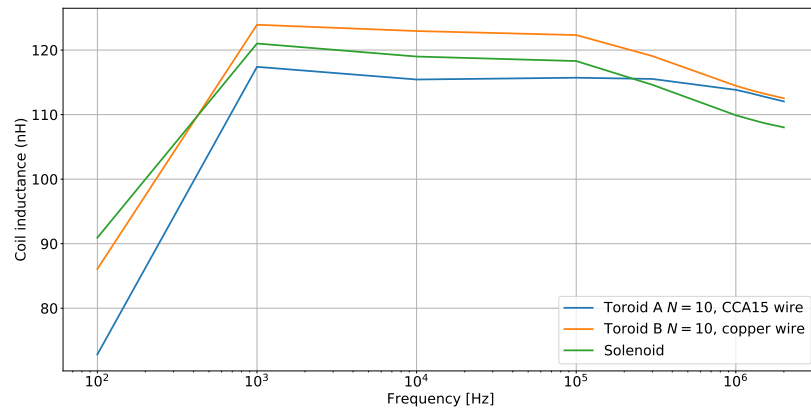


Figure 4.13: Inductance versus frequency measurement for toroidal coils with the same number of windings and geometry but a different wire material and cross section. They are compared to the default 100 nH solenoid coil.

4.3 Measurements with the bPOL2V5 evaluation board

In preparation of the PS power hybrid prototype, the developers at CERN provided Aachen with a bPOL2V5 evaluation board. The PCB was designed to host a single converter ASIC and the off-chip components. It features the ‘typical application’ design from the converter’s data sheet [14]. The evaluation board provides the possibility to test inductor prototypes in a setting that is very similar to the final application. In order to perform multiple tests with various coils and without the need of frequent soldering on the PCB, the default solenoid coil has been replaced by a pin plug. The coils under test are soldered to a matching pin header and can be exchanged easily (Figure 4.3). The DC-DC converter efficiency, the common and differential mode noise, and the electromagnetic radiation are explored. Due to the different connector, all coils are resoldered. The new pin connectors can also be attached to the LCR meter. Some small changes in the coil parameters such as inductance and resistance are observed. The values quoted in the following measurements are measured with the pin plug header. This leads to some inconsistencies compared to Section 4.2.1.

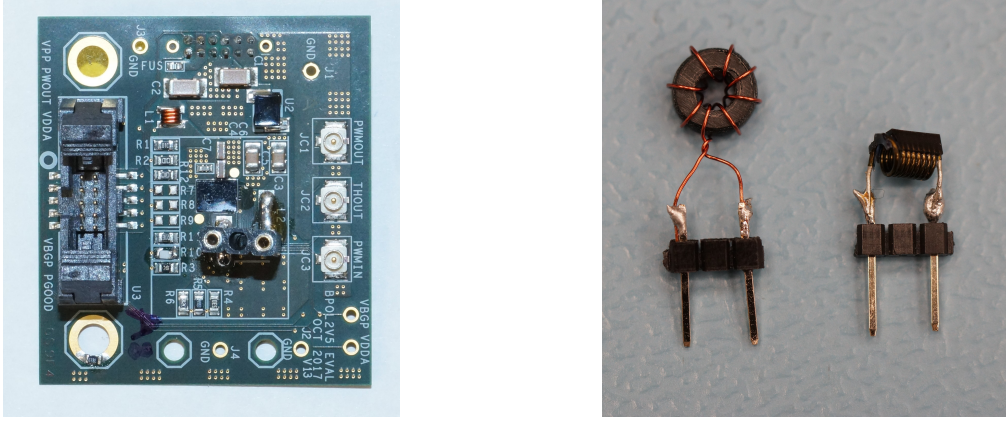


Figure 4.14: The left picture shows the bPOL2V5 evaluation board. The inductor has been replaced by a pin plug. The right picture shows two coils soldered to the matching header: left a custom toroid, and right the default solenoid.

4.3.1 Efficiency

An important measure in all DC-DC converter applications is the power efficiency. It indicates the ratio of the electrical output to input power:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{\text{out}} \cdot I_{\text{out}}}{V_{\text{in}} \cdot I_{\text{in}}}.$$

In a loss-less case, this ratio would be 1, which is not achievable with real DC-DC converters. In the context of the Phase-2 tracker upgrade the efficiency is a vital parameter. The space for cables, and therefore the amount of power that can be brought to the detector, is limited. Losses in the conversion process mainly result in additional heat, which needs to be removed from the tracking volume. Especially the multi-stage DC-DC converters approach calls for high efficiencies, since all losses in the second stage produce additional losses when the surplus power passes the first stage. From the many factors that can influence the DC-DC converter efficiency, the focus will be laid here on the main inductor coil. Contributions of direct current (I_{out}) and alternating current (ΔI_L) lead to ohmic losses due to the coil resistance R_L (DC part) and R_S

(frequency dependent equivalent series resistance, AC part). The alternating current arises from the switching processes. The total loss is given by

$$P_L = R_L I_{\text{out}}^2 + \frac{R_S}{12} \Delta I_L^2 . \quad (4.5)$$

ΔI_L is defined as $\Delta I_L = I_{\text{max}} - I_{\text{min}}$ and can be derived by integrating over dI_L/dt

$$\Delta I_L = \left| \int \frac{dI_L}{dt} dt \right| \quad (4.6)$$

$$\stackrel{\text{Equ.3.1}}{=} \left| \int -\frac{V_L}{L} dt \right| \quad (4.7)$$

$$= \int_0^{t_{\text{on}}} \frac{V_{\text{in}} - V_{\text{out}}}{L} dt \quad (4.8)$$

$$= \frac{V_{\text{in}} - V_{\text{out}}}{L} t_{\text{on}} \quad (4.9)$$

$$\stackrel{\text{Equ.3.3}}{=} \frac{V_{\text{in}} - V_{\text{out}}}{L} \frac{V_{\text{out}}}{V_{\text{in}}} T \quad (4.10)$$

$$= \frac{V_{\text{in}} - V_{\text{out}}}{Lf} D . \quad (4.11)$$

For the given application ΔI_L is approximately 0.4 A. While the switching losses decrease with increasing inductance, both losses increase with resistance. In most cases, I_{out} will be greater than ΔI_L and these losses will dominate. An optimization of the efficiency for high currents will, therefore, be driven by the length of the coil wire, its diameter, and material, rather than inductance [22].

4.3.1.1 Setup

Previous studies showed a slight temperature dependency of the DC-DC converters' efficiency [23]. The bPOL2V5 evaluation board is therefore placed on an aluminium cooling bridge (a in Figure 4.15) and fixed with Kapton tape. For electrical isolation, an additional layer of Kapton is applied between the board and the bridge. A benchtop temperature controller (b, Belektronic BTC-LAB [24]) with a temperature sensor keeps the temperature at 20 °C. All additional instruments are controlled and read out via a *LabVIEW* VI². A power supply (c, Agilent E3633A DC Power Supply [25]) provides the input voltage and measures input voltage and current. Sensing is used to correct for losses on the supply cables. The load for the DC-DC converter is provided via a load box (d, custom made by the RWTH Aachen) with a built-in multifunction I/O device (National Instruments USB-6008 [26]), which measures the output current. To avoid measurement errors of the output voltage due to cable losses, the output voltage is measured at the converter output and in parallel to the load. Therefore, the output of the bPOL2V5 evaluation board is connected directly with an additional multifunction I/O device (e, National Instruments USB-6008 [26]). The efficiency can be determined in different intervals of the input voltage and output current. The bPOL2V5 is designed to operate at 2.0 V to 2.5 V input voltage. The statistical uncertainties can be estimated by repeated measurements to be lower than one percent if the cooling is operational and good thermal contact with the cooling bridge is maintained. At high currents, losses in the fixtures can occur. This can be avoided with careful assembly. A schematic drawing of the setup is shown in Figure 4.16.

²Virtual Instrument

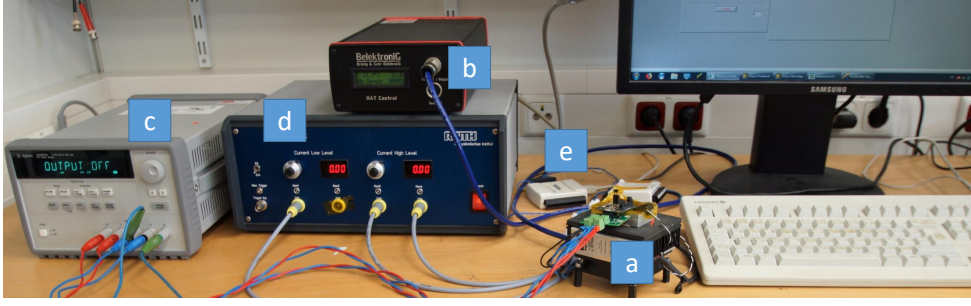


Figure 4.15: Setup for the efficiency measurement. A detailed description can be found in the text.

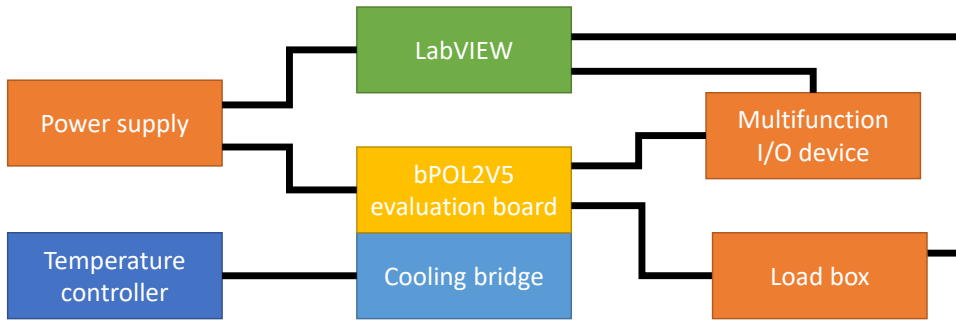


Figure 4.16: Schematic drawing of the setup to measure the bPOL2V5 converter efficiency [8].

4.3.1.2 Results

Firstly, it is confirmed that the use of a toroid instead of a solenoid does not have a negative impact on the DC-DC converter efficiency. Therefore the default solenoid and the 10-windings inductor made of 0.45 mm copper wire are measured on the setup. This particular toroid has a very similar resistance and inductance in comparison to the solenoid inductor. The results are shown in Figure 4.17. There is little difference between both measurements. The solenoid's efficiency rises from 0.80 at 0.5 A to 0.86 at 1.0 A, where it stays up to a load of about 1.5 A. Then the efficiency drops nearly linearly to about 0.81 at 3.0 A. The deviations between the two coils are within the 1 % uncertainty range and can be explained with slight differences in inductance and resistance.

In order to illustrate the influence of the inductance, three coils are considered. They are all made of the same 0.28 mm CCA15 wire but with a different number of windings, namely 6, 10, and 16. This results in them having an inductance of 60, 107, and 225 nH and a resistance of 43, 62, and 90 mΩ, respectively. The result of this series of measurements can be found in Figure 4.18. One can distinguish two different effects. At about 1 A all inductors give the same maximum efficiency of about 0.81. The efficiency then drops with rising current to about 0.72, 0.69, and 0.65 at 3 A for 6, 10, and 16 windings, respectively. These nearly linear drops with different slopes are due to the resistance, which increases with the number of windings. Above 1 A the losses due to the direct current I_{out} dominate and the efficiency decreases. For an output current below 1 A the order reverses. The alternating current losses dominate and the coil with the highest inductance has the highest efficiency, as predicted by Equation 4.11.

During operation of the Phase-2 outer tracker, the bPOL2V5 will be operated with an output current above 2 A and therefore in a phase space, where the losses due to I_{out} will dominate.

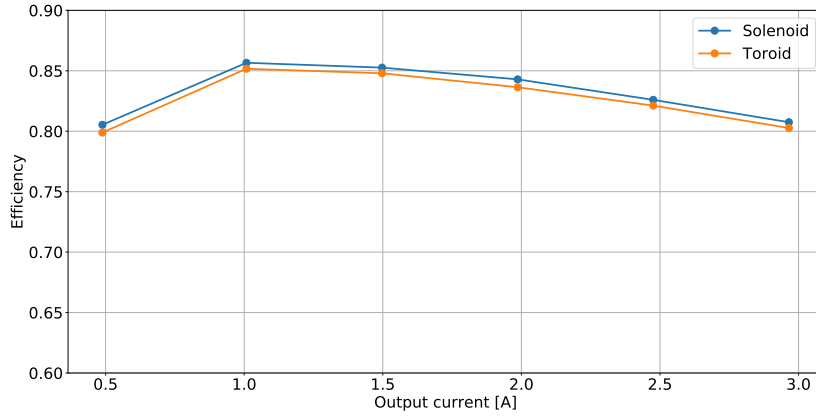


Figure 4.17: Efficiency versus output current for the default solenoid inductor and a custom toroid inductor. The toroid was chosen to mimic the resistance and inductance of the solenoid.

Therefore, it makes sense to take a closer look at the relationship between the inductor resistance and the efficiency. To do so, three different coils with ten windings each are considered. One is made up of 0.45 mm copper wire ($R = 17 \text{ m}\Omega$), one of 0.30 mm copper wire ($R = 37 \text{ m}\Omega$), and one of 0.28 mm CCA15 wire ($R = 63 \text{ m}\Omega$). Their inductances are all close to 100 nH. The corresponding efficiencies are shown in Figure 4.19. As expected, all three inductors behave similarly to the solenoid. However, the efficiency drops with the resistance and therefore the difference between the curves increases with growing output current.

This is illustrated in Figure 4.20, where the efficiency is plotted against the resistance for different values of the output current. The three efficiency values per output current align on a linear function, as indicated by the fitted straight line. In terms of inductor development, Figure 4.20 is particularly useful to identify which maximum efficiency can actually be achieved when the coil resistance is further decreased. Additionally, a prediction can be made for each choice of wire. If one plots the slopes of each straight line against the corresponding output current, the values form a straight line, too. This one yields a slope of 0.065 [percent points efficiency loss per $\text{m}\Omega$ coil resistance and Ampere output current]. The corresponding graph is shown in Figure 4.21. It allows to calculate the impact of every additional resistance in the current path and is directly linked to Ohm's law and the efficiency formula.

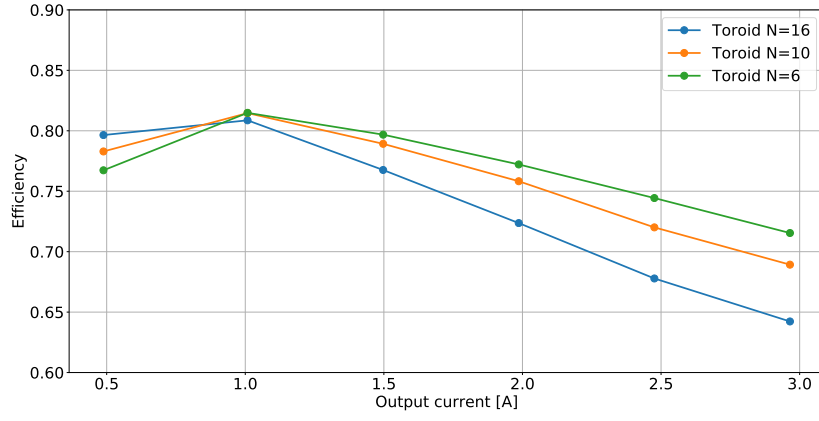


Figure 4.18: Efficiency versus output current for three toroid inductors with different numbers of windings.

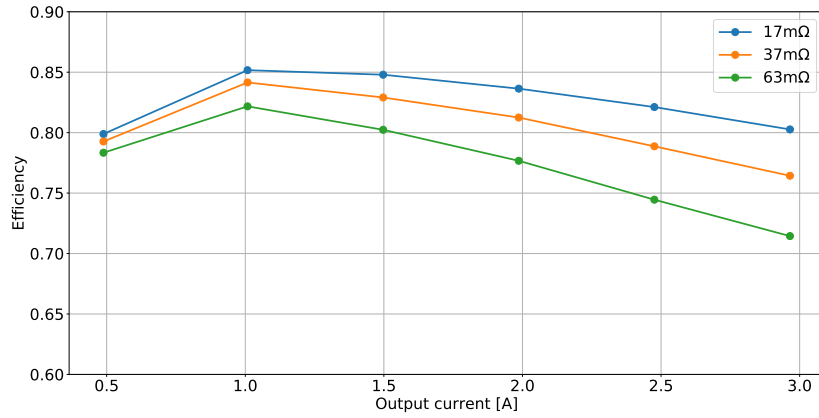


Figure 4.19: Efficiency versus output current for three toroid inductors with ten windings and different resistances.

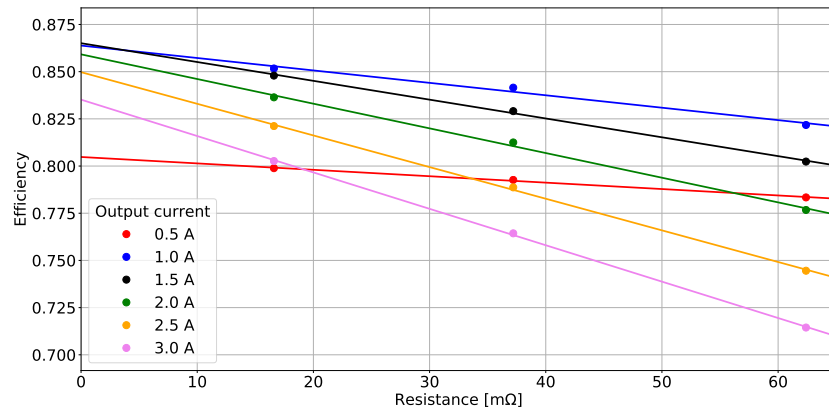


Figure 4.20: Efficiency versus resistance of inductors with ten windings. Each line corresponds to a different output current. Linear functions are fitted to the data.

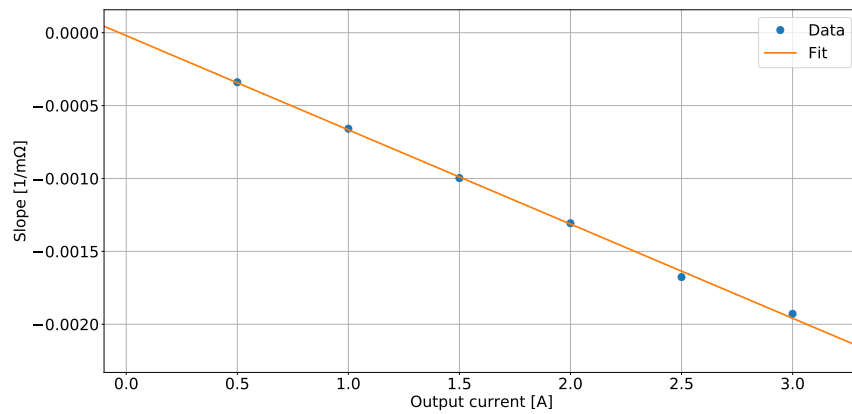


Figure 4.21: Slopes of the linear functions in Figure 4.20 versus the corresponding output currents.

4.3.2 CM/DM noise

The continuous switching of the DC-DC converter chip's transistors leads to charging and discharging of connected inductances and capacitances. This results in a modulation of the supplied direct current with high-frequency alternating currents. These occur at the switching frequency and their higher harmonics. The modulations are relevant for the powering of the readout electronics, which are sensitive to small variations in the supply voltage [27]. The variations can be divided into two categories, common mode (CM) and differential mode (DM) noise. Figure 4.22 illustrates the difference between differential mode noise I_{DM} and common mode noise I_{CM} . Differential mode noise (top) is created by the noise source V_{DM} inside the circuit. The noise propagates on the positive line to the sink and on the negative line back to the source. Common mode noise (bottom) propagates from the source V_{CM} , which is outside the circuit (e.g. additional transistors inside the DC-DC converter chip), symmetrically on both lines to the load. Parasitic capacitances close the circuit via ground. From the assumptions above one can conclude that the noise $\frac{1}{2}I_{CM} + I_{DM}$ runs on the positive line and the noise $\frac{1}{2}I_{CM} - I_{DM}$ on the negative line towards the sink. To measure CM and DM noise separately, cables must be routed in different ways through a current clamp (left side of Figure 4.22). If both lines run anti-parallel, the current

$$\frac{1}{2}I_{CM} + I_{DM} - (\frac{1}{2}I_{CM} - I_{DM}) = 2 \cdot I_{DM}$$

is measured. This results in two times the differential mode noise signal I_{DM} .

When parallel cables are used, the common mode noise I_{CM} is measured, since the current

$$\frac{1}{2}I_{CM} + I_{DM} + \frac{1}{2}I_{CM} - I_{DM} = I_{CM}$$

is running through the current clamp. The measurement is inductive and contact-free.

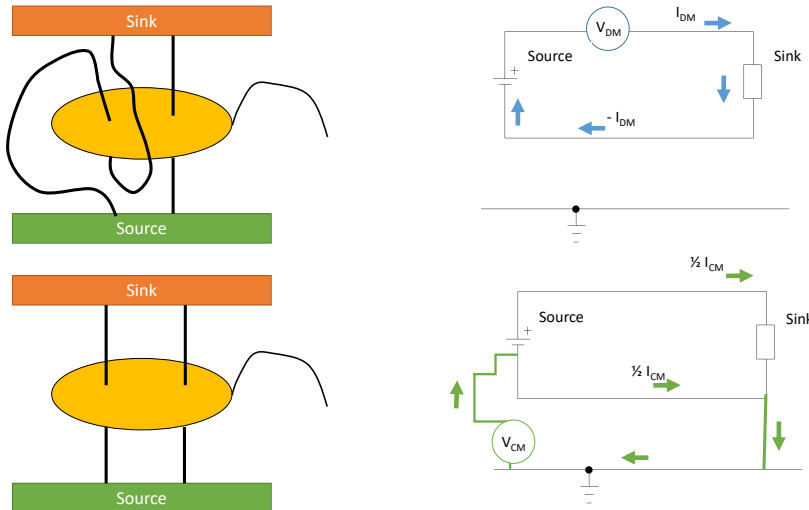


Figure 4.22: Measurement modes for the differential (top) and common (bottom) mode noise measurements. The routing of the connecting cables through the current clamp is shown on the left, the equivalent circuit diagram is shown on the right [8].

4.3.2.1 Setup

The setup to measure the CM and DM noise was prepared by Rüdiger Jussen in the course of his diploma thesis [9]. It is based on a measurement used at CERN. It has been slightly modified in the past in order to cope with the DC-DC converters under test [28].

The current setup is shown in Figure 4.23 and sketched in Figure 4.24. It is placed on a copper plate and all devices are grounded to this plate providing a reference potential. A power supply (a in Figure 4.24, Agilent E3634A DC power supply [25]) provides the input voltage of 2.5 V. A line impedance stabilization network (b, HAMEG Instruments HM6050-2 [29]) smoothens the input voltage with a low pass filter. This reduces the influence of fluctuations of the mains voltage. The electrical load is provided via an impedance stabilized load³ (d, custom made by the RWTH Aachen). It corresponds to a resistor with low pass filters placed in front. The load's monitoring outputs are terminated with 50 Ω resistors to avoid reflections. All connecting cables in this setup have an impedance of 50 Ω . The load's total resistance is about 4 Ω . The noise is measured in fully enclosed metal boxes. They are connected to the cables on the input and output side of the converter. These cables are coaxial cables and their metallic shields are connected to the copper plate's ground potential, while the centre core serves as power cable. The grounding is either performed via the coaxial cables' connectors or at the links to the bPOL2V5 evaluation board by connecting the shield directly to the plate (Figure 4.25). Inside the boxes, wires are arranged in the two different measurement modes (Figure 4.22) and are routed through a current clamp (e, Lindgren Mod. 94430-1 [30]). Their inductive signal is measured with a spectrum analyzer (f, Agilent Technologies EXA N9010A signal analyzer 9 KHz-3.6 GHz [31]). This arrangement guarantees separated potentials between measurement and noise signal [9].

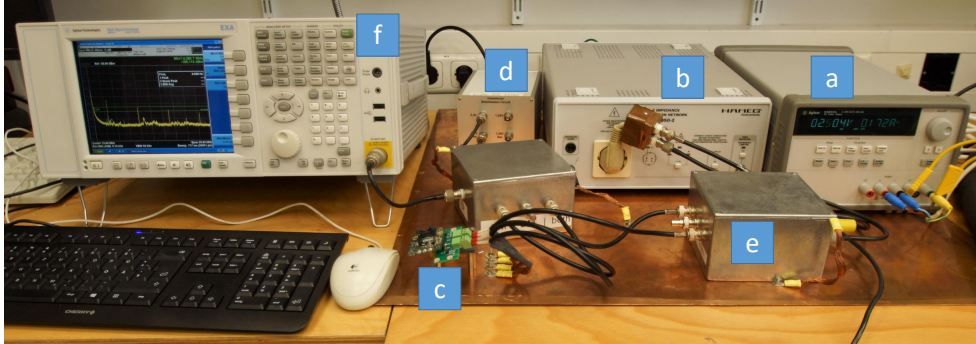


Figure 4.23: Setup for the measurement of the common and differential mode noise. Details are given in the text.

A DC-DC converter is the source of the voltage and the noise. While measuring the output noise, the ISL replaces the load and is the noise sink. During measurements at the input, the power supply is the noise sink. The signal induced in the current clamp is conducted through BNC cables, with an impedance of 50 Ω , to the spectrum analyzer. It measures frequency dependent the alternating current induced in the current clamp as a power ratio in decibel-milliwatts [dBm]. The power ratio L_P can be converted to the voltage ratio L_V , which is defined as ten times the logarithm of the ratio between incoming power and a reference power of 1 mW:

$$L_P[\text{dBm}] \equiv 10 \cdot \log \left(\frac{P_{\text{noise}}}{1 \text{ mW}} \right) .$$

³short ISL

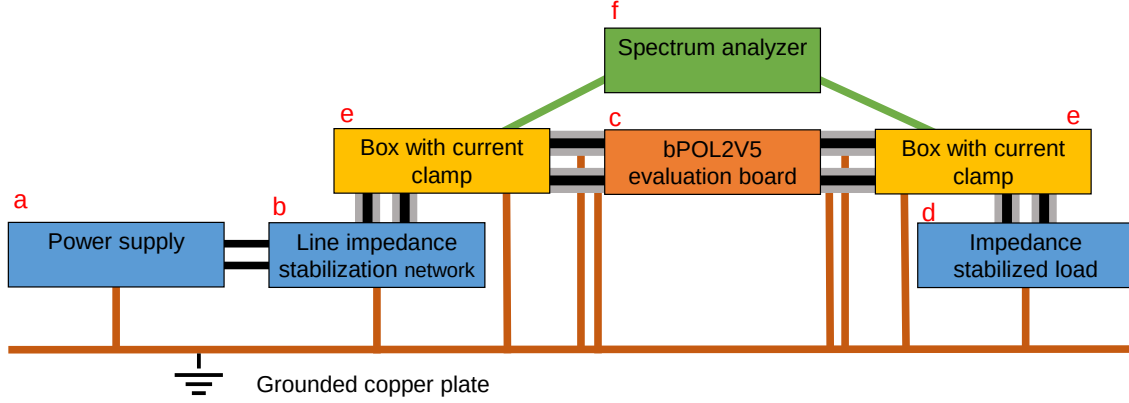


Figure 4.24: Schematic drawing of the setup to measure the DC-DC converter's common and differential mode noise.

Applying the formula for the electric power $P = \frac{V^2}{R}$ gives:

$$L_P[\text{dBm}] = 10 \cdot \log \left(\frac{V_{\text{noise}}^2}{R \cdot 1 \text{ mW}} \right) .$$

For the right side holds, after transformation and expanding with $1 \mu\text{V}$:

$$10 \cdot \log \left(\frac{V_{\text{noise}}^2}{R \cdot 1 \text{ mW}} \right) = 20 \cdot \log \left(\frac{V_{\text{noise}}}{\sqrt{R \cdot 1 \text{ mW}}} \right) = 20 \cdot \log \left(\frac{V_{\text{noise}}}{1 \mu\text{V}} \right) - 10 \cdot \log \left(\frac{R \cdot 1 \text{ mW}}{(1 \mu\text{V})^2} \right) .$$

The first term on the right side can be identified with the absolute power ratio L_V :

$$L_V[\text{dB}\mu\text{V}] \equiv 20 \cdot \log \left(\frac{V_{\text{noise}}}{1 \mu\text{V}} \right) .$$

The usage of BNC cables with a normed impedance Z_w of 50Ω gives for the second term:

$$10 \cdot \log \left(\frac{50 \Omega \cdot 1 \text{ mW}}{(1 \mu\text{V})^2} \right) = 106.989 .$$

We conclude:

$$L_V[\text{dB}\mu\text{V}] = L_P[\text{dBm}] + 106.989 . \quad (4.12)$$

In order to convert this voltage ratio to a current ratio (and thereby to the induced current), the transfer function of the current clamp is used. The manufacturer provides it in the data sheet [30]. A certain number of points is extracted from the calibration curve and via linear interpolation the frequency dependent impedance is calculated. With the transfer impedance Z and Ohm's law the current ratio

$$L_I[\text{dB}\mu\text{A}] = L_V[\text{dB}\mu\text{V}] - Z[\text{dB}\Omega]$$

follows. Each series of measurements is conducted by measuring the DM and CM noise on the input (DM In/CM In) and output (DM Out/CM Out) side. The frequency ranges from 150 kHz

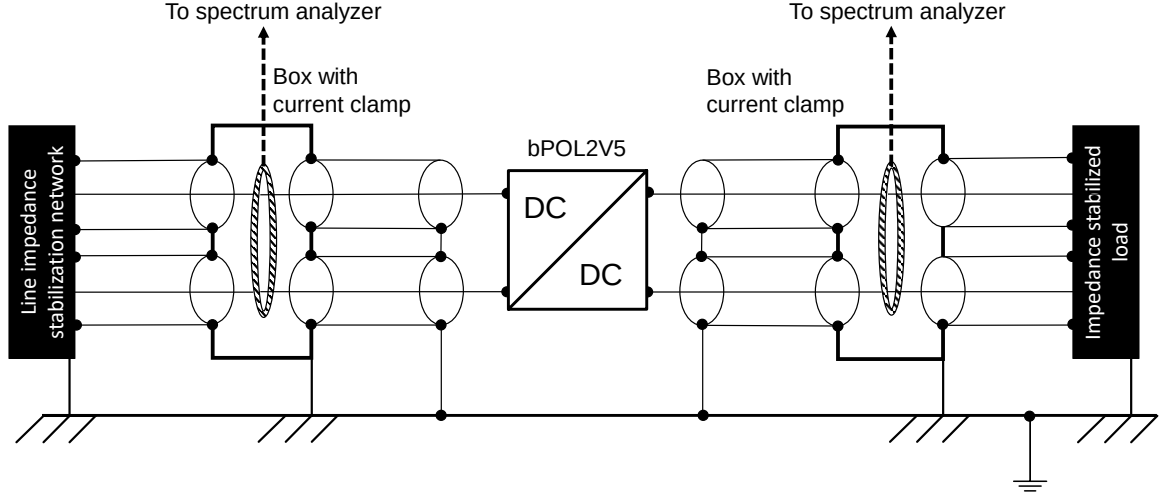


Figure 4.25: Simplified circuit diagram of the connection and grounding scheme of the setup to measure the common mode noise. To measure the differential mode noise the wires through the current clamp need to be rearranged (Figure 4.22).

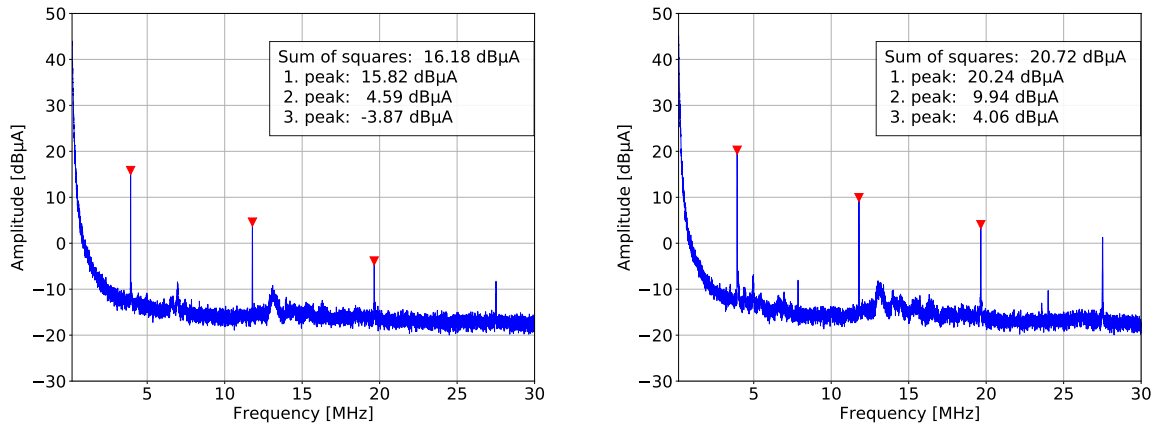


Figure 4.26: Exemplary spectra of the output differential mode noise (left) and output common mode noise (right) of a bPOL2V5 converter. Upon a continuous noise floor distinct peaks at the DC-DC converter's switching frequency and higher harmonics are visible. They are marked with red triangles. The plots also state the first three peak heights and their quadratic sum as a current ratio.

to 30 MHz. Figure 4.26 shows as an example the DM Out and CM Out measurement of the bPOL2V5 equipped with its default solenoid coil. Clearly visible is the noise floor, which is steadily decreasing with increasing frequency. Single peaks stand out of the noise floor. They occur at multiples of 4.0 MHz and therefore arise from the switching processes inside the bPOL. The height of those switching peaks is used to quantitatively compare different spectra. This is reasonable, since the scale is logarithmic and the peaks are only around three frequency bins wide. Nearly all signal is therefore concentrated in a single frequency bin per peak. A measure for the total noise is the quadratic sum of all peaks. It can be deduced in the following way. The induced current needs to be converted to absolute units

$$I = 10^{(\frac{L_I}{20})} \cdot 1 \mu\text{A} .$$

All currents are summed up quadratically:

$$\sqrt{\sum_i I_i^2} = \sqrt{\sum_i (10^{(\frac{L_{I,i}}{20})} \cdot 1 \mu\text{A})^2} .$$

Finally, this value is converted back to a current ratio:

$$\sqrt{\sum_i L_{I,i}^2} = 20 \cdot \log \left[\left(\sqrt{\sum_i (10^{(\frac{L_{I,i}}{20})} \cdot 1 \mu\text{A})^2} \right) \cdot (1 \mu\text{A})^{-1} \right] .$$

As stated above, two times the DM noise is measured. In logarithmic representation this corresponds to an offset of 6 dB μ A. This factor is not considered in the following studies, since we are mostly interested in relative differences. When absolute values, for example in the context of ISO standards, are explored, the factor needs to be applied. Earlier measurements yielded relative uncertainties for the peak heights of about 6 % and of 10 % for the quadratic sums [8].

4.3.2.2 Results

To examine the influence of the inductor choice on the bPOL2V5 common and differential mode noise, four different coils are studied in detail. Their main features are summarized in Table 4.3. This choice is motivated by Equation 4.11:

$$\Delta I = \frac{V_{\text{in}} - V_{\text{out}}}{Lf} D .$$

If one assumes that the noise is proportional to the alternating current and since all parameters except the inductance L are fixed on the bPOL2V5 evaluation board, the noise is expected to decrease inversely with the inductance. The coil geometry should not have a significant impact on the noise. Three different toroids with the same geometry, except for the number of windings, and the default solenoid are considered. Again, the 10-windings inductor is in terms of inductance and resistance similar to the solenoid, while of the two others one has a higher and one a lower inductance. The quantified comparison for all four coils for the most relevant cases (DM Out and CM Out) is shown in Figures 4.27 (highest peaks) and 4.28 (quadratic sums). The spectra can be found in Figures 4.29 and 4.30. The spectra look quite similar for all four coils. The peaks at odd multiples of 4 MHz are distinct, while the even ones are mostly suppressed. The suppression is strong in the DM, where the peaks are hardly visible in the noise floor, whilst they can be identified in the CM. With an increasing number of windings, and therefore increasing inductance, the height of the peaks decreases. The spectra of the solenoid and the comparable

Coil type	Material	Inductance [nH]	Resistance [mΩ]
Toroid inductor 6 windings	0.45 mm Cu	53	13
Toroid inductor 10 windings	0.45 mm Cu	94	17
Toroid inductor 16 windings	0.28 mm CCA15	225	90
Solenoid inductor	0.40 mm Cu	109	12

Table 4.3: Summary of the properties of the inductors that were used in the noise measurements.

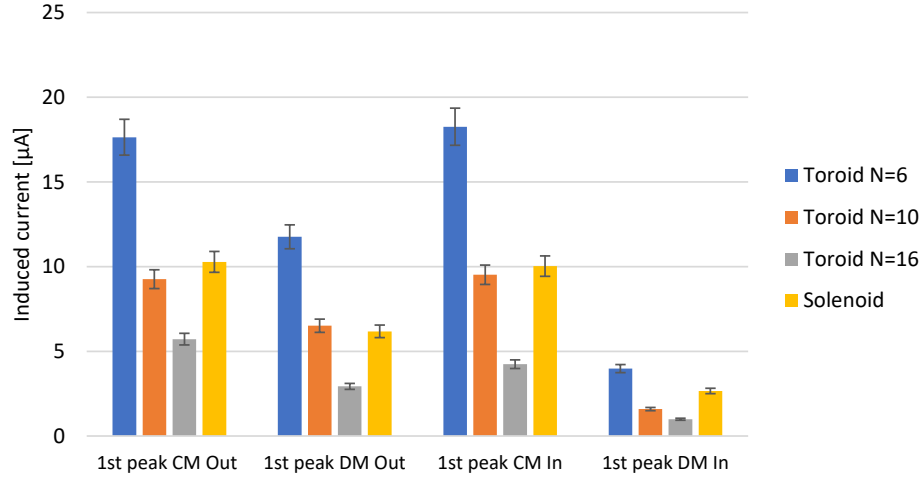


Figure 4.27: Summary of the results for the highest peak for the different coils and all four measurement modes.

toroid show no significant differences. In the quantified comparison, the results of the quadratic sums are dominated by the first and highest peak at 4 MHz. Therefore, the results in Figures 4.27 and 4.28 are very similar. The noise in the common mode is similar on the input and output side, and about a factor of 1/3 higher in the CM Out than in the DM Out. The DM In has the lowest noise, it is less than half of the noise in the DM Out. The noise decreases with a rising number of windings and the peak heights and quadratic sums of the solenoid and the comparable toroid are identical within their respective uncertainties.

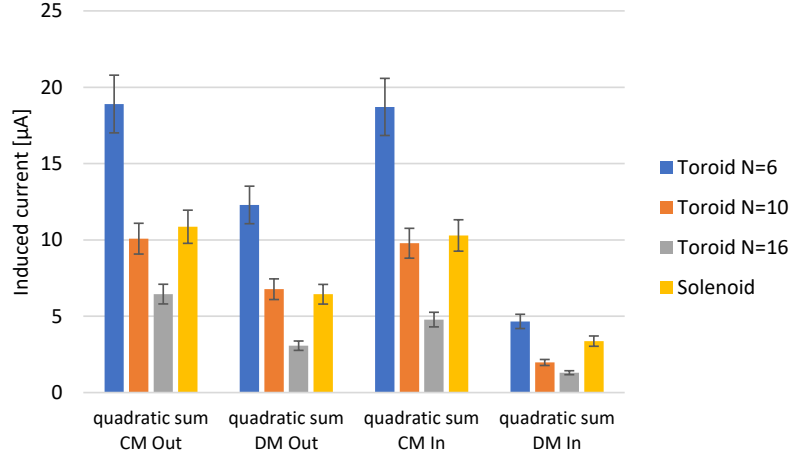


Figure 4.28: Summary of the results for the quadratic sum for the different coils and all four measurement modes.

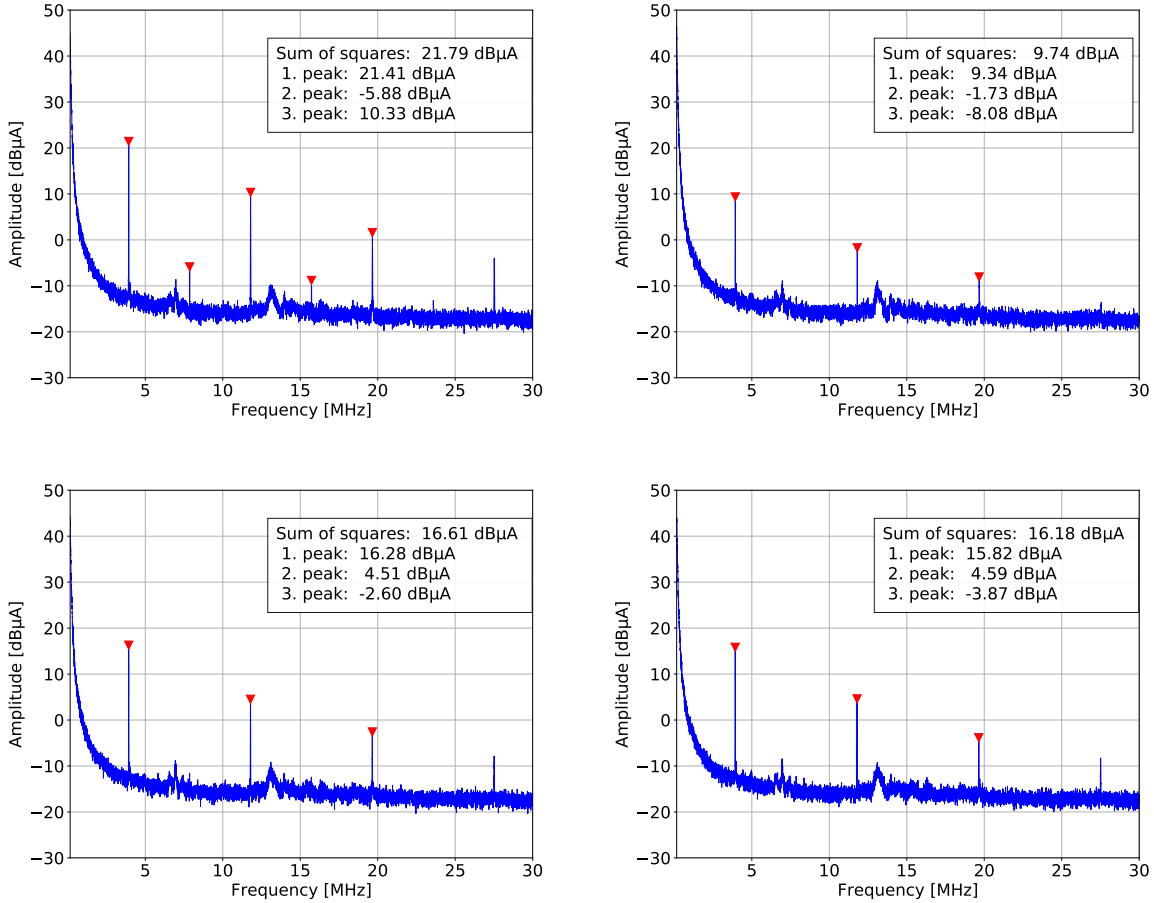


Figure 4.29: Output differential mode noise spectra of the bPOL2V5 evaluation board for four different inductors. Top left: 6 windings toroid. Bottom left: 10 windings toroid. Top right: 16 windings toroid. Bottom right: default solenoid.

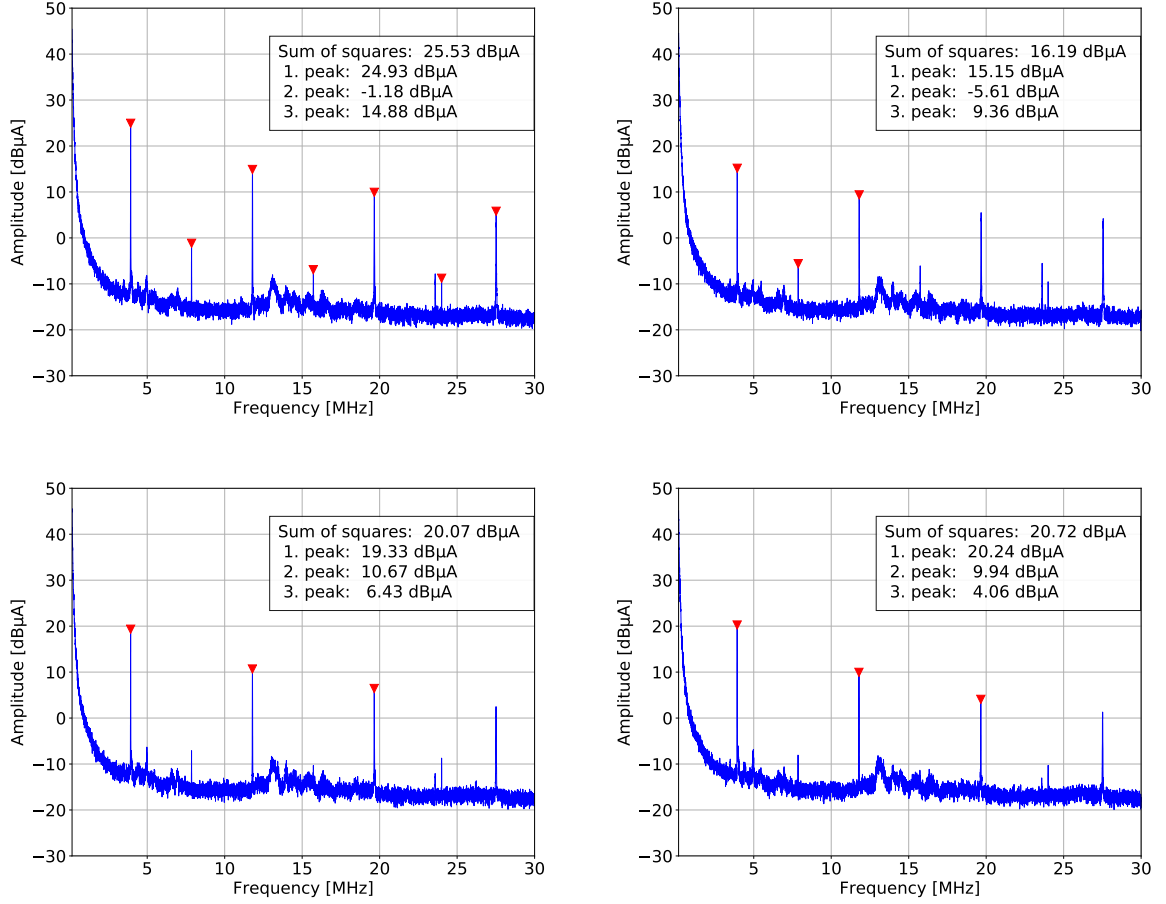


Figure 4.30: Output common mode noise spectra of the bPOL2V5 evaluation board for four different inductors. Top left: 6 windings toroid. Bottom left: 10 windings toroid. Top right: 16 windings toroid. Bottom right: default solenoid.

In order to verify the relation between noise and inductance, additional measurements are conducted with various coils of the parameter studies presented in Section 4.2. The quadratic sum of the DM Out and CM Out is measured and plotted against the inductance and the inverse inductance. The results are shown in Figure 4.31 and Figure 4.32. As visible from the linear fit, the measurements confirm the expectation of an inverse relationship between inductance and noise. No dependency of the noise on the resistance is observed in the course of the measurements. One can conclude that there is no significant difference in terms of noise in replacing the solenoid inductor with a toroid of similar properties. An increase in coil inductance leads to less noise. Therefore, simply increasing efficiency by using fewer windings and decreasing inductance comes at the cost of additional noise.

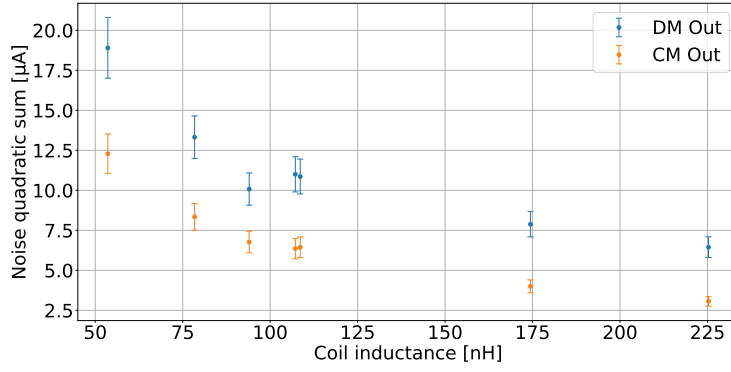


Figure 4.31: Quadratic sum of the output noise for various inductors plotted as a function of their inductance.

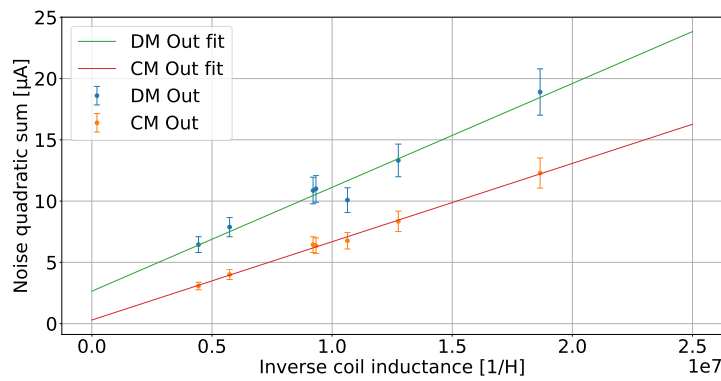


Figure 4.32: Quadratic sum of the output noise for various inductors plotted as a function of their inverse inductance, together with linear fits to the data.

4.3.3 Electromagnetic radiation

An important argument for the use of toroidal coils over solenoid coils is the reduction of electromagnetic radiation of the DC-DC converter's main inductor. The service hybrids will be placed in close proximity to the silicon sensors and the readout electronics. The main inductors radiate an electromagnetic field corresponding to their internal alternating currents. To measure the radiation and to illustrate the differences between the coil designs, a setup initially designed by Jan Sammet is used [15].

4.3.3.1 Setup

The setup to measure the field above the DC-DC converter is schematically shown in Figure 4.33. The DC-DC converter (a in Figure 4.33) is powered by a power supply (b, Agilent E3633A DC power supply [25]). A pick-up coil (c, ETS-Lindgren model 7405-703 [32]) records the radiated field and the induced voltage is measured with a spectrum analyzer (d, Agilent Technologies EXA N9010A signal analyzer 9 KHz-3.6 GHz [31]). BNC cables connect it to the pick-up coil. The area above the DC-DC converter is scanned by a controller unit (e, isel CNC controller C142-4 [33]) steering a xyz -stage (f, two isel LES 4 linear units [34] and one isel 5 linear unit [35] driven by two MS160 and one MS300 two-phase step motors [36, 37]). For a given separation in the vertical (z) direction, it scans in a 1 by 1 mm grid. During a measurement, a power ratio in dBm and the spatial coordinates are recorded for each point of the grid. The power ratio corresponds to the maximal power ratio in the frequency interval 4.0 ± 0.5 MHz. According to

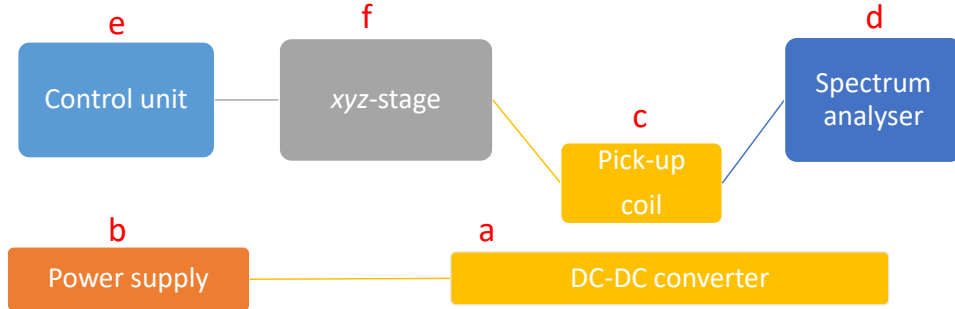


Figure 4.33: Schematic drawing of the setup to measure the DC-DC converter's electromagnetic radiation [8].

Equation 4.12 the power ratio can be converted to a voltage ratio:

$$L_V[\text{dB}\mu\text{V}] = L_P[\text{dBm}] + 106.989 .$$

This can be transformed to the voltage induced in the pick-up coil:

$$V_{\text{noise}}[\text{mV}] = 10^{\frac{L_P[\text{dBm}] + 106.989}{20}} \cdot 1000 \frac{\text{mV}}{\mu\text{V}} .$$

The transfer function of the pick-up coil is unknown, therefore the voltage cannot be transferred to a current or the absolute magnetic field. The following results will hence be stated in millivolt. The scanned area is $30 \times 30 \text{ mm}^2$ wide with its centre roughly above the middle of the inductor under test. The pick-up coil is placed around 1 mm over the inductor to avoid collisions and the resulting movements that spoil the measurement. In order to receive comparable results,

the vertical distance between the inductor and the pick-up coil needs to be as small as possible and fairly constant across all measurements. The strength of the electromagnetic field decreases rapidly with the distance to the source. For a qualitative discussion, the mere scan pictures are sufficient (for example Figure 4.35). The maximal induced voltage and the induced voltage averaged over all points serve as additional quantified measures. Earlier measurements yielded uncertainties of 0.07 mV for the maximum voltage and 0.001 mV for the average voltage.

4.3.3.2 Comparison between the electromagnetic radiation of a solenoid and a toroid inductor

The default 100 nH solenoid is compared to the 10-windings toroid made of 0.45 mm copper wire, which mimics closest the solenoid's properties. This is done in order to highlight the differences in geometry rather than other coil properties. Both coils are plugged onto the evaluation board and scans are performed with the pick-up coil oriented in the xy -, xz -, and yz -plane, thus measuring the z -, y -, and x -component of the magnetic field, respectively. The axes' orientation is according to the left picture in Figure 4.34, with the z -axis pointing up. For the scan in the yz -plane, the DC-DC converter needs to be rotated by 90° clockwise, due to the geometry of the setup.

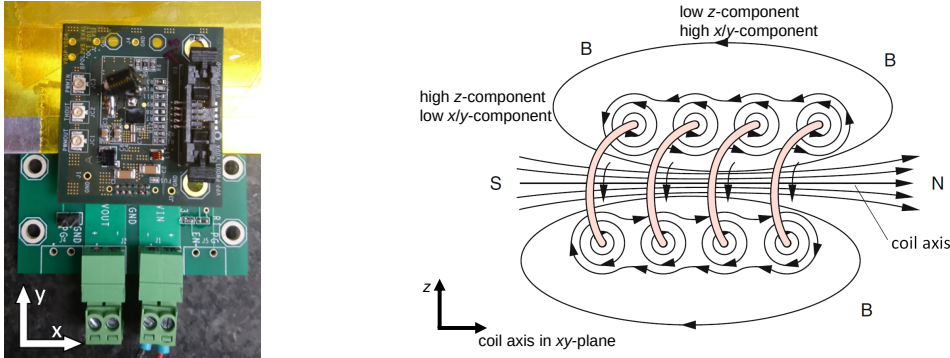


Figure 4.34: The left figure shows a picture of the bPOL2V5 evaluation board equipped with the plug extension. The coordinate system used in the scans is shown, too. The z -axis is pointing up. The right figure shows the magnetic field of a solenoid coil [38].

Figure 4.35 shows the scan of the z -component of the radiated magnetic field in the xy -plane. Since both voltage scales are the same, one can clearly see that the radiation is much lower when the toroid is used. The solenoid scan also features the dipole structure one would expect of the z -component of the field above a solenoid (Figure 4.34). The field of the toroid inductor has a dipole-like structure, too. This is not expected, since the rotational symmetry of the toroid should translate into a symmetry of the field. However, this feature can be identified with the coils' connecting wires, as shown below. The scans in the xz -plane (Figure 4.36) and yz -plane (Figure 4.37) are compatible with the assumption of a dipole field in the direction of the solenoid's coil axis or the toroid's plug, respectively. As indicated in Figure 4.34, the x - and y -components have their maxima above the centre of the coil. In these two cases, the induced voltage is smaller, since the pick-up coil needed to be turned and is placed higher above the radiating inductor. In all cases, the toroid's radiation is smaller than the solenoid's. The quantified values are given in Table 4.4.

	Maximum induced voltage [mV]	Average induced voltage [mV]
Toroid inductor xy -plane	2.67	0.984
Solenoid inductor xy -plane	7.04	2.100
Toroid inductor xz -plane	1.67	0.457
Solenoid inductor xz -plane	3.33	0.893
Toroid inductor yz -plane	0.57	0.251
Solenoid inductor yz -plane	3.43	0.837
Spaced connections toroid	1.50	0.538
Twisted connections toroid	1.06	0.200

Table 4.4: Summary table of the maximum induced voltages and average voltages, which have been measured in the scans.

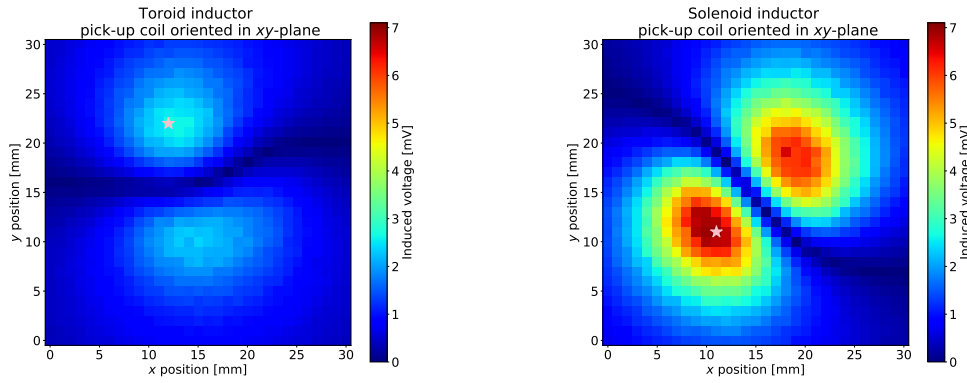


Figure 4.35: Scans of the z -component of the radiated magnetic field of a toroidal inductor (left) and a solenoid inductor (right). The scans are centred above the coil. A pink star indicates the maximal magnetic field.

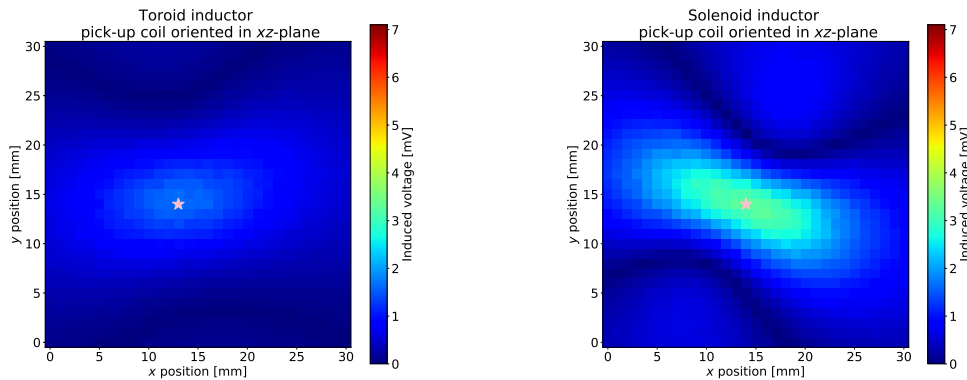


Figure 4.36: Scans of the y -component of the radiated magnetic field of a toroidal inductor (left) and solenoid inductor (right). The scans are centred above the coil. A pink star indicates the maximal magnetic field.

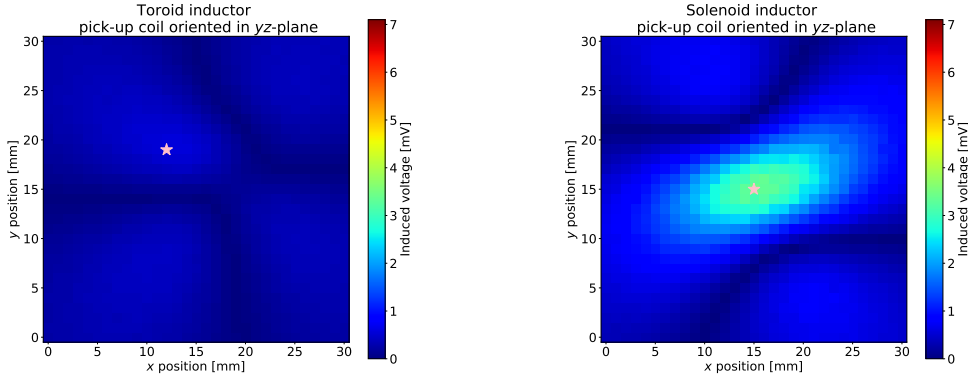


Figure 4.37: Scans of the x -component of the radiated magnetic field of a toroidal inductor (left) and solenoid inductor (right). The scans are centred above the coil. A pink star indicates the maximal magnetic field.

To illustrate the influence of the wires, which are needed to connect the coil to the plug, on the coil radiation, an extreme case is considered. A 10-windings, 0.28 mm CCA15 toroid with surplus wire (Figure 4.38) is examined in two different configurations. First, the surplus wire is left untwisted, forming an open and big loop below the inductor. In a second measurement, these wires are twisted below the inductor. The results are shown in Figure 4.39. Due to the long connection, the inductor was placed far above the other DC-DC converter components, so their influence is negligible. The untwisted scan shows clearly a dipole like structure of high field strength. Note that the scale has changed in comparison to Figures 4.35, 4.36, and 4.37. The twisted scan indicates a much smaller radiation. However, there is still some dipole like contribution, as already seen in the first measurements. The area with contributions significantly above the noise floor is much smaller, which translates to a much smaller average value (Table 4.4). The higher noise floor and its contributions for the toroid considered in Figures 4.35, 4.36, and 4.37 are related to the shorter surplus wire. The pick-up coil was placed much closer to the DC-DC converter and the loop formed by the connector pins.

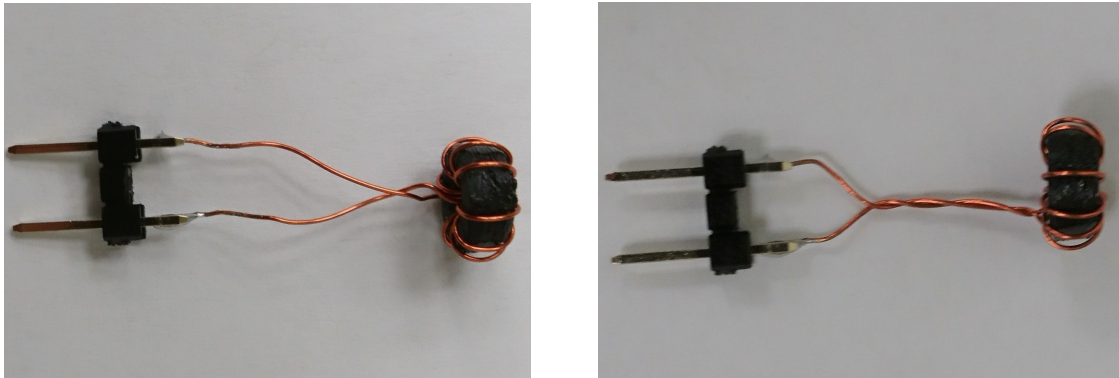


Figure 4.38: Pictures of the coil, which has been scanned for Figure 4.39. On the left, the toroid has openly spaced connection wires. On the right, it has twisted connection wires.

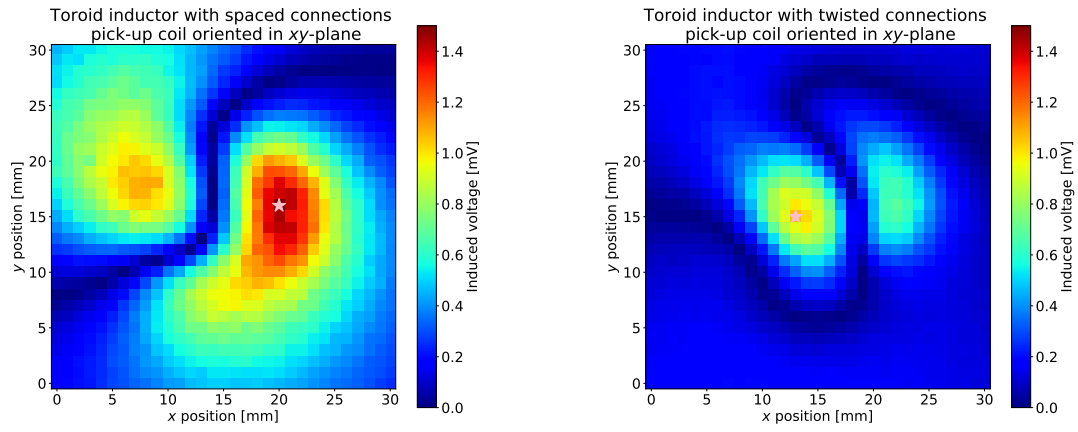


Figure 4.39: Scans of the z -component of the radiated magnetic field of a toroidal inductor with openly spaced connection wires (left) and twisted connection wires (right). The scans are centred above the coil. A pink star indicates the maximal magnetic field.

4.4 Conclusion on coil development

As a last aspect of the coil design, the material consumption needs to be discussed. It was made clear that in order to achieve high efficiency, the DC resistance of the inductor needs to be small. Since the length of the wire is more or less fixed for a given coil inductance, the two interesting parameters here are wire diameter and wire material. If one can choose freely, the resistance can be chosen at will by using a very thick wire and highly conductive material (e.g. copper). However, during the layout phase for the Phase-2 tracker, assumptions were made [6] for the amount of material allowed in the tracking volume, in order to keep the absorption low. In this material budget each DC-DC converters' main inductance is considered with 13.1 mm^3 aluminium and 5 mm^3 copper. The proposed material is, therefore, copper-clad aluminium with 28 vol-% copper. The material consumptions of some 100 nH coils considered so far are summarized in Table 4.5. All toroids are assumed to have a wire length of 19 cm. The table states the resistance in units per length. The wire for the solenoid is only about half the length of the toroid wire. Only the first toroid (made of 0.28 mm CCA15 wire) stays within the limits of the material budget. The other coils, including the solenoid, use full copper wires and, therefore, consume much more copper by design, but no aluminium. Aluminium has only 64 % of the electric conductivity of copper. However, its density is a factor of 3.3 smaller and the radiation length even by a factor of 6. Hence, it is desirable to use CCA wires. The copper cladding provides the same soldering options as for a full copper wire. Two parameter options for toroid coils made of CCA wire are presented in Table 4.6. The first choice would use a known to be available CCA15 wire. The diameter is chosen in a way to match the copper budget. This results in a 45 % higher aluminium consumption. The second option yields the use of the full material budget. It needs to be confirmed, whether the required wire material and diameter can be acquired. Both choices provide a higher resistance than the default solenoid, which limits efficiency. In the course of the optimization of the DC-DC converter efficiency, a trade-off needs to be made between the coil resistance and the material budget.

Type	Wire- $\emptyset$	Material	R/l [Ω/m]	V [Al]	V [Cu]
Toroid	0.28 mm	CCA15	0.419	9.94 mm^3	1.75 mm^3
Toroid	0.45 mm	Cu	0.105	0	30.2 mm^3
Toroid	0.30 mm	Cu	0.240	0	13.4 mm^3
Solenoid	0.40 mm	Cu	0.137	0	11.9 mm^3

Table 4.5: Material consumption of examined inductors with roughly 100 nH inductance.

Type	Wire- $\emptyset$	Material	R/l [Ω/m]	V [Al]	V [Cu]
Toroid	0.47 mm	CCA15	0.150	19 mm^3	5 mm^3
Toroid	0.35 mm	CCA28	0.250	13.1 mm^3	5 mm^3

Table 4.6: Material consumption for proposed inductors with roughly 100 nH inductance, that would stay within the coil's copper material budget.

To conclude, it is possible to replace the solenoid inductor of the bPOL2V5 with a toroid inductor. No significant difference in terms of efficiency and differential and common mode noise was observed when a similar inductance and resistance was used. Scans of the electromagnetic radiation show the advantage of the toroid, whose field is mainly contained inside the coil volume. A high inductance is favourable to achieve low noise and a higher efficiency for small output

currents. For the operational output current the direct current losses dominate and a low resistance is advised. The suggested parameters for the toroid inductor of the bPOL2V5 are listed in Table 4.7. The geometry is the same as for the coils already used on the 2S service hybrid. This reduces the number of coil cores that need to be produced. The inductance depends strongest on the number of windings. The wire was chosen according to the material budget. Additional requirements, like a smaller core size, could be easily incorporated, if necessary.

Number of windings	10
Height	3.1 mm
Outer radius	3.55 mm
Inner radius	1.5 mm
Wire material	CCA28
Wire- $\emptyset$	0.35 mm
R/l	$0.250 \Omega/\text{m}$

Table 4.7: Parameters for the favoured toroid inductor.

5 2S service hybrid test board

Roughly 7,700 2S modules with an estimated cost per module of 3,500 CHF will be needed for the Phase-2 outer tracker [4]. Each of the modules will host a service hybrid, with the functionalities laid out in Chapter 3. Since the malfunction of any major aspect of the service hybrid leads to the loss of the total module, only fully functional hybrids are allowed to be used in module assembly. To ensure the functionality of the modules and to monitor service hybrid production, a quality assurance plan was introduced. For the hybrid production, it consists of “(i) tests done by the vendor, which should be as exhaustive as possible, (ii) special verifications on the process quality (including destructive tests on samples), carried out by the institute responsible of the procurement, and (iii) full QC [quality control] on individual circuits (inspection and functionality tests), initially also done by the responsible institute, and then distributed to the module assembly lines, while the responsible institute will continue with sample testing.” [4]. In parallel to the service hybrid development, a dedicated test board, which is able to explore all functionalities of the service hybrid, was devised. It can be used in all three envisioned phases of the quality control and is designed to be scalable according to the needs. This chapter covers the layout and functions of the test board and its components. Measurements regarding the commissioning of prototypes and plans for a cooling system are presented.

My work in the scope of this thesis included the first commissioning of test board prototypes. *Python* software has been prepared to communicate with and read out a number of components associated with the test board’s Raspberry Pi miniature computer. Their functionality and capabilities have been tested with and without connected service hybrids. The goal of these studies was to earn a general understanding of the test board’s suitability for the service hybrid testing and to point out currently present shortcomings of the design. A graphical user interface and a cooling system have been designed.

5.1 Layout and components

The test board was designed to cover all aspects of the service hybrid functionalities. The procedure to test these functionalities can be divided into three major sets of test: (a) a data link test, confirming the LpGBT’s ability to send and receive data from the FE hybrids and to communicate with the back-end, (b) a power test, measuring the DC-DC converters’ output voltages and efficiencies and the integrity of the high voltage circuit, and (c) a slow control and clock test, verifying the proper distribution of clock and (hard-)reset signals of the LpGBT as well as I²C communication and power monitoring capabilities. The placement of most major test board components is shown in Figure 5.1. A graphical representation of the test sets and the full schematics can be found in Appendix B and C.

(a) Data link test (Figure B.1)

To emulate the service hybrid data stream to and from the FE hybrids, the test board hosts two GBTx ASICs, one for each side. They receive their supply voltage from a power regulator (Analog Devices LTM4643 [39]). It is powered with 5 V by an external power supply. The GBTx

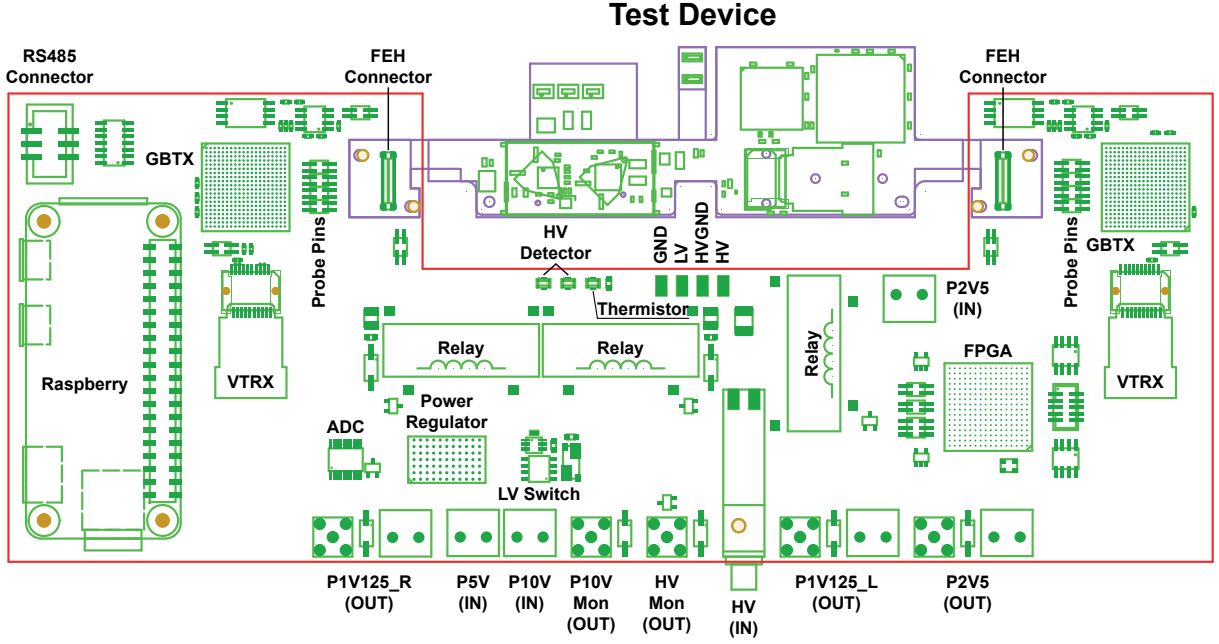


Figure 5.1: Sketch of the test board with the placement of the major components [40].

ASICs are linked to VTRx connectors (Mouser 1888247-1), in order to be optically connectable with a back-end board with an FPGA (GLIB [41] or FC7 [42]). The board runs a back-end emulation software. The test board is equipped with the same connectors as the FE hybrids (Panasonic AXF5A5012), so a service hybrid under test can be directly connected. To profit from the experience gained during the development of the service hybrid, the choice to use the GBTx and VTRx was made. The general idea of the test procedure is that the back-end board's FPGA produces a pseudo-random data pattern. It is transferred via optical fibres to the test board's VTRx and is unpacked by the test board's GBTx and forwarded to the service hybrid on the FE hybrid connector's data lines. To the service hybrid, the provided data look like the output of the FE hybrids. After it has been processed by the LpGBT and the VTRx+ and has been received back by the back-end, the data can be compared to the expected service hybrid output. The GBTx ASICs can be configured remotely via I²C. The test board holds two plugs, which are compatible with a USB to I²C converter. Software for a PC is provided by the GBTx designers for the configuration.

(b) Power test (Figure B.2)

While the data link test is managed solely by the back-end board, the power test is managed by a Raspberry Pi Zero W (later named Raspberry Pi). It is a small sized yet fully functional computer. Detailed information on the Raspberry Pi and its communication can be found in Section 5.2. The Raspberry Pi controls the low and high voltage powering of the service hybrid. The service hybrid power is provided by external power supplies and routed through the test board and appropriate connectors to the service hybrid. It is controlled by the Raspberry Pi with a switch (Infineon ISP772T) or, in the case of the high voltage, a relay (Standex Meder KT05-1A-40L-SMD, driven by an On Semiconductor SZNUD3160 inductive load driver). Both kinds of switches are controlled by the Raspberry Pi with a 3.3 V logical signal. The already mentioned FE hybrids connector routes the DC-DC converter output voltage back to the test board, where

it is measured with an analog-to-digital converter (Analog Devices AD7998 ADC [43]) for both sides separately. The analog-to-digital converter (ADC) is connected to the Raspberry Pi via I²C lines. The high voltage is returned to the test board with dedicated cables, which mimic the high voltage pigtailed glued to the sensor, but have plugs at both ends. In this way, the return voltage can be measured by the ADC, too. However, this requires the use of a voltage divider to adjust the voltage level. Two additional relays need to be switched by the Raspberry Pi to allow a measurement. The ADC can also measure the RSSI voltage of both VTRxs on the test board. In order to perform efficiency measurements, the output voltage can be connected to an external load. Additionally, the service hybrid's input voltage and current can be measured via a power and current monitor (Texas Instruments INA226 [44]). The bus voltage (the applied voltage to the service hybrid) and shunt voltage (the voltage drop across a given shunt resistor) can be measured. The current is determined from the voltage drop over the shunt resistor. The readout is managed via I²C lines.

(c) Clock and slow control test (Figure B.3)

The last set of tests requires the use of the back-end board and the Raspberry Pi. In the commissioning phase, both can be controlled manually. During mass production and testing, both will be controlled and synchronized via a central server. Two components on the test board are dedicated to these tests. To test both of the service hybrid's LpGBT I²C lines, two serial I²C F-RAMs (Cypress FM24V02A [45]) are placed on the test board. They are connected to the I²C lines of the FE hybrid connector. Note that these I²C lines are independent of each other and of the I²C lines used by the Raspberry Pi. To test the communication, the back-end will initialize I²C transactions of the LpGBT, which will write random yet known data to certain F-RAM registers. Later, this data will be read back in the same way and checked for faults. The integrity of the clock and reset signal lines are validated with help of an FPGA (Intel Cyclone III EP3C16F256C6 [46]). A custom firmware allows the Raspberry Pi, which is connected to the FPGA via SPI¹ communication, to control the tests. The firmware is used to count clock cycles during a given time window, or to count reset signals, while a gate is open. These signals can be measured separately for both sides. The test board FPGA is also capable of setting an AMUX² voltage to check the functionality of the LpGBT's internal ADCs. In a setup with multiple test boards, these tests require a synchronization between the different Raspberry Pis and the corresponding back-end boards.

The test board features a number of additional components, which are not solely dedicated to a given test. The Raspberry Pi is connected to an RS-485 connector. It is available as a secondary option for the connection to the server. The primary option, which has been explored in this thesis, is a wireless LAN connection. A temperature sensor (Texas Instruments LM95071 [47]) is placed on the test board for monitoring. To test the functionality of the FPGA, a 40 MHz oscillator is implemented. Several probe pins are available to check power and data lines of various components.

¹Serial Peripheral Interface

²Analog Multiplexer. A general term for signal inputs and outputs. In this case, it refers to a static voltage output.

5.2 Raspberry Pi communication and interfaces

A major characteristic of the test board is the effort to create a modular system. Each test board is supposed to run individually. Only minimal communication during a test sequence, e.g. to initiate necessary actions by the back-end board, will be required. This minimal communication approach is only possible by equipping each test board with its own computer, which is responsible for running the test procedure, storing the log data and uploading the test results to a central server. For this purpose, the Raspberry Pi Zero W was selected. It is a single-board computer, about the size of a credit card, and has been originally developed to promote the teaching of basic computer science in schools and in developing countries [48]. A picture is provided in Figure 5.2. A central feature is a Broadcom BCM2835 chip with a one-core CPU running at 1 GHz and a 400 MHz GPU. The Raspberry Pi design is advantageous for the use on the test board. It hosts a two-rowed 40-pin plug, which can be directly attached to the test board. These pins provide native I²C, SPI, and GPIO³ lines and allow the Raspberry Pi's powering without the use of the micro USB power input and additional cables. Its operation system *Raspbian* is a free operating system based on *Debian* optimized for the Raspberry Pi hardware. It is stored on a removable MicroSD card. In the event of a hardware failure, the board can be exchanged and no reprogramming is necessary, since all data is stored on the SD card. A screen, keyboard, and mouse can be attached via the mini-HDMI and micro-USB connector during prototyping and for debugging. The Raspberry Pi supports wireless LAN and can, therefore, be integrated into a network without the need for additional cables. The Raspberry Pi has 512 MB RAM [48]. The most important characteristics are summarized in Table 5.1.

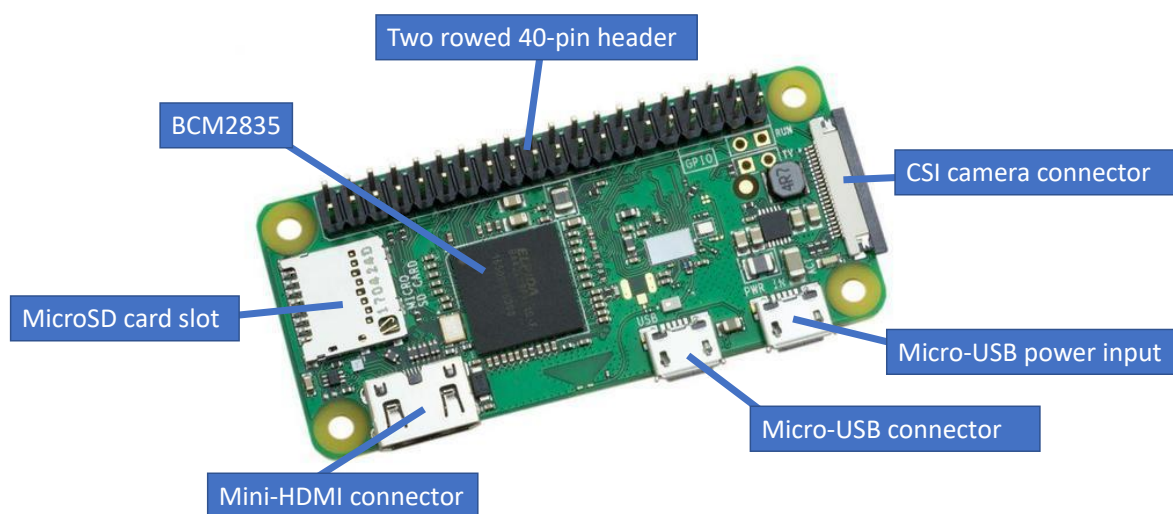


Figure 5.2: Picture of a Raspberry Pi Zero W. The most important features are labelled [49].

5.2.1 Interfaces for the on-board communication

The *Raspbian* operating system allows the use of different native interfaces, three of which are discussed below: GPIO pins, SPI bus, and I²C bus. Each interface can be controlled with dedicated *Python* libraries. Python is an interpreted and object-oriented programming language. It embodies a high number of modules, data types, and classes. Python combines a high function-

³General Purpose Input and Output

Price	10 \$
CPU	BCM2835, 1 core, 1 GHz
GPU	Broadcom Dual Core VideoCore IV, Full HD 1080p30, 400 MHz
RAM	512 MB
Data storage	MircoSD
Network	WLAN, BCM43143 2.4 GHz, b/g/n
Pins/GPIO pins	40/26
Power consumption	100-140 mA at 5 V

Table 5.1: Summary of the key parameters of the Raspberry Pi Zero W [49].

ality with a clear syntax. It features interfaces to many system calls and libraries, as well as to various window systems. The programming language is extendable in C or C++. It can also be used for applications that need a programmable interface. Python runs on many Unix variants (including *Raspian*), on Macintosh operating systems, and on Windows 2000 and later [50].

5.2.1.1 GPIO

The main functionality of GPIO pins is the setting or reading of a single static logical bit. The voltage level of the Raspberry Pi's logic is positive 3.3 V for a 1 and 0.0 V for a 0. The test board utilizes this interface to enable the switch controlling the low voltage supply to the service hybrid and to switch the three HV relays. Note that the used *Python* library and the Raspberry Pi itself are not suited for real-time or timing-critical applications. The general use of GPIO pins is presented in the code below.

```

1 import RPi.GPIO as GPIO
2 GPIO.setmode(GPIO.BOARD)
3 GPIO.setup(40,GPIO.OUT)
4 GPIO.output(40,GPIO.HIGH)

```

Listing 5.1: *Python* code example for the use of GPIO pins on the test board. In this case the low voltage switch of the service hybrid is activated.

After the *RPi.GPIO* library [51] has been imported, the numbering scheme of the Raspberry Pi's pins is set. The general pin-out is given in Figure 5.3. The Raspberry Pi has 40 pins, of which 26 can be used as GPIO pins, while the others either supply 3.3 V, are inputs for the 5 supply voltage, or are ground pins. Several GPIO pins are reserved for certain applications (e.g I²C, see below). The GPIO pins can be sorted by their number (2-27) or by their board position (1-40). Although most literature sources use the number, here the board position is used, since it conforms with the test board schematics. Line 3 connects the *Python* code to pin 40 and configures it as an output. The last line of code enables the output. A voltage of 3.3 V is applied to the pin, which enables the LV supply to the service hybrid.

5.2.1.2 SPI bus

The SPI bus is a four-wire serial bus with a master-slave architecture. The master device originates the frame for reading and writing. The serial clock (SCLK) is an output from the master, while the master-out-slave-in line (MOSI) is a data output from the master. The slave's data output is the master-in-slave-out line (MISO). These lines serially connect all slave devices and the master. Additionally, each slave has a dedicated slave select (SS) line connected to the

name	pin number		pin number	name
3.3 V DC Power	1			2 5 V DC Power
GPIO 02 (SDA1, I2C)	3			4 5 V DC Power
GPIO 03 (SCL1, I2C)	5			6 Ground
GPIO 04 (GPIO_GCLK)	7			8 GPIO 14 (TXD0)
Ground	9			10 GPIO 15 (RXD0)
GPIO 17 (GPIO_GEN0)	11			12 GPIO 18 (GPIO_GEN1)
GPIO 27 (GPIO_GEN2)	13			14 Ground
GPIO 22 (GPIO_GEN3)	15			16 GPIO 23 (GPIO_GEN4)
3.3 V DC Power	17			18 GPIO 24 (GPIO_GEN5)
GPIO 10 (SPI_MOSI)	19			20 Ground
GPIO 09 (SPI_MISO)	21			22 GPIO 25 (GPIO_GEN6)
GPIO 11 (SPI_CLK)	23			24 GPIO 08 (SPI_CE0_N)
Ground	25			26 GPIO 07 (SPI_CE1_N)
ID_SD (I2C ID EEPROM)	27			28 ID_SD (I2C ID EEPROM)
GPIO 05	29			30 Ground
GPIO 06	31			32 GPIO 12
GPIO 13	33			34 Ground
GPIO 19	35			36 GPIO 16
GPIO 26	37			38 GPIO 20
Ground	39			40 GPIO 21

Figure 5.3: Pin-out of the Raspberry Pi Zero W [48].

master. The SS lines are active low and only the slave seeing a logical zero is listening to the clock and MOSI line. The other lines are low while idle. There is no further addressing or acknowledging. The connection concept is sketched in Figure 5.4. The Raspberry Pi uses the SPI bus to read out a temperature sensor and to communicate with the test board's FPGA. It is always the master. Upon seeing an active low on its SS line and receiving a clock, the temperature sensor simply clocks out two bytes of temperature data [47]. The two bytes can be translated to a 13-bit absolute temperature (Figure 5.5 and Section 5.2.1.4). The corresponding *Python* code is shown in Listing 5.2 below. It utilizes the pre-installed *Pigpio* library⁴ [52]. The Raspberry pins 19, 21, and 22 host the MOSI, MISO and SCLK line, respectively. Pin 24 selects the slave 0 and pin 26 the slave 1. The first function establishes a connection to the local Raspberry Pi and sets up slave 1 with a baud rate of 100,000 bits per second. Then, the two bytes of temperature data are read from the sensor and converted according to its data sheet specification by the second function. Afterwards, the connection is closed. The least significant bit (LSB) corresponds to 0.03125 K (13-bit signed integer times LSB = temperature in °C).

⁴Before the library can be used, the *Pigpio* daemon needs to be launched by executing the command 'sudo pigpiod' in the Raspberry Pi's command line.

```

1  import pigpio
2
3  def mea():
4      pi=pigpio.pi()
5      spi1=pi.spi_open(1,100000)
6      temp=pi.spi_read(spi1,2)
7      pi.spi_close(spi1)
8      pi.stop()
9      return(converter(temp[1]))
10
11 def converter(array):
12     if array[0]<128:
13         return ((array[0]<<6)|(array[1]>>2))*0.03125
14     else:
15         return ((-1<<14)|((array[0]<<6)|(array[1]>>2))*0.03125

```

Listing 5.2: *Python* code example of the readout of the test board temperature sensor. No configuration is required, the sensor clocks out data upon seeing a clock. The conversion of the temperature data is explained in detail below.

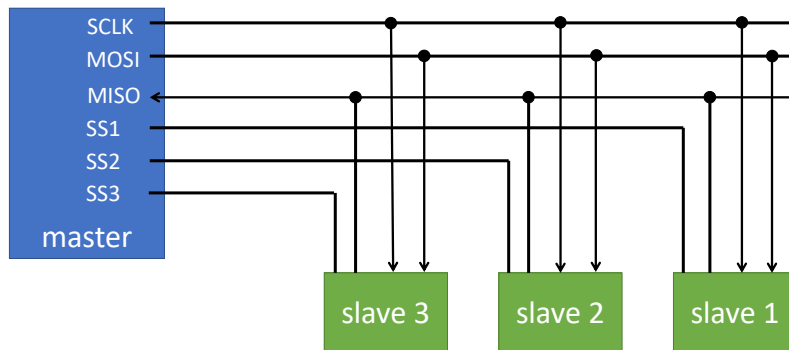


Figure 5.4: Schematic drawing of the SPI bus concept. The master and the slaves are connected with a serial clock, a master input data line and a master output data line. Additionally, each slave has a dedicated select line.

The FPGA communication uses a set of one-byte codes (also called ‘opcode’, Figure D.1 in the Appendix). The codes divide into two groups. Some codes only send a command, e.g. initializing a clock count or resetting a counter. These codes are only sent on the MOSI line. If the code belongs to the group of reading commands, e.g. read the measured number of clock cycles or the number of resets, the FPGA will send two bytes of data on the MISO line during the following 16 clock cycles (two times eight). The general form of the necessary *Python* code is given in Listing 5.3 below. After the connection to slave 0 has been established, the command (in this case 2_{hex}) is written to the slave. If necessary, two bytes are read back, before the connection is closed.

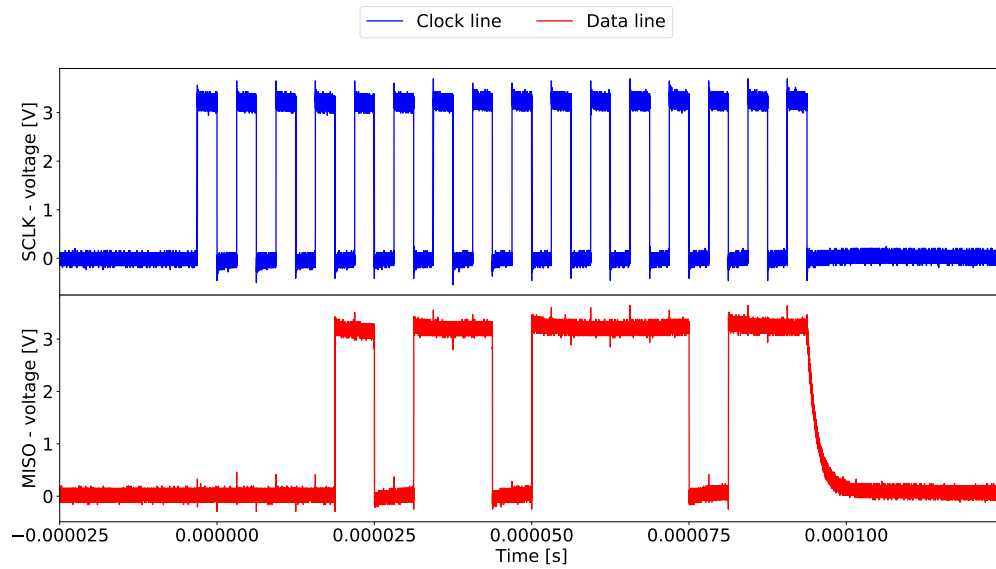


Figure 5.5: SPI readout of the temperature sensor via the Raspberry Pi, recorded with an oscilloscope. Clock and data line are low while idle. After the sensor's SS line has been pulled down (not shown), the Raspberry Pi generates a clock signal and the sensor clocks out the temperature data in two bytes. Only the first 14 bits are used, the first one holds the sign. Therefore, $00\,0010\,1101\,1110_{\text{bin}} = 734 \hat{=} 734 \cdot 0.03125^{\circ}\text{C} = 22.9375^{\circ}\text{C}$.

```

1 import pigpio
2
3 def opcode_02():
4     pi=pigpio.pi()
5     spi0=pi.spi_open(0,100000)
6     pi.spi_write(spi0,b'\x02')
7     (n,data)=pi.spi_read(spi0,2)
8     pi.spi_close(spi0)
9     pi.stop()
10    return(data) #returns 'none', if no data is read

```

Listing 5.3: *Python* code example of the SPI communication between FPGA and Raspberry Pi. The opcode '02' is sent to the FPGA on the MOSI line. During the following reading operation, two bytes are sent back on the MISO line. In this case, they contain the value stored in the right clock counter.

5.2.1.3 I²C bus

The I²C bus uses only two serial lines. One for the clock (SCL) and one for data (SDA). Both lines are high ($V_{DD} = 3.3\text{ V}$) while idle. The lines are connected to the logic voltage (V_{DD}) with pull-up resistors (R_D). A system can have multiple masters and slaves, while all slaves have a unique seven-bit address (Figure 5.6). A master initializes a communication by broadcasting the seven-bit slave address and one bit, indicating whether a read or write operation follows. A logical one indicates a read and a logical zero indicates a write operation. The addressed slave needs to acknowledge⁵. After that, data can be transmitted between master and slave depending on the operation mode. Data is transmitted in bytes followed by an acknowledge. The way devices are configured and read out depends on the devices' internal register structure and can be extracted from their data sheets. The function below in Listing 5.4 illustrates

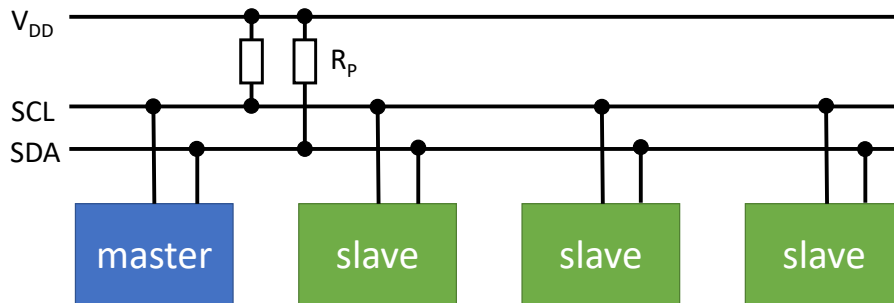


Figure 5.6: Schematic drawing of the I²C bus concept. The master and the slaves are connected with a serial clock and data line. Both lines are connected with pull up resistors to the logic voltage. All outputs are open collectors, meaning they are either disconnected (line potential is V_{DD}) or connected to ground (line potential is on ground).

the communication between the Raspberry Pi and the ADC, using the *Pigpio* library. It measures the 1.25 V output voltage of the service hybrid's left side (channel 2 of the ADC). After the connection has been set up, three bytes are written to the ADC (with the first one being the address 21_{hex}). First, the register we want to write to is sent. This byte is stored in the address pointer register. The next two bytes are the information we want to write, which in this case enables a measurement on channel 2 (Figure 5.7). Each read operation will read from the last register that has been written to the address pointer register. A measurement is performed in the *command mode* with the *i2c_zip* method. It allows a write operation directly followed by a read operation, without a stop condition in between. A byte that indicates the operation mode and the conversion result register is written to the ADC, which immediately performs a conversion on the programmed channel. The two byte result is directly read out and can be converted to a decimal value in the presented way (Figure 5.8). With a 12-bit resolution and a 2.048 V voltage reference, the least significant bit corresponds to 0.5 mV. For the channels which need a voltage divider, the conversion is adjusted accordingly off-line.

⁵The SDA line is pulled low by the receiver of a data stream during a ninth clock cycle. It is indicated with an A in the description of Figures 5.7 and 5.8.

```

1 import pigpio
2 def mea_P1V25_L():
3     pi= pigpio.pi()
4     adc=pi.i2c_open(1,0x21)
5     pi.i2c_write_device(adc,(0x02,0x00,0x28))
6     data=pi.i2c_read_device(adc,(0x07,0x01,0x70,0x06,0x02,0x00))
7     pi.i2c_close(adc)
8     pi.stop()
9     return((((data[1][0] & 15)<<8) | data[1][1])*2.048/4095)

```

Listing 5.4: *Python* code example of the I²C communication between Raspberry Pi and ADC. The ADC's second channel is read out.

The current and power monitor is also configured and read out via I²C. It needs some more configuration (listing 5.5). The first write operation to the device (address 40_{hex}) edits the configuration register (register 00_{hex}). If the the two bytes 41_{hex} and 27_{hex} are stored in the register, the device does not average and performs a bus and shunt voltage conversion continuously every 1.1 ms. The second write configures the calibration register (register 05_{hex}). The selected value of 1024 (04_{hex} 00_{hex}) provides a resolution of 50 μ A/bit in combination with the 0.1 Ω shunt resistor. After a short pause and setting the address pointer register to the current register (register 04_{hex}), where the result is stored, two bytes of current data are read out. The bytes are converted to a decimal current with the help of the second function below.

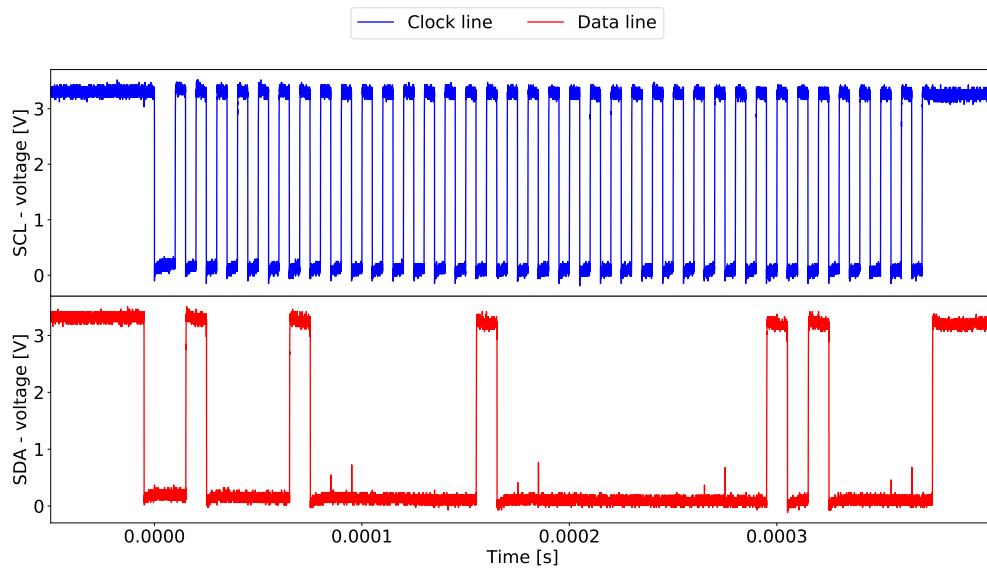


Figure 5.7: I²C operation of the Raspberry Pi addressing the ADC, which selects the desired channel (in this case channel 2). Clock and data line are high (3.3 V) while idle. First, the seven-bit address of the ADC is sent, followed by the write bit and an acknowledge of the ADC (0100 001W A). This is followed by the configuration register's address (0000 0010 A) and the two bytes of configuration data (0000 [0000] A and [0010] 1000 A). The eight framed bits in the middle represent each channel. The sampling occurs on a rising clock edge.

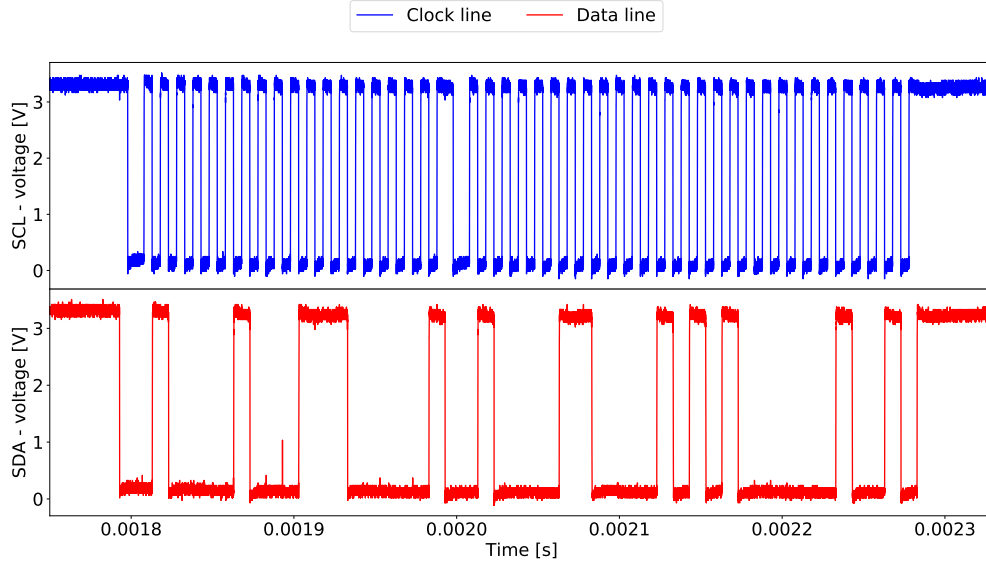


Figure 5.8: I²C operation of the Raspberry Pi addressing the ADC, which reads out the voltage of the previously selected channel. Clock and data line are high (3.3 V) while idle. First, the seven-bit address of the ADC is sent, followed by the write bit and an acknowledge of the ADC (0100 001W A). This is followed by the *command mode* command, which also selects the conversion result register for the following read operation (1111 0000 A). Without releasing the data line to a high state and thus enforcing a stop condition, a read of the ADC follows (0100 001R A). Two bytes of voltage data are sent by the ADC. The Raspberry Pi gives no acknowledge after the second byte, stopping the transaction (0001 0101 A 0000 0100 ~~A~~). The first four bits give the channel number ($0001_{\text{bin}} = 1 \hat{=} \text{channel 2}$), the last twelve bits give the voltage $0101\,0000\,0100_{\text{bin}} = 1284 \hat{=} 1284 \cdot 2.048\text{ V}/4095 = 0.6421\text{ V}$. The voltage has been measured while no service hybrid was connected and the ADC was left floating.

```

1  def mea_CURRENT():
2      pi=pigpio.pi()
3      ina=pi.i2c_open(1,0x40)
4      pi.i2c_write_device(ina,(0x00,0x41,0x27))
5      pi.i2c_write_device(ina,(0x05,0x04,0x00))
6      time.sleep(0.01)
7      pi.i2c_write_byte(ina,0x04)
8      count,data=pi.i2c_read_device(ina,2)
9      pi.i2c_close(ina)
10     pi.stop()
11     return(bitwisecurrent(data))
12
13  def bitwisecurrent(list):
14      if list[0]<128:
15          return((((list[0] & 127)<<8)|list[1]))*50.0e-6)
16      else:
17          return((((-1<<16)|((list[0]<<8)|(list[1])))*50.0e-6)

```

Listing 5.5: *Python* code example of the I²C communication between Raspberry Pi and the current and power monitor. The current is calculated from a voltage drop over a shunt resistor. Additional details are given in the text.

5.2.1.4 Bitwise operators in *Python*

In the digital communication introduced above, a frequent problem is the conversion of binary data to a decimal result. The presence of negative numbers and the fact that in most cases two separate bytes are read for a 12-, 13-, or 16-bit value, increase the difficulty. The conversion of a binary integer with any number of bits to a decimal is rather easy:

- $0 \rightarrow 0$
- $1 \rightarrow 1$
- $10 \rightarrow 2$
- $11 \rightarrow 3$
- $101001 \rightarrow 1 \cdot 2^5 + 0 \cdot 2^4 + 1 \cdot 2^3 + 0 \cdot 2^2 + 0 \cdot 2^1 + 1 \cdot 2^0 = 41$

To represent a negative binary integer x , *Python* uses the bit pattern for $(x - 1)$ with all of the bits complemented (switched from 1 to 0 or from 0 to 1) and an ‘infinite number’ of leading ones⁶.

So -1 is complement($1-1$) = complement(“..0”) = “...11111111”, and -10 is complement($10-1$) = complement(9) = complement(“...00001001”) = “...11110110”. To convert the two-bytes read operations from the respective devices into a single binary number, *Python*’s bitwise operators are used. They provide a fast calculation time and a clean syntax. The data can be processed directly in the binary format.

$x \ll y$

The result is x with its bits shifted to the left by y places. All bits entered on the right are 0. It is equivalent to the operation $x \cdot 2^y$.

Example: $5 \ll 2 = 101_{\text{bin}} \ll 2 = 10100_{\text{bin}} = 20 = 5 \cdot 2^2$.

$x \gg y$

The result is x with its bits shifted to the right by y places. All bits moved across the least significant bit are discarded. It is equivalent to the operation $x/2^y$ if the remainder of the division is discarded.

Example: $5 \gg 2 = 101_{\text{bin}} \gg 2 = 1_{\text{bin}} = 1$.

$x \& y$

Performs a bitwise ‘and’. Each output bit is 1, if the corresponding bits of x and y are 1, and 0 otherwise.

Example: $45 \& 57 = 101101_{\text{bin}} \& 111001_{\text{bin}} = 101001_{\text{bin}} = 41$.

$x \mid y$

Performs a bitwise ‘or’. Each output bit is 1, if one of the corresponding bits of x or y are 1, and 0 otherwise.

Example: $45 \mid 57 = 101101_{\text{bin}} \mid 111001_{\text{bin}} = 111101_{\text{bin}} = 61$.

$\sim x$

The result is the complement of x . Each 1 is exchanged with a 0 and each 0 with a 1. It is equivalent to the operation $-x - 1$.

Example: $\sim 21 = \sim \dots 00010101_{\text{bin}} = \dots 11101010_{\text{bin}} = -22$.

⁶In the same sense, a positive number has an infinite number of leading zeros. Applications with a limited number of bits reserve the most significant bit to indicate the sign.

$x \wedge y$

Performs a bitwise ‘exclusive or’. Each output bit is 1, if only one of the corresponding bits of x and y is 1, and 0 otherwise.

Example: $45 \wedge 57 = 101101_{\text{bin}} \wedge 111001_{\text{bin}} = 010100_{\text{bin}} = 20$.

The conversion of the temperature data (Listing 5.2) can be described using these operators:

```

1 def converter(array):
2     if array[0] < 128:
3         return ((array[0] << 6) | (array[1] >> 2)) * 0.03125
4     else:
5         return ((-1 << 14) | ((array[0] << 6) | (array[1] >> 2)) * 0.03125

```

Listing 5.6: *Python* code example of the conversion of the temperature sensor’s output data to a temperature value.

The data are contained in an array with two 8-bit integers. The first byte contains the temperature sign as first bit, followed by the first seven bits of an 13-bit integer. The second byte contains the additional six bits and its two least significant bits do not contain information. So, if the temperature is positive, the first bit of the first byte is zero and the byte is therefore smaller than 128. The remaining seven bits are shifted to the left by 6 positions, and these spots are filled by the first six bits of the second byte, which have been acquired by shifting the byte two spots to the right and discarding the two useless bits. The spots are filled by performing a bitwise ‘or’. Since the last six bits of the first integer are now all zeros they are replaced with the second integer’s bits. The resulting number is multiplied by the decimal value of the least significant bit, which is given in the data sheet. The procedure is quite similar for negative values (here the first byte is greater or equal to 128), only the series of leading ones needs to be added⁷, so *Python* interprets the result as a negative number.

5.2.2 Network

A single test board is supposed to be included in a network together with several additional test boards, the corresponding back-end board, and a main server, which coordinates the test procedures. To explore the possibilities of operating a greater number of test boards in close proximity, two racks have been equipped with 18 individual Raspberry Pis. They are all connected to the same local wifi network and received an individual permanent IP address within this network. Therefore, they can be operated ‘headless’ upon powering up. In this case, ‘headless’ operation means operation without the use of a keyboard, mouse, or monitor, as will be the case in the final application. In the network, the Raspberry Pis are considered ‘clients’. A 19th Raspberry Pi operates as ‘server’ and is operated in normal desktop mode. The same hardware is chosen for server and clients, because all software can be tested easily in this way, before transferring it to the clients. For more complex applications, e.g. additional *LabVIEW* controls of cooling devices, power supplies, and electrical loads or communication with the back-end board, a full-size PC will be needed.

5.2.2.1 Configuration and operation via SSH and SFTP

SSH stands for ‘Secure Shell’ and is a network protocol that allows the remote access to a computer’s command line. It is, together with the SSH File Transfer Protocol (SFTP), an advantageous communication method between the server and the client. SSH is supported natively

⁷ $(-1 << 14) |$

by the Raspberry Pi and only a few basic commands are needed to establish a connection or transfer a file. *Python* libraries (e.g. *Paramiko*) are available that allow the implementation of SSH in a *Python* program [53]. Only the IP address, user name, and password are needed for the connection. Since all clients have been configured with consecutive IP addresses, one can loop over the devices. This is useful to configure several clients. The libraries only need to be installed on the server. A single script can be prepared and can be used to configure all Raspberry Pis in the same way or to operate a test sequence. A test sequence could look like this:

- A file containing the *Python* code, that is supposed to run on the test board, is placed on the server. This file is transferred via SFTP to each individual client.
- The code is executed on each client via SSH. To avoid that the program stops after the SSH connection is closed, the *no hang-up* mode (by using the ‘nohup’ command) is used.
- While the test procedure is running, no direct communication between server and client is necessary. Data logs are created locally.
- After a certain time the server checks, whether all clients have finished, by checking the log files. If a client is ready, its results are downloaded to the server.

A minimal working example is shown in Listing 5.7 below. The *Python* library is imported and a connection is set up. The *host key policy* needs to be changed to suppress a dialogue. Afterwards, a connection can be established and a shell command is executed. In this case, simply the IP address of the client is requested via the command ‘hostname -I’. Any other single shell command or a series of them including key-words can be executed. After the server displayed the command line output, the connection is closed.

```
1 import paramiko
2 ssh=paramiko.SSHClient()
3 ssh.set_missing_host_key_policy(paramiko.AutoAddPolicy())
4 ssh.connect(192.168.0.13,username='pi',password='*****')
5 input,output,err=ssh.exec_command('hostname -I')
6 lines=(output.readlines())
7 for k in lines:
8     print(str(k))
9 ssh.close()
```

Listing 5.7: Minimal working example of SSH connection between two Raspberry Pis using *Python*’s *Paramiko* library. The script retrieves the IP address from the client’s command line.

This communication approach bears some disadvantages. It is slow, especially when the server needs to open a connection, logs on, performs a required action, and closes the connection for each client separately each time it performs an action. There is no feedback from the client. The server has to check the client’s status itself and problems are detected with a delay. Considering the need to synchronize tests between the test boards and the back-end boards, it provides a serious challenge. However, for debugging and the transfer of prepared code for the test setups, SSH and SFTP are suited, as they grant full control over the local client.

5.2.2.2 Asynchronous HTTP based operation

Instead of using long test scripts that run on the clients, one can also use a different approach. Each client can be set up to host its own web-server. This requires some additional software

(e.g. the *Python* libraries *Sanic* and *Aiohttp* [54, 55]). Their setup is possible and manageable by SSH. In this case, a HTTP⁸ request would not display a website, but instead a short program is started on the client. In general, this will be a subroutine of the full measurement sequence. Its result is passed on to the main server. No lasting connection needs to be kept open between the server and the test board. This approach is also promising, since it can utilize asynchronous *Python* features (asynchronous SSH *Python* libraries are also available).

The difference between a synchronous and an asynchronous approach is visualized in Figure 5.9. With synchronous requests, the server sends out the first request to the corresponding test board, waits for the response, receives and processes it, before starting a new request. In an asynchronous approach, the software is able to send out a number of requests, while waiting for responses. The order of the responses does not matter. The time it takes to handle a number of requests reduces dramatically.

An example of the application of the asynchronous and HTTP based approach is presented in Listings 5.8 and 5.9. The script in Listing 5.8 is executed on each client and sets up the web server. The web server can only handle the key-word request ‘/temperature’ at its address. It returns a measurement of the temperature sensor on the test board. The script is separated into the main function, which launches the web server, and into the definition of the key-word. Listing 5.9 is the script which is run on the server and sends asynchronous requests to the clients. The clients perform the temperature measurement and return the result. The two functions perform the HTTP request, while the code between lines 16 and 21 sets up the event loop.

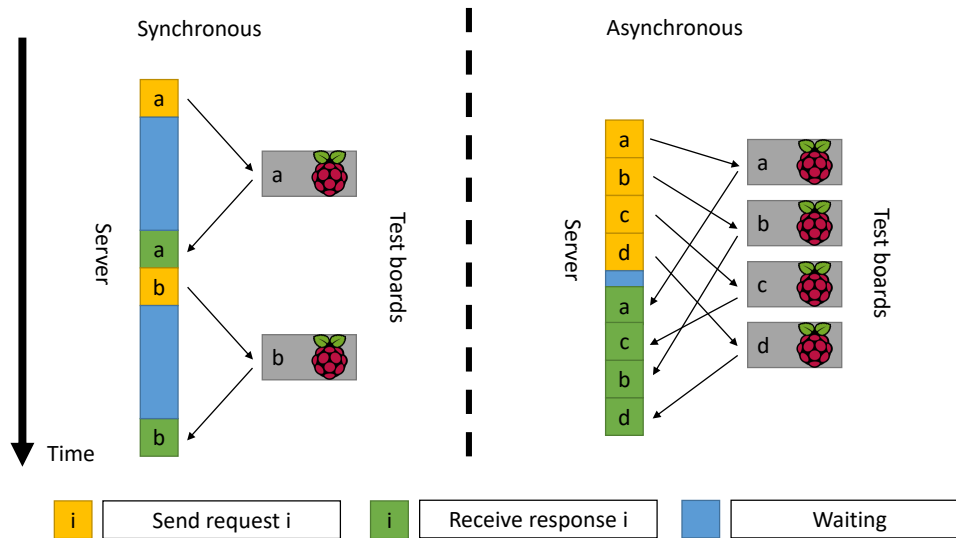


Figure 5.9: Graphical representation of the difference between synchronous and asynchronous request handling. In an asynchronous approach the waiting time can be used for additional operations.

⁸Hypertext Transfer Protocol

```
1 from sanic import Sanic
2 from sanic.response import text
3 import asyncio
4
5 app = Sanic(__name__)
6 @app.route('/temperature')
7 async def index(request):
8     return await text(meas())
9
10 if __name__ == '__main__':
11     app.run(debug=True, host='0.0.0.0')
```

Listing 5.8: Minimal working example of a *Sanic* based web server. The defined web address returns the result of the test board temperature measurement presented in Listing 5.2.

```
1 import aiohttp
2 import asyncio
3 import asyncio_timeout
4
5 async def fetch(session, url):
6     with asyncio_timeout.timeout(10):
7         async with session.get(url) as response:
8             return await response.text()
9
10 async def main(j):
11     ip='http://192.168.0.'+str(j+12)
12     async with aiohttp.ClientSession() as session:
13         temp = await fetch(session, ip+':8000/temperature')
14         print(temp)
15
16 loop=asyncio.get_event_loop()
17 tasks=[]
18 for j in range(18):
19     task = asyncio.ensure_future(main(j))
20     tasks.append(task)
21 loop.run_until_complete(asyncio.wait(tasks))
```

Listing 5.9: Minimal working example of an asynchronous *Python* script, that performs a HTTP request for a temperature measurement, as defined in Listing 5.8 on all Raspberry Pis.

5.3 Commissioning of test board prototypes

Three test board prototypes have been produced. To test their full functionality, additional components are required:

- a generation 3 service hybrid prototype with the Panasonic AXF5A5012 connector,
- a Raspberry Pi Zero W,
- a USB hub connected via micro-USB cable to a mouse and a keyboard for the Raspberry Pi,
- a monitor connected via HDMI cable to the Raspberry Pi,
- a low voltage power supply for the powering of the test board (5 V) and service hybrid (10 to 11 V) and the corresponding cables
- a high voltage power supply and appropriate cables,
- an adapter for the service hybrid LV and HV input power plugs and pigtails for the HV return,
- a crate with the back-end board
- three VTRxs (one for the service hybrid and two for the test board) and their optical fibres, which connect them to the back-end board,
- an I²C to USB adapter dongle, which enables the configuration of the GBTxs via a PC.

Figure 5.10 shows a picture of a fully assembled test board and a connected service hybrid. All cables necessary for the commissioning are attached. Their number illustrates the complexity of the service hybrid testing procedure. In the following selected measurements that prove the general functionality of most components and validate the design will be presented. All measurements are carried out directly on the local Raspberry Pi and the coordination with the back-end board is handled manually.

5.3.1 ADC

The main aspects during commissioning of the test board's ADC are the successful communication between ADC and Raspberry Pi, confirming the linearity of the ADC, and the precision of the voltage reference.

The successful communication has been shown in Section 5.2.1.3. It is possible to supply an external voltage to the inputs of the ADC via additional pin headers, in order to perform a calibration. Five different voltages are applied with a power supply (Agilent E3633A DC Power Supply [25]) and the resulting ADC count is recorded. Ten measurements per voltage point are performed and a linear fit of the averages is carried out. The uncertainties of the averages are below one ADC count. The uncertainty of the power supply voltage is always assumed to be 5 mV, which is compatible with the data sheet. The results for four channels (they are named according to the test board's schematics) are shown in Figure 5.11. Channels 1, 2, and 4 are measured directly by the ADC, while the measurement of channel 3 also includes a voltage divider (nominal reduction by a factor of 2). All measurements yield a good linear behaviour of the

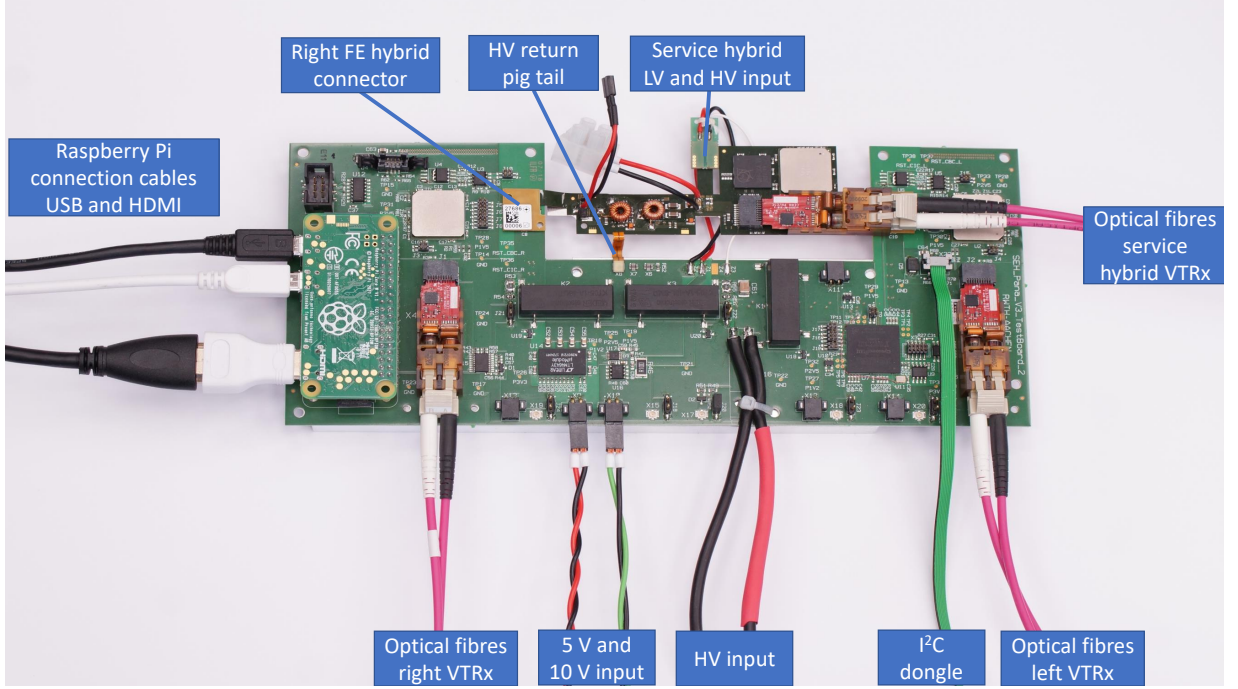


Figure 5.10: Picture of a fully assembled test board. A service hybrid, the three VTRxs, the Raspberry Pi and all cables are connected.

ADC and an offset compatible within its uncertainties with zero. The inverse of the slope yields the output voltage of the voltage reference. Its nominal value is 2.048 V. The observed value is 0.5 % higher, which corresponds to a 1σ deviation in all channels. Considering the deviation of the voltage reference, the voltage divider at channel 3 is compatible with a factor of 2. Since all results are compatible with the expected nominal values within their uncertainties, a dedicated calibration series for all test board ADCs is not necessary. All other channels are also functional and give reasonable results, as can be seen in Table 5.2. The table lists the measured ADC counts and the voltages of a service hybrid connected to a test board for each channel. The name of each channel corresponds to the schematics. The voltages are obtained considering the voltage reference and the resolution of the ADC:

$$\text{voltage} = \text{ADC count} \cdot \frac{\text{reference voltage}}{\text{resolution}} = \text{ADC count} \cdot \frac{2.048 \text{ V}}{(2^{12} - 1)}.$$

The value obtained by channel 1 is a measure for the potential difference between the high voltage and low voltage ground. In this example, the same power supply provides the low voltage and a 10 V bias voltage, which is supplied to the HV circuit. Therefore, VHVRet is expected to be zero. Channels 2 and 4 measure the output voltage of the second stage DC-DC converter for each FE hybrid side. The voltages differ slightly from the nominal 1.5 V and from each other, because of the diodes (see below) and the different length of the voltage paths inside the hybrid and the test board. While the 1.5 V (or lower because of the diodes) output voltage is provided to the FE hybrids by the FE hybrid connector, and therefore to the test board, there is currently no possibility to measure the 2.5 V output voltage directly. Channel 3 is therefore floating. Channels 5 and 8 measure the RSSI voltage for the left and right test board VTRx. Here, no VTRx is connected, so only a voltage defined by a reference voltage and a voltage divider is measured

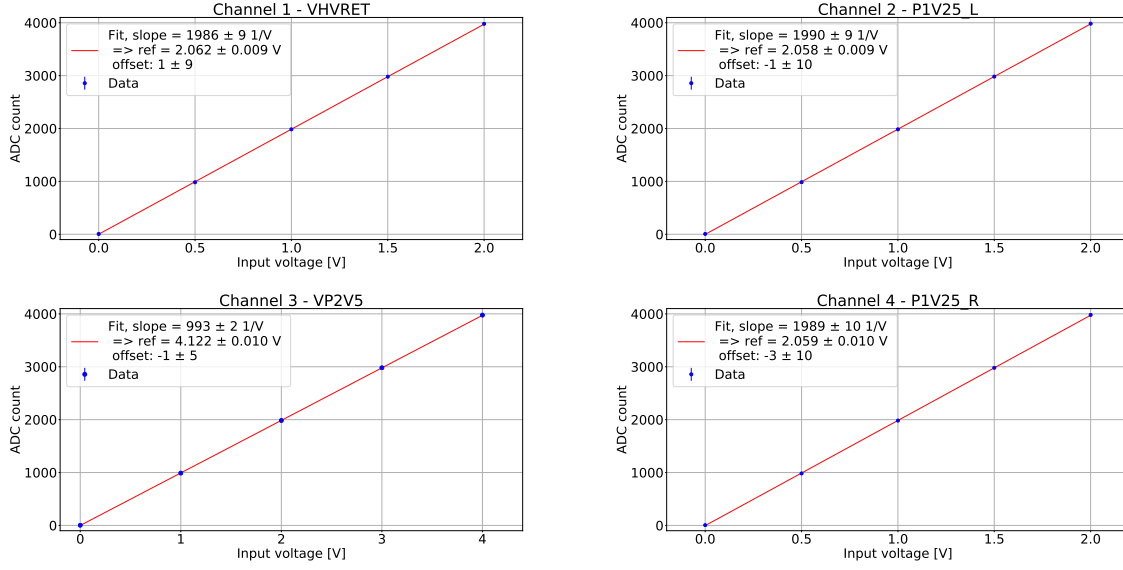


Figure 5.11: Calibration plots of channels of the test board's ADC. The data points are given in blue, a linear fit in red.

Test board ADC channel, channel name	ADC count	Voltage [mV]	Expected voltage [mV]
Channel 1, VHVRet	1	0.5	0.0
Channel 2, P1V25.L	2924	1462.0	1500.0
Channel 3, VP2V5	138	69.0	floating
Channel 4, P1V25.R	2939	1469.5	1500.0
Channel 5, RSSIL	1597	798.5	797.0
Channel 6, VHVJ7	0	0.0	floating
Channel 7, VHVJ8	18	9.0	10.0
Channel 8, RSSIR	1605	802.5	797.0

Table 5.2: ADC measurement of the ADC counts and voltages of a test board with an attached service hybrid. The expected voltages are also given.

(Figure C.7):

$$U = 2.5 \text{ V} \frac{2.2 \text{ k}\Omega}{2.2 \text{ k}\Omega + 4.7 \text{ k}\Omega} = 0.797 \text{ V} .$$

This value is observed for both sides. Channels 6 and 7 measure the HV for the upper and lower sensor (after the voltage divider with a factor 1000). In this example, only VHVJ8 has been connected to the 10 V bias voltage. Only channel 7 indicates the voltage, while the disconnected channel 6 measures no voltage.

The behaviour of the output voltage of the generation 3 service hybrid prototype behind the diode for some load currents is shown in Figure 5.12. The measurements have been performed via soldered connections to the service hybrid's second stage output capacitor and without using the test board. Both, the left and right side of the hybrid, show a similar behaviour. Due to the voltage drop across the diode, the voltage is already reduced to about 1.38 V even at the low measurement current. For non-zero currents, the voltage drops quickly to below 1.2 V and further decreases exponentially. Tests with a 2-CBC FE hybrid prototype proved the reliability of the solution [12]. It needs to be verified, if a higher number of CBCs is operational with the

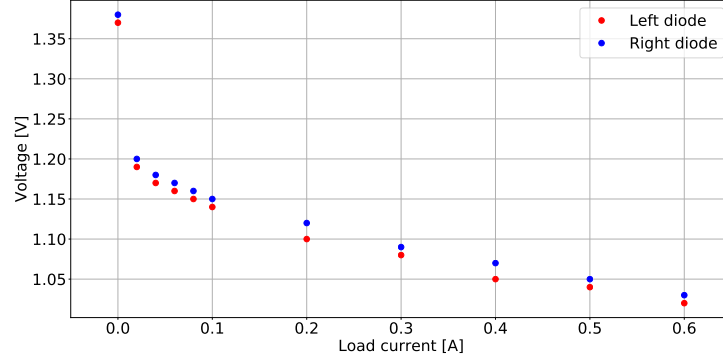


Figure 5.12: Output voltage of the two diodes at the service hybrid’s connectors to the FE hybrids versus the load current.

resulting voltage below 1.2 V. The selection of a different diode with a smaller voltage drop is difficult due to the small size of the band gap, which is required to provide 1.5 and 1.25 V.

5.3.2 HV circuit

The test of the HV circuit covers the functionality of the relays, general circuit integrity, leakage current measurements, and measurement of the voltage at the ADC after the voltage divider. The relays are switchable by the Raspberry Pi via the GPIO pins. A voltage can be applied to the test board with an external HV power supply (Keithley 2410 Source Meter [56]). Two dedicated connection cables distribute the voltage to the service hybrid and route it back to the test board, where the ADC measures it after two voltage dividers (factor 1000). To allow a correct measurement, the LV ground and the HV ground must be on the same potential. The leakage current is currently measured within the external power supply. It is a simple yet convincing measure for the circuit integrity. Two different sets of measurements are carried out. Firstly, the current versus voltage is measured, secondly, the current at a fixed voltage is measured versus time. Both measurements are shown in Figure 5.13. In a first measurement in the left plot, the bare test board without a connected service hybrid is tested. Afterwards, the hybrid and all cables are connected and the test is repeated. Both measurements were carried out in the standard lab atmosphere and in a dry atmosphere. The voltage is ramped up from 0 to 1000 V. After each 20 V step, a pause of one minute is made. Five measurements are performed and the average and its uncertainty are calculated. A measurement is only possible if the relays on the output side are closed, since each voltage divider has an internal leakage of up to $1 \text{ kV}/1 \text{ M}\Omega = 1 \text{ mA}$. This leakage dominates, as typical currents are of the order of $0.1 \text{ }\mu\text{A}$. As one would expect, the leakage current rises with the input voltage. It is also higher when the service hybrid is connected, and the dry atmosphere reduces the leakage current. However, the current rises exponentially and not linearly with the voltage, especially when the service hybrid is connected. To understand this behaviour, in a second measurement the voltage was fixed at 600 V and the leakage current has been measured every minute over 24 hours. The result is shown in the right plot. The current decreases exponentially over time. Therefore, the current versus voltage measurement is also dependent on the time between each step in the ramping process. This measurement also shows a problem with this kind of leakage current measurements. After about 20.5 hours of recording time and after the leakage current had levelled out, a drop of about 20 % occurred. The drop

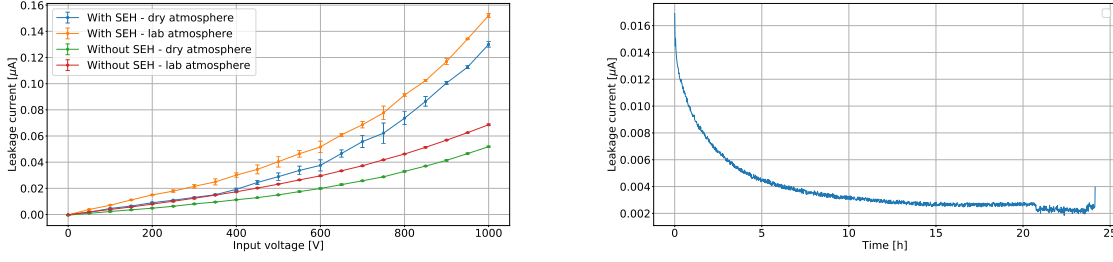


Figure 5.13: Leakage current measurements of the test board’s HV circuit. The left plot shows a measurement of current versus input voltage. It has been measured in a dry atmosphere and the standard lab atmosphere and with and without a service hybrid attached. The right plot shows a measurement of current versus time with a service hybrid and with 600 V applied.

coincided with an increase in people’s activity in the lab space. Further studies showed that the high voltage supply cables, which are placed together with the whole setup on an ESD protection mat, contribute significantly to the leakage current. The placement of the cables, even though isolated, has a non-trivial impact on the results. A quantified comparison across different sets of measurements is therefore impossible with the current setup. To overcome this issue, an onboard measurement of the leakage current is foreseen for the next test board generation.

5.3.3 Current and power monitor

The INA226 current and power monitor measures the LV input of the service hybrid. It is necessary for efficiency calculation and monitoring. The communication via I²C is explained above and works successfully on the test board. Bus voltage and shunt voltage can be measured. Although it is not inevitably necessary, the resistor value can be programmed and the current and power can be directly read from the device. Otherwise, an off-line calculation can be used. The upstream switch, which is operated via GPIO pins, is functional as well.

Two measurements are performed to characterise the monitor. First, the bus voltage output is compared to given input voltages. The input voltages are supplied by an external power supply (Rohde & Schwarz HMP4040 [57]), ten measurements are collected, and the average and its uncertainties are calculated. The uncertainties are below 1 %. No load is connected. The results are shown in Figure 5.14. Both representations show nearly perfect agreement between the input voltage and the measured value. However, below 3 V the measurement starts to diverge and fails completely for even lower voltages. An explanation could be the influence of the upstream switch, which needs to be passed by the measurement current. For small voltages, the internal resistance of the switch cannot be neglected. In a second measurement, a load is connected and the fixed input voltage and the current is measured for a number of set currents I_{set} . Both quantities are measured by the power supply, the load, and the test board. The uncertainty on the monitor’s current measurement is determined by repeated measurements to be 2 mA. Figure 5.15 shows the results. The measured voltages are close together and their descending sequence is compatible with losses along the cable path. The ratios of measured current to set current are compatible within the monitor’s uncertainty. The deviation from unity decreases with rising current, since the influence of the additional resistance in the current path becomes smaller.

Table 5.3 shows the results of a set of measurements with the current and power monitor. A

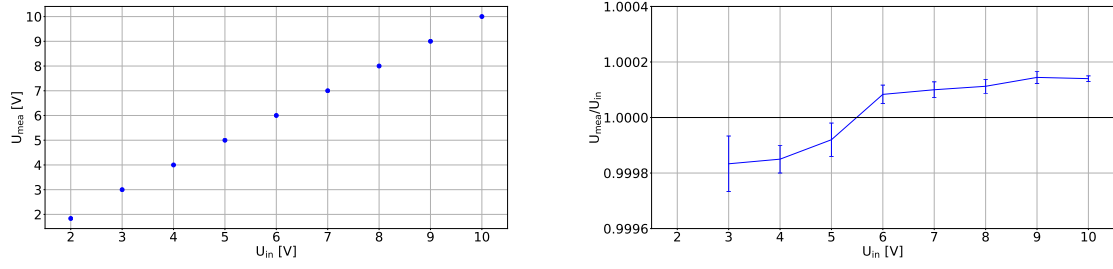


Figure 5.14: Bus voltage measurement with the current and power monitor on the test board. The left plot shows the measured over the set input voltage and the right plot their ratio over the set input voltage. The data point at 2 V has been excluded.

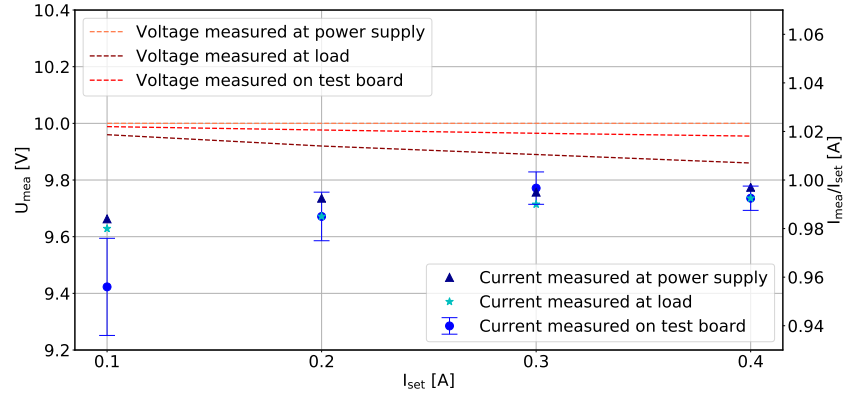


Figure 5.15: Bus voltage and current measurement of the service hybrid's input on the test board. Both values are measured at the power supply, at the connected load (no service hybrid is attached), and with the current and power monitor on the test board. Red lines represent voltage measurements (left y -axis), blue symbols current measurements (right y -axis).

service hybrid is connected to the test board and the shunt voltage, the bus voltage, and the current are measured with the current and power monitor. The output voltages of both service hybrid sides' are measured with the ADC. The input and output power can be calculated by multiplying the corresponding current and voltage. Three different cases are studied. In the first case, no load is connected, in the second case an electrical load set to 0.5 A is connected to the right output voltage, and in a third case the load is connected to the left output voltage. The shunt voltage is directly measured by the device, while the current is calculated using the programmed shunt resistance (0.1Ω). The expected factor of 0.1 V/A is observed. Without a load, the current consumption of the GBTx and GBT-SCA, as well as losses in the DC-DC converters, contribute to the input current. The bus voltage corresponds to the supply voltage and is close to the chosen value of 10 V. The deviation can be explained with losses on the supply cables. The output voltages on the unloaded sides match the observations in Table 5.2. In the loaded cases, the output voltage is reduced due to the voltage drop across the diode. The increase in output power of about 0.6 W increased the input power and current by about 1.0 W and 0.1 A. This would correspond to a poor DC-DC converter efficiency of about 60 %. However, this is not accurate due to the voltage drop across the diode and the resulting losses. Another difficulty

	No load connected	0.5 A load connected to right side	0.5 A load connected to left side
Input current [A] measured by current monitor	0.1304	0.2250	0.2245
Shunt voltage [V] measured by current monitor	0.01303	0.02244	0.02246
Bus voltage [V] measured by current monitor	9.9838	9.9713	9.9738
Right side output voltage [V] measured by the ADC	1.459	1.172	1.462
Left side output voltage [V] measured by the ADC	1.463	1.454	1.160
Input power [W] calculated	1.30	2.24	2.24
Output power [W] calculated	0.00	0.59	0.58

Table 5.3: Summary of measurements of the electrical input and output power for a service hybrid connected to a test board.

concerning efficiency measurements with external loads is the abundance of the active ASICs on the service hybrid. These lead to additional losses, which cannot be predicted precisely at the current state. When the final ASICs and their configuration become available, a typical power consumption can be determined.

5.3.4 FPGA

The FPGA has been programmed to record the clock and reset signals that are sent to the FE hybrids by the service hybrid's LpGBT (in the case of the generation 3 prototypes the GBTx and GBT-SCA). To test the communication between Raspberry Pi and FPGA without a functional service hybrid, a test mode is available, too. Instead of the service hybrid, an on-board oscillator is used to provide signals. It is possible to change between the test mode and normal operation and to read out the status register (opcode 26). All test mode functionalities are tested successfully. In a next step a service hybrid was attached. It is connected optically to a back-end board in order to receive clock and reset signals. The service hybrid simulates reset signals by enabling and disabling the corresponding GPIO outputs of the GBT-SCA as fast as possible. The length of the resulting pulses depends on the connection speed to the back-end and is orders of magnitude longer than in the final system. However, the FPGA works fine under those conditions as well as in the test mode, where 40 MHz pulses are registered. The FPGA counts the number of reset signals initiated by the back-end. These two numbers are compared off-line. The counting of clock cycles was tested for four different clock speeds. The results for the left and right side are summarized in Table 5.4. For frequencies up to 160 MHz the correct number of clock cycles is measured within the measurement interval of 100 μ s. In the 320 MHz case, the right side measurements yield a deficit of around 100 counts. To understand these measurements, the differential clocks' waveforms measured on the test board, are considered. The waveforms were courteously provided by Marius Preuten. They are shown in Figure 5.16. The red, green, blue and purple curves represent the 40, 80, 160 and 320 MHz clock, respectively. The waveforms

Clock frequency	Expected counts in 100 μ s	Measured counts left side	Measured counts right side
40 MHz	4000	4000	4000
80 MHz	8000	8000	8000
160 MHz	16000	16000	16000
320 MHz	32000	32000	31890
320 MHz	32000	32000	31881
320 MHz	32000	31999	31910
320 MHz	32000	32000	31907
320 MHz	32000	32000	31921
320 MHz	32000	32000	31925

Table 5.4: Summary of the number of clock cycles, which were counted by the FPGA. The service hybrid received the 40 MHz reference clock from the back-end board.

were recorded as eye diagrams⁹. Only the time frame around half of a 320 MHz clock cycle is shown. The waveforms are superimposed on the intersection point of the rising and falling edge in the eye diagrams.

Both sides of the test board show the same behaviour. Instead of steep edges, reflections and oscillations occur and cause a step in the edge. For the slower clocks, it covers a smaller fraction of the period than for a faster clock. The features are similar within a clock line, which hints towards an effect caused by the test board layout. The step on the right board side has less oscillation and is almost flat for the 320 MHz clock. Under these conditions, it is surprising that the clock counting with the FPGA works at all. Miscounts only occur in the case of the right 320 MHz clock with its flat feature. Additional studies showed sufficient clock and data quality of the signals coming from the service hybrid itself. Before more extensive studies can be carried out, the design of the test board lines needs to be improved.

The AMUX voltage, which is supposed to be read out by the GBT-SCA, can be set. However, the pin assignment of the FE hybrid connectors does not yet feature the necessary lines for it. They will be implemented in the next generation of hybrids.

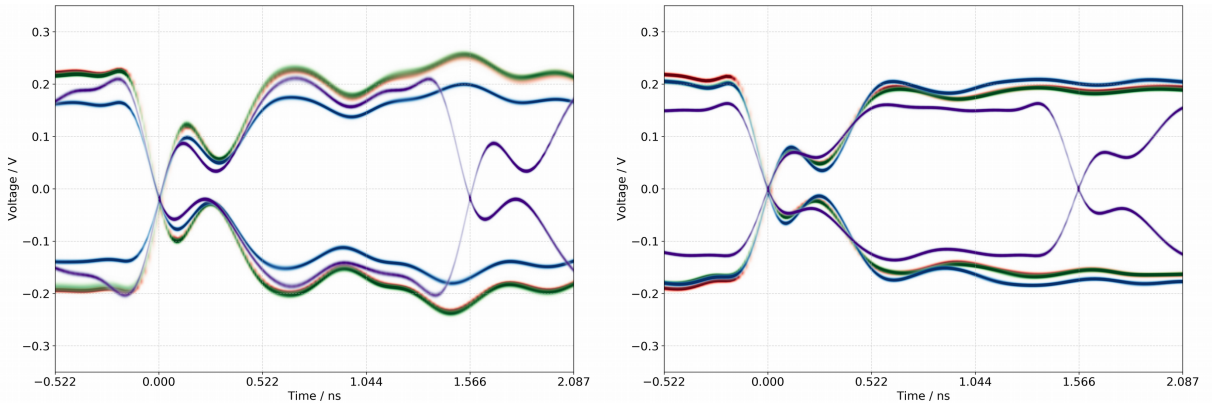


Figure 5.16: Eye diagrams of the service hybrid clock waveforms, which have been measured on the test board by Marius Preuten [12]. The red, green, blue and purple curves represent the 40, 80, 160 and 320 MHz clock, respectively. The left plot corresponds to the left service hybrid side and the right plot to the right side.

⁹Sample of a digital signal triggered on data rate.

5.3.5 I²C F-RAM

All of the modules' readout ASICs can be configured via I²C. The back-end board is responsible for the transactions, which are encoded inside its downlink data stream [4]. To test the I²C lines on both service hybrid sides the two F-RAMs are used. They have 32-thousand 8-bit registers. Since the GBT-SCA logic operates with 1.5 V and the F-RAM with 2.5 V, a level translator is used on the test board. Figure 5.17 shows a successful I²C transaction between the service hybrid GBT-SCA and the F-RAM (I²C address 50_{hex}) behind the level translator. All acknowledges are received and values stored in registers can be accessed and retrieved. The level translator causes no problems.

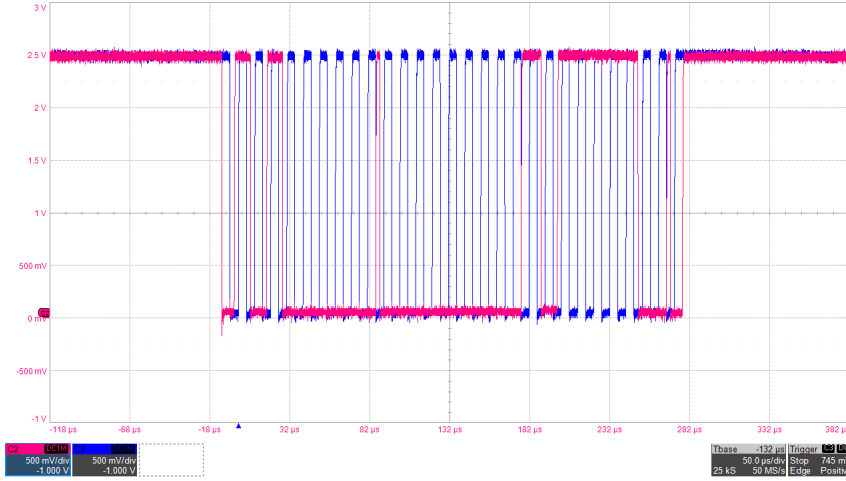


Figure 5.17: I²C operation between a service hybrid GBT-SCA and an F-RAM. It sets the address pointer to the number of the next register that is read out. Clock and data line are high (2.5 V) while idle. First, the seven-bit address of the F-RAM (50_{hex}) is sent, followed by the write bit and an acknowledge of the F-RAM (1010 000W A). One can see that the data line is released to a high state by the GBT-SCA and the F-RAM during part of the low clock state of the acknowledge. Since sampling occurs on the rising clock edges, this does not cause problems. The 16-bit address of the desired register (00_{hex} BE_{hex}) follows (0000 0000 A 1011 1110 A).

5.3.6 Data test

Currently, no back-end emulation is in place that can conduct the full data chain *back-end - test board GBTx - service hybrid GBTx - back-end*. However, Marius Preuten courteously provided commissioning measurements of the test boards' GBTxs, which will be presented here for the sake of completeness. All GBTxs were connected via the VTRxs to the back-end board and a simple bit error rate measurement was conducted. The fraction of transactions during which the GBTx was not able to identify the header pattern in the data stream (link downtime percentage) was also measured. The results for the three test board prototypes and their two sides and for a service hybrid with a GBTx are summarized in Table 5.5. The service hybrid showed no bit errors and no downtime. The test boards' GBTxs are able to establish a connection for most of the time. However, they yield significant bit error rates and downtimes. One GBTx communication fails completely. The maximal bit error rate is 50 %, because the data line is always low, which is correct for half the bits in a pseudo-random data pattern. For the same reason, the link downtime percentage is approximately two times the bit error rate. Both values

are essentially redundant. Due to the random nature of the data, the factor of two is not exactly observed. The left GBTx seems to be less prone to communication loss. It is likely that the poor quality of the clock signals is related to the poor signal link. If the data quality suffers from the same issue, communication performance will be limited. Further studies on the signal lines need to be carried out before the development of the test procedure can be continued.

	Bit error rate	Link downtime percentage
Service hybrid	0	0
Test board 1, left GBTx	$6.94 \cdot 10^{-5} \%$	$2.71 \cdot 10^{-6} \%$
Test board 1, right GBTx	$1.78 \cdot 10^{-1} \%$	$3.53 \cdot 10^{-1} \%$
Test board 2, left GBTx	$3.30 \cdot 10^{-6} \%$	$5.36 \cdot 10^{-6} \%$
Test board 2, right GBTx	50 %	100 %
Test board 3, left GBTx	3.38 %	6.63 %
Test board 3, right GBTx	$4.07 \cdot 10^{-2} \%$	$8.07 \cdot 10^{-2} \%$

Table 5.5: Results of the bit error rate measurements between the back-end board and the GBTxs on the service hybrid and the test boards [12].

5.4 Graphical user interface

All the presented *Python* code is used in a command line interface. Either the dedicated functions or small programs containing these functions are run directly on the test board's Raspberry Pi. To improve the ease of use and the integration of the Raspberry Pi in an arrangement of devices, a graphical user interface for a windows computer has been created. It was designed in *LabVIEW*. The programme makes excessive use of a custom-made VI that establishes an SSH connection from the windows shell to the Raspberry Pi and executes the prepared *Python* code in the Raspberry Pi's command line (Figure 5.18). The windows shell command used is 'plink', which is the shell implementation of *PuTTY*. *PuTTY* is a widely used SSH tool for windows systems [58]. The user can choose the requested command from a menu without knowledge of the underlying syntax (Figure 5.19). The text, which is usually displayed in the command line of the Raspberry Pi, or just the numerical value of e.g. a measurement, can be used for further *LabVIEW* operations.

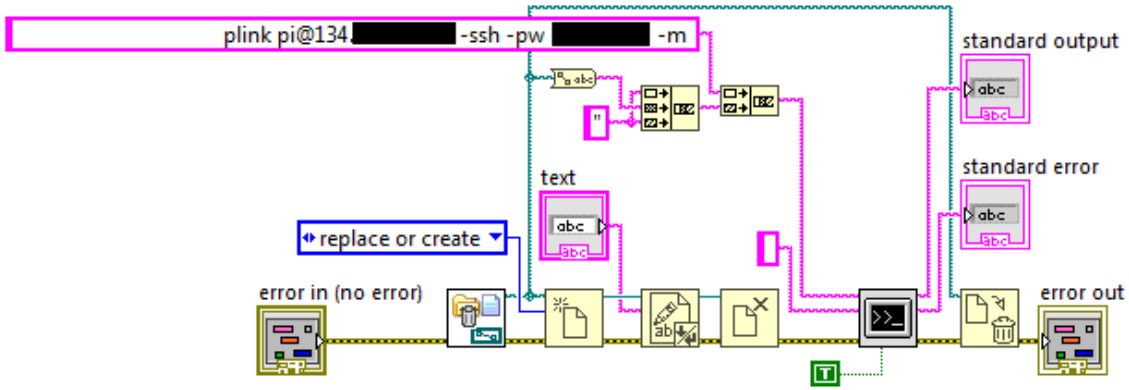


Figure 5.18: Block diagram of a *LabVIEW* VI that establishes an SSH connection via *PuTTY* to the Raspberry Pi on the test board. Any command line input can be given to the VI as a text argument and is executed on the Raspberry Pi. The command line output is returned.

5.5 Cooling system

According to the quality control measures outlined in the TDR, “all service hybrids will be subjected to a functional test, both at room temperature and operating temperature”. The functional test can be carried out with the test board, but to achieve operating temperature (of down to -30°C) an additional cooling system is necessary. A prototype of the system has been designed in the framework of this thesis with the help of the mechanical workshop. It has been build by Michael Wloch. The commissioning still needs to be done. It is not fully decided whether or not active thermal cycling is needed, too. Due to the high energy consumption of the full test board, the use of commercial components, and its size, an operation of the entire test board at -30°C is challenging. Instead, a design is proposed that uncouples the test board

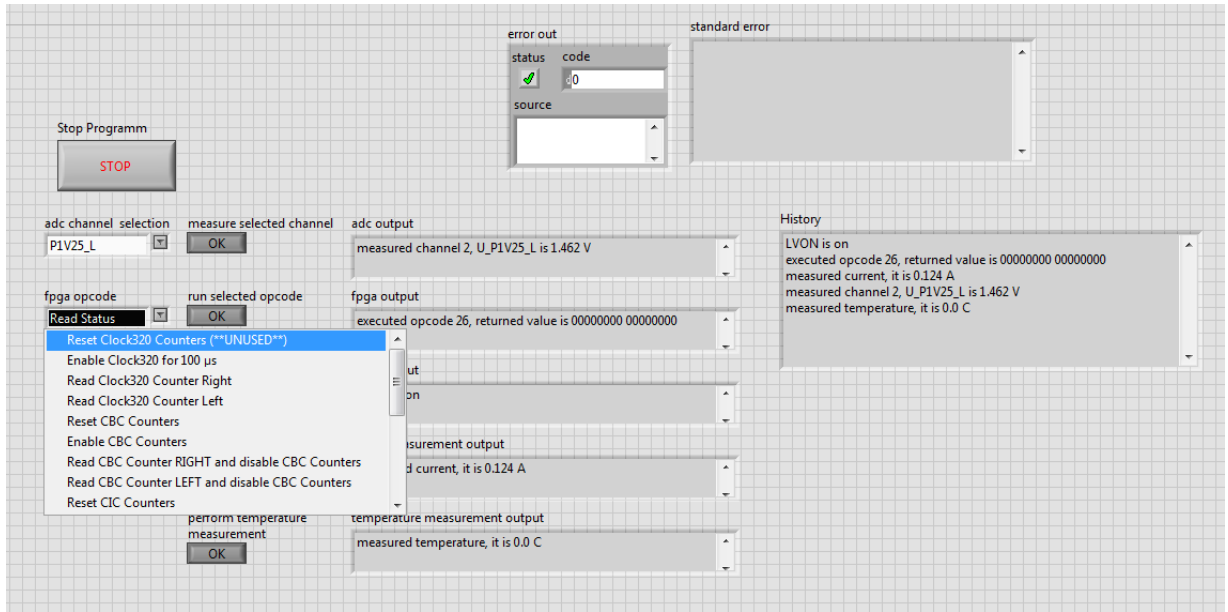


Figure 5.19: Front panel of a *LabVIEW* VI that can execute the *Python* commands to control and read out the ADC, the current and power monitor, the FPGA, the GPIO pins, and the temperature sensor. The text output is displayed. The desired functions can be chosen from a drop down menu.

and the service hybrid thermally. A technical drawing of the design is shown in Figure 5.20 and picture in Figure 5.21. The test board is placed on and screwed onto an aluminium plate, which is covered by a lid. The lid is made of 3D-printed polycarbonate and split into two pieces due to the limited size of the printer volume. Openings between the aluminium base plate and the lid allow the access of cables and optical fibres to the test board. In contrast to the previous application, the service hybrid is not directly connected to the test board via the FE hybrid connectors. Instead, a short adapter cable connects both devices. This allows a vertical separation and the service hybrid can be placed inside a polycarbonate box on top of the lid. The service hybrid is clamped down on an aluminium cooling block, which is crossed lengthwise by two copper pipes with an inner diameter of 7 mm. In addition to the inlets for the pipes, a dry air inlet and an outlet for the optical fibres are implemented. Four vertical openings between the test board and service hybrid's volume are needed. They are necessary for the already mentioned FE adapter cables, the LV and HV input cables and for the three HV and thermistor pigtails. To ensure ESD protection the box's inside will be lined with aluminium tape. All openings will be sealed with an insulating material. The lid serves mainly as a protection for the test board. The box is designed to have a small cold volume and thus is easier to cool. Its cover is pluggable to allow fast and easy access while maintaining a tight sealing. It is planned to use two separate temperature circuits. One pipe will be used for the low-temperature circuit and will be attached to a liquid chiller. The other circuit will be connected to an additional chiller at ambient temperature. This configuration allows fast changes in box temperature. Only one circuit will be running at a time.

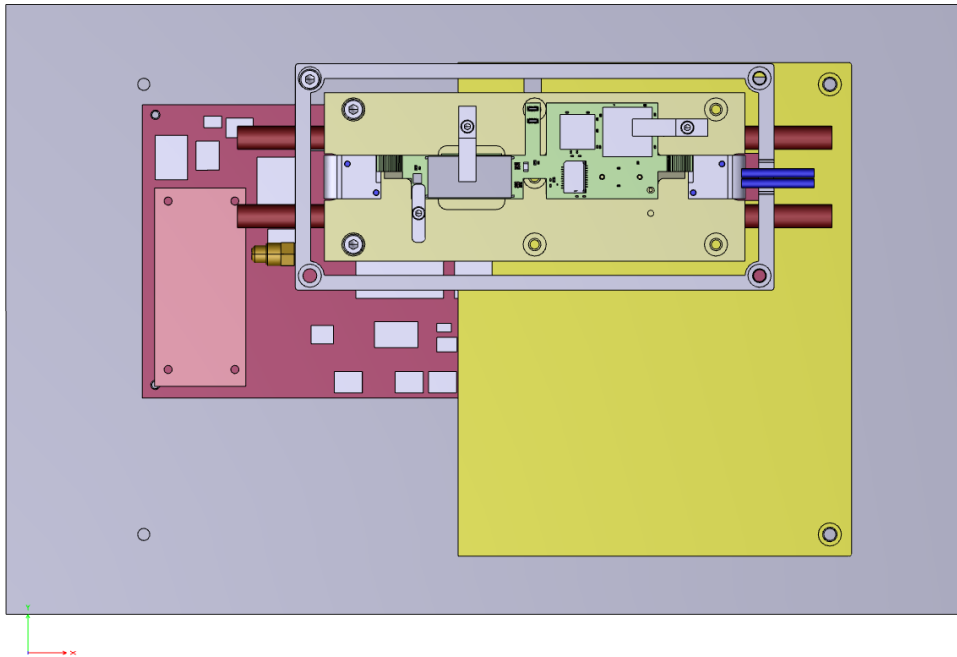


Figure 5.20: Sketch of the cooling system for the service hybrid testing. The test board (red) is placed on an aluminium base plate (dark grey). The service hybrid (light green) and its cooling block (light yellow) are placed above the test board. The left part of the test board lid (dark yellow) and the cover of the cold box (light grey) are removed.

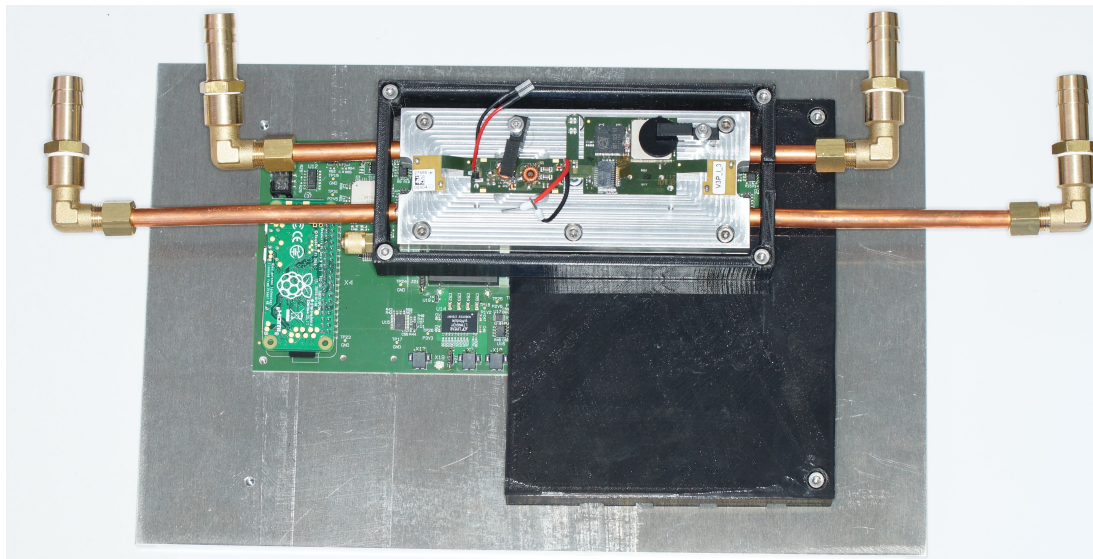


Figure 5.21: Picture of the cooling system for the service hybrid testing. The left part of the test board lid and the cover of the cold box are removed.

5.6 Conclusion

The testing scheme for 2S service hybrids based on a modular system has been presented. Individual test boards, each one equipped with a Raspberry Pi Zero W miniature computer, enable a nearly stand-alone testing procedure. Minimal communication to a central server infrastructure and a back-end board is necessary. The test board possesses the capability to test the functionality of the service hybrids' DC-DC converters, the GBTx and GBT-SCA (later LpGBT), general line integrity, and the HV circuit. The Raspberry Pi's communication was outlined in detail. It is centred around the use of the programming language *Python*, which provides a great range of applications together with an easily readable syntax. The operational capabilities for all of the test board components, as well as supporting measurements, were presented. The general concept works in all cases. Further development needs to be undertaken in the area of the on-board HV leakage current measurements. The signal integrity of the clock, the slow control, and the data lines need to be improved. An effort is made to enhance the communication between the back-end board and the test board's GBTxs. Table 5.6 summarizes the tested components. The infrastructure for the reliable communication between the test board, the central server, and the back-end board needs to be established. A *LabVIEW* based graphical user interface has been presented. The presented cooling system needs to be commissioned.

Test board component	Testing implication	Status
Raspberry Pi	Test board control, communication, data logging	Working
ADC	Voltage monitoring	Working
HV circuit	Circuit integrity, isolation test	Working with external power supply, to be integrated on test board
INA226	Current and power monitor	Working
FPGA	Clock and reset testing (counting)	Concept works, data quality needs improvement
I ² C F-RAM	I ² C test (GBT-SCA slave)	Working
GBTx and VTRx	Data test	Concept works, data quality needs improvement

Table 5.6: Summary of the test board commissioning.

6 Summary and Outlook

This thesis presented a number of contributions to the Phase-2 outer tracker upgrade of the CMS experiment. The requirements for this upgrade include a two-staged DC-DC conversion scheme. The necessary DC-DC converters are placed on the 2S service hybrid and PS power hybrid, which are attached directly to each of the two-sided modules.

With the bPOL2V5 converter ASIC, the first radiation tolerant DC-DC converter for the second stage became available. To meet the lower inductance requirements while maintaining little radiating emission, low resistance, and low material consumption, an optimization study of air-core toroid inductors was carried out. Theoretical calculations and finite-element simulations were performed and a number of hand-wound inductor prototypes produced. The prototypes were examined using a bPOL2V5 evaluation board. The tests covered efficiency, the common and differential mode noise, electromagnetic radiation, and material consumption. No significant differences between a toroidal inductor and a, in terms of inductance and resistance comparable, solenoid were observed regarding efficiency and noise. The toroid radiates a weaker electromagnetic field into the surroundings. A suggestion for an inductor that can be used with the bPOL2V5 on the service and power hybrid was presented.

In preparation for the production and testing of a greater number of service hybrids, the development of a service hybrid test board started. It can be used in all phases of the service hybrid's quality control, in combination with active thermal cycling, and can be incorporated in a scalable infrastructure. The test board design and the employment of its major components were presented. The focus was laid on the miniature computer Raspberry Pi and the elements it controls. *Python* scripts and the three native interfaces GPIO, SPI, and I²C are the foundation for the communication. In addition, a number of external components are needed, most importantly a back-end board with three optical links per test board.

Test board prototypes have been commissioned. Communication with all components has been established and their functions have been successfully explored. They are summarized in Table 5.6.

In the near future, three more milestones lie ahead:

- The production and testing of the first PS power hybrid prototype. The two staged DC-DC conversion scheme with two DC-DC converters in the second stage will be implemented for the first time.
- The commissioning of the test board cooling system. It needs to be verified that the target temperature of -30°C can be reached quickly under operational conditions.
- A number of minor design flaws have been identified in the course of additional studies of the service hybrid's GBTx and GBT-SCA circuit. They obstruct the further development of the readout chain in combination with functional FE hybrid prototypes. Therefore, an improved version of the third generation is under preparation. It will increase the understanding of the full module and the hybrids can be used to build fully functional module prototypes.

The design phase of the hybrids is scheduled to conclude in the middle of 2019, followed by a year of prototyping, and the pre-production will start in the middle of 2020. The production

needs to start in the second quarter of 2021 and can last a maximum of two years, in order to allow enough time for module assembly. The test systems need to be developed and to become available in parallel.

Appendix

A PS module communication

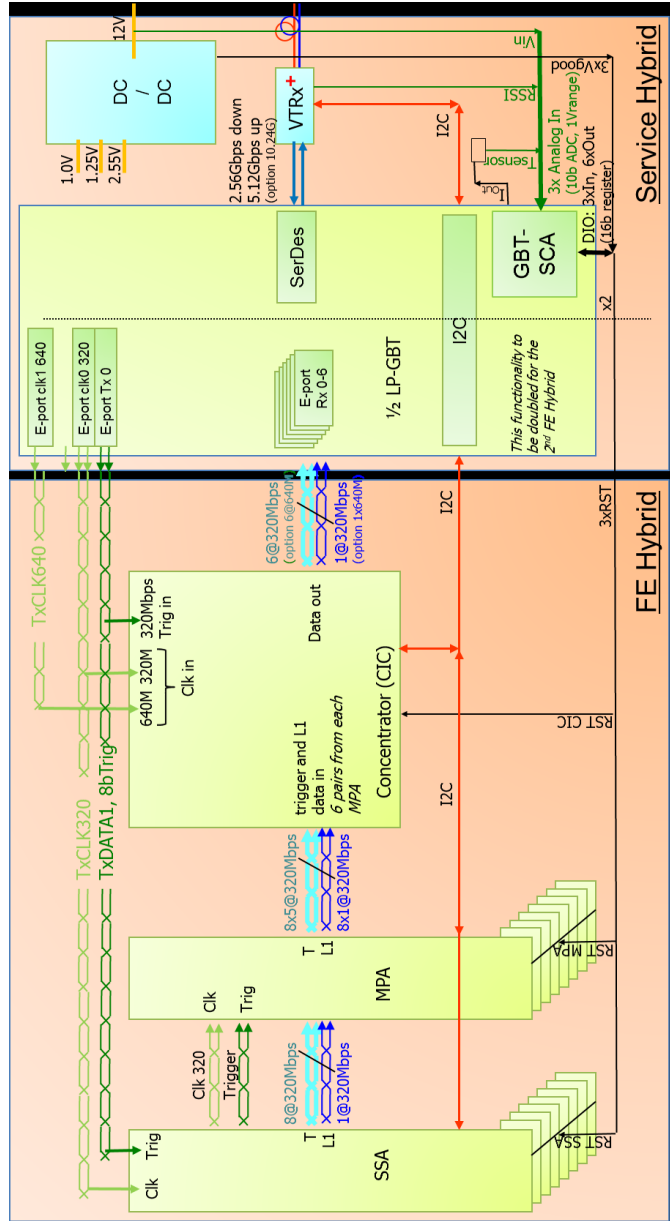


Figure A.1: Overview of the PS module communication [7].

B Service hybrid test procedures

The following three figures were courteously provided by Wacław Karpinski and Gerhard Pierschel, who also designed the test board. They summarize the different sets of service hybrid tests, which are performed by the test board. In the framework of this thesis, the figures were used as a guideline for the *Python* software development and to gain an understanding of all testing implications.

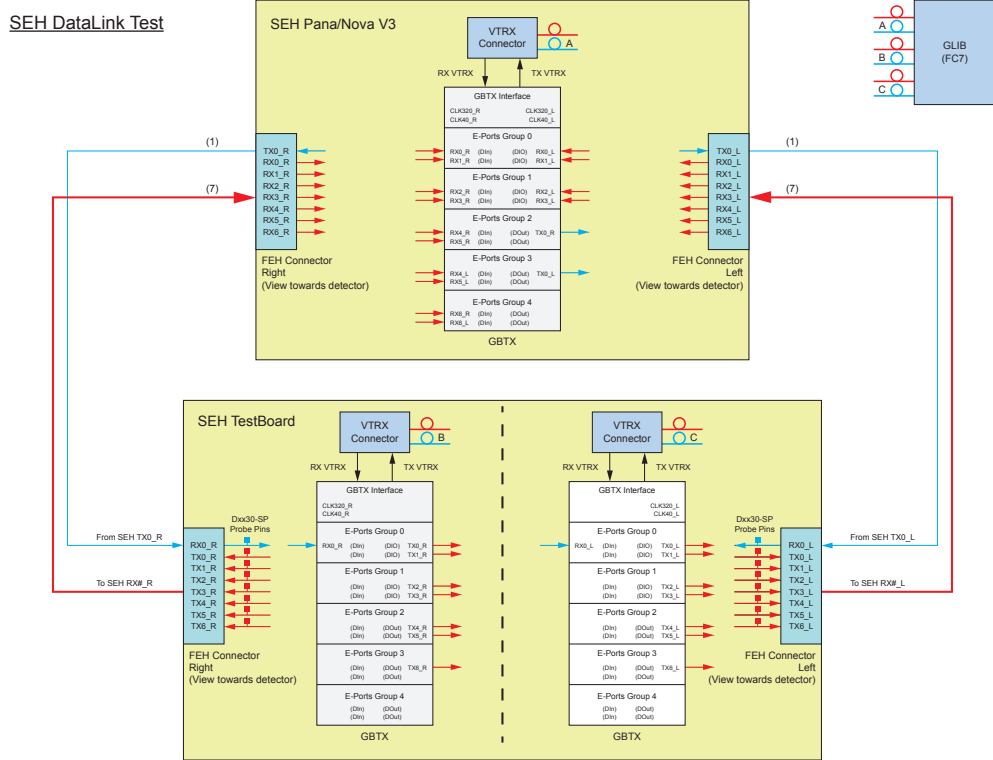


Figure B.1: Sketch of the data test procedure of the service hybrid. Courteously provided by Wacław Karpinski and Gerhard Pierschel [59].

SEH Power Test

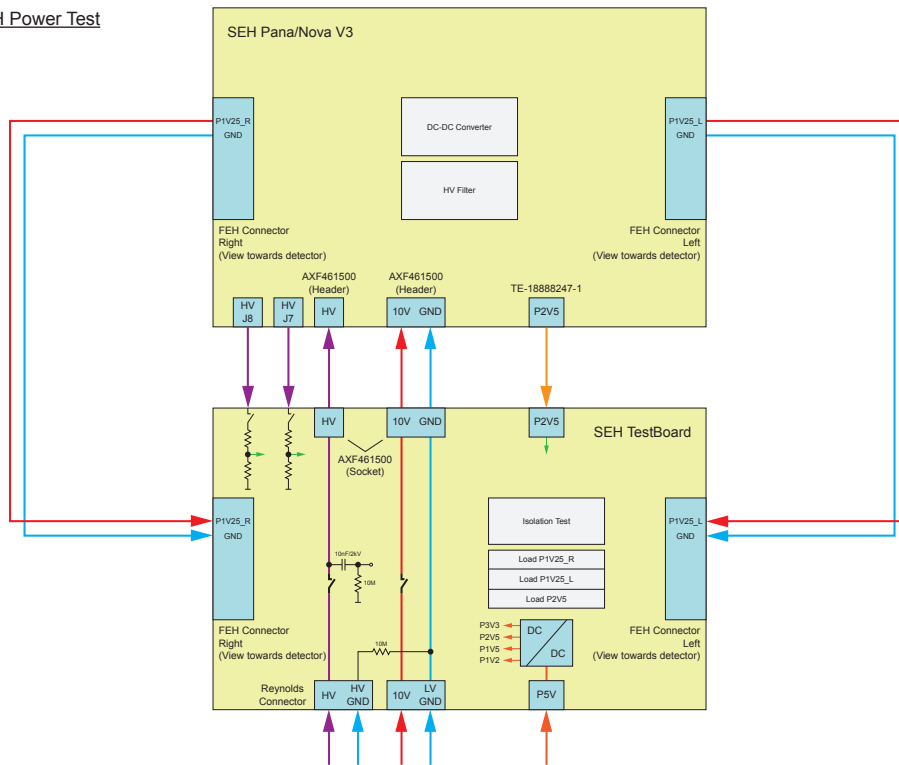


Figure B.2: Sketch of the power test procedure of the service hybrid. Courteously provided by Wacław Karpinski and Gerhard Pierschel [59].

SEH Clock & Slow Control Test

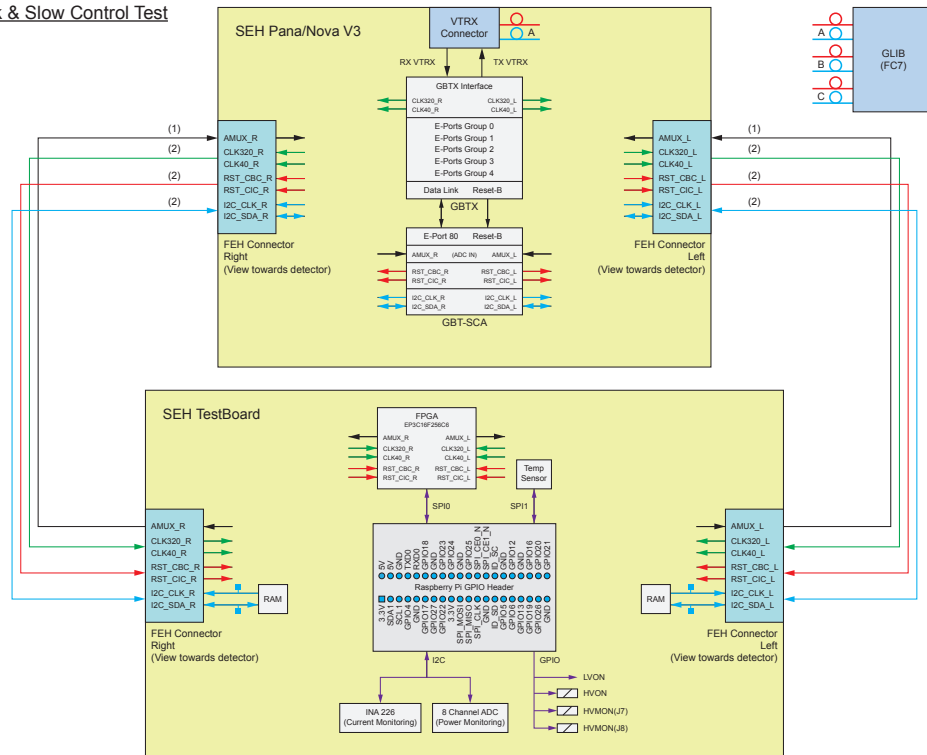


Figure B.3: Sketch of the clock and slow control test procedure of the service hybrid. Courteously provided by Wacław Karpinski and Gerhard Pierschel [59].

C Test board schematics

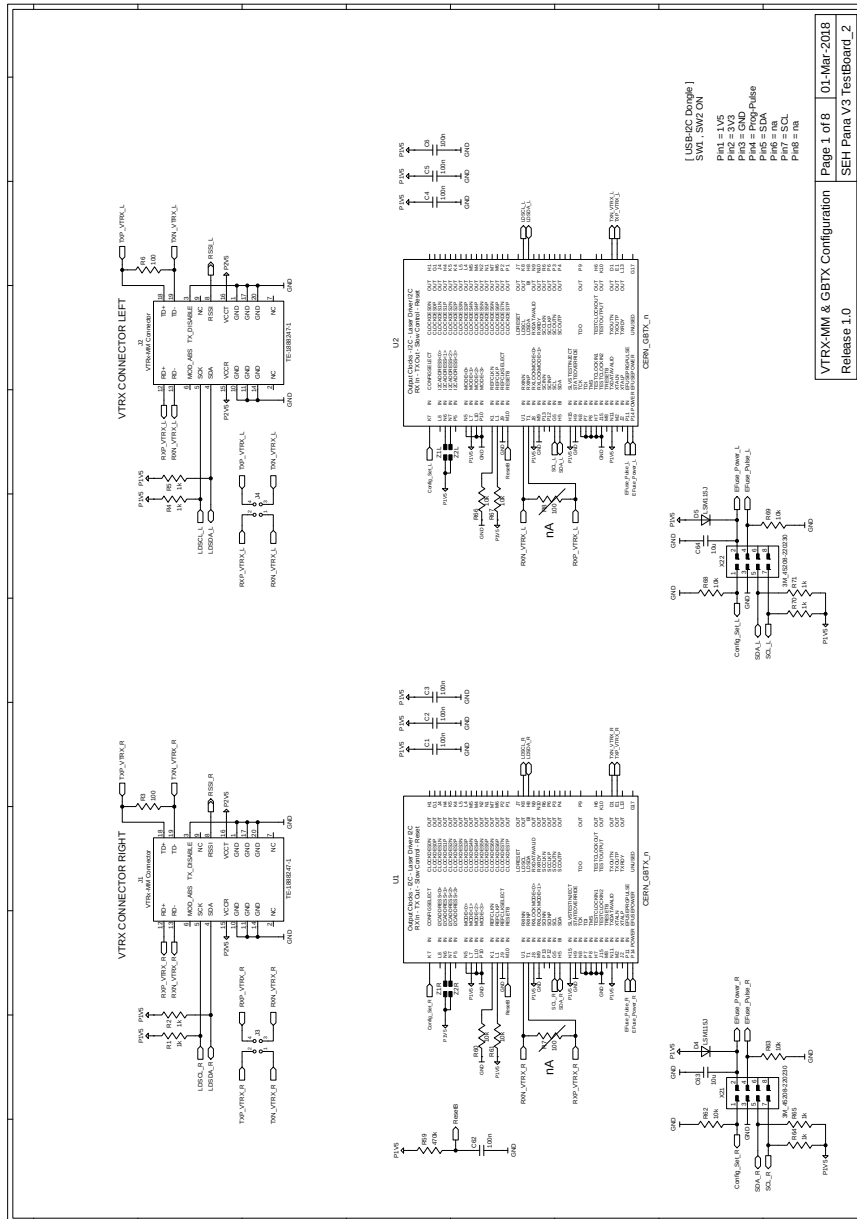
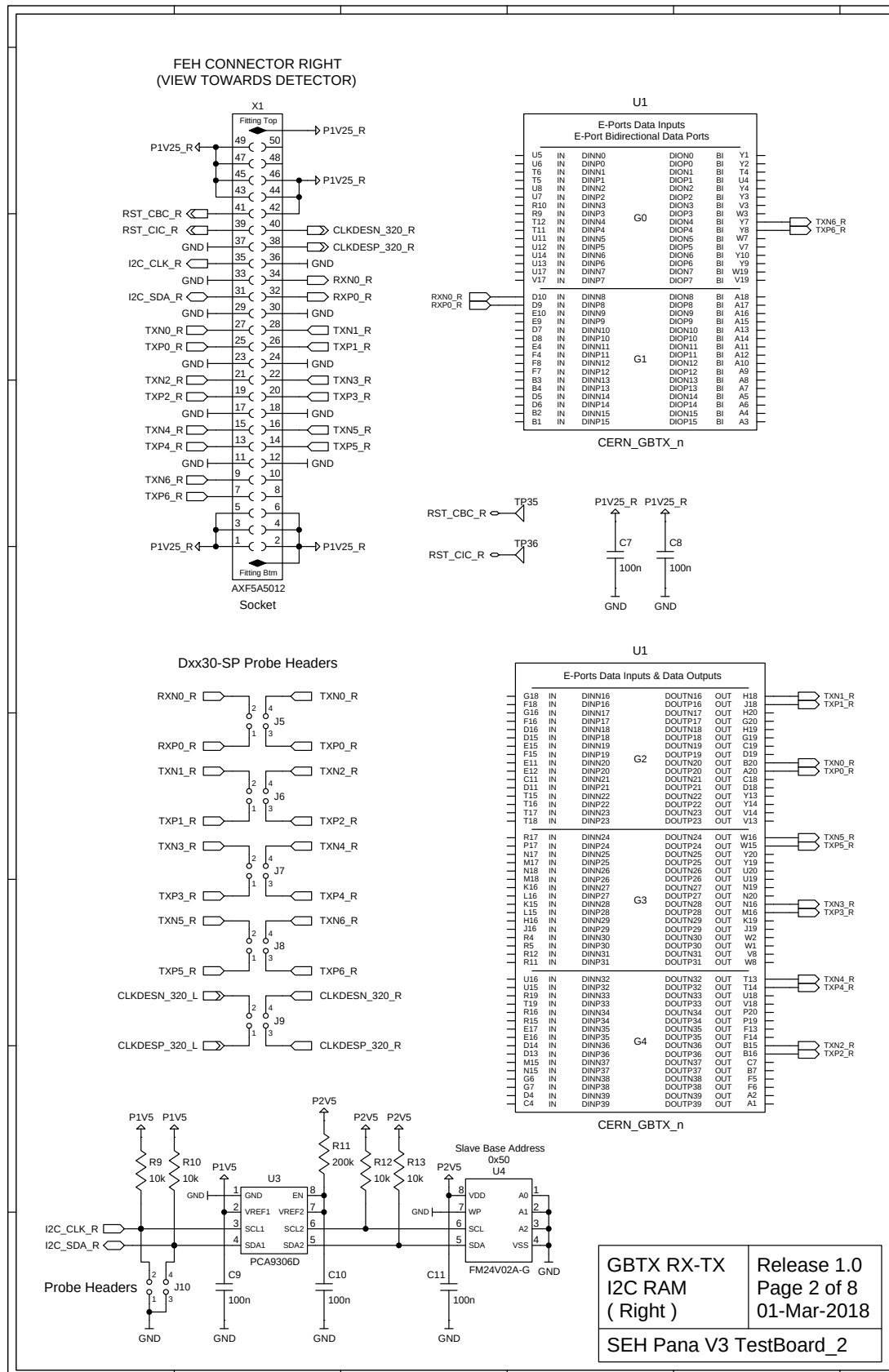


Figure C.1: Page 1 of the 2S service hybrid test board schematics [60].



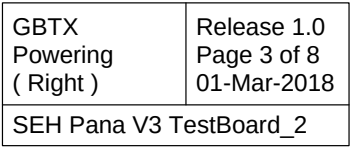


Figure C.3: Page 3 of the 2S service hybrid test board schematics [60].

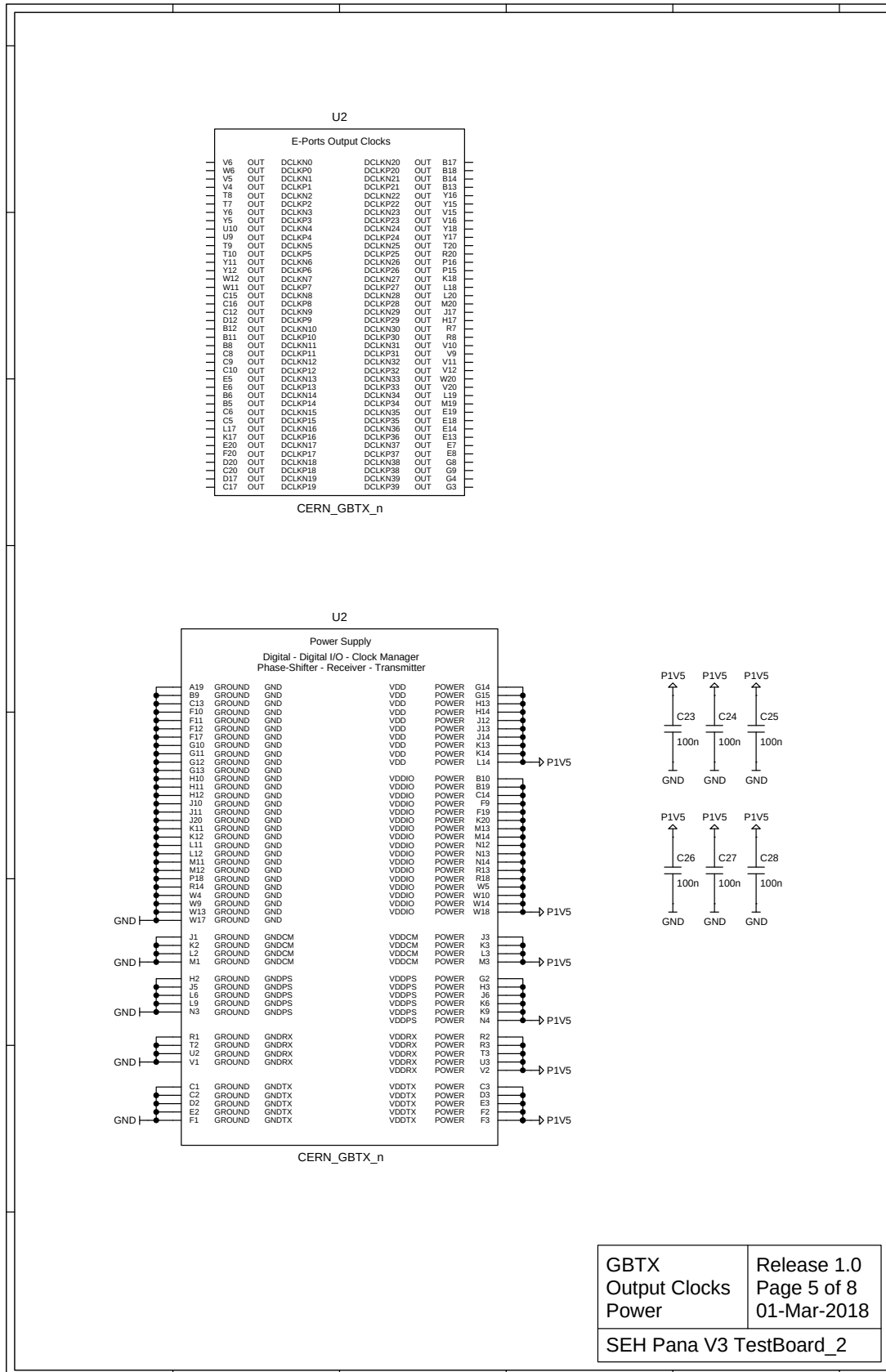
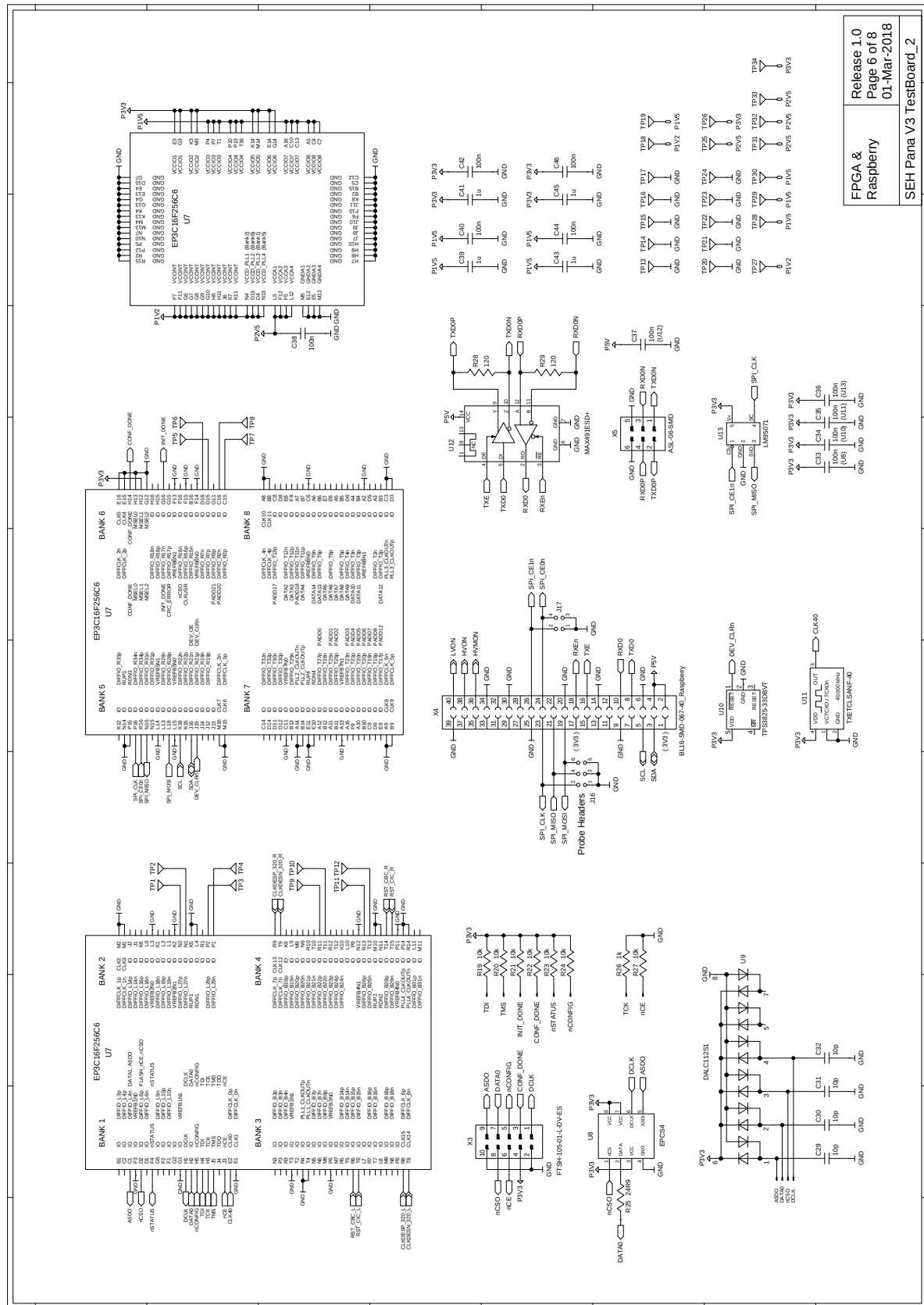


Figure C.5: Page 5 of the 2S service hybrid test board schematics [60].



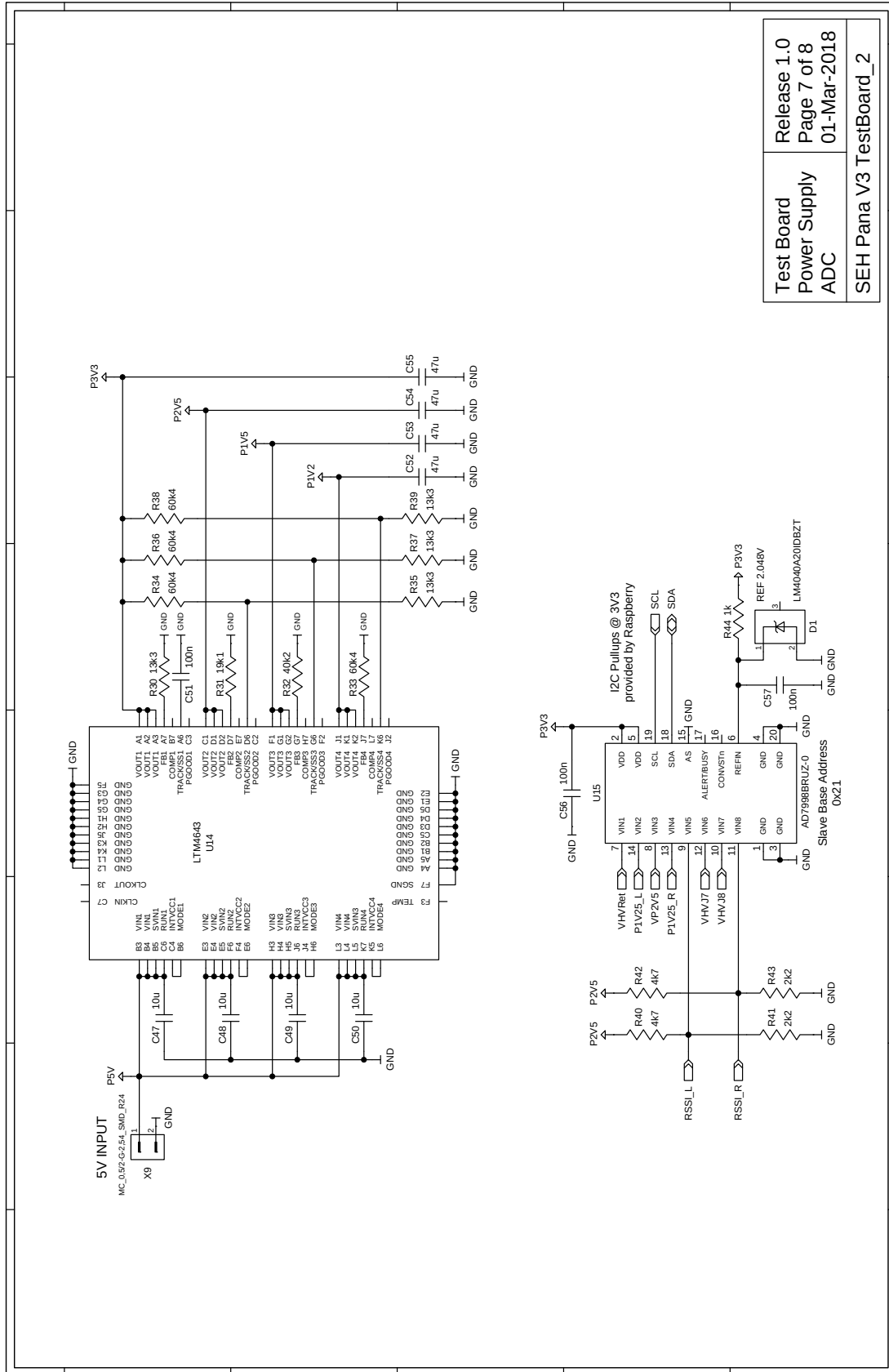


Figure C.7: Page 7 of the 2S service hybrid test board schematics [60].

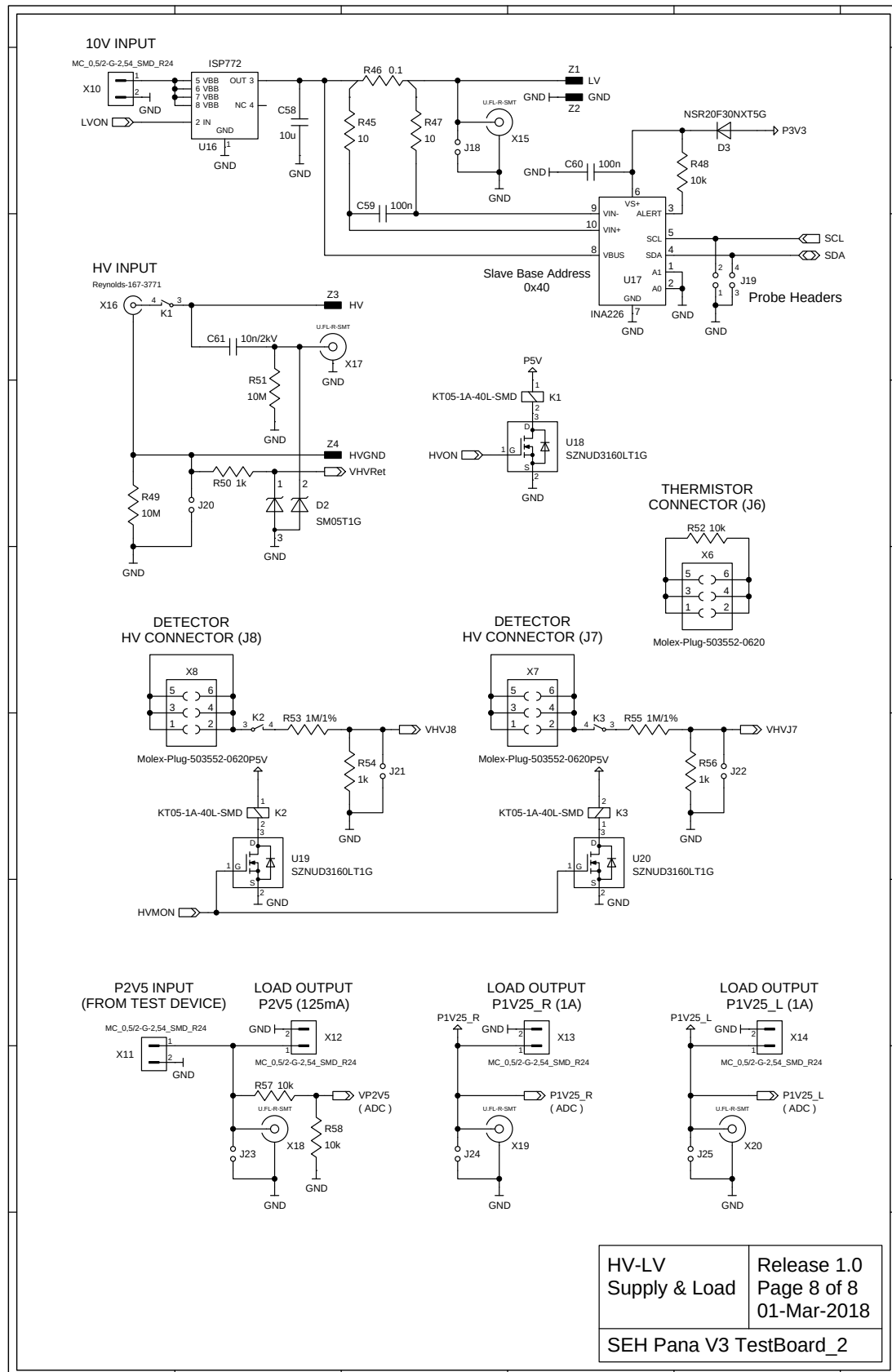


Figure C.8: Page 8 of the 2S service hybrid test board schematics [60].

D Test board FPGA opcodes

Opcode Bit Definitions:

bit 7: 0 Unused

bit 6: 0 Unused

bit 5 4 3: 0 0 0 = Clock Counter, 0 0 1 = CBC Pulse Counter, 0 1 0 = CIC Pulse Counter, 0 1 1 = AMUX

bit 2: 0 = RIGHT (Counters, AMUX), 1 = LEFT (Counters, AMUX)

bit 1: 0 = Write, 1 = Read

bit 0: 0 = Reset, 1 = Enable/Set

Opcode	Bit 76 5432 1 0	Function
0	00 0000 0 0	Reset Clock320 Counters (**UNUSED**)
1	00 0000 0 1	Enable Clock320 Counters for 100us; Test Mode: Count internal clock cycles (4000 Counts @40MHz)
2	00 0000 1 0	Read Clock320 Counter RIGHT
6	00 0001 1 0	Read Clock320 Counter LEFT
8	00 0010 0 0	Reset CBC Counters
9	00 0010 0 1	Enable CBC Counters; Test Mode: Count 100 clock cycles
10	00 0010 1 0	Read CBC Counter RIGHT and disable CBC Counters
14	00 0011 1 0	Read CBC Counter LEFT and disable CBC Counters
16	00 0100 0 0	Reset CIC Counters
17	00 0100 0 1	Enable CIC Counters
18	00 0100 1 0	Read CIC Counter RIGHT and disable CIC Counters
22	00 0101 1 0	Read CIC Counter LEFT and disable CIC Counters
24	00 0110 0 0	Reset AMUX RIGHT
25	00 0110 0 1	Set AMUX RIGHT
28	00 0111 0 0	Reset AMUX LEFT
29	00 0111 0 1	Set AMUX LEFT
32	00 1000 0 0	Reset Test Mode
33	00 1000 0 1	Set Test Mode
26	00 0110 1 0	Read Status Register
		bit 15 - 5: 0
		bit 4: Test Mode
		bit 3: CIC Count Enable
		bit 2: CBC Count Enable
		bit 1: AMUX_L
		bit 0: AMUX_R

Figure D.1: Summary of the FPGA opcodes, which are used on the test board for the slow control and clock tests of the service hybrid. Based on a work by Gerhard Pierschel [61].

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Acknowledgement

I would like to thank Prof. Dr. Lutz Feld for the opportunity to write this thesis in his working group. His close contact and critical yet constructive supervision made this work possible. Special thanks go to Prof. Dr. Jörg Pretz for his willingness to be co-corrector of this thesis.

Major thanks go to Dr. Katja Klein for her continuing support and advice and her constructive inputs to this work. I would like to thank the Ph.D. students in our working group, Marius Preuten, Max Rauch, and Martin Lipinski, for their time and advice and the welcoming working environment. I thank my co-master student Nicolas Röwert for our frequent exchange and mutual support. Special thanks go to my colleagues from the III. Physikalisches Institut B and our analysis working group. They provided many positive inputs and made common activities very enjoyable.

Special thanks also go to the CERN group, which is developing the bPOL2V5 and provided me with the evaluation board.

My work would not have been possible without the work of our mechanical and electrical workshop and the contributions of the engineers. So my thanks go especially to Dipl.-Ing. Gerhard Pierschel, who provided the test board's FPGA firmware and gave many inputs on the testing procedures, Irfan Özen, who prepared countless parts for me, and Dipl.-Ing. Wacław Karpinski, who coordinated many activities and provided a lot of insights to his designs. The test board cooling system and the cores for the inductor studies were provided by Michael Wloch and Karl-Heinz Dreger. To Franz Josef Neus and his colleagues many thanks for their help with the coil prototyping and many other electrical tasks.

I would like to thank my girlfriend Hanna, my parents, and my whole family for their lasting support.

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