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# DÉVELOPPEMENT D'UNE ÉLECTRONIQUE DE LECTURE EXTERNE POUR UN PHOTODÉTECTEUR HYBRIDE

# DEVELOPMENT OF AN EXTERNAL READOUT ELECTRONICS FOR A HYBRID PHOTON DETECTOR

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## Travail de fin d'études

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# Résumé

Ce travail de fin d'études couvre l'étude et le développement d'une électronique de lecture externe pour un détecteur de photon hybride. Ce projet a nécessité dans un premier temps une étude approfondie du bruit électronique intrinseque du système existant. Dans un deuxième temps, de nouvelles cartes èlectroniques ont été developpées. Ces dernières ont été validées au cours de tests en faisceau lors de la troisième phase du projet.

L'électronique de lecture des HPD est incorporée au sein du tube à vide des HPD. La mise à jour de toute l'infrastructure électronique du LHCb et de son nouveau système de déclenchement nécessitera donc un remplacement de tous les HPD présents dans le détecteur Cherenkov du LHCb. Le successeur de référence est le photomultiplicateur multi-anode. Une option alternative sous la forme d'une HPD avec électronique de lecture externe est étudiée dans ce travail.

Etant donné le signal relativement faible de $5000e^-$ créé lors de chaque collision d'un photo-electron dans un HPD, le point clé est le bruit électronique. La première priorité a donc été d'identifier et de comprendre les sources de bruit lorsque l'électronique de lecture est externalisée. Les deux principales sources de bruit proviennent de la puce de lecture utilisée et de l'architecture interne du boîtier céramique.

La compatibilité d'une électronique de lecture externe avec l'infrastructure actuelle du détecteur Cherenkov a été demontrée par la réalisation de nouvelles cartes électroniques de taille plus réduite. A cet effet, l'approche initiale avec deux cartes élecroniques a été réutilisée et de nouvelles cartes respectant les dimensions du détecteur ont été developées.

Ces nouvelles cartes ont été utilisées avec succès lors de tests en faisceau, ce qui a permis de valider la faisabilité et le potentiel du concept.

Dans le futur, l'amélioration du rapport signal à bruit implique le développement d'une nouvelle puce de lecture électronique à plus faible bruit ainsi qu'une refonte du design du boîtier céramique.

# Acknowledgements

This space could be dedicated to only one person who has guided me like a spiritual father: Thierry Gys. He took time to welcome me in this totally new environment and to train me up to the CERN standards.

However, I would also like to thank two wonderful teachers, who have unconditionally supported me during my whole engineer education: Jacques Tichon and Salvador Garcia.

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I am also grateful to Ian McGill and Florentina Manolescu for their various contributions in the wire bonding field, Bertrand Mehl and Sylvain Kaufmann for their advices concerning PCB manufacture and assembly, and Stephen Wotton who has played a major role in the success of HPD beam tests.

The proof-of-concept idea was warmly supported by Burkhard Schmidt and was initially fuelled by two students: Oğuz Kazan and Robert Paluch. Thanks to Hans Dijkstra, a complete readout system has been made available for the whole duration of the project.

I have a special thought about my parents and my partner for their integral support during this year.

All these persons have contributed, with their availability and their skills, to make this technical student programme possible and successful. Thank to all of them from heart.

# Contents

# Chapter 1

# Introduction

## 1.1 The creation of CERN

The acronym "CERN" comes from the French « Conseil Européen pour la Recherche Nucléaire » and dates from the year 1952 during which twelve European states signed an agreement to set up a joint venture aiming at establishing a world-class fundamental physics research organization. Geneva was selected the same year as the site and ground was broken on the Meyrin site in 1954 (8 km from Geneva). The Council was dissolved but the acronym remained afterwards [1].
The history of CERN is directly correlated to the accelerators that have been involved in high-energy particles research since its foundation [2]:

**1957** The first CERN accelerator was called Synchro-Cyclotron (SC). It was used until 1990.

**1959** The first CERN synchrotron called Proton Synchrotron (PS) was commissioned. It is still being used to accelerate and inject different kinds of particles in newer infrastructures.

**1976** The CERN Super Proton Synchrotron (SPS) starts up. This is CERN's first giant accelerator: 7 km in circumference, many different kinds of particles handled and still used for its versatility. A major highlight came in 1983 with the Nobel-prize-awarded discovery of W and Z particles, with the SPS running as a proton-antiproton collider.

**1989** The Large Electron–Positron Collider (LEP) starts colliding electrons and positrons in a 27 km underground ring. It was shut down in 2000 and dismantled to make room for the construction of the Large Hadron Collider (LHC).

**2008** Inauguration of the LHC, the most powerful accelerator ever built. It consists of a 27 km ring of superconducting magnets with a number of accelerating structures to boost the energy of the particles along the way. Two high-energy proton beams travel in opposite directions close to the speed of light within cavities under ultra-high vacuum. The beams are guided around the accelerator ring by a strong magnetic field produced by superconducting electromagnets [3]. The protons collide at four dedicated places.

## 1.2 The "Big Four"

There are currently four large experiments at the LHC:

**ATLAS** (A Toroidal LHC ApparatuS) is about 45 meters long, more than 25 meters high, and weighs about 7,000 tons. It is half as big as the "Cathédrale Notre Dame" in Paris and weighs the same as the Eiffel Tower. It aims to study basic forces that have shaped the Universe since the beginning of time, the origin of mass, extra dimensions of space, microscopic black holes and evidence for dark matter [4].

**CMS** (Compact Muon Solenoid) is an experiment which is designed to observe a wide range of particles and phenomena produced in high-energy collisions in the LHC. Like a cylindrical onion, several detector layers measure the different particles, and use the resulting key data to build up a picture of events at the heart of the collision. Given that the CMS solenoid provides a 4T magnetic field (100'000 times stronger than that of the Earth) and that the amount of iron grows in proportion with the magnetic field, the CMS experiment weighs 12'000 tonnes for only 15 metres in diameter [5].

ATLAS and CMS have announced in July 2012 the long-awaited discovery of the Higgs boson, a particle that contributes to the origin of mass. Following this discovery, F. Englert and P. Higgs were awarded the Nobel Prize in physics for their theoretical contributions in this field.

**ALICE** (A Large Ion Collider Experiment) aims at recreating the conditions just after the Big Bang, equivalent to a temperature 100'000 times higher than that in the center of the sun. This state of matter is called "quark-gluon plasma". The detector weighs 10'000 tonnes and is 26 m long, 16m high and 16m wide [6].

**LHCb** (Large Hadron Collider beauty experiment) records the decay of particles containing b quarks and anti-quarks ($b\bar{b}$), collectively known as 'B mesons'. The experiment's 4'500 tons detector is specifically designed to filter out these particles and their decay products [7].

## 1.3 LHCb

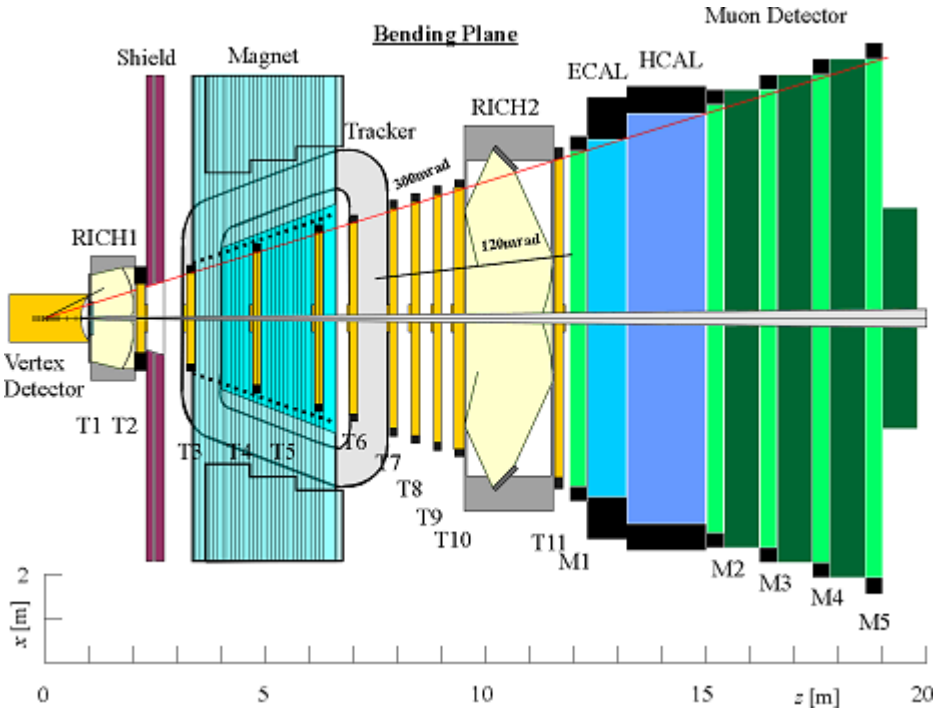


Figure 1.3.1: LHCb's sub-detectors [8]

Because LHCb is dedicated to the study of B mesons, the detector geometry is motivated by the way the ($b\bar{b}$) are produced, predominantly in the same forward cone [9]. Each sub-detector has its own functionality, they work collectively to gather information about the identity, energy, trajectory and momentum of each particle [10]. A view of all sub-detectors involved in LHCb is visible in Figure 1.3.1.

**VELO** (VErtex LOcator) picks out B mesons from the multitude of other particles produced. It uses silicon strip detector positioned close to the interaction point (where protons collide), at a distance of 5 mm [11].

**RICH** (Ring Imaging CHerenkov) detectors are used for particle identification. They will be treated specifically in section 1.4 [12].

**Dipole magnet** produces magnetic field to bend the trajectory of charged particles. From the curvature, the particle momentum can be inferred [13].

**Trackers** sample the trajectory of charged particles passing through the detector [14].

**Calorimeters** are designed to measure the particles' energy [15].

**Muon system** is located at the far end of the detector and aims to detect muons (heavy electrons) that are present in the final states of many B meson decays [16].

## 1.4 Ring Imaging Cherenkov Detectors

The LHCb experiment includes two RICH detectors. Cherenkov light is produced when a charged particle moves faster than light in a medium (silica aerogel and dense gases in the present case). The Cherenkov light cone is imaged via a set of spherical and flat mirrors as a ring onto photon detectors, as illustrated in Figure 1.4.1 [12].

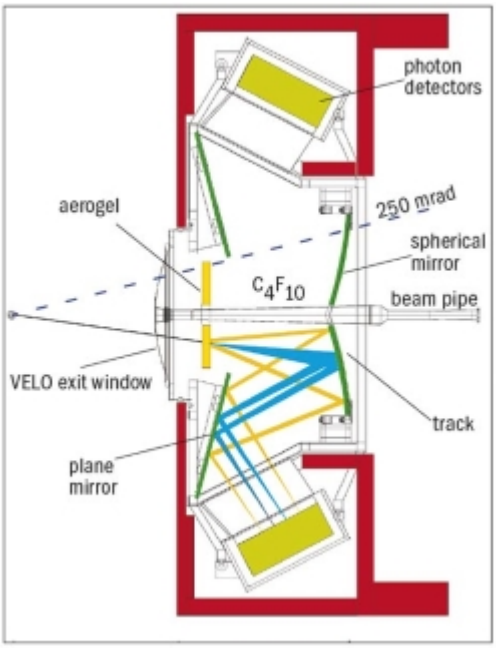


Figure 1.4.1: Layout of RICH1 illustrating how mirrors bring Cherenkov light at the detector plane [17].

The opening angle $\theta_c$ of the cone obeys the relation $\cos\theta_c = 1/n\beta$, where $n$ is the refractive index of the medium and $\beta$ is the particle velocity relative to the velocity of light in free space. Combining the information from tracking detectors for the momentum and from RICH detectors for the velocity allows to know the mass of the particle and therefore its identity [17]. In order to detect incoming Cherenkov photons, both RICH detectors use hybrid photon detectors (HPD), described in Chapter 2 and illustrated in Figure 1.4.2. The RICH detectors are equipped with 484 tubes in total. 196 are installed in RICH1 and 288 in RICH2 [12].

Figure 1.4.2: Hybrid photon detector [18].

# Chapter 2

# Hybrid Photon Detector

## 2.1 Concept

A hybrid photon detector combines in a single device vacuum photocathode tube and solid-state technologies [19]. When an incoming photon hits a photo-cathode, electron emission occurs through the photoelectric effect. The photo-electron is accelerated by a high electric field to a silicon detector (see Figure 2.1.1) and dissipates its kinetic energy within the detector surface. This process results in the creation of electron-hole pairs. The HPD gain $G$ is given by: $G = \frac{V-V_0}{\epsilon}$ where $V$ is the applied voltage, $V_0$ is the dead layer voltage, and $\epsilon$ is the average energy to create one electron-hole pair in silicon (3.6eV) [17].

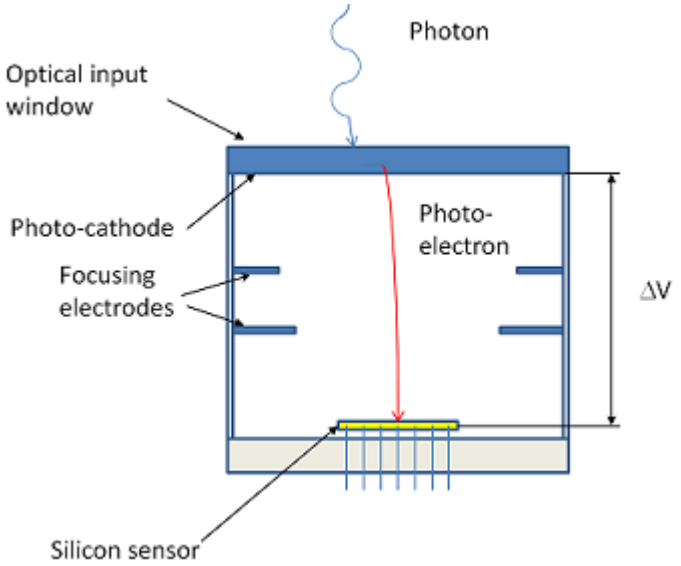


Figure 2.1.1: Schematic principle of an HPD [18].

Typical gains range between 3000 and 8000 electrons ($e^-$) [20]. Since this amplification process is achieved in one step, signal fluctuations are intrinsically very small. Consequently, the overall fluctuations are dominated by the noise of the readout electronics [21]. An HPD offers no dead zones between pixels and free choice of segmentation (50 µm - 10 mm). An HPD with demagnifying electron optics allows a large coverage with reduced number of tubes [20] and a silicon detector with reduced cell size, an advantage to optimize signal-to-noise ratio (SNR) (see later).

## 2.2 Pixel-HPD

For the LHCb-RICH detectors, the option that has been selected is the pixel-HPD developed in close collaboration with photo-sensor industry (DEP[1]) [23]. The main requirements are the following: the Cherenkov photons with wavelength from 250 to 600 nm (ultraviolet) must be detected with high efficiency over a total area of 2.9 $m^2$ and a granularity of 2.5 mm × 2.5 mm. The time resolution should be better than 25 ns to cope with the LHC bunch-crossing rate [24].

Given the 25 ns peaking time requirements and the low gain ($5000e^-$), front-end pixel readout electronics has been encapsulated in the tube. This results

[1]Delft Electronic Products, now Photonis-NL.

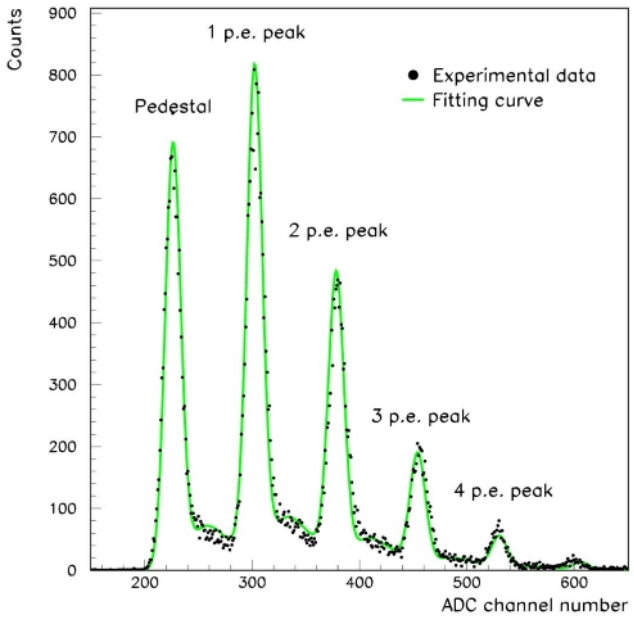


Figure 2.1.2: Typical photoelectron spectrum recorded from a full-scale prototype tube operated at 20 kV and read out with external analogue electronics (1.2 µs peaking time) [22].

in a higher signal-to-noise ratio but requires these electronics to be fully compatible with the bake-out cycles carried out prior to the deposition of high-quality photo-cathodes [19].

The silicon pixel sensor is 16×16 $mm^2$ in size and consists of 256×32 elements (62.5 µm x 500 µm each) with matching pixel electronics [25]. This pixel array is bump-bonded[2] to a binary readout chip. In this configuration, each sensor pixel is connected to a read-out chain. This flip-chip assembly is mounted and wire-bonded to a ceramic carrier.

[2]Method for interconnecting semiconductor devices to external circuitry using solder bumps.

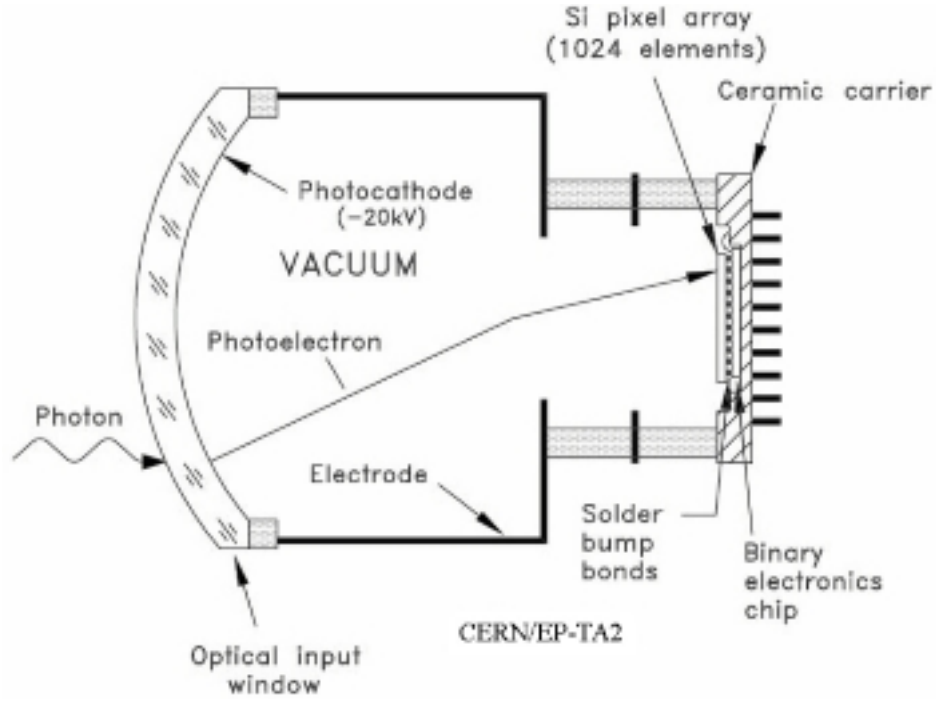


Figure 2.2.1: Schematic drawing of the baseline pixel-HPD [18].

The readout chain is composed of a differential pre-amplifier (typ. $140e^-$ RMS noise), a 25 ns shaper and a discriminator with 1100-1300 $e^-$ threshold ($30e^-$ RMS spread with 3-bit adjust) [25].

In a pixel HPD, two detrimental effects reduce the photo-electron detection efficiency: the first effect appears with segmented detectors. Charge signals created at the pixel boundaries is shared between detecting elements. The other effect is photo-electron backscattering: with 18% probability the photo-electron releases only half of its energy on average [19, 26]. This is responsible for the continuum observed between the peaks in Figure 2.1.2. These two effects are illustrated on Figure 2.2.2.

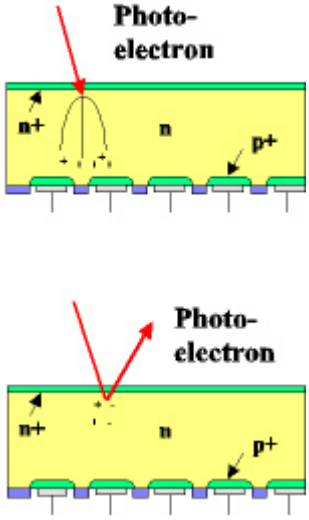


Figure 2.2.2: Illustration of charge-sharing and backscattering effects [18].

## 2.3 Upgrade of electronics infrastructure in LHCb

The operation of the current LHCb detector will be completed by 2018. In a next phase, it is foreseen to run at a beam luminosity 10 times larger. Triggering at an increased readout rate requires a substantial change in the LHCb readout architecture (see Appendix) [27]. The current first level (level-0) trigger is fully hardware-based and events are accepted at the output of the level-0 pipeline at an average rate of 1MHz [9]. In the next upgrade this will be replaced with a full software trigger. This requires performing data acquisition and event building on the event-filter farm at the full rate of 40 MHz. It implies the replacement and re-design of the whole LHCb electronics.

Because the readout electronics is currently encapsulated in the HPD vacuum, this removal means a full replacement of all HPDs of the RICH detectors [27]. The baseline option is to replace the pixel-HPDs with multi-anode photomultiplier tubes (MaPMTs) and binary readout electronics. In parallel, new HPD developments are being pursued in the interest of maintaining an alternative backup technology for the RICH photon detectors [28].

# Chapter 3

# Hybrid photon detector with external readout

Pixel-HPDs currently used in the LHCb RICHes encapsulate both the silicon detector and its front-end electronics in the vacuum. The present project aims to explore the concept of an HPD with *external* readout electronics.

External readout has the advantage of decoupling photon detector and front-end electronics developments. For the LHCb-RICH upgrade, the overall design of the HPD tube would be similar to the design of the current pixel-HPDs, allowing a significant fraction of the existing photon detector infrastructure to be retained. The main difference would be in the anode part [28].

As pointed out in Section 2.1, the limited charge signal ($5000e^-$) from an HPD combined with the 25 ns signal peaking time is the key point. In other words, maintaining an acceptable signal-to-noise ratio is crucial in the propose new HPD configuration is crucial [28].

## 3.1 Project description

In an HPD with external readout (EXTHPD), the anode part is composed of a silicon sensor directly bump-bonded to a ceramic carrier. For the LHCb-RICH upgrade, the sensor would be composed of 490 hexagonal pads each 0.8 mm in size (flat-to-flat) corresponding to a granularity of about 3.2 mm at the photo-cathode level. The signals are routed from the anode through the carrier inserted in a zero insertion force (ZIF) socket. The socket is interfaced using printed circuit boards (PCB) to dedicated ASIC[1] chips [29]. The noise

[1]Application-specific integrated circuit.

levels of these chips should be low to match those required for HPD signals.

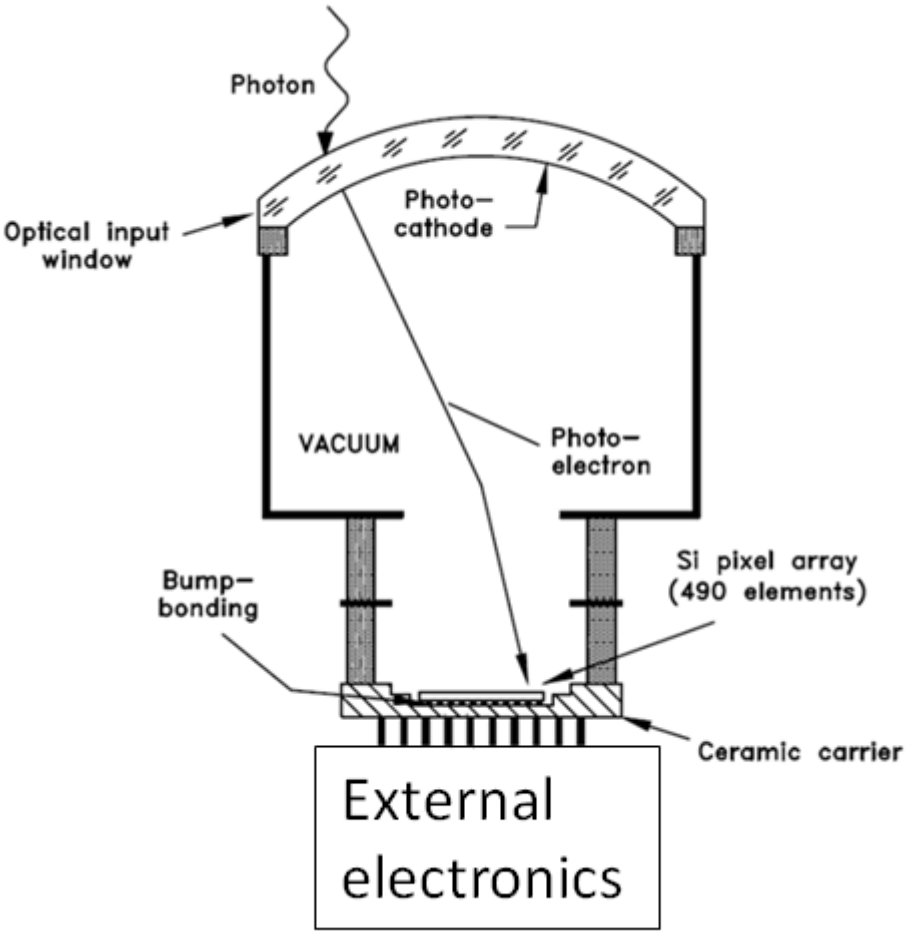


Figure 3.1.1: Sketch of an HPD with external readout [30].

### Proof-of-concept HPD

The proof-of-concept has been investigated using an HPD with 163 hexagonal pads (hexels). The HPD body design [22] is the one of the pixel-HPD and the anode was specifically developed for the BTeV experiment [31]. The hexels measure 1.4 mm flat-to-flat each in a close-packed arrangement, and are surrounded by a guard ring. Following recent promising progress in the recipe for HPD processing, which implements getter strips for lifetime improvements [32], two new HPDs with this configuration have been delivered in June 2013 [29].

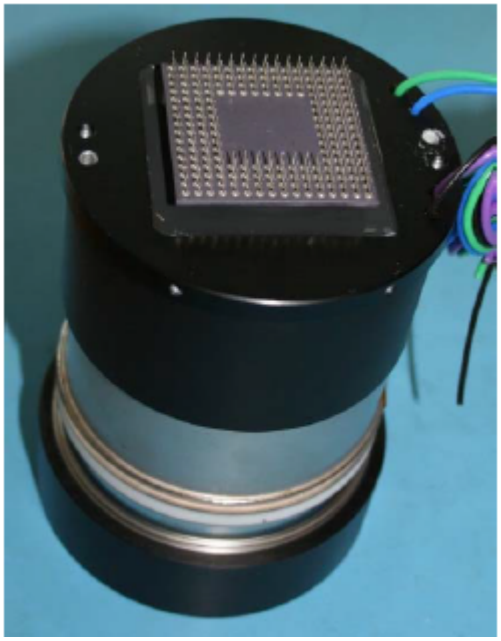

Figure 3.1.2: New HPD with [29].

**Front-end electronics**

The external front-end electronics is based on the Beetle ASIC chip [33]. This ASIC was found to be the only existing and easily available candidate with performance that is closest to the HPD requirements. In addition, Beetle chips have been implemented in a turn-key portable system developed by the Alibava company [34]. This system includes a complete readout and control electronics and the related data acquisition and analysis software.

The Beetle ASIC is a 128 channels pipelined readout chip and has been developed to match the specific requirements of the LHCb experiment. This chip is able to operate either in analogue or binary pipelined readout mode. It is currently used for the VELO, the trigger tracker and the inner tracker of LHCb.

Each channel consists of a charge-sensitive pre-amplifier, an active CR-RC pulse shaper and a buffer which form together the analogue front-end. The shaping of the front-end pulse can be tuned according to requirements. The equivalent noise charge (ENC) has been measured for a 25 ns peaking time to be $497e^- + (48.3e^-/\text{pF}) \times C_{in}$. In the binary mode, the output pulse is differentiated by a comparator. A threshold per channel is applicable with a

resolution of 5 bits, and input signals of both polarities can be processed.

The memory used as intermediate storage (pipeline) is realized as a switched-capacitor array of 130 x 187 cells operated as a ring buffer. The pipeline is filled at the same frequency as the bunch-crossing rate of the LHC. The memory provides a programmable trigger latency of a maximum 160 clock periods. This memory also includes a de-randomising trigger buffer of 16 stages, which means that up to 16 consecutive events can be read out without dead time.

The stored signal is retrieved from the pipeline by a resettable charge-sensitive amplifier which transfers it to an analogue multiplexer for serialisation. This multiplexer can operate in three different modes carrying the 128 channels on either 1,2 or 4 output ports. Within a readout time of minimum 900ns, differential current drivers bring the serialized data off chip.

There is a common mode compensation using a sense channel which provides data to be subtracted. In order to test and calibrate, each channel is equipped with an adjustable charge injector. Several Beetle chips might be linked in a daisy chain to share their output lines [33][35].

The Beetle readout chip has been designed for silicon strips detectors that provide charge signals (typ. $30000e^-$) larger than HPD charge signals (typ. $5000e^-$). The Beetle noise figures are consequently not fully optimal for HPD readout.

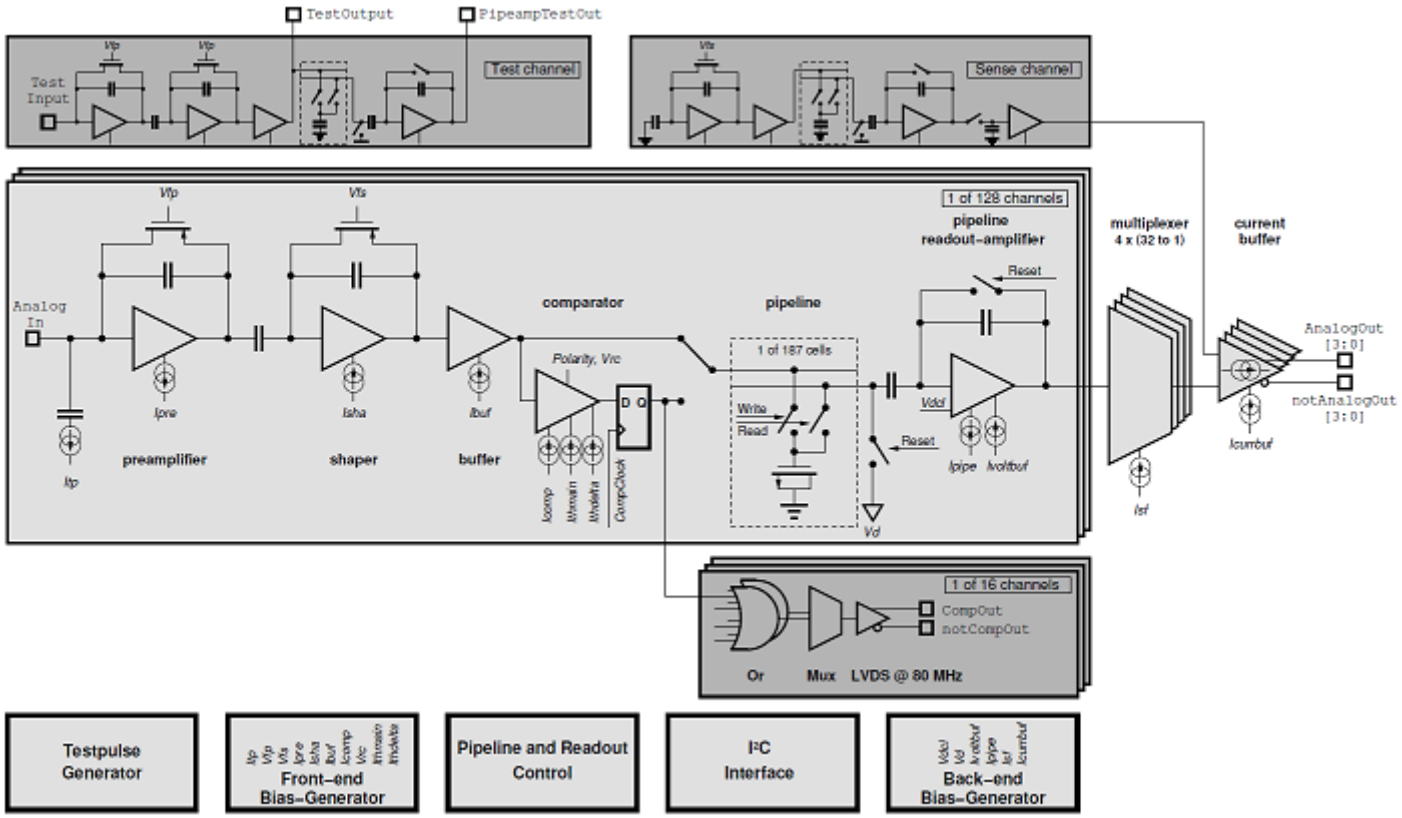


Figure 3.1.3: Beetle architecture [33].

### Alibava hardware and software

The Alibava portable readout system is based on two boards [36]:

**Daughter board** (DB) hosts two Beetle readout chips and pitch adapters (PA) to interface sensors. The 5V supply level required is sent through the motherboard. This 5V is regulated by two low drop-out linear regulators in order to match the required direct current of the readout chips (2.5V) and the buffer stage (3.3V). The detector is supplied directly from the DB. One standard DB was used to read out signals coming from the new HPDs.

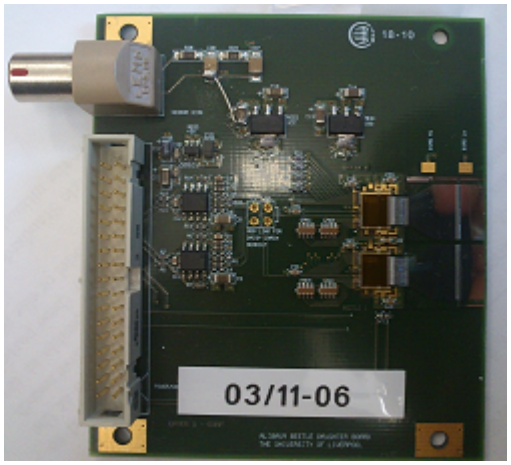


Figure 3.1.4: Standard daughter board from Alibava.

**Motherboard** This board is intended to process the analogue data from the Beetle readout chips. It manages trigger signals from outside and allows control of the whole system through a computer via USB. It is built around a FPGA Xilinx Spartan 3 clocked at 40MHz which can be reconfigured by flashing a PROM memory with a JTAG-to-USB cable.

**DAQ software** is written in Python and can be used either with a graphical user interface (GUI) or in batch mode.

**ROOT libraries** specifically written for the Alibava system are available for data analysis. ROOT [37] is a CERN object-oriented framework for large scale data analysis. ROOT incorporates an interpretor called CINT which allows to run directly C/C++ code. Explanation of the software set-up and the algorithms can be found in Appendix.

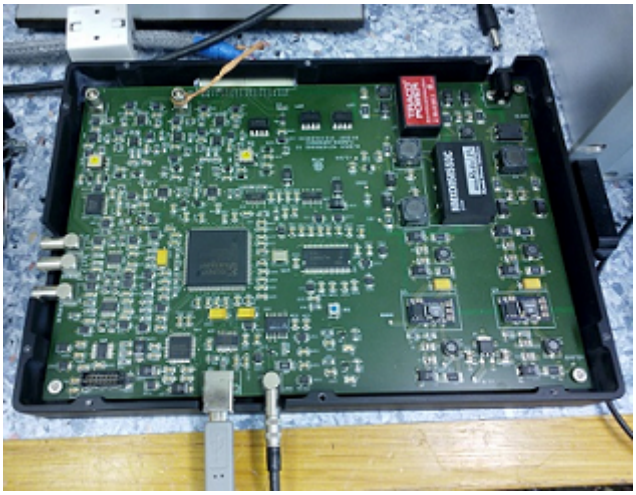

Figure 3.1.5: Motherboard from Alibava

### Ceramic carrier

The HPD anode interface with the outside is achieved with a ceramic carrier. The carrier has been designed and manufactured by the Japanese company Kyocera (Kyoto Ceramics). The carrier is made of alumina and the routing lines are in tungsten [38]. The carrier has 5 layers and 192 pins: 163 pins are dedicated to the 163 hexels, 6 pins to ground connections, 6 pins to silicon bias and 17 pins are not used and therefore will be connected to ground.

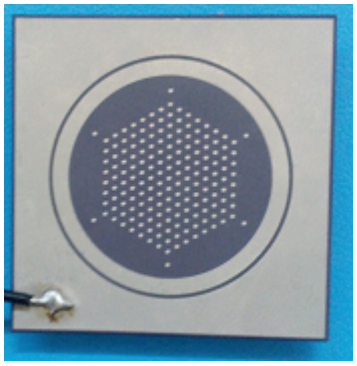

Figure 3.1.6: Top view of the bare ceramic carrier

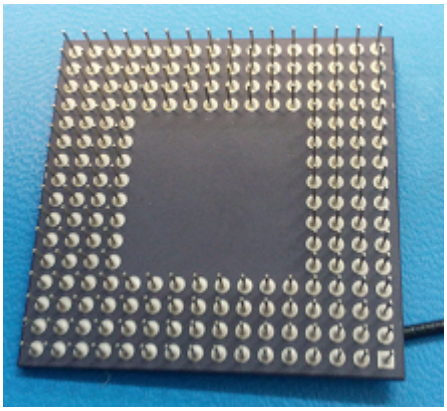

Figure 3.1.7: Rear view of the bare ceramic carrier. The 192 pins are arranged as an array of 16*16

### ZIF socket

A ZIF socket provides easy coupling of the HPD carrier to electronic boards. It integrates a lever on the side which pushes sprung contacts apart when moved, allowing an insertion with very little force. The lever is returned to its initial position which closes and grips inserted pins.

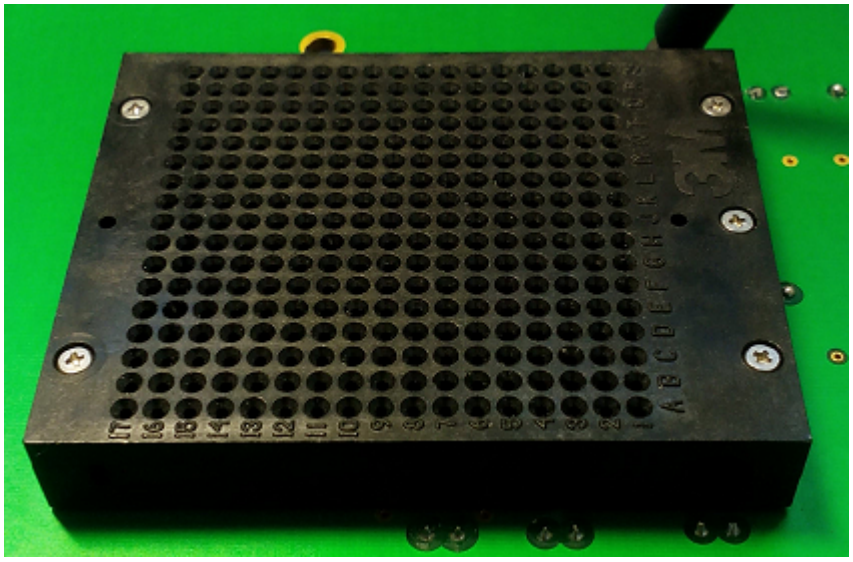

Figure 3.1.8: ZIF socket

### Initial front-end electronics

The initial front-end electronics consists of two boards, a standard DB from Alibava and a custom interface board. This board integrates footprint for the ZIF socket pins, wire-bonding pads, silicon sensor bias circuitry and calibration circuitry.

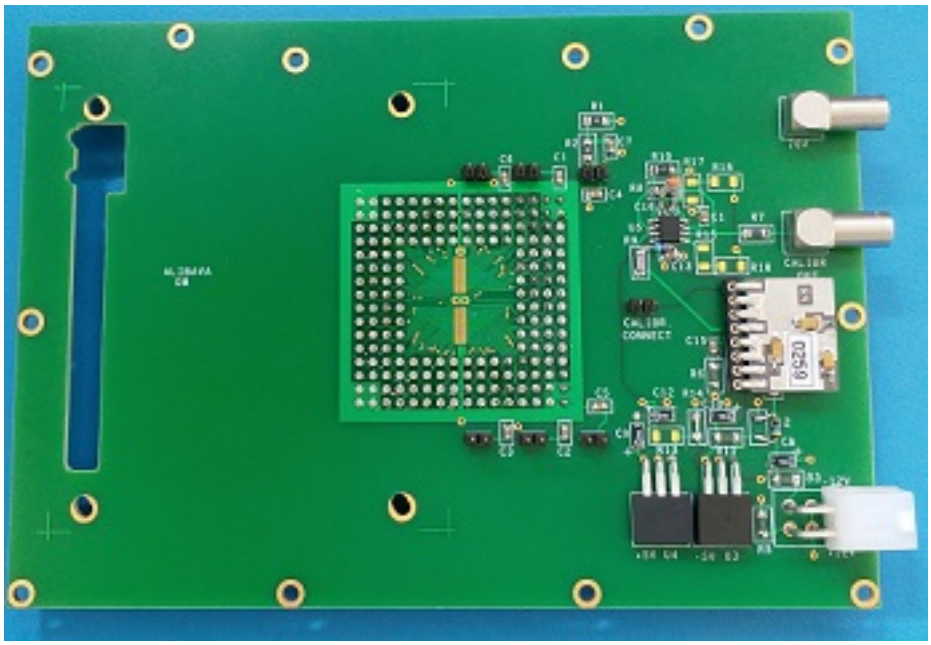

Figure 3.1.9: Initial interface electronic board

The interface board transmits signals from the HPD anode to the Beetle chips on the DB. The connections between the two boards are achieved with wire-bonding. On the left-hand side of Figure 3.1.9, there are marks and holes for the DB positioning. In the middle, there is a square region with routing lines from ZIF socket pins to wire-bonding pads. Six decoupling capacitors are placed at the periphery of this square region. On the right-hand side, the top LEMO[2] connector corresponds to the bias supply for the silicon sensor. The second LEMO connector is the output of the calibration circuit.

### Experimental set-up

The laser used in the laboratory is Hamamatsu Model PLP-10, a high-repetition picosecond pulsed laser. It offers selectable frequency up to 100MHz. The laser can be triggered externally, with a signal with an amplitude from

[2]From the company founder, Leon Mouttet

-4 to +4V [39]. Since the HPD detects single photons, and even if the laser releases only an ultrashort pulsed light, these pulses need to be filtered using neutral density filters to attenuate the number of incoming photons. The laser light is transported in optical fibers within a light-tight box. The HPD is mounted on a side wall of the box with its anode accessible from the outside as illustrated in Figures 3.1.10 and 3.1.11.

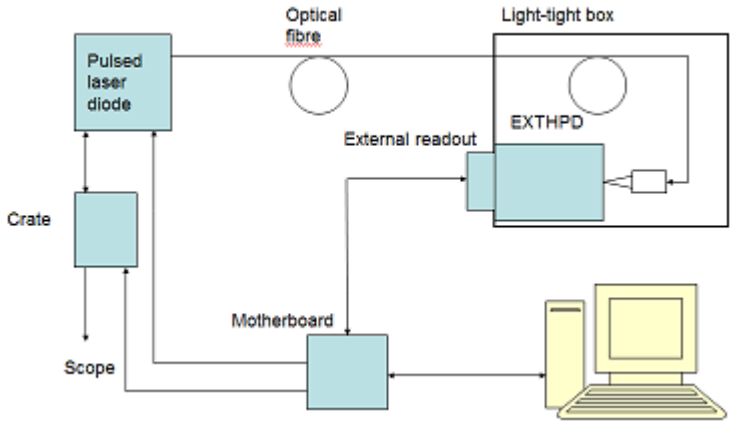


Figure 3.1.10: Schematic drawing of the experimental set-up [40]

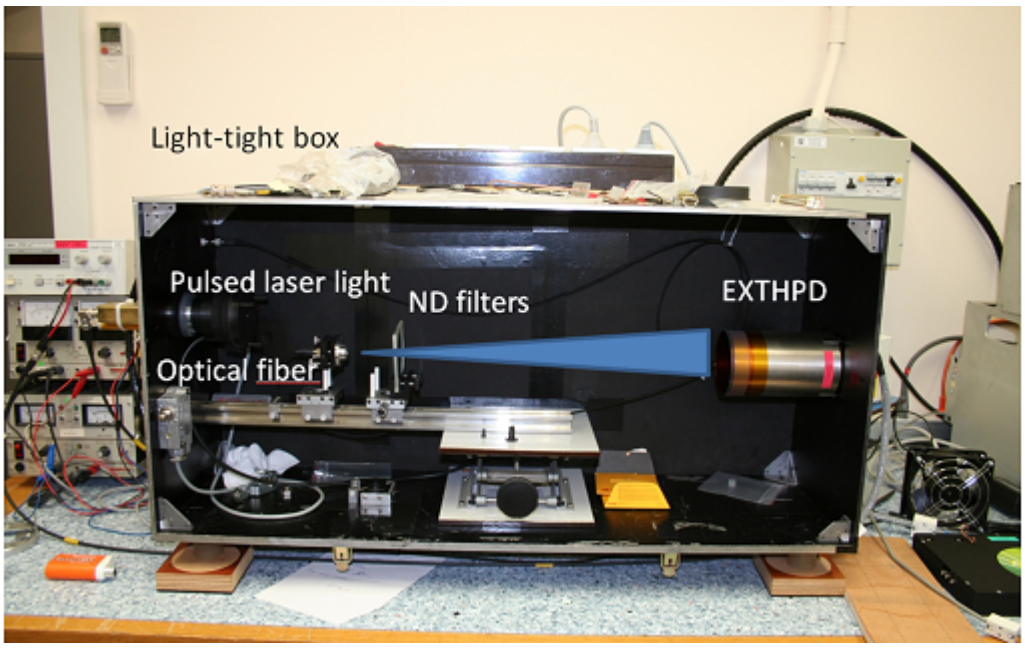


Figure 3.1.11: Picture of the experimental set-up

### 3.1.1 Initial student project

The EXTHPD was initially set up by two students[3] who commissioned both the software and the hardware. The Alibava DAQ software and specific ROOT libraries were installed under Ubuntu Linux. Bash shell and C/C++ scripts were prepared to automate the data taking and their analysis.

Preliminary assessment of the electronics was carried out on the relation between capacitive load and noise levels using discrete capacitors [41]. The first photo-electron spectra (Figure 3.1.12) were recorded with a long Beetle shaping time (50ns) to minimise the noise levels. Beetle operating parameters were further optimized towards faster shaping times (25 ns). The corresponding results were reported in the RICH upgrade technical design report (TDR) [28].

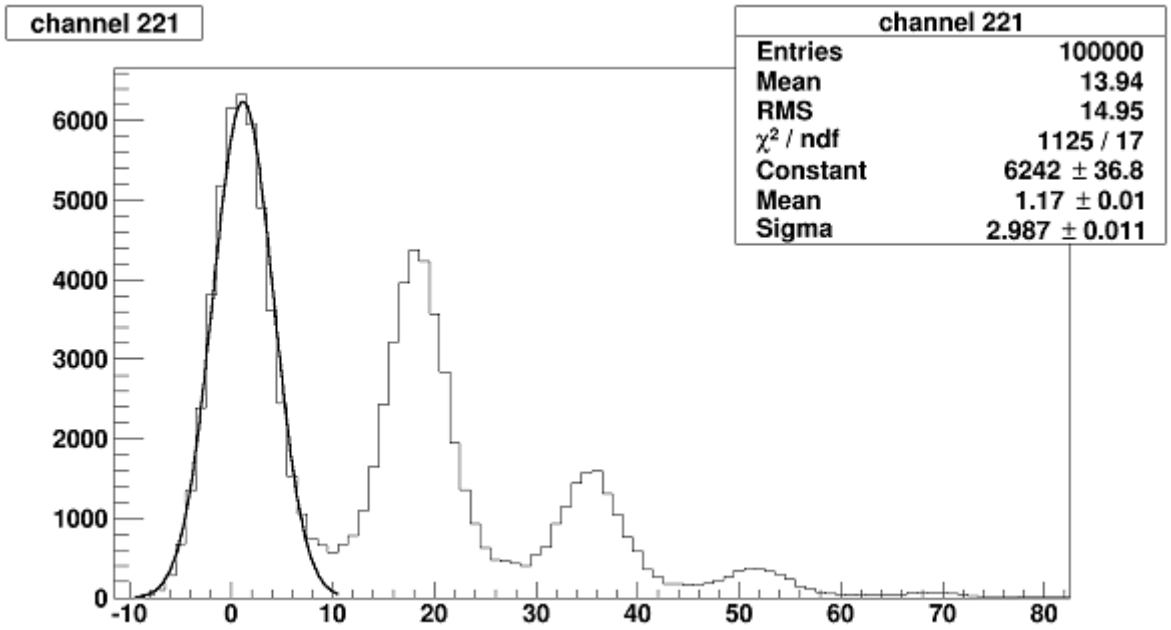


Figure 3.1.12: First photo-electron spectrum with a 50 ns shaping time

[3]O. Kazan(summer student) and R. Paluch(technical student)

## 3.2 Detailed noise measurements

Given the HPD low gain and the external readout, the electronic noise is the key point. The first phase of the project was devoted to understanding and investigating the various noise sources on the existing initial system. For these studies, all measurements were done without laser and with the following system configurations:

1. **DB** A standard DB without PA. It is used as reference.
2. **DB+PA+PCBN+ZIF** A standard DB with PA wire-bonded to the interface board (PCBN) populated with a ZIF socket.
3. **DB+PA+PCBN+ZIF+HPD** The previous system configuration 2 is connected to the ceramic carrier which is part of the anode of the HPD.
4. **DB+PA+PCBN+ZIF+HPD+HV** The previous system configuration 3 with high voltage (HV) on.

Figure 3.2.1 displays the results of the noise measurements for all four configurations. The noise figures include "default" common mode noise correction built in the Alibava code (see section 3.6).

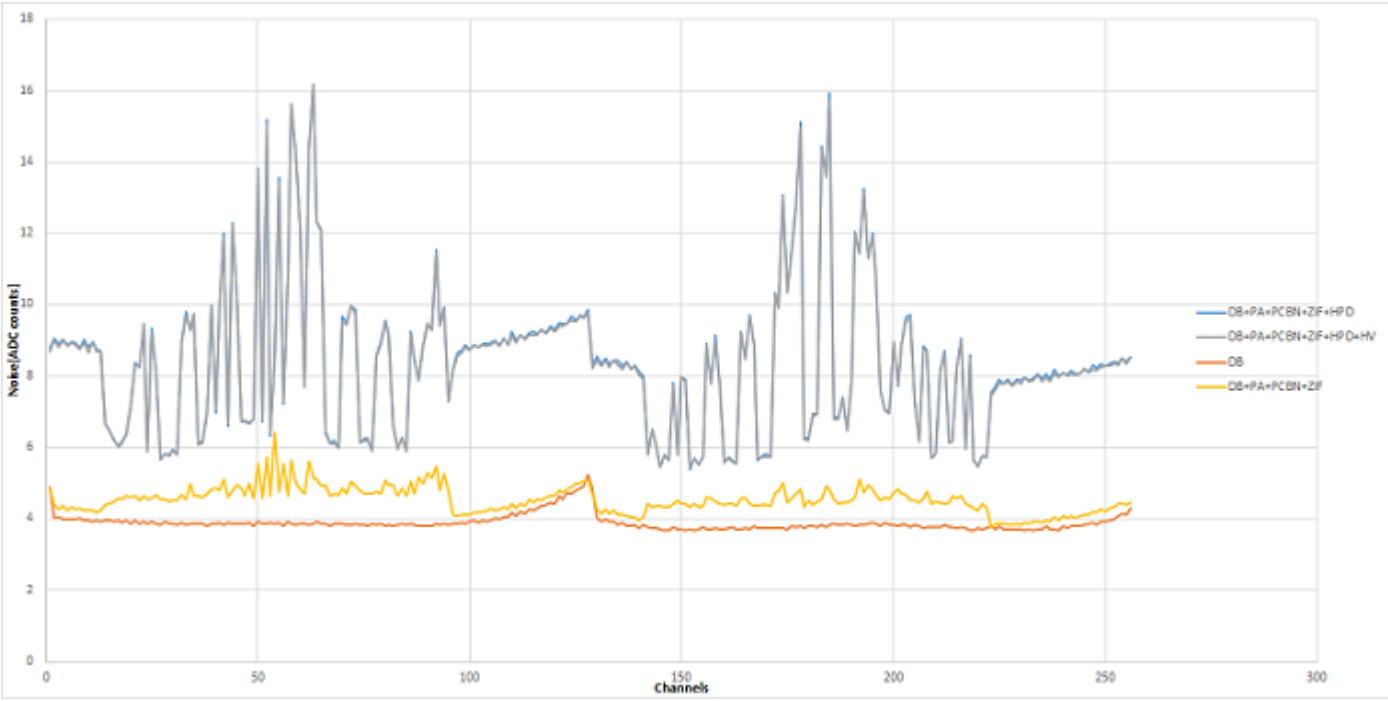


Figure 3.2.1: RMS noise values for various system configurations

The noise is expressed in analogue-to-digital converter (ADC) units that will be later converted in electrons using calibration facilities (charge injector) from the Beetle chips (see section 3.7). The noise measured from the reference DB itself (configuration 1) is low and uniform. The system with two boards not connected to the HPD (configuration 2) shows slightly larger noise values, in particular for the Beetle channels wire-bonded to the electronic board. When the system is fully connected (configurations 3 and 4), the noise tends to follow a pattern, with some hexels having very large noise values in comparison with the previous configurations. In these last configurations 3 and 4, no significant difference is seen (i.e. the noise contribution of the HV is marginal).

## 3.3 Routing line length and noise

The first attempt to understand the noise pattern observed in Figure 3.2.1 was to find a correlation between the length of the routing lines and the corresponding noise value.

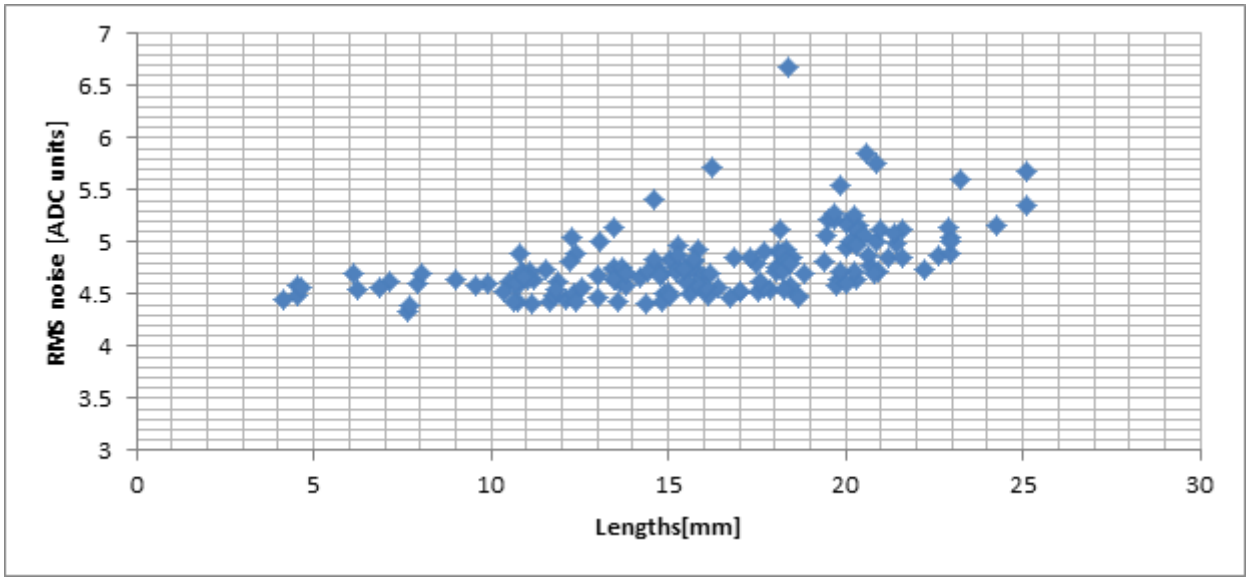


Figure 3.3.1: Noise in function of routing line lengths for each hexel, configuration 2

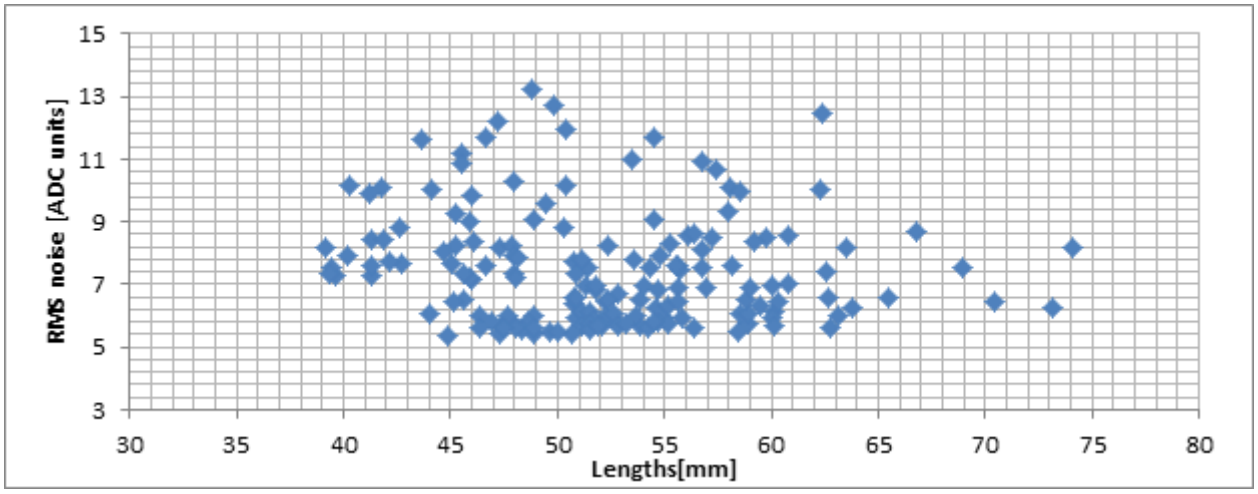


Figure 3.3.2: Noise in function of the lengths for each hexel, configuration 3

A correlation between routing line length and noise is observed for configuration 2, as shown in Figure 3.3.1. Once the system is connected to the EXTHPD (Figure 3.3.2), other effects take place and will be discussed specifically in Section 3.5.

| | PA+PCBN+ZIF[pF] | Carrier[pF] |
|---|---|---|
| Hexel 82 | 3.46 | 6.22 |
| Hexel 95 | 3.15 | 6.15 |
| Hexel 49 | 3.00 | 4.00 |

Table 3.1: Simulated capacitive loads (in pF) for hexels 82, 95 and 49

| | PA+PCBN+ZIF[$e^-$] | Carrier[$e^-$] |
|---|---|---|
| Hexel 82 | 227 | 464 |
| Hexel 95 | 192 | 463 |
| Hexel 49 | 253 | 367 |

Table 3.2: Measured RMS noise values (in $e^-$) for Hexels 82, 95 and 49

## 3.4 Capacitive load and noise

For a 25 ns peaking time, the Beetle noise follows the relation: $497e^- + (48.3e^-/\text{pF}) \times C_{in}$ where $C_{in}$ is the capacitive load at the channel input [33]. It is possible to calculate the amount of capacitive load added along the way up to the silicon sensor. There are two types of capacitive loads: backplane line capacitance and line-to-line capacitance. The first type is calculated using the formula $C = \epsilon_0 \epsilon_r \frac{A}{d}$ where $A$ is the line surface and $d$ is the distance from the line to a reference ground plane. The second type can be estimated using an on-line calculator[4].
The carrier manufacturer Kyocera provided simulated values for 2 routing lines. These values have been used to validate the estimates from the calculator. For line 95, the simulated value is 6.2pF and the calculated value is 6.15pF. The calculation was performed for the full routing path of the following 3 lines:

Hexel 82, the hexel illustrated in the RICH upgrade TDR [28].

Hexel 95, the hexel with information given by Kyocera.

Hexel 49, the hexel located on the carrier layer 3PA (see later).

The detailed calculation can be found in Appendix. The capacitive load estimates are summarized in Table 3.1. Table 3.2 displays the corresponding measured RMS noise values.
From these tables, it is seen that the capacitive loads and noise figures are similar. However, while hexels 82 and 95 show slightly larger noise values

[4]http://www.skottanselektronik.com/

when the HPD is connected (configurations 3 and 4), hexel 49 shows in this case a much larger noise level despite a similar capacitive load estimate. Section 3.5 investigates the reason for this difference. Section 3.6 explores the solution to this difference.

## 3.5 Noise contribution of the ceramic carrier

The second step in the understanding of the noise sources was the link between the large noise seen in Figure 3.2.1 (HPD connected - configurations 3 and 4) and the ceramic carrier design. A 2D view of the noise level in the 163 hexels is reproduced in Figure3.5.1 where the color code is proportional to the RMS noise level. A clear effect is observed when the system is connected to the HPD.

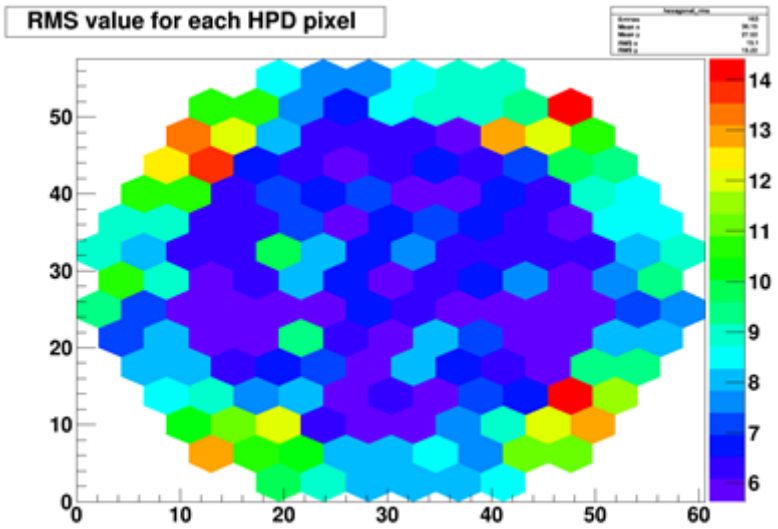


Figure 3.5.1: RMS noise in ADC units for each hexels, configuration 3

A much larger noise is measured on the peripheral hexels. All these hexels are routed out on carrier layer 3PA (Figure 3.5.2).

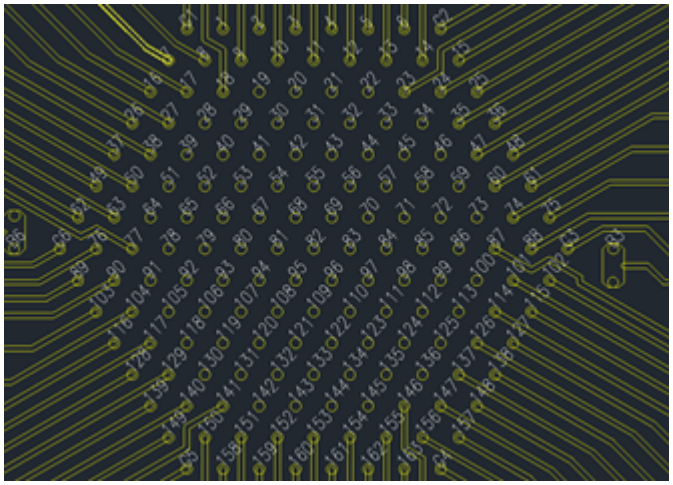

Figure 3.5.2: Layout of carrier layer 3PA, courtesy Kyocera

In the layer-stack view of the ceramic carrier (Figure 3.5.3), routing lines are located on layers 3PA, 4PA and 5PA. Layer 1PA is metallized (nickel-plated tungsten). The largest noise is observed on layer 3PA which is the closest to the metallisation of layer 1PA.

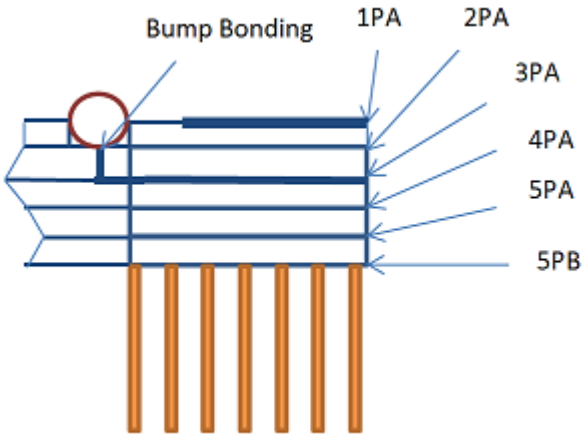


Figure 3.5.3: Layer stack of the ceramic carrier

This peripheral effect is also observed on all older BTeV tubes which share the same anode design and in particular the same ceramic carrier. To reproduce this effect, a bare ceramic carrier was made available from the HPD manufacturer. With this carrier, two additional tests have been performed:

The first test with the bare carrier simply inserted in the ZIF socket while the metallisation of layer 1PA is left floating.

The second test with the same bare carrier plugged in the ZIF socket and the metallisation of layer 1PA connected to ground (see Figure 3.5.4), as is the case with an HPD connected (configurations 3 and 4).

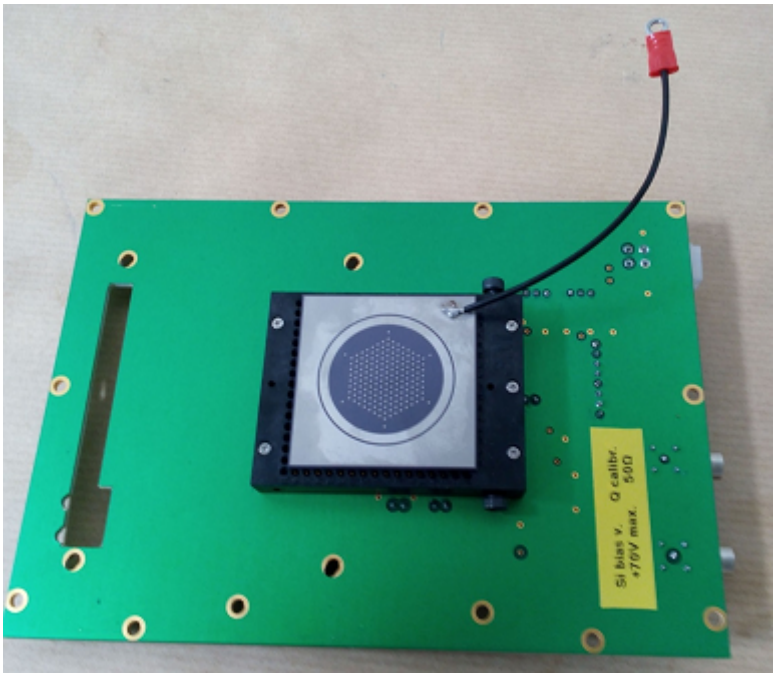


Figure 3.5.4: Bare carrier plugged in the ZIF socket for additional noise studies

Figures 3.5.5 and 3.5.6 illustrate the results of the two tests. The peripheral noise pattern is not visible when the carrier metallisation is floating (Figure 3.5.5, left plot). The peripheral pattern appears when the metallisation is connected to ground (Figure 3.5.5, right plot). The corresponding noise curves are reproduced in Figure 3.5.6 together with the noise curves of Figure 3.2.1.

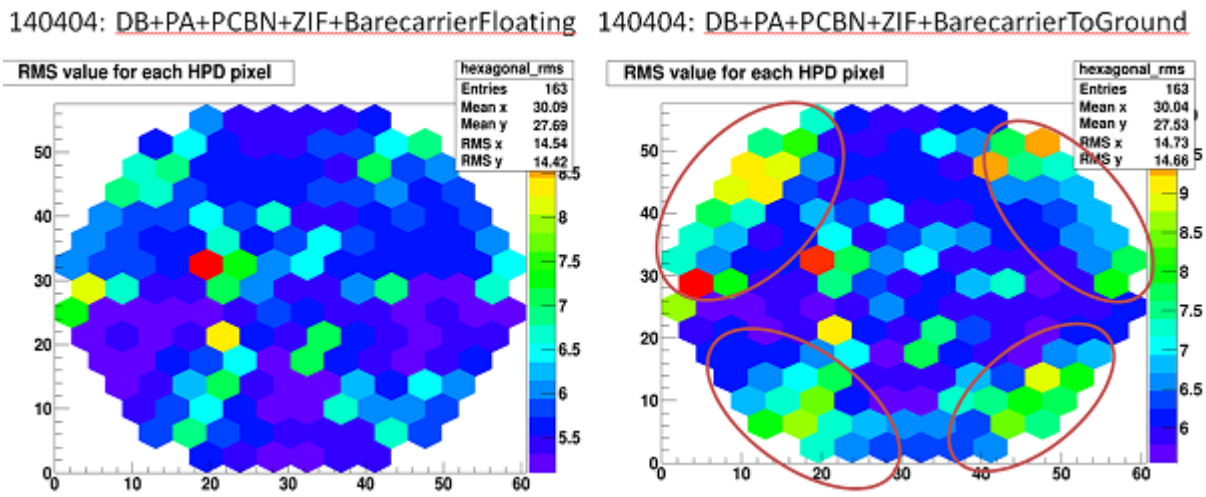


Figure 3.5.5: Noise pattern measured with bare carrier, top metallisation floating (left) or connected to ground (right)

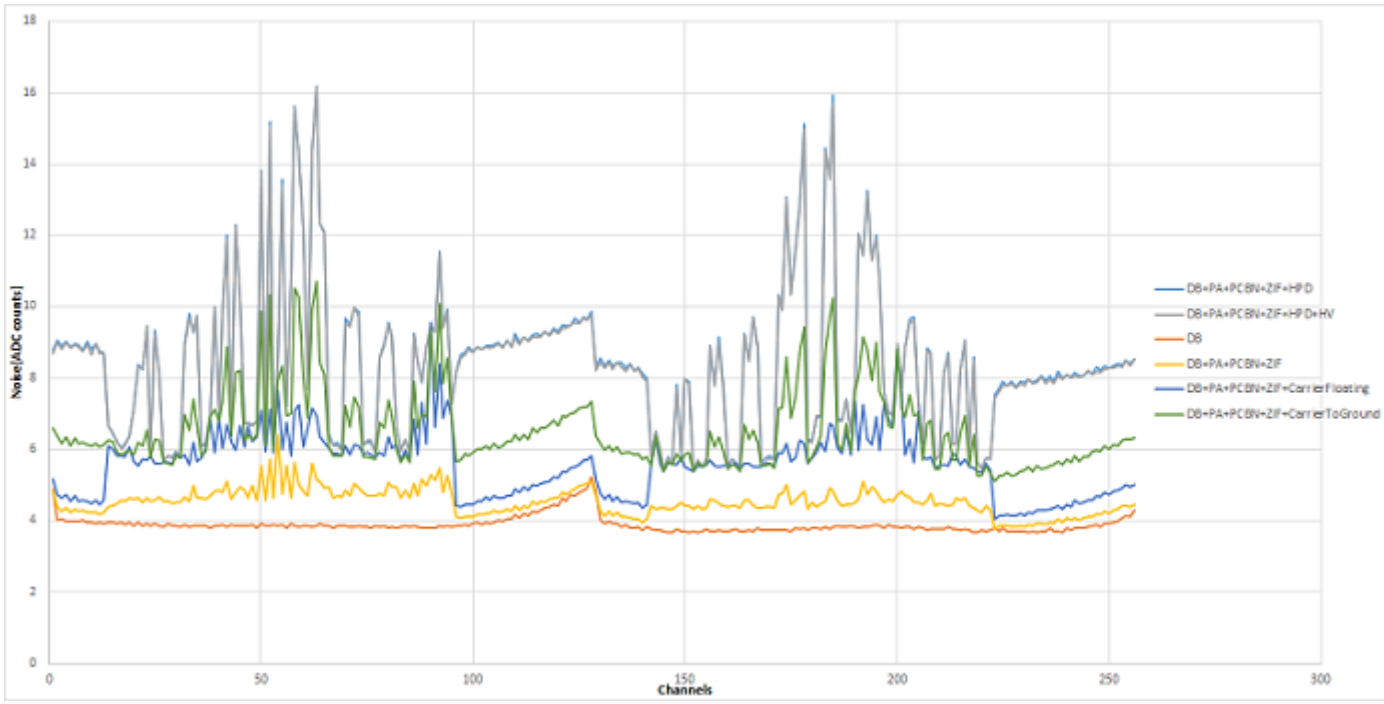


Figure 3.5.6: RMS noise values for various system configurations and bare carrier measurements

## 3.6 Common mode noise correction

To investigate this problem further, several hardware changes and tests have been done: changing ground cable length, system operated in complete darkness, measuring the influence of the silicon bias voltage and the Beetle parameters, etc. All these investigations are detailed in Appendix. On the off-line analysis side, the important step has been the understanding of the common mode noise correction. Common-mode noise is the noise common to a set or a subset of elements on an electrical pathway [42]. For example, a slight electrical surge in the power grid might push all the data values up for one event and down for the next.

By default, pedestal subtraction is performed on a per-channel basis, to normalise the values at about zero. The pedestal is calculated as follows: an average of the raw values is calculated for a particular channel over all events. For channel x, using N events, the pedestal is:

$$P_x = \frac{1}{N} \sum_{k=1}^{N} A_x^k \tag{3.1}$$

where $A_x^k$ is the raw data value for channel $x$ and event $k$. $P_x$ is the pedestal for channel $x$, a different pedestal is evaluated for each channel.

In the default common mode noise correction built in the Alibava system, the common mode noise for event k is calculated per Beetle chip using all 128 channels of that chip:

$$C^k = \frac{1}{n} \sum_{x=1}^{n} B_x^k \tag{3.2}$$

where $C^k$ is the common mode noise correction for all $n$ channels in a chip for event k and $B_x^k$ is the pedestal-subtracted data value for channel $x$ and event $k$[5]. In contrast to the pedestal calculation, where all events are averaged, the common mode noise changes for each event. This default common mode noise correction is adapted to silicon strips, which tend to behave rather uniformly in this respect.

Noise investigations in the EXTHPD have shown that a common mode noise correction *specifically* adapted to the ceramic carrier stratification was required. A specific common mode noise correction is calculated by grouping the channels per carrier layer:

[5]In reality, those channels affected by a real signal are excluded in the pedestal estimate and the common mode noise correction

$$C^{k,l} = \frac{1}{n_l} \sum_{x=1}^{n_l} B_x^{k,l} \tag{3.3}$$

where $C^{k,l}$ is the common mode noise correction for a block of $n_l$ channels in layer $l$ and $B_x^{k,l}$ is the pedestal-subtracted data value for channel $x$ of layer $l$ and event $k$.

The first attempt for a specific correction on the EXTHPD was realized with the software MathCad using raw data specifically from carrier layer 3PA. The result is visible in Figure 3.6.1. The corrected noise is more uniform and decreased by a factor of 2.

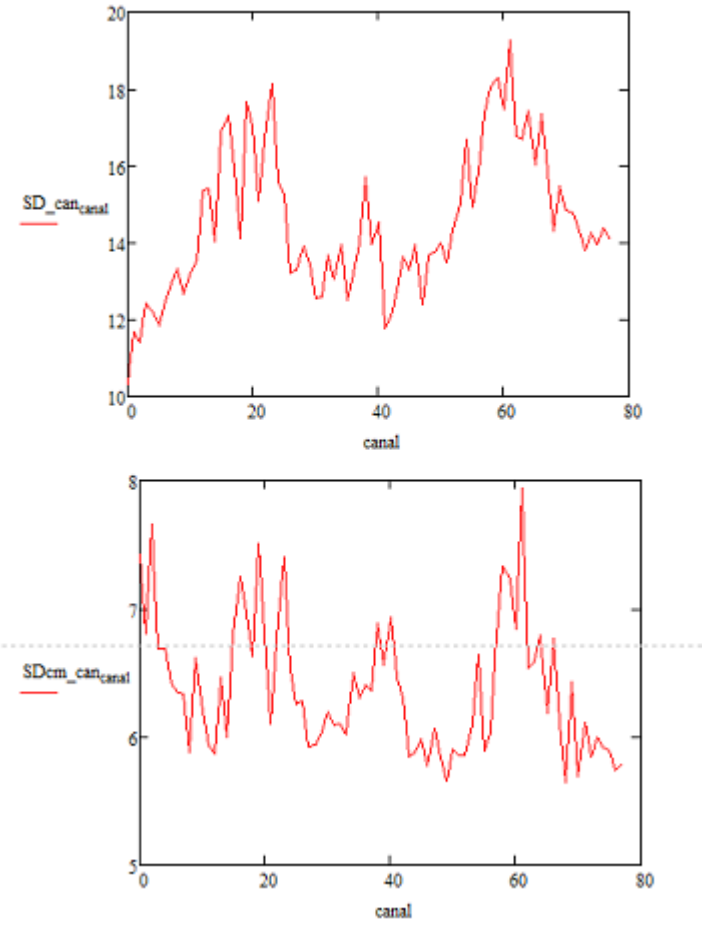


Figure 3.6.1: Layer 3PA noise values before (top plot) and after (bottom plot) specific common mode noise correction. The vertical scale is expressed in ADC units

When this specific common mode noise correction is performed for the full system, the noise levels are dramatically reduced, as illustrated in Figure 3.6.2.

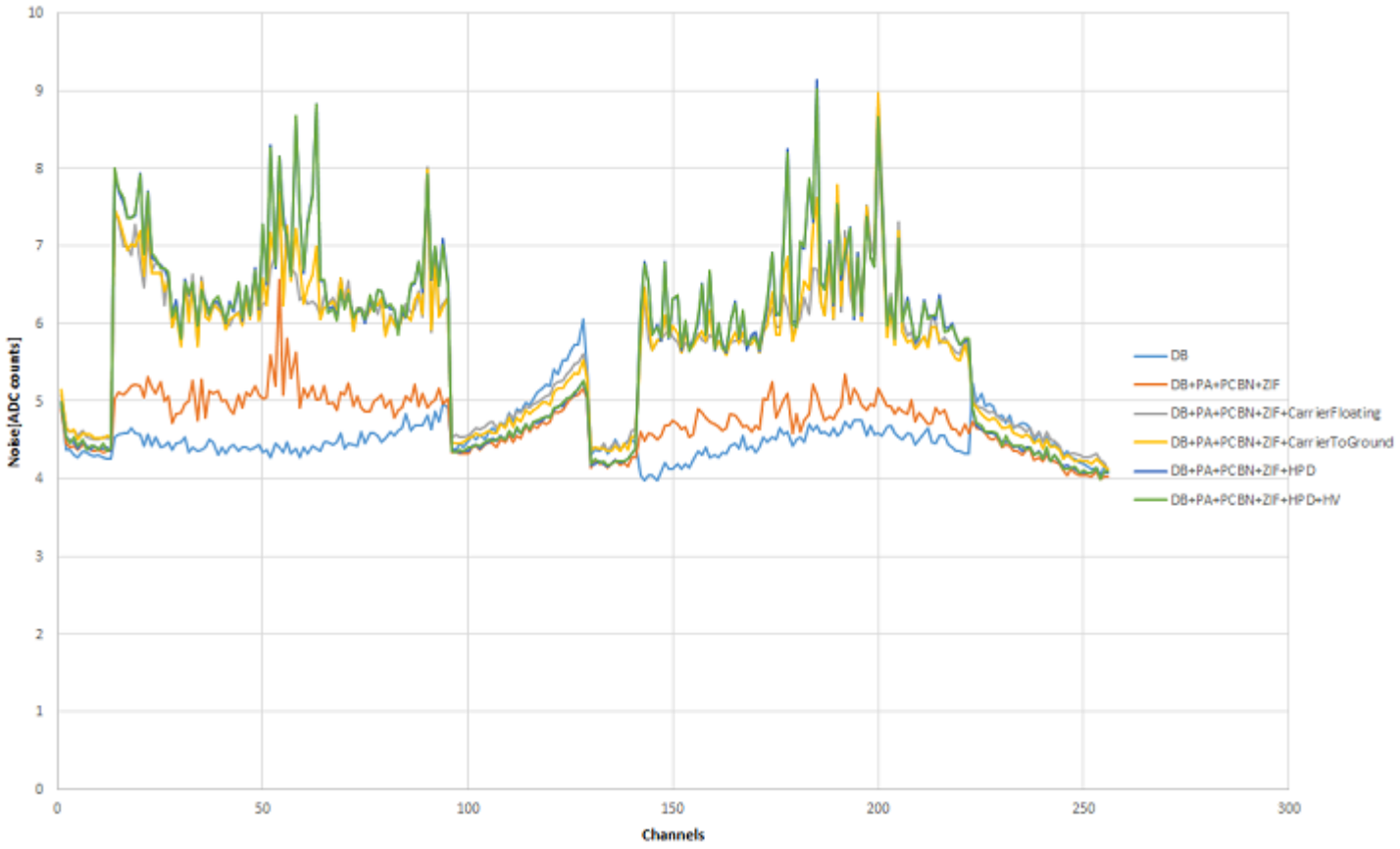


Figure 3.6.2: RMS noise values for each system configuration, after specific common mode noise correction

## 3.7 ADC units/electrons conversion

In order to translate ADC units in charge, a conversion is mandatory. The Alibava software provides a calibration mode that establishes a surface plot (Figure 3.7.1) with ADC units in function of the charge injected in each Beetle channel. From this plot, it is possible to extract the slope of the curve corresponding to the conversion factor.

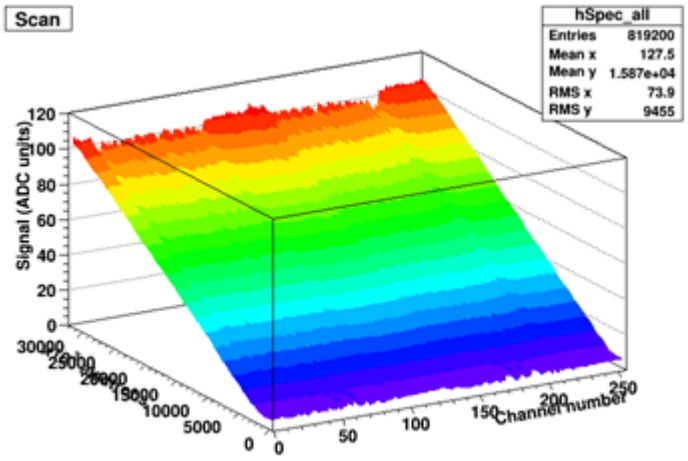


Figure 3.7.1: Calibration surface plot with x-axis:channel number y-axis:injected charge and z-axis:ADC units

As an example, and considering the photo-electron spectra of Figure(s)[], the RMS noise value in the pedestal is 6.209 ADC units equivalent to about $1290e^-$ (See Figure 3.7.2). The signal corresponding to the first photo-electron peak is 22.416 ADC units equivalent to about $4670e^-$ (see Figure 3.7.3). As expected from the Beetle noise levels, the separation between pedestal and first photo-electron peak is not optimal.

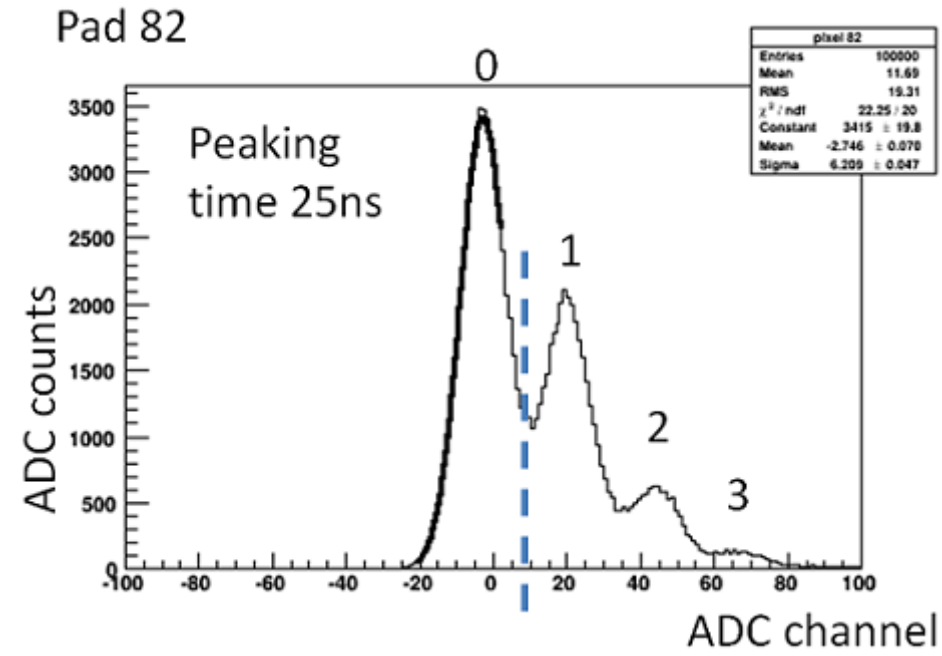


Figure 3.7.2: Photo-electron spectra with underlined pedestal, representing 6.2 ADC units translated in $1290e^-$

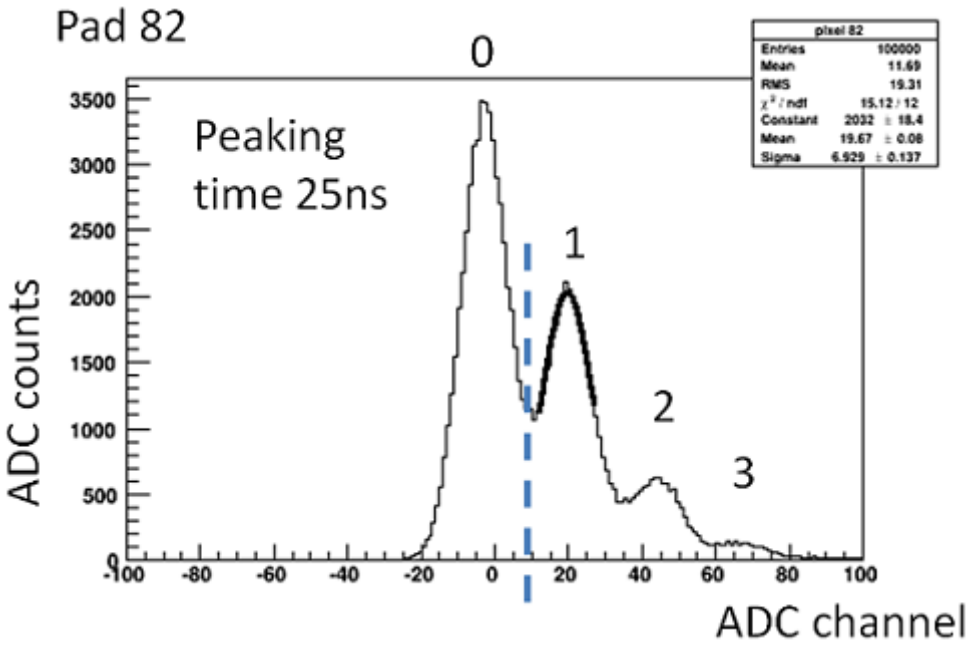


Figure 3.7.3: Photo-electron spectra with underlined first peak, representing 22.4 ADC units translated in $4670e^-$

## 3.8 Design and realisation of new electronic boards

The second phase of the project was devoted to the re-design of electronic boards. The new design must respect the mechanical architecture of the LHCb-RICH photon detector plane, especially the current HPD mounting part. Conceptually, the electrical design remains similar.

### HPD mounting support

In order to support the HPD in the RICH infrastructure, a aluminium mounting piece is mandatory. This piece is illustrated in Figure 3.8.1 and will be referred to as the "cup" in the following sections.

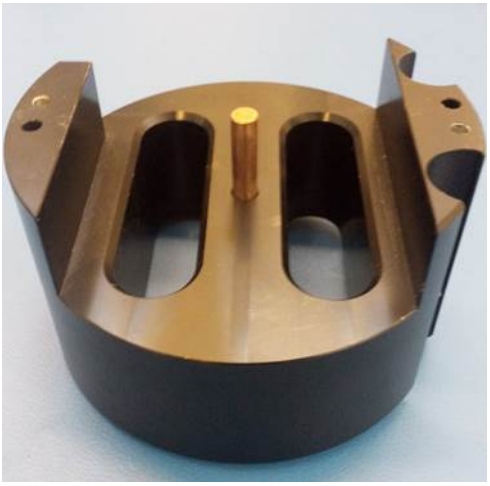

Figure 3.8.1: HPD mounting support

### Electronic board re-design

For the re-design of the boards, the two possible options were: a similar architecture with two smaller-size boards or a single smaller-size board which integrates all functionalities. The first option was preferred for the following two reasons:

**Cost** : a single board would reduce the trace length between silicon sensor and Beetle readout chips. However given that the noise mostly originates from the ceramic carrier and the Beetle chips, a single board would be too expensive, when taking into account design, development and production aspects for only a possible small improvement. Moreover a board containing components from the DB and interface board

with a size that respects the RICH architecture would be physically complicated to design.

**Proven concept** : the two-board concept was used for the previous initial version of the electronics. It gives the possibility to relocate some components and circuitry on other boards that would be connected whenever required. The basic design already exists, it only requires a physical re-design.

To fit in the HPD cup, a smaller-size DB should be re-designed by Alibava. In addition, the previous interface board design included a calibration circuitry that is not required during "normal" HPD operation (i.e. in the RICH detectors). This explained the actual size of that board. The first question was therefore to know precisely which components would be relocated on complementary boards. For normal HPD operation, the interface board itself requires only a few components: a filter for the silicon bias, decoupling capacitors and a Ball Grid Array[6] (BGA) footprint.

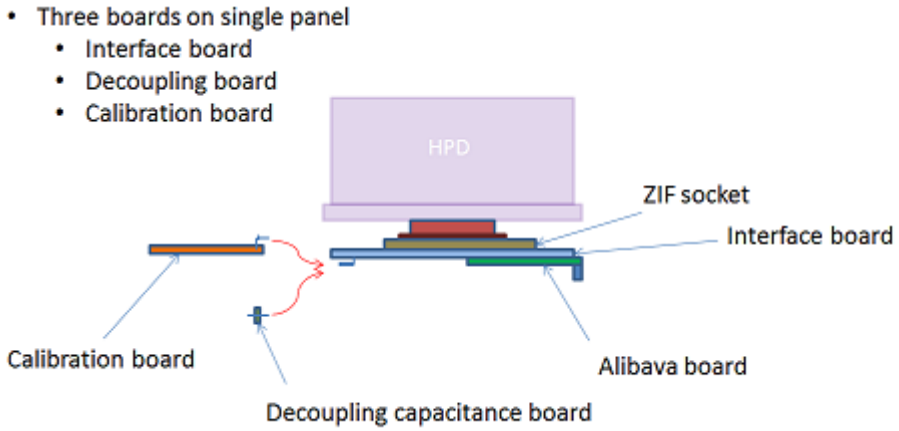


Figure 3.8.2: Concept drawing of the new boards

On the previous interface board, "jumpers" were used to connect the different parts of the circuit according to the desired use. The calibration system cannot be operated properly if decoupling capacitors are connected. Moreover, jumpers would take too much space on the new boards and inside the cup. Dimensional constraints limit the board dimensions to a 80 mm length and a 55 mm width. The previous interface board was 160 mm in length and 110 mm in width. The solution chosen consists of four boards as follows:

[6]Type of surface-mount packaging, using solder balls instead of pins as for a PGA.

**Custom DB** measures 40 mm×55 mm, includes previous DB components with the exception of the input connector for the detector bias. This board has been re-designed and manufactured by Alibava.

**Interface board** measures 74 mm×55 mm, includes a filter and a LEMO connector for the detector bias, BGA/bonding pads and a connector with 12 pins. This connector allows connection and mechanical support with one of the two other boards that follow.

**Decoupling capacitance board** measures 3.4 mm×35 mm and contains only six decoupling capacitors. It is tiny because this board will be connected to the interface board in normal HPD use. Its pinout is designed to be symmetrically reversible on the 12-pin interface board connector.

**Calibration board** measures 55 mm×40 mm and is also designed to be symmetrically reversible. This board will be only used for laboratory purposes and therefore has less dimensional restrictions. Particular attention was given to the placement of the various input/output components.

All boards were designed with 4 layers so that they can all be placed on the same panel when manufactured to minimise cost. The thickness of the boards is the standard 1.6 mm with a stratification as follows:

**Top layer** contains routing lines from 0.1 mm to 0.5 mm in width. Near to wire-bonding pads, the line width is reduced to 0.1 mm because of the required density. Otherwise a line width of 0.5 mm is used.

**First internal layer** is separated by 0.1 mm of FR-4 from the top layer. It is used whenever crossing of lines is inevitable. This layer mainly concerns the calibration board.

**Second internal layer** is separated from the first layer by 1.2 mm of FR-4. This layer is used to distribute the voltage supply, especially for the decoupling board and 6 pins of the BGA on the interface board.

**Bottom layer** is mostly reserved for ground planes, with the exception of routing lines between BGA to vias (through holes) which bring signals to the top layer.

### 3.8.1 Interface board

The front view of the re-designed interface board is reproduced on Figure 3.8.3. On the right-hand side, the 4 mounting holes for the re-designed DB are visible. They have been made larger with 3 mm diameter compared to the 2.5 mm diameter for the daughter board, to allow for some mechanical adjustment with respect to the wire bonding.

On the left-hand side, the detector bias voltage is supplied through a straight LEMO connector. This bias is filtered and routed to the second internal layer.

Wire-bonding pads were made identical to those on the previous interface board. They each measure 1 mm $\times$ 0.1 mm and are spaced by 0.06 mm. The pad location was discussed very early in the development of the boards with people in charge of the wire-bonding at CERN[7]. Considering the placement of a 0.5 mm spacer between DB and interface board to prevent any short circuit, the appropriate distance between the axis of the bonding pad layout and the edge of the pitch adapter is 3.5 mm.

The other important change is the use of a BGA adapter instead of a ZIF socket. The BGA footprint allows the routing lines to be placed more freely on the overall surface. In this way, the number of blind vias is dramatically reduced, because they can be replaced by through holes. Determined by High Density interconnect (HDI) design rules, the dimension of these holes is 0.3 mm [43].

[7] Ian McGill

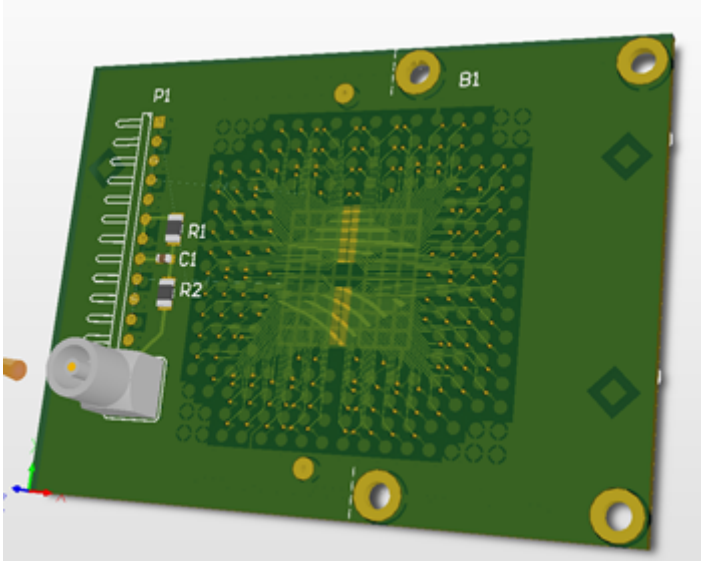


Figure 3.8.3: Front view of the new interface board

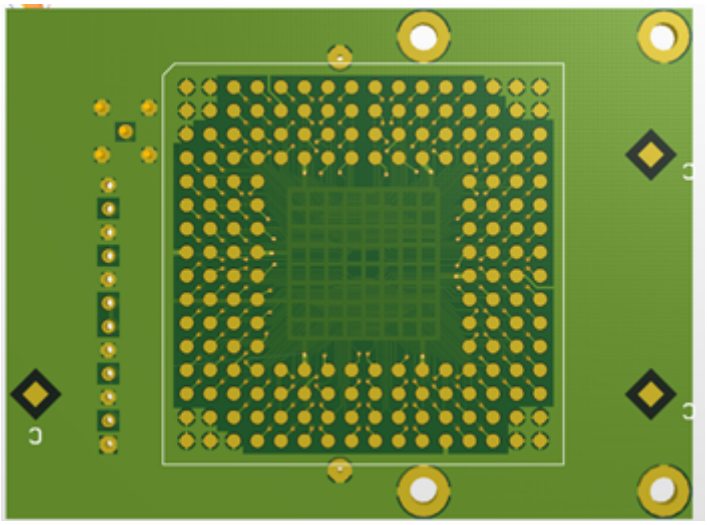

Figure 3.8.4: Rear view of the new interface board

The rear view of the new interface board (Figure 3.8.4) shows the BGA footprints. Are also visible, the 3 rhombus (fiducial marks) which allow the positioning of the BGA soldering machine. These marks were introduced after a discussion with the soldering department, since the BGA was delivered with no solder balls. Three conditions need to be fulfilled to ensure appropriate BGA soldering:

**1** The BGA matrix and its pins should withstand oven treatment at 260 °C

for 10 seconds.

**2** At least 3 fiducial marks should be placed on the panel to help the BGA soldering machine with the placement and the orientation during the process.

**3** A 5 mm free space left on the board edges to clamp the boards during the assembly process. This last condition was satisfied by the panel configuration.

### 3.8.2 Decoupling capacitance board

This board is designed with 6 surface-mounted decoupling capacitors of 1nF each. Its size has been reduced as much as possible since the board is connected in normal HPD use and should fit within the cup dimensions.

Figure 3.8.5: Decoupling capacitance board

### 3.8.3 Calibration board

Except for the components required for filtering and decoupling, all other components removed from the previous interface board are placed on this board (Figure 3.8.6). The calibration signal from the detector bias line is input to a low-noise charge pre-amplifier[8] (LNA). The output of this LNA is connected to the non-inverted pin of a BiMOS amplifier and the output of

[8]PR304 from Eurorad

this amplifier is connected to a straight LEMO connector labelled "calibration out".

The supply voltage of the LNA is ±12V and brought through a 2×2 Molex connector. These ±12V are also used to provide supply for the amplifier for which voltages are regulated to ±5V.

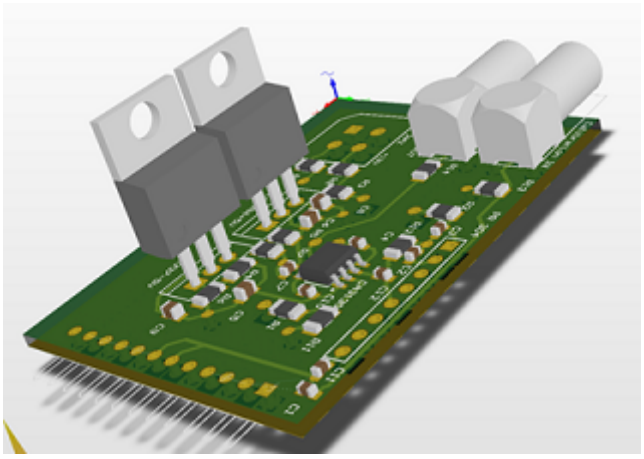

Figure 3.8.6: Calibration board

The LNA input is located as close as possible to the connector, in order to prevent the LNA output line to cross the input line and to avoid loops. High-value electrolytic capacitors have been placed near the regulators for filtering. Ceramic capacitors were placed close to the amplifier to improve the behaviour in pulsed regime.

### 3.8.4 Mechanical compatibility

In order to thoroughly check the new front-end electronics, the whole system was designed in Autocad[9]. This allowed to visualise the different possibilities regarding the positioning of components. The cup is visible in green, the interface board in white, the BGA footprint in red and the ZIF socket in purple.

[9]Drawing initiated by T. Gys

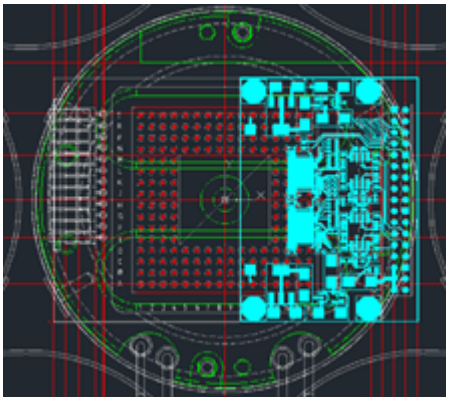

Figure 3.8.7: Mechanical drawing (rear view) of the re-designed front-end electronics

This drawing ensured that no conflict would appear between the cup and the boards, especially while connecting the decoupling board. To avoid any issue, the decoupling capacitance board was placed at the edge of the interface board with a straight connector.

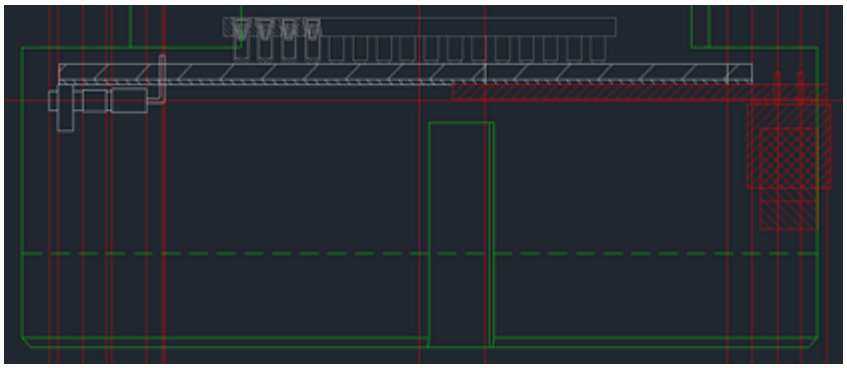

Figure 3.8.8: Mechanical drawing (side view) of the re-designed front-end electronics

# Chapter 4

# Beam tests

### 4.0.5 Preparation of the setup

After thorough qualification of the new front-end electronic boards in the laboratory, the full system was tested in a real environment. Beam tests correspond to time slots dedicated to tests in a particle beam. In the context of the LHCb-RICH upgrade, two sessions were scheduled in the SPS (see 1.1). The EXTHPD system was tested in the second session at the end of November 2014 using a dedicated RICH-Upgrade test box (Figure 4.0.1). The box contains an optical lens which generates and images a Cherenkov light cone as a ring onto the photon detectors (Figure 4.0.2).

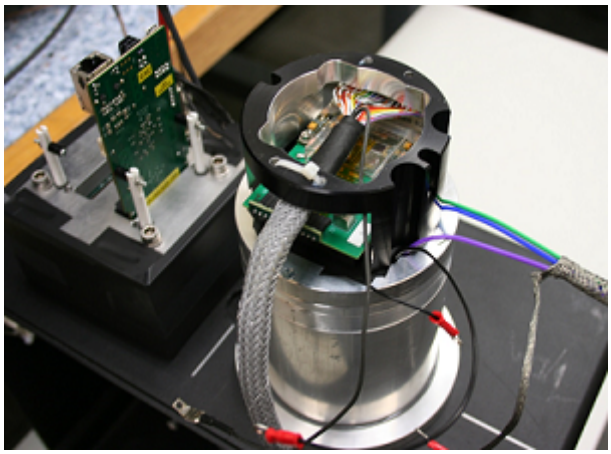

Figure 4.0.1: RICH-upgrade beam test box with one EXTHPD on the right and MaPMTs on the left

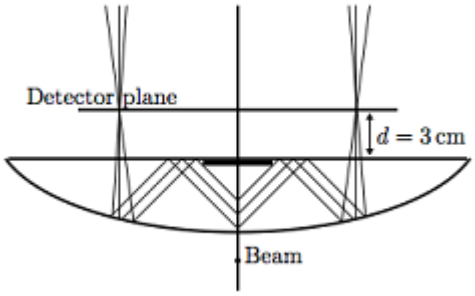


Figure 4.0.2: Schematic drawing of the optical lens (courtesy of J.He)

The box was initially prepared and used to test MaPMTs with two sets of electronic boards to detect the Cherenkov ring. One of the two sides has been adapted for the EXTHPD to work with both photon detector types simultaneously (Figure 4.0.3). Due to the HPD mu-metal[1] shield the photocathode is not located in the lens focal plane but 26 mm away.[2]

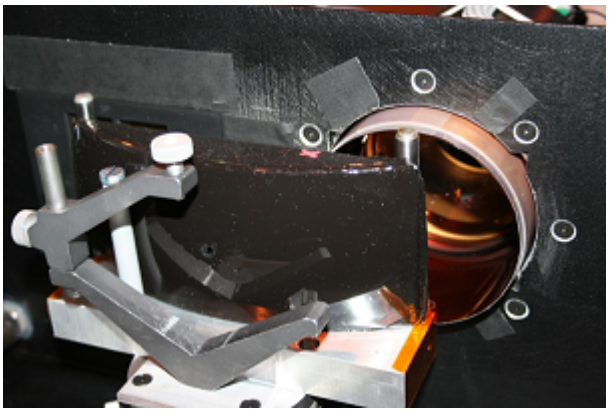

Figure 4.0.3: Optical lens inside the test-box

In the laboratory, the Alibava system generates the signal that triggers the pulsed laser. In beam tests, the signal generated by the passage of a particle in scintillators is used to trigger externally the HPD readout electronics.

[1] Nickel, cobalt and iron alloy.

[2] The lens position has been inadvertently offset laterally by 8 mm towards the Salève side. In the beam test facilities at the SPS and considering the beam direction, the Monts-Jura are on the left and Mont Saleve on the right.

### 4.0.6 Results

Part of the Cherenkov ring has been successfully detected as illustrated in Figure 4.0.4. The color code in each hexel is proportional to the average number of Cherenkov photons detected in that hexel.

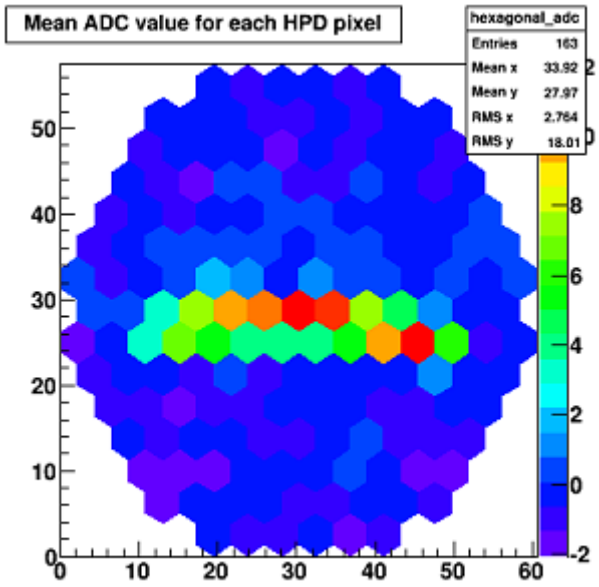


Figure 4.0.4: ADC value for each HPD pixel.

The photo-electron spectrum recorded in hexel 83 is illustrated in Figure 4.0.5. A detailed analysis of the test beam data is on-going.

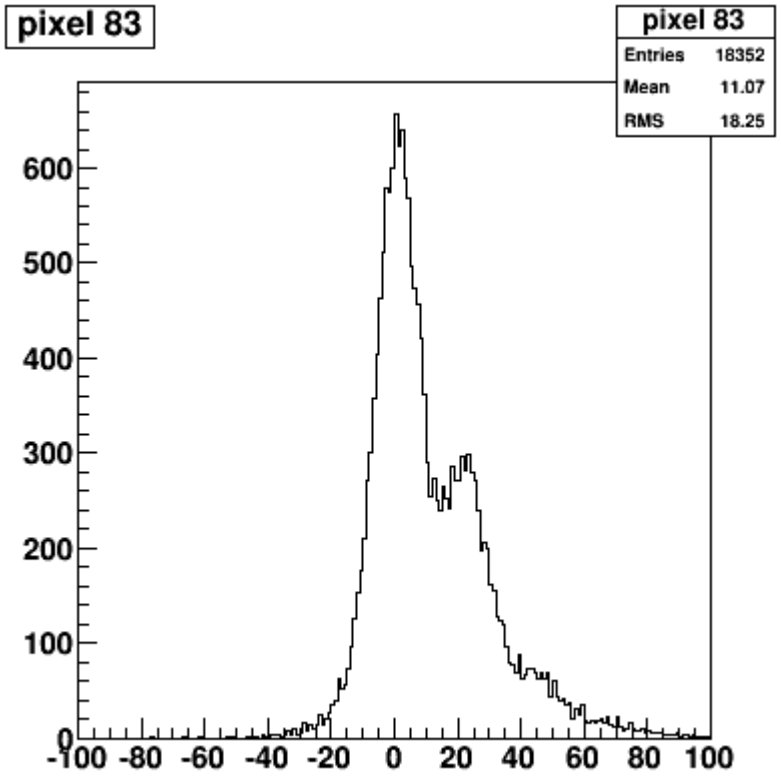


Figure 4.0.5: Photoelectron spectrum of the hexel 83.

# Summary and conclusion

This master thesis covered a R&D phase to investigate the concept of an HPD tube with external readout electronics. It required first an extensive study of the initial electronics system especially on noise aspects. The second phase of the project involved the development of new front-end electronic boards that were in a third phase successfully tested in a particle beam.

The pixel-HPDs currently installed in the LHCb Cherenkov detectors encapsulate readout electronics in the vacuum tube envelope. The LHCb upgrade and the new trigger system will require the replacement of all pixel-HPDs with new photon detectors. The new baseline photon detector candidate is the multi-anode photomultiplier. An HPD with external readout is investigated as a backup photon detector option.

Given the low signal (typ. $5000e^{-}$) created for each photo-electron hit in an HPD, the key point is the electronic noise. The first priority was consequently to understand and identify the noise sources with an external readout configuration. This study underlined the noise contribution from the Beetle chip used as front-end readout ASIC and also the noise contribution from the HPD ceramic carrier.

The second phase of the project was dedicated to re-designing new front-end electronic boards to make them fully compatible with the existing LHCb-RICH infrastructure. During this phase, the two-board approach was kept with the development of a new custom daughter board and a new interface board and complementary boards.

The new electronic readout system was successfully tested in a real particle beam environment. It validated the proof-of-concept and demonstrated its feasibility and potential.

In the future, improving the signal-to-noise ratio implies the design and development of a readout chip with lower noise and a re-design of the HPD ceramic carrier.

# Appendix

## Additional information about HPD

**Photo-cathode** is an S20 type (semi-transparent Sb$Na_2$KCs), deposited on the inside surface of a 7 mm-thick fused-silica window [44]. When an incoming photon hits the photo-cathode, the absorbed energy causes electron emission through the photoelectric effect. The photo-electron created is accelerated by a high supplied voltage of 20 kV.

**Solid-state** for the anode part of the HPD. The accelerated photo-electron is electro-statically focused (with a demagnification factor of around five [45]), hits a reverse-biased silicon detector where it dissipates all its kinetic energy.

When a photo-electron loses energy in silicon, it creates electron-hole pairs at an average yield of one for every 3.6 eV of deposited energy. It results in the creation of 5000 pairs released in the silicon [17].

### Inside silicon structure

The hereby used semiconductor (Figure 4.0.6) is n doped by two implants located at the top and bottom edges, respectively n+ and p+. The n+ implant (photo-electron side) forms the ohmic contact. The p+ implants allow the establishment of PN junctions.

A particle passing through the depletion zone will generate free carriers - electron-hole pairs. The depletion region is a space without free carriers forming a capacitor where the electrodes are the p and n areas and the depletion area is the dielectric.

Potential formed by the p-n junction is however not sufficient to create an electric field capable of directing all the free carriers to the electrodes. There are recombination occurring and therefore the collection of carriers is not

complete.

However the size of the depletion zone and the strength of the electric field may be increased if an opposite difference of external potential is applied. Collection holders will be more effective and the useful area will be larger [46].

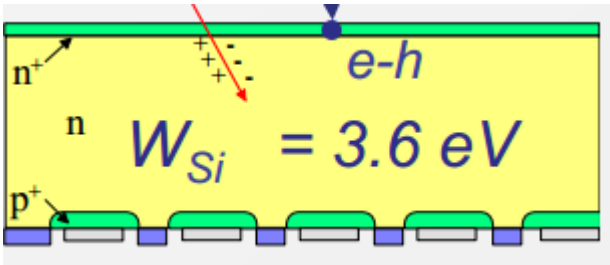


Figure 4.0.6: HPD'silicon sensor inside structure[21].

## Focus on the triggering of LHCb

The bunch-crossing rate of the LHC is currently at 40MHz, but in the LHCb experiment the accepted event rate is currently at 1MHz. It comes from the first level trigger called "Level 0" implemented in hardware which uses calorimeter and muon detector signals to have a preliminary idea of the primary vertices and thus reduce the accepted event rate.

There are two more level of triggering that are software running on a large farm of CPUs. The first level of software trigger uses information from VELO, silicon tracker and a summary from the Level 0 trigger (Figure 4.0.7).

The Level 1 trigger reconstructs primary vertices and the impact parameters of tracks to these vertices. The rate is reduced to 40 kHz at this stage. The trigger algorithm has a maximum running time because it requires all data to be stored during the execution and thus is limited by the buffer size in the front-end electronics (which corresponds to 58 ms).

Complete detector data, including RICH data, are read and fed into the second level trigger software called "High Level Trigger" as soon as an event is accepted. Precise measurements of the impact parameters, repeating and improving the algorithm used at the preceding level, are obtained using complete tracking information. The accepted rate of events is reduced to 10kHz

at which a more exclusive selection starts. Only 2kHz are finally recorded to tape and 200Hz are promptly reconstructed and made available for immediate analysis [47].

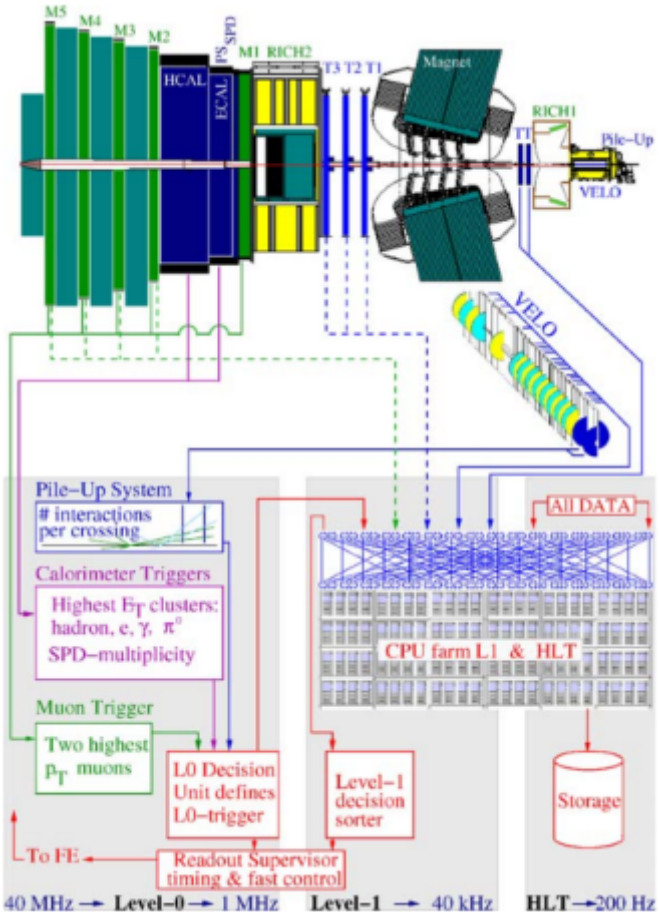


Figure 4.0.7: LHCb current trigger system [47].

## Closer look at the Level 0 trigger system

In order to control different front-end implementations with an unified interface and a predictable behaviour the Timing and Trigger Control (TTC) system has been established. It aims to distribute all time-critical signals to the front-end electronics.

The Level 0 trigger latency has been set to 4.0μs as a compromise between the cost and complexity of the front-end pipeline buffers and the processing

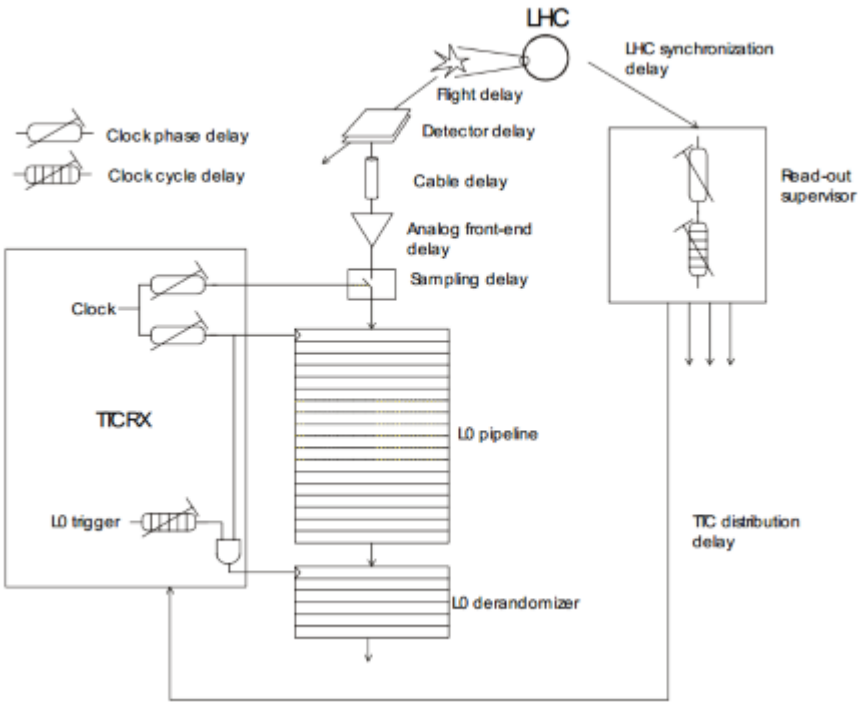


Figure 4.0.8: Bunch crossing synchronisation of front-end [48].

time (plus signal collection and distribution) available for the L0 trigger system. The L0 latency is defined as the maximum delay from the actual bunch crossings to the L0 trigger decision arrives to the output of the L0 pipeline buffer in any sub-detector [48].

In the RICH pixel readout electronics, 8 pixel cells included in one larger pixel will combine hit information from 8 front-end stages using OR-logic. There are 16 delay units within these 8 pixels. Each unit can delay a single hit for a period of time which can be set to math the trigger latency. Data is stored in a de-randomizing buffer (see Figure 4.0.8) implemented as a FIFO memory with a 16-event capacity. The number of columns (32) is common to the global LHCb architecture. The readout speed of 32 channels from a chip corresponds to  900 ns, which includes 32 parallel lines with 25 ns and data headers [44].

## Upgrade of the LHCb trigger system

The upgraded LHCb trigger system will contain exclusively software-based triggering. A throttling mechanism will be designed to control the data flow

into the data acquisition as illustrated Figure 4.0.9.

The front-end electronics will be upgraded to allow reading events at the LHC clock rate. In principle the upgrade should allow to perform data acquisition and event building on the event filter farm at the full rate of 40 MHz [27].

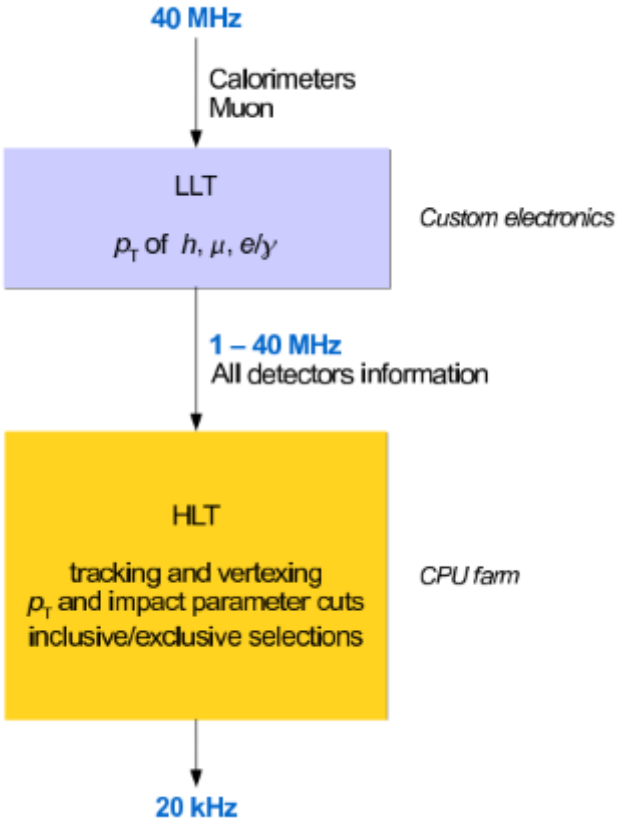


Figure 4.0.9: LHCb upgraded trigger system [27].

# Capacitance calculation

## Routing line 95

The first part of routing line 95 is located on carrier layer 5PA with a length of 18.72 mm. The line then migrates to layer 4PA with a length of 7.76 mm. On layer 5PA, line 95 is running over a distance of 9.43 mm opposite to

line 118 located on layer 4PA. The calculation for the backplane line capacitance gives: Co = 130.29 pF/m for layer 5PA. The line-to-line capacitance: 242.69 pF/m. For layer 4: Co = 153 pF/m. The contribution from adjacent lines is not included as their are distant by 0.495 mm or more.

### Routing line 82

The first part of routing line 82 is located on carrier layer 5PA, with a length of 12.14 mm. It then migrates to layer 4PA with a length of 10.3 mm. In layer 5PA, vias are ignored because their distance from line 82 is larger than 0.3 mm. On layer 5PA, line 82 is running over a distance of 5.84 mm opposite to line 79 located on layer 4PA. The calculation for the backplane line capacitance gives: Co = 130.29 pF/m. The line-to-line capacitance: 272.12 pF/m.

For layer 4: Co = 153 pF/m. Tracks of layer 3 are superimposed : 76, 89 and 90 totalling 2.46 mm that will add a contribution of 1.55 pF.

### Routing line 45

The start of routing line 45 is located on carrier layer 3PA with a length of 14.62 mm. The calculation for the backplane line capacitance gives: Co = 182 pF/m. The line-to-line capacitance: 231.87 pF/m.

## Influence of the light

In order to check if ambient light can affect the Beetle chip operation, the following 3 tests have been carried out using the reference DB:

DB operated without protecting cover.

DB top surface covered with opaque material.

DB completely surrounded with opaque material.

The results are visible in Figure 4.0.10 and show a small but clear effect. It is consequently recommended to cover the DB with opaque material.

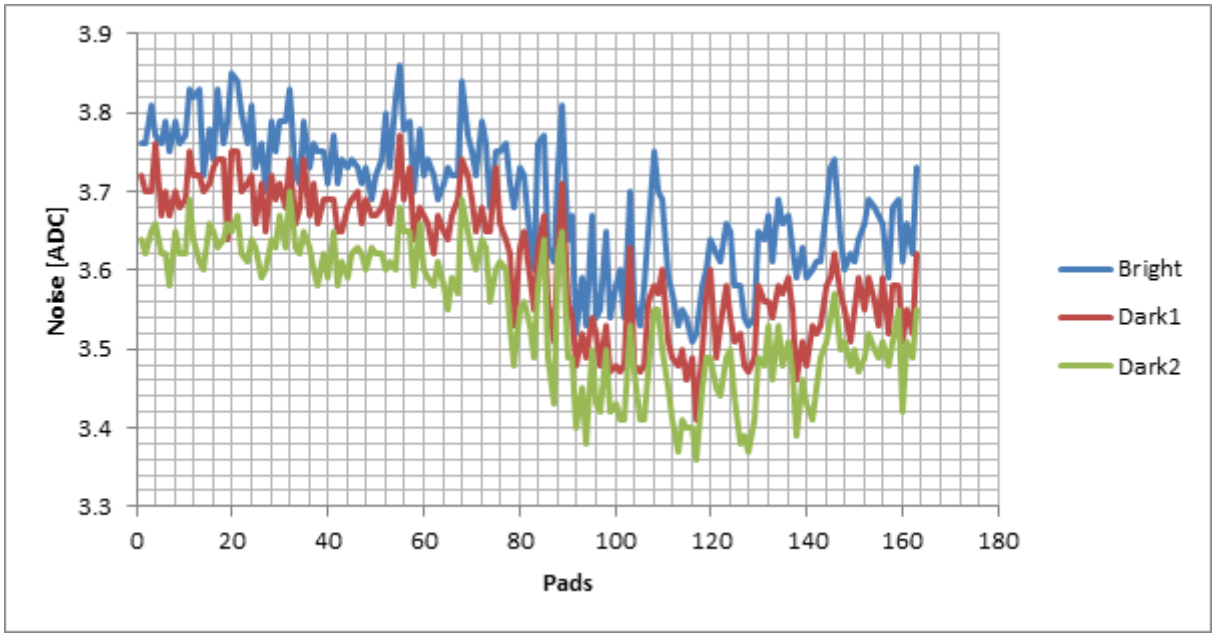


Figure 4.0.10: Influence of the light on the measurements.

## Influence of the main Beetle chip parameters

In this section, the most significant Beetle chip parameters will be presented. These parameters correspond to internal registers that tune elements inside the Beetle chip. The internal Beetle architecture is reproduced in Figure 3.1.3 (Section 3.1).

The table reproduced in Figure 4.0.11 summarizes the allowed range for each parameter. The physical value is the register value multiplied by the least significant bit (LSB). In the following, rather than the physical values, the register values will be used: they are easier to manipulate and are input in this format to the Beetle chip.

| Reg. no. | Reg. Name | Range | Res. of LSB | Nominal Setting Value | Nominal Setting Reg. content | Description |
|---|---|---|---|---|---|---|
| 0 | *Itp* | 0 - 2 mA | 7.8 µA | 0 µA | 0x00 | test pulse bias current |
| 1 | *Ipre* | 0 - 2 mA | 7.8 µA | 600 µA | 0x4C | preamplifier bias current |
| 2 | *Isha* | 0 - 2 mA | 7.8 µA | 80 µA | 0x0A | shaper bias current |
| 3 | *Ibuf* | 0 - 2 mA | 7.8 µA | 80 µA | 0x0A | front-end buffer bias current |
| 4 | *Vfp* | 0 - 2.5 V | 9.8 mV | 0 mV | 0x00 | preamplifier feedback voltage |
| 5 | *Vfs* | 0 - 2.5 V | 9.8 mV | 0 mV | 0x00 | shaper feedback voltage |
| 6 | *Icomp* | 0 - 2 mA | 7.8 µA | 40 µA | 0x05 | comparator bias current |
| 7 | *Ithdelta* | 0 - 2 mA | 7.8 µA | — | — | current defining incremental comparator threshold |
| 8 | *Ithmain* | 0 - 2 mA | 7.8 µA | — | — | current defining common comparator threshold |
| 9 | *Vrc* | 0 - 1.25 V | 4.9 mV | 0 mV | 0x00 | comparator RC time constant |
| 10 | *Ipipe* | 0 - 2 mA | 7.8 µA | 100 µA | 0x0D | pipeamp bias current |
| 11 | *Vd* | 0 - 2.5 V | 9.8 mV | 1 275 mV | 0x82 | pipeamp reset potential |
| 12 | *Vdcl* | 0 - 2.5 V | 9.8 mV | 1 030 mV | 0x69 | pipeamp reference voltage |
| 13 | *Ivoltbuf* | 0 - 2 mA | 7.8 µA | 160 µA | 0x14 | pipeamp buffer bias current |
| 14 | *Isf* | 0 - 2 mA | 7.8 µA | 200 µA | 0x1A | multiplexer buffer bias current |
| 15 | *Icurrbuf* | 0 - 2 mA | 7.8 µA | 800 µA | 0x66 | output buffer bias current |
| 16 | *Latency* | 10 - 160 | — | 160 | 0xA0 | trigger latency |
| 17 | *ROCtrl* | — | — | cf. table 11 | | readout control |
| 18 | *RclkDiv* | 0 - 255 | — | 0 | 0x00 | ratio between `Rclk` and `Sclk` |
| 19 | *CompCtrl* | — | — | cf. table 12 | | comparator control |
| 20 | *CompChTh* | 0 - 31 | — | — | — | comparator channel threshold shift register implementation and *Beetle* revision Id. (cf. table 13) |
| 21 | *CompMask* | — | — | 0 | 0x00 | comparator mask shift register implementation |
| 22 | *TpSelect* | — | — | 0 | 0x00 | test pulse selection shift register implementation |
| 23 | *SEUcounts* | 0 - 255 | — | — | — | sum of Single Event Upsets |

Figure 4.0.11: Beetle's default registers values [35].

The influence of two key parameters will be illustrated below using the "Laser Synchronisation" mode proposed by the Alibava interface. This mode allows to reconstruct the Beetle output pulse shape over a specified time range.

## Voltage feedback shaper

The voltage feedback shaper (VFS) registry controls the voltage that sets the shaper feedback resistor. The shaper is an active CR-RC shaper, the CR part filtering the low frequencies and the RC part the high frequencies. It is located after the pre-amplifier to minimize noise. Changing the value of the VFS registry will affect the frequency response of the Beetle chip.

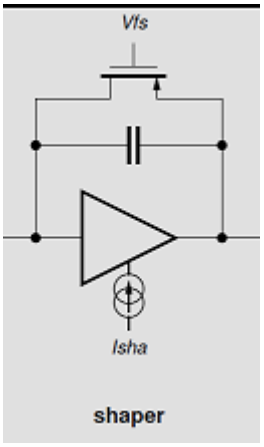


Figure 4.0.12: Shaper inside Beetle's data acquisition chain [35].

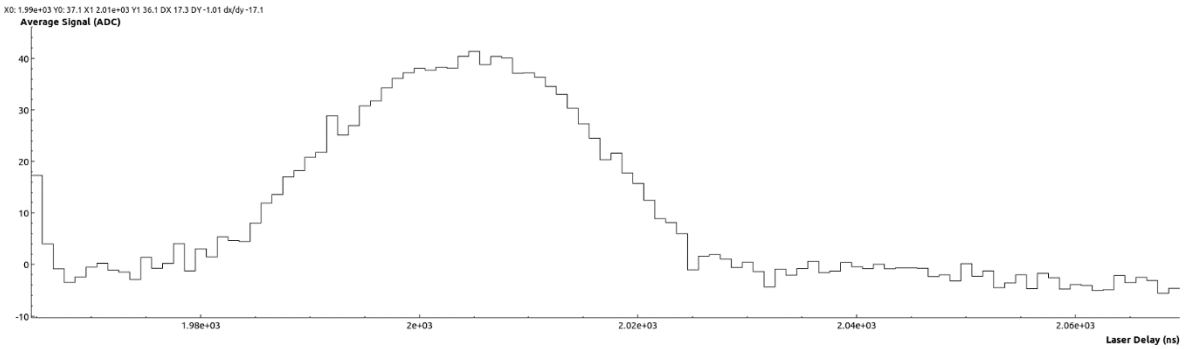


Figure 4.0.13: Beetle output pulse shape with VFS=0

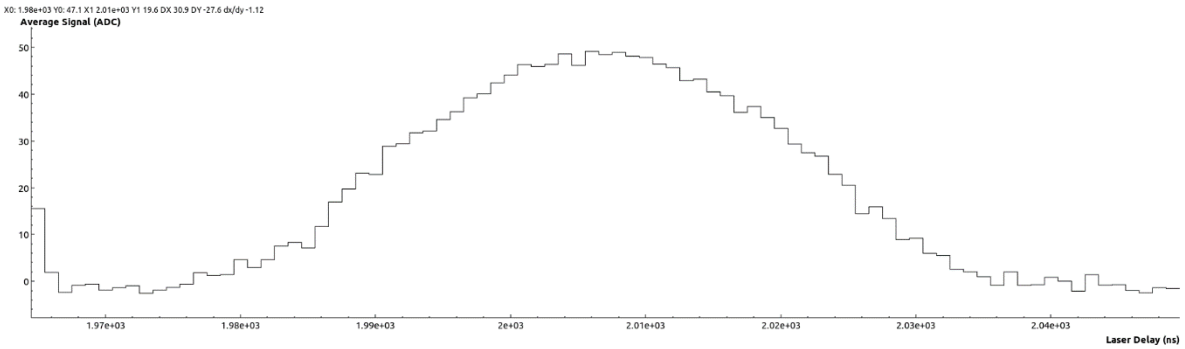


Figure 4.0.14: Beetle output pulse shape with VFS=45

## Reference potential of the non-inverting readout-amplifier of the pipeline

The pipeline-amplifier reference voltage (VDCL) corresponds to the reference potential of the non-inverting amplifier input of the pipeline. The feedback is applied at the inverting input. Decreasing the value in the VDCL registry will increase the output gain of the operational amplifier (with a possible saturation effect).

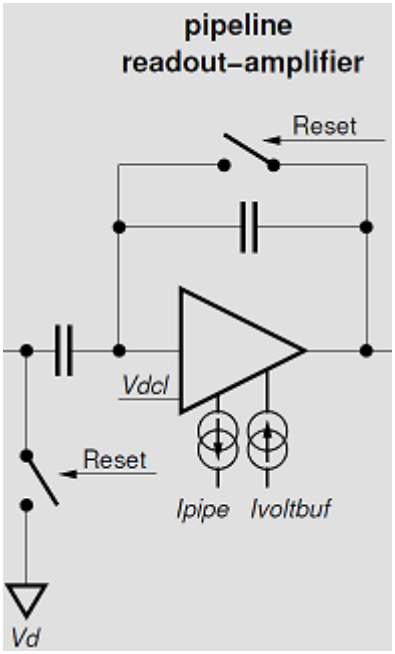


Figure 4.0.15: Reference potential of the non-inverting amplifier of the pipeline [35].

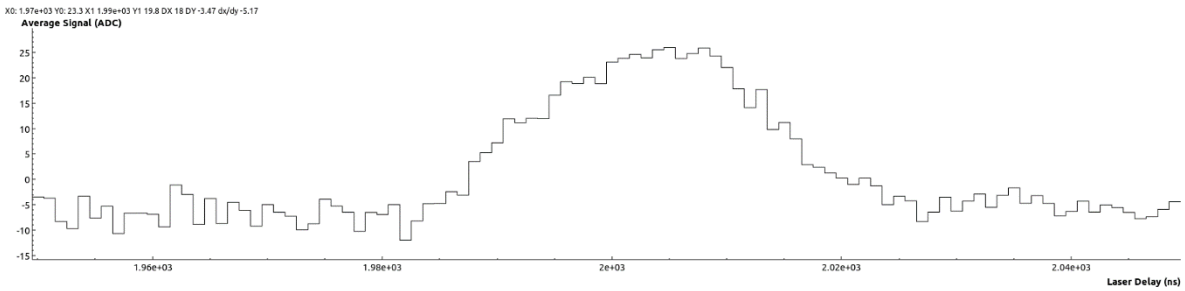


Figure 4.0.16: Beetle output pulse shape with VDCL=10

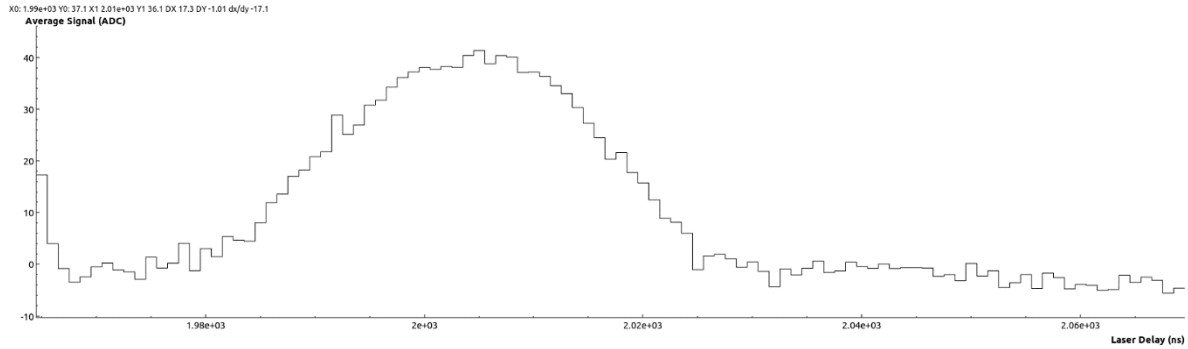


Figure 4.0.17: Beetle output pulse shape with VDCL=105

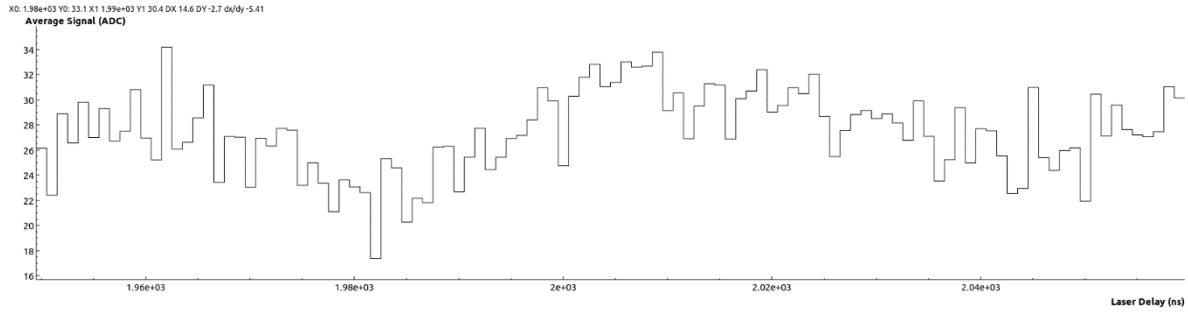


Figure 4.0.18: Beetle output pulse shape with VFS=120

# Commissioning of the new custom Alibava daughter boards

Immediately after delivery, the new Alibava DBs have been tested with the Alibava GUI. Using default Beetle chip parameters, their basic functionality was checked and their noise levels measured (Figures 4.0.19 and 4.0.20). These were seen to be similar to those observed with the reference standard DB (Figure 4.0.21).

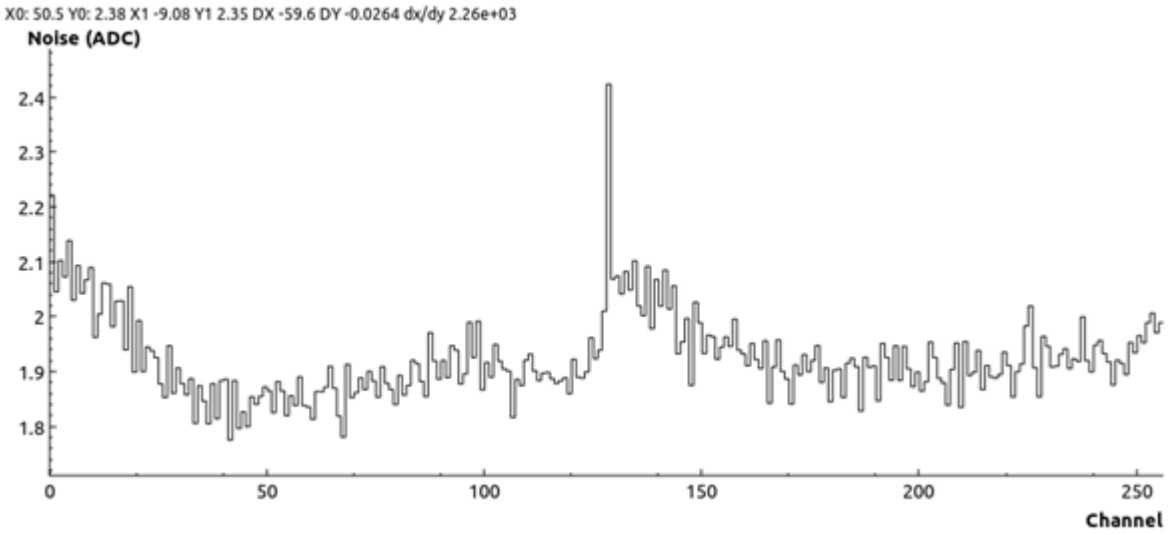


Figure 4.0.19: Noise levels of new DB 1 with default Beetle chip parameters

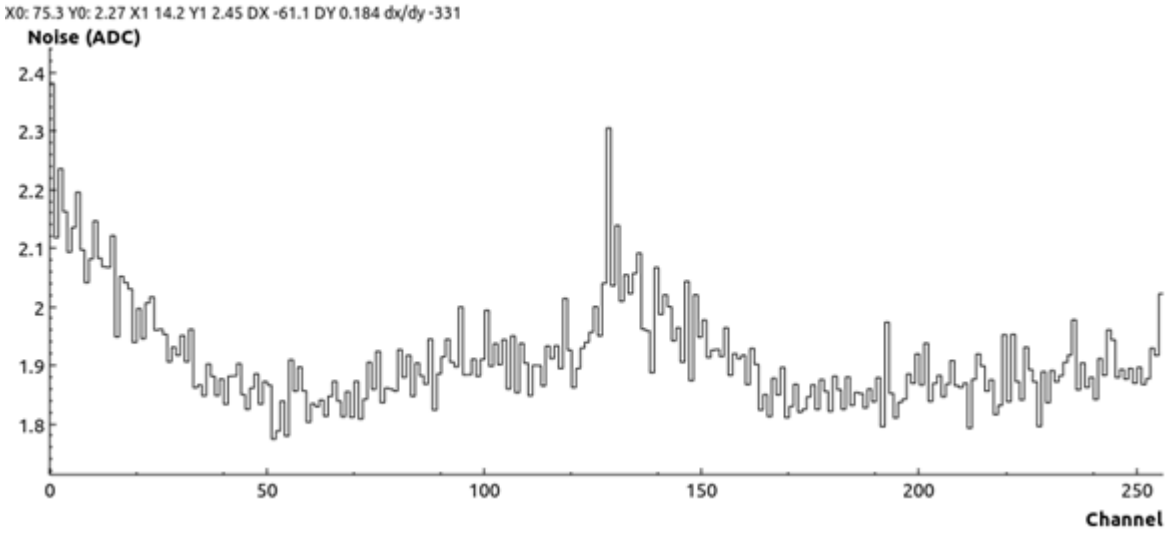


Figure 4.0.20: Noise levels of new DB 2 with default Beetle chip parameters

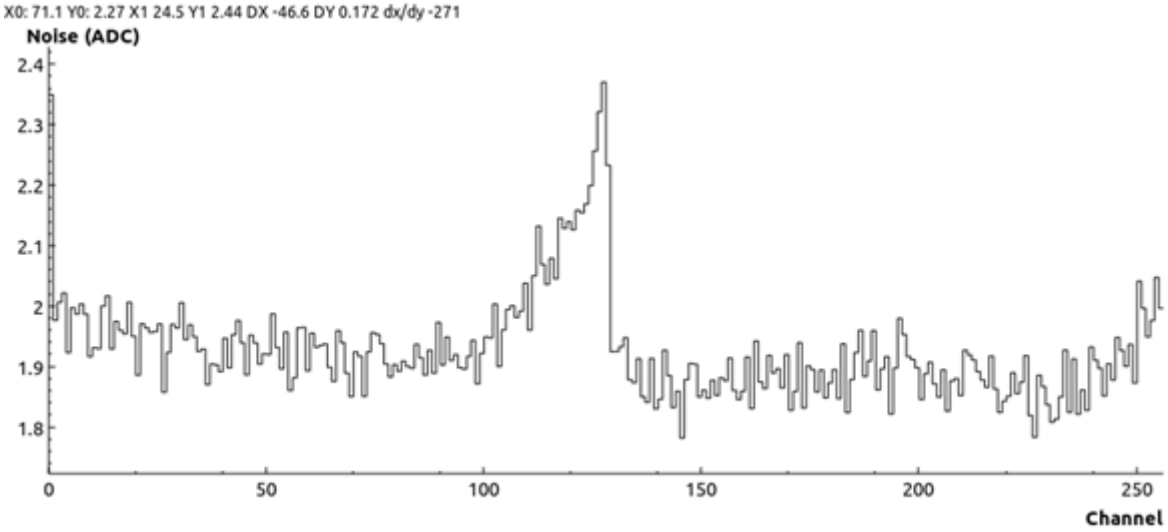


Figure 4.0.21: Noise levels of reference standard DB with default Beetle chip parameters

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