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Development and Evaluation of Test Stations for the Quality Assurance of the Silicon Micro-Strip Detector Modules for the CMS Experiment

Von der Fakultät für Mathematik, Informatik und Naturwissenschaften
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Zusammenfassung

CMS (**C**ompact **M**uon **S**olenoid) ist einer von vier Großdetektoren, die am LHC (**L**arge **H**adron **C**ollider) Beschleuniger des European Laboratory for Particle Physics (CERN) errichtet werden. Für die Suche nach neuer Physik ist die Rekonstruktion der Kollisionsprodukte und ihrer Eigenschaften notwendig. Im innersten Teil des CMS Detektors werden die Spuren von ionisierenden Teilchen mittels eines Silizium-Spurdetektors gemessen. Ein großer Teil dieses Detektors ist mit Silizium-Streifen-Modulen bestückt, die eine präzise Ortsauflösung in einer Dimension liefern. Ein Modul besteht aus einem Sensor für den Nachweis der Teilchen, der dazugehörigen Auslese-Elektronik (Hybrid) und einer Tragestruktur. Da die 15148 Module, die in den Silizium-Streifen-Detektor eingebaut werden, eine gesamte sensitive Oberfläche von ungefähr 198 m^2 haben, ist der innere Spurdetektor von CMS der größte Silizium-Spurdetektor, der je gebaut wurde.
Während die Sensoren und Hybride in der Industrie gefertigt werden, wird der Zusammenbau und die Überwachung der Qualität von den Mitgliedern der 21 teilnehmenden Institute durchgeführt. Da der Zugang zu dem Silizium-Streifen-Detektor sehr eingeschränkt sein wird, wenn der Detektor in CMS eingebaut ist, müssen die eingebauten Module von hoher Qualität sein. Aus diesem Grund werden die Module gründlich getestet und die Testergebnisse in einer zentralen Datenbank gespeichert.
Durch die Entwicklung eines Auslese-Systems und der dazugehörigen Software hat das III. Physikalische Institut einen wichtigen Beitrag für die elektrische und funktionelle Qualitätskontrolle von Hybriden und Modulen geleistet. Das Testsystem verfügt über alle Vorrichtungen für den Betrieb und den Test von Hybriden und Modulen und zeichnet sich durch hohe Zuverlässigkeit und einfach Handhabung aus. Wegen der sehr anwenderfreundlichen und hoch automatisierten Software wurde das Testsystem zum offiziellen Testgerät bestimmt und in verschiedene Teststände integriert.
Die Teststände, in denen das Auslesesytem zum Einsatz kommt, und die in der jeweiligen Software implementierten Tests werden beschrieben. Auf die erwarteten und experimentell ermittelten Signaturen von verschiedenen Fehlern und die Qualitätskontrolle nach den einzelnen Fertigungsschritten wird eingegangen. Im Besonderen wird die Optimierung der Teststände für die Qualifizierung von Modulen der Endkappe des Streifen-Detektors behandelt. Die Signaturen der typischen Fehler sind in allen Teststänten so einheitlich, dass eine Fehlererkennungsroutine entwickelt werden konnte, die Fehler anhand von einheitlichen Kriterien identifiziert. Da die Routine auf alle Moduldaten angewendet wurde kann die Gesamtrate der defekten Streifen über die Datenbank abgeschätzt werden. Die auf diese Weise ermittelte Fehlerrate beträgt weniger als 1 % und zeugt für die hervorragende Qualität der Module.

Abstract

CMS (**C**ompact **M**uon **S**olenoid) is one of four large-scale detectors which will be operated at the LHC (**L**arge **H**adron **C**ollider) at the European Laboratory for Particle Physics (CERN). For the search for new physics the reconstruction of the collision products and their properties is essential. In the innermost part of the CMS detector the traces of ionizing particles are measured utilizing a silicon tracker. A large fraction of this detector is equipped with silicon micro-strip modules which provide a precise space resolution in 1-dimension. A module consists of a sensor for detection of particles, the corresponding read-out electronics (hybrid) and a mechanical support structure. Since the 15,148 modules, which will be installed in the silicon micro-strip detector, have a total sensitive surface area of about 198 m^2, the inner tracker of CMS is the largest silicon tracking detector, which has ever been built.

While the sensors and hybrids are produced in industry, the construction of the modules and the control of the quality is done by the members of the 21 participating institutes. Since the access to the silicon micro-strip tracker will be very limited after the installation in the CMS detector the installed modules must be of high quality. For this reason the modules are thoroughly tested and the test results are uploaded to a central database.

By the development of a read-out system and the corresponding software the III. Physikalisches Institut made an important contribution for the electrical and functional quality control of hybrids and modules. The read-out system provides all features for the operation and test of hybrids and modules and stands out due to high reliability and simple handling. Because a very user-friedly and highly automated software it became the official test tool and was integrated in various test stands.

The test stands, in which the read-out system is integrated in, are described and the tests which are implemented in the corresponding software. The expected and observed signatures of various faults is elaborated and the quality control after the single production steps. In particular the comparison of the test stands for the qualification of the modules for the end caps of the micro-strip tracker is dealt with. The signatures of typical failures is are uniform in all test stands so that a failure identification routine could be developed which provides detection and distinction by means of unique criteria. Since this routine was applied to all module data the total rate of defect strips can be assessed via the database. The excellent quality of the modules stands out due to a failure rate of less than 1 %.

Contents

Chapter 1

Introduction

A reasonable physics theory describes the fundamental particles and their interactions as precisely as possible. To increase the trust into a theory experiments have to proof its predictions. If experiment and theory show identical results within the uncertainties, the trust into the theory increases while a single difference can lead to its end. In that case the theory needs to be modified or replaced.

The state of the art theory describing the known particles and their interactions at high energies is the *standard model*. The predictions of this theory have been proved by many experiments at high precision over the last 30-40 years. A main field of experimental high energy physics is the search for the *Higgs boson* which is demanded by the standard model to explain the well known property of every body, the mass. The Higgs boson is the only elementary particle in the framework of the standard model that has not been discovered yet. Only the mass range of this very heavy particle is known (114.4 GeV / c^2 < m_{Higgs} < 182 GeV / c^2) by earlier and present experiments [1] [2]. The dream of all high energy physicists is the discovery of a unified theory, which describes all known forces and particles. Some major disadvantages of the standard model are the high number of parameters, the missing explanation for the number of particle generations and the missing implementation of the gravitational force.

These unsatisfactory features of the standard model motivate experimentalist and theorists to search for evidences of physics beyond the standard model and the corresponding theory.

1.1 The Large Hadron Collider

The LHC [3] (**L**arge **H**adron **C**ollider) is a collider which will allow to search for new physics on the TeV mass scale. It is located at the European laboratory for particle physics (CERN[1]) close to Geneva and will accelerate protons in two counter-rotating beams to create collisions at a centre-of-mass energy of 14 TeV. An important design

[1]CERN is an abbreviation for Conseil Européen pour la Recherche Nucléaire but the legal name is European Organization for Nuclear Research

parameter of a collider is the *luminosity*. The optimum choice for this parameter is influenced by physics, accelerator and detector constraints. Physics demands the highest possible luminosity not only to ensure that even rare physics events are discoverable but also to have good statistics. An upper limit of the luminosity follows inherently from the accelerator itself where the amount of protons in each bunch, the ability to focus the beam and the time difference between consecutive bunches underlies technological limits. Last but not least the detectors have to be able to cope with the rate of particles without losing performance. Two luminosity phases are foreseen for the LHC. At the beginning the luminosity will be $2 \cdot 10^{33}$ cm^{-2} s^{-1}. During this period of time it will be easier to calibrate the detectors which will be more difficult later when the luminosity is increased by a factor of five. At that time about ten $t\bar{t}$ pairs will be created per second which has to be compared with about 1000 pairs that have been created since the discovery of the top quark at the Tevatron[2] in 1998. On overview on various cross sections versus the centre-of-mass energy is shown in the appendix A.1. The LHC provides four interaction points where huge detectors are placed to record data for event reconstruction and physics analysis. The four detectors are LHC-B (**L**arge **H**adron **C**ollider **B**eauty Experiment), ALICE (**A** **L**arge **I**on **C**ollider **E**xperiment), ATLAS (**A** **T**oroidal **L**HC **A**pparatu**s**) and CMS (**C**ompact **M**uon **S**olenoid). The LHC-B detector will focus on b-physics. ALICE will be mainly active during the heavy ion program where the LHC accelerates heavy ions instead of protons. These vast objects compared to protons will create an environment where evidence of the quark gluon plasma, a predicted state of particles at very high density of energy, may be observable through the generated quarks. The two general purpose detectors are ATLAS and CMS. A large physics program is covered by these experiments which is presented in the physics technical design reports of the two experiments [4] and [5]. The start of data acquisition is planed for 2008.

1.2 The CMS Detector

Many aspects have to be taken into account for the design of a complex detector like CMS. The main aim is to understand the physics processes with maximum detail which results in the capability of a clean reconstruction and identification of leptons, photons and high density stream of hadronic particles (jets). Other constraints arise from the LHC bunch crossing frequency, the high radiation level and promising physics decay channels. For this reason CMS focused on:

- good muon reconstruction
- robust tracking performance
- precise energy measurement

[2]The Tevatron is an accelerator which is located at the research centre Fermilab close to Chicago. At present it is the most powerful accelerator and reaches a centre-of-mass energy of 1.96 TeV.

- high magnetic field

The basic structure of CMS consists of steel wheels which serve as an iron return yoke and allow the compact dimensions. A schematic view of the CMS detector with the main components is shown in figure 1.1. Information on the single sub-detectors and the magnet is given in the following sections.

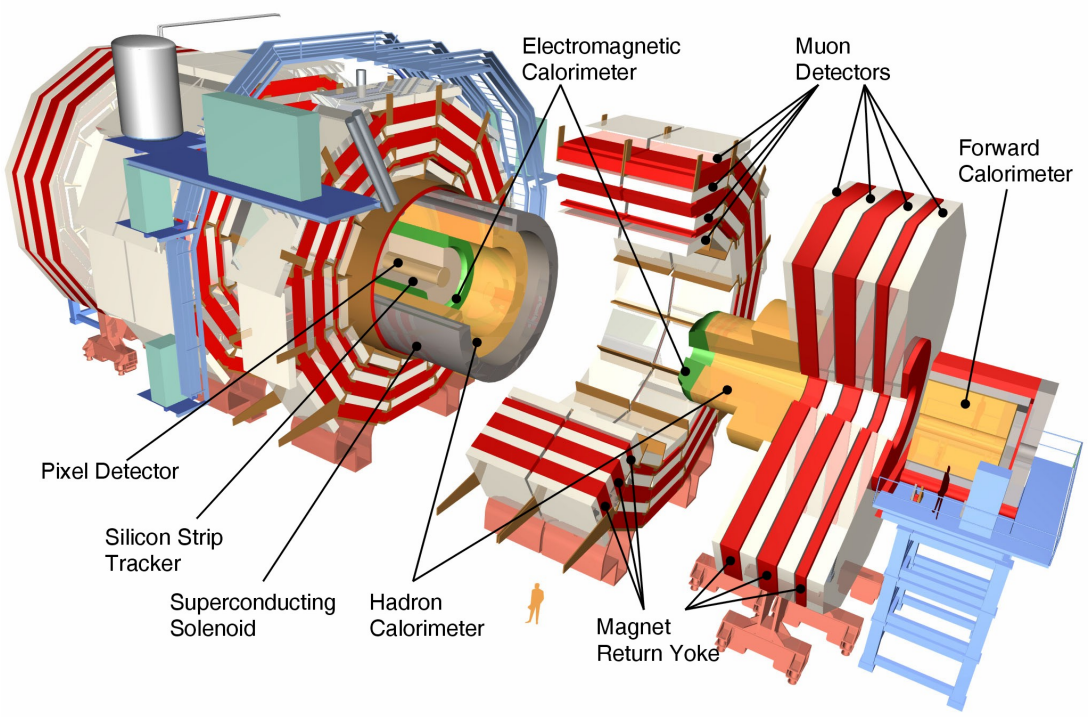


Figure 1.1: Schematic image of the CMS detector. This image and further information is provided at [6].

1.3 The Magnet System

The Magnet System is formed by a superconducting coil of 12.5 m length and an inner diameter of about 6 m and an iron yoke of 1.8 m thickness, which serves as return path for the magnetic field. The solenoid provides a magnetic field of 4 T and surrounds the central tracking system as well as the barrel and end cap parts of the calorimeters. Because of the chosen design particles do not traverse the coil before reaching the calorimeters which allows a more precise energy measurement. The high magnetic field in combination with a high resolution central and muon tracking system provides an excellent transverse momentum resolution even at high momenta.

1.4 The Muon Detectors

A very large surface area is covered by muon chambers which are built into and cover the iron return yoke. The large difference in the particle flow, about 10 Hz / cm^2 in the barrel and up to 1 kHz / cm^2 in the end caps and the strength and homogeneity of the magnetic field drove the design of the CMS muon detection system. In total three types of muon chambers are installed to adapt to the constraints. The barrel region ($|\eta| \leq 1.26$) is instrumented with drift tubes while the end caps ($0.91 \leq |\eta| \leq 2.4$) are equipped with cathode strip chambers. Resistive plate chambers are used in combination with the other detector types all over the muon detector as they provide fast signals which are used for the initiation of the first trigger level.

1.5 The Hadron Calorimeter

The energy of strong interacting particles is measured by the hadron calorimeter. It is therefore the most important tool for the determination of the energy of jets. A sampling calorimeter is used in CMS which is built up by a brass absorber structure with slits for scintillator tiles. The light is guided by wavelength shifting fibres which are embedded in grooves cut in the tiles. The shifted light is coupled into clear light guides for off detector amplification and sampling.
The hadron barrel, the hadron end cap and the hadron outer detector cover the region $|\eta| \leq 3$. The total absorber thickness amounts to approximately 11 interaction lengths so that the total energy is absorbed and the muon chambers are protected from high energetic hadrons. The forward calorimeter is placed in the region $3 \leq \eta \leq 5$ allowing the measurement of jets with low transverse momentum. Because of the high radiation environment the absorber material is made of steel with embedded quartz fibres which detect Cherenkov radiation. As particles from radioactive decays and other slow particles do not reach the Cherenkov threshold the forward calorimeter provides a fast and clean signal.

1.6 The Electromagnetic Calorimeter

The electromagnetic calorimeter measures the total energy of light charged particles like electrons and photons. Thus it plays a crucial role for the detection of the Higgs boson when decaying into two photons one of the benchmark processes CMS was designed for.
The electromagnetic calorimeter is made of about 76.000 $PbWO_4$ crystals. The choice of material allows the design of a fast, fine granularity and radiation hard detector with excellent energy resolution. The crystals have a rectangular tapered shape. The front face dimensions are approximately 22 $\times$ 22 mm which equals the Moliere radius and allows to separate nearby electromagnetic showers. The length of the crystals is 230 mm which corresponds to approximately 26 radiation lengths. The crystals of

the barrel are read out by avalanche photo diodes and the crystals of the end caps are connected to photo multiplier tubes).

1.7 The Central Silicon Tracker

A precise measurement and assignment of tracks is necessary for momentum and vertex reconstruction. The all silicon design of the central tracker provides this feature because of the fast signal processing and the high granularity along with an excellent spatial resolution.
The central region of the tracker will be instrumented with a silicon pixel detector providing unambiguous 3 dimensional space points. The pixel detector is surrounded by a silicon strip detector providing 2 dimensional space points. The schematic build-up of the central tracker is shown in figure 1.2. As this thesis deals with the development and evaluation of test systems for the silicon strip tracker the detection elements of this part of the tracker are described in more detail in the following chapter.

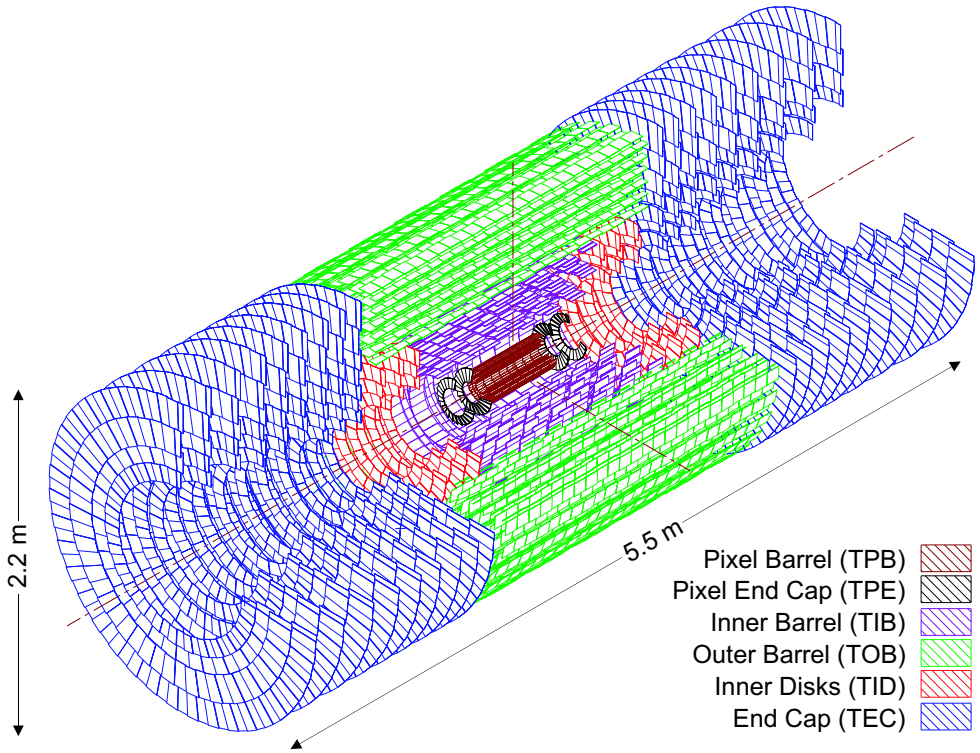


Figure 1.2: Schematic view of the inner tracker [7].

1.7.1 The Pixel Detector

The Pixel Detector is divided in three barrel layers and two end caps consisting of two disks each. The barrel layers are located at mean radii of 4.4 cm and 7.3 cm, the third

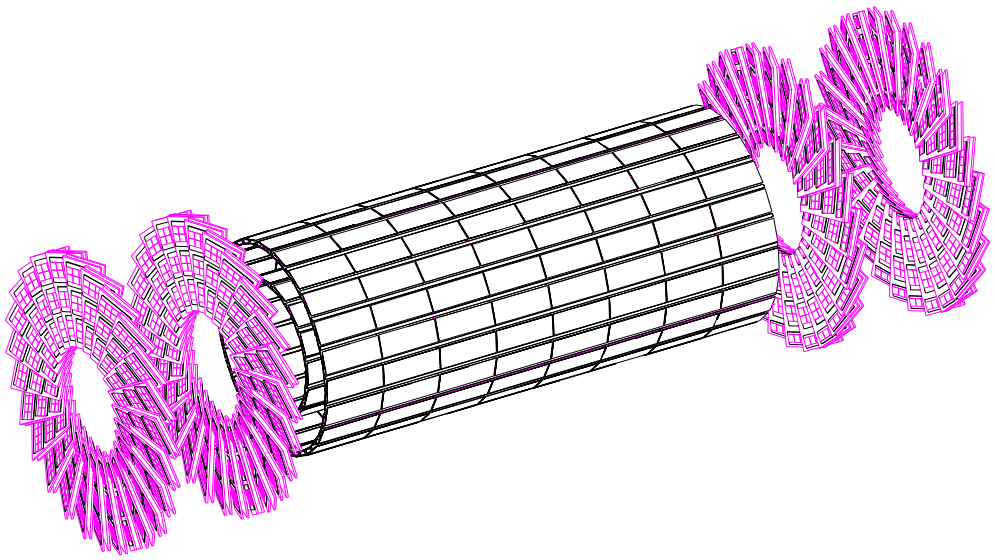


Figure 1.3: Schematic view of the pixel detector.

layer will be added later at 10.2 cm. For identical vertex reconstruction ability in φ and z the pixel sensors in the barrel have a square geometry of 150 µm × 150 µm. The centres of the end caps are located at a distance of $|z|$ = 34 cm and 43 cm from the interaction point. The pixel sensor geometry is rectangular 150 µm × 300 µm. The spatial resolution will be increased by analogue signal interpolation since the charge is shared because of the large Lorentz drift.
A schematic view of the pixel detector is shown in figure 1.3. The pixel detector has about 66 million channels which corresponds to a sensitive surface area of about 1 m^2.

1.7.2 The Silicon Micro-Strip Detector

The silicon strip detector reaches from r = 0.2 m to 1.1 m and has a total length of 5.5 m. It is build up by four parts: the **t**racker **i**nner **b**arrel (TIB), the **t**racker **o**uter **b**arrel (TOB), the **t**racker **i**nner **d**isks (TID) and two **t**racker **e**nd**c**aps (TEC). The sensitive surface area of the SST (**s**ilicon **s**trip **t**racker) is 198 m^2 which makes it the biggest all silicon tracker ever built.

The basic detection units are the modules. They are built up by a sensing element which detects traversing particles and the corresponding read-out unit. The tracker barrel has ten layers of modules, four in the inner and six in the outer barrel. Two layers of the TIB and TOB allow the reconstruction of 3D space points. These layers are equipped with two single sided modules which are mounted back to back and including a stereo angle of 100 mrad. Three inner disks and the end caps enhance the acceptance of the tracker up to η = 2.5. The TID has three and the TEC nine disks on which the modules are organized in rings. Ring one, two and five are double sided layers in same meaning as in the barrel. A quarter cut through the SST gives an im-

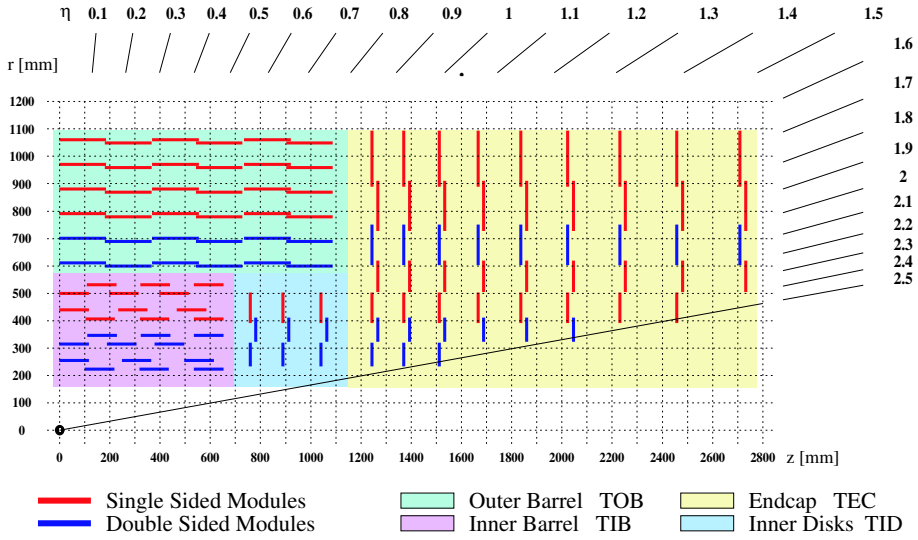


Figure 1.4: Quarter cut through the silicon strip detector. Double sided modules (red) instrument the inner TIB and TOB layers and rings one, two and five in the end cap region. Single sided modules are highlighted in blue [8].

pression on the position of the single and double sided layers (figure 1.4).

For easier handling, testing and maintenance reasons the modules are organized in higher level structures. The structures are summarized in table 1.1.

part of the tracker	denomination of sub-assembly	description
TIB	shells	16 half cylinders
TID	disks	three discs on both barrel sides
TOB	rods	ladders with 6 or 12 modules
TEC	petals	carry up to 28 modules arranged on seven rings

Table 1.1: The sub-assemblies for the four tracker regions. A modular design allows a distributed production scheme and thus more flexibility.

In the TIB and the TID the modules are mounted on the final mechanical supports while the 288 petals are mounted on one of 18 disks and the 688 rods are inserted in the openings of a wheel. A more detailed description of the tracker relevant detection units is given in chapter 2.

1.7.3 The Expected Performance of the Central Silicon Tracker

The plots which are shown here were derived from simulations for the CMS physics technical design report [4]. The expected global *transverse momentum resolution* for single muons, which is an important measure for the physics performance, as a function of pseudo-rapidity is depicted in figure 1.5(a). Up to $|\eta| \leq 1.6$ the momentum

resolution is below 2 %. Since the lever arm gets worse for higher pseudo-rapidity the resolution decreases in this range. The expectations for the transverse and the longitudinal *impact parameter resolution* are shown in figures 1.5(b) and 1.5(c). The transverse resolution varies significantly with the momentum of the muon. For low momenta multiple scattering governs the resolution while it is determined by the resolution of the first hit in the pixel detector for high momenta. The resolution of the longitudinal impact parameter is also governed by multiple scattering for low momenta. For 100 GeV muons the resolution is better than 70 µm over the full acceptance range.

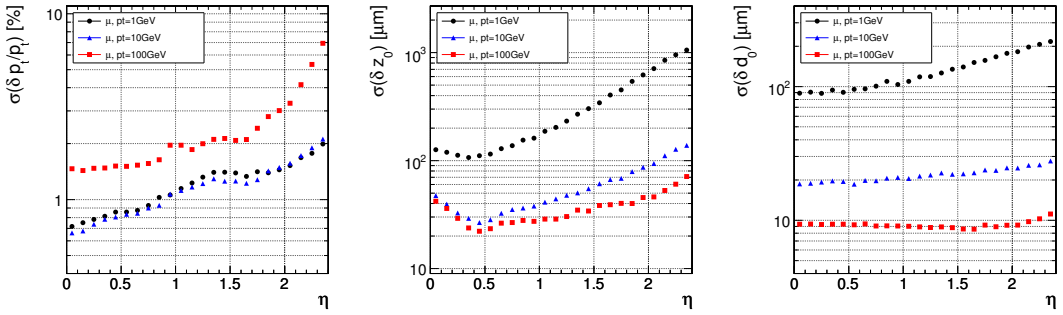


Figure 1.5: The expected momentum (a) and impact parameter resolution in z (b) and transverse (c) of muons utilizing the inner tracking system.

The global reconstruction efficiencies for muons and pions of various transverse momenta with respect to the pseudo-rapidity are illustrated in figure 1.6. The efficiency for muons is about 99 % over nearly the full acceptance range. For pseudorapidities close to zero and higher than 2.1 the efficiency is reduced because of gaps between the ladders of the pixel detector and its accecptance range. The efficiency for pions is in general worse compared to muons because of interactions with the material of the tracker.

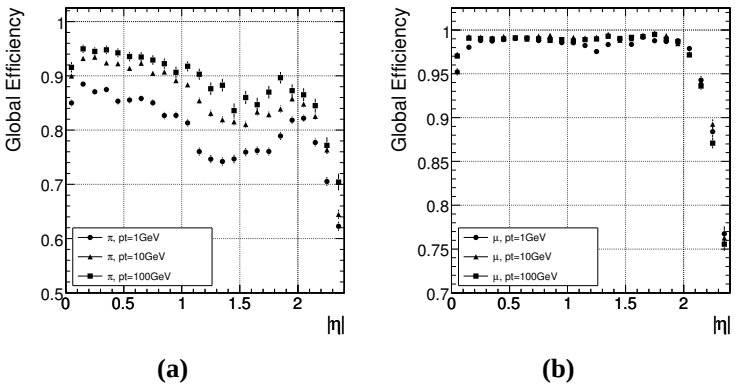


Figure 1.6: The simulated global efficiencies for the reconstruction of pions and muons.

Chapter 2

The Modules for the CMS Silicon Micro-Strip Tracker

The basic detection elements of the SST (**s**ilicon **s**trip **t**racker) are the silicon micro-strip modules. The modules consist of a mechanical support structure (frame), one or two daisy chained silicon strip sensors and an electrical read-out unit (hybrid). The read-out chips which are mounted on the hybrid are connected electrically to the strips on the sensors via wedge bonds and a pitch adapter. In total 15,148 modules are mounted in the SST. A sketch of a module is shown in figure 2.1.
The design of the CMS tracker modules is mainly driven by the harsh LHC radiation environment at a bunch crossing rate of 40 MHz. Robust tracking performance and a lifetime of at least ten years, which is the expected LHC operation time, is mandatory and a thoughtful component qualification and module production scheme is highly desired to ensure an excellent module quality and yield at high production throughput.
In this chapter the module constituting components are introduced, their function is described and the module production scheme is illustrated. As an example the chain of production for TEC (**t**racker **e**nd **c**ap) modules is described.

2.1 The Silicon Micro-Strip Sensors

The silicon micro-strip sensors are the actual particle detecting elements, 24,244 sensors are mounted on modules resulting in a sensitive surface area of about 198 m^2. The working principle and the basic properties of semiconductor detectors are described in the first subsection. In the second subsection the focus is put on the actual design of the sensors which are used for the SST.

2.1.1 Working Principle, Operation and Radiation Issues

The principle build-up of these semiconductor detectors is a p-n diode. At the junction of the p- and n-doped region, holes (unoccupied states in the valence band) from the p-doped side diffuse into the n-doped region and electrons from the n-doped side diffuse

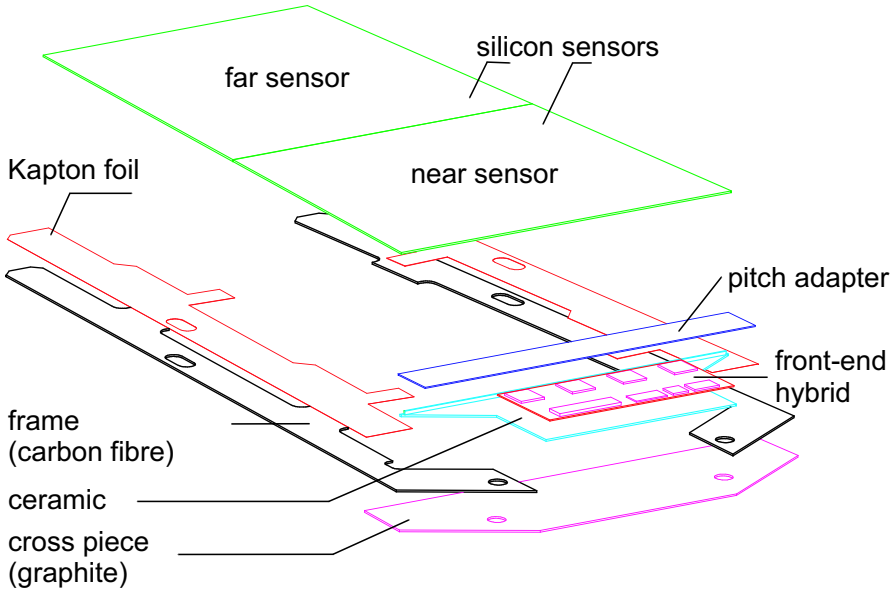


Figure 2.1: Exploded view of a module which contains the main constituents. The module is of TEC ring 6 type which has two sensors in sequence.

into the p-doped region leading to a surplus of stationary positive charge on the n-side and stationary negative charge on the p-side of the junction. The resulting electrical field causes a current which compensates the diffusion current so that no effective current flows in thermal equilibrium. The charge distribution, the electrical field and the potential at a p-n junction are depicted in figure 2.2.

Working Principle

Charged particles lose part of their energy in elastic collisions with electrons when passing through matter. When the energy transfer to a single electron exceeds the bad gap energy the corresponding electron is disentangled from the responding atom and leaves behind a positively charged ion also called hole or defect electron. As the electrons and holes have opposite charge, they move in different directions in the presence of an electric field like in the space charge region of a p-n junction and cause a temporary increase of current. The spatial resolved detection of these currents allows the determination of space points which were passed by a particle. The principle build-up of a semiconductor detector is shown in figure 2.3.
As described above the detection of particles using semiconductor sensors can be split in two main topics:

1. the basic physics process of charge generation by the interaction of charged particles with matter and

2. the operation of semiconductor detectors for the extraction of the charge.

Both topics will be addressed in more detail below.

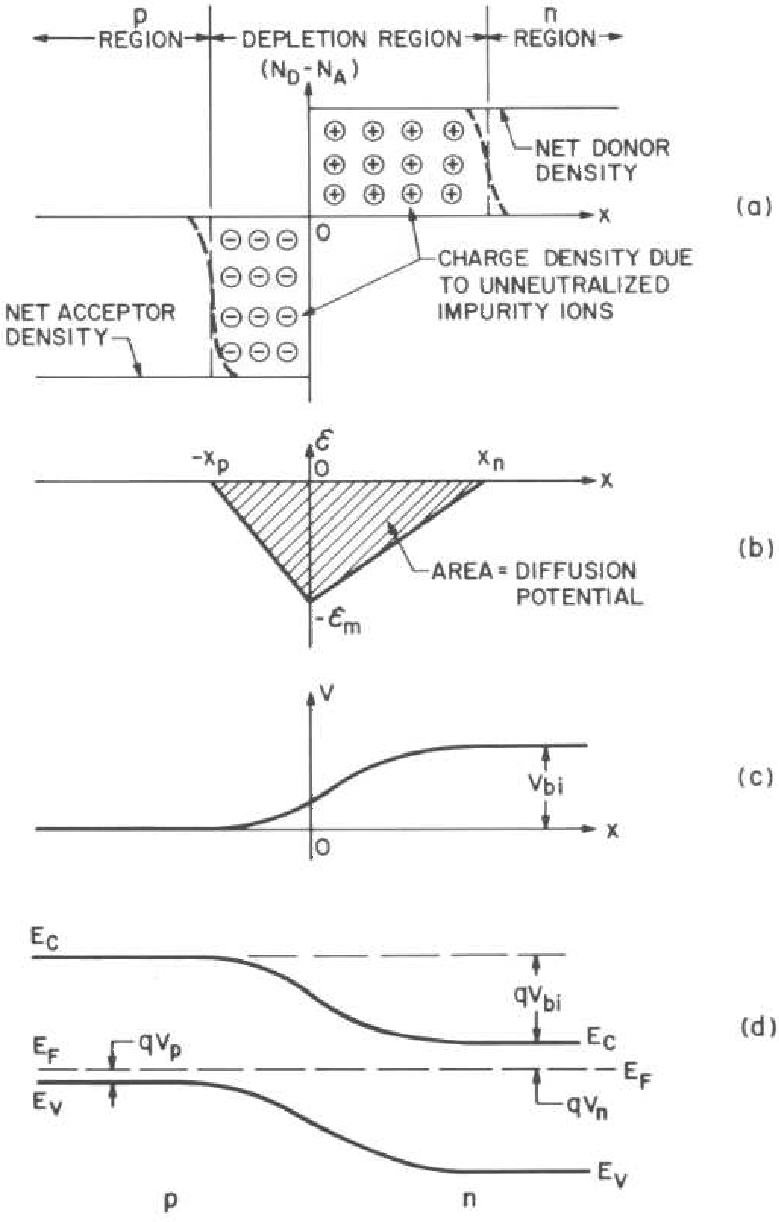


Figure 2.2: Charge distribution (a), field configuration (b), potential (c) and band structure (d) of a p-n diode [9].

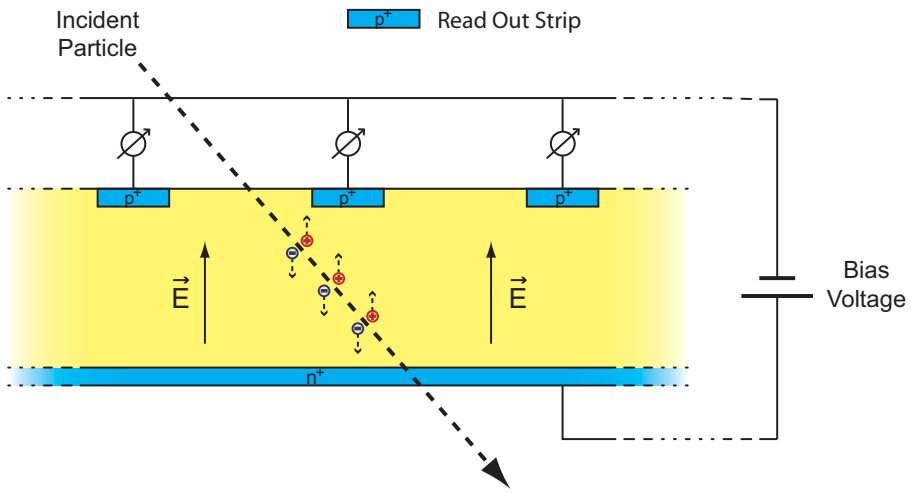


Figure 2.3: Working principle of a semiconductor detector: An ionizing particle generates electron-hole pairs along its trace. The electrical field at the p-n junction separates the mobile charge carriers which can be detected as an electrical signal at the terminals of the diode.

The amount of primary charge which is generated by an ionizing particle depends on its energy loss or the stopping power respectively. The basic theory of the energy loss by electromagnetic interaction between incident particles and matter was developed by Bohr, Bethe and Bloch. While Bohr used classical arguments, the latter two physicists considered quantum mechanics and give the established equation describing the energy loss due to ionisation and atomic excitation their name, the Bethe-Bloch formula 2.1. The energy region where the Bethe-Bloch formula describes the total mean energy loss is shown in figure 2.4. The formula applies to moderately relativistic, charged particles except for electrons where corrections are needed because of their low mass. More information about the energy loss in the Anderson-Ziegler and the Lindhard-Scharff region is given in [10], [11], [12] and [13]. The high energy limit of the Bethe-Bloch formula is reached when radiation processes dominate the energy loss. The energy loss due to ionization is indicated by the dash dotted line in figure 2.4 and approaches an almost constant level for highly energetic particles. This is called the Fermi plateau.

The classical approach for the calculation of the energy loss is the electromagnetic interaction of a heavy particle with an electron at rest. The precision of the formula in the energy range where the naive model starts to become invalid is improved by correction terms. In dependence of the considered corrections the Bethe-Bloch formula can be written in different ways. The expression used in [15] is presented here.

$$-\frac{dE}{dx} = 2\pi N_0 r_e^2 m_e c^2 \rho \frac{Z z^2}{A\beta^2}\left[ln\left(\frac{2m_e\gamma^2 v^2 W_{max}}{I^2}\right) - 2\beta^2 - \delta - 2\frac{C}{Z}\right] \qquad (2.1)$$

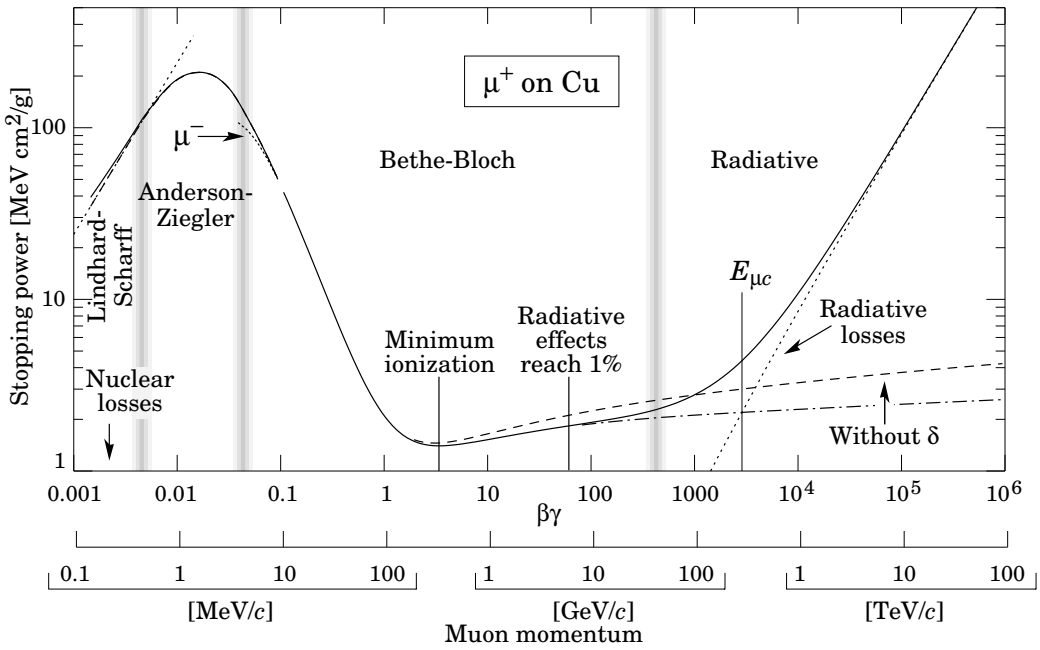


Figure 2.4: The mean rate of energy loss for positive muons in copper over nine orders of magnitude in momentum. The solid lines indicate the total stopping power. The vertical bands separate the regions where the various approximations hold. In the Bethe-Bloch region particles lose their energy because of ionization and excitation [14].

with:

x : path length in g/cm^2,

r_e : the classical electron radius $2.817 \times 10^{-15} m$,

m_e : the electron mass 9.109×10^{-31} kg,

M : mass of incident particle,

N_0 : Avogadro's number $6.022 \times 10^{23} mol^{-1}$,

I : effective ionization potential averaged over all electrons,

Z : the atomic number of the medium,

A : the atomic weight of the medium,

ρ : the density of the medium,

z : charge of particle in units of elementary charge e,

β : velocity of the incident particle in terms of the speed of light $\frac{v}{c}$,

γ : Lorentz factor $\frac{1}{\sqrt{1-\beta^2}}$,

δ : density correction due to polarization effects,

C : shell correction,

W_{max} : maximum energy transfer in a single collision, $\frac{2\, m_e\, c^2\, \beta^2\gamma^2}{1 + 2\frac{m_e}{M}\sqrt{1+\beta^2\gamma^2}}$

As shown in figure 2.4 the energy loss decreases with increasing particle energy in the non-relativistic regime. This behaviour is caused by the β^2 term which expresses the decrease of the interaction time which is $\propto 1/v$, the inverse of the incident particle velocity. For high energies the energy loss increases logarithmically because of the Lorentz term γ grows while v and β converge to c and 1. The correction terms C and δ increase the precision of the formula at the higher and the lower energy limit.
The basic model neglects atomic binding forces which play a role in the low energy limit where the electron cannot be treated like being at rest. The reduction of the energy transfer is expressed by the shell correction term $\frac{C}{Z}$. At the high energy limit the polarization of the material reduces the logarithmic increase of the energy loss towards higher energies. The density correction called δ term is added to the formula for description of this effect. Due to these corrections the formula describes the energy loss in a wide energy range at high accuracy.
Particles which suffer minimum ionization losses ($\beta \cdot \gamma \approx 4$) are called mips (**m**inimum **i**onizing **p**article**s**). Since the energy loss due to ionization of high-energetic particles does not differ much from minimum ionization losses the expression is also used as a synonym for particles where $\beta \cdot \gamma > 4$. For all practical purposes in high energy physics the stopping power in a given material in determined only by β and particles with identical velocity lose the same amount of energy per mass volume in different materials other than hydrogen.
The mean energy loss as given by the Bethe-Bloch formula cannot be derived from the measurement of the number of generated electron-hole pairs by a single particle in a thin absorber because of the stochastic nature of the energy loss. The probability distribution function which is assigned for the energy loss in an absorber of thickness x is usually called Landau distribution. The exact treatment of the interaction of particles with matter is a non trivial problem. The calculation of the probability distribution function of pions with an energy of 500 MeV in silicon of variable thickness was made by Bichsel [14] and is shown in figure 2.5.
As shown in the figure, the energy loss per unit length has a non negligible probability over a wide region of energy. The large tail of the distribution shifts the mean energy loss rate to much higher values than the most probable rate which is below 70 % for typical silicon sensors. The most probable energy loss rate per unit length increases for thicker absorbers and the ratio w/Δ_p decreases, where w is the fullwidth at half maximum and Δ_p is the most probable loss rate as indicated in the plot.

While charged particles are seen in the detector, photons become visible only if they interact with single electrons by photo effect or Compton scattering. Photons with an energy above the rest mass of an electron-positron pair, which is about 1 MeV, may lose energy in the presence of nuclei by electron-positron pair creation. The tracker is blind for very high energetic photons as present in the Higgs decay into two photons.

Operation

In the following part of this subsection the operation of semiconductor detectors is addressed. The charge which is generated by an incident particle needs to be extracted

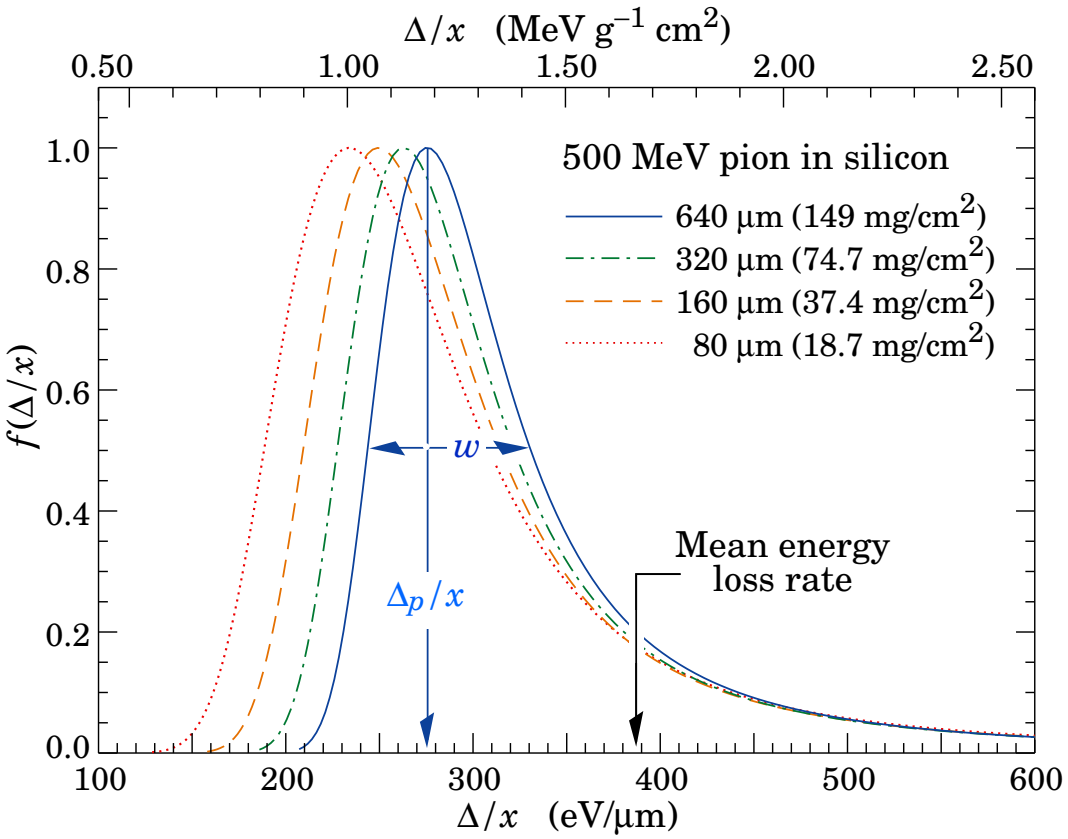


Figure 2.5: Energy loss probability of 500 MeV pions in silicon of different thickness. The most probable value is usually less than 70 % of the mean energy loss rate. The difference is caused by rare hard-collision losses that create a long tail. The functions are normalized to unity at the most probable value Δ_p/x [14].

from the semiconductor and transferred to the read-out electronics. As described at the beginning of this subsection the principle build-up of a semiconductor detector is a p-n diode. In applications the diode is usually biased in reverse direction. By this action the width of the space charge region is increased and the capacity of the diode is reduced.

The longer the path a charged particle passes within the sensitive volume, the more electron-hole pairs are separated and the detection of the electrical signal becomes easier. The sensitive volume is proportional to the depth d of the space charge region, which is given by the following equation:

$$d = \sqrt{\epsilon\epsilon_0 \frac{N_A + N_D}{qN_AN_D}(V_{\text{bi}} - V_{\text{depl}})} \tag{2.2}$$

with the constants, the material properties and the parameters::

ϵ_0 : permittivity of free space
k : Boltzmann's constant
q : elementary charge
ϵ : permittivity of semiconductor
V_{bi} : built in voltage $kT\ln(\frac{N_C N_V}{(n_i)^2})$
n_i : intrinsic charge carrier concentration; $\sqrt{N_C N_V}\mathrm{e}^{-\frac{E_g}{2kT}}$
N_C : effective density of states in conduction band
N_V : effective density of states in valence band
E_g : band gap energy
N_D : donor concentration
N_A : acceptor concentration
V_{depl} : externally applied depletion voltage

For a given semiconductor and depletion voltage the depth of the space-charge region only depends on the doping concentration as indicated by equation 2.2. The maximum number of charge carriers can be extracted when the space charge region expands over the full detector. For this reason the bulk material is usually doped slightly to reduce the needed depletion voltage.
A further reason for depletion of the full detector is the capacitance C. The noise of an amplifier is proportional to the input capacitance [16] which is mainly determined by the capacitance of the p-n diode. Like for a plate capacitor where the capacitance decreases with increasing plate distance, the capacitance of the p-n diode decreases with the depth of the space charge region. Thus the capacitance is lowest if the full detector is depleted.

Radiation Issues

While the interaction of radiation with the electron clouds is used to sense particles and does not harm the detector, interactions with the nuclei can cause a permanent change in the structure of the silicon crystal.
Typical defects are interstitials, atoms which sit between regular lattice sites, and vacancies, not populated lattice sites. These primary defects are not stable at room temperature. They can move and anneal if an interstitial fills a vacancy but they can also form stable stationary clusters. While the first effect is desirable, stationary clusters predominantly deteriorate the performance of the detector which should be avoided. If high radiation tolerance is desired, like in CMS where the fluence at the innermost silicon layer is $1.6 \cdot 10^{14}$ 1 MeV equivalent neutrons per square centimetre after ten years of operation, the silicon detectors are operated at lowered temperature, where the

formation of clusters is suppressed. The dislocation defects which cannot be avoided as they are part of the primary interaction cause an increase of leakage current, signal charge trapping and change the effective doping concentration. The effects are explained in more detail below.
The power dissipation of the sensors is proportional to the leakage current. As the temperature of the sensors has to be sufficiently low the cooling system must consider the additional heat load. A lavish margin is needed since the leakage current depends exponentially on temperature which can lead to thermal runaway. Furthermore the leakage current is a source for additional noise [17].
Defects in the crystal can act as charge traps. These are states of energy within the band gap where charge is temporarily trapped and released at certain time constant. If charge is trapped longer than the charge collection lasts the total signal height is decreased which has a negative affect on the performance. In applications the sensors are usually slightly over-depleted to reduce the effect of charge traps.
In high energy physics the bulk material of silicon sensors is usually n-doped. The radiation induced dislocation defects in silicon act as an effective increase of the acceptor concentration. Since the acceptor concentration rises with time, the n-bulk converts to p-bulk when the detector has suffered a certain dose of radiation. For this reason the influence of radiation on a semiconductor is called type inversion. While the doping concentration decreases at the beginning, which coincides with a lower necessary depletion voltage, the bulk doping concentration rises again after type inversion. The initial n-type doping delays the time where the p-type concentration gets so large that the necessary depletion voltage exceeds a level where electrical breakdown becomes a serious problem.
The change of the doping concentration with fluence is shown in figure 2.6. The type inversion occurs at the spikes where the effective doping concentration is lowest. The fluence at which the type inversion occurs is determined by the initial doping concentration of the bulk. At fluences $> 5 \cdot 10^{14}/\mathrm{cm}^2$, this means above the expectation for the silicon of the SST, the effective doping concentration is independent from the initial concentration. More detailed information on radiation damages can be found in [18].

2.1.2 The CMS Sensor Design

The design of the sensors for CMS is mainly driven by the harsh radiation environment in the CMS tracker. To guarantee a reliable performance of the sensors during the foreseen ten years of operation an intense research and development phase was launched where radiation tolerance, high voltage stability and good signal-to-noise ratio were the key issues [20]. The most important design aspects and the relevant silicon properties are described below.

A schematic view of the CMS sensor design is shown in figure 2.7. A structured aluminium layer which forms the read-out strips and rings for sensor depletion sits on the top side of the sensor while the backplane is homogeneously covered with alu-

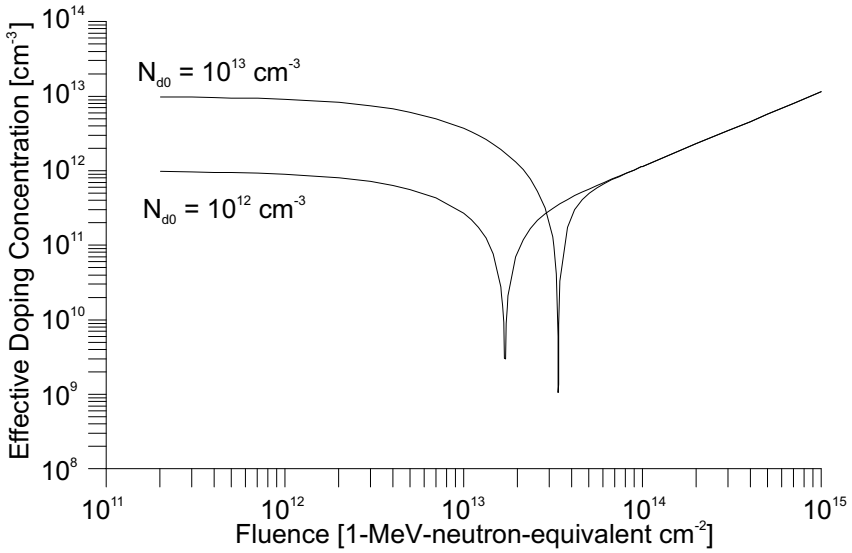


Figure 2.6: Calculated effective doping concentration vs. high energy proton fluence for silicon of different initial donor concentration [19].

minium[1]. The depletion voltage is applied between the aluminium backplane which is located below a heavily n^+-doped region and the bias ring which is connected to p^+-implanted regions below the read-out strips via 1.5 ± 0.5 MΩ poly-silicon bias resistors.

The sensor edges get seriously damaged when the sensors are cut out of the wafer. The damaged surface acts like an effectively n-doped region with low resistivity compared to the bulk region. While this region hinders electrical discharge over the cutting edge it also brings the potential of the sensor backplane to the sensor top where a n-implanted region increases the high voltage stability. For the protection of the bias ring from voltage fluctuations over the sensor edges, a guard ring is implemented. As the guard ring provides a low resistive path around the whole bias ring it reduces the influence of the edges on the sensor performance. The parameters for the save operation of the sensors are summarized in [21].

The aluminium read-out strips are capacitively coupled to the underlying p-implanted regions. The electrical insulation between the strips and the p-implant is realized by thin layers of SiO_2 and Si_3N_4. The breakdown performance of this *read-out capacitor* called structure is increased significantly by aluminium strips which are 15 % wider than the underlying p-implant as part of the field lines are moved from the p-implant into the dielectric [20].

The sensors are cut out of 6″ inch wafers with <100> *crystal orientation*. Sensors cut out of silicon with <111> characteristic showed an increase of the interstrip capacity after irradiation. The capacitance depended on the depletion voltage and rose up to a factor of two while sensors with <100> orientation were nearly unaffected by irradiation. A possible explanation for this feature is the accumulation of electrons below the

[1]The tracker is aligned with laser beams. For this reason part some of the modules were prepared with a hole in the aluminium backplane to increase the transmission of the beam.

dielectric in the region between the strips caused by positive charge in the dielectric after irradiation [22]. The front surface of the sensors is passivated to reduce the handling fragility and to increase the electrical stability.
A parameter of the silicon sensors is the dimension of the width w and the pitch p of the aluminium strips. Both distances are depicted in figure 2.7. The ratio of the two parameters determines the strip capacitance per unit length, which is smaller for low ratios and the break down performance at high depletion voltage, which is better for high ratios. The optimum value for the parameter was determined in a series of tests. A ratio of 0.25 was found to suit best [22]. The *width-to-pitch ratio* is identical for all sensors which are built into the SST of CMS.
Two types of sensors will be used to accommodate the different demands for modules

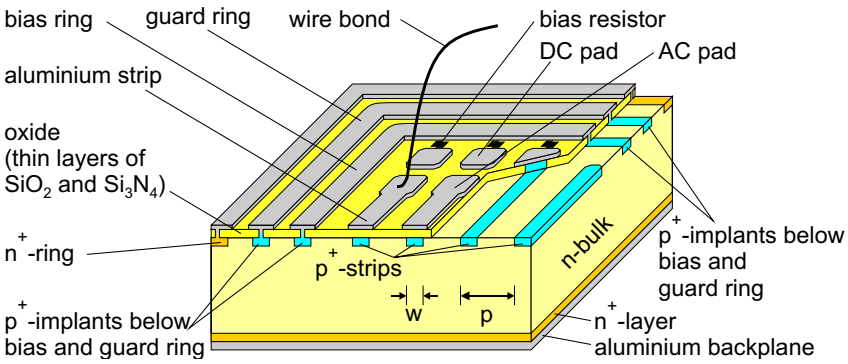


Figure 2.7: Design of the silicon strip sensors for the CMS tracker. The read-out strips are coupled capacitively to the p-doped terminal of the p-n diode. The bias voltage is applied between the bias ring which is connected to ground and the aluminium backplane which is put at positive potential.

containing one or two daisy chained sensors and their position in the tracker. The one sensor modules will equip the inner part of the tracker and thus suffer more radiation damage. They will therefore be equipped with sensors of 320 µm thickness so that the material budget is low but also enough charge is generated. The outer part of the tracker will be instrumented with two sensor modules. As the capacitance is higher for these modules and the particle fluence is lower, thicker sensors of 500 µm thickness are used to increase the amount of primary charge.
As explained in subsection 2.1.1 the doping of the substrate is of great importance since radiation damage will cause dislocation defects in the crystal and change the effective doping of the bulk material. Since the thin sensors will suffer higher fluences the initial doping concentration is higher compared to the thick sensors which expresses in lower initial resistivity. The depletion voltage is about 150 V at the LHC start up and is expected to increase to 300 V after ten years of operation. During tests the sensors are screened to tolerate bias voltages up to 500 V. This increases the safety margin and allows the operation at voltages higher than the depletion voltage which is desirable as explained in subsubsection 2.1.1. Some properties of both sensor types are summarized in table 2.1.

	thin sensors	**thick sensors**
vendor	HPK	STM and HPK
thickness	320 µm ± 20 µm	500 µm ± 20 µm
flatness	100 µm over total sensor length	
dicing accuracy	± 20 µm	
implant precision	± 1 µm	
crystal lattice orientation	⟨1 0 0⟩	
resistivity μ	1.5. . .3.25 k Ω cm	4. . .8 k Ω cm
bias resistors	1.5± 0.5 M Ω	
width-to-pitch ratio	0.25	
pitch	80. . .158 µm	122. . .205 µm
width of p^+-implant	20. . .39 µm	30. . .51 µm
width of aluminium	28. . .51 µm	40. . .67 µm

Table 2.1: Parameters of the silicon sensors used in CMS (source [23]).

The sensors for the SST are produced by STM (ST Microelectronics[2]) and HPK (Hamamatsu Photonics[3]). Originally STM was supposed to produce the thick sensors but after a series of problems the contract was modified and HPK took over the rest of the production. Less than 5 % of the modules which will go into CMS will be made with sensors from STM. Further information is provided in table C.7 in the appendix.

2.2 The Frames

The frames serve as a mechanical support and provide holes for precise mounting of modules on the sub-assemblies. The material used for the construction of the frames has to act as a sufficient heat flow path, accommodate the thermal expansion coefficient of silicon and has to be reasonably radiation tolerant, like all constituents of the tracker. Carbon fibre and graphite were found to suit these needs. The frames carrying one sensor consist of a single graphite piece while the frames carrying two sensors are made from two acrylic coated carbon fibre pieces and a middle cross-piece made from graphite. A typical frame for a module with two sensors is shown in figure 2.8.

Before the frames can be used for module assembly a circuit embedded in kapton[4] is glued to the frame. The main aim of the circuit is to bring the high voltage to the sensors and to insulate electrically the frame from the backside of the sensors. The bias circuit has an R-C element which acts as a filter for the incoming voltage and a coupling capacitor to apply pulses on the backplane of the silicon sensors as shown in figure 2.9. The filter capacitor C2 is not mounted on the circuit. It was foreseen as

[2]STMicroelectronics, Stradale Primosole 50, I-95121 CATANIA, Italy; http://www.st.com
[3]Hamamatsu Photonics, Hamamatsu 435, Japan; http://www.hamamatsu.com
[4]Kapton is a registered polyimide product from DuPont, http://www.dupont.com/kapton.

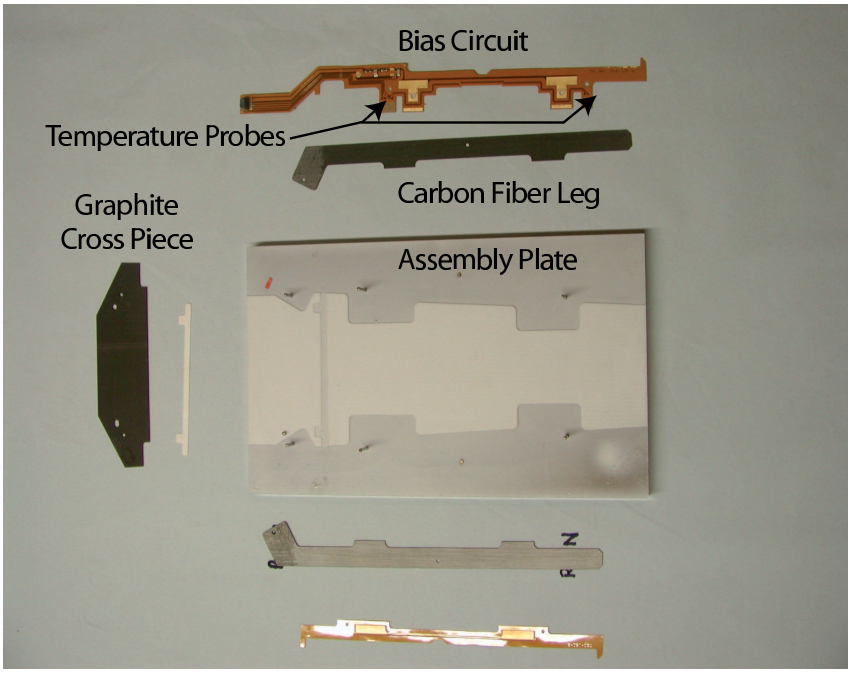


Figure 2.8: Photograph of the parts constituting a TEC ring six frame. Frames serve as mechanical support for the modules and provide a heat path.

a fall back solution in case of noise problems. If C2 is mounted the backplane pulse injection becomes ineffective as the coupling capacitor C3 is much smaller than C2.
For measurement of the temperature of the silicon sensors three temperature probes are mounted on the circuit. One probe is connected to an external read-out system. The remaining two are switched in parallel and read out by a chip on the hybrid (see subsection 2.3.4). On modules with two sensors the temperature of the sensor which located closer to hybrid is measured externally. The chip on the hybrid is connected to the probes sitting on both sensors.
The kapton bias circuit is not necessarily in good contact with the sensor at the position of the probes, which has to be considered in the results.

2.3 The Hybrids

The hybrids are the front-end electrical read-out units. They are mainly build up by a four-layer printed circuit board with a flex cable soldered to a 50 pin NAIS[5] connector which serves as interface. The circuit carries passive components and four different ASICs (**a**pplication **s**pecific **i**ntegrated **c**ircuits) which are needed for data acquisition and monitor of relevant module operation parameters. A photograph of a hybrid with a description of the components is shown in figure 2.10.

[5]NAIS: a series of connectors from Matsushita Electric Works, Ltd. 1048, Kadoma, Kadoma-shi, Osaka 571-8686, Japan. `http://www.mew.co.jp/ac/e/`

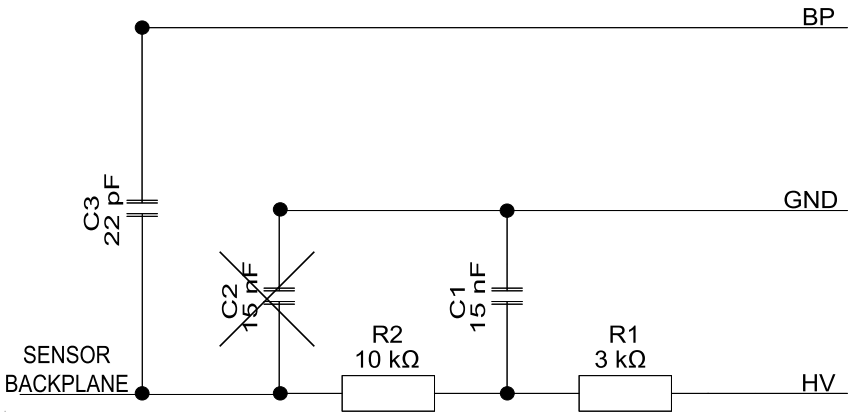


Figure 2.9: The bias circuit for TEC ring 6 modules. The bias voltage for the silicon sensors is filtered and a coupling capacitor is implemented to apply a pulse on the back-plane of the silicon sensors. It was decided to leave the position for the capacitor unpopulated.

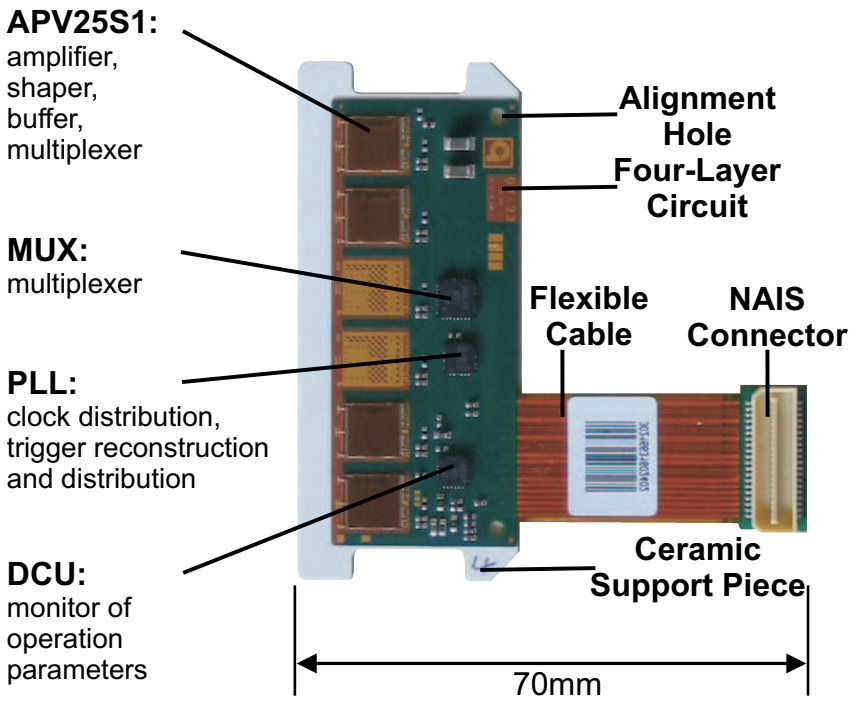


Figure 2.10: The photograph shows the top view of a TEC hybrid with four APV chips and the connector oriented upwards. In total more than 21.000 hybrids were produced for the tracker not including prototypes.

There are basically three basic hybrid designs: one for TIB/TID, one for TEC and one for TOB. While the difference between TEC and TOB hybrids is basically the length of the flexible cable, TIB and TID hybrids are smaller because of the reduced space available in the inner part of the SST. The hybrids of a certain design are equipped with four or six APV chips, the NAIS connector is oriented in up or down direction and the ceramic support plate may have different shapes. In total twelve types of hybrids are constructed for completion of the tracker. The various types are listed in table C.5. More detailed information is provided in section C.1 in the appendix.

The most critical issue in the design of the hybrids are the small dimensions which are mandatory to avoid gaps in the acceptance of the single layers of modules. In particular the high density and the small diameter (100 µm) of the inter-layer electrical connections (vias) as well as the difficult integration of the flexible cable became the key elements in the choice of the substrate technology after the production of reliable hybrids made with ceramic substrates had failed. After an intense research and development program a robust design and substrate technology was found[6].
The final version of hybrids consist of a four layer copper circuit embedded in kapton with an additional fifth intermediate kapton layer. The kapton substrate allowed the flex tail to be part of the circuit which is a great advance compared to the earlier ceramic substrate where the tail was soldered. The layers of kapton provide sufficient mechanical stiffness before the circuit is laminated on a ceramic support plate which turns the hybrids into a rigid object. The support plate is a flat object and simplifies the integration of the hybrids during module assembly. As ceramic has good heat transfer properties compared to kapton it also provides a good heat flow path. The layer structure of a final version hybrid is shown in figure 2.11.

The hybrids are supplied with two voltages 2.5 V and 1.25 V. The current drawn on each line depends on the number of APVs which is four or six, the register settings of the chips and the trigger rate. The maximum total power consumption of a hybrid is about 2 W. Since about 15,000 hybrids will instrument the tracker the total power dissipation of the hybrids will be about 30 kW.

2.3.1 The APV Chip

The chip reading out the strips of the silicon micro-strip sensors is the APV25-S1 (**a**nalogue **p**ipeline **v**oltage). The APV is a CMOS chip developed for the CMS silicon micro-strip detector and is fabricated in a radiation hard D-MILL 0.25 µm technology. The bare chip is mounted on the hybrid because of the small pitch of the input channels. The key features of the APV are:

- 128 input channels
- 192 stage analogue pipeline
- 128:1 multiplexer

[6] An overview on the various versions of hybrids is shown in table C.1 in the appendix.

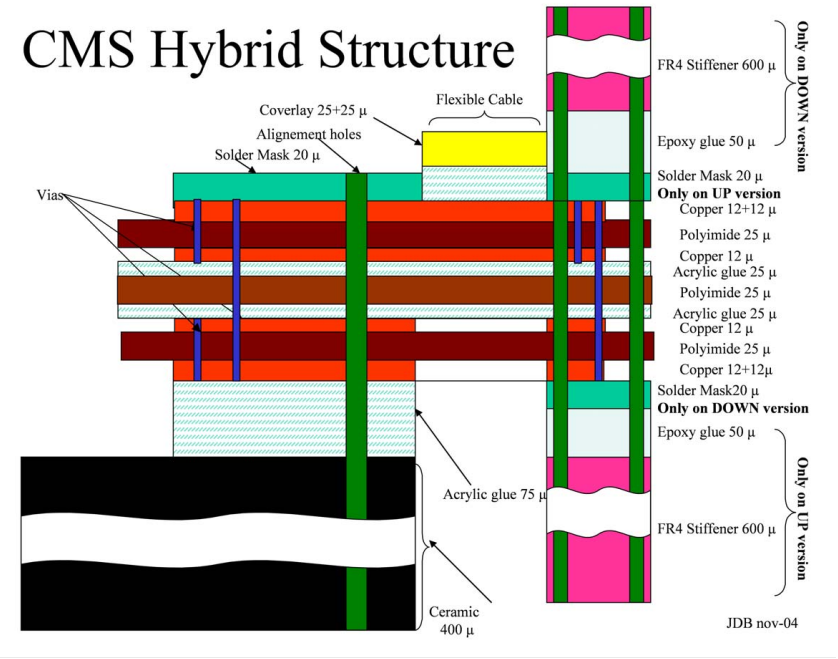


Figure 2.11: The circuit of final version hybrids is build up by layers of copper, polyimide and acrylic glue. The stiffener, the dimension of the vias and the innermost layer of polyimide are critical parts for construction of reliable hybrids (see subsection 5.1.1).

- single differential current output line
- programmable latency
- calibration unit
- I^2C interface for register access

The signals coming from the sensor strips are amplified, inverted (in dependence of the operation mode), CR-RC shaped and sampled at the rate of the externally provided clock. The data samples are stored in a 192 stage pipeline awaiting read-out. Upon trigger reception the charge of a pipeline column is transferred to an APSP (**a**nalogue **p**ulse **s**hape **p**rocessor) and subsequently to a 128:1 staged multiplexer with selectable gain. A schematic view of the analogue read-out chain is shown in figure 2.12.

The memory of the APV is implemented as a ring buffer. The address of the pipeline where the data is stored is determined by an address pointer which is incremented each clock cycle. Because of the 192 stage pipeline and the LHC clock of 40 MHz, the APV can hold data for a maximum of 4.8 µs before a pipeline location is reached again and old data is overwritten. When the APV receives a trigger a certain pipeline is marked for read-out. This pipeline is protected from being overwritten until the whole pipeline column was read out. The logic of the APV allows up to 32 pipeline columns to be marked for read out. As these columns are not available for

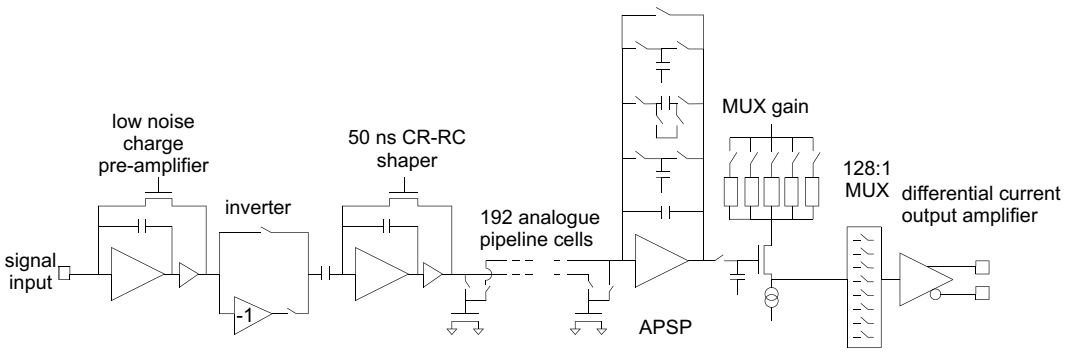


Figure 2.12: The analogue chain of an APV. The signals from the silicon strips are amplified, inverted, shaped and stored. Upon trigger reception the data from a certain pipeline column is pulse shape processed and multiplexed onto a single differential current output line with selectable gain [24].

sample storage the maximum storage time for a data sample is 160 $\times$ 25 ns at high trigger rate. The maximum possible trigger delay time is therefore limited to 4 µs which gives some margin as the foreseen delay of the first level trigger is 3.2 µs. In the running experiment the time difference between a certain event and the corresponding trigger decision will be constant. The programmable latency register of the APV allows to provide the chip with the given delay in multiples of the LHC clock cycles. When the APV receives a trigger the pipeline column containing the data of the event which caused the trigger initiation is marked for read out.
Depending on the mode of operation one or three consecutive pipeline columns are marked for read out upon trigger reception. In *peak mode* a single column is marked and a single data frame is put out. In *three sample mode*, which is implemented for test purposes only, three columns are marked and the data of each column is send out in a separate data frame. The third operation mode is the *deconvolution mode*. In this mode the pipeline column containing the sample of an interesting event plus the two preceding data samples are marked for read out. The out-put is a single data frame which contains the information of the three samples deconvoluted into one. The method reduces the effective time shaping constant from 50 ns to 25 ns and thus single bunch crossing timing resolution. In the first year of operation the LHC luminosity will be low enough to allow operation in peak mode where the signal-to-noise ratio is maximized and the non-linearity of the signal is minimized. During the high luminosity phase the deconvolution mode will be used where the time resolution is of main interest because of the high number or tracks in the detector. The three sample mode is implemented for test purposes and works like the peak mode but with an increased number of out put data samples.
The deconvolution of the data samples is done by an APSP (**a**nalogue **p**ulse **s**hape **p**rocessor) which is implemented as a three weight FIR (**f**inite **i**mpulse **r**esponse) filter. The deconvolution method is explained in more detail in [25].
The APV can drive the data output at 20 or 40 MHz. For CMS the 20 MHz output frequency will be used because the output of two APVs is multiplexed by the MUX chip and leads to an output data rate of 40 MHz per APV pair. At 20 MHz output rate

the APV needs 7 µs to send out a complete data frame which consists of 128 analogue data samples plus a preceding 12 bit digital header. Therefore the maximum average first level trigger rate the APVs can tolerate is about 140 kHz, which is well above the 100 kHz rate foreseen for the CMS level one trigger.
A typical APV data frame is shown in figure 2.13. The first three bits of the digital header called header bits define the beginning of a header. The following eight bits indicate the pipeline column the data was read from, which is of use for synchronization checks with other APVs. The twelfth bit is an error bit where a low level is used to report a problem. When no data is marked for read out the APV puts out a tick mark every 35th clock cycle. A tick mark is a single digital one which is used to synchronize the data output with the MUX chip.
Two types of errors are reported via the error bit. A mismatch between the chosen

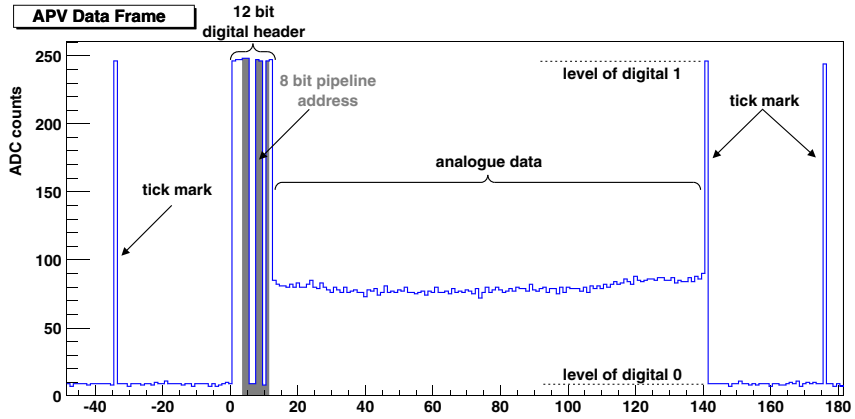


Figure 2.13: The data output format of an APV. A data frame starts with a 12 bit digital header followed by 128 analogue data samples from the APV inputs. The pipeline address and an error bit is encoded in the header which starts with three digital ones. Tick marks are sent out in fixed time intervals when no pipeline column is marked for read out.

latency and the pipeline column, which is marked for read out, causes wrong data to be assigned to a certain bunch crossing. This situation is fatal as the reconstruction of tracks will likely fail. The second error type is a fifo (**f**irst **i**n **f**irst **o**ut) error. A fifo error is reported when a trigger was sent while 32 pipelines are already marked for read out. Since both errors are indicated by the ERROR bit an error register is implemented in the chip. By access to this read-only register the actual failure type is accessible.
The APV implements an internal calibration circuit which is suited for check of the analogue chain of each input channel. As this feature is very useful for the detection of failures it is heavily used during the qualification of hybrids and modules.
The APV is controlled and monitored via 17 eight bit wide registers which are accessible via the I^2C link of the chip. The registers allow to select the operation mode, to adjust the internal calibration unit, to change the properties of the shaper etc. The complete list of registers and further information on the APV are given in the APV manual [26]. The most relevant registers for tests are mentioned below.
The basic APV settings are determined by the MODE register. The meaning of the single bits is listed in table 2.2. For most of the bits there is only one reasonable set-

Bit Number	Function	Value = 0	Value = 1
7	Not Used	-	-
6	Not Used	-	-
5	Preamp Polarity	Non-Inverting	Inverting
4	Read-out Frequency	20 MHz	40 MHz
3	Read-out Mode	Deconvolution	Peak
2	Calibration Inhibit	Off	On
1	Trigger Mode	3-Sample	1-Sample
0	Analogue Bias	Off	On

Table 2.2: The APV MODE register provides access for basic settings [26].

ting for the operation in CMS. The read-out frequency is set to 20 MHz as mentioned above, the calibration inhibit bit is set to zero, the trigger mode is „1-sample“ and the analogue bias bit is set one. The two remaining bits determine the read-out mode and the polarity of the preamplified signals. Whenever the APV operation mode is referred to the combination of these two bits is meant. In the final experiment both read-out modes are used as mentioned before. The signals of the preamplifier will be inverted as the dynamic range of the shaper is larger is this case.
Four registers are used when the internal calibration circuit is used. The ICAL register determines the amount of charge which is applied on the inputs of the APV. The eight bits of the CDRV register determine the groups of channels on which the pulse is applied. The first group are channels 0, 8, 16 and so on, the second group are channels 1, 9, 17 and so on, etc. The shape of the pulse is measured by adjustment of the timing. The gross timing in multiples of 25 ns is set by the LATENCY register. Fine time adjustment in multiples of 3.125 ns is achieved via the CSEL register.
Other registers of interest are the ERROR and the VPSP register. As mentioned before the ERROR register provides information if an error occurs, it is the unique register with read-only access. The level of the analogue output is adjustable via the VPSP register. For some tests the level is tuned to make sure that the dynamical range is not exceeded.

The I^2C bus is a field bus. Thus each device which is connected to the same controller must be identified by a unique address. The addresses of the APVs are determined by bonds which pull the address pads low. The I^2C bus uses seven bits for address selection and an eighth for selection of write or read access. The most significant bits of the I^2C address are fixed to the logical high-level inside the APV, the remaining five bits can be used for selection of unique addresses with one exception. The address where the five remaining bits are set one is the broadcast address which is used to address all APVs at once. Since in CMS each hybrid is connected to a unique I^2C controller six addresses are used only. These addresses are in hexadecimal notation 0x20, 0x21, .. 0x25. On a hybrid with four APVs the two innermost APV are not mounted and the addresses 0x22 and 0x23 are not occupied.

The initiation of actions which need to run synchronously with the externally provided clock is done by application of certain digital patterns on the trigger input line of the APV. These actions are reset (pattern 1-0-1), calibration signal initiation (pattern 1-1-0) and trigger (pattern 1-0-0). Only after reception of a reset pattern the APV the address pointers for the pipeline columns are reinitialized. For this reason a reset must be applied each time the latency is modified as latency errors are reported otherwise.

Common Mode Suppression

An intrinsic feature of the APV is the internal common mode suppression which is the tendency of the APV to compensate for the average signal on all inputs. The effect of the compensation is shown in figure 2.14. The average entry of each channel in absence of applied signals is called pedestal and indicated by the blue bars. A sample where a signal is present, shown in red is not seen at the APV output but the shifted sample shown in green is output by the APV. In other words the effect fixes the sum of all signals which are the differences between the red and the blue line to zero. For better visualisation the effect is slightly overestimated in the figure.

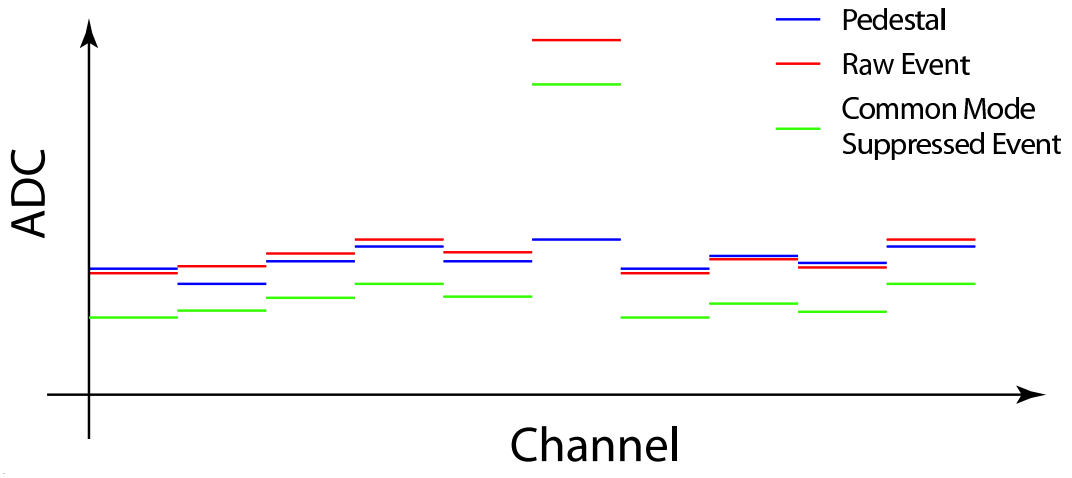


Figure 2.14: The APV internally compensates all channels for the average signal on its inputs. The scheme shows the outcome in the case of a signal which is present on a single channel. Instead of the red sample, which is present at the inputs of the APV, the sample shown in green is put out. The average entry of each channel in absence of signals is called pedestal (blue lines).

The effect is negligible if a small fraction of APV inputs see a charge equivalent to minimal ionizing particles and the total charge is small. If a larger total signal is applied to the inputs like during the calibration pulse test (see 3.6.4), the effect results in a reduced pulse height and needs to be considered in the calculation.
Most critical are very large amounts of charge. In a beam test experiment it was observed that large signals as caused by the interaction of particles with nuclei of a silicon sensor are able to disable an entire APV temporarily [27]. In this case the total signal

is so large that the other channels are shifted to the minimum possible value and the chip needs O(µs) to recover from this situation. As the whole chip is insensitive in the meantime 128 channels are taken out in this situation.
The feature is caused by the build-up of the inverter stage of the APV which is shown in figure 2.15. The 128 inverters of an APV are commonly powered via a single resistor. A large signal present only on one of the APV inputs is transferred to the to the corresponding inverter, switches it hard on and causes a voltage drop over the bias resistor. Hence the supplied voltage for all inverters is reduced. If the total input signal is equivalent to about 150 minimal ionizing particles the voltage drop is so large that the entire APV becomes insensitive to incoming signals. The calculation of the expected efficiency loss, making assumptions which were proven in lab and beam test experiments, was shown to be about 0.65 % of tracker occupancy. As the voltage drop scales with the size of the bias resistor it was proposed to reduce the resistance from initially 100 to 50 Ω. In this configuration the inefficiency drops down to 0.05 % of tracker occupancy which is negligible [28].

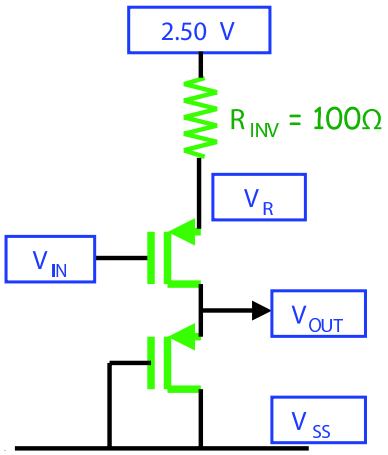


Figure 2.15: Schematic of the APV inverter stage. As the inverters of all channels are commonly powered via one resistor (R_{INV}) a large current because of single inverter causes a feedback on all other inverters. On the final hybrids the inverters are powered via a 50 Ω resistor.

2.3.2 The PLL Chip

The PLL (**p**hase **l**ocked **l**oop [29], [30]) chip decodes trigger and clock signals which are transmitted to the hybrid on a single line as shown in figure 2.16. Furthermore the PLL can delay the output of the clock and trigger signals up to 25 ns in steps of 1.04 ns. The timing precision is needed to use the full performance of the APV deconvolution mode where the plateau of the maximum signal height is in the order of a few nanoseconds (see figure 3.11). Because of the tracker dimensions it is impossible to achieve the necessary timing precision without the possibility of local time adjustment.
The most valuable information concerning the operation of the chip is provided in the

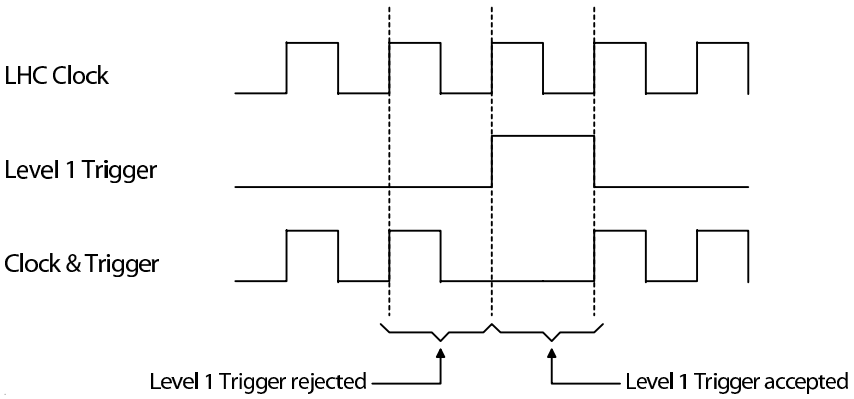


Figure 2.16: The clock and trigger information are encoded onto a single line before transmission to the hybrid. The PLL decodes the information and provides separate clock and trigger lines for the other ASICs on the hybrid. (Source [30]).

control and status register 1. The bits of most interest are summarized below:

MODE: The mode bit indicates if the PLL is running in normal mode where the operation is controlled by the autocalibration circuit of the PLL or in test mode. As the chip should not be operating in test mode a warning is given if it is active.

DISABLE T1: The bit should always be set to 0 because the trigger output is disabled otherwise.

TEST SELECT <1:0>: Both bits should be set to 0 during normal operation where trigger signals should be put out on the trigger output. If one of the bits is set the phase detector output is present on the trigger output which is only useful for test purposes.

SEU: The single event upset bit is set if the triple voting logic detects an error. Single event upsets are not expected during normal operation but may occur in a high radiation environment. For this reason the test failed if the bit is set.

FORCE PFD: The phase frequency detector bit is 0 if the phase is locked. Hence a digital 1 is seen as an error.

GOING: The going bit is set if the phase is locked. This is the default case after a normal reset sequence. If the going bit is 0 the PLL is not working properly.

At power up the PLL starts an auto-calibration procedure where a VCO (**v**oltage **c**ontrolled **o**scillator) is adjusted until the output clock frequency matches the incoming LHC clock. If the procedure finishes successfully the PLL is „locked“ and the going bit in the status register is 1. The data output of the hybrid is corrupted if the going bit is not set.
Five registers are implemented in the PLL which are accessible via four I^2C addresses (0x44 - 0x47).

2.3.3 The MUX Chip

The MUX (**mu**ltiple**x**er [31]) chip multiplexes the differential current output of a pair of APVs onto a single line. Since a hybrid carries up to six APVs the chip provides the equal number of differential inputs. The signal output rate of the pair of APVs needs to be set to 20 MHz if operated in combination with the MUX which has an output rate of 40 MHz. A scheme of the internal build-up of the MUX is shown in figure 2.17.
The MUX contains eight resistors for each input which can be switched in parallel.

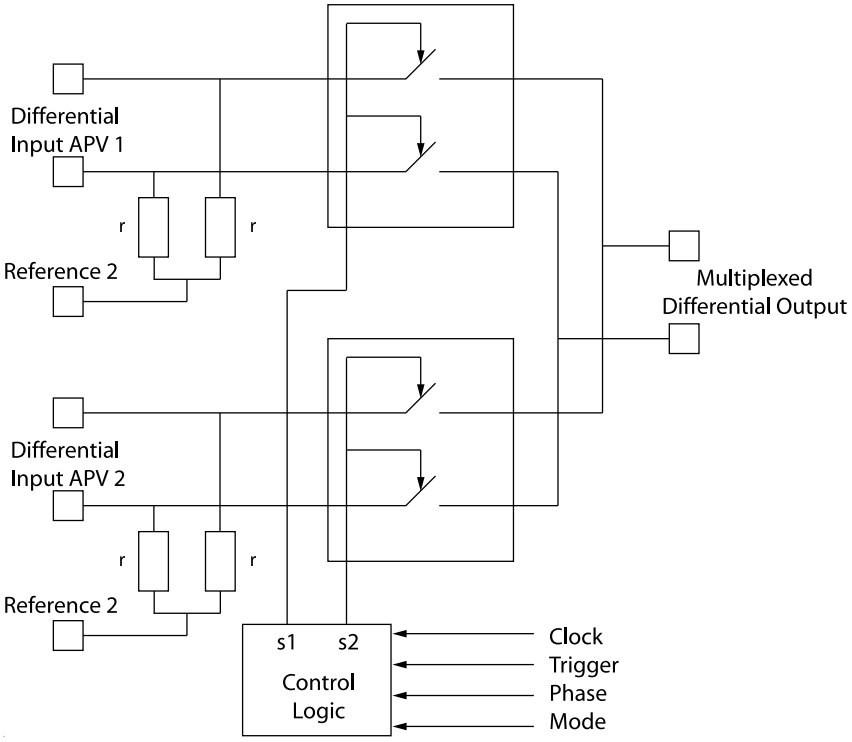


Figure 2.17: The internal build-up of the MUX chip. The amount of resistors switched in parallel determines the resistance r and thus the voltage drop over the input which is passed to the output of the chip.

The data loaded into the single register, which is assigned to I^2C address 0x43, determines the switch state for the resistors which is equal for all inputs. The more resistors are switched on the lower is the resistance and the smaller is the remaining current on the output of the hybrid.
The MUX is synchronized with the APVs if a reset pattern (1-0-1, see also 2.3.1) is applied on the trigger input. The APVs with an odd I^2C address start their signal output with a delay of $T_{output}/2$ compared to the APVs with even I^2C address.

2.3.4 The DCU Chip

The DCU (**d**etector **c**ontrol **u**nit [32]) chip monitors relevant module operation parameters. The chip has seven analogue inputs and an eighth which is connected to an

internal temperature sensor. The inputs are multiplexed onto a 12 bit ADC (**a**nalogue to **d**igital **c**onverter) which uses an internal band gap reference.
For better robustness against bit flips caused by incident particles the sampled data is stored in three different storage elements. When the sampled data is read the content of the three locations is compared and the SEU (**s**ingle **e**vent **u**pset) bit in the status register is set in case of a mismatch. The data which is read In that case the data registers contain the results which are stored in two of the three locations.
The DCU implements two constant current sources for determination of the resistivity of temperature probes. As shown in the external wiring 2.18 the DCU monitors:

- channel 0: temperature of silicon strip sensor, sensor is driven by 20 µ A constant current source
- channel 1: applied voltage on 2.5 V line of hybrid
- channel 2: applied voltage on 1.25 V line of hybrid
- channel 3: sensor depletion current
- channel 4: hybrid temperature, sensor driven by 10 µ A constant current source
- channel 5: not used, floating
- channel 6: not used, internally connected
- channel 7: temperature of DCU, connected to internal temperature sensor

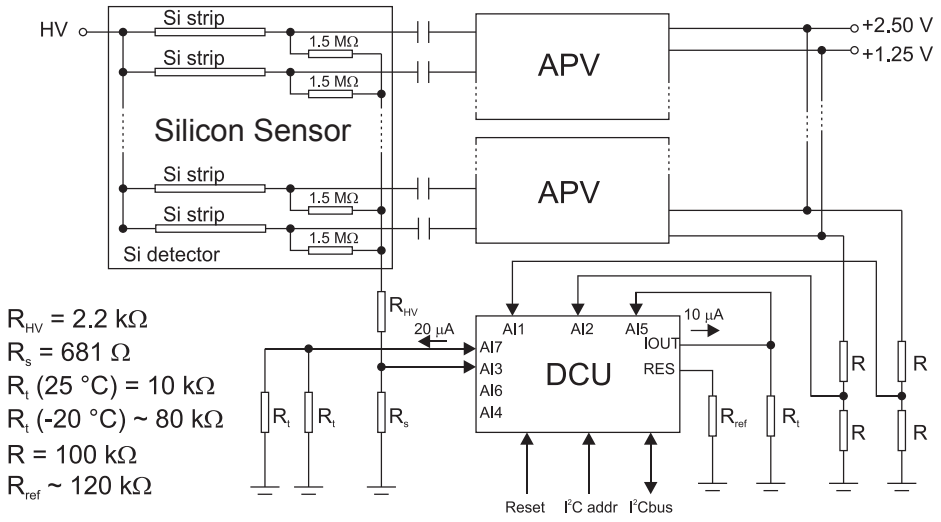


Figure 2.18: The connection of the DCU inputs with external probes for the measurement of parameters which are relevant for module operation.

The DCU provides three read-only registers. The combination of three bytes results in a unique number, the DCU ID (see also 3.19), which identifies each DCU. Since this this information is contained in many database tables for hybrid and module

tests D it is very useful for consistency checks.
In total eight registers are implemented in the DCU which are accessible via the I^2C addresses 0x0, 0x1,..0x7.

2.4 The Module Production Scheme

In this section the module production scheme is described. As an example the production flow in the TEC community is depicted in the diagram 2.19. The single production steps are identical for all modules and described in more detail below.

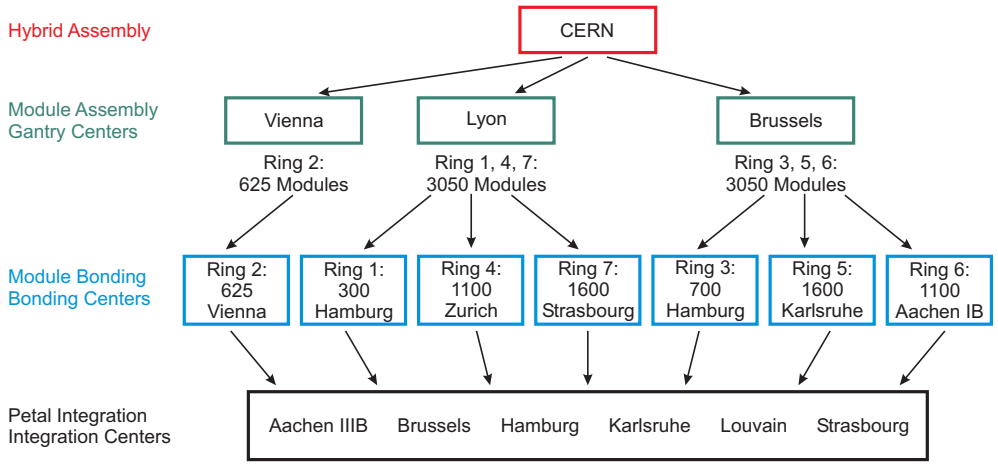


Figure 2.19: The original production flow in TEC community[7]. The single production steps is indicated by a different colour.

2.4.1 Hybrid Assembly

The circuits for the final version hybrids are produced by Cicorel[8]. From there they are sent to Hybrid SA[9] for lamination of the ceramic support piece and surface mounting of the passive components and ASICs. As the APVs are not packaged the control and power pads are wedge bonded to the circuit which turns the hybrid into an object which needs to be handled very carefully.
The electrical and functional characterization of the hybrid is done throughout the whole production. This procedure allows to spot yield relevant steps in the production chain but puts a constraint on the number of plug cycles the hybrid connector must be able to guarantee. Since the small hybrid NAIS connector is fragile and difficult to plug, a small adapter card, which simply transfers the NAIS connector to a 50 pin ERNI[10] connector, is attached to the hybrid. The adapter card stays with the hybrid

[8]Cicorel SA, Route de l'Europe 8, 2017 Boudry, Switzerland; http://www.cicorel.ch
[9]Hybrid SA, Combamare 19, 2025 Chez-le-Bart, Switzerland; www.hybrid.ch
[10]SMC - 1.27 mm (0.05") Connector System for SMT from ERNI: ERNI Elektroapparate GmbH, Seestraße 9, 73099 Adelberg, Germany. `http://www.erni.com/smcfront.htd`

until the module is mounted on a substructure, e.g. a petal (see section 1.7.2).
Pitch adapters are mounted on the hybrids at CERN. The pitch adapters consist of a glass substrate with aluminium lines and are produced by Planar[11] and RMT[12]. They are needed for adaptation of the small pitch of the APV inputs to the much larger pitch on the sensors. The pitch adapters carry the same amount of read-out strips as the sensors they are connected with in the last production step. In an addition an aluminium line is implemented which returns the high voltage. The assembly is done by a robotic assembly system called gantry. A Photograph of the gantry at CERN is shown in figure 2.20. The machine has a provision for pick up of various tools, e.g. a dispenser for glue or a vacuum chuck for lifting items. The pitch adapters are precisely positioned on top of the ceramic support piece which was prepared with a small line of glue. When the glue under the pitch adapter has hardened the APV inputs are bonded to the lines of the pitch adapter. Since pitch adapter bonding is the bottle neck in the production at CERN, pitch adapters from Planar are bonded at Fermilab. The next step is the assembly of modules.

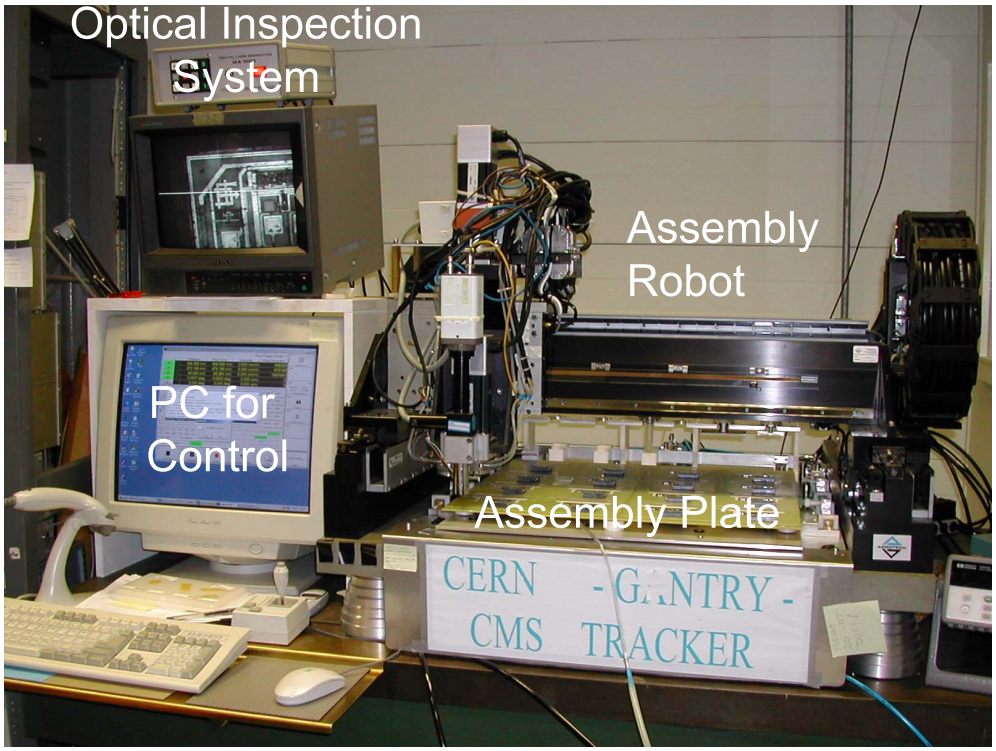


Figure 2.20: A photograph of the robotic assembly system which assembles the hybrids with a pitch adapter.

[11] Planar Systems GmbH, Airport Business Center, Am Soeldnermoos 17, 85399 Hallbergmoos, Germany; www.planar.com

[12] Reinhardt Microtech AG, Aeulistrasse 10, 7323 Wangs , Switzerland; www.reinhardt-microtech.ch

2.4.2 Module Assembly

The assembly of the modules in done by the gantry centres which use similar machines like the one gluing the pitch adapters to the hybrids. The frames are placed on fixed positions on an assembly plate, the hybrid and the sensors are lifted by special-designed tools and aligned with the help of fiducial marks which are used as reference points. The gantries guarantee a good and reproducible precision which is automatically checked at the end of the assembly. The modules stay on the plate until the glue has cured which takes about one day. As an example for the placement precision the difference between the measured and the nominal position of the sensors perpendicular to the direction of the strips is shown in figure 2.21. The RMS of the distribution is 10 µm.
As a module is delicate to handle they are mounted on a transport frame which is removed when the modules are mounted on the sub-assemblies.

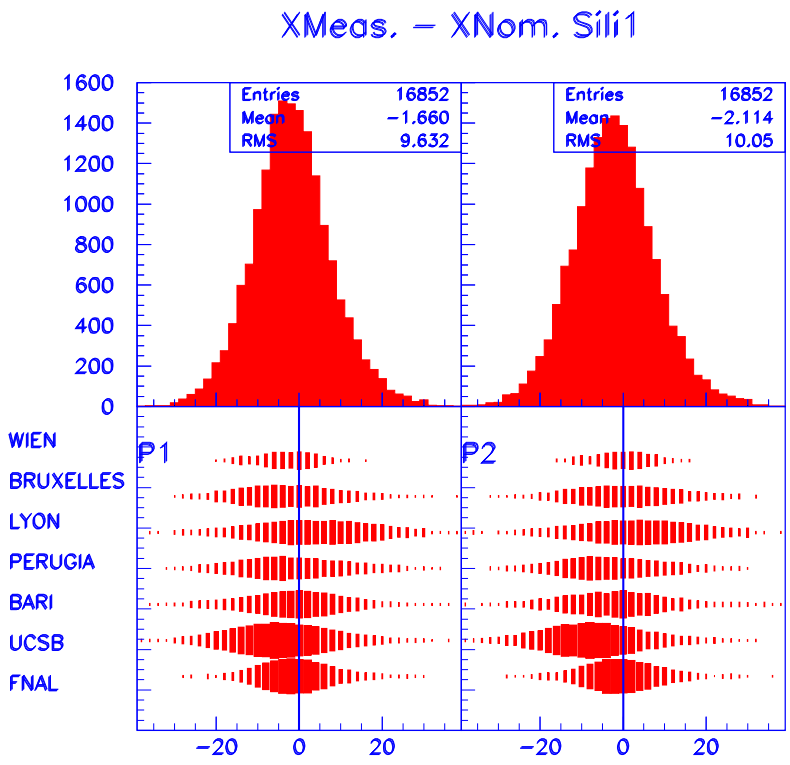


Figure 2.21: An indicator for the mechanical precision of the modules is the deviation of the sensors from the nominal position. The RMS of the data from various centres is 10 µm [33].

2.4.3 Module Bonding

The last step of the production is the electrical connection of the sensors which is done in the bonding centres. The electrical connection between the strips on the sensors and the pitch adapter lines is done by wedge bonding(read-out bonds). Additional bonds are placed between the high voltage line of the pitch adapter and the bias ring on the sensor (high voltage bonds). On modules with two sensors additional bonds are placed to daisy chain the aluminium strips of the sensors and the bias rings. For assurance of a reliable sensor backplane contact bonds are also placed between the kapton bias circuit and the sensor backplane. After this final step the modules are ready for the integration on the sub-assemblies. The various module types which are needed for the completion of the tracker are listed in table C.8 in the appendix. As an example a TEC ring six module is shown in figure 2.22.

A lot of tests are performed on the single components before they are allowed to enter

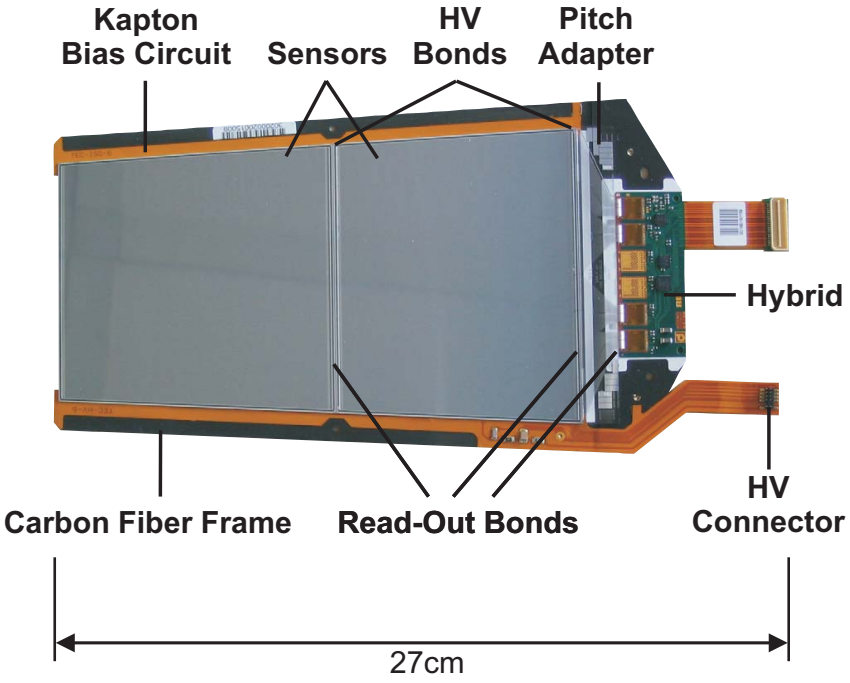


Figure 2.22: Photograph of a completed TEC ring six module.

the production chain. Even the partly assembled modules are permanently checked for early faults detection and identification of problematic steps. The read-out system which is used for the electrical characterization of hybrids and modules is described in the following chapter. The faults which were detected during the production and the single qualification steps for hybrids and modules are presented in the second next chapter.

Chapter 3

The ARC System

The ARC (**A**PV **r**ead-out **c**ontroller) system is an electrical read-out system which was developed at the III. Physikalisches Institut in Aachen. It was originally designed as a *test system* for read out of the CMS tracker hybrids which are based on the front-end read-out chip APV25 2.3.1. By the time it emerged to a test tool not only for hybrids but also for CMS tracker modules and became the official tool for the electrical and functional qualification of hybrids and modules throughout the module production chain.
Since the ARC system is integrated in all test stands, which are mentioned in chapter 4, the hardware components and the dedicated software *ARCS* (**A**PV **r**ead-out **c**ontroller **s**oftware) are described in the first sections of this chapter. For tests at tracker operation conditions a cold box control serial interface (COOLI) was developed for test stands where the temperature is reduced to $\approx$ -20°C. The COOLI device and the corresponding software *ACDC* (**A**achen **c**ooling **d**evice **c**ontrol) are described at the end of this chapter.

A complete ARC set-up consists of five different printed circuit boards. The *PCMIO card*, the *ARC board*, the *ARC front-end adapter*, the *DEPP board* and the *LEP16 board*.
In dependence of the test object it is not necessary to have a all boards. In any case the PCMIO, the ARC and the ARC FE adapter are mandatory parts for the read-out of hybrids and modules while the DEPP and the LEP16 boards are add ons for sensor depletion and sensor signal injection. The latter two boards are needed for the detailed characterization of modules. In combination with a PCMIO card they can be used as standalone tools which may be of interest for other applications.
A picture of a basic set-up is shown in figure 3.1.

The ARC, DEPP and LEP16 boards consist of a printed circuit board in double Euro format (160 mm $\times$ 233 mm) which fit into a standard 19"crate. Each board has a male 64 pin HI-CON[1] VG connector and a D-Sub9[2] male connector on its backside.

[1] HI-CON is a product of Pancon GmbH, Siemensstr.7, 61267 Neu-Anspach, Germany; `http://www.pancon.de`

[2] 9 pole connector, sub-miniature type D.

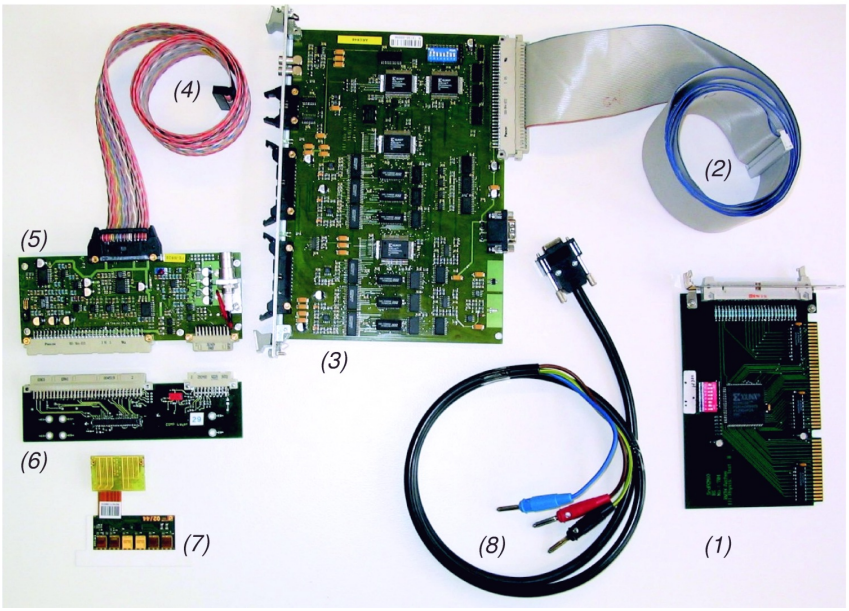


Figure 3.1: The basic ARC system consists of a PCMIO interface card (1), a 50 pin flat cable (2), an ARC board (3), a 26 pin twisted pair flat cable (4) and an ARC front-end adapter (5). The system is usually powered via a the power cable (8). The v-utri adapter card (6) exists in three versions to adapt to the different interfaces of TIB (TID), TEC and TOB modules and hybrids (7). More than 100 ARC systems were produced and distributed within in the tracker collaboration.

50 pins of the VG connector are used for communication and interface the PCMIO (**PC m**ulti **i**nput/**o**utput) card. The 14 remaining pins of the VG connector are used to supply the boards with power via a backplane. The pin layout of the VG connector of the various boards allows to use a common backplane and to operate the boards in a single crate. As an alternative the boards can be powered via the D-Sub9 connector which is the best choice for small set-ups. Each board has a selectable address which is determined by a DIL (**D**ual **In**l**i**ne) switch. As there are eight address bits 256 boards can be connected to a PCMIO card. All boards are supplied with $\pm$ 5 V and ground. The interfaces and features of the single boards are mentioned onwards.

3.1 The PCMIO Card

The PCMIO card interfaces the ISA bus of a standard PC and serves for communication with the the ARC, DEPP and LEP16 boards. The connection between the PCMIO card and the boards is established via a 50 pin flat cable with a female ribbon cable connector to interface the PCMIO card and a 64 pin VG female connector for each board. Instead of the female VG connectors the cable may have a male connector to interface the backplane of a crate that houses the boards.
The PCMIO card has a DIL switch for I/O address and communication mode selection. The I/O address has to be set to 0x300 for the operation of the ARC system with

ARCS. The communication with the connected boards can be done in two different modes. In its delivery state the PCMIO card uses the I/O access mode. In the alternative memory mapped mode the access rate is determined by the chosen wait state which allows to tune the access rate for highest tolerable access to the boards. Since this mode can cause conflicts if the access rate is too high, the usage of this mode is not recommended.

3.2 The ARC board

The ARC board is a six layer printed circuit board produced and component mounted in industry. It is a custom designed board for the read-out of CMS tracker hybrids and modules and is a further development of the PSRD[3] board which was developed in cooperation with the ETH-Zurich.
A photograph of the ARC board is shown in figure 3.2. There are two 26 pin ribbon cable connectors on the front side of the ARC board. Each one can interface a hybrid or module via an ARC front-end adapter. The LEDs (**l**ight **e**mitting **d**iodes) on the left side of each connector indicate if the connected object is powered. The expansion bus allows to daisy chain ARC boards which can share the same clock and trigger if one board is selected as master and the others as slave. Via the TRG LEMO[4] connector an external trigger can be applied. The BUSY LEMO connector provides a digital one as long as data is sampled. Both ports work with NIM compliant signals.
The great advantage of the ARC board in contrast to the final read-out, is the incor-

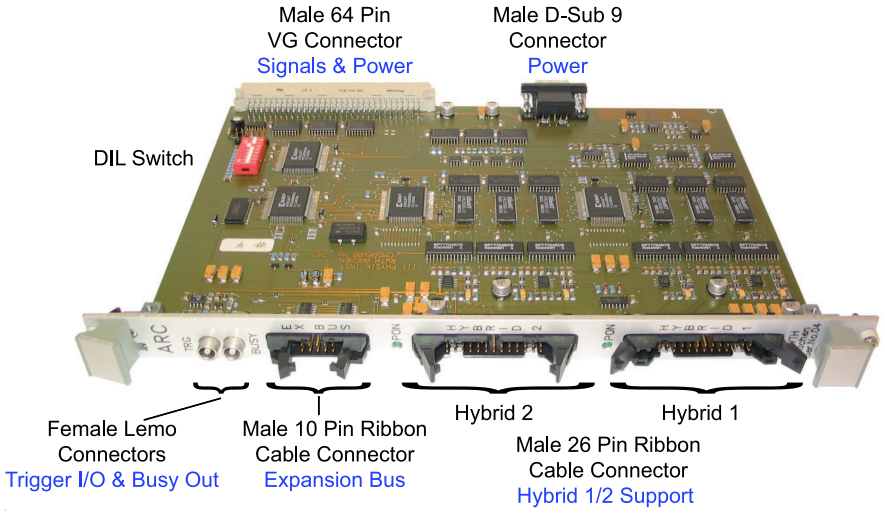


Figure 3.2: Photograph of an ARC board with description of the various interfaces. Two hybrids can be read out by an ARC board. The expansion bus allows to run multiple ARC boards with a synchronized clock and trigger.

[3]The PSRD (**p**rototype **s**ynchrotron **r**adiation **d**etector) was developed for the AMS (**a**lpha **m**agnetic **s**pectrometer) experiment [34].
[4]The connector is of type EPL.00.250; `www.lemo.de`

poration of all features needed for full hybrid support in a single card. This feature makes it a handy and robust test system for hybrid and module characterization and was one of the convincing reasons for it to become the main test tool in the CMS module production. The most important features are listed below.

- A 40 MHz *clock* is provided which is generated by a quartz oscillator.
- The *trigger* can be applied by clock missing pulses as needed by the PLL chip (see subsection 2.3.2).
- Two independent groups of three *ADCs* (**a**nalogue to **d**igital **c**onverters) with 8 bit resolution convert the hybrid output into digital data.
- A *variable offset* is added to the hybrid output signals to make use of the full dynamic range of the ADCs.
- Three I^2C *controllers* are mounted on an ARC board. Each hybrid is connected to a dedicated controller while the front-end adapters share one.

The ARC board itself needs to be supplied with 1.5 A on the +5 V line and 100 mA on the -5 V line. As the ARC board shares its power with the front-end adapters and the hybrids the total power consumption rises up to 2.5 A on the +5 V line and 300 mA on the -5 V line if two hybrids with six APVs are read out.

3.2.1 Data Acquisition

Triggers to the hybrid are sent as clock missing pulses. For this reason a trigger can only be sent synchronously with the applied clock. This synchronization is done by the ARC board and it takes two clock cycles before the trigger pattern is send out. A trigger sequencer modulates the trigger pattern which is determined by one of the eight 16 bit wide registers on the ARC board onto the clock signal. The demodulation of the trigger pattern is done by the PLL chip on the hybrid as illustrated in figure 2.16. A *trigger spacer* of 0 to 255 clock cycles can be added between the first and the second byte of the trigger pattern, which is an essential feature for tests where triggers are applied to a single APV column. The maximum number of APV triggers which fit into a single trigger pattern is six.
There are three ways to apply a trigger to the ARC board.

- A trigger is initiated by *software* if the memory address register of the ARC board is read accessed. This is the most frequently used way for the data acquisition during hybrid and module testing.
- The trigger pattern is sent out if an *external* NIM pulse is applied on the TRG connector of the ARC board.
- When the ARC board is operated in slave mode, clock and trigger have to be provided at the pins of the *expansion bus*.

The ADCs on the ARC board sample the incoming APV data non stop. When the complete trigger pattern is sent out data storage is activated and the digitized data are written into the RAM of the ARC board. There is a memory pointer for each hybrid group which points to the address of the RAM where the data is written to. The pointer is incremented automatically by one for each stored sample. The data storage is stopped when the address pointer has reached the stop address. The record length is defined by the difference between the start and the stop address. As there is one writeable stop address register for each of the two hybrid groups the stop address is software selectable and can be chosen independently for each hybrid port. When the stop address is reached on both hybrid ports, the DAV (**d**ata **av**ailable) bit is set in the status register of the ARC board. For this reason the bit is polled after the trigger pattern was sent out. When the bit is set the data acquisition is finished and the data can be read out.
Data is read out by setting the address pointer register of the ARC board to the value it was set to before the acquisition started. Each time the memory is read accessed the address pointer is automatically incremented by one and the consecutive sample is read in the following access. As the memory has a depth of 8 kbit a maximum of 8,192 data samples can be stored for each trigger pattern. The maximum number of relevant data samples is 5,040 since a trigger pattern may hold up to six APV triggers, the data frame of an APV contains 140 samples, two frames are multiplexed onto a single line and three data samples are put out when the APV is operated in the three sample mode. The difference between start and stop address is usually chosen much smaller because only a single APV trigger is contained in the trigger patterns which are used for hybrid and module tests and the three sample mode is not used for data acquisition.
As the data storage is enabled when the complete trigger pattern has been sent out, it is possible to miss a part of a data frame when the trigger pattern is long. If the trigger spacer is set close to its maximum of 255 clock cycles and an APV trigger is placed in the first byte of the trigger pattern a fraction of the APV data frame has already passed the ADCs when the ARC board is still busy sending the pattern. For hybrid and module tests the pattern is always short enough for reliable data acquisition.
The external trigger is used only when externally generated signals are applied to the sensors for instance during the LED test (see subsection 3.6.9). The expansion port is very useful when a synchronized read out of more than two modules is desired. This is normally only needed for beam tests or for the measurement of cosmic particles.

3.2.2 ARC Firmware

There are four XILINX XC95108[5] PLDs (**p**rogrammable **l**ogic **d**evices) on each ARC board. These devices contain programmable gate arrays and thus provide some flexibility for adding or changing features of the ARC board. The chips fulfil three different tasks. The *address decoder* matches the address chosen via the PCMIO bus with the correct lines on the ARC board. The *APV controller* handles the clock and trigger

[5]The data sheet is provided at: `http://www.xilinx.com/products/silicon_solutions/cplds/xc9500_series/xc9500/index.htm`

distribution and APV timing. One *ADC controller* for each hybrid group synchronizes the data sampling and memory access for the corresponding group.
The first change of the firmware was applied in mid 2002. The release concerned the expansion bus and the trigger pattern. While the expansion bus did not support any functionality before the change it was now providing clock, trigger, synchronized and APV trigger as LVDS (**l**ow **v**oltage **d**ifferential **s**ignals) signals on its pins which can be set as inputs or outputs. The feature allowed to built up the first test stand for the measurement of cosmic muons [35]. The trigger pattern was limited to 16 bit before the update and did not allow to trigger a single APV pipeline. As this feature was very desirable to test the APV analogue memory column by column, the possibility of adding a spacer of up 255 clock cycles between the first and the second byte of the trigger pattern was implemented.
A second firmware update was applied in late 2003 and concerned the backplane pulse. The possibility of adding a voltage pulse on the backplane of the sensors was expected be a useful feature to spot broken bonds and APV inputs. Experience with this test was seen as especially valuable because this type of signal injection was known to be possible even inside the tracker. The backplane pulse functionality was added at the cost of being able to switch the sampling clock for the ARC ADCs from 40 MHz to 20 MHz. As the output of the APV can be switched between 20 and 40 MHz this feature was desirable for the analysis of very early prototype hybrids where the MUX chip was missing. Since then the feature became obsolete because of the fixed data output rat of 40 MHz. The firmware change became critical in combination with ARCS versions 7.1 and 7.2 which caused hybrid initialization problems when used with boards of old firmware. The problem was corrected with the release of ARCS 7.2 beta.
All ARC boards were programmed with the most recent firmware version available at the date of shipment. As the firmware was not modified during the mass production of modules only boards with the final version should be located at the collaborating institutions.

3.3 The ARC Front-End Adapter

The FE (**f**ront-**e**nd) adapter is the interconnecting board between ARC board and test object. The connection to the ARC board is realized via a 26 pin twisted pair cable which carries power and signal lines. There are two versions of the front-end adapter as shown in figure 3.3. The early version FE adapter 3.3(a) consists of two separate boards which are connected via a flat band cable. The design was driven by the idea to leave the more power dissipating part outside the cold environment for tests at lowered temperature. This version of the adapter has a 64 pin SAMTEC[6] and a male 50 pin NAIS connector. The NAIS connector matches the connector of the hybrid while the SAMTEC connector was added upon request from people working on the FHIT test

[6]Product Series TST of SAMTEC: SAMTEC USA, P.O. Box 1147, New Albany, IN 47151-1147; `http://www.samtec.com/technical_specifications/overview.aspx?series=TST`

system which is described in section 4.1.
The adapter was redesigned because the first version was not suited for module tests, e.g. because of the missing implementation of a high voltage connector. The front-end adapter for modules FE_M has an integrated Suhner SHV connector [7] for the application of the sensor depletion voltage and two interfaces to connect all types of hybrids and modules. A 50 pin ERNI connector facilitates the connection of hybrids via a small adapter card (see also section 2.4.1). Two VG connectors form the second interface. A male 64 pin connector provides full hybrid support and a female 20 pin connector is used for sensor depletion power, access to the thermistors and the coupling capacitor on the kapton bias circuit. The connectors are arranged to interface the v-utri adapter card[8]. The FE_M was designed as a single printed circuit board (see figure 3.3(b)).
The full electrical functionality of the FE was transmitted to the FE_M which incorporates one additional IC. The key features of both front-end adapters are summarized below.

Data Buffer: The data output of the hybrid is buffered prior to the transmission to the ARC board over a twisted pair cable. The APV is not capable of driving signals over cables of a metre length without a performance loss.

I^2C Level Shift: The I^2C voltage levels need to be shifted in both directions because the digital part of the hybrid is supplied with 2.5 V which is not compliant with the 5 V high level of the I^2C bus protocol controller on the ARC board.

Hybrid Supply Voltage: The ± 5 V supply voltage from the ARC board is converted into 2.5 V and 1.25 V which are requested hybrid supply voltages. The regulation is built up discrete and protected to assure that the voltage on the 1.25 V line is always half of the voltage on the 2.5 V line to avoid reverse currents. The 5 V supply line from the ARC board carries a 2 A fuse to protect the electronics on the board and the hybrid from over currents.

Monitoring and Control: Two PCF8591 chips[9] are mounted on the adapter. The devices provide an I^2C interface and a selectable address. For monitor and control each device provides four ADCs and one DAC (**d**igital to **a**nalogue **c**onverter). One chip is used to measure the hybrid supply voltages and currents. Its DAC is used to change the nominal applied voltage by +4 % and -15 %. The other chip monitors the DCU 20 µA constant current output via a 10 kΩ sense resistor, the voltage drop over the temperature sensor on the kapton bias cable, the voltage drop over the onboard temperature

[7] Product series SHV of The Huber+Suhner Group: HUBER+SUHNER AG, Degersheimerstrasse 14, CH-9100 Herisau AR; `www.hubersuhner.com`

[8] This board was originally developed at CERN to connect TOB modules to the v-utri card which is part of an early predecessor of the CMS tracker final read-out. Similar boards were designed to interface TIB, TID and TEC modules. For this reason the chosen interface is suited for all types of modules.

[9] The data sheet is provided at: http://www.philips.semiconductors.com/cgi-bin/pldb/pip/PCF8591

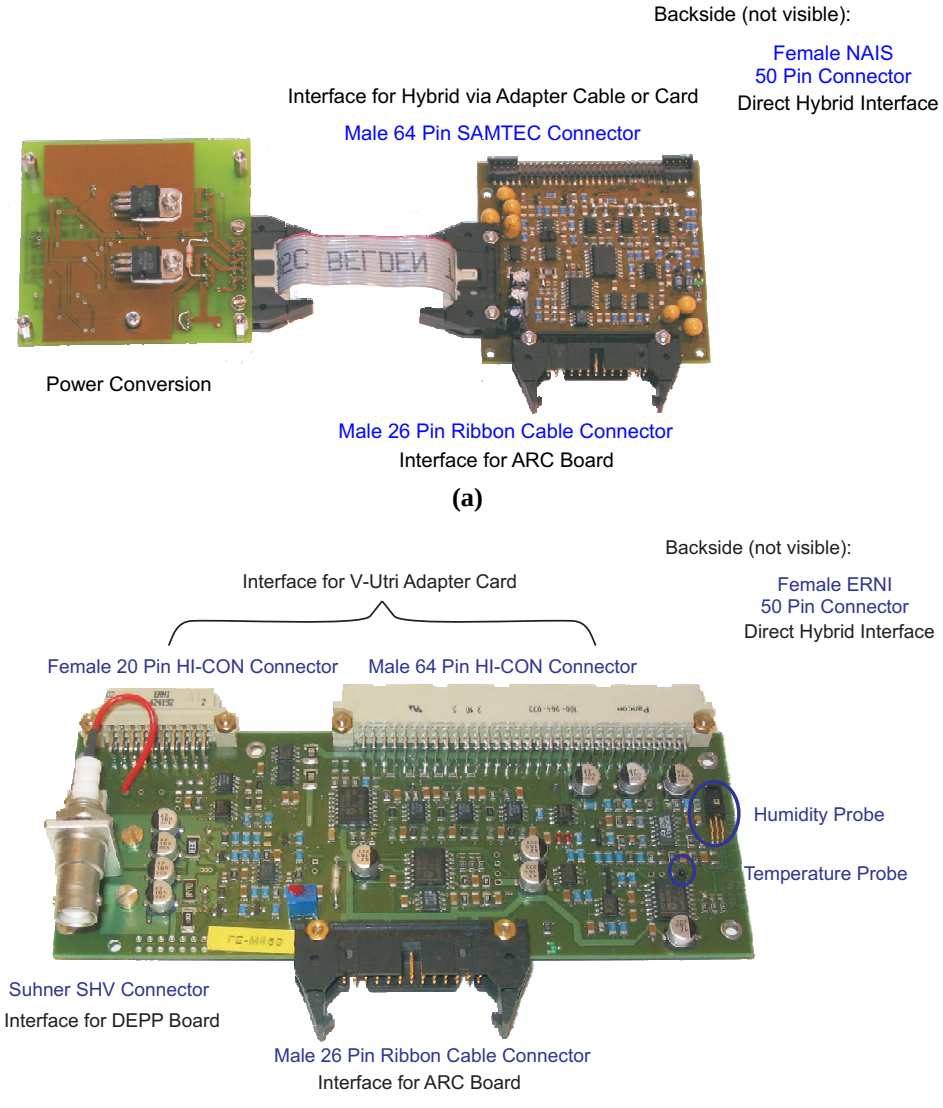


Figure 3.3: Photographs of the ARC front-end adapter. In (a) the first version of the front-end adapter is shown. It consists of two separate printed circuit boards and was designed for the test of hybrids. The redesigned adapter is shown in (b). This version is suited for module tests because of the integrated high voltage connector and a humidity and temperature probe.

probe (only FE_M) and the output of the humidity sensor (only FE_M). The DAC is used to generate a hardware reset for the hybrid. The FE_M owns a PCA9554 chip[10] which is not present on the older version. Teh chip has 8 digital I/O ports, four of them are used as inputs to indentify the hybrid type, one is used as output and enables the sensor backplane pulse[11] and the remaining three are not used.
For the correct operation of two front-end adapters on one ARC board the I^2C addresses of the PCF chips have to be adjusted. It is not allowed to connect two devices with identical address to the same bus. The test software ARCS (see 3.6) assigns the I^2C addresses 0x90 and 0x92 to the PCF8591 chips of hybrid port one and the addresses 0x98 and 0x9a to the chips of hybrid port two. The same is done with the PCA9554 chip which needs to be adapted from 0x40 to 0x4a for hybrid port 2. Solder bridges on the front-end adapter allow to change the addresses of the chips without much effort. Apart from the address changes there is no difference between the front-end adapters for port one and two.

3.4 The DEPP Board

The DEPP (**dep**letion **p**ower) board has the same dimensions as the ARC board. It consists of four layers and provides up to 600 V for the depletion of the sensors. The connectors on the back side are identical with the ARC board. Two Suhner SHV connectors are implemented on the front side for the supply of two modules. Depending on the current and voltage settings the board operates in constant voltage or current mode. The mode is indicated by LEDs beneath the high voltage connector and a signal on the mode connector. When a NIM compliant high level is applied on the kill input, the board switches the outputs off. This applies only if the feature was enabled by software which is not the default setting. The board can also switch off instead of changing into the constant current mode if an over-current is detected. This feature is not enabled until changed by software.
The maximum power consumption of the board is 1 A on the +5 V line and 0.2 A on the -5 V line. It is very important to provide the correct operating voltages. Its a known issue that a supply voltage of less than 4 V on the +5 V supply line effects the reference voltage of the board. In dependence of the nominal voltage the output voltage can rise up to 700 V in this case. A photograph of a DEPP board is shown in figure 3.4.
The voltages are generated via a 180 kHz chopper and a transformer with a ratio of 1:150. The channels of the DEPP board are independent and can source up to 1 mA each. The applied voltages and currents can be monitored during operation which is important for the measurement of the I-V behaviour of a module. A limit for the ramp up and down speed is not implemented and has to be controlled by software. The output voltage is completely decoupled from the low voltage input so that the depletion voltage is floating which is highly desirable for module tests as a source for noise because of ground loops is excluded.

[10] http://www.philips.semiconductors.com/pip/PCA9554_9554A_6.html
[11] This feature depends on the firmware version of the ARC board see subsection 3.2.2.

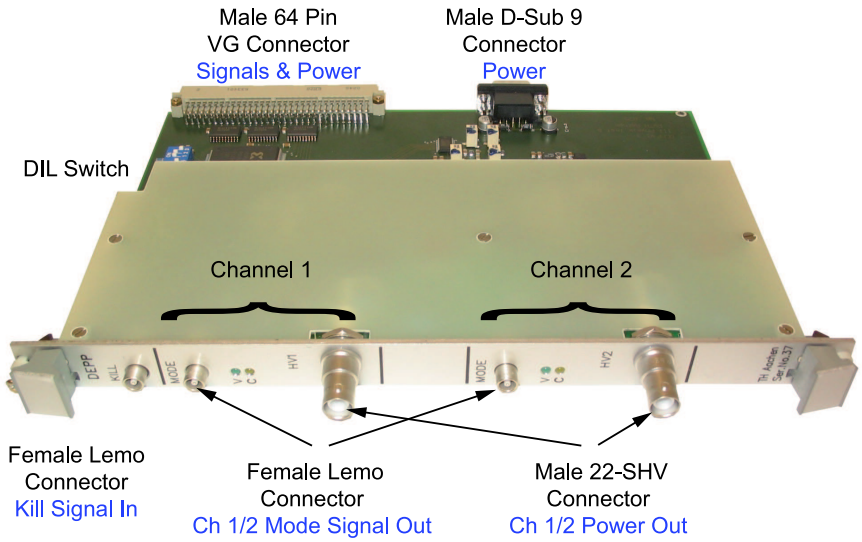


Figure 3.4: Photograph of a DEPP board. The device has an integrated current and voltage regulation and provides two independent channels. The output voltage is floating and is limited to ≈600 V with a precision of 1 V. The maximum output current is 1 mA.

The DEPP boards are calibrated manually to guarantee a deviation of less than 1 V from the nominal voltage which can be set in the range between 0 - 614 V in steps of 0.15 V. Three current ranges are supported. The best current resolution is 2.5 nA for the first range where the maximum current limit is 10 µA. The intermediate range between 0 and 100 µA has a resolution of 25 nA and the third range provides currents up to 1 mA with 250 nA resolution. As the depletion current does not exceed 10 µA for regular modules, usually the range with the highest resolution is used.

3.5 The LEP16 Board

The LEP16 (**l**ight **e**mitting diode **p**ulser)) board was designed for external signal injection on the silicon sensors via LEDs diodes. The printed circuit board consists of six layers and has the same double Euro format and back side contacts as the ARC and the DEPP boards as shown in figure 3.5. Two male 10 and 32 pin ribbon cable connectors and two LEMO connectors are the implemented interfaces on the front side of the board.

The board provides 16 current outputs which are accessible via the 32 pin ribbon cable connector. The current (LED intensity) is selectable for each output via 8 bit DACs (range 0 - 100 mA) while the width (range 25 - 3175 ns in multiples of 25 ns or infinity) is common for all outputs. When the LEP board is operated in *constant illumination* mode (pulse width set to infinity) the silicon sensor leakage current increased which is used for the pinhole test 3.6.6. In the pulsed mode fast signals are injected into the sensors which can be seen in the APV output. The LED test 3.6.9 uses this feature.
Three trigger sources are implemented:

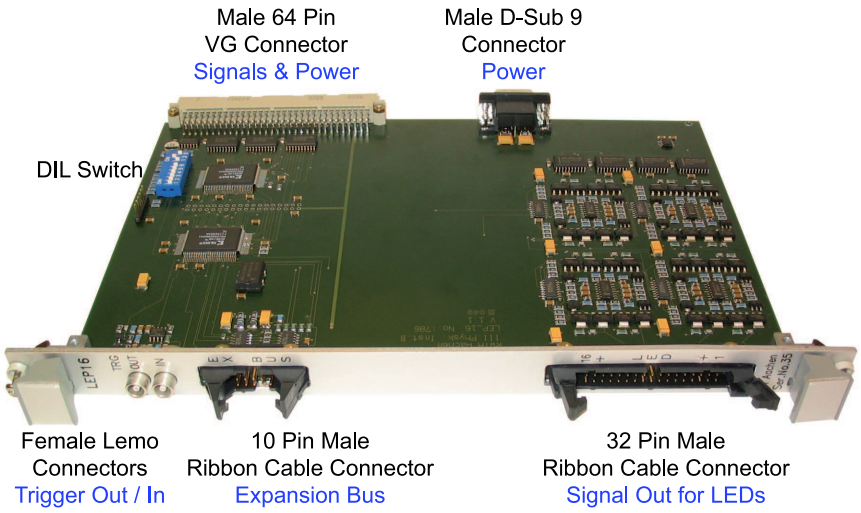


Figure 3.5: The LEP16 board was developed for external signal injection on the silicon sensors via diodes. The device has 16 outputs with selectable pulse height, width and repetition rate.

- *software* trigger - write access to a dedicated register
- *external* trigger - NIM compliant signal on the TRG LEMO connector[12]
- *autorepeat* trigger - internally generated at a selectable rate between 610 Hz and 312 kHz

For each trigger a NIM compliant signal is provided at the TRG OUT connector. The expansion bus interface is identical with the ARC interface of the same name. The ARC board the LEP board can act as master or slave and provide clock and trigger or accept it from an external source.
The LEDs are fixed in an aluminium block where the light is coupled into four optical fibres per LED. The other side of the 64 fibres are fixed to holes in a plate (fibre array) which is placed close to the sensor surface. For test purposes it is best if the total signal on a single APV is low but the signal on the illuminated strips is high. For this reason the fibres of the first LED are fixed to the positions 1,17,33 and 49, the fibres of LED two are located at positions 2, 18, 34 and 50 and so on. Because of this arrangement each APV is illuminated by a single fibre when one LED is switched on. A photograph of a fibre array is shown in figure 3.6.
The chosen design has a number of advantages compared to a system where the light of the LEDs penetrates the sensors directly.

- The electrical lines for the LEDs are far away from the sensor. Thus only the optical signal is seen in the data and not the electrical pulse.
- The light of a single LED is shared among some APVs so that the total signal for a single APV is small enough to hinder saturation effects.

[12] When the LED board is operated in slave mode the trigger may alternatively be applied via the expansion bus.

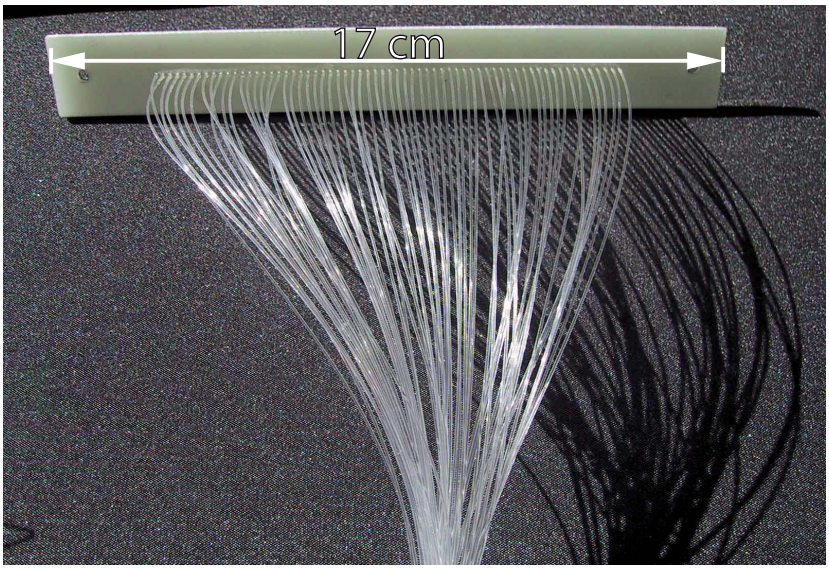


Figure 3.6: The fibres end in an array which is placed on top of a sensor. Because of the sequence of the fibres only one led spot is seen on an APV when single LEDs are switched on.

- Because of the small size of the fibres and the safe operation at little distance to the sensor surface a large signal is injected in a small number of strips which is of advantage for the detection of failures.

The LEDs chosen are of type SFH 4501 from OSRAM[13]. The diodes provide a fast signal rise time of 10 ns and a wavelength of about 950 nm. The penetration depth of the light is about 50 µm in silicon. The maximum leakage current which is achieved for constant illumination at maximum intensity is a few hundred microampere is reached. The current consumption of the LEP board is highly setting dependent. At constant illumination and maximum intensity the board draws 1.6 A on the +5 V line and 100 mA on the -5 V line.

3.6 The ARC Software

The ARC dedicated software package is ARCS (**A**PV **r**ead-out **c**ontroller **s**oftware). The ARCS code consists of two parts and was developed for the operation on Windows[14] platforms. The GUI (**g**raphical **u**ser **i**nterface) is created with LabView[15] while hardware access, data acquisition, analysis and storage are programmed in C++. The GUI is compiled into a LabView executable file which necessitates the installation

[13]OSRAM GmbH, Hellabrunner Straße 1, 81543 München, Germany, the data sheet is available at `http://catalog.osram-os.com/media/_en/Graphics/00029741_0.pdf`

[14]Windows is a registered trademark of the Microsoft Corporation, One Microsoft Way, Redmond, WA 98052-6399, USA; `http://www.windows.com`

[15]LabView is a program which is provided by National Instruments. National Instruments Corporation, 11500 North MoPac Expressway, Austin, Texas, USA; `http://www.ni.com`

of the LabView Run-Time Engine version 6.0.2 which is available for free from the National Instruments homepage. As LabView provides an interface to call DLLs (**d**ynamic **l**ink **l**ibraries), the C++ code is compiled into a DLL and thus linked to the executable program only at run time.
The ARCS DLL requires two software packages. For data analysis and storage ROOT version 3.05/02 is needed. ROOT is an object oriented data analysis framework which is written in C++. The root project was started at CERN to have a powerful data analysis tool for the LHC era. The ROOT classes are used to fit functions to data, generate graphs and for data storage[16].
ARCS provides the generation of an XML (e**x**tensible **m**arkup **l**anguage) result file. The XML file generation is done using XERCES which is provided by the Apache Software Foundation[17].
ARCS was developed between early 2001 and early 2006. The focus of the software development altered from hybrid read-out and qualification to module qualification. Earlier versions are used for the FHIT system (see 4.1) and the hybrid test station 4.2. The most important ARCS versions and the test stands they are used for are listed in table 3.1.

ARCS version	**usage**
5.1	FHIT system
6.1	hybrid rapid thermal cycler
8.1	single module test stands

Table 3.1: The ARCS versions which are used for the test stands involved in module production.

3.6.1 The Operation of ARCS

The main purpose of ARCS is the automated detection and identification of faults on hybrids and modules. A main request was a very user-friendly graphical interface and an intuitive handling so that the hybrids and modules can be tested by the technicians which are involved in module production.
The ARCS package contains the executable, the DLLs and some additional settings files. Except of the one file, named „ARCS_main_config.cfg“, the settings files should not be modified for assurance of identical chip settings and database compliant XML result files. The file which should be modified contains a number of centre specific settings like the tool id, a unique number which identifies a test stand or machine, the name of the operator, the addresses of the ARC components, the disk storage location for the result files, the tests which should be performed by default and so on.
When ARCS is executed the software automatically initializes the single boards, asks for the identification number of the test object, which can be entered via a bar code

[16] The software can be downloaded at `http://root.cern.ch`.
[17] Apache Software Foundation, 1901 Munsey Drive, Forest Hill, MD 21050-2747, USA; `http://xml.apache.org/index.html`

reader and the appropriate XML file for the execution of the tests and the data analysis (test-settings file). When this is done ARCS initializes the test object, reports the success of the initialization and displays the data frames of APVs. If the data frames look fine (see 2.13) the operator starts the data acquisition. From this moment ARCS automatically steps through the chosen tests, stored all data in a single ROOT data file and analyses it after the last test. The overall result is displayed by a green light if the test object has passed or a red light if not. The results like the bad channels and their failure type are displayed in a human readable format which is stored on disk along with a database compliant XML file. The XML file is uploaded to a central database with the BigBrowser, an application which is provided by the persons in charge of the database [36]. Because of the few interventions there is almost no chance for malpractice from the operator which is highly desirable.

A brief summary of the tests which are implemented in ARCS is given in the following subsections. More technical information, e.g. the used trigger pattern are described in [37]. The known failures and the classification of the test objects is covered in chapter 5.

3.6.2 I-V Test

The sensor leakage current versus the applied depletion voltage is measured in the I-V test. The test which is implemented in ARCS interfaces a DEPP board for control of the depletion voltage and measurement of the corresponding current. The maximum ramp up speed for the voltage is limited to 10 µA and the ramp down speed to 20 µA respectively. As the performance of the PCs ARCS is operated on can vary a lot a selectable delay is implemented in the software to adjust the ramp speed to the PC. When the desired voltage step is reached the software adds a delay before the current is read since a significant decrease is observed in the first seconds. The I-V curve of a typical module and module with bad I-V performance is shown in figure 5.14.

3.6.3 Pedestal and Noise Test

The noise plot of a module provides the fastest overview on the module performance. Typical failures like missing bonds, broken read-out lines or defects in the sensor insulation layer affect the input capacitance of the APV and thus the noise of the corresponding channel.
For the calculation of pedestals and noise software routines are used which were developed by a group of scientists before the ARC system existed. The routines were originally developed for tests with a predecessor of the final read-out. The pedestal and noise calculation of the routines is described below.
Each measurement consists of N events where a single event is indicated by the small type n. $DR_{ch,n}$ is the raw (sampled) data of channel ch in event n. The average output of a certain channel ch when no signal is present is called *pedestal* P_{ch} (see eq. 3.1).

The pedestal of a channel is essential for calculation of signal heights, e.g. when a strip is hit by an incident particle.

$$P_{ch} = \frac{1}{N} \cdot \sum_{n=1}^{N} DR_{ch,n}. \tag{3.1}$$

The typical increase of the pedestals towards higher channel numbers is a feature of the APV. The reason for the slope is most probably a voltage drop over the chip. The pedestals of a typical hybrid are shown in figure 3.7.

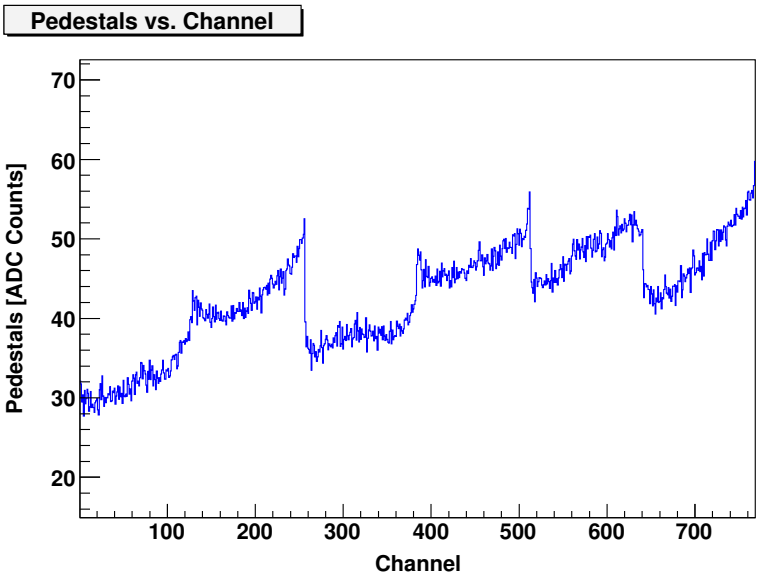


Figure 3.7: Pedestal plot of a typical hybrid. The slope of the pedestals across each APV is most probably caused by a voltage drop over the APV.

The raw signal $SR_{ch,n}$ measured for channel ch in event n is defined by the difference between the raw data $DR_{ch,n}$ and the pedestal P_{ch} of the corresponding channel.

$$SR_{ch,n} = DR_{ch,n} - P_{ch} \tag{3.2}$$

The RMS (**r**oot **m**ean **s**quare) of the raw signal is called raw noise NR_{ch}. It is calculated over a number of events N and is a measure for the deviation of the raw data from its average value.

$$NR_{ch} = \sqrt{\frac{\sum_{n=1}^{N} SR_{ch,n}^2}{N}} = \sqrt{\frac{\sum_{n=1}^{N} (DR_{ch,n} - P_{ch})^2}{N}} \tag{3.3}$$

The noise which is important for the determination of the performance of a channel is given by the common mode corrected noise. A common up or down shift of all channels is caused by current fluctuations in the silicon sensor or noise pick up from external sources. For this reason common signals are calculated for groups of channels

and subtracted from the raw signals. The common mode corrected noise N_{ch} is given by the RMS of the corrected raw signals $SCMC_{ch,n}$:

$$N_{ch} = \sqrt{\frac{\sum_{n=1}^{N}(SCMC_{ch,n})^2}{N}} = \sqrt{\frac{\sum_{n=1}^{N}(SR_{ch,n} - CM_{group,n})^2}{N}} \tag{3.4}$$

In ARCS the 128 channels of each APV are divided into four groups of 32 channels to determine the common mode $CM_{group,n}$:

$$CM_{group,n} = \frac{1}{32}\sum_{ch \in group} SR_{ch,n} \tag{3.5}$$

The number of groups and thus the number of channels per group is a compromise between best compensation of common shifts and identification of strips with exceptional noise. In the extreme case of 128 groups the common mode subtraction would take out all noise and faulty channels would not show up anymore. On the other hand a shift of a limited number of channels would not be corrected in the case of a single group.
A typical noise plot of a module is shown in figure 3.8. The applied common mode

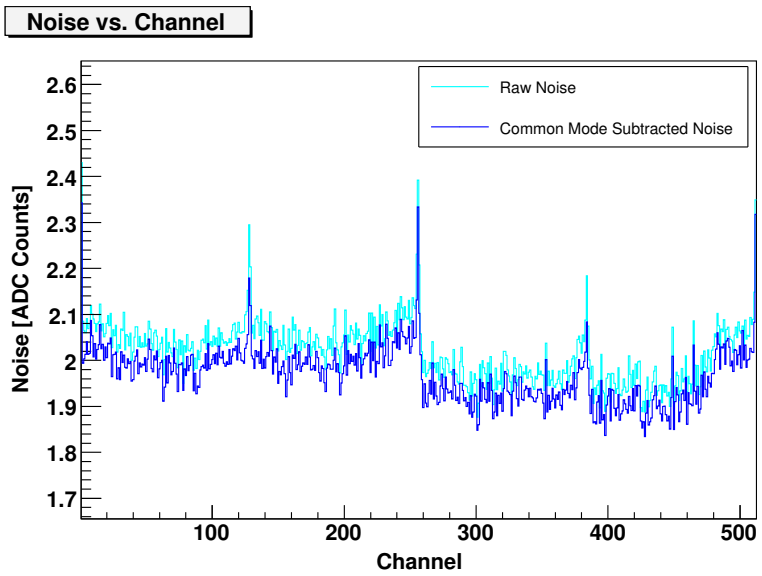


Figure 3.8: Noise plot of a typical module. The increase of the noise at the sensor edges is a feature of all modules. For this reason the noise cuts which are applied for the identification of bad strips are different for these channels.

correction is recorded in a histogram for each group of channels. The RMS of the histogram is sensitive on the radio frequency shielding and the grounding scheme of a test stand and therefore of main interest to judge the quality of a test stand (see 5.2.3). The common mode distribution of the four common mode groups of an APV and the sum of the distributions is shown in figure 3.9. The data was derived from the identical pedestal and noise test as the noise in figure 3.8.

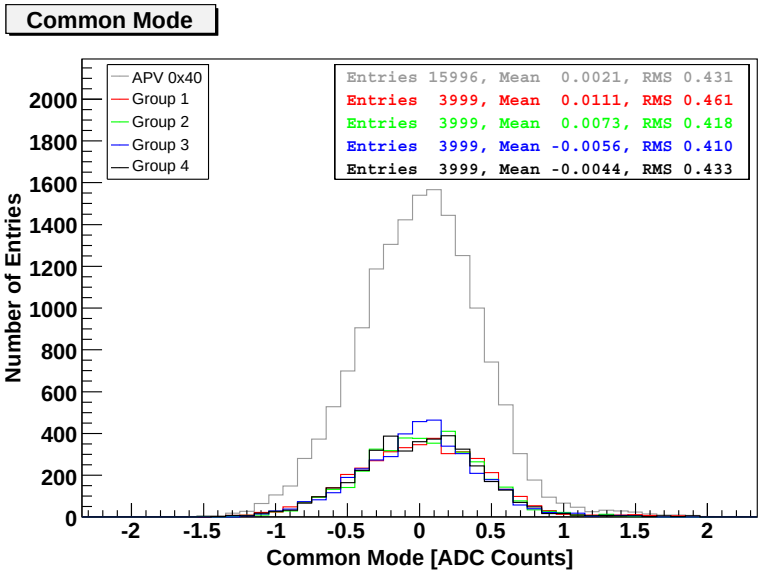


Figure 3.9: Common mode histogram for the four groups of channels of an APV and the sum of the the four distributions. The RMS of the histogram for the APV mainly depends on the radio frequency shielding and the grounding scheme of the test stand.

The principle way of pedestal, noise and common mode calculation is described above. The calculation of these values by software is somewhat more complicated because not all raw data can be kept in the memory of the PC and the influence of abnormal channels needs to be considered. In [37] it was shown that the calculated exactly noise differs less than 1 % from the noise which is caculated with the method used by ARCS if more than 5,000 events are acquired. More detailed information on the noise calculation is given in appendix B.

3.6.4 Calibration Pulse Test

The calibration pulse test uses the APV internal calibration unit which allows to inject a certain amount of charge into selectable inputs of an APV. The time evolution of the APV response is recorded and analysed in the calibration pulse test. Since the position and the height of the maximum of the pulse are sensitive to the APV input capacity, the test is very useful for the detection of certain faults.
The timing is shifted by the LATENCY and the CSEL registers of the APV. At the beginning of the test and after each change of LATENCY register the pedestals P_{ch}^{LAT} are determined. The charge is injected on a single group of channels which is selected by the CDRV register of the APV. The mean signal height of the sixteen channels the charge was applied on is calculated for ten events. For check of the cross talk between channels the same data is stored for the neighbouring and second next neighbouring channels.
The signal height for each event is given by the pedestal and common mode corrected raw data $DR_{ch,n}^{LAT,CSEL} - P_{ch}^{LAT} - CM_n$. In the calibration pulse test the common mode

CM_n is corrected APV-wise and is determined by the mean signal of the channels where no charge was injected. The common mode is significant because of the APV internal common mode suppression (see 2.3.1).

$$CM_n = \frac{1}{112} \sum_{chnosignal} (DR_{ch,n}^{LAT,CSEL} - P_{ch}^{LAT}) \tag{3.6}$$

The average signal height $\bar{S}_{ch}^{LAT,CSEL}$ for a certain timing is given by :

$$\bar{S}_{ch}^{LAT,CSEL} = \frac{\sum_{n=1}^{10} (DR_{ch,n}^{LAT,CSEL} - P_{ch}^{LAT} - CM_n)}{10} \tag{3.7}$$

After ten events the timing is modified and the next data point is measured. The pulse height versus time and the cross talk information are stored for each channel. A pulse is characterized by four measures:

- The maximum *pulse height* (PH).
- The *time offset* (TO).
- The *peak time* (TP).
- The *rise time* (RT).

The measures are obtained by an APV mode dependent function which is fit to the data. The function for approximation of the pulse in peak mode is given by:

$$f_{peak}(t) = PH \frac{t - TO}{TR} \exp\left(1 - \frac{t - TO}{TR}\right) \tag{3.8}$$

A typical pulse which was taken in peak mode and the corresponding fit function is shown in figure 3.10. In peak mode the fit is applied in the range of PT − 40 ns and PT + 100 ns where PT is the time where the largest signal was measured. The fitted data is stored in the ROOT file and used for the detection of failures. For the peak time the sum of TO and TR is stored.

In deconvolution mode a Gaussian function is fit to the data which is a good approximation at the maximum of the pulse:

$$f_{dec}(t) = PH_{fit} \exp\left(-\frac{1}{2} \frac{(t - TP_{fit})^2}{\sigma^2}\right) \tag{3.9}$$

The plot of a typical pulse and the fitted function for the deconvolution mode are shown in figure 3.11. The fit range for the Gaussian function is PT ± 20 ns. The maximum pulse height PH and the peak time TP are directly obtained from the fit. The rise time TR is set to 2.3 · σ, a good approximation as shown in [38], where σ is the standard deviation of the Gaussian function. The time offset TO is calculated from the difference between TP and TO.

The measures which are used by the ARC analysis routines for the detection of fail-

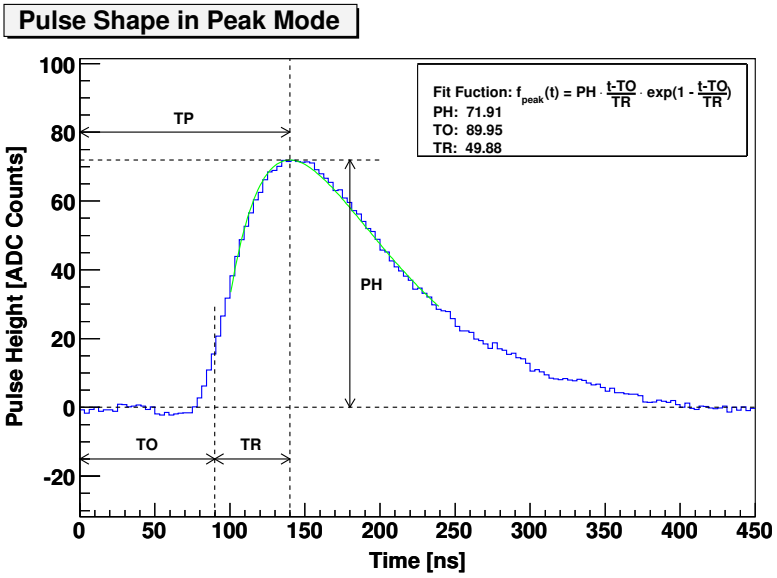


Figure 3.10: The APV response to injected signals for the peak mode. The maximum of the pulse PH, the time offset TO and the rise time RT are derived from the fit.)

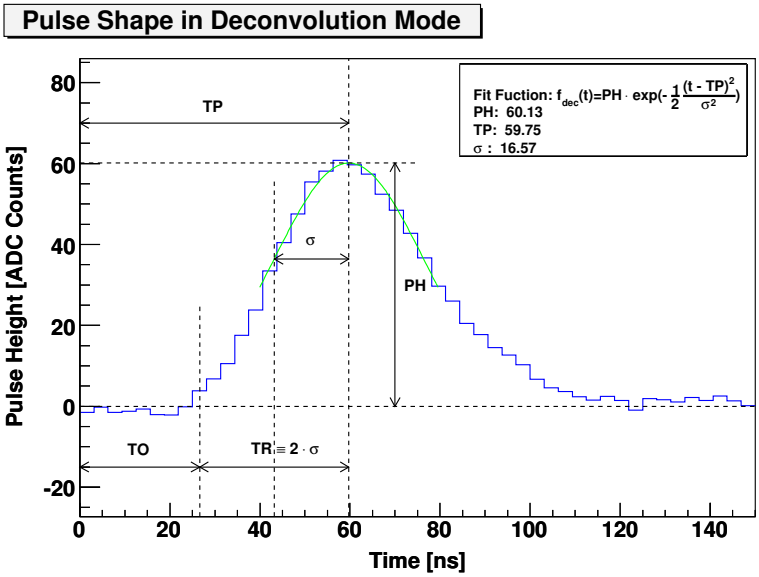


Figure 3.11: The APV response to injected signals for the deconvolution mode. The maximum pulse height,

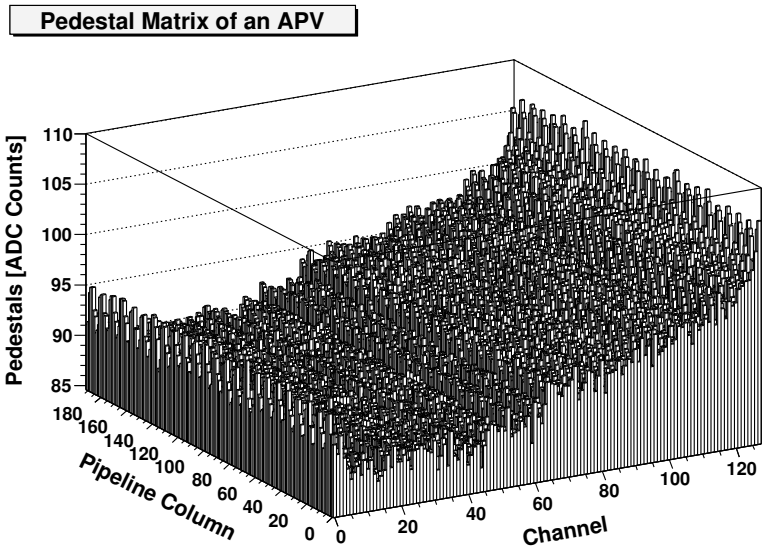
ures are PH and RT [37]. If no fit was applied because of a low pulse height or if the difference between the maximum pulse height of the data and the fit is larger than 15 ADC counts all parameters are set zero.

3.6.5 Pipeline Test

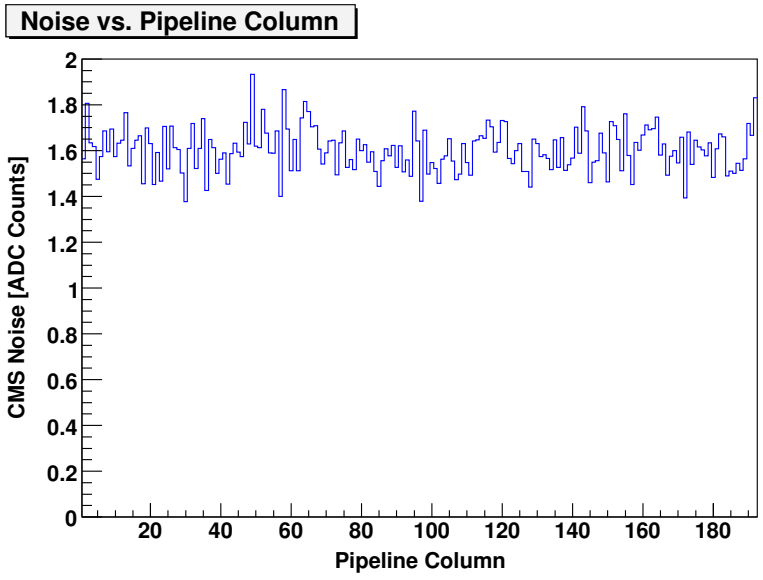
The pipeline test is designed for detection of APV pipeline dependent problems which are hidden in the results of other tests where data is always averaged over all pipeline locations. A complete pipeline or single pipeline cell can show high noise, a large pedestal offset or no response to injected signals. The pipeline test performs a pedestal and noise test for each of the 192 pipelines and performs a signal injection test on each pipeline cell. Thus the test spots all pipeline related problems. The calculation method for pedestals and noise is described in subsection 3.6.3. The response to signal injection is comparable with the calibration pulse test. In contrast to the pulse shape test the calibration pulse is measured for a single time setting in the region of the maximum pulse height.
A certain pipeline can only be triggered when the position of the address pointers of the APV is exactly known. This is the case when the APV is reset and a trigger is applied with a selectable delay. The feature is provided by the ARC board. When the first byte of the trigger pattern contains a reset sequence and the second byte contains a trigger sequence the trigger spacer governs the selection of the pipeline. The same procedure is applied for the calibration pulse part of the test where the second byte contains a calibration and a trigger sequence.
The pedestal, noise and gain data of the test can be visualized in matrices which provide an overview over all data in a single plot. A typical pedestal matrix of an APV is shown in figure 3.12(a). The size of the matrix is determined by the 128 channels and the 192 pipeline columns of an APV. The common mode subtracted noise of a single channel with respect to the 192 pipeline columns is shown in figure 3.12(b).

3.6.6 Pinhole Test

The gain of the single APV inputs versus the potential of the p-implanted regions of the strips is measured in the pinhole test. The denomination of the test is based on its potential for identification of defects of the same name(see 5.1.2).
The gain of the single channels is monitored by the response to signals which are applied via the APV internal calibration unit. As for the pipeline test the pulse applied is sampled close to its maximum and the timing is not changed. The potential of the p-implant is adjusted via the intensity of LEDs which are controlled by the LEP16 board operating in constant illumination mode. The fibres are arranged perpendicular to the strips of the module.
The potential difference V_{strip} between the hybrid ground and the p-implanted region of a certain strip is a function of the total leakage current I_{tot} and the leakage current



(a)



(b)

Figure 3.12: The pedestal matrix of an APV shows the typical increase for all pipeline columns (a). The common mode subtracted noise of a channel with respect to the various pipelines is shown in (b).

of the corresponding strip I_{strip}. The total leakage current shifts the potential of the bias ring V_{bias} via the resistors R_s and R_{HV} in figure 2.18.

$$V_{bias} = I_{tot} \cdot (R_s + R_{HV}) \tag{3.10}$$

The strip current I_{strip} causes a voltage drop V_{strip}^{poly} over the corresponding poly-silicon R_{strip}^{poly} resistor.

$$V_{strip}^{poly} = I_{strip} \cdot R_{strip}^{poly} \tag{3.11}$$

V_{strip} is given by the sum the voltages.

$$V_{strip} = V_{poly} + V_{strip}^{bias} \tag{3.12}$$

On modules with two sensors only one sensor is illuminated. Hence the p-implanted regions of sensor which is not illuminated is affected by the potential shift of the bias ring only. The leakage current which is monitored by the DEPP board reaches typically somewhat more than 300 µA at maximum LED intensity. For safety reasons the DEPP board limits the current to 500 µA. This precaution avoids exceptionally high sensor current densities which might apply stress. The minimum potential shift V_{min} for all strips is given by:

$$V_{\text{min}} = 300\ \mu\text{A} \cdot (2.2\ \text{k}\Omega + 0.68\ \text{k}\Omega) \approx 0.86\ V \tag{3.13}$$

For the detection of pinholes this shift of the potential is sufficient (see 5.1.2).
The APV output versus the LED intensity is recorded for each channel. A typical example is shown in figure 3.13.

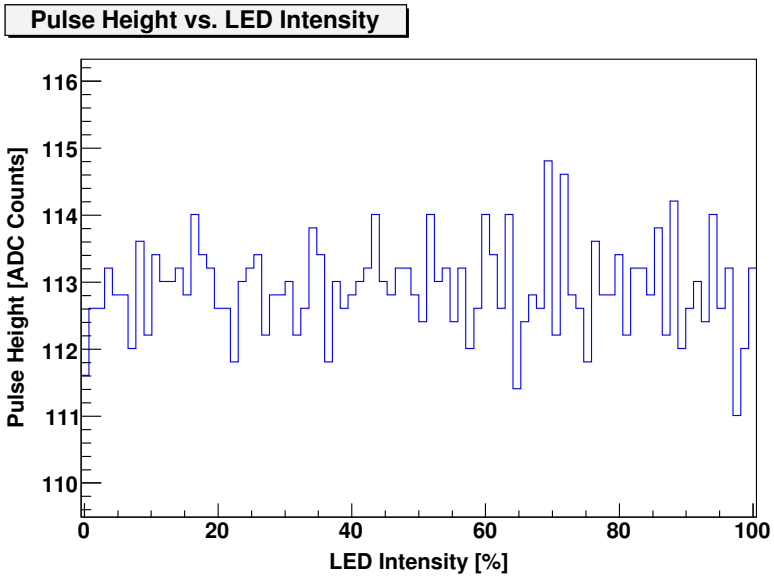


Figure 3.13: The signal height versus the LED intensity is recorded in the pinhole test. The behaviour of a typical channel is shown in the plot.

3.6.7 Gain Test

The APV internal calibration unit permits to apply a certain amount of charge on the APV input. Like for the pinhole and the pipeline test the evolution of the pulse is not of interest but the height at a fixed position in time in the region of the maximum of the pulse.
The amount of injected charge is controlled by the ICAL register of the APV. The test starts at ICAL 0 and stops at ICAL 100 with a step width of 10. The amount of injected charge is 625 electrons per ICAL unit which corresponds to a maximum charge of 62,500 electrons and equals 2.5 MIPs[18]. Since the APV is known to have a constant gain up to five MIPs a linear fit is applied to the data which is described by a slope SL and an offset OFF where the value $ICAL$ of the ICAL register is zero.

$$f(ICAL) = SL \cdot ICAL + OFF \tag{3.14}$$

The plot of a typical channel is shown in figure 3.15(a) The signal height is calculated

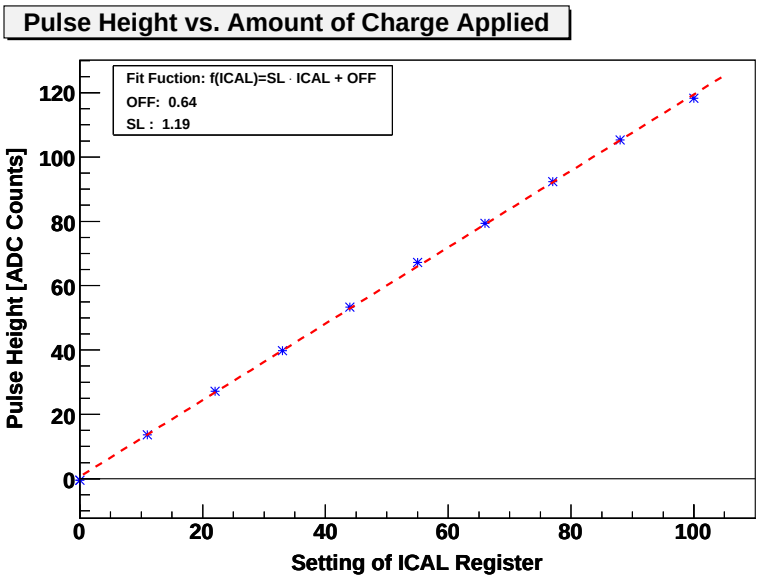
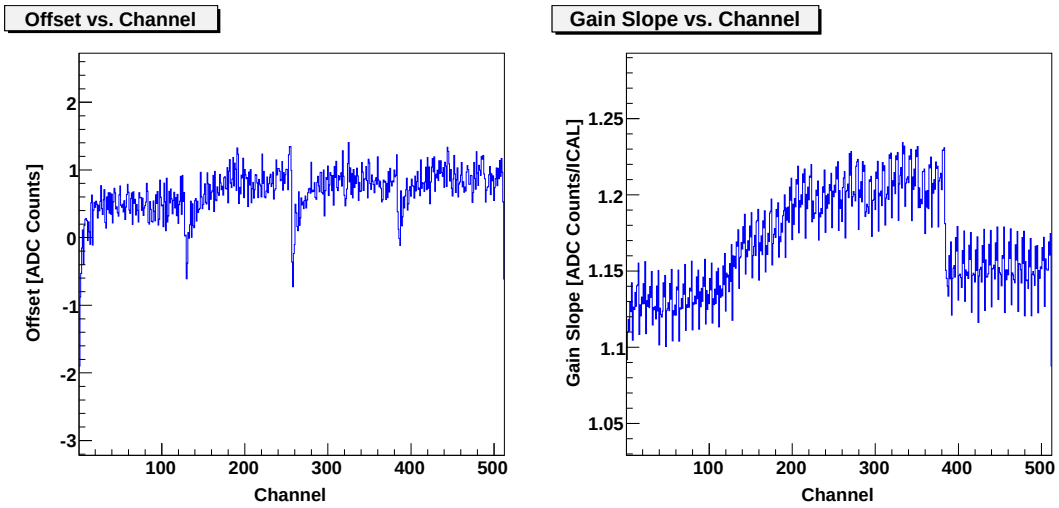


Figure 3.14: The increase of the pulse height versus the setting of the ICAL register of an APV. The register setting transfers linearly to the amount of charge applied. A straight is fitted to the data as the APV response is linear for the chosen amounts of injected charge.

in the same way as in the calibration pulse test. Large signals have a non negligible influence on neighbouring channels which are therefore excluded from the common mode calculation in equation 3.7.
The slopes and offsets of a typical module are shown in figure 3.15. The height of the output signal depends on the gain of the APV, the amount of injected charge and the input capacitance of the APV. For this reason the test is sensitive to defects where the

[18] A minimal ionizing particle produces about 25,000 electron - hole pairs in a silicon sensor of 320 µm thickness.

APV input capacitance is affected but also to gain inhomogeneities.



(a) **(b)**

Figure 3.15: The fitted data of the gain test. In (a) the offsets of the fitted straights are shown which are nearly zero. The APV gain is given by the slope of the straights which is plotted in (b).

Like for all tests the parameters for the gain test are determined by the test-settings file. For instance three parameters for the gain test are the starting and end values for the ICAL register and step width. It is worth to know that whatever values are chosen for these parameters, the maximum value for the ICAL register is internally limited to 150 because of the risk of exceeding the dynamic range of the ARC ADCs and the expectation of a linear response.

3.6.8 Backplane Pulse Test

A coupling capacitor for signal injection into the high voltage line is integrated in the module kapton bias circuit (see figure 2.9). When a pulse is applied on the coupling capacitor the potential of the sensor backplane changes and a signal is coupled into all sensor read-out capacitors. The ARC board provides a pulse of $\approx$ 2 V and 10 ns rise time each time a trigger is initiated. The pulse is applied on the coupling capacitor if this feature is enabled by a chip on the FE_M adapter. The backplane pulse test records the time evolution of the APV response in steps of 25 ns.
The applied pulse is seen as a common signal by all APV inputs except of those where the electrical connection to the sensor read-out capacitor is broken. Because of the internal common mode suppression of the APV (see 2.3.1) these inputs show a response which is of opposite polarity in contrast to the common signal.
The response of a typical channel is depicted in figure 3.16(a). The integrated response of the single channels is shown below. The integral of a channel which is disconnected

from the read-out capacitor is positive.

The feature of direct signal injection on the sensors without the need of additional

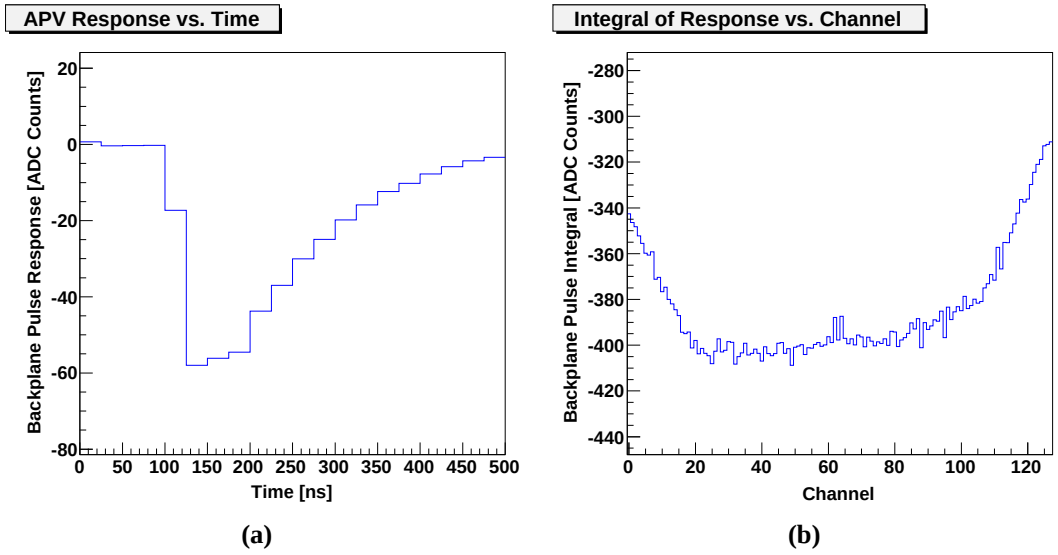


Figure 3.16: The time evolution of the response to an injected backplane pulse is shown in (a). The integral of the signal for the channels of an APV is shown in (b).

equipment is a great advantage of the test. The backplane pulse offers the possibility of signal injection even in the CMS tracker since the needed lines to the coupling capacitor are foreseen and the pulse can be generated by the CCU (**c**ommunication and **c**ontrol **u**nit [39]), the front-end chip which is in charge of clock, trigger and I^2C signal distribution.

3.6.9 LED Test

When the LED pulser (see section 3.5) is operated in pulsed mode, signals can be applied to the APV via the silicon sensors. During the test one LED is pulsed at a time. Since each LED couples infrared light into four light guides up to four light spots become visible in the output of the tested module. As the intensity profile of the light spot is Gaussian so is the APV response across the input channels.

The ARC board is set to external trigger mode for the data acquisition because the trigger for the APVs needs to be synchronized with the LED board trigger. When the TRG output of the LEP16 board is connected to the TRG input of the ARC board the LED trigger is automatically transferred to the ARC board. It is not necessary to synchronize the clocks of the boards via the expansion bus because the signal on the sensors does not change noticeably during 25 ns. The LED board is operated in autorepeat mode and thus the ARC DAV bit is polled to check for available data.

During a LED test 16 data sets are taken, one for LED of the LED array. A single data set contains the average raw data for each channel which was gained in 100 events. The analysis of a data set is done for single APVs as the signal height does not transfer smoothly across APV edges. First a Gaussian function (see equation 3.9) is fitted to

the average raw data. The fit range is given by the channel with the highest entry $\pm$ 20 channels. As the width of the led spot is unknown for the first fit a second fit is applied with a modified width of the fit range. The width for the second fit is $\pm$ 1.3 $\cdot$ σ where σ is the standard deviation of the Gaussian function of the first fit. The average raw data and the second fit function of a single data set are shown in figure 3.17(a).
The procedure is not useful if a LED spot hit only the border channels of an APV because a fit is likely to fail in this particular case. For this reason the χ^2 of the fit is checked if the channel with the largest signal is found on one of the four outermost APV channels. If the χ^2 is exceeds 30, the fit is assumed to have failed and a linear fit is applied instead. If the slope of the straight is correct which means negative on the left APV border or positive on the right one and the χ^2 of the fit is lower than 30, the linear fit is used as an approximation of the data up to the channel where the result becomes negative. The data of the remaining channels is set to zero.
In figure 3.17(b) the fit functions to all data sets of an APV and the envelope of the functions are shown. The envelope describes the expected maximum response of the channels because of the typical profiles of the LED spots. The number of fits is less than 16 as the fibres of some LEDs are not located on top of the channels which are connected to the APV shown in the figure.
For comparison of the expected and the current maximum response of the channels the envelope of the fit functions and the envelope of the raw data sets are plotted in figure 3.17(c). The measure which is used for identification of bad strips is the difference between the envelopes. It is shown in figure 3.17(d). The difference is only few ADC counts for typical channels with a tendency to slightly higher values at the APV edges where the data is not described as well as in the centre. A difference of more than ten ADC counts is seen as an indication for an APV input which is disconnected from the corresponding strip or an input with low gain. The various failures are described in section 5.1.

3.6.10 Fast Test

The fast test was designed to check the basic functionality of a hybrid or module within short time. For this reason it is used in combination with the FHIT system (see 4.1) where testing time is very limited. By the time the test became more and more sophisticated. In the final version all known chip specific problems are checked for and an exact error description is given.
When the test is started interesting information like the status of the test and the test results are immediately displayed in a message box. Like all other tests the fast test results are stored in a ROOT file but in contrast to the other test also an ASCII file is created which contains the text of the message display. This feature is very useful to get a quick overview over the fast test result. The early version of the fast test which is used for the FHIT system does not support data storage in root files. Data is stored in a second ASCII file instead.
The final version of the fast test is divided into nine individual tests, which are selected or deselected by check boxes in the GUI which is displayed in figure 3.18. The squared

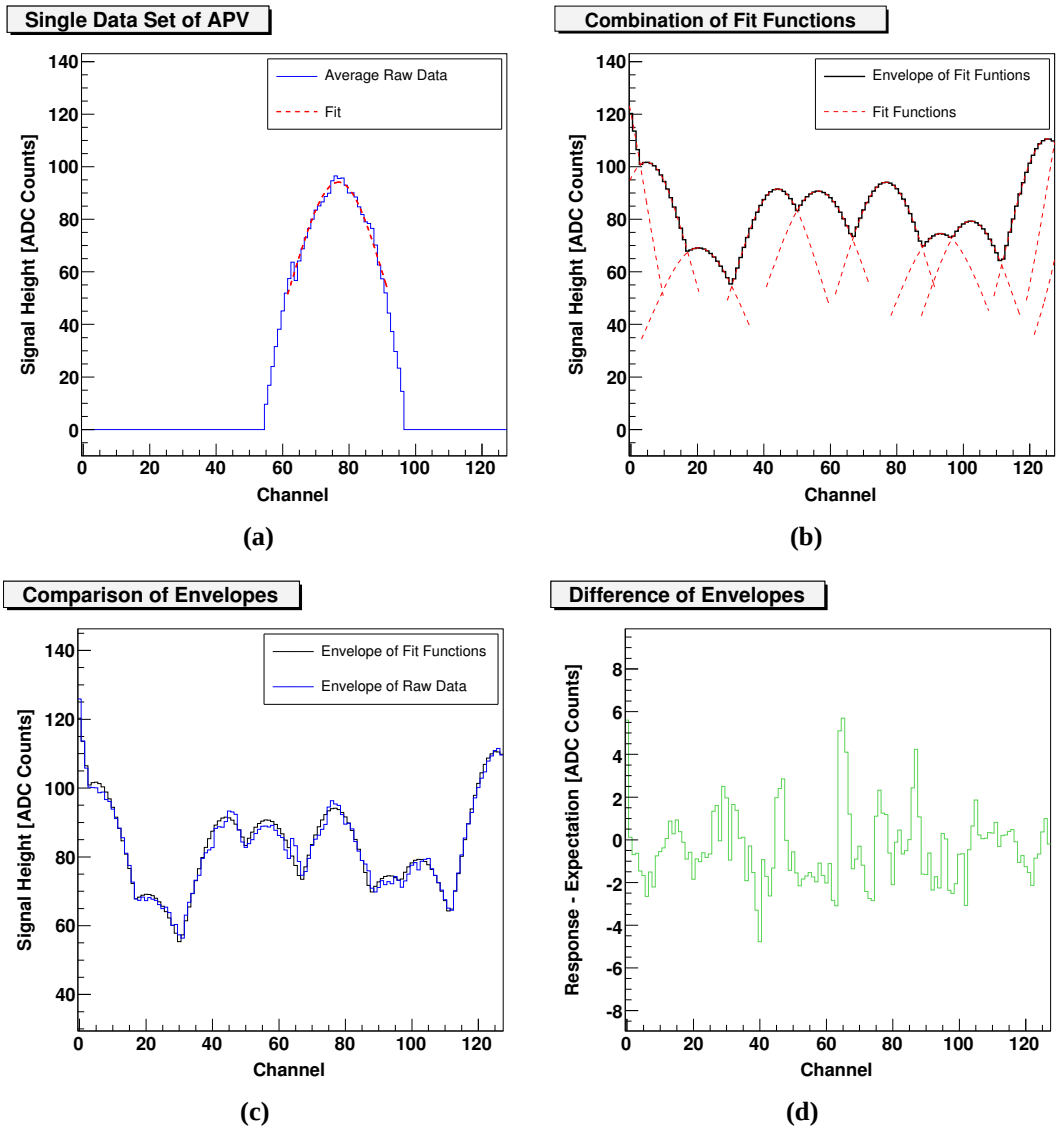


Figure 3.17: The data acquisition and analysis procedure for the LED test. First a Gaussian function is fit to describe the average raw data of each LED signal (a). The envelope of all fit functions is seen as the expected maximum signal output of each channel (b). The expected output and the maximum measured average raw data are shown in (c). The indicator for bad channels is the difference of the data in (c) and shown in (d).

boxes indicate the results of the each check. A green box indicates a passed check, the colour is orange if a non fatal error occurred and red if the test was not passed. The overall test result is mirrored by the indicator for the grade of the object.
The implemented test are:

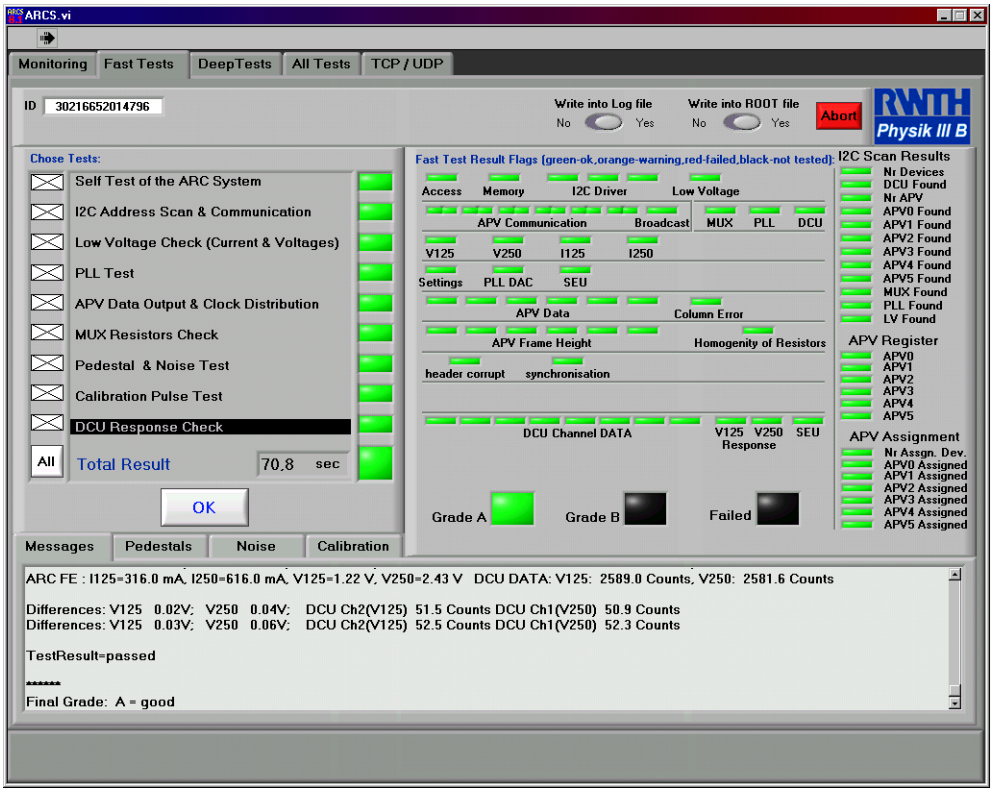


Figure 3.18: Screenshot of the fast test panel of ARCS. The tests are selected via the check boxes on the left hand side. Each test has big squared indicator which views the overall result of each test. The small squared boxes on the right indicate the the result of the single sub-tests within the individual tests. The text output of the tests and the results are displayed in the bottom window.

1. self test of the ARC system
2. I^2C address scan and communication
3. low voltage check
4. PLL test
5. APV data output & clock distribution
6. MUX resistors check
7. pedestal and noise check

8. calibration pulse check

9. DCU response check

The sequence of the tests is more logical compared to the early version of the test and the origin of an error can be exactly traced back.
The importance of the final fast test is grounded on its central role for evaluation of the readiness of modules for integration on the sub-assemblies. In TEC collaboration a quick test is performed before the modules are mounted on the petals (see 5.2.3). The check consists of an I-V test and a fast test which is the final instance for the judgement of the electrical and functional quality of single modules. For this reason the final fast test was designed for high sensitivity on the known failure modes of the chips on the hybrid. The individual tests are described below.

1) Self Test of the ARC system

The ARC self test is the only test which cannot be deselected because it guarantees the reliable operation of the ARC system. If the test fails all other results would be meaningless. For this reason the self test is also performed right after the execution of ARCS before the test object is accessed.
The self test starts with an access test of the status register of ARCS. The status register contains several bits which can be read and write accessed. The communication check accesses only those bits of the status register which will not influence the test object. Two different patterns are written to the board and read back in total 1,000 times. If the read back value does not match the written value the test failed. At the end of the communication check the initial status of the board before the check is restored.
The ARC memory access is checked in the second step. Like the status register the memory of the ARC board is read and write accessible. Three tests are performed to check if all memory locations are accessible and each bit can hold a digital 1. For this reason the three 13 bit wide and 8 bit deep memory chips are filled with running numbers. If the correct numbers are read back the memory is completely addressable. The second test writes the pattern 0x55 and the third the pattern 0xaa to all memory locations. If the correct patterns are read back the memory test is passed. In principle many more tests could be done but here only the basic functionality is checked to save time.
The communication with the ARC front-end adapter and the chips on the hybrid is done via I^2C controllers from Philips[19]. Access to all of the three ICs is essential to monitor and control the settings of the chips on the hybrid. The PCF8584 chip[20] supports three different parallel bus protocols. The selection of the protocol is done by the first sequence of signals on two input pins. If the chip is not operated in 80XX mode it cannot be accessed and the power to the ARC board needs to be switched off

[19]Royal Philips Electronics; Philips head office, Amstelplein 2, 1096 BC Amsterdam, The Netherlands; `http://www.philips.com`

[20]The data sheet is provided at: `http://www.philips.semiconductors.com/cgi-bin/pldb/pip/PCF8584`

to reset the Chip. Since the chip keeps its mode even at a very low supply voltage it is necessary to remove also the flat band cable to the PC. When the chips are accessible they are initialized to communicate with a clock frequency of about 90 kHz.
The self test is passed finally when also an ARC front-end adapter is found. Depending on the type of front-end adapter two or three chips should send an acknowledgment in an I^2C address scan. The test object is not affected by the scan because there is a separate controller for each hybrid port on the ARC board. The scan is performed with the third one which is only used for communication with ARC components. If no chip responds to I^2C communication the test failed because a test object must be interfaced through an adapter.

The following step depends on the test which is performed next. If no additional test is chosen the fast test ends at this point. For additional tests the power to the hybrid is switched on if this was not already the case and an I^2C address scan on the hybrid I^2C link is done. Two more actions are necessary to allow certain tests. The registers of the APVs are set to fixed values to get comparable results and an assignment of APV outputs to the corresponding read-out channel is needed. The assignment is done once while the APV register settings need to be reloaded after an assignment since the registers of the APVs are modified by the procedure.

2) I^2C Address Scan and Communication

The I^2C address scan and communication test proves the reliable I^2C communication with all chips on the hybrid. The full I^2C address range is scanned 10 times and the found addresses are assigned to the corresponding chips. The test fails if the number of found addresses is not constant during the scans or if the DCU, the PLL or the MUX are not found. Furthermore all APV addresses must be found and the number of found APVs must match the number of APVs expected from the hybrid or module type.
When the scan is finished the communication with each chip is checked. The read and write accessible registers of each APV are written and read ten times. At the beginning the initial register settings are read for restoration of the initial settings at the end of the test. An error is reported if the a chip does not send an acknowledgment or the read back register data does not match the data written.
The check of the communication with the MUX is done next. When the initial register setting is stored the 256 possible settings of the 8 bit register are written and read back. Missing I^2C acknowledgments or a mismatch of written and read back data causes an error message and a failure of the test. At the end of the test the initial value is restored.
The PLL communication is checked by read access. Each of the five registers is read three times. The read access includes a write access because the PLL has four I^2C addresses but five registers. A bit in the status and control register is used to select between two registers which are accessible on a single I^2C address.
The initial value of the DCU control register is read next. Whenever a register of the DCU was written, it is read back again to check if the data match. The control register is filled with all values between 0x8 and 0xf ten times and afterwards the auxiliary

register undergoes the same procedure but the data ranges from 0x0 to 0x8. The communication check ends by switching the band gap reference on and off ten times. If the DCU sends the expected acknowledgments and the written and read back data always match the DCU communication check is passed.
During the test a few 1,000 read and write accesses are performed to assure reliable I^2C access to all of the chips on the hybrid.

3) Low Voltage Check

The power dissipation of the hybrid is used as an indicator whether all chips and passive components are working correctly. The first implementation of the test did the measurement of voltages and currents when no trigger is applied to the hybrid. This was changed when it was found that the power dissipation increases by at least 10 % when triggers are applied. Since triggers are applied during standard operation of the hybrid the power dissipation under working conditions is used for grading.
When the test is started the APV registers are set to fixed values. This is inevitable because the current consumption of the chips is correlated with the register settings. The measurement of the power dissipation without trigger is done first then 500 triggers are send and the currents and voltages are measured again. As the trigger frequency is much higher than 10 Hz the power dissipation is measured in a regime where no dependence on the trigger frequency is expected [40].

4) PLL test

If the PLL works properly clock and trigger signals are present on the corresponding inputs of the APVs and the MUX. According to the PLL manual [30] this is the expected behaviour after a hard or software reset is applied. Since the ARC system generates a hard reset when the hybrid is powered up, the chip should be in the correct state and work properly. The state of the PLL is indicated by certain bits in its status and control register 1. For this reason the main task of the PLL test is to check if the register settings are as expected and to bring the chip into the correct state in case of problems.
The expected settings after the successful initialization of the chip are given in the subsection on the PLL chip 2.3.2. If the register settings of the PLL indicate no problems the registers which determine the setting of the DAC for the VCO (**v**oltage **c**ontrolled **o**scillator) are read. The DAC is set automatically during the auto-calibration procedure of the chip at start up which is known to fail on a fraction of chips when operated at low temperature(see 5.1.1). The DAC setting at ambient temperature might be useful to derive the correct settings at low temperature where the register is loaded manually to overcome the initialization problem.
The functionality of the PLL clock and trigger delay is checked in the subsequent test where the APV data output is analysed.

5) APV data output & clock distribution

The data frames which are put out by the hybrid should look like the data in figure 2.13. The aim of the test is therefore to find APVs with a correct output and to assign the data frames of an APV to an ARC read-out channel.
While the APVs are usually operated in one sample mode where one data frame is sent upon trigger reception, a single APV can be identified by switching it to the three sample mode where three frames are sent out. For this reason single APVs are set to the three sample mode and the detection of the specific data output allows the assignment to a particular ARC read-out channel. The number of assigned APVs must match the number of APVs which is given by the selected test object type at the start up of ARCS. Since the mode is selected via the mode register of an APV which is accessed through the I^2C addresses of the corresponding APV, I^2C addresses are effectively combined with read-out channels. For this reason not only the number of assigned APVs is checked but also the correct sequence of I^2C addresses and thus the bonding of the APV address pads. The assignment was successful if the APV with I^2C address 0x40 is assigned to the first read-out channel and the APV with address 0x4A is assigned to the sixth.
At the end of the assignment the registers of the APVs are reset to the values which are also used for the low voltage check. The correct data output is checked for 500 events. Possible failures are datasets where the header cannot be identified, the APVs do not run synchronously or the error bit of the digital header indicates a problem.
The procedure for header recognition takes into account that a wrong data fragment might be recognized as a header. The sequence of digital ones and zeros of the pipeline address bits in the header is assigned to a pipeline number. If a wrong data segment is treated as a header it is very likely that in at least one of the events no pipeline column is assigned to the sequence.
The synchronous run of the APVs is checked by comparison of the pipeline address bits of the APV headers. The sequence of bits must be identical for all APVs. Otherwise the data was not taken at the same point in time. It is easy to imagine that a mix of data from different bunch crossings cannot be used to determine the trajectories of particles in the experiment.
When the error bit of the header is at digital low level a fifo (**f**irst **i**n **f**irst **o**ut) or latency error was detected by the APV. In this case the error register of the corresponding APV is read to determine the correct error type.
In the next step the PLL clock and trigger delay is checked. As the sample timing of the ARC board is fixed with respect to its 40 MHz clock which is the incoming clock for the PLL, the tick mark height changes if the PLL delay works correctly. The ARC board samples the output of the APVs on the plateau of the tick marks before the delay is enabled. The delay shifts the data output and thus the timing of the ADCs with respect to the tick marks. When the edge of the tick mark is sampled a much lower height is measured and the delay is known to work. The PLL functionality check was not done in the PLL test because the correct data output of the APVs needs to be checked first.
The last part of the test deals with the stability of the APV register settings when a

high trigger rate is applied. The ARC board allows to read out single events at a rate of about 150 Hz which is far off the 100 kHz foreseen for the CMS first level trigger. The ARC board is capable of applying high trigger rates when the sampled data is not extracted from the RAM. Since the data is not of interest for the test but the APV register setting 100,000 triggers are send and the register settings are checked to match the initial settings.

6) MUX resistors check

The height of APV tick marks allow to check the proper electrical connection between the APV analogue output and the MUX chip and between the MUX chip and the hybrid connector. Furthermore the homogeneity of the MUX resistor is accessible.
If the APVs have not been assigned and the APV registers have not been set to their default values this is done first. The resistor homogeneity and the absolute signal height of the tick marks is checked with different combinations of two MUX resistors being switched in parallel to the APV output lines. In this case the tick marks cover almost the full ARC ADC input range and inhomogeneities of the MUX resistors cause a larger change of the tick mark height. First bits zero and one of the MUX register are set and 50 events are taken for the evaluation of the tick mark height. In the next step the second and third resistors are switched in parallel to the inputs, 50 events are taken and so forth. At the end of this test the difference between the maximum and minimum tick mark height is calculated for each APV as well as the mean signal height. The homogeneity of the resistors is good if the height difference is less than five ADC counts.
The average height of the tick mark is expected to be around 230 ADC counts. A height of less than 210 ADC counts is seen as an insufficient output. The expected average tick mark height of an APV is reduced by a factor of about two if one of the two electrical lines is not connected to an input of the MUX. If a pair of APVs suffers from this low signal output the connections between the MUX and the hybrid connector is more likely to be affected. The most probable error is output by the test.
Since the absolute header height is of importance to judge the homogeneity of the resistors the test is modified if the input range of the ADC is reached for 50 % of the events. In this case the measurement is redone with three resistors switched on. In this case the signal gets smaller and thus the cuts have to be correct by a factor F_{corr}. The factor depends on the number of switched on resistors NR_{res} and was obtained in measurements. When the number of resistors is reduced from NR_{res} to $NR_{res} - 1$ the factor is given by:

$$F_{corr} = \frac{50 + (NR_{res} - 1) \cdot 8.75}{50 + NR_{res} \cdot 8.75} \tag{3.15}$$

The second part of the MUX test deals with the change of the signal height when the number of MUX resistors is changed. The correct height is only measured if the tick mark signal does not exceed the input range of the ADCs. This is usually only the case for two or more resistors. For completeness the tick mark height is measured for zero to eight resistors being switched in parallel.

7) Fast Pedestal and Noise Check

The pedestal and noise test calculation does not differ from the pedestal and noise test which is part of the deep tests (see 3.6.3). The number of events is 500 to keep the testing time at low level. A special feature of the fast pedestal and noise check is the storage of a histogram keeping the number of hits for each pipeline column and a synchronization check for each event. The synchronous run of the APVs is also checked in the APV data output & clock distribution test but when the fast pedestal and noise test is done some time has passed since the last reset was applied to synchronize the APVs. For this reason the sensitivity is increased to cases where the desynchronization happens after about 20 s. As these failures usually become apparent after few seconds all hybrids suffering from this feature should be found.
If a DEPP board was assigned to the ARC board during the initialization of ARCS the depletion voltage and current are recorded before and after the test.

8) Fast Calibration Pulse Check

The fast version of the calibration check is a standard test as described in subsection 3.6.4 but at a fixed timing. The test is also comparable with a gain test (see 3.6.7) at fixed amount of injected charge. The test uses the internal calibration circuit of the APV and 50 events are acquired for evaluation of the average signal height.
Like for some other tests the APVs need to be assigned and the APV registers have to be set to their default values before the test is started. Like for the fast pedestal and noise test the depletion voltage and current are recorded before and after the test.

9) DCU Response Check

Before the DCU test is started the APV registers are set to their default values and the three registers for the DCU ID are read out. The bytes are combined to form a 24 bit unique identifier as shown in figure 3.19.

Next the DCU is set into a fixed state for data acquisition under fixed settings. The following data is written into the write accessible registers:

- CREG = 0x00
- TREG = 0x10
- AREG = 0x00

Because of these settings the following settings are chosen:

- low resolution (12 bit instead of 14 bit)

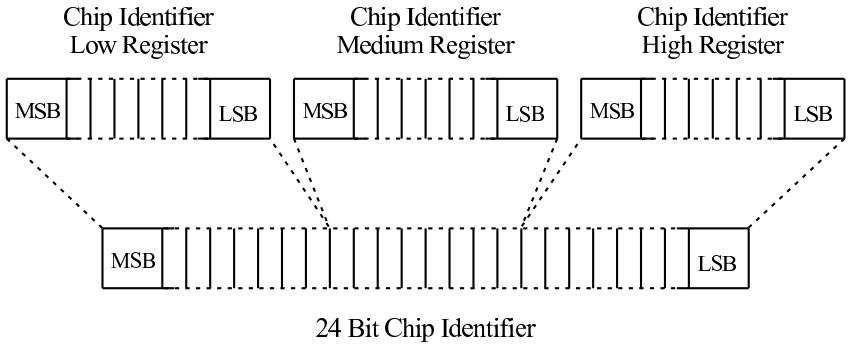


Figure 3.19: The combination of ID bytes held by the three DCU identifier registers to a unique 32 bit integer as programmed in ARCS. The number is unique and thus identifies each DCU unambiguously.

- high input range mode[21] (1.25 V $>$ range $\leq$ 2.5 V)
- test options disabled

Ten samples are taken for each DCU input channel, the average data is calculated and compared with the values expected. The expected values are contained in the test-settings XML file. For each taken sample the SEU (**s**ingle **e**vent **u**pset) bit in the SHREG register of the DCU is checked. If the bit is set a software reset as described in the DCU manual [32] is applied.
The last part of the test checks the response of the DCU when the hybrid supply voltage is changed. The nominal voltage of 2.5 V and 1.25 V is applied to the hybrid when the DAC for the low voltage control on the ARC front-end adapter (see 3.3) is disabled, which is the case during normal operation. The supply voltages are measured by the ARC front-end adapter and by the DCU. The first measurement is done when the DAC is still disabled, further measurements are done with enabled DAC. The DAC has a resolution of 8 bit and is set to 225, 200 and 175. As the DAC can change the nominal voltage by 19 %, 25 DAC counts result in a voltage change of about 47 mV on the 2.5 V line and half of this on the 1.25 V line. The measurement is not extended to lower supply voltages because the I^2C communication with the DCU may become unstable.

3.7 The Cooli Box

The cooli box was developed at the III. Physikalisches Institut B in Aachen for the performance of tests at temperature which are similar to the environment in the final experiment. The device is used for controlling and monitoring of temperatures and relative humidity. It is used for test stands where temperature controlled measurements are done via peltier elements.

[21] During the data acquisition procedure the setting is automatically changed to the low input range mode (0 V $>$ range $\leq$ 1.25 V)

The central unit of the cooli is an ATMEL[22] AT90S8535 micro-controller[23] which has many programmable digital in and outputs as well as analogue inputs. The chip provides a SPI (**s**erial **p**eripheral **i**nterface) interface for programming and communication with other chips and an RS232 interface which is used for access via a PC serial interface. The ATMEL chip is configured by firmware to provide additional functionality. A second RS232 interface is implemented and an interface for DALLAS[24] single wire temperature sensors of the serie DS1820[25] as well as an interface for SENSIRION[26] humidity probes of type SHT10[27].
The cooli box provides eight analogue inputs in the range of 0 - 5 V with ten bit resolution, two analogue outputs in the range between 0 V and 10 V with twelve bit resolution and two in the range between 0 V and 5 V with equal resolution. Furthermore eight digital ports are accessible which can be selected as input or output. An external power supply can be controlled by the cooli DAC output or more sophisticated power supplies may be controlled via the slave RS232 interface of the micro-controller. The polarity of the power supply current can usually not be switched by an external signal. For this reason two relays are implemented which allow to control the heat flow in peltier elements.
The micro-controller is triggered by commands which are sent via its serial interface. The single commands are listed in the cooli manual [41].
For safety reasons a watch dog timer is implemented. Each time a command is sent to the micro-controller the timer is reset automatically. When the reset is not applied within 120 s the watch dog switches off the relays. In this state the peltier elements become passive and the test box returns to ambient temperature. This safety feature is especially useful if the cooling control software is hung up.
An additional safety feature is an interlock which protects the peltier elements from overheating, e.g. when the cooling liquid was not switched on. Peltier elements are usually equipped with a temperature sensor which is realized by a bimetallic strip and put in series to the current supply circuit. When the sensor is heated up it disconnects the circuit and closes it once the peltier elements are cooled down again. The sensor is connected to the interlock of the cooli box which switches off the relays if the circuit is disconnected.
The picture of the cooli box with its interfaces is shown in figure 3.20

[22] Atmel Corporation, 2325 Orchard Parkway, San Jose, CA 95131, USA

[23] The data sheet is provided at: `http://www.atmel.com/dyn/products/product_card.asp?family_id=607\&family_name=AVR+8%2DBit+RISC+\&part_id=2000`

[24] Dallas Semiconductor is a wholly owned subsidiary of Maxim; Maxim Integrated Products Inc., 120 San Gabriel Drive, Sunnyvale, CA 94086, USA

[25] The data sheet is provided at: `http://pdfserv.maxim-ic.com/en/ds/DS1820-DS1820S.pdf`

[26] Sensirion AG, Laubisruetistrasse 50, CH-8712 Staefa ZH, Switzerland

[27] The data sheet is provided at: `http://www.sensirion.com/en/02_sensors/03_humidity/00_humidity_temperature_sensor/01_humidity_sensor_sht10.htm`

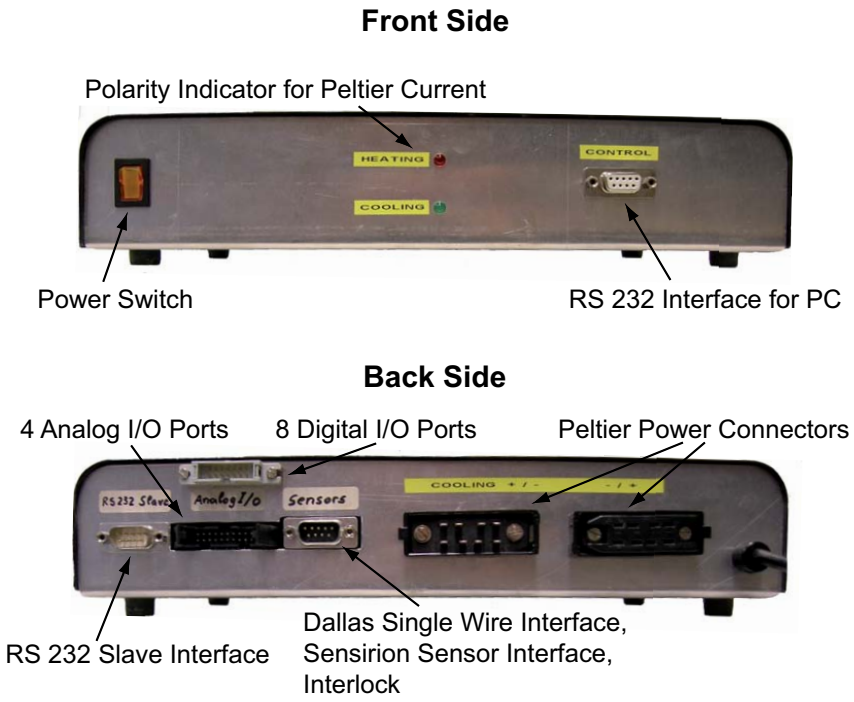


Figure 3.20: Front and read view of the cooli box.

3.8 The Cooli Control Software ACDC

The cooli control software ACDC was developed for communication with the cooli box. The software serves mainly as a GUI for the sensors read out by the cooli box and provides a PID (**p**roportional **i**ntegral **d**ifferential) regulation for temperature control. The software is completely implemented in LabView and is used in combination with test stands where tests are done in a temperature and humidity controlled environment.

The software development started with the build-up of the first test station which was designed for module tests at tracker operation conditions [42]. The software was modified for read-out and monitoring of the sensors for the hybrid test station (see 4.2). The latest version is used for the module cold box (see 4.4) which replaced the test station the software was originally designed for.

The latest version of the software is described here. More information on the version for the hybrid test station is given in the software subsection 4.2.2. The versions mainly differ in the layout of the GUI which adapts to the read out hardware and implemented regulation features. The graphical front-end of the latest ACDC version is shown in figure 3.21. It is dominated by the temperature and humidity display and the status of the peltier power supply. The status of the relays for the peltier current polarity indicates whether the peltier heats up or cools down the test box connected.

Next to the graphical presentation of relevant environment parameters some security features are implemented in the software. The hardware implemented security features cover severe problems, for instance the break down of the PC. If the hardware takes control over the temperature regulation the test station is brought back to ambi-

Figure 3.21: Screenshot of the monitoring and control panel of ACDC.

ent temperature and all tests are skipped. In the case of problem detection by software immediate feed back is given to the operator who can solve the problem and continue the tests.
The security panel of the software is shown in figure 3.22. The software allows to define temperature and humidity ranges for each probe. If the range is exceeded by one of the probes an alert is given and the current to the peltier elements is switched off. When all parameters are back to the allowed ranges the temperature control can be switched on again to continue the test scenario.

ACDC is the central application if a test scenario is performed. The scenario is defined by a file written in XML syntax. The following actions are implemented:

wait n: Wait n minutes before the next action is taken.

temp T: Set the temperature of the test box to T before the next action is taken.

measure m: Perform test on all test objects which were initialized by ARCS. The parameter m is an array of up to 25 zeros and ones which is the number of tests which are implemented in ARCS.[1] A test is performed if a one is written in the corresponding position of the array. The sequence of the tests is shown in the all tests panel of ARCS.

[1] The multiplicity of most of the tests which are described in section 3.6 is four because each APV operation mode is counted as a single test.

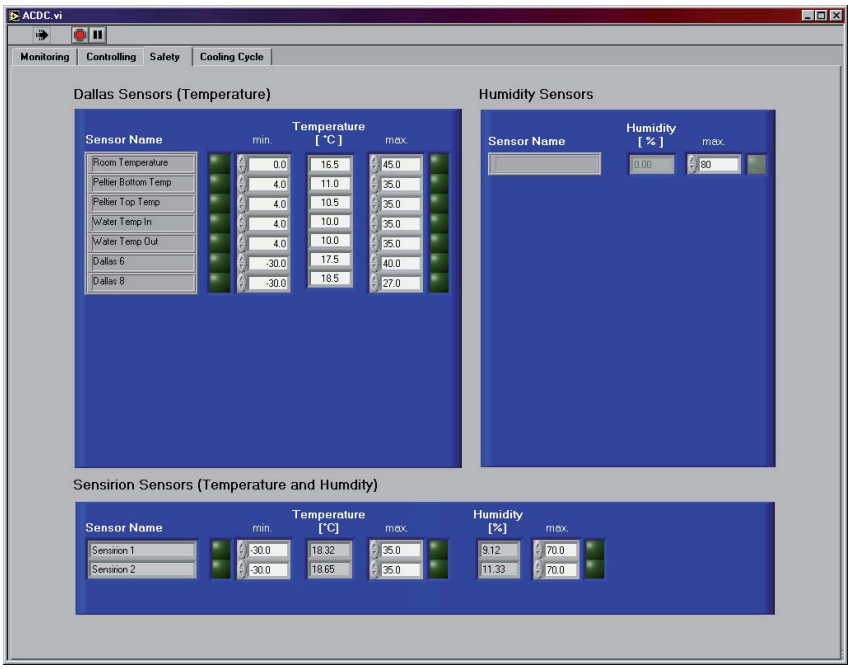


Figure 3.22: Screenshot of the security panel of ACDC.

If the action is measure, ACDC passes the test array m to ARCS via the tcp\ip protocol and waits for a report on the completion of the tests. For this procedure the remote modus must be enabled in ARCS. Because of this feature complete test scenarios can be run in a fully automated way which is highly desirable for the series qualification of modules.

Chapter 4

The Test Stands for Hybrid and Module Qualification

The four types of test stands which are involved in the electrical and functional qualification of the CMS hybrids and modules are described in this chapter. The first two sections cover the test stands for the qualification of hybrids, the following two are utilized for module characterization. All test stands are based on the ARC read-out system (see chapter 3).

4.1 The FHIT System

The *FHIT* (**f**ront-end **h**ybrid **i**ndustrial **t**ester) and the corresponding software *FHITS* (**f**ront end **h**ybrid **i**ndustrial **t**ester **s**oftware) were developed at the Institut de Physique Nucléaire - Physique des Hautes Énergies in Louvain (Belgium). As the name of the test system indicates it was designed for the test of hybrids in industry.
The main purpose of the tester is to provide a fast quality feedback on the object tested. The system requires a minimum of interaction which is essential to reduce the risk of operating errors and the need for skilled personnel.

4.1.1 Build-Up of the FHIT System

The FHIT system is build up by a standard ARC board and a modified ARC front-end adapter. The adapter contains the mandatory parts of the ARC front-end adapter like data buffer and I^2C level shifter but also micro-controllers and other components which provide the FHIT special functionality. A male 64 pin SAMTEC connector is implemented to interface a hybrid via a SAMTEC to female 50 pin ERNI transition card. The components are encased by an aluminium box.
The test system exists in several versions. The most important version for hybrid testing is the dual-FHIT which provides two hybrid interfaces. As the tests are done in turns, a tested hybrid can be exchanged while a test is running on the other interface which results in the desired high throughput. A photograph of a dual-FHIT system is

shown in figure 4.1.
The FHIT is interfaced via a PC serial port and a PCMIO card for communication with the ARC board. LEDs indicate the state of the system and the grade of the tested object. More information on the FHIT system is given on the FHIT web page [43].

Figure 4.1: Photograph of a dual-FHIT test system.

4.1.2 Front-End Hybrid Industrial Tester Software

FHITS consists of a FHIT and an ARC part with a common graphical interface which is created with LabView (see figure 4.2). The FHIT part of the software initiates a connectivity and electrical test. The tests themselves are implemented in the firmware of the micro-controllers of the system. The commands which start the tests are sent via the PC serial port. The communication with the micro-controllers is completely implemented in the LabView code. When FHIT specific tests are performed the ARC board is passive.

The ARC part of the software is based on ARCS 3.6 and thus uses DLL calls to interface the ARC board. Only the fast test of ARCS is performed for determination of the functionality of the hybrid. A deeper analysis would be too time consuming and reduce the test throughput.

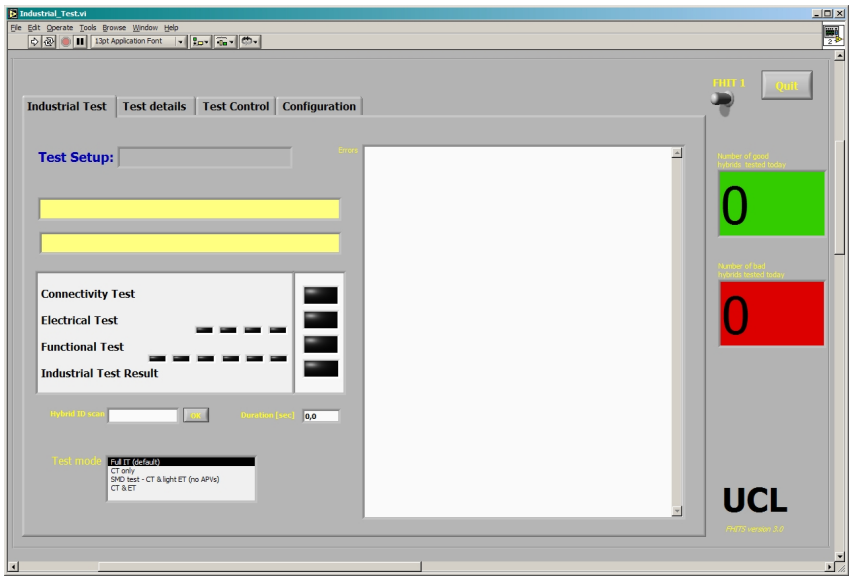


Figure 4.2: Screenshot of the GUI of FHITS. A test on the selected interface is initiated when the hybrid bar code is entered. If only a sub-set of tests should be performed the test mode can be changed. The red and the green box indicate the number of tests which were passed (green) and failed (red) since the program was started.

For the qualification of hybrids the three types of tests are performed in the following sequence:

1. connectivity test
2. electrical test
3. functional test

The connectivity test proves the electrical resistivity between certain lines(source [44]).

- Each type of power line (GND, V125, V250) must be connected to the other power lines of identical type.
- Each power line must be disconnected from the power lines of a different type.
- The termination resistors must be in place.

When the test was passed ten times the electrical test is performed. Otherwise further tests are skipped because the hybrid cannot be operated reliably if the circuit is broken. The electrical test checks for communication problems with the chips on the hybrids and calibrates the DCU. The following items are checked:

- the supply voltages
- the response of all chips to I^2C communication

- the access to the registers of all chips
- the presence of the decoupling capacitors
- the output of the DCU
- the change of the current consumption when the analogue power of single APVs is switched on

The electrical test is done at three different hybrid supply voltages. The first turn is done at the nominal voltages of 1.25 V and 2.5 V. The nominal voltages are increased by $\approx$7 % for the second and reduced by $\approx$18 % for the third turn. The test is failed if the communication with one of the chips was not reliable. The DCU output and calibration is not used for determination of the grade as the DCU is not essential for the operation of the hybrid.
The last test is the functional test which is performed using the ARC system. Since this part of the FHITS code was programmed in Aachen and differs from the latest version of the ARC fast test which is described in subsection 3.6.10 it is briefly described here.

The FHIT Functional Test

The functional test which is performed by FHITS is based on the fast test of ARCS version 5.1 as shown in table 3.1. The main difference between this version and the latest version of the fast test is the sequence of access to the chips, the implementation of some tests and most of all the feedback which is given in case of errors. For instance the previous version of the fast test does not act on all I^2C communication errors and does not inhibit the execution of further sub-tests if problems are observed. The basic functionality of the fast tests is similar. The version which is used by FHITS is described in detail in [38].
The FHIT functional test does not execute all sub-tests of the of the ARCS 5.1 fast test. The sub-tests which are performed are:

1. ARC self test
2. APV I^2C access test
3. APV data test
4. MUX resistors test
5. Pedestal and noise test
6. Calibration pulse test

4.1.3 FHIT Data Handling

For the generation of a database compliant XML result file, a standalone program is started from a command prompt which turns the ASCII output of FHITS into an XML file. This file is uploaded to the central database [36] by a second standalone application. The relevant tables are described in appendix D.2.

4.2 The Hybrid Test Station

The *hybrid test station* was designed for the test of hybrids and hybrids with assembled and bonded pitch adapter at tracker operation temperature. It was planed and constructed by CERN in cooperation with the III. Physikalisches Institut of the RWTH-Aachen in 2002. The expression *hybrid rapid cycler* or simply the *test station* are alternative denominations for the hybrid test station. In the further process of this section the name hybrid test station will be used to avoid confusion.
The first tests of hybrids with assembled pitch adapter at reduced temperature were performed with the hybrid test station. These tests provided important information on the principle mechanical and electrical stability of the hybrid and were thus a milestone in the validation of the design. A special feature of the test stand is a provision for external signal injection on the pitch adapter, a feature which is useful for the detection of pitch adapter lines which are not in electrical contact with the corresponding APV input channels. Information on the design of the test box, its verification and the operation of the test stand is given in the following subsections.

4.2.1 Build-Up of the Hybrid Test Station

When the hybrid test station was planned it was foreseen that the entire hybrid to pitch adapter assembly, bonding and testing would be done at CERN. For this reason high throughput is a main constraint for the hybrid test station. At the same time the safe handling of the hybrids was a mayor concern. Especially when the hybrids are assembled with a pitch adapter bad handling can easily cause serious damage.
A photograph of the hybrid test station is shown in figure 4.3. A purpose-build test box houses the hybrids which are read out by ARC boards in combination with the sandwiched version of the ARC front-end adapter. The temperature and the humidity inside the test box are monitored and controlled via the cooli box (see section 3.7). The single components of the test stand and their tasks are described in more detail in the following sub-subsections.

The Design of the Test Box

The test box is build on top of a ground plate which consists of a thin metal sheet of 1 mm thickness. The metal shield is laminated on wood so that the test box is build

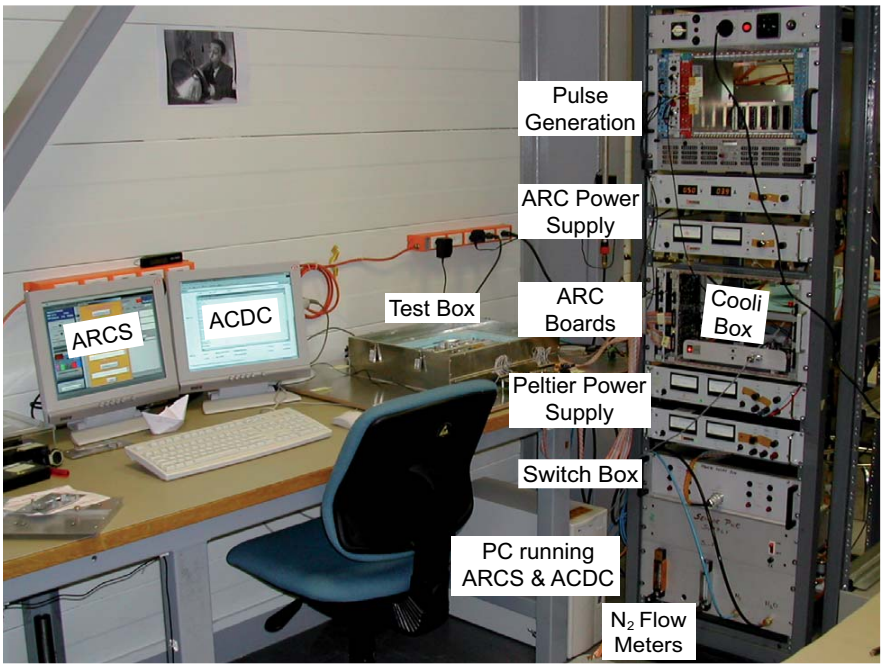


Figure 4.3: Photograph of the hybrid test station. The test objects are mounted in the test box. The test stand is operated via ARCS and ACDC which control the components in the rack.

on top of a rigid but light footing. For enabling the fixation of pipes and cables, the ground plate is bigger than the test box, which sits in the centre of the plate and insulates the test volume from the environment. Since the total test time is dominated by the duration of the thermal cycles and not by the time for data acquisition the test box was designed for insertion of up to four hybrids. The inside of the box is lined with insulating foam and the top plate of the box is detachable for mounting the test objects. The box is supplied with nitrogen to avoid condensation of humidity and cooling water for one peltier element[1] which is mounted below a central aluminium plate. The ARC front-end adapters are left outside the test box to keep the volume small. A photograph of the opened box is shown in figure 4.4.

Before insertion into the test box the hybrids are attached to rectangular shaped aluminium plates. For good thermal contact to the plates the hybrids are clamped down by a lever arm. The small adapter card of the hybrid is fixed with a spring loaded mechanism to simplify the electrical connection inside the box. The central plate is prepared for fixation of the hybrid support plates and carries the temperature and humidity sensors as well as a circuit for the injection of signals on the pitch adapter (see 4.2.1). A photograph of a mounted hybrid with assembled pitch adapter is shown in figure 4.5.

As a consequence of the chosen design the connection between the hybrids and the ARC front-end adapter is established via extension cables which influence the output signal of the hybrids. The investigation which was started to evaluate the impact of the cable is described in the next sub-subsection.

[1] Supercool , part id DL-290-24-00-00-00; Supercool AB, Box 27, S-401 20 Göteborg, Sweden; `www.supercool.se`

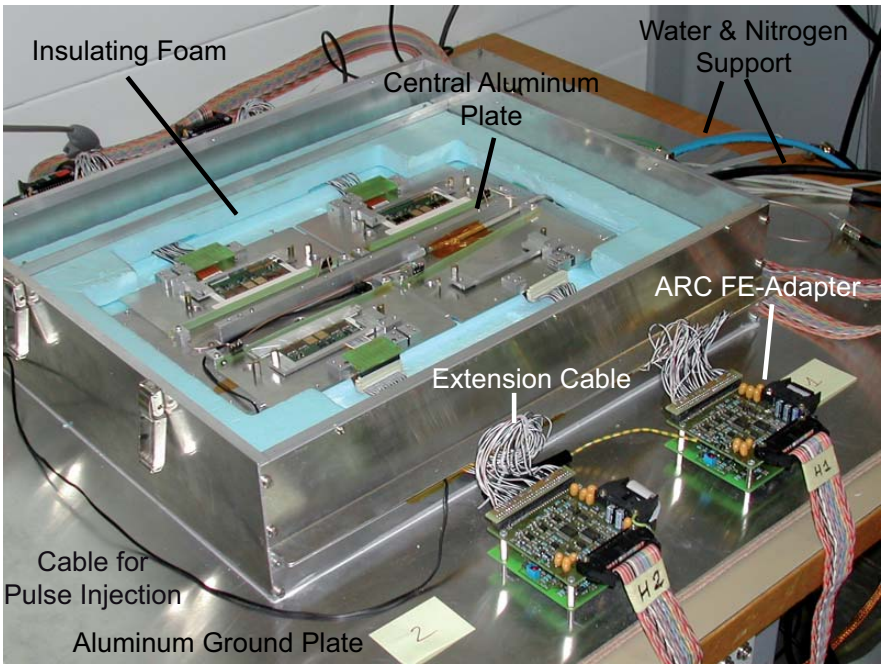


Figure 4.4: Detailed view of the opened test box. Tests are performed with an aluminium lid on top of the box which leads to an effective shielding. Good thermal insulation is achieved by foam which covers the inside of the box.

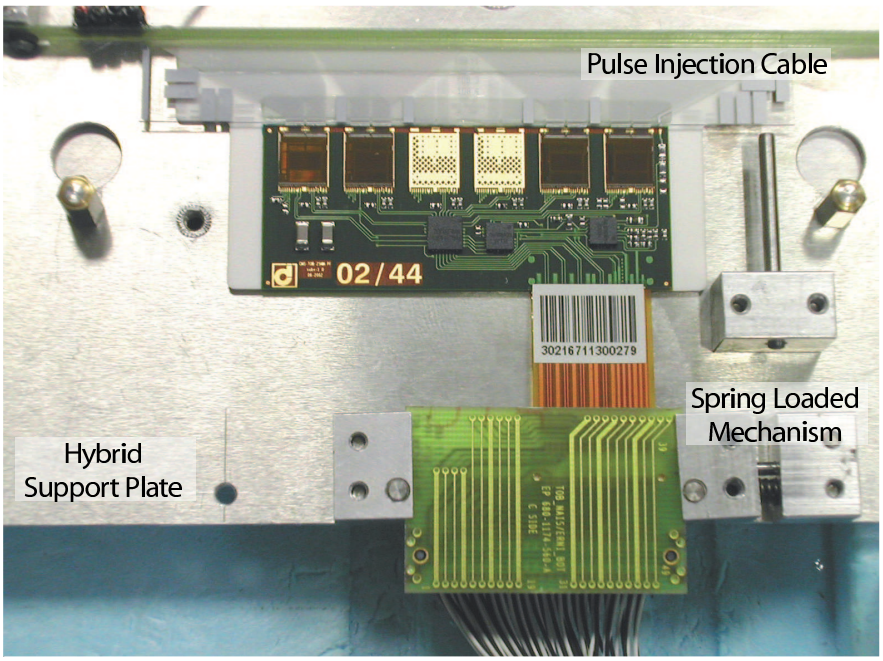
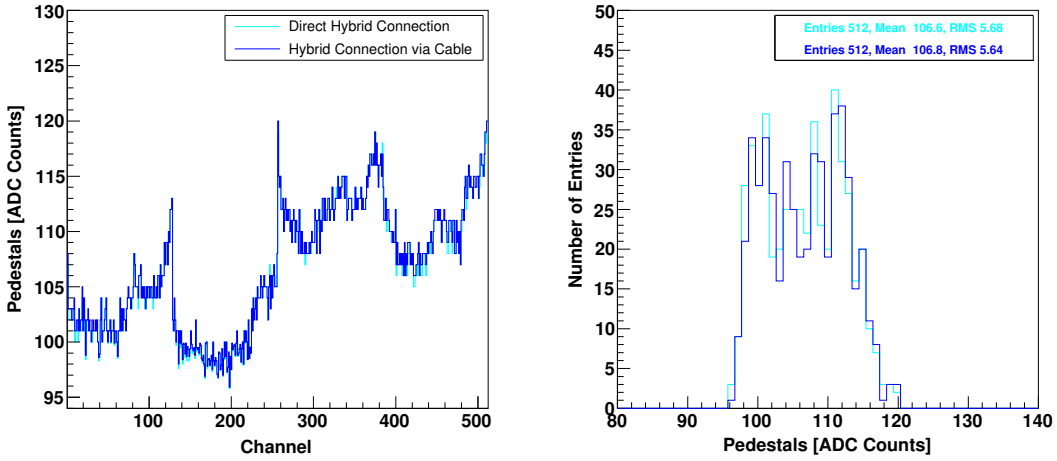


Figure 4.5: Photograph of a hybrid with pitch adapter which is mounted inside the test box. The support plate simplifies the mounting procedure as it provides a handle far off the fragile bonds and the pitch adapter. As the various types of hybrids have different geometries several types of support plates exist. The pulse injection cable is flexible and aligns automatically with the pitch adapter.

Influence of the Extension Cable

The hybrids are connected to the ARC front-end adapters via self made extension cables. It is best to install a short connection between the data buffer and the hybrid as the impedance of long cables might cause a significant degradation of the signal and noise might be coupled into the cable which overlays with the noise of the hybrids.
The capacity of the cable slows down the rise and fall time which is most critical when the output signal height changes a lot. Since the outputs of two APVs are multiplexed onto a single line the output signal height changes a lot during the transition between the error bit of APV2 the first channel of APV1 and the last channel of APV2 and the tick mark of APV1. Thus the height of channel 1 and 256 of each hybrid output line are will be affected most likely. The pedestals of a hybrid measured with and without the extension cable are shown in figure 4.6. As no significant difference is observed for the most sensitive channels there is no indication for a significant distortion of the hybrid output.

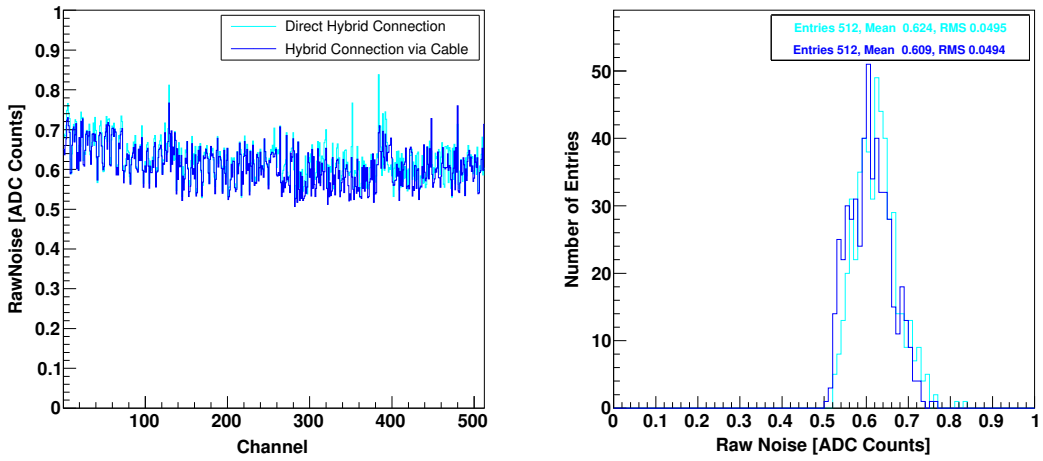
The noise of the same hybrid was measured with and without the extension cable.



(a) **(b)**

Figure 4.6: Comparison of pedestals with and without intermediate extension cable. The cable will most likely affect the channels 1, 257, 258 and 512. As no significant difference is observed there is no indication for a significant signal degradation.

The result is shown in figure 4.7. Under the assumption that the reproducibility of such measurement is about the same as for hybrids (see section A.2) there is no indication for external sources to have a significant effect on the noise when the cable is used.
The measurements verify that the adapter cable does neither cause a significant distortion of the hybrid output nor introduce additional noise. For this reason the chosen design of the test box is appropriate for the evaluation of hybrids.



(a) **(b)**

Figure 4.7: Comparison of noise with and without intermediate extension cable. The cable does not pick up noise.

Shielding and Grounding Issues

The pitch adapter lines act as antennas. While this feature is useful for intentional signal injection it is hindering the determination of the hybrid noise if external noise sources are present. For this reason a reliable measurement of the noise is only possible if a grounding and shielding scheme is implemented. The effect of a proper grounding and shielding scheme is shown in figure 4.8.

Proper shielding is provided by the test box because the test objects are completely surrounded by aluminium when the box is closed. The grounding scheme which was implemented for the test box is shown in figure 4.9. When the power supplies for the ARC system provide a floating output as recommended, the ground is determined by the PC via the 50 pin flat band cable that interfaces the ARC board on one side and the PCMIO PC card on the other side. As the flat band cable to the PC is about 1.5 m long and the diameter of the wires is small a good grounding scheme is not provided by the read-out. Theoretically the best grounding scheme is a single grounding point and a star like distribution of the ground. The cable should have a sufficient diameter, it should be short and ground loops should be avoided. In the case of the hybrid test station local ground loops were found to be necessary to minimize the pick up of noise. Most important is the connection of the central aluminium plate with the local ground of each hybrid and a proper connection between all front-end adapters and the ground plate.

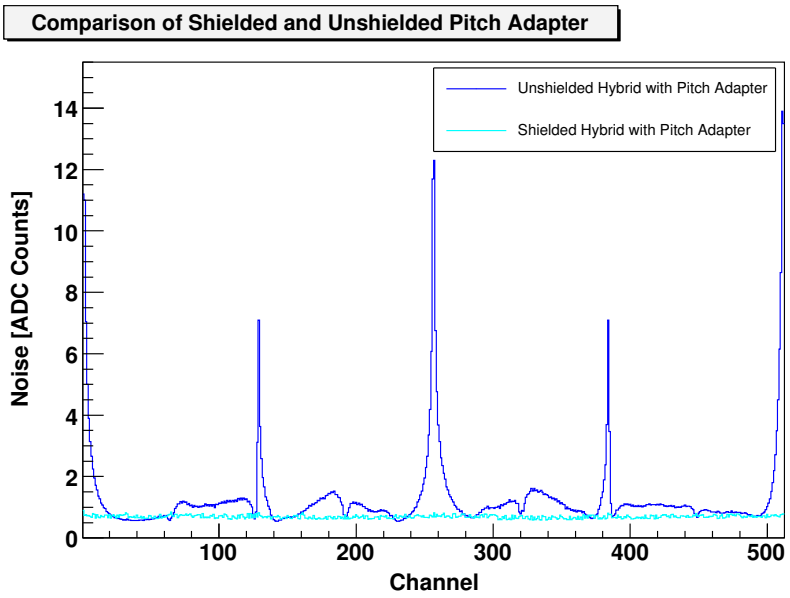


Figure 4.8: The noise of an unshielded hybrid with pitch adapter compared to the noise of a hybrid with pitch adapter which was tested inside the test box. The pitch adapter can pick up a significant amount of noise.

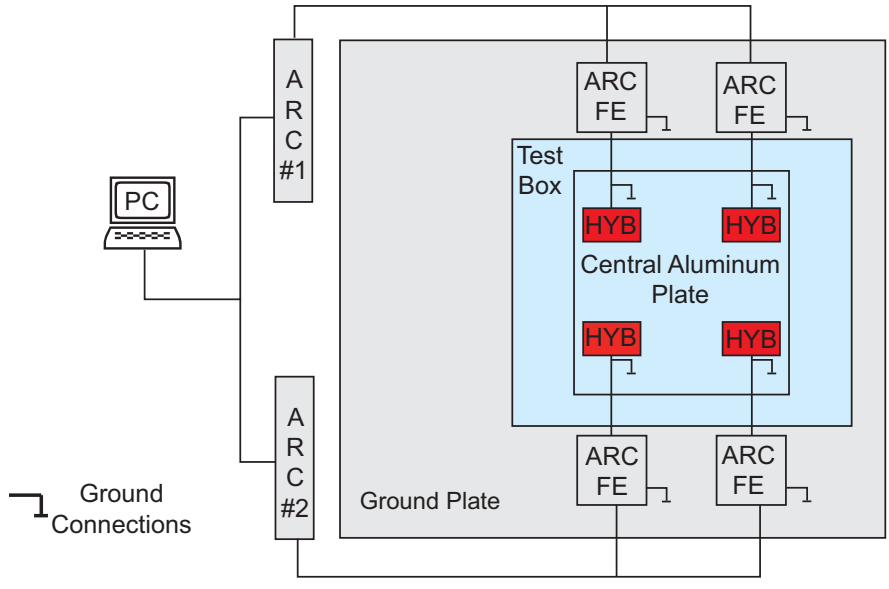


Figure 4.9: The grounding scheme of the hybrid test station. The ground is provided by the PC. The ground of the front-end adapters is connected to the ground plate and the central heat sink plate is connected to the hybrid ground.

Signal Injection on Pitch Adapter

An external signal can be applied to the APV via the lines on the pitch adapter which act as antennas. The scheme of the signal injection is shown in figure 4.10. The LVDS trigger out signal on the expansion bus of the ARC board is used for the initiation of a TTL signal which is applied on the pulse injection cables. The TTL pulse is synchronized with the APV trigger by a timing unit. The signal injection is en- and disabled by the cooli box which sends a veto during normal operation. The injection of signals on the pitch adapters is a feature which is very useful for the detection of missing or broken bonds as shown in subsection 5.1.1).

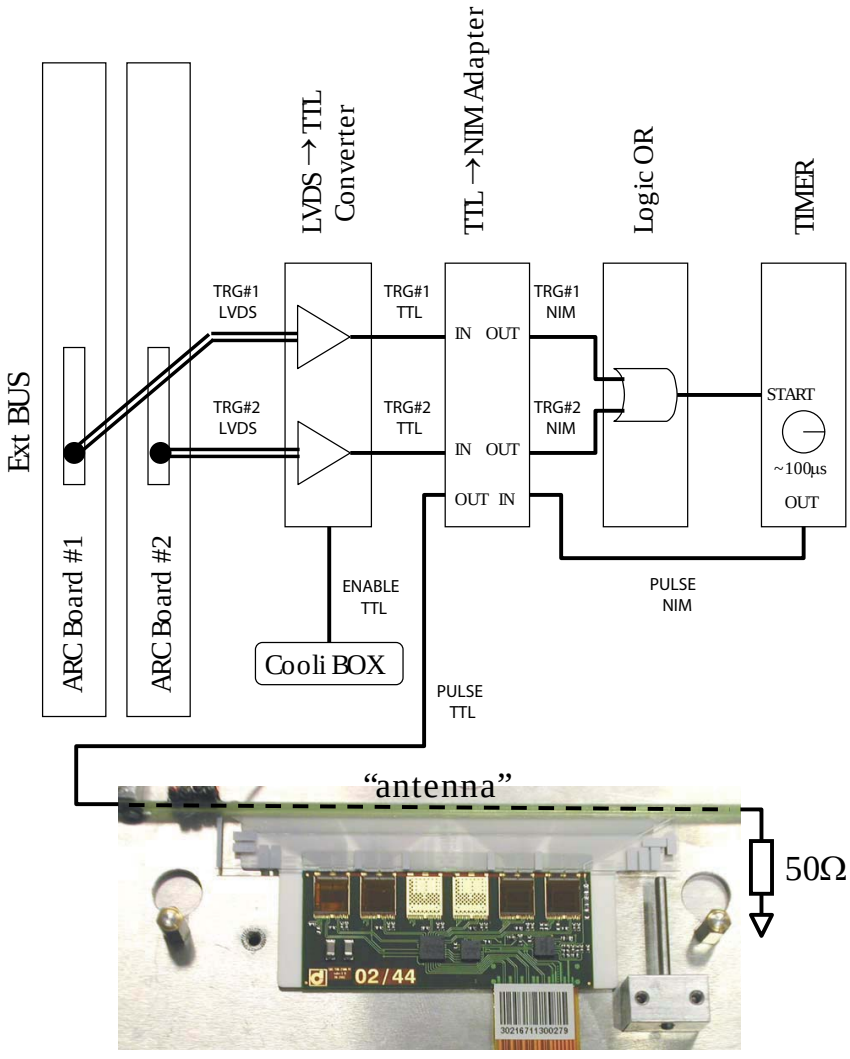


Figure 4.10: The scheme of signal injection on the pitch adapter. The APV trigger on the expansion bus of the ARC board is used to initiate TTL pulses which induce signals into the pitch adapter.

Humidity and Temperature Monitoring and Control

The performance of tests in a temperature reduced environment requires the careful monitoring and control of the humidity because condensation of humidity is very likely when the temperature is reduced by 40°C. The temperature and the humidity are monitored by the cooli box which is interfaced by a CERN special version of ACDC (see subsection 4.2.2).
Humidity sensors of type hih3610[2] by Honeywell[3] are placed in the test volume for humidity measurement. The sensors provide an analogue voltage output which is connected to an analogue input of the cooli box. The humidity is controlled via a *switch box* which is interfaced by the digital outputs of the cooli box. The switch box has four digital inputs for control of the same number of electro-valves. The flow of dry gas is controlled via two valves with a manual gas flow meter in series as indicated in figure 4.11. One of the two gas flow meters is set to a high flow of 200 l/h while the other one is set to 10 l/h. The valves are switched automatically on an off depending on the humidity level inside the test box. The relative humidity is always kept below 30 % during operation.

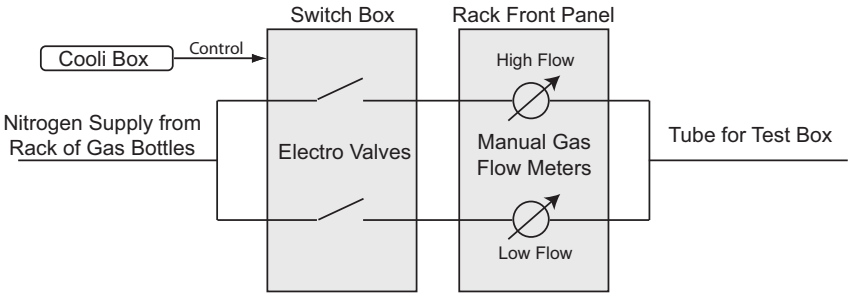


Figure 4.11: Gas flow control in the test box.

The temperature is measured by DS18B20 sensors by Dallas Semiconductor (see section 3.7). The sensor are located in dedicated recesses in the central aluminium plate. They are thermally decoupled from the plate and measure the temperature of the hybrid via its support plate.
The temperature is controlled by the polarity and the magnitude of the current for the peltier element. The current is provided by a power supply with an analogue input which is interfaced by a DAC of the cooli box. The DAC setting and the setting for the relays which determine the polarity of the current are calculated by ACDC. One of the electro-valves of the switch box is used to switch the water for the peltier element on and off. The fourth valve of the switch box is not used.

[2]The data sheet is provided at: `http://content.honeywell.com/sensing/prodinfo/humiditymoisture/009012_2.pdf`
[3]Honeywell International Inc., 101 Columbia Road, Morristown, NJ 07962, USA; `www.honeywell.com`

Security Features

Next to the temperature and humidity range warnings which are implemented in the standard version of ACDC (seesection 3.8) and the security features of the cooli box (watch dog timer and interlock), two sensors are implemented for immediate detection of missing water or nitrogen supply. A water flow meter is installed in the water supply tube. The sensor has a voltage output which is connected to an analogue input of the cooli box. Another analogue input of the cooli box is used for the measurement of the gas flow. The gas flow meter is self made and consists of a pair of thermocouples which are fixed inside and outside the gas supply tube. When gas is supplied to the test box the sensor inside the tube cools down to the nitrogen temperature while the reference probe heats up. The resistivity difference is converted to a voltage information. The states of both sensors are displayed in the software. A message box pops up and the peltier current is switched off if no gas or water is supplied while a cooling cycle is running.

4.2.2 Software

The software for the hybrid test station consists of two applications. The ARC boards are operated with a software which is based on ARCS version 6.1 and the test procedure, control and monitor of temperature and humidity is done by ACDC. The versions of the applications for the hybrid test station are similar to the software which is described in the sections 3.6 and 3.8.
The modified ARCS version fulfils the special needs for the test station which is a highly automatized and intuitive design. For this reason a simple interface was implemented where the operator only scans the bar codes of the hybrids and choses the desired test scenario. A screenshot of the software is shown in figure 4.12.

The central application of the hybrid test station is ACDC. The software monitors and controls the temperature and the humidity of the test box, triggers ARCS to run tests if the desired temperatures are reached and gives alerts if one of the sensors shows unexpected results. The main tasks and the interfaces involved are summarized in table 4.1.

Data Handling

At the end of a test the data is stored in an ASCII file. For production and quality control the relevant data is send to the central tracker database. For this reason the result files are browsed by an XML generator which creates a database compliant XML file. The table which was implemented for the needs of the hybrid test station is described in section D.2.2 in the appendix.

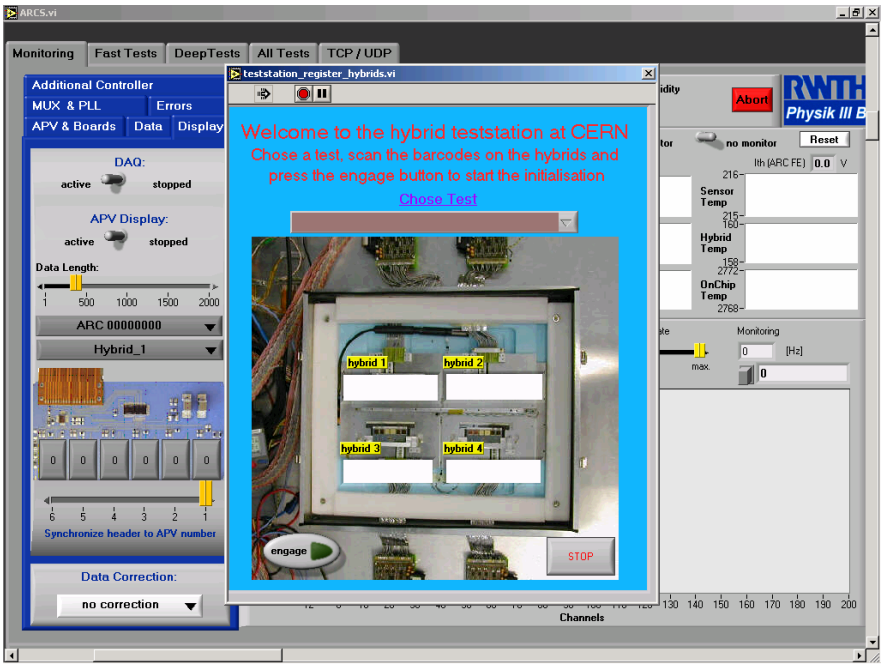


Figure 4.12: The screenshot of the ARCS version for the hybrid test station shows the initialization panel where the bar codes of the hybrids are entered and a test scenario is chosen.

Task	Interface
temperature monitor	cooli Dallas single wire
temperature control	PID regulation for calculation of the peltier current cooli relays for current polarity cooli DAC for control of peltier power supply
monitor humidity	cooli analogue input
humidity control	cooli digital outputs for control of the switch box
monitor water flow sensor	cooli analogue input
monitor nitrogen flow sensor	cooli analogue input
start tests in ARCS	software: tcp/ip protocol
enable signal injection	cooli digital output

Table 4.1: Summary of the tasks for ACDC and the involved interfaces.

4.3 The Single Module Test Stand

The *single module test stand* was developed for the test of single modules and single hybrids with assembled and bonded pitch adapter. Each institute which is involved either in module assembly, module bonding or module integration is equipped with a single module test stand. For this reason the single module test stands are the most important tools for the evaluation of the quality of modules.

4.3.1 Build-Up of the Single Module Test Stand

The obligatory components which constitute the read-out of all single module test stands are an ARC board, a front-end adapter and the PCMIO card. The test stands which are used for the test of bonded modules are also equipped with a DEPP board and a LEP16 board including the optical fibre array. The test stands are completed by an appropriate test box which shield the test objects from external noise sources and provide darkness for I-V measurements. As the test stands were needed in many institutes when the first module components became available a number of test boxes were developed in parallel. Although the read-out system is identical for all test stands, the various collaborating institutes working for a certain tracker part made cross checks to compare the properties of the various test boxes. The comparison of the test stands which were used in the tracker end cap community is described in sub-subsection 5.2.3. The design of the various test boxes does not vary much as the requirements are identical. Thus the general features of the test box which is described below applies to all boxes.

4.3.2 Build-Up of the Test Box

Here the single module test box of the III. Physikalisches Institut Aachen is described[4]. The test box was designed after some experience on hybrid and module tests were gained. At that time the components of the ARC system which needed to be integrated were known and essential features the box needed to provide had been sorted out. The issues which drove the test box design are:

- Fast and safe insertion of hybrids and modules.
- Good shielding from external noise sources.
- Robust grounding scheme
- Integration of the fibre array for signal injection on the silicon sensors
- Light tightness for exact measurement of the depletion current

[4]The basic design was adopted from the I. Physikalisches Institut Aachen and slightly modified for better noise performance.

A photograph of the Aachen test box is shown in figure 4.13. The test box is completely made from aluminium and thus shields the test object perfectly if all components are in good electrical contact. The hf (high frequency) springs on the ground provide a good electrical contact and a robust closing mechanism. The box is light tight because of fabrics which were added along the lid. As the outer dimensions of all module transport frames are identical the implemented guides are useful for the insertion of all module types. Thus the modules stay on their transport frame during a test and handling mistakes are very unlikely. Hybrids can be tested when a metal sheet with the dimensions of a transport plate is inserted. The optical fibre array for signal injection on the sensors is integrated into the mechanics. For module tests the array is located on top of the far end of the last sensor. Tubes for the supply with nitrogen or dry air are added to the box to keep the humidity low when a module is under test. The test box is air-tight to a level that the humidity stays below 30 % when dry gas is supplied at 10 l/h. The box is electrically grounded via the ARC front-end adapter which is connected to the ground of the PC. Additional grounding connection are not necessary.

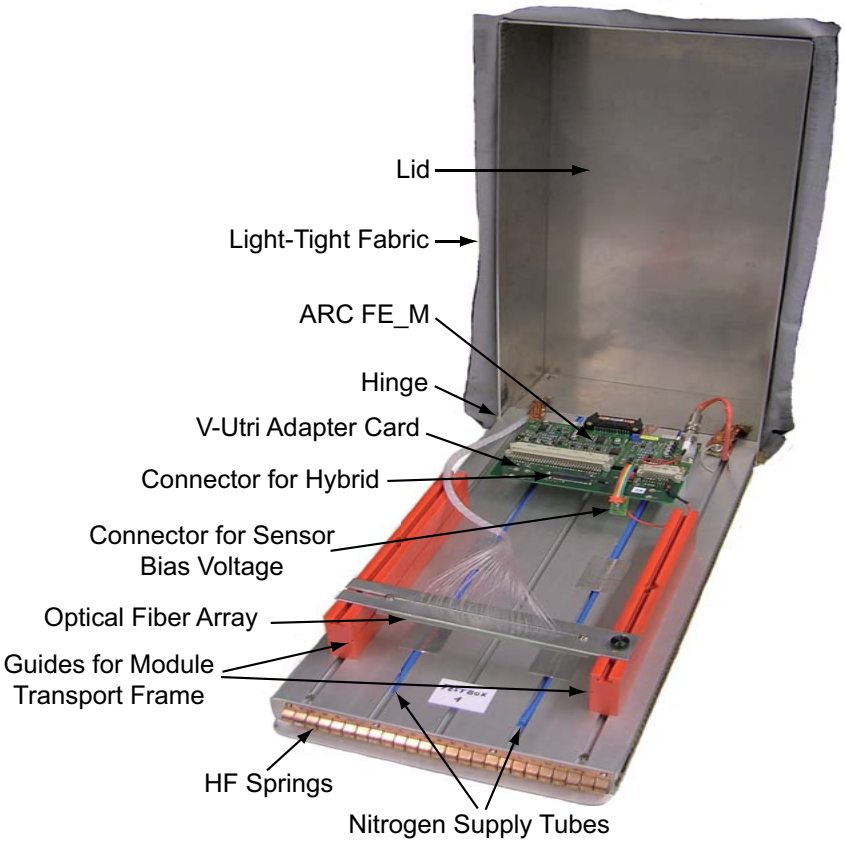


Figure 4.13: Photograph of the single module test box in Aachen. The design features the safe insertion of the test objects, light tightness and good shielding and grounding. Similar boxes are used by all institutes participating in the module production.

4.3.3 The Software for the Single Module Test Stand

The software which is used for the single module test stands is the standard ARCS version which is described in section 3.6. When ARCS is started the operator selects the test object and its type from a drop down menu. For this reason ARCS can be used for hybrid, hybrid with pitch adapter and module tests.

4.4 The Module Thermal Cycling Test Stand

The module cold box was designed for the performance of module tests in a CMS tracker like environment. The four tracker communities followed different strategies for the module design validation at CMS tracker operation temperature. While all modules for the TIB and TID undergo a test in a module cold box, modules for the TOB and TEC are mounted on sub-assemblies before thermal cycles are done. The module cold boxes in the TEC and TOB communities were only used at the beginning of the production when the mechanical and electrical components for the assembly and the test of the sub-assemblies were not available.
The test stand which is described here was designed in the framework of a diploma thesis [45]. It is the only test stand of this kind which is read out by the ARC system.

4.4.1 Build-Up of the Thermal Cycling Test Stand

The module cold box is build up by an aluminium frame which is surrounded by insulating foam and plastic sheets as outer boundary. Guides are milled into the top an the bottom plate of the frame for the insertion of up to ten module boxes which house the modules. The boxes minimize the risk of handling failures and simplify the mounting procedure significantly. Springs are implemented on the bottom and top side of the frame to provide good thermal contact. For cooling two peltier elements[5] are fixed are fixed to the frame. The cold box is provided with water for the peltier elements and with nitrogen or dry air to keep the humidity below 30 % at all operating temperatures. A photograph of the module cold box test stand is shown in figure 4.14.
As the cold box can house up to ten modules five ARC boards are used for read-out. They interface ten ARC FE_M adapters which are attached to the backplane of the test stand. The ten channels for sensor depletion power are provided by five DEPP boards. The ARC boards and the DEPP boards are inserted in a single crate which is interfaced via the PCMIO card. The temperature control and monitoring is done via the cooli box.

[5] The type is identical with the one for the hybrid test station (see section 4.2)

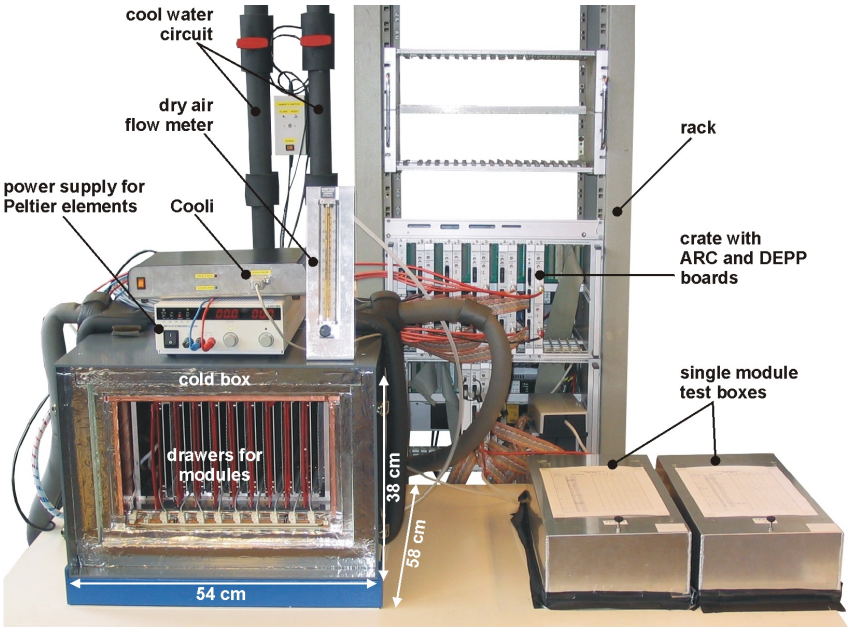


Figure 4.14: The module thermal cycling test stand is designed for module tests at CMS tracker operation environment. The test box can house up to ten modules and reaches a minimum temperature of about -30°C.

4.4.2 Software

The thermal cycling test stand is interfaced by the standard ARCS and ACDC versions which are described in the sections 3.6 and 3.8. Like for the hybrid test station ACDC is the central application which sets temperatures and communicates with ARCS to initiate tests. Since ACDC was designed to work off user defined test procedures tests can be performed fully automated.

Chapter 5

Faults and Qualification Procedure for Hybrids and Modules

This chapter focusses on two topics. The faults which were found during the production of hybrids and modules and the qualification procedure which is installed for quality assurance.

5.1 Fault Description and Detection

The faults, which are described here, are features of hybrids or modules which may complicate a production step or impair the performance or reliability of the affected component. A fault may affect single read-out channels, an entire APV or a complete hybrid or module in the worst case.
In the further progress of this section the faults are distinguished by their origin. The first subsection covers faults which are detectable during hybrid assembly while the second subsection covers module specific faults.

5.1.1 Hybrid Faults

The faults on hybrids are assigned to one of the following categories:

1. circuit related problems
2. chip faults
3. bond related failures
4. pitch adapter failures
5. other defects

1) Circuit Related Problems

Faults of the hybrid circuit are discontinued or short circuited lines but also bad solder joints of the ASICS and passive components. The failures are caused by production flaws. The rate of bad circuits is significantly influenced by the circuit design.

Two incidents caused a loss of complete batches of circuits during the production period. The first loss was initiated by a design change of the hybrid kapton tail. In the first engineering run a small support plate on the back side of solder pads for the NAIS connector was omitted. The intention of the design change was a reduction of the number of different circuit design which simplifies the production. The removal of the support was identified to cause problems when a large number of hybrids suffered damage when the hybrid cable was bent at small radii. Since all cables are bent when the modules are installed on the sub-assemblies a return to the original design was necessary.

The origin of the problem is a combination of gold and nickel layers. The layers are needed for good reliability of the solder joints between the circuit and the NAIS connector. At the same time the connection becomes very brittle and does not tolerate shear forces. About 700 hybrids and roughly 4700 circuits were excluded from further assembly [46]. A picture of a cracked cable is shown in picture 5.1.

The largest impact on the hybrid production was caused by low quality electrical inter-

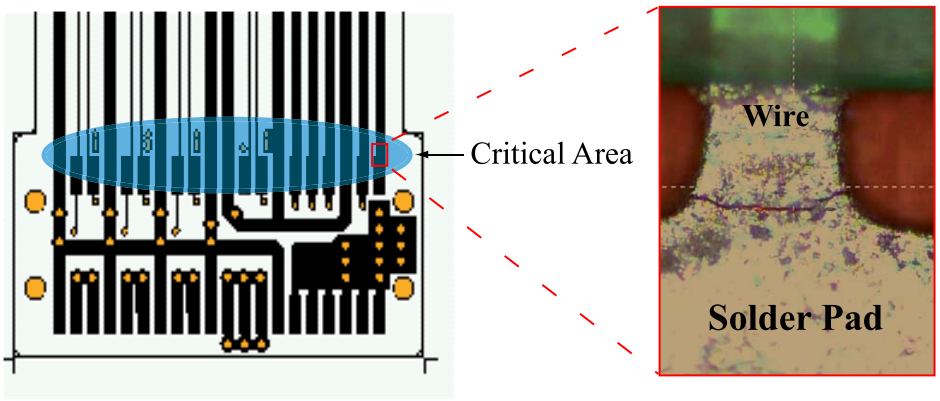


Figure 5.1: The wires of the hybrid kapton tail snap off and break close to the NAIS connector where the force is strongest when the cable is bent.

connections between the four metal layers of the circuit. These connections, so-called vias (see also figure 2.11), have a diameter of 100 µm and the most critical ones go straight through all layers.

The holes for the vias are made by laser drilling. The method causes an indentation in the innermost layer of the hybrid which is made from glue. Because of the indentation the proper flow of chemicals which is part of the metal deposition process is hindered. In this case likely only a little amount of gold covers the edges and the reliability of the contact is poor.

A modification of the sequence of layers in addition to the increase of the via diameter were found to solve the problem. The thick layer of glue is replaced by two thinner layers which are separated by an additional kapton layer. The diameter of the vias is

120 µm in the final design. Vias of the earlier and the latest circuit design are shown in figure 5.2. The cross sections prove that the formation of an indented region is suppressed in the new design. During the investigation of the problem the production was stopped and relaunched with a new design two months later.

Apart from the two incidents which caused the loss of a high number of circuits and

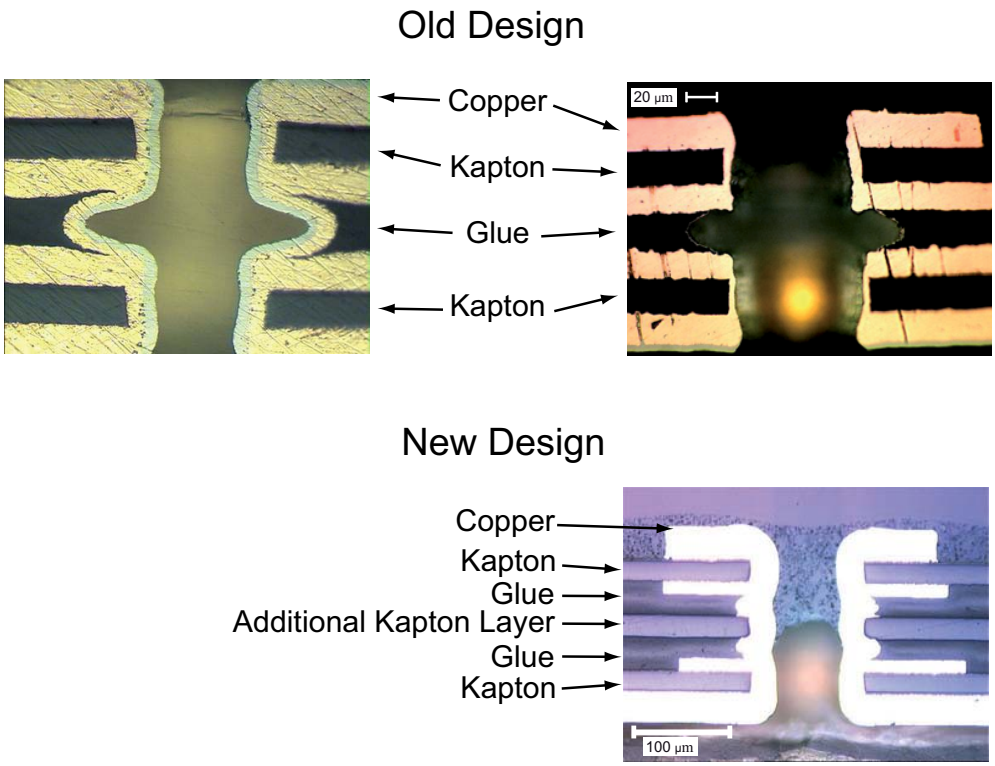


Figure 5.2: Cross sections through vias of old and new design hybrids. The formation of an indentation is suppressed in new design. Thus the metallization process is less critical and the electrical connections are more reliable.

assembled hybrids, circuit related problems occur at a rate which is determined by the stability of the manufacturing process. This process was carefully monitored after the incidents had happened since further problems would have governed the overall production schedule. As a result the quality of the metallization was monitored thoroughly via dedicated test structures (see section 5.2.1).

Circuit related problems like discontinued and short circuited lines can have many implications like bad I^2C communication, missing power or clock signals, a decreasing baseline etc.. The failures are detected by the FHIT tester.

2) Chip Faults

Chip faults are features of a fraction of chips. They are already present after the production in the forge. The failures which were observed on the various chips are described below.

Some **PLL** chips do not provide proper clock and trigger signals when the chip is powered up or after initiation of a hardware reset. A comparison of scope measurements is shown in figure 5.3. The probes are put on the trigger and clock output of the chip. Figure 5.3(a) shows the situation at room temperature. As desired a trigger is seen on the trigger line and the 40 MHz clock is output. In figure 5.3(b) the situation at low temperature is shown. The clock is output properly while triggers are seen on the trigger line although no triggers were applied.

An investigation was started to find out if the feature is a threat for the operation of

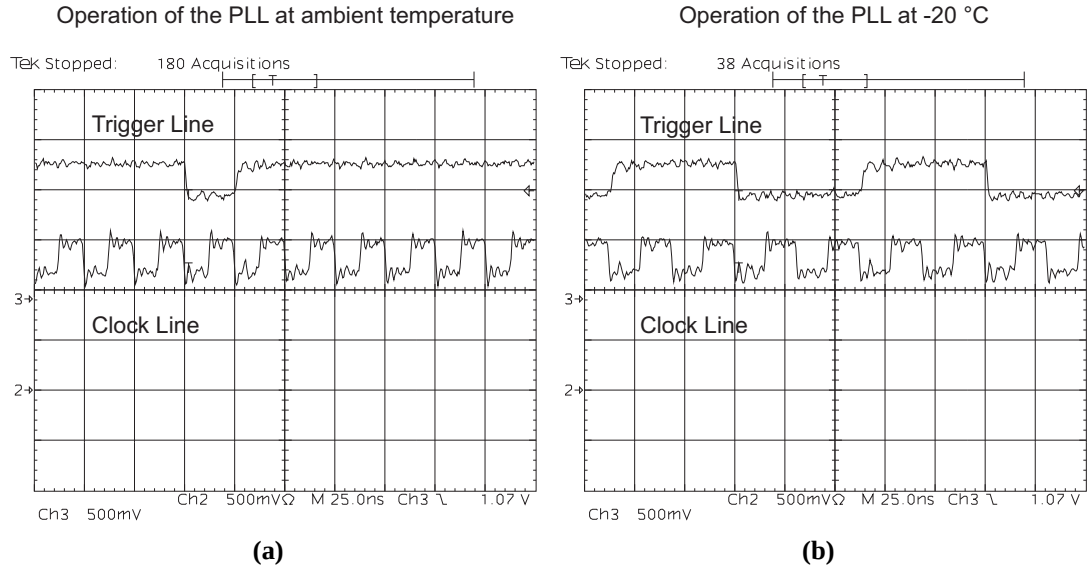
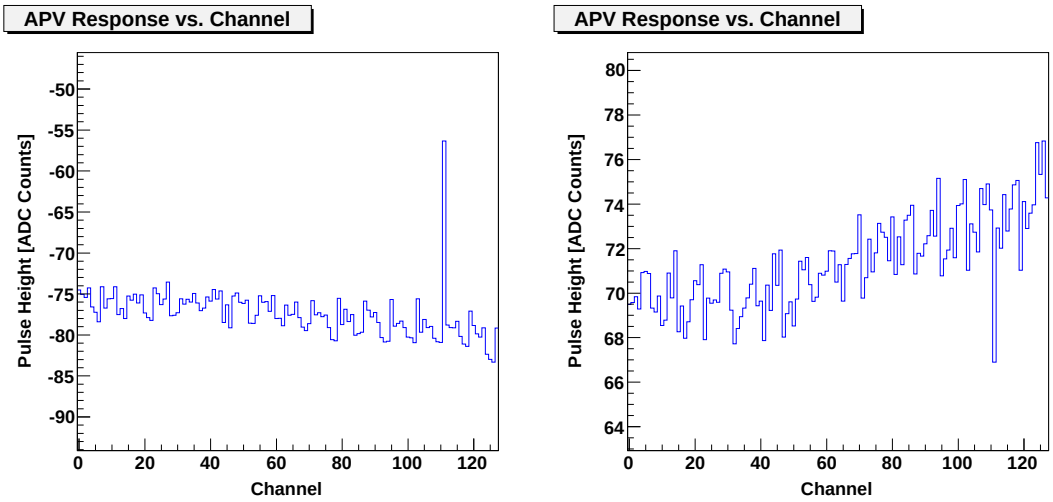


Figure 5.3: Scope measurements on the PLL clock and trigger output lines. The shapes of the signals are bad because of the difficult connection of the probe on the hybrid. In a) the expected output of the PLL is shown when a trigger is applied. In b) the output at low temperature is shown where signals on the trigger line are present although no trigger was applied by the read-out.

the tracker [47]. It turned out that it is caused by the auto-calibration circuit of the chip. The feature is highly temperature dependent and turns on at about -11°C. At low temperature the calibration logic does not find proper values for the DACs. Thus the output signals of the chip are disturbed and the hybrid analogue output is corrupted. The feature is not seen too critical for the operation of the tracker as it can be bypassed. The chip can be forced to work by certain settings of its registers. The procedure is given by[1]:

1. Set the chip in test mode.
2. Write proper settings into DAC low and high register.
3. Activate the high loop gain.
4. Set the „FORCE GOING“ bit.

[1]Information on the various registers and bits are given in the PLL manual [30].



(a) **(b)**

Figure 5.4: The fault which reduces the maximum response height in the inverter on APV operation modes are called broken inverter (a). As shown in (b) the response in the inverter off modes can also be reduced but the effect is less pronounced.

As the feature is only present at low temperature it can only be detected in the hybrid test station or the module cold box.

The **MUX** chip multiplexes the output of two APVs onto a single line. Some of the chips do not switch between the two inputs but output the data of a single APV twice. The failure is critical as data of an entire APV is lost. The missing output of one chip is spot during the assignment of APV I^2C addresses to read-out channels. The procedure is done during the initialization phase of ARCS and during the fast test (subsection 3.6.10). Since the initialization is an essential part of all test stations, faulty MUX chips are discovered by all test stations. Hybrids suffering from this problem are not used for module construction.

An **APV** input suffering from a *broken inverter* shows a reduced response to calibration signals. The typical effect is present in inverter on and off APV operation modes. As the effect is much more pronounced in inverter on modes it is called defect inverter. Although the tracker will be operated in inverter on mode a channel with a broken inverter may still have a signal to noise ratio above 20. Thus the channels are not necessarily lost.
A broken inverter is identified by means of response to signal injection in inverter off and on mode. While the maximum amplitude of the affected channel is comparable with mean amplitude of all channels in inverter off mode, it is obviously reduced in inverter on mode. The effect is depicted in figure 5.4.

Bad pipeline cells are cells with exceptional high or low pedestal values or reduced gain. The typical failure affects complete pipeline columns which show abnormal

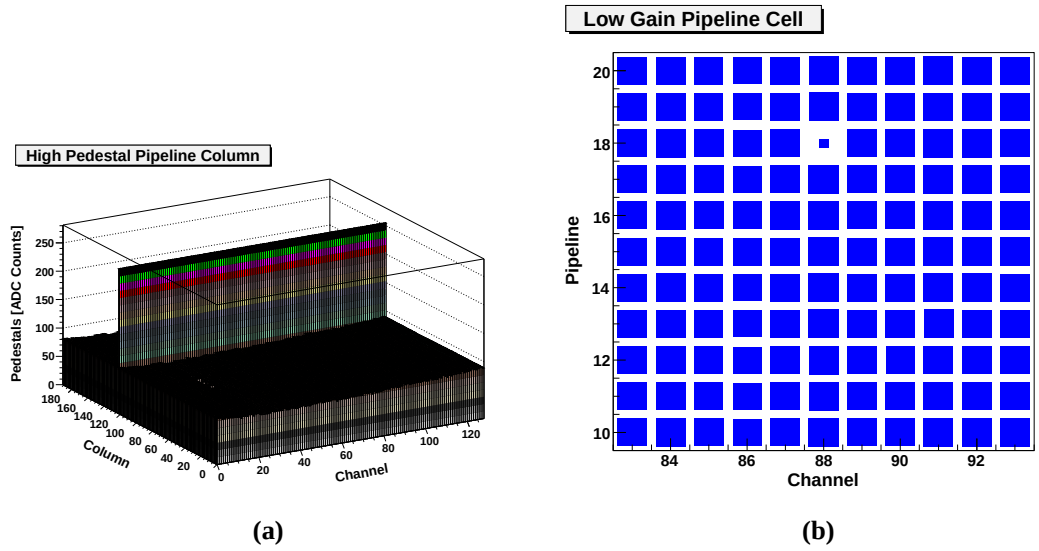


Figure 5.5: The plots illustrate typical examples for pipeline failures. A pipeline column which is stuck at the extreme high level of the APV analogue output is shown in (a). The response to pulse injection of an extract of the APV pipeline cells is shown in (b). A single pipeline cell has 90 % less response compared to a typical cell. The measured response is proportional to the area of the boxes.

pedestal values. Large pedestal variations along pipelines of APV25 chips were reported first in 2002 [48]. Since APVs with pipeline problems are not built into the tracker, the corresponding hybrids are excluded from production. For avoidance of these unnecessary losses the on wafer chip screening was modified. APVs with a large pedestal variation along the 192 pipeline columns are sorted out as well as APVs with individual pipeline cells with abnormal pedestal values [49].
A pipeline failure which is not detected by the screening procedure are pipeline cells with reduced gain. When a signal is applied on the APV input the response signal signal height is strongly reduced compared to other cells of the identical pipeline column. Low gain memory locations reduce the efficiency of the corresponding strips. As there a 192 cells per channel the effect of a single bad cell is almost negligible. Low gain cells are detected unambiguously in the calibration data of the pipeline test. An example for a broken pipeline column and a bad memory cell is shown in figure 5.5.

3) Bond Related Failures

Bond related failures are missing, broken, short circuited and weak bonds. The latter failure type is of great interest because of the of the strong magnetic field in the tube of the CMS solenoid. Weak bonds may reduce the long term reliability of the hybrids significantly. The pull strength is determined using dedicated machines. More information on pull tests is provided in the section on the qualification of hybrids and modules 5.2. About 900 hybrids were lost because of weak bonds in early 2004 [50].

The consequence of a short circuited, missing or broken bond depends on the type

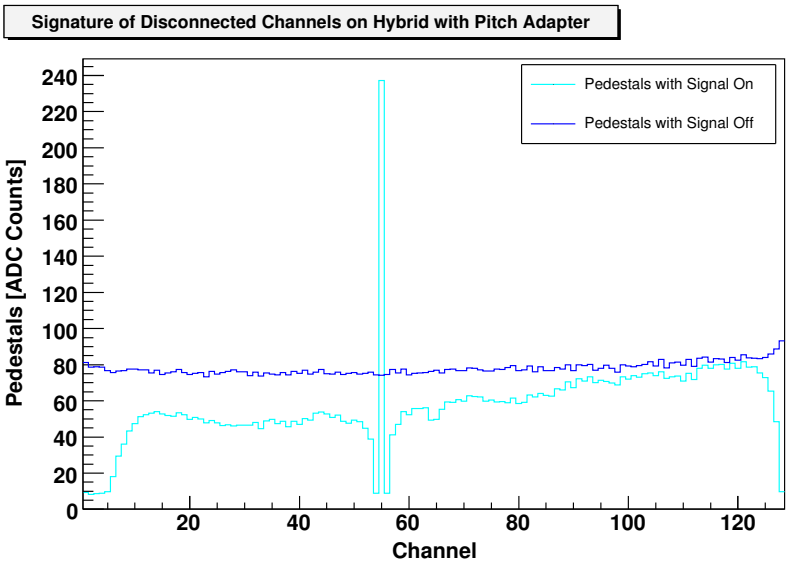


Figure 5.6: Comparison of pedestals with enabled and disabled pulse injection on the pitch adapter. The channels where no signal is applied on stick out sharply from the others. The sign of the response has opposite sign because of the APV internal common mode suppression.

of the affected bond. The hybrid carries control, read-out and high voltage bonds (see 2.4). As the control bonds connect the circuit to the APV a particular failure can have the same implications as a circuit related defect. Since the affected APV does not work properly the defects will be revealed by one of the FHIT tests.

Defect *high voltage bonds* can only be found by a visual inspection. The electrical functionality of these bonds cannot be proved unless the hybrid is assembled on a module.

Missing or broken *read-out bonds* disconnect the APV inputs from the corresponding lines on the pitch adapter. For this reason the channel will be dead when the hybrid is assembled on a module. As long as the module is not assembled, the disconnected channels can only be found by signal injection on the pitch adapter. If roughly the same signal is injected into all APV inputs only those channels will show a response which are disconnected from the pitch adapter. The reason for this unexpected behaviour is the internal common mode correction (see also 2.3.1) of the APV. The situation is different if most of the APV inputs are disconnected from the pitch adapter lines since in this case the total signal on the APV inputs is small. Thus the signals are seen on the connected channels but with opposite sign. In the latter case a huge number of bonds must be broken or missing which will be easy to spot by eye. For this reason those hybrids are sorted out before a test is performed. The feature of signal injection on the pitch adapter is a speciality of the hybrid test station. The pedestals of an APV with enabled and disabled pitch adapter pulse injection are illustrated in figure 5.6.

Short circuited read-out bonds bring the corresponding APV inputs in electrical con-

tact. A signal which is applied on one of the inputs automatically spreads to the other inputs as well, thus it receives a reduced amount of charge. For this reason the signal-to-noise ratio will be lower for short circuited channels and the spatial resolution is reduced. These effects do not seem to significantly harm the overall tracker performance because of the high precision single point measurement and the high signal-to-noise ratio of normal channels. In fact short short circuited APV inputs can have a much worse impact. If four or more pairs of channels on a single APV are short circuited the gain of the entire APV may be reduced. This effect is described in more detail below. The open drain inputs of the APV are not fixed to a common potential. For this reason a current flows between short circuited channels which can significantly distort the inverter stage. The situation is similar to the effect of highly ionizing particles (see also 2.3.1). The higher the signal on the APV input the higher is the voltage drop over the bias resistor of the APV inverter stage. When a certain current is exceeded the inverter stage stops working and all channels of the affected APV become insensitive to incoming signals. The reduction of the response versus the number of shorted APV inputs was measured when the impact on the APV was understood. The APV which was tested became insensitive when four pairs of channels were short circuited. The hybrid which was used for the measurement had a 100 Ω bias resistor for the inverter stages. The hybrids which are used for the tracker carry a 50 Ω resistor which reduces the vulnerability of the APV. Since the potential of the single inputs varies it has to be kept in mind that the exact number of tolerable short circuited inputs depends on the pairs of inputs which are in contact.

Short circuited read-out bonds are detected in the calibration pulse test data. If a channel receives less amount of charge than injected, the response signal height is lower than expected. Furthermore the missing part of the charge is seen at the input of the next or next to next channel. These signatures are definite indications for short circuited inputs. The maximum output signal height of a hybrid with a pair of short circuited channels is shown in figure 5.7.

4) Pitch Adapter Failures

Typical failures of the pitch adapter are short circuited or broken lines. The impact is identical with a short circuited or missing read-out bond and as well is the signature in the data. Only a visual inspection allows to detect the actual error type.
The metallization on the pitch adapter is of great importance. Any contamination can cause difficulties during the bonding procedure.

5) Other Defects

A typical defect which cannot be assigned to one of the other categories are cracks in the ceramic support plates. As the thickness is merely 380 µm to keep the material budget of the tracker low, the hybrids are shock-sensitive. Another threat are twisting

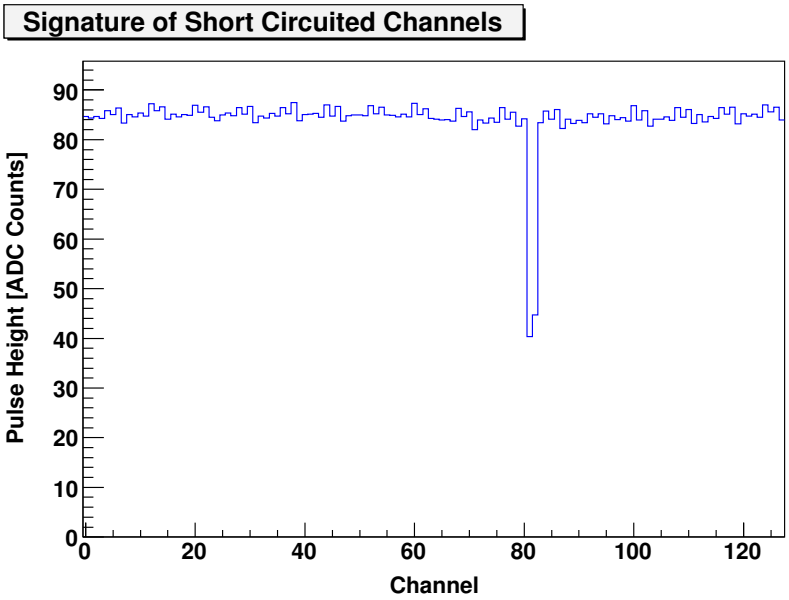


Figure 5.7: Short circuited channels are clearly visible in the maximum APV output signal of the calibration test. While the signal height is reduced by a factor of about two in the inverter off APV operation mode the signal height of shorted channels can vary much more in the inverter on mode.

forces. A repair is not possible because the circuit cannot be easily removed.

5.1.2 Module Faults

In this subsection the various faults on modules are described. As the hybrid is a component of a module all faults which are found on hybrids are in principle also detectable on modules. As bad hybrids should not escape the quality control only good hybrids are found on modules unless they suffered damage after the final inspection. The faults on modules are assigned to one of the following categories:

1. mechanical defects
2. bond related failures
3. sensor defects
4. high ohmic backplane contacts

1) Mechanical Defects

Typical mechanical problems are misaligned components and broken frames. For achievement of spatial resolution in the order of a few micrometres the single components of the tracker have to be aligned at high precision. The alignment of the module constituents is checked on the gantry itself or a coordinate measurement machine.

Some module assembly plates use the precision holes in the frames for fixation during the assembly. In this case dedicated pins on the plate keep the frame in a fixed position. Some frames suffered cracks because the diameter of holes varied and in some cases the rigid steel pins applied a large force. In the case the frame was not seriously damaged the cracks were covered with glue and ceramic rings to guarantee the precision of the hole and to return the mechanical stability. Broken precision holes are spotted by visual inspection under a microscope. The cracks are not easy to find even if the frame is slightly twisted.

2) Bond Related Failures

Like for the hybrid bond related failures on modules are missing, broken, short circuited or weak bonds. Apart from the bonds on the hybrid with bonded pitch adapter modules carry additional read-out and high voltage bonds. Bond failures on modules have the same impact on the tracker performance as the corresponding failures on hybrids.
While the method for the detection of short circuited channels on modules does not differ from hybrids (see subsubsection 5.1.1) the detection of missing and broken bonds is less complicated. A channel with a missing or broken bond is missing a connection to one or two sensor read-out strips. Thus the input capacitance of these channels is reduced which is visible in the data. In dependence of the position of the discontinuity two types of disconnected APV inputs are distinguished. Pitch adapter - sensor opens are missing connections between the APV input and the sensor, Sensor - sensor opens are missing connections between two sensors.
When a test pulse is applied using the APV internal calibration circuit, the response is the more delayed the higher the input capacitance is. At the same time the height of the APV response is lower the higher the capacitance is. For this reason the maximum height of the APV response to signal injection is highest and the delay is lowest for pitch adapter - sensor opens as the sensor read-out capacitor is disconnected from the APV input. The maximum pulse height is lowest and the delay is highest for normal channels while the response of sensor - sensor opens lies in between. The effect is depicted in figure 5.8.

Another measure which is influenced by APV input capacitance is the noise. The lower the capacitance is the lower is the noise. In principle the noise of either type of disconnected channel should be lower compared to normal channels. Because of the APV internal common mode suppression (see 2.3.1) the common up and down movement of the channels is important. The movement is mainly influenced by the potential of the bias ring which is not absolutely stable because of leakage current fluctuations. Disconnected channels are not influenced by the potential of the bias ring in the same way as normal channels. Thus they do not follow the common movement of the majority of the channels and have higher noise because of the internal common mode suppression. If the common mode noise (see 3.6.3) exceeds a certain threshold disconnected channels show higher noise than normal channels. For this reason the noise is not necessarily a good indicator for disconnected channels. Nevertheless the

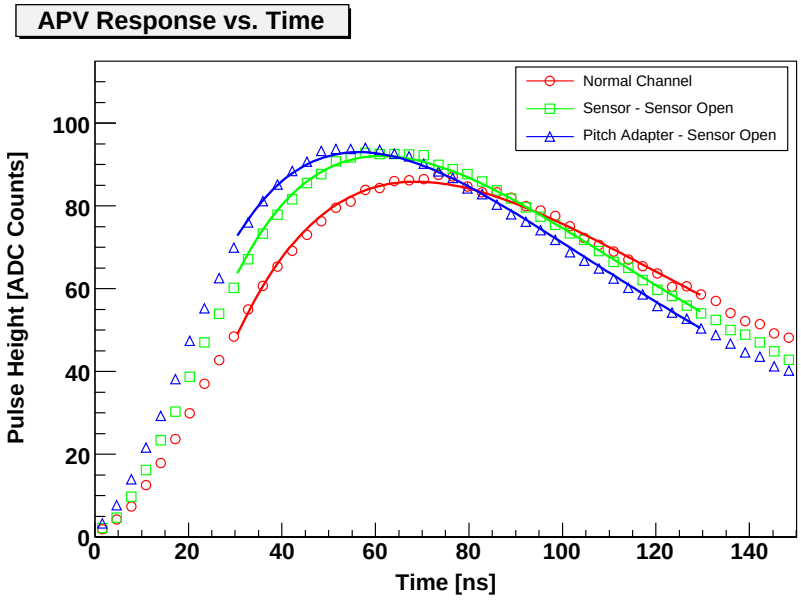


Figure 5.8: The impact of missing or broken read-out bonds on the APV response. The higher the input capacitance of the APV is the more the signal is delayed.

common mode noise is an indicator for proper grounding and shielding of the corresponding test stand (see subsubsection 5.2.3).

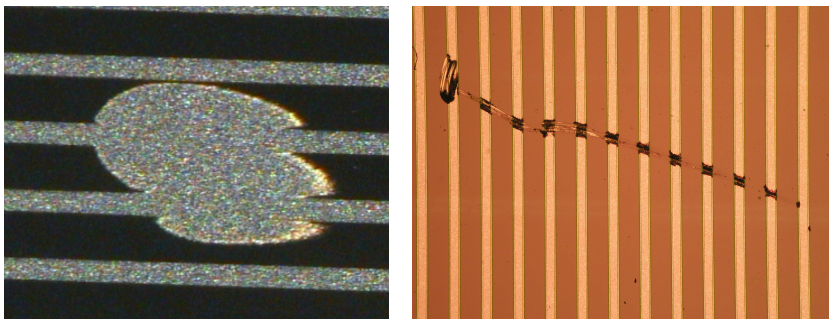
Missing or broken highvoltage bonds are a threat for the module. When the bias ring is disconnected from the hybrid ground its potential is floating. Under bias the potential on the bias ring can rise up to the potential of the sensor backplane. If the strips of the sensor are bonded to the APV inputs the depletion voltage drops across the read-out capacitors which are not proven to stand several hundred volts. Although no damage was observed when a module was operated unintentionally in this way a module should not be biased when the bias ring is floating and the read-out strips are bonded.
The capacitance of an unbiased sensor is large compared to a biased sensor. All channels of an unbiased module show noise values which are at least a factor of two higher compared to modules under bias. The capacity is such high that no response to on chip generated signals is visible in the APV output. Furthermore the measured leakage current is zero.
The higher the number of switched in parallel high voltage bonds is, the lower is the current per bond and the lower is force per bond in the high magnetic field of the CMS solenoid. For the save operation of the modules over years the qualification criteria demands for four redundant high voltage bonds for each connection.

3) Sensor Related Defects

The sensor related defects which affect single channels are short circuited or disconnected aluminium strips and short circuited read-out capacitors. The latter defect can

be persistent in time (pinhole) or temporary (microdischarge). An entire module is lost in case of high sensor leakage currents which are usually caused by a low resistive path between the bias and the guard ring. The single defects are described in more detail below.

From the electrical point of view short circuited aluminium strips are identical with short circuited read-out bonds and pitch adapter lines. All of these failures endanger the function of the entire APV because of their feedback on the inverter stage. Typical reasons for short circuited channels are contaminations during the manufacturing process of the sensors and scratches on the surface which are caused by bad handling. Photographs of these failure types are shown in figure 5.9. The signature of short circuited channels is described in the subsection on short circuited bonds on hybrids 5.1.1.



(a) **(b)**

Figure 5.9: The typical reason for short circuited strips are remnants of metal because of the manufacturing process (a) and scratches (b). The latter failures can also disconnect part of a strip from the read-out.

Aluminium strips which are disconnected on the sensor reduce the dimension of the read-out capacitor. Thus the signal which is injected into the APV because of a traversing particle is reduced. Since the p-implant region is still connected to the bias ring the sensitive region is not reduced.
The signature in the test data is similar to disconnected channels because of missing bonds. The position of the discontinuity determines the dimension of the read-out capacitor. Thus the behaviour in the pulse shape data reaches from normal channels to pitch adapter - sensor opens. The noise of these channels is usually higher compared to normal channels which might be caused by the different interstrip capacitance in combination with the internal common mode suppression of the APV. A strip can be disconnected because of a scratch on the sensor surface (see figure 5.9(b)).

A *short circuited read-out capacitor*, also called *pinhole*, is an aluminium strip which is in electrical contact with the underlying p^+-implant region. As the p-implant is connected to the hybrid ground via a poly-silicon resistor (see figure 2.7) so is the APV input. Since the unaffected potential of the APV input is about 0.75 V with respect to the hybrid ground, a current flows from the APV input into the p-implanted

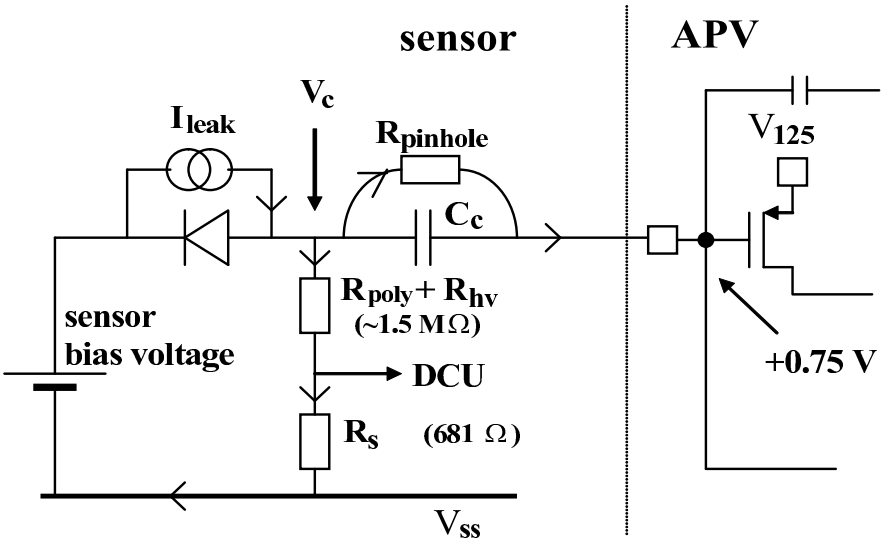


Figure 5.10: The schematic depicts the effect of a bypassed read-out capacitor C_c on the APV input voltage. The APV input voltage accommodates to V_c which is determined by the leakage current I_{leak}. In dependence of V_c the APV sources or drains a current via the resistor R_{poly} (source [27]).

region which is connected to the hybrid ground via a high ohmic path. The schematic in figure 5.10 illustrates the situation. The corresponding channel loses its working point and becomes insensitive to applied charge. While this situation leads to a single lost channel the situation is worse at high leakage currents. After ten years of operation the leakage current of the sensors is expected to be in the order of 1 mA. In this situation the potential of the implanted region is higher than 0.75 V and the current flows reversely. In this situation a transistor in the inverter stage of the APV switches on and draws large currents which affects all inverter stages because of a common bias resistor (see figure 2.14). If the potential for all inverter stages decreases too much the entire APV becomes insensitive in the inverter on mode. Between these two extremes, low and high leakage current, the channel works fine as long as the potential of the implant region is about 0.75 V.

The more pinholes are located on a single APV the larger is the sourced or drained current and the more endangered is the entire chip. An investigation showed that an APV with a 50 Ω inverter bias resistor can tolerate up to four pinholes at nominal supply voltages [27]. An APV which is operated in inverter off mode does not use the inverter stage and tolerates more than 7 pinholes which was the maximum number of pinholes which were mimicked in the investigation.

Since the average number of pinholes is less than one per module and the number is not expected to increase in time pinholes will hopefully not be a threat for the CMS detector. Nevertheless the bonds connecting APV inputs with pinholes are removed for safety reasons.

The gain dependence of channels which are connected to pinholes with respect to the leakage current is a characteristic which applies to no other defect. Thus this signature is an unambiguous indicator for pinholes. The pinhole test (see subsection 3.6.6) shifts

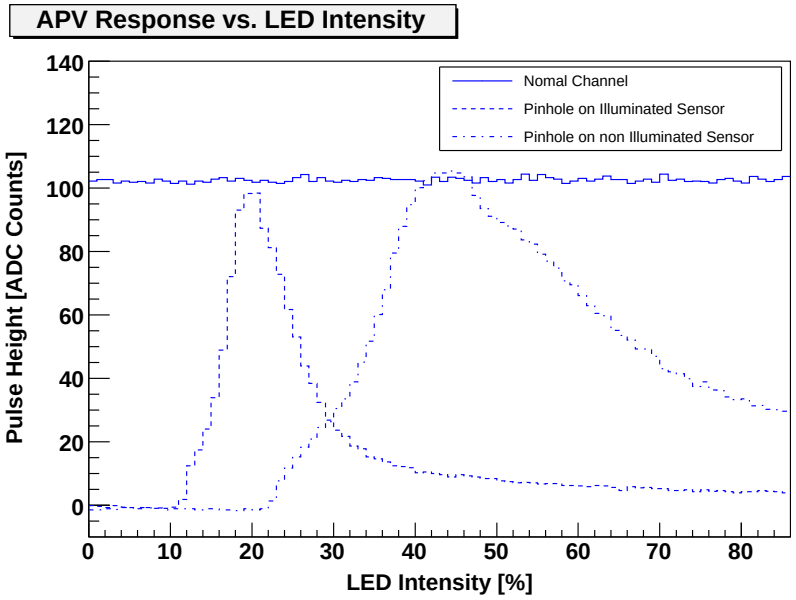


Figure 5.11: The pulse height dependence on the LED intensity is a characteristic of pinholes. At a certain LED intensity (leakage current) the working point of the APV is restored. For lower and higher LED intensities the gain of the APV is negligible.

the potential of the p-implants via the leakage current which is imprinted by the settings of the ARC LED Pulser. As the potential is shifted by at least 0.86 V according to equation 3.13 the above explained sensitivity curve becomes visible. The typical gain dependence versus leakage current is shown in figure 5.11.

The LED intensity at which the maximum signal height is restored provides information on the position of the pinhole. The LED array which is part of an ARC system for module tests illuminates only one sensor. If there is a second sensor the potential of the implants is shifted via the voltage drop over the return resistors (R_{HV} and R_S in figure 2.18) while the potential on the illuminated sensor is also shifted by the additional current across the poly-silicon resistors. Therefore a lower LED intensity is required to bring a channel on the illuminated sensor back to the region of normal operation. At the same time the slope on the rising and falling edge is steeper and the plateau at which the APV works fine is less pronounced.

A special kind of pinhole is called high leakage current or high resistivity pinhole. When the read-out capacitor is bypassed by a high ohmic connection the APV input potential is not identical with the potential of the underlying implant. The voltage drop over the pinhole is such high that the APV does not lose its working point. At high leakage currents the voltage drop over the pinholes becomes such high that the APV cannot source enough current and becomes insensitive. For this reason the signature of high leakage current pinholes differs from standard pinholes. The APV channel works fine at low LED intensities and a decrease in the response height is only seen at high LED intensities.

An effect which is characterized by pulsed signal injection into typically one or two APV inputs is called microdischarge effect. The reason for the effect is not ex-

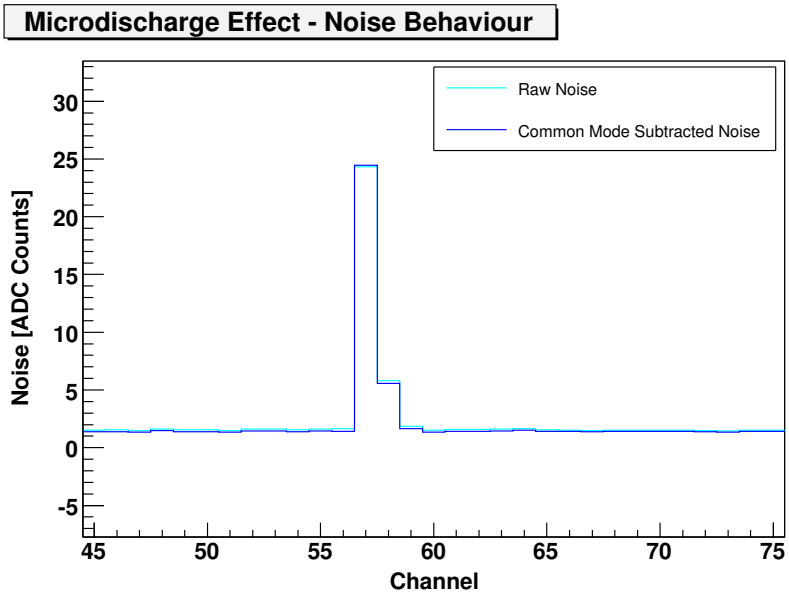


Figure 5.12: The microdischarge effect is detectable in the exceptionally high noise of the corresponding channels. The effect is caused by strips suffering temporary breakdowns of the read-out capacitor.

actly understood as the affected channels have no visible abnormalities. The most favoured explanation is the occurrence of a high electrical field between the edge of an aluminium strip and the underlying p-implant region [51]. The field relaxes by electrical discharge over the insulation layer of the read-out capacitor, increases and again, relaxes and so on. The effect turns on at a certain depletion voltage and influences an entire APV in case the total signal becomes large. Only sensors from STM suffered from this effect.

The strips which suffer from the microdischarge effect show up in very high noise. The raw and the common mode subtracted noise of an affected module is shown in figure 5.12. The noise of a typical channel is often ten times higher compared to the mean noise of all normal channels.

Because of the internal common mode suppression of the APV the discharges may affect all channels of the corresponding chip if the total charge is large. Since the APV internal common mode subtraction does not cancel out the full signal the common mode subtraction which is applied by software for the calculation of the common mode subtracted noise is an additional tool for the detection of the microdischarge effect. The histograms of the common mode corrections for the APV shown in figure 5.12 and an unaffected APV on the same module is shown in figure 5.13.

Modules suffering from microdischarges are not built into the tracker to avoid the possible loss of an entire APV. Furthermore the leakage current of these module is increased and not stable in time. A module which was tested for 20 hours showed a slow decrease of the electrical resistance. Within this time the current rose up to the chosen current limit of the 100 µA. The depletion voltage was 450 V and steadily decreased to 308 V when the current limit was reached [52].

Unexpected high leakage currents are caused by low resistive paths between the

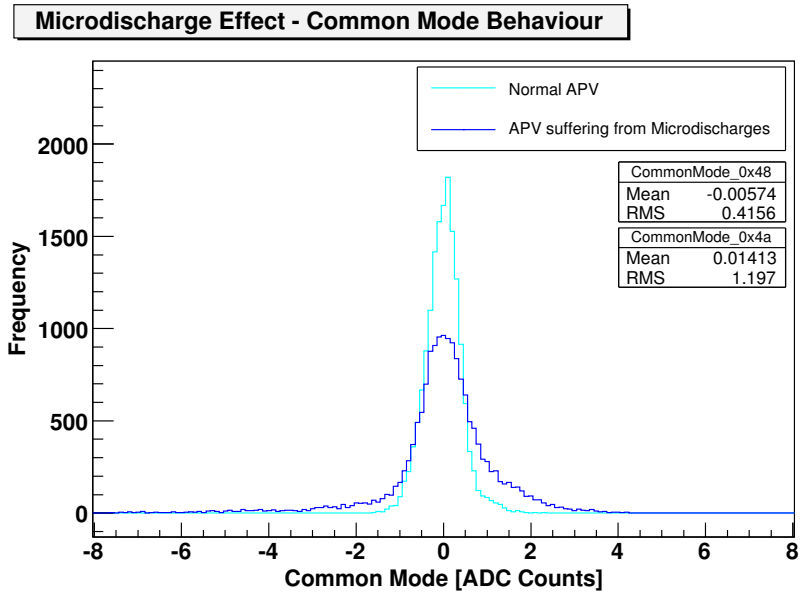


Figure 5.13: The common mode corrections which are applied for the calculation of the common mode subtracted noise depend on the signals which are present on the APV inputs. Since the internal common mode correction of the APV does not compensate for the full signal the RMS of the corrections is larger for APVs seeing large signals.

sensor backplane and the hybrid ground. These paths are created by scratches on the top side of the sensor edges where the electrical potential degrades from the edge via the guard ring to the bias ring (see figure 2.7). The residuals of the ablated metal are deposited between the rings. Thus the electrical fields are stronger and electrical breakdown is much more probable.
The leakage current of an average module is about 1 µA at 450 V. The I-V curve has the typical shape of a diode which is biased reversely. The typical plots of modules with bad depletion voltage stability show a linear increase of the current. In some cases a strong increase of the leakage current is seen when a certain voltage is reached. Examples of typical I-V curves are shown in figure 5.14.

The IV curves are sensitive to the relative humidity and the temperature. The test facilities are usually located in air conditioned rooms. Thus the temperature is about 20°C. For suppression of surface leakage currents it was decided that the relative humidity must be below 30 % when the module is under test. For better comparison of I-V measurments the environmental parameters are automatically determined by sensors on the ARC FE-Adapter when the modules are tested. The reproducibility of data is best when the modules are kept at low relative humidity for a day. Measurements which are done after a shipment, e.g. or directly after intense illumination with light reduce the desired reproducibility. The modules are always tested in absolute darkness because of the extreme sensitivity of the sensors.

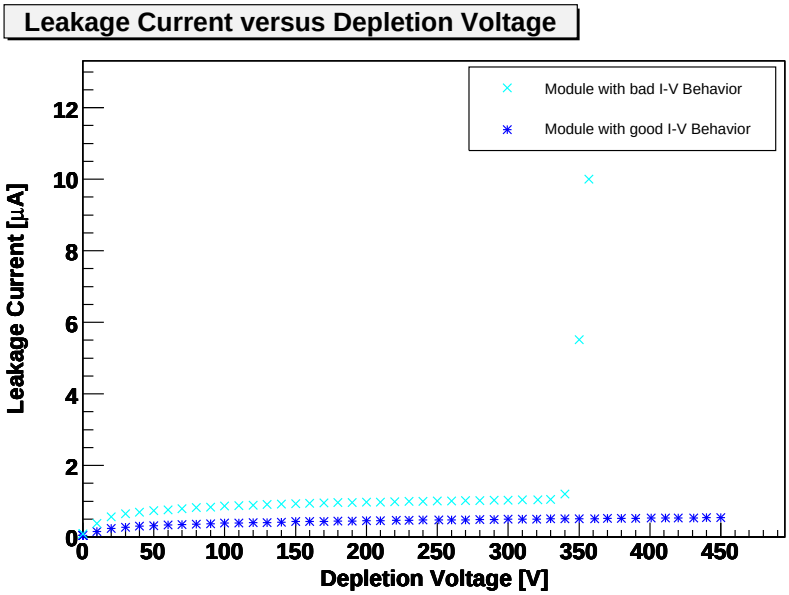


Figure 5.14: The leakage current versus depletion voltage of a normal module has the typical shape of a p-n diode which is biased in reverse direction. Bad I-V behaviour expresses often by a sudden electrical breakdown at a certain voltage as shown in the figure.

4) High Ohmic Backplane Contacts

In the original design for TEC and TOB modules the high voltage is supplied to the sensor backplane via a conductive glue connection. When some connections failed after some time a probing campaign was launched to examine the resistivity of the connections and to assess the increase of the resistivity in time. Furthermore some modules underwent many cooling cycles to get an impression on the reliability of the contact at tracker operation temperature. The original connection which is realized by two dots of glue between the sensor backplane and the copper pad of the kapton cable which carries the high voltage line, was found to be unreliable because of an insulating aluminium oxide layer on the sensor backplane. In the new design the connections are enhanced by adding more glue and the mechanical removal of the oxide layer prior to the application of the glue. For safety reasons the largest fraction of the modules is also equipped with bonds between the copper pads and the sensor backplane.
Failing high voltage connections connections are found in the functional tests as the sensors are not depleted which results in high noise and zero leakage current. If the resistivity is less than $\approx 1\,\mathrm{M}\,\Omega$ the failure remains undetected by the tests as the sensor leakage current is typically 1 µA and the voltage drop over the contact is negligible. The test which is most sensitive to this fault is the pinhole test. When the leakage is several hundred µA the voltage drop over the contact is not negligible. The higher the leakage current the higher is the voltage drop over the contact. When the corresponding sensor becomes not fully depleted, the capacity rises and the response to the test signals decreases. In the data of the pinhole test it looks as if all channels were affected by high leakage current pinholes. As pinholes are rare it is very unlikely to mix the

failures up.

5.2 Qualification Procedures

For the construction of good modules, components of high quality are needed. For this reason all module components undergo a qualification procedure which consists of visual inspections and measurements for the determination of relevant properties.
In the following two subsections the qualification procedure from the bare hybrid to a fully functional module is described. The focus is put on the electrical and functional characterization since these measurements are done with the ARC system. Information on the screening procedure for the front-end read-out chips and the sensors are given in [49] and [53].

5.2.1 Hybrid Qualification

The hybrids are assigned to production batches which contain typically 300 pieces of identical type[2]. The hybrid circuits are cut out of plates each carrying between 32 - 42 pieces. The quality of each batch is determined by a number of checks which are done at the manufacturers (Cicorel and Hybrid SA), CERN and IRES[3]. Regular hybrids, dummy hybrids[4], bare circuits and test structures which are implemented on the plates are investigated for determination of the overall batch quality.
The results of the distinct tests are summarized in a report. If no indication for serious problems is observed a batch is accepted for the next assembly step which is the pitch adapter assembly.
The chosen approach has two major advantages.

- The quality of each batch is well documented.
- The manufacturers are integrated in the quality control.

The documentation provides an overview on the evolution of the production quality. In case of degrading properties actions can be taken before the hybrids run out of the specifications. The integration of the manufacturers provides a fast feedback loop to the production sites in case of problems.
The procedure for the hybrid quality assurance at CERN consists of the following steps.

1. registration in the database and assignment to the corresponding batch

[2] A list of types is shown in table C.5.
[3] Institut de Recherches Subatomique Strasbourg, `http://ireswww.in2p3.fr`
[4] Dummy hybrids are hybrids which are mounted with mechanically intact but electrically broken APVs.

2. incoming inspection
3. pull tests
4. daisy chain measurements
5. FHIT measurements

1. Registration and Batch Assignment Each hybrid is stored in an ESD (**e**lectro-**s**tatic **d**ischarge) protected box. A unique number is printed on a label which is attached to each hybrid and the corresponding box at the manufacturer. When the hybrids arrive at CERN the identification numbers, so-called object ids, are registered in the database. The second step is the assignment of hybrids to the corresponding production batch. Whenever data is uploaded to the database the corresponding object information is available because of the object id which is part of all tables which contain information on individual objects. The most important ones for the electrical and functional qualification of hybrids are described in appendix D.2. For the detection of production related problems it is essential that the hybrids can be traced once they are registered and that data can not only be assigned to the hybrid but also to the corresponding batch.

2. Incoming Inspection The mechanical properties are determined by the measurement of the circuit thickness and a visual inspection. The thickness of the circuits is measured on the bare pieces. Large thickness variations cause difficulties during bonding and module assembly. The visual inspection covers the following items:

- cleanliness of the circuits
- quality of the solder joints
- adhesion of the circuit on the ceramic support plate
- position of the APVs
- mechanical integrity of the APV surface
- roughness of the metal surface
- determination of the bond feet width on the APV and the circuit
- loop height and shape of the bonds

3. Pull Tests The quality of the control bonds is determined by pull tests. Dedicated machines remove single bonds and measure the force at which the bond wire breaks loose. As it is not easy to replace removed bonds on the APV the pull tests are performed on dummy hybrids. Additional pull tests are performed on the plates the circuits a cut from.
Roughly speaking a good bond brakes lose close to the bond foot where the diameter of the wire is smallest. The typical pull force is about 8 - 9 g equivalent. Bonds with a pull force of less than is 5 g equivalent are called weak. More information on pull tests at CERN is given in [54].

4. Daisy Chain Measurements An impression on the metallization quality of the layer interconnecting vias is gained in daisy chain measurements. Beneath each circuit 80 daisy chained vias are implemented for test purposes. As all test structures on a certain plate are connected in sequence a single resistivity measurement proves the function of up to $42 \cdot 80$ vias. The daisy chained vias of all plates are measured at CERN and compared with the results from Hybrid SA. High resistivity and discontinuities are indicators for badly metallised vias.

5. Measurements with the FHIT tester The first electrical and functional characterization of hybrids is done at the company which is in charge of mounting the chips and passive components, Hybrid SA. A „Full IT“ test is performed which consists of all tests which are available in the FHIT software (connectivity, electrical and functional test). An identical test is done at CERN. The initial test is called production test in comparison to the CERN reception test. At both sites a dual FHIT tester is used for the measurements to increase the throughput.
The faults which are detected by the FHIT measurements are all faults which influence the electrical behaviour of the hybrid and almost all faults which distort the function. Three APV failures are not detected by the FHIT. The detection of sticky pipeline columns or cells, low gain pipeline cells and defect APV inverters is a time consuming task as a deep study of the pipeline columns is required or a pulse injection test in inverter on and off mode must be performed. These rare faults are detected in the single module test stands where many sites are involved and test time is less critical. The hybrid under test is illuminated with a table lamp during the FHIT test. This is done to increase the sensitivity to a circuit fault which disconnects a reference voltage to the APV. The missing reference causes a slow baseline drop which is not detected by the tests. When the APVs are illuminated the baseline drops within seconds.
Because of the time constraints the number of acquired events in the functional tests is rather small. For example the number of events which are acquired for the determination of the noise and the response to calibration signals is 1000. Since the data acquisition rate of the ARC board is ≈ 140 Hz the two tests take ≈ 14 s which is a fourth of the total test time. The total test time for each hybrid test is measured by the FHIT and recorded in the database. The distribution is shown in figure 5.15. The data regards those tests which were done at Hybrid SA and where the latest FHIT firmware

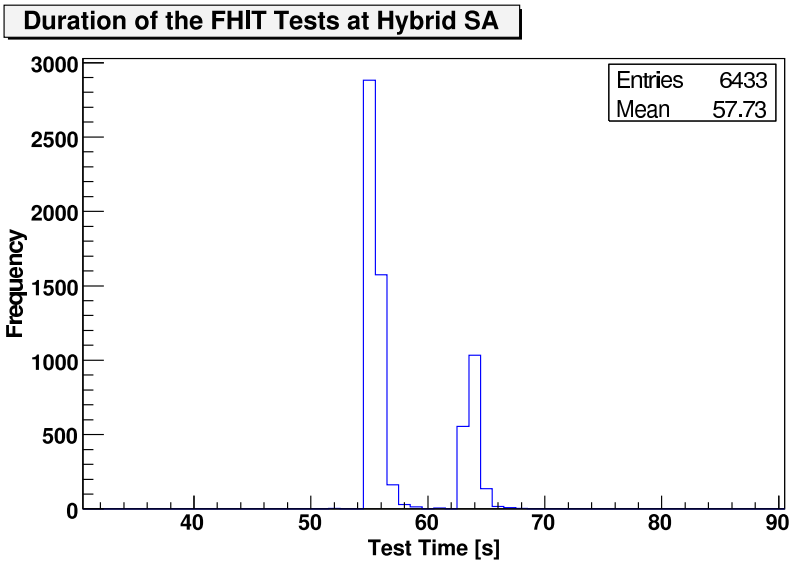


Figure 5.15: The distribution of the duration of FHIT tests at Hybrid SA. The total test time for six APV hybrids is higher compared to four APV hybrids. For this reason two peaks are visible in the data.

grade	**criteria**
A	total number of bad channels < 1 % no connectivity or communication errors
B	total number of bad channels < 2 % no connectivity or communication errors
C	total number of bad channels $\geq$ 2 % or connectivity of communication failures

Table 5.1: The criteria for the assignment of hybrids to certain grades of quality.

was installed. The two peaks in the distribution are caused by the different numbers of APVs on the hybrids. A test lasts longer for six APV hybrids as more I^2C accesses are performed. The mean test time is about one minute.

Several cuts are implemented for the detection of faults. The height of the digital header DH_h must be $200 \leq DH_h \leq 255$ when two resistors of the MUX chips are enabled. The MUX resistors must be homogeneous. When different combinations of two resistors are switched in parallel the absolute difference from the mean height must be less than five ADC counts. The tolerated common mode subtracted noise $CMSN_i$ of a channel i is not allowed to exceed 30 % around the mean noise $\bar{CMSN}$. Furthermore an absolute noise cut is implemented. The noise of each channel must be within $0.2 \leq CMSN_i \leq 1.5$ ADC counts. The last cut concerns the response of the APV to injected signals which must be higher than 20 ADC counts at the maximum.
The grade of the hybrid is determined according to table 5.1. The test results are not always reproducible. Hybrids which fail the reception test are retested on both positions of the dual FHIT. If these tests are passed the hybrid is used for module production. The hybrids with persistent errors are sent to IRES.

The quality of a batch is determined when all tests are done. The results are summarized and discussed with Hybrid SA. If the batch is accepted the good hybrids are used for further production.

5.2.2 Hybrid with Pitch Adapter Qualification

The hybrids which pass the qualification tests are assembled with a pitch adapter which are visually inspected under a microscope prior to the assembly. Short circuited strips are not tolerated as well as more than three discontinued channels. After the assembly process on the CERN gantry the position of each pitch adapter is verified and the glue deposition is checked by eye. The assembled objects which pass the control are provided with read-out bonds between the APV and the pitch adapter and high voltage bonds between the hybrid circuit and the pitch adapter. The hybrids which are not bonded at CERN undergo a final visual inspection before they are sent to the other centres which participate in hybrid bonding activity.
The quality of the bonds is assessed by pull tests. The APV input bond pads have a rectangular geometry of 136 $\times$ 58 µm and a pitch of 44 µm. For this reason the clearance between the bonds which have a diameter of 25 µm is small the more so as the bond feet are typically 25 % wider than the bonds.
When a bond is pulled the foot usually remains on the bond pad and reduces the available space for a replacement bond. For this reason pull tests on APV to pitch adapter bonds are limited to a minimum. The pitch adapters provide dedicated pads for test bonds which provide information on the adhesion of the bonds to the metal of the pitch adapter. Since the bonding quality of the metal on the hybrid was already checked on the plates for the circuit during the qualification of the bare hybrids the quality of the high voltage bonds is derived from these measurements and the pitch adapter test bonds. Like for the control bonds the minimum pull force must be at least 5 g equivalent. At least three high voltage bonds must be placed between the circuit and the high voltage return line to increase the reliability over the years of LHC operation.

The electrical and functional qualification of the hybrids with assembled and bonded pitch adapter is done on the hybrid test stations. The measurements which are performed are intended for verification of the electrical and functional integrity of the hybrid after assembly and bonding. Furthermore the electrical connection of the APV inputs to the corresponding pitch adapter lines is checked and the behaviour of the hybrid at tracker operation temperature and humidity.
The tests which are performed are:

1. pedestal and noise test (APV operation mode: deconvolution, inverter on)
2. pedestal and noise test with switched on pulse injection
3. calibration test (APV operation mode: peak, inverter off)

The single tests are described in subsection 4.2.2. Since not all hybrids are bonded at CERN the tests are performed in various centres. The time constraints vary

centre	number of thermal cycles	rate
CERN	0	$\approx$ 80 %
	10	$\approx$ 20 %
UCSB	1	$\approx$ 80 %
	5	$\approx$ 20 %
Fermilab	1	100 %

Table 5.2: The number of thermal cycles applied on hybrids with assembled and bonded pitch adapter during the mass production.

from centre to centre and thus the chosen test scenario does. While ten thermal cycle runs were an integral part of the qualification for each hybrid with pitch adapter at the beginning of the production, the qualification procedure was adapted during mass production. As no serious incidents were observed at low temperatures the number of thermal cycles and the rate at which they are performed were reduced to increase the throughput. The rate and the number of cycles which are performed in the three centres which are equipped with a hybrid test station is summarized in table 5.2. The thermal cycles typically range from 30°C to -25°C. During a typical scenario the hybrid is read out before the cycles are started and after the last cycle. A third measurement is done during one of the low temperature phases. This series of tests is started when the temperature of the test station is stable by $\pm$ 1°C. The number of tests per month is indicated in figure 5.16.

The integrity of the hybrid is checked during the initialization phase of the test station software. The noise of each channel is determined in the pedestal and noise test. An additional run this time with the external pulse injection switched on serves for the detection of electrical discontinuities between the APV inputs and the sensor side of the pitch adapter. The calibration test is performed for the detection of short circuited channels.

It takes about 35 minutes to cool the test station from 20°C down to -22°C. The temperature change with opposite sign takes typically 6 minutes. As the total test time per hybrid is about one minute a test run including one thermal cycle and three read-out cycles on each of the four hybrid positions takes about 53 minutes. If mounting and initialization phase are included four hybrids can be tested per hour.

The APV is operated in deconvolution inverter on mode during the pedestal and noise test. The noise criteria for a good channel is $0.6 \leq CMSN_i \leq 1.3$ ADC counts. Where $CMSN_i$ is the common mode corrected noise of channel i. The criteria for the detection of short circuited channels is a reduced response to injected signals. While the response of normal channels in peak inverter off mode is about 70 ADC counts a shorted channel is identified by a response of less than 50 ADC counts. Discontinuities are detected by a cut on the pedestals with enabled external pulse injection. For each channel ch the pedestal difference to its neighbours is calculated
$PDIFF_{ch} = 2 \cdot P_{ch} - P_{ch-1} - P_{ch+1}$ and the absolute value minus the mean value of the corresponding APV $PCOR_{ch} = P_{ch} - \frac{1}{128} \sum_{ch \in APV} P_{ch}$. The plot for a hybrid

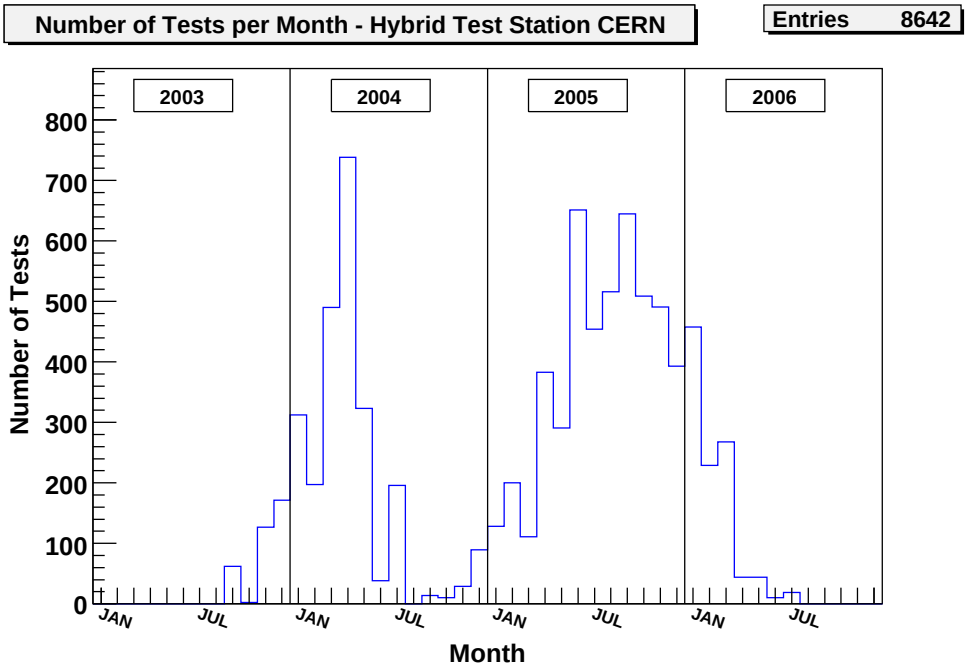


Figure 5.16: The number of tests which were performed at the hybrid test station at CERN. The rate of the performed tests dropped to zero when the problem with the layer interconnecting vias was found.

with a single disconnected channel is depicted in figure 5.17. The black line marks the regions for good channels and disconnected channels. The criteria for bad channels is given by:
$PCOR_{ch} > 140 - PDIFF \cdot 0.1$.

The hybrids are assigned to quality classes according to table 5.3. A certain number of noisy channels and missing bonds are tolerated while short circuited channels are not. The reason for not accepting short circuited channels is the possible impact on the entire APV as mentioned in subsubsection 5.1.1.
The hybrids which pass all tests undergo a final visual inspection with a microscope and an optional cleaning process with dry air, pure water or alcohol, before they are sent to the gantry centres. The inspection is done to spot pushed bonds, contaminations on the pitch adapter and the hybrid and to verify the integrity of the fragile object.

5.2.3 Module Qualification

The gantry centres receive the hybrids with assembled pitch adapter[5] to assemble them with a frame and one or two sensors. Before the hybrids are assembled a visual inspection is done to screen the physical integrity of the object after the shipment. Furthermore the electrical and functional behaviour is checked by an ARC fast test.
After the assembly of a module the position of the single module constituents is proved

[5] In the further progress of this section simply called hybrid.

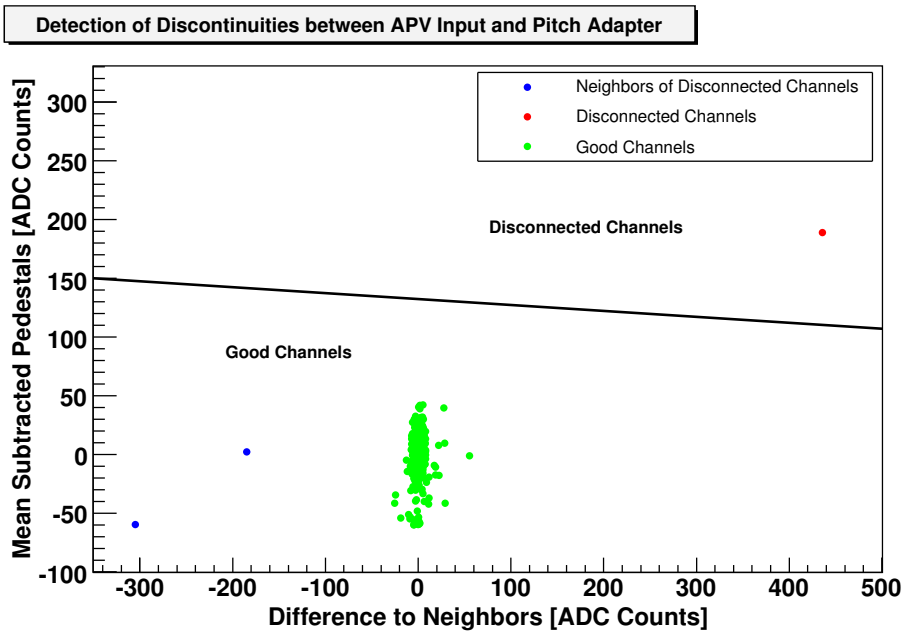


Figure 5.17: Discontinued electrical connections are found by a cut on the absolute pedestal value corrected by the mean pedestal of the corresponding APV and the difference to the neighbours.

grade	number of APV	criteria
A	4	total number of bad channels < 3 and no shorted channels
	6	total number of bad channels < 4 and no shorted channels
B	4	$3 \leq$ total number of bad channels < 5 and no shorted channels
	6	$4 \leq$ total number of bad channels < 7 and no shorted channels
C	4	total number of bad channels ≥ 5 or at least one pair of short circuited channels
	6	total number of bad channels ≥ 7 or at least one pair of short circuited channels

Table 5.3: The assignment of hybrids with pitch adapter to categories of quality.

by the gantry or a coordinate measurement machine. As an example the achieved precision in the coordinate perpendicular to the strips is shown in figure 2.21 (see also [55]). CMS notes on the final results from all collaborations are in preparation.
At the end of the assembly the modules are visually inspected. The glue must be deposited properly to assure the mechanical stability of the module. At the same time glue is not allowed to contaminate the bond pads on the pitch adapter or the sensors.
The bonding centres turn a module into a fully functional detector by adding the missing read-out and high voltage bonds. The quality of the bonds is checked by pull tests of every 50th bond. The pull force of each bond must be at least 5 g equivalent to pass the test. Furthermore it is assured that each high voltage connection is guaranteed by at least three bonds.
The next qualification step determines the electrical and functional behaviour of the completely functional module. The test is performed on the single module test stations in the various bonding labs and is intended for detection and identification of all faults which influence the electrical behaviour of a module. The tests which are performed are:

1. I-V test
2. fast test
3. pedestal and noise test in all APV operation modes
4. calibration pulse test in all APV operation modes
5. pipeline test, APV operated in peak inverter on mode
6. pinhole test, APV operated in peak inverter off mode

The I-V test is done first because all consecutive tests are designed to probe the properties of a depleted module. The voltage is ramped from 0 V to 450 V in 45 steps. When a chosen voltage is reached ARCS waits five seconds before the current is measured since the current decreases significantly in the first few seconds. A the maximum voltage a second measurement is performed with a delay of five seconds after the first measurement for judgement of the time dependence of the current. The test starts in the best resolution current range of the DEPP board. If the leakage current exceeds 10 µA the test is restarted with 50 µA current limit. At the end of the test the voltage is ramped down to 400 V which is the depletion voltage all other tests are performed at.
The fast test proves the communication with the single ships. Since this is essential for all consecutive tests the fast test is performed before the other tests are started. The pinhole test is performed last because a high leakage current is created which might still have an effect when the test is finished. The sequence of the other tests is arbitrary. Two tests are done in all APV operation modes to be sensitive on mode dependent faults. The qualification procedure was worked out by a group of people who authored a CMS internal note which provides further information [56].
Some faults are detected unambiguously in a dedicated test, e.g. the MUX switching failure in the fast test. Other failures like broken APV inputs, disconnected and

shorted channels or pinholes leave a signature in various tests. Thus a combination of test results is suited best for exact failure identification. The strategy for the detection of faults is the usage of a set of cuts for each module type. These cuts are applied in all centres since it would be extremely difficult to compare the final results if each centre would have its own set of cuts. The cuts which are used by ARCS are absolute, percentage and σ cuts. The method which is used to derive the cuts and the algorithm for failure identification in ARCS is described in [37].
The signature of the defects in the various tests is summarized in table 5.4.

	CMS Noise	Pulse Height	Crosstalk	Peak Time	Pinhole Difference	Pinhole Maximum	Pipeline
disconnected channel	low[1]	high !		short !		high	
short circuited channel	low or high	$\approx \frac{1}{2}$[2]	high !		low	$\approx \frac{1}{2}$[2]	
noisy channel	high !						
pinhole	low	≈ 0			high !		
dead APV channel	low	≈ 0 !					
defect inverter		low ![3]					
defect pipeline cells						high[4]	!
discharge effect	very high !	-	-	-	-	high[5]	-

[1] Except for discontinuities on the sensor for which the noise is high.
[2] This rule applies only for inverter off operation modes.
[3] The effect is more pronounced in inverter on modes.
[4] When a low gain pipeline cells is hit the average pulse height is reduced.
[5] If the injected charge is very large the difference is large for all channels

Table 5.4: Overview on the signatures of the faults in the various tests. Empty fields indicate data which is not sensitive or significant for the identification of the corresponding fault. An exclamation mark indicates data which is most typical for the corresponding failure type. A hyphen indicates data which is corrupted by the fault.

At the end of the test ARCS assigns a quality flag on each channel which is part of the XML file for the database. The possible flags are listed in table D.1 in the ap-

grade	number of APV	criteria
A	4	total number of bad channels < 6 and I_{leak}/sensor < 10 µA
	6	total number of bad channels < 9 and I_{leak}/sensor < 10 µA
AF	4	total number of bad channels < 6 and $I_{leak} < 5 \cdot \sum_{sensors} I_{leak,sensor}$
	6	total number of bad channels < 9 and $I_{leak} < 5 \cdot \sum_{sensors} I_{leak,sensor}$
B	4	$6 \leq$ total number of bad channels < 11 and I_{leak}/sensor < 10 µA
	6	$9 \leq$ total number of bad channels < 16 and I_{leak}/sensor < 10 µA
BF	4	$6 \leq$ total number of bad channels < 11 and $I_{leak} < 5 \cdot \sum_{sensors} I_{leak,sensor}$
	6	$9 \leq$ total number of bad channels < 16 and $I_{leak} < 5 \cdot \sum_{sensors} I_{leak,sensor}$
C	4	total number of bad channels ≥ 11 or I_{leak}/sensor ≥ 10 µA
	6	total number of bad channels ≥ 16 or I_{leak}/sensor ≥ 10 µA

Table 5.5: The criteria for the assignment of modules to categories of quality.

pendix. Furthermore a human readable file is created which contains the list and the type of the detected faulty channels as well as the total grade. The grade depends on the number of bad channels and the leakage current. If pinholes or dead APV channels are detected the corresponding strip is disconnected by removal of the bond. This procedure increases the reliability of the corresponding APV. All channels suffering from pinholes are turned into disconnected channels. The criteria for the assignment of a grade after the removal of all pinholes is given in table 5.5. The conditions are applied on all test results of single module tests.

Modules of grade A and B are assembled on the tracker sub-assemblies. Modules of grade C are not used unless they are turned into a grade A or B module because of a repair. Unrepairable grade C modules are dismounted for recuperation of the valuable sensors.

A further step in the electrical and functional qualification of single modules is a test at tracker operation temperature. The modules are assembled at about 20°C and operated at $\approx$ -15°C. Since modules are constructed from components with different thermal expansion coefficients the mechanical integrity of the modules at tracker operation temperature is a concern. All TIB and TID modules undergo the test while single TEC and TOB modules were only tested at the beginning of module production for evaluation of the design.

Thermal cycles on single modules are performed on the module thermal cycling test

stands. Apart from the pinhole test which cannot be performed because of the missing LED array the same tests as for the qualification of modules after bonding are performed.
When the modules arrive at the integration centres a final visual inspection is performed for control of the mechanical integrity of the bonds, the frame and the sensors. The final electrical performance is assessed by an I-V test and a fast test on single module test stations. If the module is of grade A or B according to table 5.5 it is assembled and the qualification of single modules has come to an end. The tests and the grading of the tracker sub-assemblies is not part of this thesis. Papers and notes on the qualification procedure for the assembled objects are in preparation.

The fault detection strategy demands for a set of cuts which is applied by all centres. This approach allows to derive the reproducibility of results by comparison of the raw data. While all test stands are based on the ARC read-out system which is the basis for the chosen approach each test centre designed their own test box. As the test box is known to significantly influence the noise behaviour of disconnected channels a campaign was started to assess the reproducibility of test results. The comparison of the single module test stands in the TEC collaboration is described below.

Comparison of the TEC Single Module Test Stands

A campaign was risen for comparison of the signatures of the most typical faults affecting single channels on modules. The consistent behaviour of faulty channels is essential for distinction of failures on the basis of a common set of cut parameters which is highly desirable to simplify the comparison of results and the development of a fault finding algorithm which works for all centres.
The detection of typical faults is based on data from the pedestal and noise, the pulse shape and the pinhole test. When the investigation was started faults were identified by the absolute level of the common mode subtracted noise, the position of the peak time with respect to the average channel of the corresponding APV, the pulse height divided by the average pulse height of the corresponding APV and the pulse height difference in the pinhole test. Since the peak time, the pulse height and the pulse height difference were known to be good indicators for faults, the noise especially of pitch adapter - sensor opens were known to be somewhat problematic because of their dependency on the common mode noise. For this reason the aim of the campaign was the assurance of common mode noise levels which do not govern the common mode subtracted noise of disconnected channels. Furthermore the distinction of failures in the more robust data was a key issue. Each collaboration started its own comparison of the test stands. During the so-called TEC cross-calibration tour a hybrid, a hybrid with assembled and bonded pitch adapter and two modules were tested. The participating TEC centres in alphabetical order are:

- Aachen, Rheinisch-Westfälische Technische Hochschule, I. Physikalisches Institut B

- Aachen, Rheinisch-Westfälische Technische Hochschule, III. Physikalisches Institut B
- Brussels, Vrije Universiteit
- Karlsruhe, Institut für Experimentelle Kernphysik
- Lyon, Institut de Physique Nucléaire
- Strasbourg, Laboratiore d'Électronique et de Physique des Systèmes Instrumentaux
- Wien, Institut für Hochenergiephysik
- Zürich, Eidgenössische Technische Hochschule

Although Brussels and Lyon are not involved in module testing they participated for check of their test stands for hybrids with bonded pitch adapter. Before the tests were started all ARC boards were flashed with the latest firmware version. ARC components were replaced if a substitution seemed necessary, e.g. the DEPP board was not programmed with the correct oscillator frequency. During the test of modules the relative humidity was reduced to less that 30 %. All tests were performed with ARCS version 6.1. A complete set of tests consisted of the following measurements:

- fast test
- pedestal and noise test in all APV operation modes
- calibration pulse test in all APV operation modes
- gain test in all APV operation modes
- pipeline test in all APV operation modes
- pinhole test in peak inverter off mode (only modules)

The tests were performed on the test stands which were located in the labs where the qualification of the components was intended during series production. The most relevant tests for a particular centre were repeated on a reference test system which was provided by Aachen IIIB. Tests on modules were only performed in the centres that are involved in module testing while the other test objects were tested in all centres. A summary table indicating the tests which were performed with the read-outs of the various centres is shown A.9 and A.10 in the appendix. Each centre is identified by a number for anonymisation.

Measurement of bare Hybrid The measurement of the bare hybrid is performed for basic comparison of the ARC read-out systems. The mean common mode corrected noise in deconvolution inverter on mode is shown in figure 5.18. The reproducibility of such measurements was determined by a measurement which is described in appendix A.2. The rms of the mean noise is about 0.001 ADC counts. Because of the small errors the difference in the data of the various centres is significant but such small, the maximum difference in the plot is 0.012 ADC counts, that no influence on the fault detection is expected. The largest difference was 0.042 ADC counts which was observed for peak inverter on mode. Even this difference is negligible. Plots which provide an overview on the mean raw and common mode subtracted noise are shown in appendix A.3.

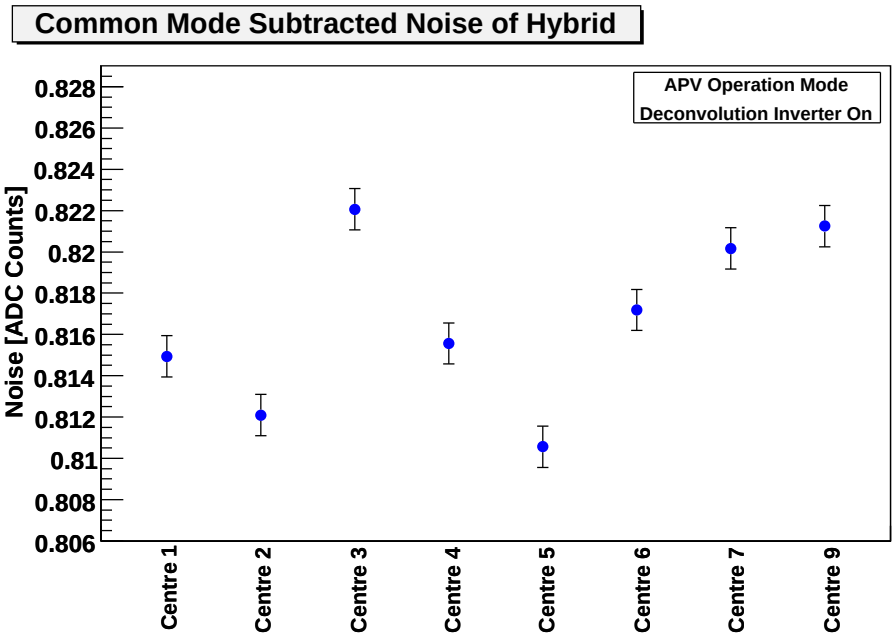


Figure 5.18: Mean common mode subtracted noise of hybrid measured in peak inverter on mode. The error bars are derived from a measurement which is described in appendix A.2.

Measurement of Hybrid with Pitch Adapter The hybrid with assembled and bonded pitch adapter is sensitive to the environmental conditions and the grounding and shielding scheme of the test box. For the reference test system a proper connection between the four grounding points in the corners of the ARC FE_M printed circuit board and the test box is established. Furthermore all parts constituting the outer part of the box are in good electrical contact. As floating power supplies are used the common ground is realised via the flat cable from the PC. If applicable the same scheme was established on those test stands where increased noise was observed. The common mode corrected noise after the modification of the test stands is depicted in figure 5.19. In three centres additional measurements were performed with the reference test system.

The „body“ of the distributions where most channels are contained look quite differ-

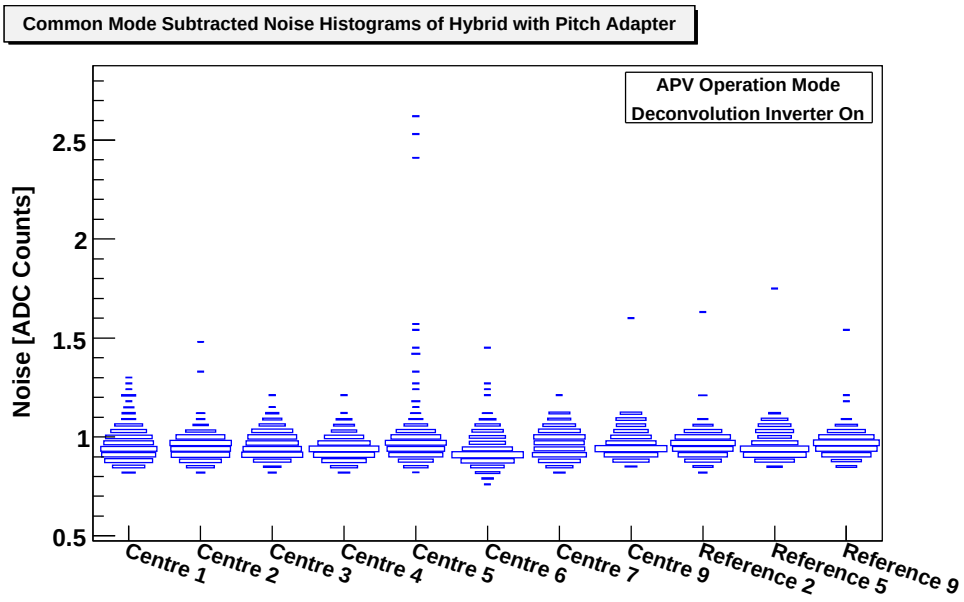


Figure 5.19: Mean common mode subtracted noise of hybrid measured in different centres.

ent from centre to centre and even for the reference test system. Although these shapes catch the eye they are not really interesting as they are cause by small noise variation. Most interesting is the noise level of the channels with high noise and the number of these channels. There is an obvious discrepancy in the data of centre five where the test stand consisted of a heat sink for but no shielding was foreseen. The measurement which was performed with the reference test system in the same centre shows that the noise can be significantly reduced if an operated properly test box is used instead. The data of the three reference measurements and the data of centre five is superposed in figure 5.20. Usually the outermost channels show the highest noise values. For centre five the noise is highest at the edges of the central APVs which is unusual. Although the noise pick up is not as bad as depicted in figure 4.8 a test box is needed to decrease the noise and allow tests under controlled conditions.

Measurement of Module Two modules were tested in the seven TEC centres that are involved in the qualification of completed modules. Both modules are of TEC ring six type and are made of two sensors. Since defects are rare the modules were prepared with additional faults. Some read-out bonds between the pitch adapter and the first sensor and between both sensor were removed intentionally to disconnect strips. Short circuits were caused by additional bonds which connect two aluminium strips of a sensor. Bonds which are placed between the DC pad and the read-out strip of a particular channel mimic pinholes as they short circuit the read-out capacitor. Photographs of the modifications are shown in figure 5.21.

Two modules were tested to have a backup solution in case one module would have

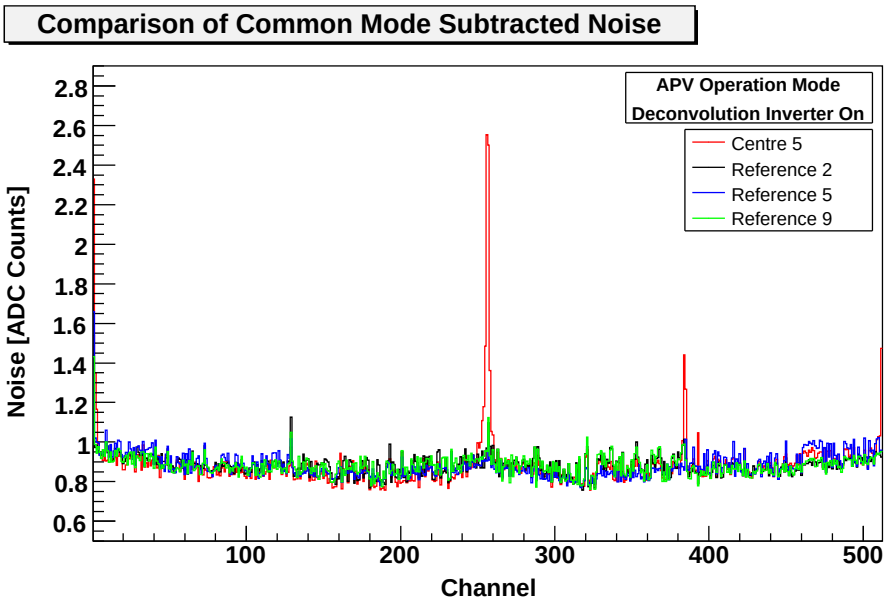
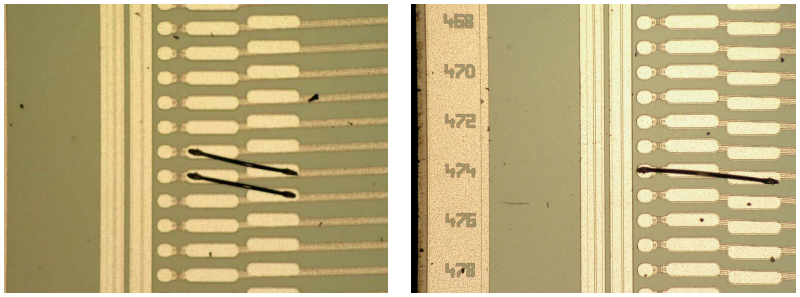


Figure 5.20: Mean common mode subtracted noise of hybrid measured in different centres.



(a) **(b)**

Figure 5.21: Short circuits and pinholes are created by electrical connections between the strips of adjacent channels (a) and between the dc pad and a strip (b).

suffered serious damage during transport or handling. The modules are distinguished by the last three digits of their identification number. Here the data of module 664 is shown. The modifications which were applied on this module are summarized in table 5.6.

A measure which is suited to characterize the grounding and shielding of a test stand is the RMS of the common mode also named common mode noise. The mode which is most sensitive to the above named properties of the test stand is the deconvolution inverter off mode. The common mode noise of the seven test stands is given in figure 5.22 where each point represents the common mode noise which was determined for a certain APV.

The data represents the situation after the successful modification of some test stands. Most striking is the common mode noise for centre six. While the mean common

type of failure	strips
pitch adapter - sensor open (PSO)	83, 256, 512
sensor - sensor open (SSO)	23, 113, 413
pinhole	213, 474, 490
short circuits (shorts)	44 + 46, 151 + 152, 171 + 172 + 173

Table 5.6: The strips that were prepared on Module 664.

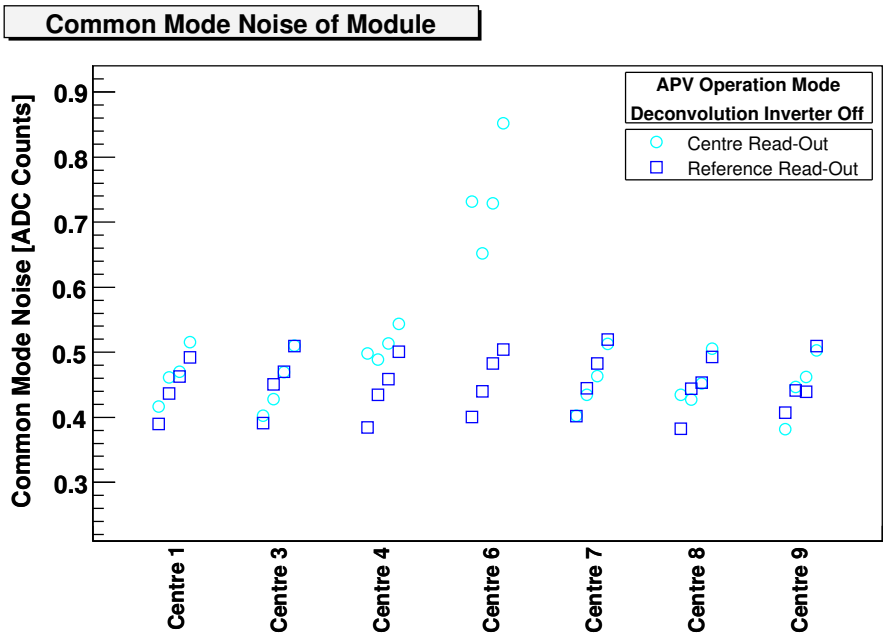


Figure 5.22: Common mode noise of the various test stands and the reference test system in deconvolution inverter off APV operation mode.

mode noise for all centres is about 0.52 ADC counts there it is about 0.75 ADC counts. The reason for the high common mode levels is the length of the read-out cable for the hybrid. Since the box in centre six was designed for performance of measurements at ambient and lowered temperature with the ARC FE adapter staying outside the cold volume an extension cable is used for feeding the signals through the thermal insulation of the box. Hence the high voltage ground and the ground of the hybrid are not connected via a low resistive, short path which is essential to keep the common mode noise at low level.

The impact of the common mode noise on the common mode subtracted noise of a disconnected channel is illustrated in figure 5.23. The input capacity of a channel suffering from a missing bond is lower compared to normal channels which should coincide with a low noise level. While the disconnected channels meet the expectation if the common mode noise is smaller than about 0.5 ADC counts in deconvolution inverter off mode an increase of noise is observed at higher common mode levels. The increase of the common mode subtracted noise with increasing common mode noise is more pronounced for channels which are completely disconnected from the sensors. These channels do not follow the common movement of normal channels because of

the potential on the bias ring of the sensors. The internal common mode suppression of the APV which is explained in subsubsection 2.3.1 causes them to suffer high noise levels. As visible in the plot the noise level is higher compared to normal channels when the common mode noise is 0.85 ADC counts. At this level channels which are connected to the strip of a single sensor still show lower noise compared to normal channels but the difference is small. Since the reproducibility of data in the various centres is highly desirable a modification of the badly performing test station was proposed. As we will see in the further progress of this section the modification is not mandatory.

Since the common mode noise is not low for all centres one cannot expect to be able

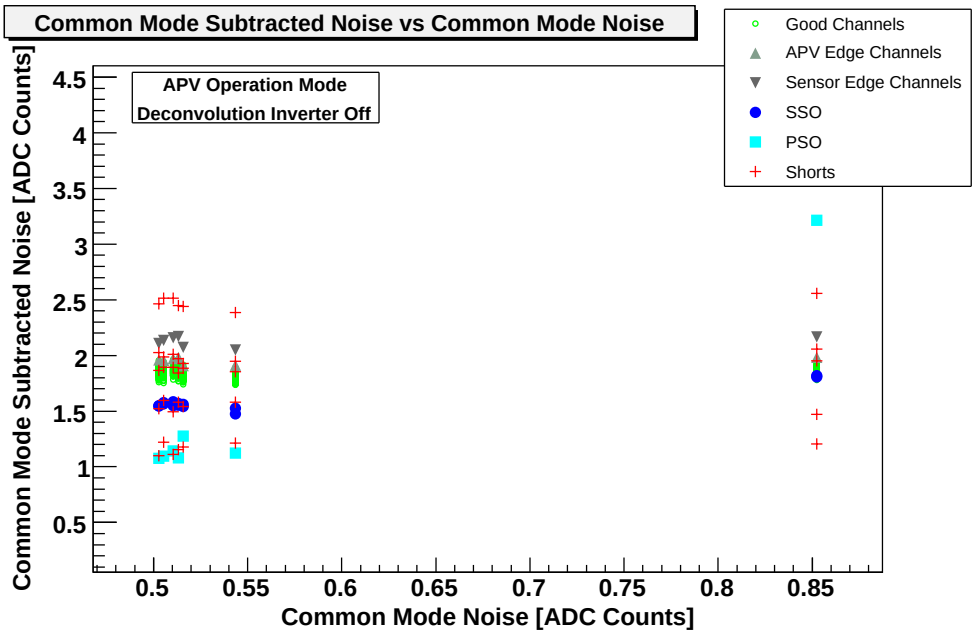


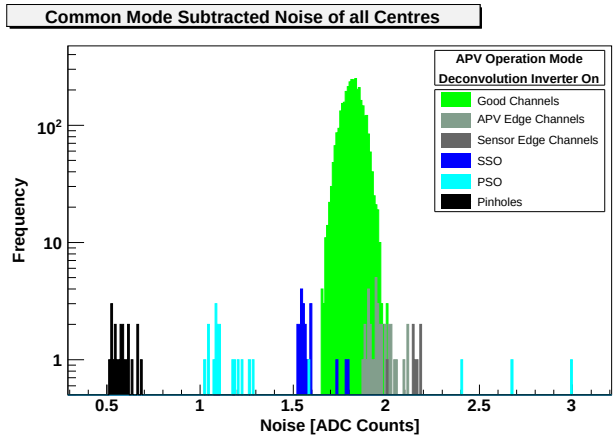
Figure 5.23: Common mode noise of the various test stands and the reference test system in the deconvolution inverter off APV operation mode.

to distinguish the various failure types in the noise data. The histogram which was derived from the datasets of all centres is shown in figure 5.24(a). As expected there are some entries from disconnected channels which are shifted to high noise levels. These entries are caused by the test stand of centre six as illustrated in figure 5.24(b) where the data of this centre is not considered. The best distinction of faults is expected from measurements which were performed with the reference read-out. The bottom histogram 5.24(c) displays the data. Even in this histogram a distinction between pitch adapter - sensor opens and sensor - sensor opens is not possible. It has to be considered that the seven entries of the pitch adapter - sensor open with the highest noise levels are caused by a missing bond on channel 512 which is located at the edge of the sensor. The outermost channels and to some extent also the APV edge channels show higher noise levels. Thus pitch adapter - sensor opens which are located on these positions are more difficult to distinguish from sensor - sensor opens. The position of the removed bonds on module 664 were chosen on purpose for evaluation if even these faults can

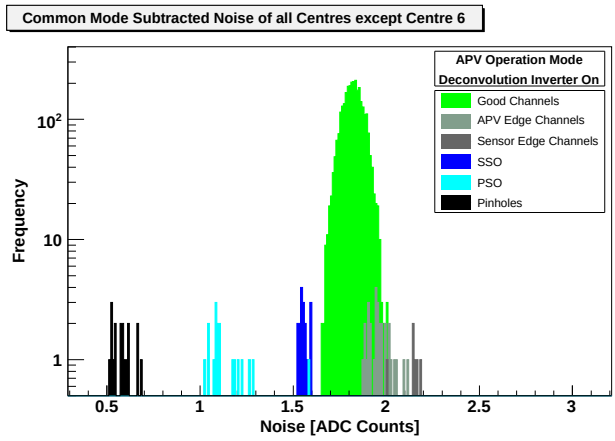
be correctly assigned by their noise behaviour. This is not the case and different criteria are needed for save distinction of the types of disconnected channels. The short circuited channels are not shown in the histograms as other tests are suited better for identification.

In the standard ARCS pulse shape test the maximum pulse height of a normal channel is about 80 ADC counts. As short circuited channels share their charge the pulse height is expected to be about $\frac{1}{2} \cdot 80$ ADC counts for the two pairs of short circuited channels and $\frac{1}{3} \cdot 80$ ADC counts for the group of three channels which are in contact. Disconnected channels show higher maximum pulse heights. The maximum is higher the lower the input capacitance is. Therefore the pulse height of pitch adapter - sensor opens is greater compared to sensor - sensor opens. As the pulse height of pinholes is about zero no pulse is fitted and the pulse height of the corresponding channel is set zero.
Since the pulse height varies significantly from APV to APV and also slightly between the eight calibration groups of an APV the median pulse height is determined for each APV and calibration group. The Quotient between the maximum pulse height of each channel and the median pulse height of the corresponding calibration group is shown in figure 5.25.
As expected the quotient is larger than one for the disconnected channels and much smaller than one for the short circuited channels. The pulse height for the pinholes is zero since the maximum pulse height is determined by the maximum of a fit which is not applied when the maximum pulse height is too low (see 3.6.4). The APV edge channels and the sensor edge channels are good channels since they are fully functional. In the histogram they are highlighted because of their special behaviour compared to the other good channels. The quotient is a good measure for the distinction of the various faults since apart from the sensor - sensor opens all faults clearly separate from the good channels and from each other. Even for the sensor - sensor opens the separation from the large distribution of good channels is good because the sigma of the distribution of good channels is 0.012 and thus small compared to the difference between the mean of the good channels 0.99 and the position of the first sensor - sensor open 1.21, only the APV edge channels complicate the distinction.

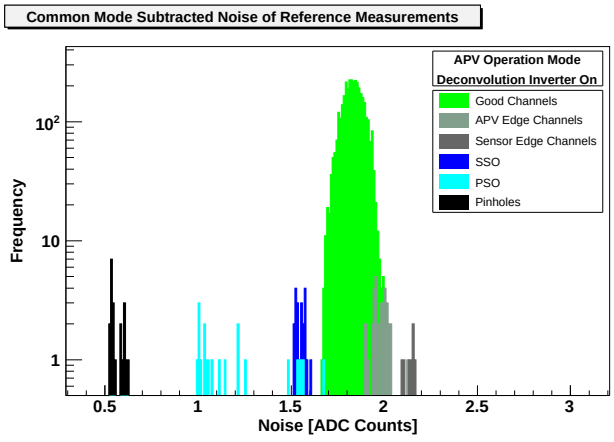
The best distinction of disconnected channels is achieved for the peak time as viewed in figure 5.26. Like for the pulse height a correction is applied before the data is added to the histogram. Here the difference between the peak time of each channel and the median peak time of the corresponding calibration group is calculated. The corrected peak time of the sensor - sensor opens and the pitch adapter - sensor opens clearly differ from the good channels. The mean of a gaussian fit on the distribution of the good channels is 0.012 ns and the sigma is 0.27 ns. Since the mean of the sensor - sensor opens is -7,73 ns and the RMS is 0.44 ns an overlap of the two distributions is very unlikely. Since the mean and the RMS of the pitch adapter - sensor opens are -15,68 and 0.65 ns the distinction of both error types is also very good. For clearness the short circuited channels are not added to the histogram their position is not predictable as the maximum of the pulse shape can be shifted in either direction.



(a)



(b)



(c)

Figure 5.24: Comparison of the noise behaviour of various faults. The histogram (a) contains the data of all centres. In (b) only the centres with low common mode subtracted noise values are considered. The best distinction is expected in histogram (c) where the measurements with the reference read-out are summarized.

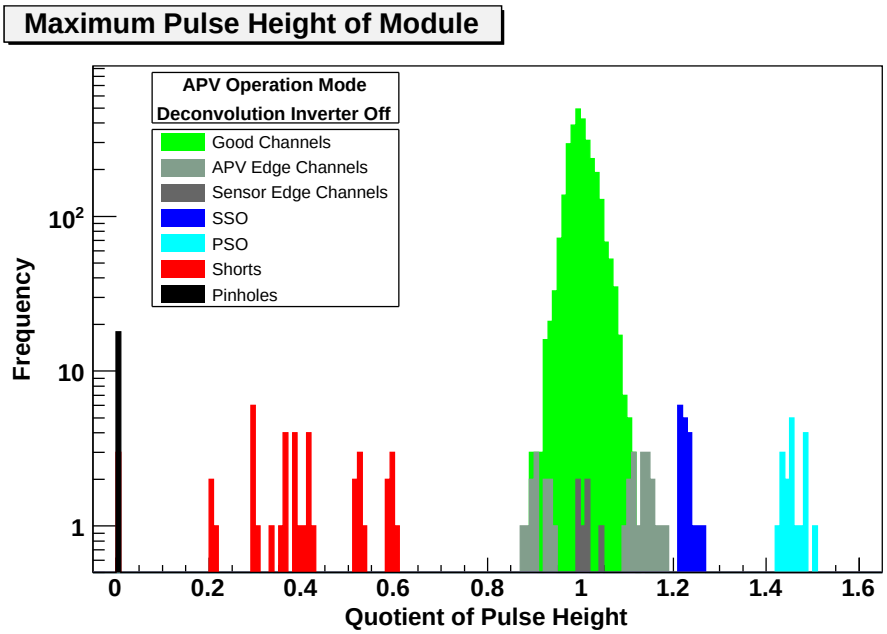


Figure 5.25: The maximum pulse height in deconvolution inverter off mode. The input capacitance of disconnected channels is lower compared to good channels. Thus the maximum pulse height is increased for these channels. The short circuited channels share part of the injected charge. Thus the pulse height of these channels is lower while the pulse height for pinholes is zero as the absolute pulse height is such small that no fit is applied to the data.

However the unique pulse height behaviour of short circuited channels is adequate for their distinction.

The very special behaviour of pinholes in the pinhole test provides an unambiguous signal in the data. While the pulse height difference is less than ten for all channels only pinholes show the characteristic increase and decrease of the pulse height when the leakage current is varied. The histogram in figure 5.27 illustrates the unique separation power of the pinhole test.

The test stands were compared to assure that faults are detectable by a set of cuts which are common for all centres. The measurements showed that the sensor - sensor opens and pitch adapter - sensor opens are definitely detectable and distinguishable in the peak time data. The pulse height measurement clearly identifies short circuited channels and pitch adapter - sensor opens furthermore it provides hints for sensor - sensor opens. Pinholes are visible in all tests but they are unambiguously detected by the pinhole test. Since the separation of the faults is large there is no evidence that the desired fault detection strategy cannot be implemented. A further positive outcome of the investigation is that a non perfect noise performance does not necessarily interfere with the detection capability of other tests. Although all faults are in principle visible in the noise data even the measurements with the reference read-out did not provide the desired distinction of faults. For this reason the noise can only give hints but not compete against the more robust tests.

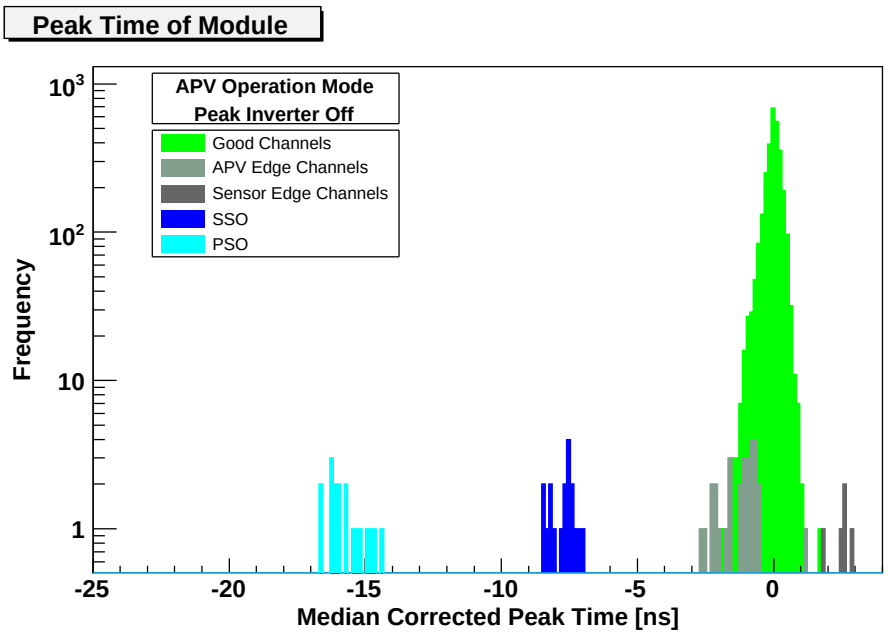


Figure 5.26: The maximum pulse height in deconvolution inverter off mode. The input capacitance of disconnected channels is lower compared to good channels. Thus their pulse height is highest. The short circuited channels share the applied charge. Thus the pulse height of these channels is lower while the pulse height for pinholes is exactly zero as the absolute pulse height is such small that no function is fit to the data.

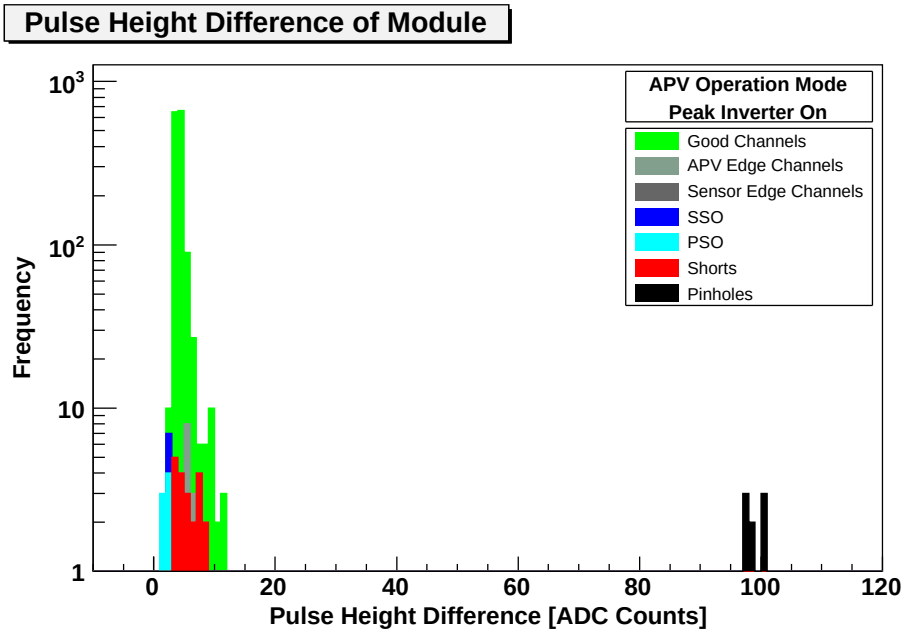


Figure 5.27: The pulse height difference is large for pinholes and comparably small for all other channels. The pinhole test thus provides an unambiguous signal for pinholes.

Although the investigation was performed on a very limited number of test objects it provided a reliable basis for the preparation of the fault finding algorithm which is used for the analysis of ARC data. The development of the fault finding algorithm is described in [37]. The algorithm was tested on 581 modules with known failures. Because of the conservative approach of the algorithm all faults were found while only few good channels were falsely flagged bad. In dependence of the fault type between 85 und 99 % of the faults were correctly assigned.

The Number of Faulty Channels in the Tracker End Caps

Because of the excellent performance of the fault finding algorithm it became an integral part of ARCS and was used in almost all institutes. Since for instance the members of the TEC community used the software it is possible to extract reliable channel flag information on the modules which are located in the tracker end caps. Most interesting are the number of bad channels and the failure types. The information is stored in the „CHLAG“ tag of the MODULBASIC_2_MOD_ table which was originally implemented for single module tests with the ARC system. Further information is provided in the appendix D.3.
The number and the type of the faulty channels which are located in the tracker end caps are illustrated in figure 5.28. From the 3,865,600 channels of the tracker end caps only 5,537 channels were faulty after the module production. This corresponds to a failure rate of only 0.14 % and confirms the excellent quality of the modules and the effective quality assurance. Most of the faulty channels are assigned to missing bond connections. Bonds can easily break because of bad handling other bonds were left out on purpose to disconnect pinholes from APV inputs. A large fraction of the bad channels suffers from high noise. The choice of a cut for high noise is always a bit arbitrary. A channel with slightly higher noise can still be usefull for the tracker. Furthermore the APV and even to some more extent the sensor edge channels are known to suffer from increased noise levels. 446 channels are short circuited and only 29 are connected to pinholes out of which only five are regular pinholes. This extremely low number is an idicator for a very good quality control and shows that the responsibles in the laboratories an the operators made a very good job. Nearly 500 chip failures where found on the modules which is less than 0.015 % and points to a good preselection of the chips, the more so as the gantrys are known to have broken APV inputs due to elctrostatic discharges.
Of course the numbers which are given here are lower limits since additional defects will have been caused during the assembly on the petals and the insertion in the disks. Nevertheless the basis for excellent tracker performance was realized by the imposed quality assurance strategy.

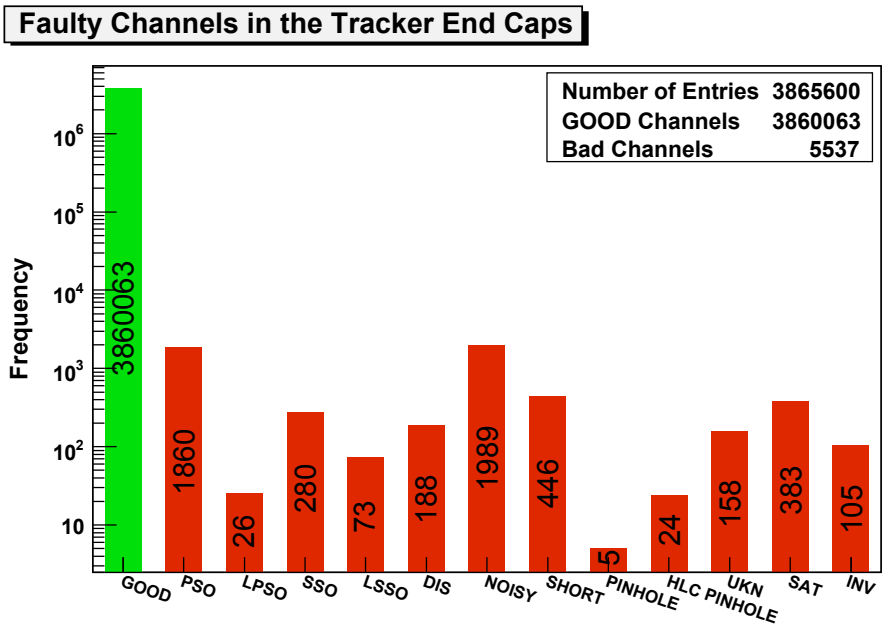


Figure 5.28: The number of faulty channels in the tracker end-caps. The various defects are listed in table D.17.

Chapter 6

Conclusion

The construction of large-scale detectors is an enormous challenge for the high-energy physics community. For the CMS silicon micro-strip tracker 15,148 modules have to be produced in a distributed production. This high number demands for a thoughtful logistics and a sophisticated quality control in close collaboration with the manufactures of the most relevant components. After initial problems with the production of the thick sensors and the hybrids, the CMS tracker collaboration installed an effective quality control system which stands out due to short feedback loops to the manufacturers, thorough tests after each production step, the verification of the components under CMS like conditions and excellent documentation of measurements and transfers via a central database. This thesis describes the single qualification steps and addresses especially the electrical and functional quality control of hybrids and modules. A very important tool for the quality control of hybrids and modules are functional tests which are performed with the ARC system. The read-out instruments the FHIT system, the hybrid test station, the single module test stands and the module thermal cycler in Aachen. For this reason the read-out is involved in the quality control of bare hybrids, the verification of the electrical connections between the pitch adapter and the APVs and the thorough evaluation of completed modules. Side-developments allow the test of components under CMS like environmental conditions which were essential for the early first control of the hybrid and module design. The ARC system became famous because of its robustness, easy handling and the user-friendly software combined with excellent support from the developers. For this reason the read-out system was produced more than 100 times and distributed among the institutes and institutions participating in the construction of modules.
The implemented tests provide robust fault detection and in combination with a fault finding algorithm also correct identification at the 90 % level. The rigorous quality control, excellent fault indentification and the central documentation of results in a database permit the extraction of a reliable estimation for the module quality. From the 3,865,600 read-out channels of the tracker end caps only 5,537 were broken prior to the assembly on the subsytems which corresponds to a rate of only 0.14 %. Even though the final rate of faulty strips in the CMS experiment will be higher the low rate approves the excellent quality assurance during module production which is also a merit of the ARC system.

Now that the construction of modules has come to an end and the tracker is close to being inserted into the CMS detector the ARC measurements are still of interest because of the high reliability of the channel flags which could not be reproduced by tests on subsystems of the tracker. For this reason the measurements with the ARC system are most probably even present when physicists reconstruct the first traces of particles at the LHC start up in 2008.

Appendix A

Additional Plots and Figures

A.1 Cross Sections and Branching Ratios for Higgs Decay

The cross sections for a number of processes versus the centre-of-mass energy is shown in figure A.1. The expected cross sections for very heavy particles are much higher at the LHC compared to the Tevatron. For this reason a detailed study of the properties of the top quark will be performed at the LHC. Furthermore about ten Higgs bosons are expected to be generated per hour. If this particle exists it should be discoverable by the properties of its decay products.

The branching ratio for the decay of the Higgs boson versus the Higgs mass m_{Higgs} is shown in figure A.2. Depending on the Higgs mass two decay channels are favoured for the Higgs search: $H \rightarrow \gamma\,\gamma$ and $H \rightarrow Z\,Z^* \rightarrow l^+\,l^-\,l^+\,l^-$. While the former decay channel is preferred for light Higgs masses $m_{Higgs} < 130\ \mathrm{GeV/c^2}$ the second channel is expected to provide evidence in the region $130\ \mathrm{GeV/c^2} \leq m_{Higgs} \leq 180\ \mathrm{GeV/c^2}$. The Feynman diagrams and the expected signatures in the data are shown in figure A.3 and A.4.

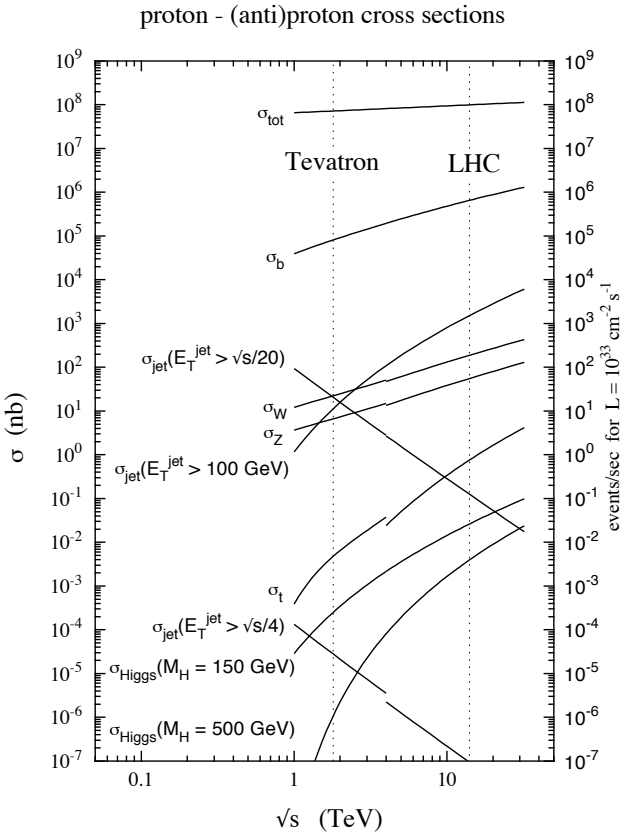


Figure A.1: Comparison of the cross sections at the Tevatron and the LHC [57].

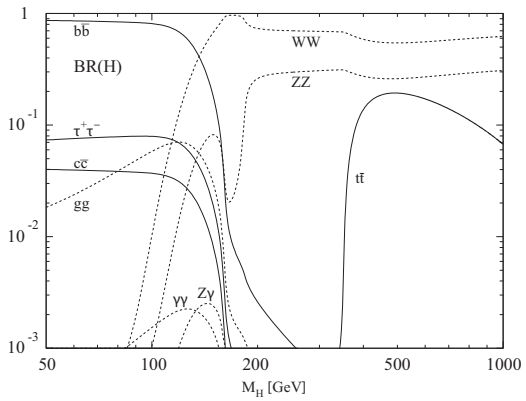


Figure A.2: The branching ratios for the Higgs decay [58].

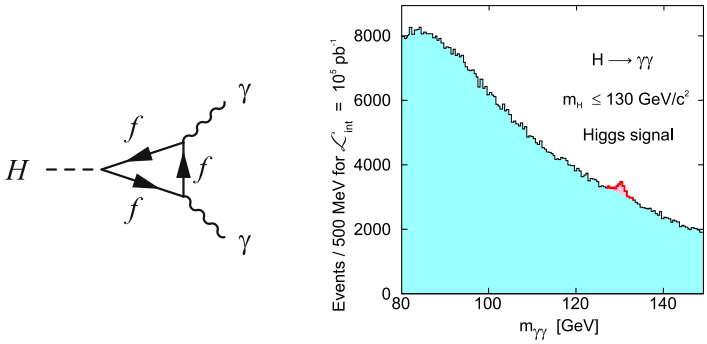


Figure A.3: The most promising decay channel for the detection of a light Higgs boson. (a) The Feynman diagram and (b) the signature in the data [59]).

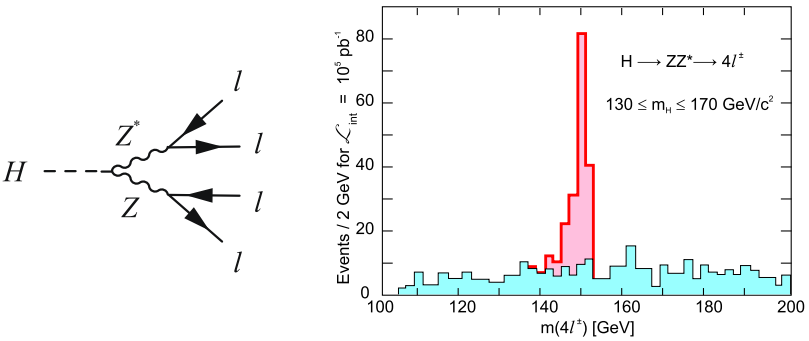


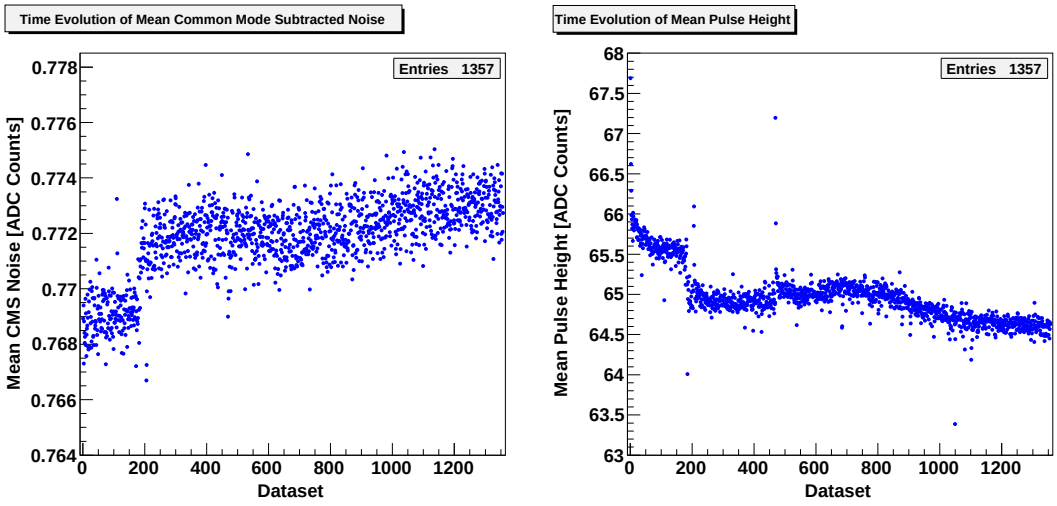
Figure A.4: The favoured channel for the discovery of a heavy Higgs boson. (a) The Feynman diagram and (b) the evidence in the data [59].

A.2 Reproducibility of Measurements

This chapter deals with the reproducibility of noise and pulse height measurements. In the course of the search for the MUX error :-34:[1] hybrids were loop tested for determination of the error rate. The plots which are shown here are derived from 1357 FHIT tests which were performed on a single six APV hybrid. First the stability of the measurements is evaluated and second the reproducibility of the noise and the pulse height of single channels.
The evolution of the mean noise and the mean pulse height is shown in figure A.5. The data acquisition took twenty eight hours during which the temperature of the hybrid was constant at 40ºC. At dataset 200 the noise increased and the pulse height decreased as the lights in the lab were switched off. For the ongoing investigation these dataset are not taken in account.

The histograms of the mean common mode subtracted noise and the mean pulse height are shown in figure A.6. As the ratio of the RMS and the mean noise is about 0.12 % and the same measure for the mean pulse height is 0.33 % the measurements

[1] A synonym the FHIT software uses for a failure which is detected in the MUX test part of the fast test.



(a) **(b)**

Figure A.5: The mean noise versus the dataset is shown in (a) and the corresponding plot of the pulse height is depicted in (b). The jump at dataset 200 was caused when the lights in the lab were switched off.

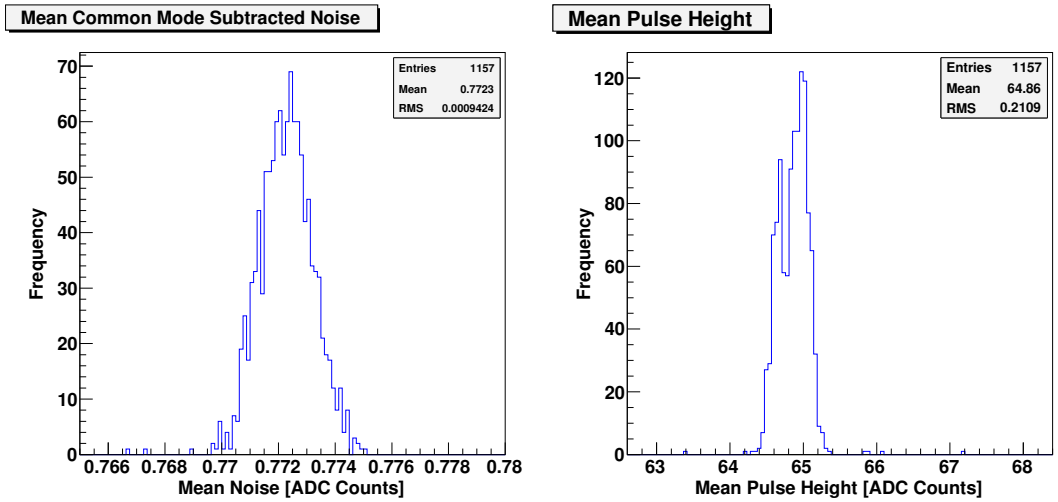
ran very stable.

As the overall measurement ran stable the reproducibility of the noise and pulse height data for single channels can be derived from the corresponding histograms for single channels. Typical histograms for the noise and the pulse height of a single channel are shown in figure A.7.

The histograms in figure A.8 summarize the situation for all channels. The spread of the RMS of the noise is rather large. There is almost a factor of two between the channel with the lowest and the one with the highest RMS. For the pulse height the situation is different. The distribution looks more homogeneous. Apart from some channels with lower values most of the channels are located around 0.32 ADC counts.

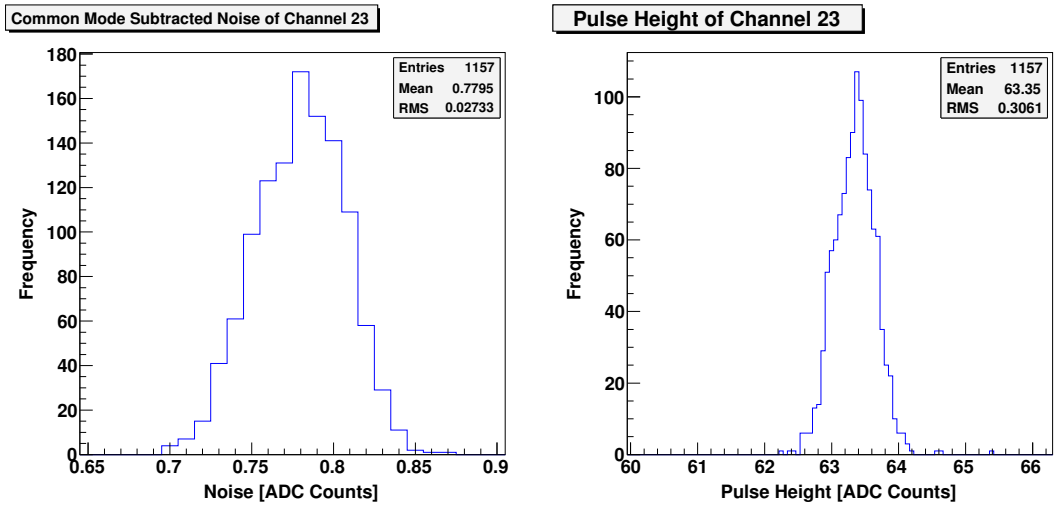
A.3 Comparison of TEC Test Stands

The tests which were performed in the various test centres are shown in table A.9 and A.10.



(a) **(b)**

Figure A.6: Histograms of the mean common mode subtracted noise (a) and the mean pulse height (b). The RMS is very small in comparison to the mean. Thus the measurement was performed under stable conditions.



(a) **(b)**

Figure A.7: The histograms show the typical distribution of the noise (a) and the pulse height (b) for single channels.

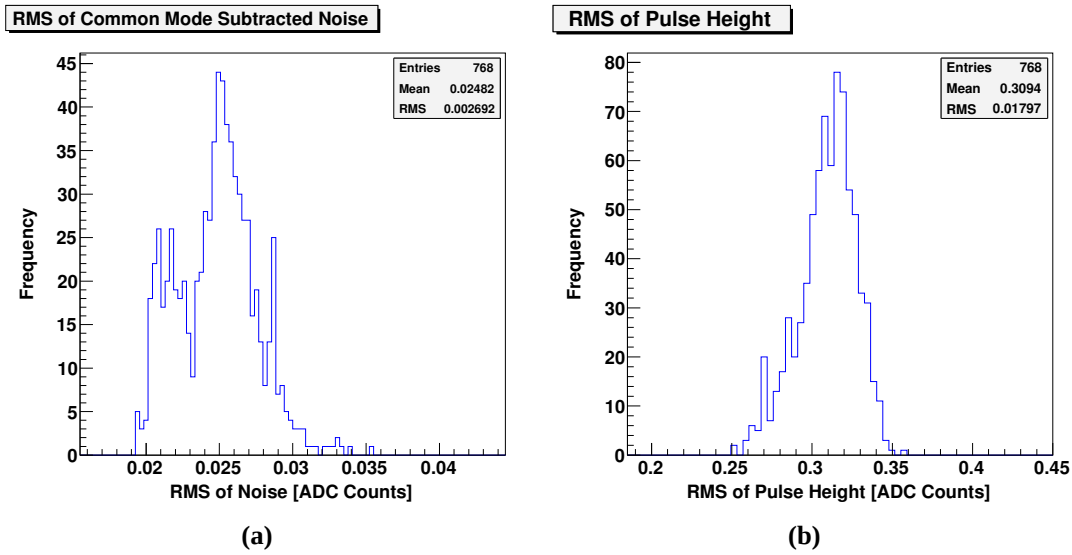


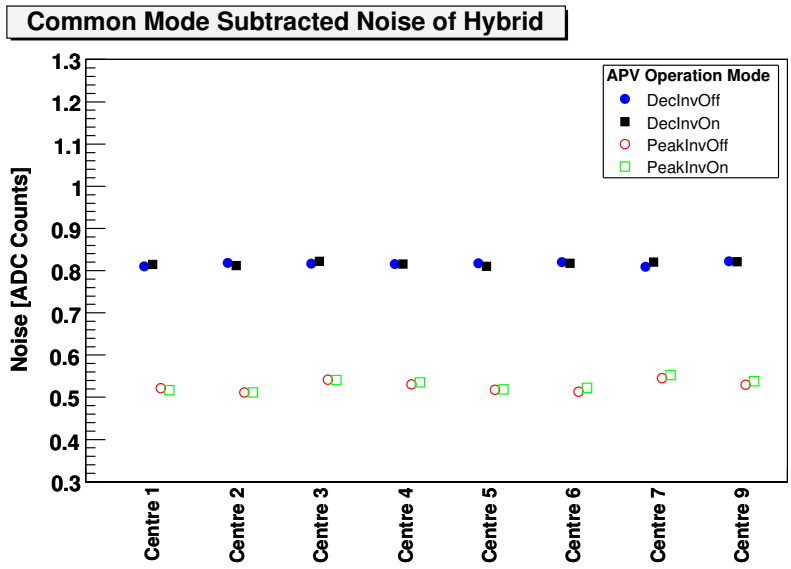
Figure A.8: Histograms of the RMS of the common mode subtracted noise (a) and the mean pulse height (b).

		Pedestal & Noise Test				Calibration Pulse Test				Gain Test				Pipeline Test					
		Dec Inv Off	Dec Inv On	Peak Inv Off	Peak Inv On	Dec Inv Off	Dec Inv On	Peak Inv Off	Peak Inv On	Dec Inv Off	Dec Inv On	Peak Inv Off	Peak Inv On	Dec Inv Off	Dec Inv On	Peak Inv Off	Peak Inv On	Pinhole	LED
Center 1	Hybrid	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Hybrid+PA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Mod 642	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Mod 664	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Center 2	Hybrid	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Hybrid+PA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Mod 642																		
	Mod 664																		
Center 3	Hybrid	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Hybrid+PA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Mod 642	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Mod 664	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Center 4	Hybrid	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Hybrid+PA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Mod 642	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Mod 664	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Center 5	Hybrid	✓	✓	✓	✓									✓	✓	✓	✓		
	Hybrid+PA	✓	✓	✓	✓									✓	✓	✓	✓		
	Mod 642																		
	Mod 664																		

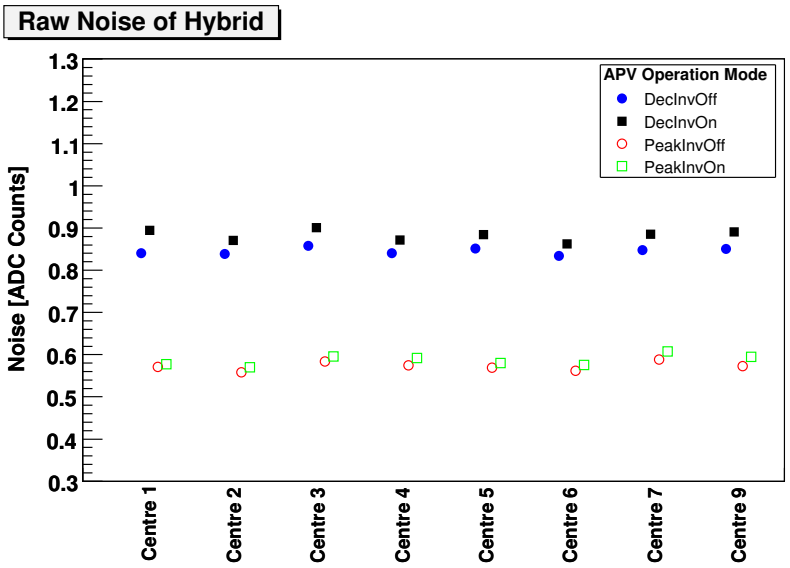
Figure A.9: Overview on the tests which were done in the various test centres.

		Pedestal & Noise Test				Calibration Pulse Test				Gain Test				Pipelin Test					
		Dec Inv Off	Dec Inv On	Peak Inv Off	Peak Inv On	Dec Inv Off	Dec Inv On	Peak Inv Off	Peak Inv On	Dec Inv Off	Dec Inv On	Peak Inv Off	Peak Inv On	Dec Inv Off	Dec Inv On	Peak Inv Off	Peak Inv On	Pinhole	LED
Center 6	Hybrid	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Hybrid+PA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Mod 642	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Mod 664	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Center 7	Hybrid	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Hybrid+PA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Mod 642	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Mod 664	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Center 8	Hybrid																		
	Hybrid+PA																		
	Mod 642																		
	Mod 664	✓	✓	✓	✓														
Center 9	Hybrid	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Hybrid+PA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Mod 642	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Mod 664	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Figure A.10: Overview on the tests which were done in the various test centres.



(a)



(b)

Figure A.11: Mean raw (a) and common mode subtracted noise (b) of hybrid measured in various centres. The error bars are smaller than the marker in the plot.

Appendix B

Noise Calculation Details

. The noise and common mode calculation in ARCS starts when 20 % of the chosen number of data samples are taken. Usually the number of events is 10000. Thus 2000 samples are used as starting point for the pedestals. In [37] it is shown that this method and the iterative calculation which is needed to limit the allocation of memory leads to comparable noise results.
The calculation routines for the noise are not allowed to be influenced by single abnormal events and channels with large noise. Noisy channels for example may rule the common mode by their significant contribution to the total signal. Three input parameters which only effect the common mode correction are used to make the calculation routines more robust. They are called $tskip$, $pskip$ and $tbad$. Their meaning in described further on.
The parameter $tskip$ is used to skip channels for the calculation of the common signal in an event n when an exceptional large signal was present. Two criteria identify a large signal. A channel is skipped if the corresponding raw signal $SR_{ch,n}$ is $tskip$ times larger than the noise N_{ch}^{n} which is calculated up to the recent event n.

$$|SR_{ch,n}| > tskip \ \cdot \ N_{ch}^{n} \tag{B.1}$$

A channel is also excluded from the calculation if the raw signal is much higher than the average raw signal in a certain event :

$$|SR_{ch,n}| > \frac{1}{128} \sum_{ch=1}^{128} |SR_{ch,n}| \, tskip \tag{B.2}$$

In ARCS $tskip$ is set to 4. For this reason only large signals which could govern the common mode calculation are excluded. Channels which are identified as bad by the software are skipped permanently for the calculation of the common mode. The parameters which are used to deduce if a channel is bad or not are $pskip$ and $tbad$. If a channel was skipped more than $pskip \cdot 100$ times the total number of events because of equations B.1 and B.2 a channel is excluded. The rms of the noise N_{ch}^{n} in combination with the parameter $tbad$ is a further criterion for bad channel determination.

$$N_{ch}^{n} > \sqrt{\frac{\sum_{ch=1}^{128}(N_{ch}^{n} - \bar{N}^{n})^{2}}{128}} \cdot tbad + \bar{N}^{n} \tag{B.3}$$

The defaults settings for the parameters $pskip$ and $tbad$ are 0.2 and 5. They are defined in the testsettings file which is selected when ARCS is started.

Appendix C

Additional Object Information

The relevant objects which will be part of the CMS tracker are assigned to numbers. Each number and three attributes which provide information on the object are registered in the central tracker database [36]. The numbers are unique and usually encoded in a one of two dimensional bar code which is machine-readable. The bar codes are printed on labels which are attached to the objects or their transport boxes. All production steps and transfers, an object undergoes, are recorded in the database for production overview and management of the logistics.
The number which is assigned to each object consists of 14 digits. The coding of information in the single digits is shown in figure C.1.

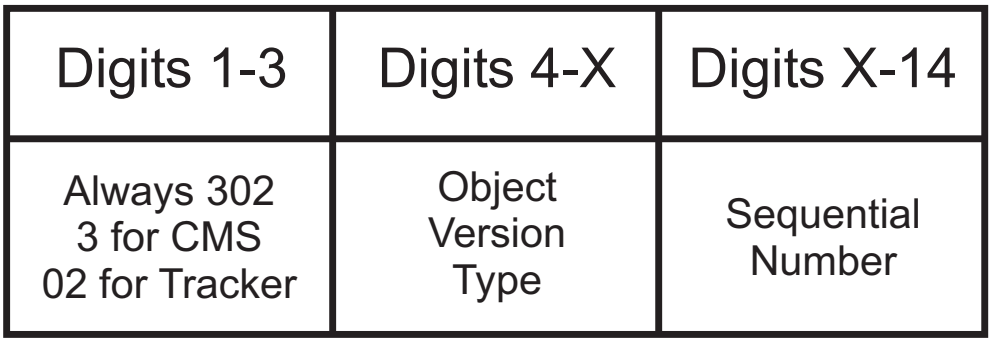


Figure C.1: The number for the identification of the CMS tracker components starts with 302 followed by an object identifier which may contain version and or type information. The last digits are reserved for the identification of each single object.

The three attributes which are assigned to each object at registration are:

object	an acronym for the object, e.g. 'HYB' for hybrids
version	a single number, the version is used for distinction of objects from different production series, e.g. prototypes are usually identified by version 99
type	a series of numbers which are separated by dots indicate the type of an object, e.g. the type of a module can be TEC ring 4

When an object is assembled into a composite object, e.g. a sensor into a module, the id of the composite object and the position within the composite object is add to the table holding the object information. For this reason the position of each object in the tracker can be traced back.
Since the type information is cryptic a table is implemented which holds a self-explanatory description of each combination of object, version and type. In the further progress of this chapter the encryption of information in the types is given as well as the description of the single object types.

C.1 Hybrid Versions and Types

The hybrids of various periods of production are identified by a version. A version change is applied each time the substrate material, the layout of the schematics or the layer structure was modified or changed. In total 21 different versions of hybrids exist. Table C.1 lists those versions which where produced in appreciable numbers. The hybrids of these versions are manufactured by Cicorel and Hybrid SA. The version of a hybrid is encrypted in its identification number (see C.1.1).
Most of the hybrids which are assembled on final modules for the CMS tracker are of production version 6 and 7 as table C.2 indicates. These hybrids were produced after the via problem was solved by the introduction of an additional layer (LF101 layer).
The data in table was extracted from the database. The queries are given in appendix E.1.

The hybrid type consists of four numbers a, b, c and d. The first number indicates the association to a certain detector part. The second number indicates the number of APVs and c provides information on the orientation of the hybrid connector. The fourth number depends on geometry of the ceramic support piece. There are pieces for the assembly of normal and stereo modules. The fourth number is one regardless of the ceramic type if there is only one type of ceramic for a certain combination of a, b and c. An overview on the encryption of information is given in table C.3.

[1] TIB and TID hybrids are identical.

version	production version	description
various	0	prototype version
15	1	preproduction version : cable weakness problem
16	2	production version : stiffener added
17	3	production version : modified outer layers + stiffener
18	4	production version : modified outer and inner layers + stiffener
19	5	production version : modified outer and inner layers + stiffener + modified laser drilling parameters
20	6	final version : slightly modified inner layers + laser drilling parameters + LF101 layer
21	7	final version : slightly modified inner layers + laser drilling parameters + LF101 layer + modified solder mask

Table C.1: Relevant hybrid versions. The description was extracted from the object_description table of the central database.

version	total amount	mounted on modules	mounted on TOB or TEC subassembly
0	351	127	3
1	799	277	5
2	3762	2119	513
3	1673	930	99
4	2008	471	56
5	319	221	204
6	9137	7700	4634
7	6883	5890	5127

Table C.2: The number of hybrids for all production versions, their assembly status and usage for a TOB or TEC subassembly.

a	1	2	3
Sub Detector	TIB [1]	TEC	TOB

b	1	2
Number of APV	4	6

c	1	2
Connector Orientation	up	down

d	1	2
Normal or Stereo	normal	stereo

Table C.3: The encryption of hybrid properties into distinct hybrid types.

digit	value	description
1	1-7	layer or ring of corresponding sub-detector
2	0	ring or layer contains no stereo modules
	1	pitch adapter for r-φ module
	2	pitch adapter for stereo module
3	0	not stereo type or only one type exists
	1	sensor is tilted counter-clockwise (module face up)
	2	sensor is tilted clockwise (module face up)

Table C.4: The encryption of pitch adapter properties into distinct pitch adapter types.

For practical reasons the hybrids which are assembled with a pitch adapter are still assigned to the identification number of the hybrid. For control of the production flow the type of the composite object is changed after the assembly. Four numbers indicate the type of a hybrid with assembled pitch adapter. The first three numbers are determined by a,b and c of the corresponding hybrid [1]. The fourth number consists of three digits and indicates the pitch adapter type. The encryption of the pitch adapter type is summarized in table C.4.

The number of different hybrid types is twelve. The single types are translated into a part id which is encrypted in the hybrid identification number (see C.1.1). In total 26 combinations of hybrids and pitch adapters are produced. The single types and the hybrid part ids are listed in table C.5.

[1] There is a single exception to this rule. As TIB and TID hybrids are identical, the first number of the hybrid type is changed from one to four if a TID pitch adapter is attached.

Before Assembly			After Assembly	
Type	Description	Part ID	Type	Description
1.1.2.1	IB_P.4D	1668	1.1.2.300	IB_300.4D
1.2.1.2	IB_S.6U	1677	1.2.1.121	IB_121.6U
			1.2.1.122	IB_122.6U
1.2.2.1	IB_P.6D	1670	1.2.2.110	IB_110.6D
2.1.1.1	EC.4U	1663	2.1.1.300	EC_300.4U
			2.1.1.400	EC_400.4U
			2.1.1.600	EC_600.4U
			2.1.1.700	EC_700.4U
2.2.1.1	EC.6U	1665	2.2.1.120	EC_120.6U
			2.2.1.220	EC_220.6U
			2.2.1.520	EC_520.6U
2.2.2.1	EC.6D	1666	2.2.2.110	EC_110.6D
			2.2.2.210	EC_210.6D
			2.2.2.510	EC_510.6D
3.1.1.1	OB_P.4U	1671	3.1.1.110	OB_110.4U
3.1.1.2	OB_S.4U	1675	3.1.1.120	OB_120.4U
3.1.2.1	OB_P.4D	1672	3.1.2.110	OB_110.4D
3.1.2.2	OB_S.4D	1676	3.1.2.120	OB_120.4D
3.2.1.1	OB_P.6U	1673	3.2.1.500	OB_500.6U
1.1.2.1	IB_P.4D	1668	4.1.2.300	ID_300.4D
1.2.1.2	IB_S.6U	1677	4.2.1.121	ID_121.6U
			4.2.1.122	ID_122.6U
			4.2.1.221	ID_221.6U
			4.2.1.222	ID_222.6U
1.2.2.2	IB_S.6D	1678	4.2.2.110	ID_110.6D
			4.2.2.210	ID_210.6D

Table C.5: The various types of hybrids with pitch adapter.

C.1.1 Hybrid Identification Numbers

The identification number of a hybrid provides information on the hybrid type and version. The type is indicated by the part id which is contained in digits four to seven of the identification number. The link between part id and type is shown in table C.5. The hybrid version is contained in digits eight and nine of the identification number. The most important versions are shown in column 'version' of table C.1.
The remaining five digits contain a sequential number which identifies the single objects.

C.2 Sensor Versions and Types

The versions of the sensors are either 1 or 99. The later version is assigned to prototype sensors.
The sensor type consists of two numbers. The first number is used for distinction of the various geometries while the second number indicates the thickness of the sensor. The CMS tracker is equipped with 17 types of sensors. The TIB, the TID and the TEC sensors for ring one to four are 'thin' sensors of 320 µm thickness. TOB and TEC sensors for rings five to seven are 'thick' sensors of 500 µm thickness.
The various sensor types, the quantities which are needed for the CMS tracker and some additional information are listed in table C.6.

Type	Description	Width1 [mm]	Width2 [mm]	Length [mm]	Pitch [µm]	Strips	Multiplicity
1.1	IB1	63.3	-	119.0	80	768	1536
2.1	IB2	63.3	-	119.0	120	512	1188
3.2	OB1	96.4	-	94.4	122	768	3360
4.2	OB2	96.4	-	94.4	183	512	7056
5.1	W1 TEC	64.6	87.9	87.2	81-112	768	288
15.1	W1 TID	63.6	93.8	112.9	80.5-119	768	288
6.1	W2	112.2	112.2	90.2	113-143	768	864
7.1	W3	64.9	83.0	112.7	123-158	512	880
8.1	W4	59.7	73.2	117.2	113-139	512	594
18.1	W4S[1]	59.7	73.2	117.2	113-139	512	414
9.2	W5A	98.9	112.3	84.0	126-142	768	1440
10.2	W5B	112.5	122.8	66.0	143-156	768	1440
11.2	W6A	86.1	97.4	99.0	163-185	512	1008
12.2	W6B	97.5	107.5	87.8	185-205	512	862
20.2	W6BS[1]	97.5	107.5	87.8	185-205	512	144
13.2	W7A	74.0	82.9	109.8	140-156	512	1440
14.2	W7B	82.9	90.8	90.8	156-172	512	1440

Table C.6: The various sensor types and the needed quantities for the construction of the CMS tracker (source [53]).

C.2.1 Sensor Identification Numbers

The identification number of a sensor provides information on the manufacturer, the sensor type and the batch id. The fourth digit of the identification number is one if the sensor was produced by STM. A two indicates HPK to be the manufacturer. Digits

[1] Special sensors with partly removed metal backplane. The backside is polished for the transmission of a laser beam which is used for the alignment.

five and six contain the first number of the sensor type (see table C.6). The remaining eight digits are used for the identification of the batch and the single sensors within a batch. The number of sensors per batch is 100. Thus digits seven to twelve indicate the batch id and the two least significant digits the sensors within a batch.
Initially HPK was foreseen for production of the thin sensors while STM should have produced the thick sensors. As STM did not produce sensors with constant quality, a large fraction of the production was shifted to HPK. For this reason a large fraction of the thick sensors was produced by HPK. The fraction of thick sensors from STM and HPK in the CMS tracker is shown in table C.7.

Description	Installed in Tracker	Produced by STM		Produced by HPK	
		Multiplicity	Percentage	Multiplicity	Percentage
OB1	3360	-	-	3360	100
OB2	7056	-	-	7056	100
W5A	1440	126	8.8	1314	91.2
W5B	1440	126	8.8	1314	91.2
W6A	1006	-	-	1006	100
W6B	862	-	-	862	100
W6BS	144	-	-	144	100
W7A	1440	161	11.2	1279	88.8
W7B	1440	161	11.2	1279	88.8

Table C.7: The amount of thick sensors in the tracker and manufacturer information. Sensors from STM were only installed on ten percent of the positions for ring five and seven modules. The data was extracted from the database. The corresponding queries are described in section E.1

C.3 Module Types and Versions

There are four versions of modules. Prototype modules are constructed from prototype hybrids or sensors. These version of these modules is 99. Modules of version 95 were used for demonstration purposes, e.g. for proof of data acquisition of larger structures. The versions which are usable for the tracker indicate the manufacturer of the sensor. A version one module was assembled from HPK sensors. The version is two if sensors from STM were used. There are no modules with sensors from both manufacturers.
The CMS modules are constructed from 26 different types of hybrids with pitch adapters (see table C.5)and 17 types of sensors (see table C.6). The number of the various module types which are installed in the CMS tracker and the components they are constructed of are listed in table C.8.

C.3.1 Module Identification Numbers

Modules are identified by a 200 in digits four to six of the identification number. The remaining digits are used for the identification of the single modules.

Hybrid with Pitch Adapter Description	Sensor 1 Description	Sensor 2 Description	Module Type	Module Description	Multiplicity
IB_110.6D	IB1		1.1.1.1	IB_L12P.6D	768
IB_121.6U		-	1.1.2.2	IB_L12SL.6U	384
IB_122.6U		-	1.1.3.3	IB_L12SR.6U	384
IB_300.4D	IB2	-	1.2.4.1	IB_L34P.4D	1188
					2724
EC_110.6D	W1 TEC	-	2.5.17.14	EC_R1P.6D	144
EC_120.6U		-	2.5.18.15	EC_R1S.6U	144
EC_210.6D	W2	-	2.6.19.16	EC_R2P.6D	288
EC_220.6U		-	2.6.20.17	EC_R2S.6U	288
EC_300.4U	W3	-	2.7.21.18	EC_R3P.4U	640
EC_400.4U	W4	-	2.8.22.19	EC_R4P.4U	594
	W4S	-	2.18.22.19	EC_R4P.4U-S	414
EC_510.6D	W5A	W5B	2.9.23.20	EC_R5P.6D	720
EC_520.6U			2.9.24.21	EC_R5S.6U	720
EC_600.4U	W6A	W6B	2.11.25.22	EC_R6P.4U	864
		W6BS	2.19.25.22	EC_R6P.4U-S	144
EC_700.4U	W7A	W7B	2.13.26.23	EC_R7P.4U	1440
					6400
OB_110.4D	OB2	OB2	3.4.14.12	OB_L12P.4D	540
OB_120.4D			3.4.16.13	OB_L12S.4D	540
OB_120.4U			3.4.15.13	OB_L12S.4U	540
OB_110.4U			3.4.12.12	OB_L12P.4U	540
			3.4.12.11	OB_L34P.4U	1368
OB_500.6U	OB1	OB1	3.3.13.11	OB_L56P.6U	1680
					5208
ID_110.6D	W1 TID	-	4.15.5.4	ID_R1P.6D	144
ID_121.6U		-	4.15.6.5	ID_R1SF.6U	72
ID_122.6U		-	4.15.7.6	ID_R1SB.6U	72
ID_210.6D	W2	-	4.6.8.7	ID_R2P.6D	144
ID_221.6U		-	4.6.9.8	ID_R2SF.6U	72
ID_222.6U		-	4.6.10.9	ID_R2SB.6U	72
ID_300.4D	W3	-	4.7.11.10	ID_R3P.4D	240
					816

Table C.8: The various module types and the needed quantities for the construction of the CMS tracker.

Appendix D

The Database Tables for ARC Test Results

The measurements of all ARC based test stations are uploaded to the central tracker database [36]. Dedicated tables are implemented for each test. These tables are described in the following sections of this chapter.

D.1 General Aspects

The data files which are taken at the various test stands are analysed and converted to XML format. The typical XML files for ARC based hybrid and module tests contain the most relevant test results, a flag for the bad channels and a data quality flag (status) which is selected by the operator who performed the test. When a regular qualification test was performed the status of the data is „reference“, the various flags are listed in table D.1. A dedicated so-called basic action table is assigned to each measurement, e.g. the FHIT test in industry. These tables contain the most relevant data and the results, e.g. a list of error flags for each channel, of the corresponding measurement. Whenever an XML file is uploaded to the database a record is created in the appropriate table. Another type of table are the so-called composite action tables. As the denomination indicates these are higher-level tables which provide links to the records of one or more basic action tables. The composite action tables are implemented for overview on the qualification control. For this reason they are only updated if the sta-

reference	a standard qualification test was performed
valid	the data is not suited for grading, e.g. a subset of tests was performed only
not valid	the data does not represent the quality, e.g. because of problems with the read-out system

Table D.1: The various data quality flags.

tus of the uploaded data is „reference“.
A basic action table contains only one reference record for each test object even when a certain standard qualification test was repeated and several XML files with status „reference“ were uploaded to the database[1]. Since the actual quality of an object is determined by the most recent standard qualification measurement the record which was created last is given the status „reference“ while the status of a previous „reference“ record, if it exists, is changed to status „valid“.
The names for the tables that contain test results consist of three parts separated by underscores. The first part reflects the purpose of the table like “MODVALIDATION“, the second part is a number for the table version and the last part indicates the object the table was implemented for, e.g. HYB. The initial version of a table is one. By the time some tables were modified because a different content seemed to be more appropriate. For these tables the version is two. The various tables which are implemented for the electrical and functional qualification of hybrids and module are described in the following sections.

D.2 The Database Tables for Hybrid Tests

Three composite action tables are implemented for ARC based hybrid and hybrid with pitch adapter qualification tests. The names of the composite action tables and the corresponding basic action tables are given in table D.2.

composite action table	**basic action table**
HYBPRODUCER_1_HYB_	FHITPRODUCTION_1_HYB_
HYBMEASUREMENTS_1_HYB_	FHITRECEPTION_1_HYB_ TESTWITHPA_1_HYB_
HYBMEASUREMENTS_2_HYB_	FHITRECEPTION_1_HYB_ TESTWITHPA_1_HYB_

Table D.2: The composite and the corresponding basic action tables for the qualification of hybrids.

[1]There are basic action tables which are assigned to more than one composite action table. These basic action tables can contain up to the same number of reference records for each test object as the number of composite action tables they are assigned to.

The measurements the basic action tables are assigned to are given in table D.3.

name of basic action table	**description**
FHIT_PRODUCER_1_HYB_	table for hybrid data which was taken with the FHIT system at HSA
FHIT_RECEPTION_1_HYB_	table for hybrid data which was taken with the FHIT system for a reception test
TESTWITHPA_1_HYB_	table for hybrid with pitch adapter data which was taken with the hybrid test station

Table D.3: The measurements for the qualification of hybrids and the corresponding basic action tables.

The content of the three basic action tables is given in the following subsections.

D.2.1 The FHITPRODUCTION_1_HYB_ and the FHITRECEPTION_1_HYB_ Table

The FHIT tests which are done at Hybrid SA are identical with the tests which are done at CERN. For this reason the content of the FHITPRODUCTION_1_HYB_ and the FHITRECEPTION_1_HYB_ tables are identical. The single entries are listed in table D.4.

identifier	**meaning**
OBJECT_ID	14-digit hybrid identifier
TEST_ID	unique number added by db for the correlation with the parent action
TOOL_ID	unique test station identification number
PARENT_ACTION	name of the parent action table, HYBPRODUCER or HYBMEASUREMENTS
INPUT_ID	database internal number for table identification
TDATE	date and time of test
OPERATOR	name of operator who did the test
FHIT_NUMBER	FHIT identification number
GOAL	goal of test, e.g. production or reception
CENTER	name of test centre
FHIT_TEST_TYPE	performed test type, usually full industrial test or just a subset
FHIT_FIRMWARE_VERSION	firmware version of FHIT
FHIT_BOARD_VERSION	board version of FHIT
TEMP_AMBIENT_DEGC	not used
TEMP_APV_DEGC	not used
FHIT_VREF_IN_MV	FHIT reference voltage in mV
VCC_IN_MV	supply voltage on V_{CC} in mV should be 5000
VP12_IN_MV	supply voltage on VP_{12} in mV should be 12000
VM5_IN_MV	supply voltage on VM_5 in mV should be -5000
ET_SETTINGS_IN_ADC	electrical test ADC settings for measurement at nominal, increased and reduced hybrid supply voltage
ET_V125_IN_MV, ET_V250_IN_MV	supplied voltage on 1.25 and 2.5 V line for nominal, increased and reduced supply voltage

identifier	**meaning**
ET_LIMITS	not used
FT_LIMITS	not used
FHITMEASUREMENT_DATE	date and time of measurement
FEH_GRADE	grade of hybrid
INSERTION	FHIT connector, number of plugging cycles
TEST_DURATION_S	duration of FHIT test in s
CT_ERR, ET_ERR	number of errors in connectivity and electrical test
FT_GRADE	grade of functional test
TEMP_TEST_STATION	temperature of FHIT
PART_NUMBER	hybrid identification number, part of hybrid identification bar code
APV_NUMBER	number of APVs
CT_GND_OPEN	connectivity test: number of discontinued ground lines
CT_V125_OPEN, CT_V250_OPEN	connectivity test: number of discontinued 1.25 and 2.5 voltage supply lines
CT_SUPPLY_SHORT	number of short circuited power supply lines
CT_SIGNAL_ERR	number of signal errors during connectivity test
ET_I2C_SCAN_NB	electrical test: number found I^2C addresses
ET_MUX_ERR	electrical test: number of MUX commuication failures
ET_PLL_ERR	electrical test: number of PLL commuication failures
ET_DCU_ERR	electrical test: number of DCU commuication failures
ET_APV_ERR	electrical test: number of APV commuication failures
ET_RC_ERR	electrical test: number of decoupling network failures
ET_DCU_ID	three bytes read from DCU indentification registers
DCU_ID	24-bit DCU identifier, combination of identification bytes to a single number

identifier	**meaning**
DCU_CAL_LOWINPUT_MV	DCU calibration data at low input
DCU_CAL_LOW_VNOM	DCU calibration low data at nominal voltage
DCU_CAL_LOW_VMAX	DCU calibration low at increased voltage
DCU_CAL_LOW_VMIN	DCU calibration low at nominal voltage
DCU_CAL_HIGHINPUT_MV	DCU calibration data at high input
DCU_CAL_HIGH_VNOM	DCU calibration high at nominal voltage
DCU_CAL_HIGH_VMAX	DCU calibration high at increased voltage
DCU_CAL_HIGH_VMIN	DCU calibration high at reduced voltage
DCU_FHIT_MICROVPADC	not used
DCU_CAL_A_MICROVPADC	not used
DCU_CAL_B_MICROV	not used
DCU_x_FHIT_MV	DCU channel x data in mV
DCU_x_RAW	DCU channel x data in ADC counts
DCU_x_MV	not used
IV125_IDLE_MA, IV250_IDLE_MA	current on 1.25 and 2.5 V line, all APV analogue power off
IV125_APV2x_MA, IV250_APV2x_MA	current on 1.25 and 2.5 V line, only APV2x analogue power on
IV125_ALL_MA, IV250_ALL_MA	current on 1.25 and 2.5 V line, all APV analogue power on
STABILIZATION_TIME_S	current stabilization time
DETECTOR_RETURN	test of detector return input of DCU
FT_FRAMEHEIGHT_APV2x_ADC	functional test, APV2x digital header height in ADC counts
FT_PED_APV2x_ADC	functional test, pedestals of APV2x
FT_RAWNOISE_APV2x_ADC	functional test, raw noise of APV2x
FT_CMSUBNOISE_APV2x_ADC	functional test, common mode subtracted noise of APV2x
FT_CALHEIGHT_APV2x_ADC	functional test, calibration height of APV2x
FT_CALBASE_APV2x_ADC	functional test, baseline of APV2x during calibration run
FT_BADCHANNEL_LIST_APV2x	functional test, bad channel list of APV2x
FHITPRODUCTION_VAL	FHIT final result
STATUS	status of data, e.g. reference, valid, not valid
TCOMMENT	comment

Table D.4: The content of the FHIT_PRODUCER_1_HYB_ and the FHIT_RECEPTION_1_HYB_ table.

D.2.2 The TESTWITHPA_1_HYB_ Table

The data and the results of the hybrid test station are stored in the basic action table TESTWITHPA_1_HYb_. The single entries are listed in table D.5

identifier	**meaning**
OBJECT_ID	14-digit hybrid identifier
TEST_ID	added by db for correlation with parent action
TOOL_ID	unique test station identification number
PARENT_ACTION	name of the parent action table, HYBMEASUREMENTS
INPUT_ID	database internal number for table identification
TDATE	date of test
OPERATOR	name of operator who did the test
PEDESTAL	pedestals of each channel
NOISE	raw noise of each channel
FLAG	channel failure flag: 0 ok, 10 discontinuity, 20 short circuit, 30 noise out of limits
HYBRIDSETTINGS	I^2C settings for APVs
TESTSETTINGS	configuration file for the test, number of events etc.
SCRIPT	name of the scenario, scenario determines the number of thermal cycles
TESTWITHPA_VAL	final result
STATUS	status of data, e.g. reference, valid, not valid
TCOMMENT	comment on measurement, contains information on failed PLL initialization
HYBTEMP	hybrid temperature in °C, measured by test station internal sensor
DCUCH0	DCU raw data, measurement of voltage drop over 10 kΩ resistor on ARC front-end adapter
DCUCH4	DCU raw data, hybrid temperature
DCUCH7	DCU raw data, DCU temperature

Table D.5: The content of the TESTWITHPA_1_HYB_ table.

D.3 The Database Tables for Module Tests

Four composite action tables are implemented for ARC based single module tests. All of these tables are linked the same basic action table. The tables and the test stations they are implemented for are listed in table D.6.

The numbers of different tests which were uploaded to the MODULBASIC_2_MOD_

composite action table	test station	basic action table
MODVALIDATION_2_MOD_	single module test station	MODULBASIC_2_MOD_
MODULLTFIRST_2_MOD_	module thermal cycling test stand	
MODULLTCOLD_2_MOD_		
MODULLTLAST_2_MOD_		

Table D.6: The composite and the corresponding basic action tables for single module tests.

table are shown in table D.7. The numbers are given by the amount of records with different combinations of object identification number and measurement date. This constraint avoids multiple counting of tests which were uploaded more than once, for instance when a data file was reanalysed or an XML file was accidentally resent to the database. The database query for the table is given in appendix E.3.

More than 26,000 single module tests were uploaded to the database which indicates

composite action table	number of tests
MODVALIDATION_2_MOD_	26221
MODULLTFIRST_2_MOD_	9809
MODULLTCOLD_2_MOD_	9811
MODULLTLAST_2_MOD_	9811

Table D.7: The number of tests in the MODULBASIC_2_MOD_ table. The table represents the situation on 30th of September 2007.

that many modules were tested more than once. A thermal cycle for single modules was done for TEC and TOB modules only as long as the test stations for rods and petals where not operable. For TIB and TID modules the test was performed on all modules as part of the qualification. Hence the number of MODULLT tests is smaller than the number of modules which instrument the tracker. The data which was taken at the module thermal cycling test stand is uploaded to three composite action tables. Since a complete test was performed in most cases the numbers are almost identical.

D.3.1 The MODULBASIC_2_MOD_ Table

The single tags of the basic action modulbasic are discribed in the table below.

identifier	**meaning**
OBJECT_ID	14-digit module identifier
TEST_ID	unique number added by db for the correlation with the parent action
TOOL_ID	unique test station identification number
PARENT_ACTION	name of the composite action table, see table D.6
INPUT_ID	database internal number for table identification
TDATE	date and time of test
OPERATOR	name of operator who did the test
STATUSAPV	status of the APVs, see explanation below table
STATUSMUX	status of the MUX, see explanation below table
STATUSPLL	status of the PLL, see explanation below table
STATUSDCU	status of the DCU, see explanation below table
STATUSHYBRID	status of the hybrid, see explanation below table
STATUSSENSORS	not used
DCUID	24-bit DCU identifier, combination of identification bytes to a single number
PLLDAC	setting of the DAC for the VCO of the PLL when the auto-calibration was finished
NBADCHAN	number of bad channels
BADCHANLIST	list of bad channels
SETTINGS	name of the test settings file
TEMPSETUP	temperature °C, measured via temperature probe on ARC FE adapter
TEMPEXT	temperature in °C, measured by an external probe
HUMSETUP	relative humidity in %, measured by humidity sensor on ARC FE adapter
HUMEXT	relative humidity in %, measured by an external probe
TEMPHYBDCU	temperature of the DCU measured by the DCU (channel 7) in ADC counts
TEMPHYBNTSC	temperature of the hybrid measured by the DCU (channel 4) in ADC counts

identifier	**meaning**
TEMPSENNTSC1	voltage drop over thermistors on module measured by ARC FE adapter, thermistor is driven by DCU 20 µA output current
TEMPSENNTSC1DCU	like TEMPSENNTSC1 but measured by the DCU (channel 0)
TEMPSENNTSC2	not used
IHYB250, IHYB125, VHYB250,VHYB125	hybrid supply voltages and currents measured by ARC FE adapter
VHYB25DCU, VHYB125DCU	hybrid voltage supply measured by the DCU (channel 1 and channel 2)
HVBIAS, ILEAK	bias voltage in V and current in nA which were applied during tests
ILEAKDCU	leakage current measured by the DCU (channel 3)
VTEST1, ITEST1	depletion voltage and current when voltage is set to 300 V
VTEST2, ITEST2	depletion voltage and current when voltage is set to 450 V
NOISEPION, NOISEPIOFF, NOISEDION, NOISEDIOFF	list of common mode subtracted noise for each channel for various APV operation modes, the data is multiplied with 100
RAWNOISEPION, RAWNOISEPIOFF, RAWNOISEDION, RAWNOISEDIOFF	list of raw noise for each channel for various APV operation modes, the data is multiplied with 100
CMNNOISEPION, CMNNOISEPIOFF, CMNNOISEDION, CMNNOISEDIOFF	list of common mode noise for each APV for various operation modes multiplied with 100
AVGCMNPION, AVGCMNPIOFF, AVGCMNDION, AVGCMNDIOFF	average common mode noise of module for various APV operation modes
AVGNOISEPION, AVGNOISEPIOFF, AVGNOISEDION, AVGNOISEDIOFF	average noise of module for various APV operation modes
PEDPION	list of pedestals for each channel multiplied with 10 in peak inverter on mode

identifier	**meaning**
AVGPEDPION	average pedestal of module in peak inverter on mode
RMSPEDPION	root mean squared of pedestals in peak inverter on mode
BADCHPED	list of bad channels with corresponding flag from pedestal and noise test (see also section D.3.1 and table D.13)
CALPAPIOFF, CALPAPION, CALPADIOFF, CALPADION	list of maximum calibration pulse amplitude for each channel for various APV operation modes, the data is multiplied by 10
CALPTPIOFF, CALPTPION, CALPTDION, CALPTDIOFF	list of calibration pulse peak time for each channel for various APV operation modes
AVGCALPAPIOFF, AVGCALPAPION, AVGCALPADIOFF, AVGCALPADION	average calibration pulse amplitude for each APV for various operation modes
AVGCALPTPIOFF, AVGCALPTPION, AVGCALPTDIOFF, AVGCALPTDION	average calibration pulse peak time for various APV operation modes
BADCHCALPROF	list of bad channels with corresponding flag from calibration test, see also section D.3.1 and table D.14
APVMODEPINHOLE	APV operation mode during pinhole test
CALAPINHOLE	difference between maximum and minimum pulse height in pinhole test for each channel, data is multiplied with 10
AVGCALAPINHOLE	average difference between maximum and minimum pulse height in pinhole test over all channels
IPINHOLE	maximum detector leakage current during pinhole test
BADCHPINHOLE	list of bad channels in pinhole test, see also table D.16
APVMODECAL	APV operation mode for data taken at fixed timing
CALA	list of calibration pulse amplitude at fixed timing for each channel, data is multiplied with 10
AVGCALA	average calibration pulse amplitude at fixed timing for module

identifier	meaning
BADCHCAL	list of bad channels found in calibration test at fixed timing, see also table D.15
APVMODEBP	APV operation mode during backplane pulse test
CALBP	list of backplane pulse signal height at fixed timing for each channel, data is multiplied with 10
AVGCALBP	average backplane pulse signal height at fixed timing for module
BADCHBP	list of bad channels found in backplane pulse test
CHFLAG	list of bad channels with fault identification flag
VOLTAGEIV, CURRENTIV	list of detector depletion voltage and leakage current during IV test
TIMEIT,CURRENTIT	change of leakage current with time, data is not taken in ARCS
MODULBASIC_VAL	total result of test, see subsubsection D.3.1
STATUS	status of data, see also table D.1
TCOMMENT	comment

Table D.8: The content of the MODULBASIC_2_MOD_ table.

The following sections provide information on the tags with binary-coded information.

The Status Tags

The status tags in the modulbasic table are coded bit by bit. When a fast test is performed the status of the chips is determined and stored in the fast test folder of the corresponding record in the ARCS root file. The ARC XML parser extracts the results and fills them into the XML result file which is send to the database.
There is a dedicated status tag for the APVs, the PLL, the MUX, the DCU, the hybrid and the sensors. The STATUSSENSORS tag is not used because sensor problems can be described in much more detail in a so-called free action. More information about the usage of the free action is given on the CMS tracker construction database web page [36]. The meaning of the single bits of the filled status tags are listed in the tables below.

The Channel Flag Lists

The module tests which were expected to be useful for the detection and identification of channel failures at the time when the MODULBASIC_2_MOD_ table was designed, were given dedicated channel flag lists. These lists contain the channel numbers and a flag for all channels which showed a non typical behaviour in a particular test. The flag indicates in what respect and which property of the channel differs from the average channel behaviour. The modulbasic table contains five channel flag lists for single

bit	meaning
1	no APV responded to I^2C communication
2, .. 7	APV 0x40,.. 0x4A showed I^2C problems
8, .. 13	APV 0x40, .. 0x4A showed data problems
14, .. 19	APV 0x40, .. 0x4A has low header height
19, .. 24	APV 0x40, .. 0x4A has noise problems
25, .. 30	APV 0x40, .. 0x4A has low calibration amplitude
31	not all APVs could be assigned to ARC read-out channel

Table D.9: The coding of APV properties in the STATUSAPV tag.

bit	meaning
1	I^2C failures occurred during PLL communication
2	PLL reported too many single event upsets
3	PLL did not lock

Table D.10: The encoding of PLL properties in the STATUSPLL tag.

bit	meaning
0	I^2C failures occurred during MUX communication
7, .. 14	resistance of MUX resistor 0, .. 7 differs from others

Table D.11: The encoding of MUX properties in the STATUSMUX tag.

bit	meaning
1	I^2C failures occurred during DCU communication
2	DCU reported too many single event upsets
3, .. 10	acquisition or data out of range failure on DCU channel 0, .. 8
19	DCU ID could not be determined

Table D.12: The encoding of DCU properties in the STATUSDCU tag.

tests and a sixth which contains the summary of all tests. The flags of this tag inform about physical faults causing the different behaviour if this can be derived from the measurements.
The lists badchped, badchcalprof and badchcal are generated from the lists for the various APV operation modes. Each channel which failed the acceptance criteria in at least one mode is listed. For the badchped and badchcalprof lists the disjunction of the flags for the single modes is calculated for each channel. In the case of the badchcal list the channel flag is determined by the mode where the absolute value of the flag was highest. The flags for the pinhole test do not need to be combined as the test is done for a single mode. As the backplane pulse test did not become a part of the test scenario for module qualification [56] the test is usually not done and thus the flag list

is not filled. The meaning of the single flags for the five remaining channel flag lists are listed in the tables below.

flag	**meaning**
2	very very low noise, $noise_{ch} < absPinholeNoise$
4	very low noise, $absPinholeNoise \leq noise_{ch} < absTwoOpenNoise$
8	low noise, $absTwoOpenNoise \leq noise_{ch} < absOneOpenNoise$
16	high noise, $absNoisy < noise_{ch}$

Table D.13: The flags for the BADCHPED tag.

The cut is applied on the common mode subtracted noise which is taken in the deep test part of ARCS. The limits for the noise are defined in the testsettings files (see 3.6).

flag	**meaning**
2	small maximum pulse height, $PH_{ch} < medianPH_{APV} \cdot (1 - Height\_Perc\_lo)$
4	high maximum pulse height, $medianPH_{ch} \cdot (1 + Height\_Perc\_hi) < PH$
8	very very small peak time, $PT < medianPT_{calgroup} \cdot (1 - PeakTime\_Abs\_vevelo)$
16	very small peak time, $medianPT_{calgroup} \cdot (1 - PeakTime\_Abs\_vevelo) \leq PT <$ $medianPT_{calgroup} \cdot (1 - PeakTime\_Abs\_velo)$
32	small peak time, $medianPT_{calgroup} \cdot (1 - PeakTime\_Abs\_velo) \leq$ $PT_{ch} < medianPT_{calgroup} \cdot (1 - PeakTime\_Abs\_lo)$
64	high peak time, $medianPT \cdot (1 + Height\_Perc\_hi) < PT_{ch}$

Table D.14: The flags for the BADCHCALPROF tag.

For the BADCHCALPROF tag the maximum calibration pulse height and the peak time is analysed. The cuts for the identification of failures are defined in the testsettings file (see 3.6).

The flags for the BADCHCAL list are extracted from the root file. For this reason the flags are fixed once a calibration pulse test was done. This implies that the flags are not recalculated if different cuts are applied on the data.

Like the BADCHCAL list the BADCHPINHOLE flags are extracted from the root file.

The flags of the CHFLAG tag indicate the estimated failure cause which is usually a physical defect of a read-out line or capacitor or a broken APV input. A detailed analysis of the reliability of fault identification was done in [37].

flag	meaning
-3	very very small pulse height, $PH_{ch} < \overline{PH}_{APV} \cdot (1 - Height\_Perc\_vevelo)$
-2	very small pulse height, $\overline{PH}_{APV} \cdot (1 - Height\_Perc\_vevelo) \leq PH_{ch} < \overline{PH}_{APV} \cdot (1 - Height\_Perc\_velo)$
-1	small pulse height, $\overline{PH}_{APV} \cdot (1 - Height\_Perc\_velo) \leq PH_{ch} < \overline{PH}_{APV} \cdot (1 - Height\_Perc\_lo)$
1	high pulse height, $\overline{PH}_{APV} \cdot (1 + Height\_Perc\_hi) \leq PH_{ch} < \overline{PH}_{APV} \cdot (1 + Height\_Perc\_vehi)$
2	very high pulse height, $\overline{PH}_{APV} \cdot (1 + Height\_Perc\_vehi) \leq PH_{ch}$

Table D.15: The flags for the BADCHCAL tag.

flag	meaning
1	high difference between maximum and minimum calibration pulse height, $PinDiff_Abs_hi \leq PH_{diff} < PinDiff_Abs_vehi$
2	very high difference between maximum and minimum calibration pulse height, $PinDiff_Abs_vehi \leq PH_{diff}$

Table D.16: The flags for the BADCHPINHOLE tag.

flag	token	meaning
2	PSO	discontinued line between pitch adapter and sensor
4	LPSO	likely discontinued line between pitch adapter and sensor
8	SSO	discontinued line between sensors
16	LSSO	likely discontinued line between sensors
32	DIS	unlocalised discontinued line
64	NOI	noisy channel
128	SHORT	short circuited read-out channels
256	PINHOLE	broken read-out capacitor, pinhole
512	HLC PINH	broken read-out capacitor at high leakage currents, high leakage current pinhole
1024	UKN	fault is unknown
2048	SAT	saturated channel, channel with no response to calibration pulse injection
4096	INV	broken inverter, channel works only in APV inverter off modes

Table D.17: The flags for the CHFLAG tag indicate the physical fault of bad channels.

The MODULBASIC_VAL

The total test result is indicated by the value of the MODULBASIC_VAL tag. Positive numbers qualify a module as usable for the tracker, a negative number is applied when the quality of the module is insufficient and a zero indicates modules of the best per-

forming category.
The grade of a module is determined by the percentage of bad strips S_{bad} and the leakage current averaged over the number of sensors $\overline{I}_{leak}$. The leakage current $\overline{I}_{leak,sensor}$ is the average leakage current of the bare sensors which is measured by the sensor manufacturer or sensor quality test centre and needs to be extracted from the database. The various flags from the result tag are listed in table D.18.

flag	**meaning**
:8:	grade B_F, 1 $\% \leq S_{bad} < 2\ \%$ and $\overline{I}_{leak}$ < 10 µA and $5 \times \overline{I}_{leak,sensor} \leq \overline{I}_{leak}$
:4:	grade B, 1 $\% \leq S_{bad} < 2\ \%$ and $\overline{I}_{leak}$ < 10 µA and $\overline{I}_{leak} < 5 \times \overline{I}_{leak,sensor}$
:2:	grade A_F, $S_{bad} < 1\ \%$ and $\overline{I}_{leak}$ < 10 µA and $5 \times \overline{I}_{leak,sensor} \leq \overline{I}_{leak}$
:0:	grade A, $S_{bad} < 1\ \%$ and $\overline{I}_{leak}$ < 10 µA and $\overline{I}_{leak} < 5 \times \overline{I}_{leak,sensor}$
:-1:	grade C, 2 $\% \leq S_{bad}$ and $\overline{I}_{leak}$ < 10 µA
:-2:	grade C, $S_{bad} < 2\ \%$ and 10 µA $\leq \overline{I}_{leak}$
:-4:	grade C, 2 $\% \leq S_{bad}$ and 10 µA $\leq \overline{I}_{leak}$
:-8:	grade C, module cannot be read out
:-16:	grade C, module is mechanically damaged
:-32:	grade C, dismounted

Table D.18: The possible flags for the MODULBASIC_VAL tag which indicate the test result by the grade applied on a module.

Appendix E

Queries

The various queries which are used for extraction of information form the central tracker database [36] are given in the various sections of this chapter. The basic syntax of all queries is:

$select$ content $from$ table $where$ selection

content	the data of interest
table	one or more tables which contain the data of interest
selection	the conditions the data has to meet

E.1 The Database Queries for Extraction of Additional Object Information

The database queries for extraction of the data in tables C.2 and C.7 are described in this section. In the first part the extraction of hybrid information is described. The queries for the sensor manufacturer information are covered by the second part.

The number of hybrids is given by the number of distinct object identification numbers which are the object_ids. The number of distinct object_ids which are assigned to hybrids of identical version are counted by the first query 1). The number of assembled hybrids is given by the number of hybrid objects which have a container id. The container id identifies the composite object the hybrid is built in (query 2). The third column is filled with the number of hybrids which are assembled on a TEC or TOB substructure which is ready to go into the final detector. These hybrids are assembled on module which are assembled on petals or rods. The petals and rods are not prototypes and they are not broken (query 3). TIB and TID hybrids are not considered because the assembly of the corresponding modules is not documented in the central database. The TID and TIB consortium decided to document the assembly on shells and the inner disks in a separate database.

1.
```
select
  count (distinct object_id), version from object_assembly
where
  object='HYB'
group by
  version
```

2.
```
select
  count (distinct object_id), version from object_assembly
where
  object='HYB' and container_id is not NULL
group by
  version
```

3.
```
select
  count(distinct OA.object_id) MOD, HYB.HYB_VER
from
  object_assembly OA,
  object_assembly OA2,
  history H,
  (select
    object_id ID, max(history_id) MAX
     from
      history group by object_id) HIST,
  (select
    container_id MOD_ID, version HYB_VER
     from
      object_assembly where object='HYB´) HYB
where
  H.history_id=HIST.MAX and H.object_id=HIST.ID and
  OA.object_id=HYB.MOD_ID and OA2.object_id=OA.container_id and
  OA2.version<'90' and OA2.object_id=H.object_id and H.faulty='F'
group by
  HYB.HYB_VER
```

The manufacturer of the sensors is encoded in the identification numbers of the sensors. For this reason the number of distinct sensor identification numbers in a certain range is counted. Furthermore only those sensors are counted which are assembled in modules which are assembled in petals or rods and so on. The tracker database contains no information on the assembly status of TIB and TID modules. This is not of relevance for the calculation as these parts of the tracker use thin sensors which were entirely produced by HPK. The query for the number of thick sensors from HPK is

given by:

```
select
 count (distinct object_id), type_description
from
 object_assembly oa,
 object_description od,
 (select
   object_id ID
    from
     object_assembly

»where

»object='TEC' or object='TOB')TECTOB,
 (select
   object_id ID, container_id CID
    from
     object_assembly
    where
    (object='DISK' or object='TOBCS') and
     container_id is not NULL) DISKTOBCS,
 (select
   object_id ID, container_id CID
    from object_assembly where
     (object='TECCR' or object='TOBCR') and
      container_id is not NULL) TECCRTOBCR,
 (select
   object_id ID, container_id CID
    from
     object_assembly
    where
     (object='PETAL' or object='ROD') and
      container_id is not NULL) PETALROD,
 (select object_id ID, container_id CID
   from
    object_assembly
   where
    object='MOD'and container_id is not NULL)MOD
where
 oa.object=od.object and oa.version=od.version and oa.type=od.type and
  oa.object='SEN' and oa.object_id>30220000000000 and
  oa.object_id<30230000000000 and oa.version=1 and
  oa.container_id=MOD.ID and MOD.CID=PETALROD.ID and
  PETALROD.CID=TECCRTOBCR.ID and TECCRTOBCR.CID=DISKTOBCS.ID
```

```
  and DISKTOBCS.CID=TECTOB.ID
group by
 type_description
```

For extraction of the numbers from STM the constraint on the identification number range has to be modified.

E.2 The Rate of PLL problematic Hybrids

The rate of PLL problematic hybrid is given by the quotient of the number of hybrids with a PLL problem and the number hybrids tested for this particular problem. The number of distinct hybrids with the PLL problem is determined.

select count (distinct object_id) from testwithpa_1_hyb_ where tcomment like 'PLL Force%'

The answer of this query is 2317.
For the determination of the number of hybrids tested for the feature the date of the first report tells since when the test station software was capable to detect and report the problem. This date must be determined for each teststation involved. All test stations have a distict tool_id.

select min (tdate), tool_id from testwithpa_1_hyb_ where tcomment like 'PLL Force%' group by tool_id

The problem is detected in test scenarios including at least one cooling cycle. The relevant scenarios must have found the PLL problem at least once. These scenarios are given by:

select distinct script from testwithpa_1_hyb_ where tcomment like 'PLL Force%'

The number of hybrids which were checked for the PLL feature is given by the number of hybrids which was tested with one of these scripts. At the same time the date of the measurement must be past the first occurance of a PLL Force comment.

```
 select count ( distinct object_id ) from testwithpa_1_hyb_ where (
    ( tool_id=707 and tdate > to_date ( '2004-08-27' , 'YYYY-MM-DD' )) or
    ( tool_id=300 and tdate > to_date ( '2003-12-09' , 'YYYY-MM-DD' )) or
    ( tool_id=801 and tdate > to_date ( '2004-07-21' , 'YYYY-MM-DD' )) )
and script in (
    '//PCEPCMT69/teststation/bin/crater_cycle_01.cfg' ,
    '//PCEPCMT69/teststation/bin/crater_cycle_02.cfg' ,
    '//PCEPCMT69/teststation/bin/onecycle_02.cfg' ,
    '//PCEPCMT69/teststation/bin/onecycle_03.cfg' ,
```

'//PCEPCMT69/teststation/bin/onecycle_04.cfg' ,
'//PCEPCMT69/teststation/bin/onecyclenopulser.cfg' ,
'//PCEPCMT69/teststation/bin/overnightcyclesnopulser.cfg' ,
'//PCEPCMT69/teststation/bin/tencycle_04.cfg' ,
'//PCEPCMT69/teststation/bin/torture_qualif_01.cfg' ,
'/C/CMS/HybARCS_7_02_04/UCSB_Binaries_7_2/fivecycle_SC.cfg' ,
'/C/CMS/HybARCS_7_02_04/UCSB_Binaries_7_2/onecycle_02.cfg' ,
'/C/CMS/new_code/UCSB_Binaries_7_1/onecycle_02.cfg' ,
'/C/N1/onecycle_02.cfg' ,
'/C/teststation/bin/fiftycycle_01.cfg' ,
'/C/teststation/bin/onecycle_02.cfg' ,
'/C/teststation/bin/onecycle_04.cfg' ,
'/C/teststation/bin/tencycle.cfg' ,
'/C/teststation/bin/tencycle_02.cfg' ,
'/C/teststation/bin/tencycle_03.cfg' ,
'/C/teststation/bin/tencycle_04.cfg' ,
'/C/teststation/bin/tencycle_no_pulser_04.cfg' ,
'/C/teststation/bin/torture_qualif_01.cfg' ,
'/C/teststation/bin/torture_test_01.cfg' ,
'/C/teststation/bin/torture_test_02.cfg')

The answer of the query is 10928. The rate is thus:

$$\frac{2317}{10928} = 0.212 \tag{E.1}$$

The rate of hybrids where the PLL failure was detected is 21.2 %.

E.3 Number of Tests in MODULBASIC_2_MOD_ table

The query for extraction of the data in table D.7 is:

```
select
 count(T1.OBJ), T1.ACT
from
 (select distinct (tdate), object_id OBJ, parent_action ACT
  from
   modulbasic_2_mod_)T1
group by
 T1.ACT
```

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