

Development of a Test System for the Quality Assurance of Silicon Microstrip Detectors for the Inner Tracking System of the CMS Experiment

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Zusammenfassung

Beim Bau des inneren Spursystems des CMS-Experiments (Compact Muon Solenoid) am Beschleuniger LHC (Large Hadron Collider) des europäischen Kernforschungszentrums CERN (Genf, Schweiz) sollen zwei unterschiedliche Silizium-Detektor-Technologien zum Einsatz kommen. Während die innere Region des Spurdetektors aus Silizium-Pixel-Detektoren besteht, wird der äußere Bereich mit Silizium-Mikrostreifen-Detektoren bestückt. Der Silizium-Mikrostreifen-Spurdetektor wird aus etwa 15 000 einzelnen Modulen aufgebaut sein, die jeweils aus einem bzw. zwei Silizium-Sensoren, der Ausleseelektronik (Front End Hybrid) und einer mechanischen Halterung bestehen. Dieser Detektor stellt eine aktive Fläche von 198 m^2 zur Verfügung und besitzt ca. zehn Millionen analoge Kanäle, die mit einer Frequenz von 40 MHz ausgelesen werden. Die Herstellung dieser großen Anzahl von Modulen stellt eine beispiellose Herausforderung dar, die zahlreiche Industriebetriebe und Forschungseinrichtungen verschiedener Länder einbezieht. Die vorliegende Arbeit beschäftigt sich mit der Physik der Silizium-Sensoren und der Vorbereitung der Modul-Massenproduktion, welche etwa ein Jahr in Anspruch nehmen wird. Während dieser Phase ist es erforderlich, eine effiziente Produktion zu gewährleisten. Dies erfordert ein Testsystem, das die komplette Produktionsphase überwachen kann und auf diese Weise eine zuverlässige Qualitätssicherung sowohl der Hybride als auch der Module sicherstellt. In Aachen wurde das Testsystem ARC (APV Readout Controller) entwickelt und allen beteiligten Instituten zur Verfügung gestellt.

Diese Arbeit führt das ARC-System ein und beschreibt die Entwicklung der speziell für dieses System entworfenen Auslese- und Analysesoftware (ARCS). Basierend auf der Charakterisierung von 21 Prototyp-Modulen, der sogenannten Expressline-Serie, die im Jahr 2002 von der Spurdetektor-Endkappen-Kollaboration gebaut wurden, konnten die Eignung und die Funktionalität des ARC-Systems demonstriert werden. Desweiteren ermöglichten die Tests der Module bei Raumtemperatur und bei tiefen Temperaturen eine Verbesserung der existierenden Analyse-Routinen sowie die Entwicklung neuer Tests, die in die ARCS-Umgebung eingebettet wurden. Ein zentrales Ziel dieser Messungen war eine umfassende, redundante Fehlerermittlung. Insgesamt zeigten sich drei verschiedene Fehlerarten: offene Bonds, Kurzschlüsse und Pinholes. Von den 21×512 Auslesekanälen wurden 29 Kanäle als defekt identifiziert und konnten einem der drei Fehlertypen zugeordnet werden. Diese kleine Fehlerrate von weniger als 0.3% unterstreicht die gute Qualität der ausgewählten Modulkomponenten und der fertigen Module. Hinsichtlich der anstehenden Massenproduktion der Silizium-Module sind insbesondere die vergleichbaren und reproduzierbaren Messergebnisse ermutigend.

Abstract

The inner tracking system of the Compact Muon Solenoid (CMS) experiment at the Large Hadron Collider (LHC) which is being built at the European Laboratory for Particle Physics CERN (Geneva, Switzerland) will be equipped with two different technologies of silicon detectors. While the innermost tracker will be composed of silicon pixel detectors, silicon microstrip detectors are envisaged for the outer tracker architecture. The silicon microstrip tracker will house about 15,000 single detector modules each composed of a set of silicon sensors, the readout electronics (front end hybrid), and a support frame. It will provide a total active area of 198 m^2 and ten million analogue channels read out at the collider frequency of 40 MHz. This large number of modules to be produced and integrated into the tracking system is an unprecedented challenge involving industrial companies and various research institutes from many different countries.

This thesis deals with the physics of silicon sensors and the preparation of the large-scale production of front end hybrids and modules which will span over one year. During this period it is essential to assure efficient and reproducible manufacturing as well as diagnostic procedures among all centres. This demands a test environment capable of supervising the complete production phase while providing a reliable quality assurance of front end hybrids and modules. To meet these requirements, the test setup ARC (APV Readout Controller) was developed in Aachen and distributed among all collaborating institutes. In this thesis, the ARC system is introduced and, in particular, the development of test procedures implemented in the corresponding readout and analysis software (ARCS) are described.

Based on the characterization of a pre-series of 21 silicon modules, called express-line, built in the year 2002 by the tracker end cap collaboration, the functionality and suitability of the ARC system could be demonstrated. The measurements of these modules, performed at ambient and at low temperatures, allowed the improvement of existing test procedures as well as the development of new tests incorporated in the ARCS environment to guarantee a comprehensive and redundant failure determination.

Three types of faults showed up during the different test procedures: open bonds, shorts, and pinholes. In total only 29 channels (of 21×512 channels) were identified as faulty channels affected by one of the failures mentioned above. This leads to a failure rate of less than 0.3% which emphasizes the good quality of the components used and the accurate manufacturing methods. Especially the reproducibility and the comparability of the test results are encouraging with respect to the enormous challenge of the large-scale production the CMS experiment is facing.

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Preface

This thesis deals with the quality assurance of front end hybrids and silicon microstrip detector modules envisaged for the inner tracking system of the Compact Muon Solenoid detector (CMS) at the future Large Hadron Collider (LHC) at CERN. The CMS tracker will be equipped with about 15,000 silicon microstrip detector modules which have to be produced within a short period. In order to keep track of every single component of a module assembled in industry and in the various CMS production centres, a reliable diagnostic and test system is needed. Such a system requires appropriate hardware and software designs matching the specifications of the test objects. In this thesis the developments of the APV Readout Controller test setup (ARC) and the corresponding readout software, called ARCS, are presented.

The [first chapter](#) gives a short introduction into the Standard Model of Particle Physics, and pose still open questions concerning the nature of matter. Presumably, the LHC will be able to answer some of these basic questions. Thus a brief description of this collider and of one of the advanced experiments, the CMS detector, are also given in the first chapter.

The principle of particle detection using silicon material is presented in [chapter 2](#). The harsh radiation environment expected in the tracking region of the CMS experiment limits the silicon sensor technology suited to be used. This is also true for the detector's readout electronics, called front end hybrid, which is composed of seven (or nine) ASIC chips and several SMD components mounted on a specific substrate. This front end electronics is the topic of [chapter 3](#). [Chapter 4](#) deals with the final layout of the silicon microstrip detector modules as well as their production problems and flaws to be expected during a large-scale manufacturing.

Based on the features and characteristics of the hybrids and modules, an advanced test system for their quality assurance was developed. Thus [chapter 5](#) is dedicated to the ARC test setup suited to provide the complete access of the test objects. The interface between the ARC setup and the operator is realized with the specific C++ and LabVIEW based readout and analysis software ARCS. The test procedures and calculation algorithms implemented in ARCS are described in detail in [chapter 6](#).

The production of 21 tracker end cap modules in two batches, called express-line 1 and 2, were used to improve and to establish the ARC software routines. The measurements performed with ARCS were done at ambient temperature in a clean room environment and at low temperatures in a specific cooling box. [Chapter 7](#) presents the results obtained from the characterization of both express-line batches.

Chapter 1

Introduction

High energy physics basically deals with the study of the ultimate constituents of matter and the nature of their interactions. Experimental research in this field of science is carried out with specific particle accelerators and their associated detection devices. With the scheduled construction of the *Large Hadron Collider (LHC)* at CERN¹ until 2007, the understanding of the structure of matter will continue to be an active subject of high energy physics.

1.1 The Standard Model of Particle Physics

The present knowledge of the constituents of matter is incorporated in the so-called *Standard Model of Particle Physics (SM)* which is the result of an immense experimental and inspired theoretical effort, covering more than fifty years of experience and precise measurements. This section is not intended to give a comprehensive introduction into the SM, but to discuss its most essential ideas and problems. For a detailed description see [1].

The SM asserts that the material in the universe is made up of elementary fermions interacting through fields, of which they are the sources. The particles associated with the interactions fields are gauge bosons. All fermions have spin $\frac{1}{2}$ while bosons are characterized by an integer spin both given in units of $\hbar$.

Table 1.1 depicts an overall view of the fundamental fermions which can be divided into two categories: leptons (electron e , muon μ , tau lepton τ , and the associated neutrinos) and quarks (up u , down d , charm c , strange s , top t , and bottom b). The leptons and quarks are organized in generations each including a left-handed doublet of the weak isospin and right-handed singlets of particles. For every particle there exists an antiparticle which has the same mass, spin, and isospin as the particle. An antiparticle differs from its particle in the signs of all additive quantum numbers to which the electric charge belongs, for instance.

There are four known interactions between the fundamental fermions: the electromagnetic, the weak, the strong, and the gravitational² interaction. Each interaction is

¹Conceil Européenne pour la Recherche Nucléaire, Geneva, Switzerland.

²The gravitation force is not yet implemented in the SM, since on the scales of particle physics

Fermions	Generation 1	Generation 2	Generation 3	Q [e]	T ₃
Leptons	$\begin{pmatrix} \nu_e \\ e \end{pmatrix}_L$	$\begin{pmatrix} \nu_\mu \\ \mu \end{pmatrix}_L$	$\begin{pmatrix} \nu_\tau \\ \tau \end{pmatrix}_L$	0 -1	+1/2 -1/2
	e_R	μ_R	τ_R	-1	0
Quarks	$\begin{pmatrix} u \\ d \end{pmatrix}_L$	$\begin{pmatrix} c \\ s \end{pmatrix}_L$	$\begin{pmatrix} t \\ b \end{pmatrix}_L$	+2/3 -1/3	+1/2 -1/2
	u_R	c_R	t_R	+2/3	0
	d_R	s_R	b_R	-1/3	0

Table 1.1: Fundamental fermions in the Standard Model of Particle Physics. Q is the particle charge whereas T₃ is referred to as the weak isospin. Doublets of the weak isospin are indicated by parenthesis. The chiral states are named left-handed (*L*) and right-handed (*R*).

mediated by specific gauge bosons, such as the massless photon γ , which is responsible for the electromagnetic force. The massive quanta of the weak interaction fields between fermions are the charged $W^\pm$ bosons and the neutral Z^0 boson. Eight massless gluons g mediate the strong force. Table 1.2 summarizes some properties of the gauge bosons.

From the theoretical point of view the SM is based on the quantum field theories of the strong interaction, the electroweak interaction, the *Quantum Electrodynamics (QED)* and the *Quantum Chromodynamics (QCD)*. The QED represents the unification of the electromagnetic and the weak interaction developed by Glashow, Salam, and Weinberg. In this context the existence of the gauge bosons is a direct consequence of the demand for local gauge invariance of the theory under the combined symmetry group $SU(3)_C \times SU(2)_L \times U(1)_Y$.

Bosons	Interaction	Mass [GeV/c ²]	Spin [$\hbar$]	Q [e]	Range [m]
Photon γ	electromagnetic	0	1	0	∞
Z^0	weak	$\simeq 91.2$	1	0	$\ll 10^{-16}$
$W^\pm$	weak	$\simeq 80.4$	1	± 1	$\ll 10^{-16}$
8 Gluons g	strong	0	1	0	10^{-15}
Graviton G	gravitational	0	2	0	∞

Table 1.2: Forces and the associated fundamental gauge bosons in the Standard Model. Again the gravitation is included for the sake of completeness.

Although the theoretical predictions of the SM agree remarkably well with the experimental results obtained up to the present, there are still open questions to be answered. Local gauge invariance requires all gauge bosons to be massless which contradicts the experimental measurements ($m_{W^\pm} \simeq 80.4 \text{ GeV}/c^2$ and $m_{Z^0} \simeq 91.2 \text{ GeV}/c^2$).

gravitational forces are insignificant. The gravitation is mentioned here for the sake of completeness.

The implementation of an additional complex doublet into the SM, called *Higgs field*, provides an explanation for the origin of the masses of the W and Z bosons.

The Higgs field couples to these bosons and creates their masses by spontaneous symmetry breaking. Thus the Higgs field has a non-vanishing vacuum expectation value. As a consequence of this Higgs mechanism, a scalar Higgs boson H must exist and should be observable [2–5]. In the energy regime of previous high energy physics experiments the Higgs boson could not be discovered.

Although the mass of the Higgs boson is not predicted by the SM, a certain mass range is constrained by the combination of theoretical considerations and experimental observations. The requirement of unitarity sets the upper bound to 1 TeV while the four LEP³ experiments ALEPH, DELPHI, L3 and OPAL at CERN established a lower bound for the Higgs mass of $114.4 \text{ GeV}/c^2$ at 95% confidence level [6]. In addition, indirect experimental constraints are obtained from precision measurements of the electroweak parameters depending logarithmically on the Higgs boson mass through radiative corrections. Currently the combined measurements⁴ result in an upper limit of $219 \text{ GeV}/c^2$ at 95% confidence level. Since the LEP experiments have been terminated in November 2000, the essential question about the origin of mass has to be answered by the next generation of particle accelerators, such as the LHC at CERN.

Despite its success, the SM is not able to explain the nature of matter completely. There are several open questions to be answered:

- Why does the model contain 18 free parameters⁵ to be obtained experimentally (three coupling constants, two boson masses, three lepton masses, six quark masses, and four parameters given by the Cabbibo-Kobayashi-Maskawa (CKM) matrix)?
- Why do exactly three generations of quarks and leptons exist?
- Why are all fermion masses so different from each other? The question is also known as hierarchy problem of the SM.
- Do the fundamental particles have a sub-structure?
- What happens to the four forces at extremely high energy scales?
- What is the mass of the Higgs boson (if it exists)?

Although the SM is not the final description of nature, it has to be included in each succeeding model. At present a favoured model candidate is represented by the *Minimal Supersymmetric Standard Model (MSSM)*. It postulates that every fermion gets a boson as supersymmetric partner and vice versa. Therefore the fundamental particle

³Large Electron Positron Collider.

⁴The LEP results are combined with electroweak measurements from other experiments, notably NuTeV, CDF, D0, and SLD [6].

⁵Recent experimental results prove that neutrinos show oscillations thus not being massless [7]. As a consequence, the neutrino sector has to be modified in the SM leading to at least seven additional free parameters.

spectrum will be doubled in the MSSM. Also the Higgs sector will be affected introducing four additional Higgs particles: two charged Higgs bosons ($H^\pm$), one scalar Higgs boson (h^0), and one pseudo-scalar Higgs boson (A^0). But presently no experimental hint for any kind of *Supersymmetry* (*SUSY*) exists.

New collider experiments will be able to prove the validity of the Standard Model up to the TeV energy regime within the next few decades. In particular the search for deviations from the SM is essential with respect to a consistent theory of the structure of matter.

1.2 The Large Hadron Collider

During the last decade a great contribution to the development of the Standard Model of Particle Physics has come from the LEP collider operated at CERN until the end of 2000. At present a big effort is being made to build a new collider machine as a direct LEP successor with respect to the location, the Large Hadron Collider [8]. First particle collisions are scheduled for 2007.

The Large Hadron Collider will provide proton-proton collisions at a centre-of-mass energy $\sqrt{s}$ of 14 TeV, as well as heavy ion collisions (lead-lead) up to 1,3 TeV. The accelerator ring will be housed in the former LEP tunnel with a circumference of about 27 km. Protons will be injected in the LHC ring after three pre-acceleration stages using already existing infrastructures at CERN: the Proton Linac⁶ (accelerating protons up to 50 MeV), the Proton Synchrotron (up to 25 GeV) and the Super Proton Synchrotron (up to 450 GeV). Separated beam pipes will be used to counter-rotate the injected protons which are bent in a 8.4 T magnetic field produced by superconducting magnets and accelerated by superconducting radio frequency (RF) cavities.

LHC aims for a final design luminosity $\mathcal{L}$ of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Before reaching this unprecedented value a so-called low luminosity phase at $\mathcal{L} \approx 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ will be aspired. For heavy ion collisions the luminosity will be about $10^{27} \text{ cm}^{-2} \text{ s}^{-1}$. To achieve the design luminosity the two beams have to contain up to 2808 bunches each filled with about 10.5×10^{10} protons. The bunch crossing time, called LHC clock, will be 25 ns which is equivalent to a bunch crossing rate of 40 MHz. Table 1.3 gives an overview of the most important collider parameters.

Four experimental sites situated at the bunch crossing points are established to provide a wide range of physical observations. Figure 1.1 shows the LHC tunnel with the corresponding detector sites. The experiments are named as follows:

- **ATLAS** → A Toroidal LHC ApparatuS (Point 1) [10],
- **ALICE** → A Large Ion Collider Experiment (Point 2) [11],
- **CMS** → Compact Muon Solenoid (Point 5) [12],
- **LHC-b** → Large Hadron Collider Beauty Experiment (Point 8) [13].

⁶Linear Accelerator.

Parameter	Value
particles	protons
centre of mass energy $\sqrt{s}$	14 TeV
circumference	26.7 km
luminosity $\mathcal{L}$	$10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
luminosity lifetime	10 h
filling time	7.5 min
bunch crossing frequency	40 MHz
bunch crossing time	25 ns
crossing angle	300 μrad
bunch length	7.5 cm
bunches/ring	2,808
particles/bunch	10.5×10^{10}
number of dipoles	1,232
dipole field	8.4 T
dipole length	14.3 m
number of quadrupoles	506
beam radius	16 μm
beam current	536 mA
stored energy	334 MJ

Table 1.3: List of some important LHC design parameters.

Source: [9]

CMS and ATLAS are general purpose detectors, while LHC-b is specially designed to study CP violation in B meson decays or other phenomena related to B meson physics. ALICE deals with heavy ion collisions and the observation of strongly interacting particles at very high densities forming the quark-gluon plasma, a special phase of matter.

1.3 Physics at the Large Hadron Collider

The main field to be covered by the proton-proton physics at the LHC can be divided into Standard Model processes such as heavy flavour and Higgs physics and into phenomena originating from physics beyond the SM (e.g. SUSY).

Standard processes include those physical phenomena that need detailed investigation or statistical confirmation within the energy range provided by LHC. Especially the total cross section σ_{tot} for proton-proton collisions is of great interest. At present σ_{tot} has to be extrapolated considering results obtained by previous hadron experiments (e.g. CDF⁷, UA1⁸) at lower energies. When LHC operates at design luminosity, a total cross section in the order of 100 mb is predicted. Some interesting cross sections and event rates for different physical processes produced by proton-proton collisions are shown in figure 1.2. The high production rate of $W^\pm$ and Z^0 bosons

⁷Collider Detector at Fermilab, USA.

⁸Underground Area 1, CERN.

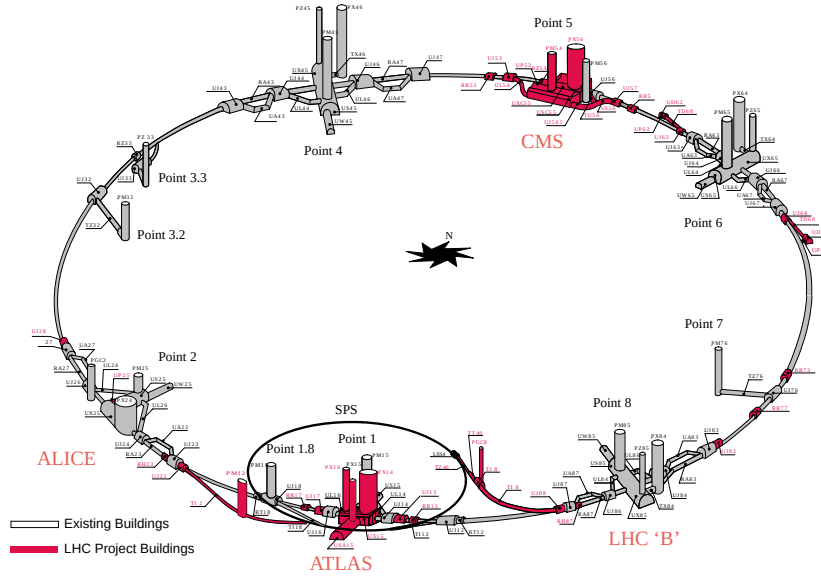


Figure 1.1: Overall view of the LHC experiments.

Source: [14]

allow investigations of electroweak SM characteristics. In addition, about 10^8 $t\bar{t}$ pairs will be produced per year (at design $\mathcal{L}$). Thus top quark properties can be determined with excellent precision including its mass, production cross section, couplings, and branching ratios.

Figure 1.2 also reveals the potency of LHC with respect to B meson physics. Due to the large number of $b\bar{b}$ pairs produced per year (about 10^{13}), studies of CP violation and precise measurements of the three interior angles of the CKM matrix unitary triangle can be envisaged.

The production of the SM Higgs boson H will be possible within the full mass range from $100 \text{ GeV}/c^2$ to $1 \text{ TeV}/c^2$ covering the actual allowed experimental and theoretical limits on the Higgs mass. This broad range provides a variety of production and decay processes. The principal mechanism for producing the SM Higgs boson over the complete mass range is called *gluon-gluon fusion* ($gg \rightarrow H$). Only in the case of a large Higgs mass the cross section for *vector-boson fusion* ($qq \rightarrow Hqq$) becomes competitive with the one for gluon-gluon fusion (see figure 1.3(a)). Within the presently favoured Higgs mass range between $114 \text{ GeV}/c^2$ and $219 \text{ GeV}/c^2$ the cross section for gluon-gluon fusion is about one order of magnitude larger than for the other processes. The most important processes for SM Higgs production are illustrated by the Feynman diagrams depicted in figures A.1 and A.2 in appendix A⁹.

Since the Higgs boson couples proportional to particle masses it decays preferentially into the heaviest particle kinematically allowed. Thus the preferred decay of the Higgs boson depends on its own mass. The most relevant decays for the favoured H mass range are shown in figure 1.3(b). For masses below $140 \text{ GeV}/c^2$ decays into fermion anti-fermion pairs ($f\bar{f}$) dominate and $H \rightarrow b\bar{b}$ has the largest branching ra-

⁹In the following the addendum “appendix X” will be omitted, since the numbering of a figure or a table in the appendix is unique.

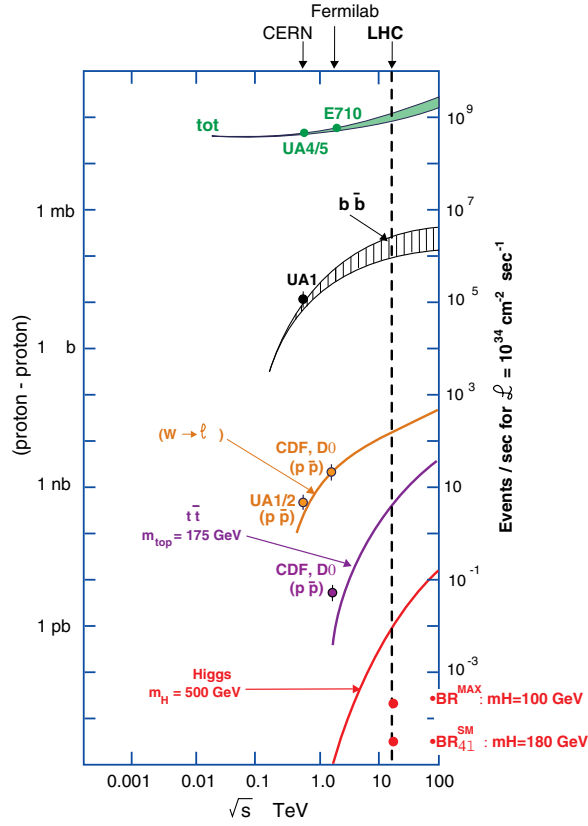


Figure 1.2: Energy dependence ($\sqrt{s}$) of some characteristic cross sections at hadron colliders assuming the LHC design luminosity. Source: [15]

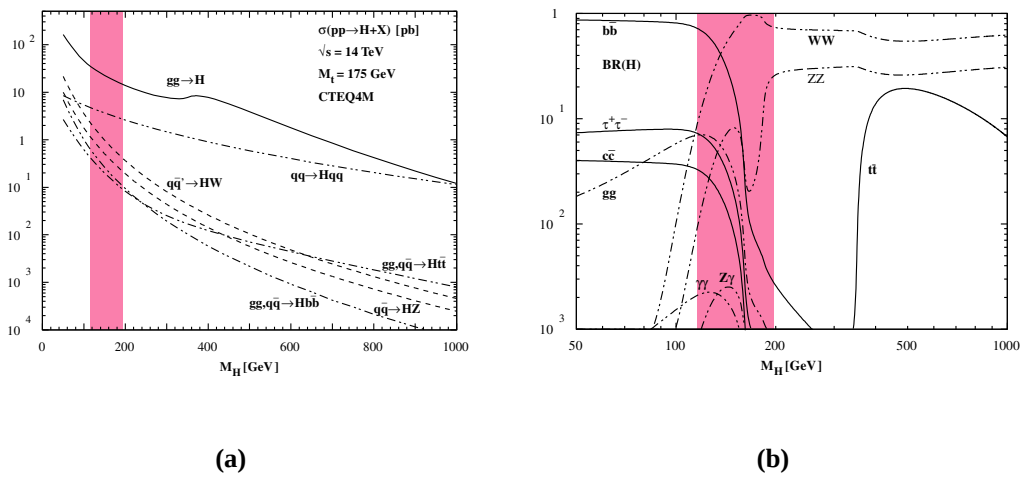


Figure 1.3: (a) Cross sections of the main production cross sections and (b) branching ratios (BR) of the SM Higgs boson. The coloured bands indicate the favoured mass range. Both figures use natural units, where c is defined to have the value 1. Source: [16]

tio. Because of the enormous QCD background superimposed the identification of this decay mode is difficult. Another promising signature is the decay $H \rightarrow \gamma\gamma$ for masses between $80 \text{ GeV}/c^2$ and $140 \text{ GeV}/c^2$ which contributes to the SM Higgs decay with a branching ratio of about 2×10^{-3} . Due to a large irreducible QCD di-photon background, a good mass resolution of the calorimeters (better than 1%) is needed. The mass range above $140 \text{ GeV}/c^2$ is dominated by $H \rightarrow WW^{(*)}, ZZ^{(*)}$ decay modes whereas $H \rightarrow WW^{(*)} \rightarrow l\bar{\nu}l\nu$ has the highest branching ratio in the mass range of $140 \text{ GeV}/c^2$ to $190 \text{ GeV}/c^2$. Since the signature relies on the determination of the missing energy of the two neutrinos, the hermetics of the detector used is crucial. For Higgs masses between $120 \text{ GeV}/c^2$ and $500 \text{ GeV}/c^2$ the decay $H \rightarrow ZZ \rightarrow l\bar{l}l\bar{l}$ is characterized by the clearest signature, since four muons or electrons are easy to detect. Thus this decay channel is also called *gold plated channel*.

Moreover, the LHC experiments will provide a large coverage of the MSSM parameter space by direct searches for the h^0, H^0, A^0 and $H^\pm$ bosons and by detecting the h^0 boson in cascade decays of SUSY particles.

1.4 The Compact Muon Solenoid

The *Compact Muon Solenoid (CMS)* is a general purpose high energy physics detector composed of several sub-detectors. Its task is to detect all decay products originating from the proton-proton collisions. To cover almost the complete solid angle around the pp interaction point, a cylindrical geometry is chosen, a so-called *barrel*, with the beam pipe as symmetry axis in its centre. The barrel part of the detector is sealed with *end caps* that are installed perpendicular to the beam axis. CMS will be a detector with a length of 22 m, a diameter of 14.6 m and a total weight of about 12,500 t.

The specific CMS layout is driven by the physical goals described in section 1.3. Inevitable properties of the CMS detector are in particular robust tracking, calorimetry and vertex reconstruction in a strong magnetic field to identify and measure precisely muons, photons, electrons, and hadron jets. Especially the so-called *b-tagging* will play an essential role with respect to *b*- and *t*-physics¹⁰ or Higgs studies in the favoured mass regime. Therefore a good impact parameter resolution and secondary vertex reconstruction are necessary. Figure 1.4 gives a three-dimensional view of the CMS detector: The central tracking system [17, 18] composed of silicon pixel detectors and silicon micro strip detectors is located nearest to the interaction point. Electromagnetic [19] and hadronic calorimeters [20] instrument the region between the tracker and the superconducting 4 T magnet [21] whereas the magnet is surrounded by an iron return yoke which holds the muon system [22]. Another huge challenge is the trigger system of CMS. The 40 MHz bunch crossing rate has to be reduced to about 100 Hz output rate for data recording while keeping high efficiency on all interesting physics channels.

Figure 1.5 shows a longitudinal view of CMS, where the origin is defined by the interaction point. The natural coordinate frame used to describe the CMS detector geometry is a right-handed Cartesian system with the x axis pointing to the centre of the LHC ring, the y axis directing upward along the vertical, and the z axis being

¹⁰The top quark decays via $t \rightarrow bW$ with a branching ratio of nearly 100%.

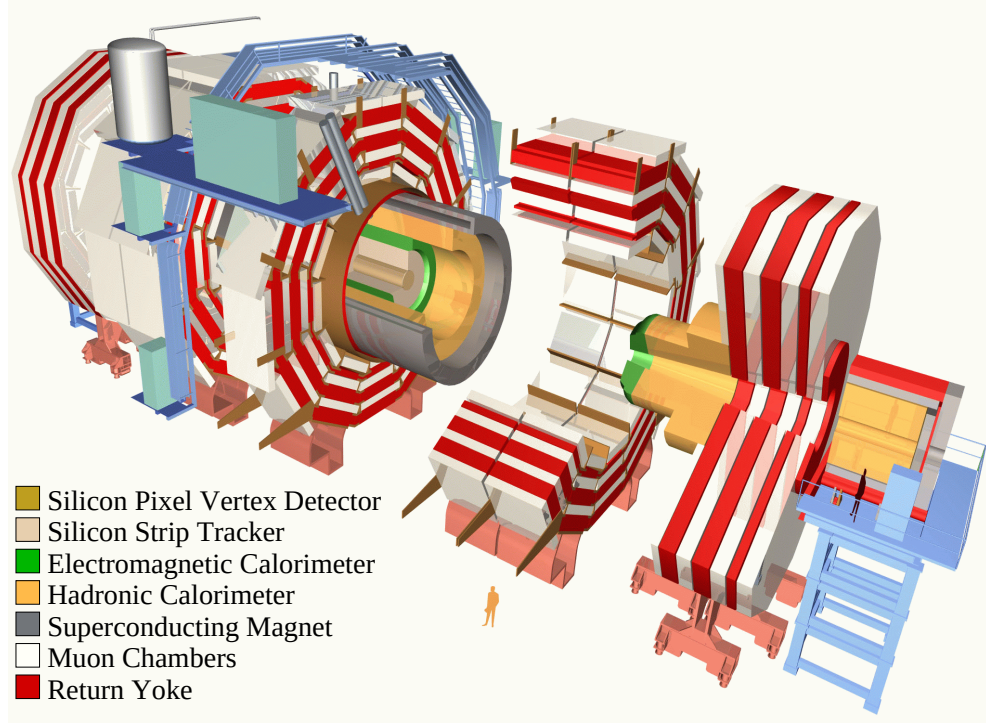


Figure 1.4: 3-d view of the CMS detector with its most important components which are listed in radial order. Source: [23]

coincident with the CMS barrel axis (the beam axis). Usually, the detector segmentation is characterized by a kinematic variable, called *pseudo-rapidity* $|\eta|$, defined in equation 1.1.

$$\eta = -\ln \left(\tan \frac{\theta}{2} \right), \quad (1.1)$$

where θ is the polar angle with respect to z axis. In the following sections some important details of the different sub-detectors will be discussed.

1.4.1 The Muon System

Four tasks have to be accomplished by the muon spectrometer, which are muon identification, muon charge determination, and muon momentum measurement, as well as a fast constitution of level 1 trigger information (see section 1.4.4). Since muons are often present in the final state, e.g. in the leptonic decay of the Higgs boson, a fast and reliable muon identification with a high momentum resolution is essential. A stand-alone muon system provides a momentum resolution of 6 – 20% for muons which have a transverse momentum p_t smaller than 100 GeV/c, and 15 – 35% for $p_t \simeq 1$ TeV/c. This can be improved by combining the muon track segments with those from the precise tracker measurement (2 – 6% for $p_t > 100$ GeV/c and 8 – 18% for $p_t \simeq 1$ TeV/c). Thus an advanced alignment system has to be envisaged. First developments and aspects of the CMS alignment system are described in [25].

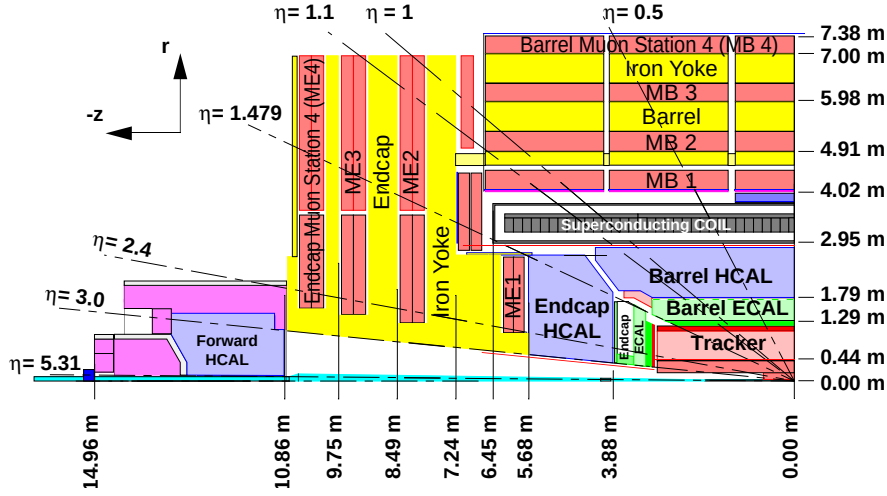


Figure 1.5: R-z cut view of the CMS detector layout.

Source: [24]

In order to cover the pseudo-rapidity range up to $|\eta| = 2.4$, three kinds of different detector technologies will be used by CMS. The barrel region will be composed of big drift chambers, the *drift tubes*. Due to the high particle rates expected in the forward region, the end caps will be made of fine segmented *cathode drift chambers*. Both detector technologies will be supported by so-called *resistive plate chambers* that are integrated in the CMS trigger system, due to their fast response.

1.4.2 The Calorimeter System

The CMS detector will be equipped with two different kinds of calorimeter systems: an inner high resolution *electromagnetic calorimeter (ECAL)* and an outer sampling *hadronic calorimeter (HCAL)*. In general, the calorimeters have to measure the direction and energy of isolated electrons, photons, and hadron jets. In addition, the calorimeter system plays an important role in the CMS trigger scheme.

The physical process that influences the material decision for the ECAL is given by the Higgs boson decay into two photons. A good energy resolution is needed to reduce the background and enhance the signal-to-noise ratio. Thus the ECAL will be a homogeneous calorimeter made of lead-tungsten PbWO_4 crystals read out by avalanche photo diodes to compensate the low light yield of the crystals.

The barrel and end cap hadronic calorimeters are made of copper absorber plates and plastic scintillators covering a rapidity range up to $|\eta|=3$. To guarantee measurements up to $|\eta|=5$, an additional forward hadronic calorimeter is placed outside the muon system near the beam axis as indicated in figure 1.5. This forward part consists of alternating layers of steel absorbers and quartz fibers.

The energy resolution of both calorimeters can be parameterized by

$$\frac{\sigma_E}{E} = \frac{a}{\sqrt{E}} \oplus \frac{\sigma_n}{E} \oplus b, \quad (1.2)$$

where a represents a stochastic term, b a constant, and σ_n the energy equivalent noise.

The energy E is given in units of GeV. For the barrel region at small $|\eta|$ the parameters for ECAL (HCAL) are as follows: $a \leq 3\%$ ($a \approx 80\%$), $b \approx 0.5\%$ ($\leq 3\%$) and $\sigma_n = 15\%$ ($\sigma_n \approx 100\%$).

1.4.3 The Tracking System

The CMS tracker is designed to provide a clean identification and a precise measurement of charged particles up to an acceptance range of $|\eta| = 2.5$. In particular the detailed vertex recognition within the strong magnetic field is a crucial factor to reach the physical goals. The tracker should meet the following demands: reconstruction of isolated high p_t muons with an efficiency of at least 98%, reconstruction of tracks within jets with 85% (for $p_t \simeq 1$ GeV) to 95% (for $p_t > 10$ GeV) efficiency, and provision of a momentum resolution of $\delta p_t/p_t \simeq (15 \cdot p_t \oplus 0.5)\%$ (p_t in TeV) for particles in the rapidity range $|\eta| < 1.6$.

Since December 1999 an all-silicon tracker is planned to equip the CMS detector [18]. In the definition of the tracker design several experimental constraints have to be considered which are correlated to the extreme radiation environment, the limits on the material budget, and the size and complexity of the system planned. In particular the expected average fluence of 1.6×10^{14} 1-MeV-equivalent neutrons per cm^2 over the operating time of ten years represents an enormous demand to the detector design.¹¹ As a consequence, the complete tracker has to be operated at -10°C to prevent the silicon material from being radiation damaged (see chapter 2.2.2 for details).

Two different silicon detector technologies will benefit the CMS tracker architecture. The innermost part of the tracker will be equipped with *silicon pixel detectors* spanning a radius from $r = 40$ mm to 200 mm with respect to the interaction point and setting up an active silicon surface of about 0.92 m^2 . Subsequently *silicon microstrip detectors* will span the outer tracker region up to $r = 1100$ mm. This part of the tracker houses an active silicon area of about 198 m^2 thus building the biggest silicon strip detector in the world.

The Pixel Tracker

Interesting events at the LHC are likely to contain several b-jets or τ -jets originating from the decay of heavy particles. In order to allow an efficient tagging of these jets, the tracking has to be extended as closely as possible towards the reaction vertex.¹² Owing the extremely high particle fluxes at these small distances, pattern recognition arguments require the innermost tracking layers to be composed of silicon pixel devices delivering true space point information with high resolution [17].

Over the full acceptance of the CMS detector the pixel system should provide at least two hits per track thus allowing secondary vertices to be determined. As a consequence, the CMS pixel system will be divided into a *barrel* and two *end cap*

¹¹The track length of particles per unit of volume per unit of time is called *flux* whereas the *fluence* is the time integral of flux. Usually the expected fluences of photons, neutrons, and charged hadrons (e.g. kaons and pions) are normalized to an equivalent fluence Φ_{eq} of neutrons with an energy of one MeV.

¹²LHC vacuum conditions require a minimal beam pipe radius of 25 mm to 30 mm.

regions. During the low luminosity phase, the barrel will be composed of two pixel layers located at a radius of 40 mm and 70 mm. Before entering the high luminosity run, a third layer will be installed at a radius of about 110 mm. Two end disks will be placed at each end of the barrel in order to complement the $|\eta|$ -coverage for two pixel hits.

The length of the pixel system with respect to the beam axis (z coordinate) is $-50 \text{ cm} \leq z \leq 50 \text{ cm}$. Figure 1.6 shows a perspective view of the CMS pixel system in the high luminosity configuration.

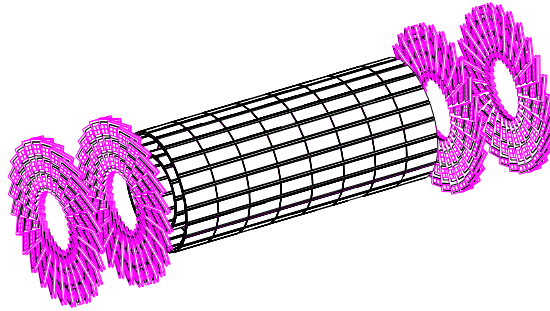


Figure 1.6: Perspective view of the CMS pixel system in the high luminosity configuration. Source: [17]

The Silicon Microstrip Tracker

Figure 1.7 illustrates the general layout of the CMS silicon microstrip tracker in r - z view. The fundamental units of the tracker are silicon strip sensors, organized in modules of different shapes and dimensions in order to match the different regions of the detector. The sensors will be either $320 \mu\text{m}$ or $500 \mu\text{m}$ thick (details about the sensor design will be presented in section 2.2.3). About 15,000 of those modules are needed to equip the complete CMS tracker resulting in 9.6 million readout channels. Since single sided microstrip detectors only give two-dimensional information about a traversing particle, some detectors are made of double sided modules which are composed of two single sided detectors tilted by an angle of 5.6° .

Similar to the pixel system, the strip tracker is divided into two main regions, the barrel and end cap. Two *tracker end caps (TEC)* will be built, each consisting of nine disks equipped with up to seven rings of wedge-shaped detector modules. The barrel region is subdivided into a *tracker outer barrel (TOB)* and a *tracker inner barrel (TIB)* part. TOB and TIB use rectangular-shaped detector modules which are mounted on six or four layers respectively. Three *tracker inner disks (TID)* each composed of three rings close the region between TIB and TEC.

The mechanical structure of a TEC disk is built of carbon fibre/honeycomb composite. Figure 1.8(a) shows a schematic of a TEC disk being composed of 16 sub-elements, called *petals*. Eight petals, called front petals, are mounted onto the front of a support wheel whereas the other eight petals, the back petals, equip the back side of the wheel. Each individual petal is made of carbon fibre/honeycomb plates carrying

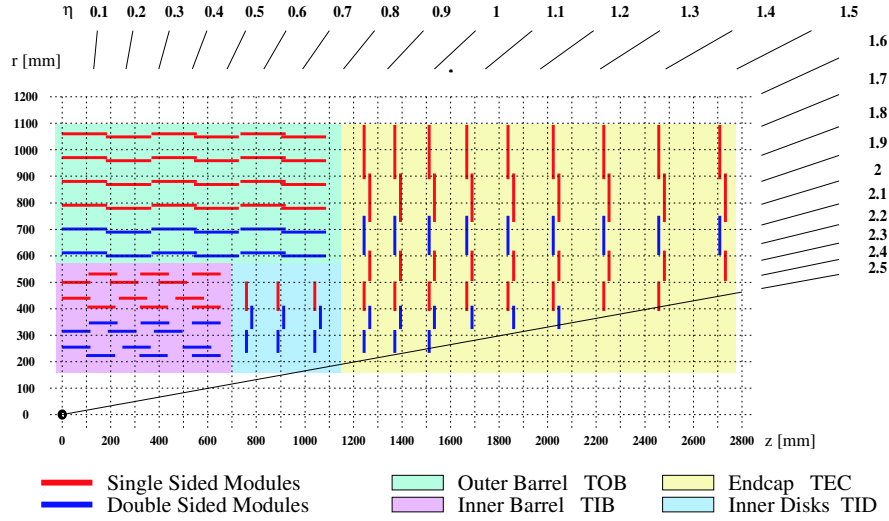


Figure 1.7: General r - z view of the CMS silicon microstrip tracker. Only a quarter of the tracker is shown. The detector can be segmented in units of $|\eta|$. Source: [26]

modules at odd ring locations on the front side and at even ring places on the back side. Figure 1.8(b) depicts the mock-up of a front petal. Rings 1, 3, 5 and 7 have to be equipped with modules which are indicated by aluminium replacements.

1.4.4 The Trigger and the Data Acquisition System

At LHC design luminosity approximately 25 inelastic collision events occur every bunch crossing corresponding to an interaction rate of the order of 1 GHz. This input rate has to be reduced by a factor of approximately 10^7 to 100 Hz.¹³ CMS has chosen to reach this reduction in two steps which are called *level 1 trigger (L1)* and *high level trigger (HLT)* [27, 28]. The L1 system is based on custom mode electronics while the HLT relies on commercial processors.

The L1 trigger involves the calorimetry and muon systems, and some correlation of information from these systems. Especially the identification of muons, electrons, photons, and jets, as well as missing transverse energy play an essential role in the L1 trigger decision. A first decision to abandon data from a particular beam crossing requires the time of about 128 bunch crossing units which is equivalent to $3.2 \mu\text{s}$. During this period, trigger data must be collected from the front end electronics and decisions must be accumulated that discard a large fraction of the data while retaining the small portion belonging to interactions of interest. Thus the readout architecture of several sub-detectors have to provide pipeline memories with a depth of the order of these 128 bunch crossings. For instance, the CMS tracking system will implement pipeline readout chips (APV pipeline: 192 bunch crossings deep, see section 3.2.1) that guarantee an almost dead time free data processing at the first trigger level.

¹³The reason for this reduction is given by the limitations of present funding resources and computing technologies.

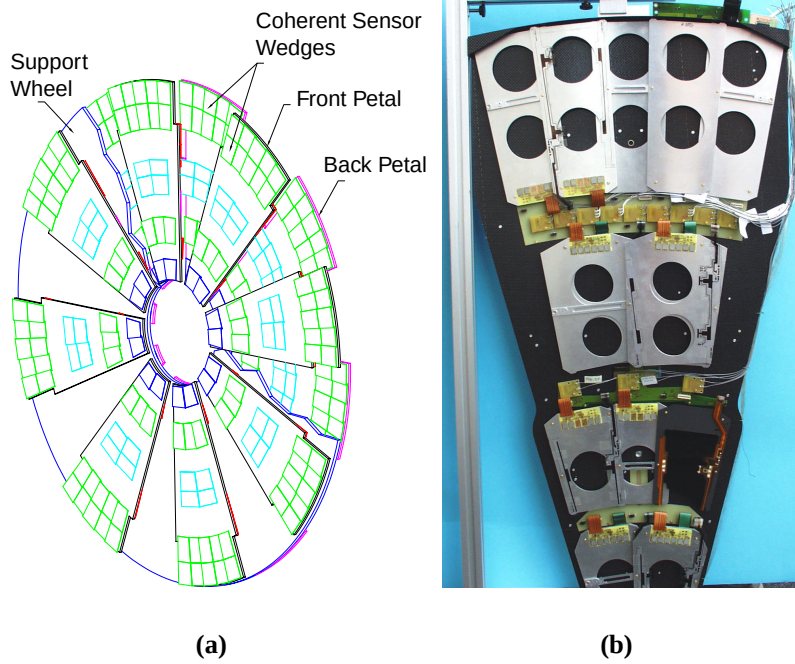


Figure 1.8: (a) Schematic of a TEC disk composed of 16 petals. (b) Mock-up of a TEC front petal. Each petal is suited to house several fundamental units, the silicon strip detector modules which are symbolized here by aluminium replacements.

The high level trigger represents a cluster of several decision stages implemented purely by software. Starting from L1 seeds and validating the L1 decision, the full granularity of the calorimeter and muon systems as well as precise tracking data will be taken into account. Last steps of the trigger processing include track reconstruction and event filtering to separate kinematically and topologically different signatures. Figure 1.9 gives a general view of the CMS trigger system. The HLT is implemented as a processor farm allowing a data input rate of 75 kHz. This rate has to be reduced to 100 Hz that will be written to a mass storage system. The high level trigger decision will take from a few ms up to 1 s.

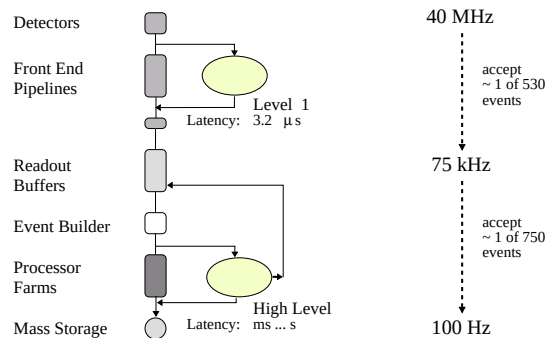


Figure 1.9: General CMS trigger architecture containing level 1 trigger and high level trigger.

Chapter 2

CMS Silicon Microstrip Sensors

In the last two decades semiconductor detectors for nuclear radiation and particles have been established in nuclear and particle physics. Josef Kemmer is one of the pioneers in the development of silicon detectors due to his adoption of production technologies used in micro-electronics to the fabrication of silicon detectors [29]. The so-called *planar technology* (see appendix B.1) has allowed to build segmented pn-junctions to design detectors for extremely precise position measurements with an accuracy of down to a few microns. In combination with new manufacturing techniques for building large area sensors, 6" wafers instead of 4" wafers, silicon detectors could evolve from a custom technology to an industrialized technology. Thus this kind of detector provides perfect properties for the use in large-scale high energy projects within high-rate environments, such as the Large Hadron Collider.

2.1 Basic Silicon Properties

Silicon (Si) is a semiconductor element belonging to the fourth group of the periodic table. It is composed of a diamond lattice type building the typical crystal structure which affects its electrical and physical properties. In a diamond lattice the atoms are arranged in a tetrahedron and each atom shares its four valence electrons with those of the neighbours, thus forming covalent bonds. At low temperatures all valence electrons remain bound, while at higher temperatures some of the covalent bonds can break up. As a result, some of the valence electrons become free and each of them leaves a hole behind. The free electrons as well as the holes participate in the conduction process.¹

Figure 2.1(a) shows a simplified band scheme of pure silicon illustrating the meaning of important energy levels: the valence band edge E_V (the highest point of the valence band), the conduction band edge E_C (the lowest point of the conduction band), the band gap $E_G = E_C - E_V$, as well as the Fermi energy E_F . In thermal equilibrium the population of these energy bands can be derived from Fermi-Dirac statistics considering the Pauli principle. Such populations are characterized by charge carrier densities given in equation 2.1. The electron density is named n whereas the hole densities are symbolized by p .

¹In the following electrons will be abbreviated by e while holes are named h .

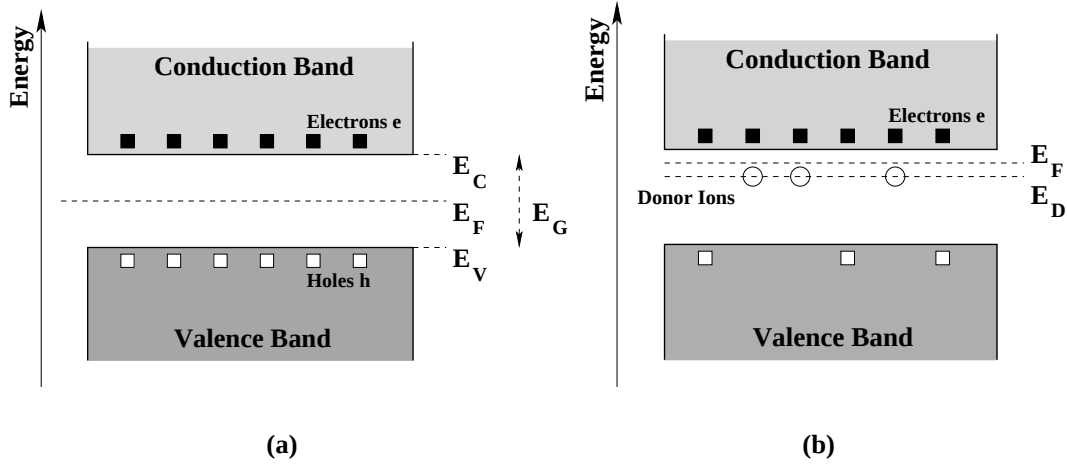


Figure 2.1: Energy band structures of (a) pure intrinsic silicon and (b) n-type extrinsic silicon.

$$n = N_C e^{-\frac{E_C - E_F}{k_B T}}, \quad p = N_V e^{-\frac{E_F - E_V}{k_B T}}, \quad (2.1)$$

where N_C and N_V are effective, temperature dependent ($\propto T^{3/2}$) densities of states at the conduction and valence band, respectively. The parameter T represents the temperature whereas $k_B = 8.617 \times 10^{-5}$ eV/K is the Boltzmann constant.

Pure silicon is an intrinsic semiconductor, since the thermally produced hole and electron densities are equal. Most semiconductor devices base their operation on the addition of a carefully controlled fraction of foreign atoms to the crystal structure. The ratio of foreign atoms and silicon atoms is typically about $1 : 10^6$. This process is known as doping of semiconductors which changes the intrinsic silicon to extrinsic silicon.

The electrical material properties will not only be affected by the type and the concentration of these foreign atoms but also by the way they are built into the material. Usually, silicon is doped with elements of the periodic table belonging either to group III such as boron (B), aluminium (Al), gallium (Ga), indium (In), and tellurium (Tl), or to group V such as nitrogen (N), phosphorus (P), arsenic (As), antimony (Sb), and bismuth (Bi). Doped silicon material is indicated as p-type or n-type, respectively.

Elements from group V have five valence electrons. Four of them interact via covalent bonds with the Si atoms while the fifth electron is weakly bound. Thus the thermal excitation at ambient temperature is sufficient to break the bond leaving a positively charged ion behind in the crystal lattice. Therefore these elements are called donors. In n-type silicon electrons are majority carriers. The energy states in n-type silicon are depicted in figure 2.1(b). Due to the doping process a new energy level, the donor energy E_D , is generated between valence band and conduction band. For phosphorus doped silicon the difference between E_C and E_D is 45.3 meV. Elements from group III are only able to contribute with three valence electrons to the covalent bond. Therefore an electron from the silicon atoms can be attached easily and create a hole. This hole may be filled by an electron from a neighbouring atom which is equivalent to a movement of the hole in the opposite direction.

Elements from group III act as acceptors and the holes represent the majority carriers in that case. Equivalent to the n-type case a new energy level is generated near the edge of the valence band, called acceptor energy E_A . The difference between E_V and E_A for gallium doped silicon is 71 meV, for instance. In both p- and n-type materials there are carriers of the other type, resulting from thermal excitation of silicon atoms. They are called minority carriers.

Regardless of the type of dopant, the concentration of electrons and holes obey a simple law of mass-action when the material is in thermal equilibrium. Thus the increase of majority carriers is accompanied by a decrease of minority carriers according to

$$n_i^2 = n \cdot p = N_C N_V e^{-\frac{E_G}{k_B T}}, \quad (2.2)$$

with n_i being the intrinsic charge density.

The material resistivity ρ plays an important role in the design of silicon detectors, since it is strongly correlated to the carrier densities n and p , as well as to the carrier mobilities μ_e and μ_h . Equation 2.3 depicts these dependencies:

$$\rho = \frac{1}{q(\mu_e n + \mu_h p)}, \quad (2.3)$$

with q being the electron charge.

Table 2.1 gives an overview of the most important physical properties of pure silicon.

Properties	Quantity
Lattice	diamond
Lattice spacing [$\text{\AA}$]	5.43
Atomic number Z	14
Atomic weight A	28.1
Density ρ_{Dens} [g/cm^3]	2.33
Dielectric constant (relative) ϵ_r	12
Intrinsic resistivity ρ (at 300 K) [$\text{k}\Omega \text{cm}$]	230
Energy gap E_G (at 300 K) [eV]	1.1
Energy gap E_G (at 0 K) [eV]	1.21
Mean energy for electron-hole creation $\bar{E}_{Gen}$ (at 300 K) [eV]	3.62
Mean energy for electron-hole creation $\bar{E}_{Gen}$ (at 77 K) [eV]	3.81
Electron mobility μ_e (at 300 K) [cm^2/Vs]	1,350
Hole mobility μ_h (at 300 K) [cm^2/Vs]	480
Radiation length [cm]	9.36
Mean excitation potential I [eV]	173
Mean energy loss dE/dx_{Mean} [$\text{eV}/\mu\text{m}$]	390

Table 2.1: Some physical properties of silicon.

Source: [30, 31]

2.1.1 Carrier Generation in Silicon

Free electron-hole pairs may be generated by lifting electrons from the valence band to the conduction band. Semiconductors such as silicon have *indirect* band gaps where the maximum valence band energy and the minimum conduction band energy do not occur at the same momentum.

In such case, an electron is not able to make a *direct* transition from the top of the valence band to the bottom of the conduction band, corresponding to $E_G = 1.1 \text{ eV}$, as this would violate conservation of momentum. Thus a two-step excitation is acquired. In contrast to the indirect transition, the direct change needs more energy which is about 3.6 eV at ambient temperature. Figure 2.2 depicts a sketch of the energy band structure of silicon.

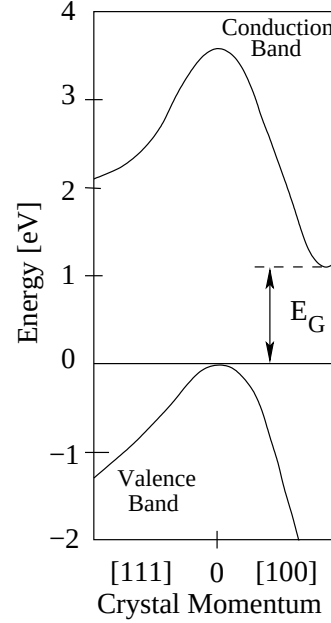


Figure 2.2: Sketch of the energy band structure of silicon.

In the next sections some typical transitions will be discussed that can be effected by various mechanisms capable of matching the necessary energy, such as *optical excitations*, *ionization by traversing charged particles*, as well as *thermal excitations*.

Generation by Electromagnetic Radiation

The behaviour of electromagnetic radiation in matter is characterised by three main effects: *Compton scattering*, *photoelectric effect* and *pair production* [30]. Equation 2.4 includes these effects and describes the absorption of electromagnetic radiation in solid materials.

$$I(x) = I_0 \cdot e^{-\alpha \cdot x}, \quad (2.4)$$

where $I(x)$ being the intensity at depth x and I_0 being the initial intensity. α represents the absorption coefficient which is correlated to the cross sections of the three effects mentioned above. In this context the *penetration depth* of photons into matter can be defined by the reciprocal value of α .

From the theoretical point of view α can be calculated considering the densities of states in the energy bands, the occupancy probabilities, as well as the transition probabilities from the initial to the final states. As silicon is an indirect semiconductor, special attention has to be paid to the two-step electron transition from the valence band into the conduction band. In this case, the incoming photon carries the acquired band gap energy while crystal phonons are in charge of the needed momentum to be transferred.

Taking these aspects into account, a simple approximation of the indirect gap absorption coefficient α can be derived as described in [32]:

$$\alpha \approx C_{ind} \cdot (h\nu - E_G)^2, \quad (2.5)$$

with C_{ind} being a material dependent factor absorbing phonon dependencies as well as temperature effects and $h\nu$ representing the photon energy. The temperature dependence of the absorption coefficient is based on the fact that the gap energy E_G changes from -20°C to $+20^\circ\text{C}$ by approximately 1% and the phonon phenomena are also affected by temperature.

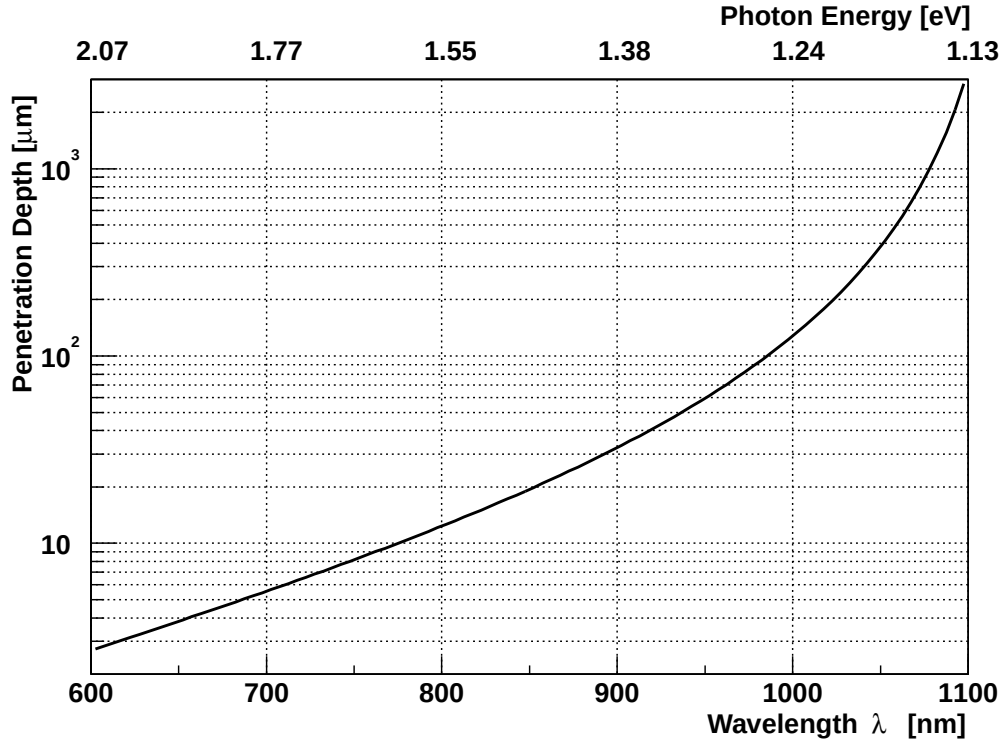


Figure 2.3: Penetration depth of photons into pure silicon at ambient temperature calculated with equation 2.5.

Figure 2.3 shows the penetration depth of photons into pure silicon at ambient temperature using a proportional factor of $C_{ind} = 4 \times 10^3 \text{ cm}^{-1} \text{ eV}^{-2}$. The penetration depth varies within three orders of magnitude considering wavelengths in the near infrared regime, that means between 600 nm and 1100 nm corresponding to a range of 2.1 eV to 1.1 eV.

Generation by Charged Particles

In the early years of the 1930's, H.A. Bethe [33] and F. Bloch [34] described the mean energy loss of charged heavy particles in matter². The basic expression known as

²Although the basic mechanism of energy loss due to collisions outlined for heavy particles is valid, the Bethe-Bloch formula have to be modified for electrons and positrons. The reasons are their small

Bethe-Bloch formula is given in equation 2.6.

$$-\frac{dE}{dx} = \kappa \rho_{Dens} \frac{Z}{A} \frac{z^2}{\beta^2} \left[\ln \left(\frac{2 m_e \gamma^2 v^2 W_{max}}{I^2} \right) - 2\beta^2 - \delta - 2\frac{C}{Z} \right], \quad (2.6)$$

with

$$\kappa = 2\pi N_0 r_e^2 m_e c^2 = 0.1535 \text{ MeVcm}^2/\text{g},$$

$$N_0 = 6.022 \times 10^{23} \text{ mol}^{-1}: \text{Avogadro's number},$$

$$r_e = 2.817 \times 10^{-13} \text{ cm}: \text{the classical electron radius},$$

$$m_e = 9.109 \times 10^{-28} \text{ g}: \text{the electron mass},$$

$$\rho_{Dens}: \text{the density of the medium},$$

$$Z: \text{the atomic number of the medium},$$

$$A: \text{the atomic weight of the medium},$$

$$z: \text{the charge of the traversing particle},$$

$$\beta = v/c: \text{the velocity of a traversing particle in units of speed of light},$$

$$\gamma = \frac{1}{\sqrt{1-\beta^2}},$$

$$I: \text{the effective ionization potential averaged over all electrons},$$

$$\delta: \text{a density correction due to polarization effects},$$

$$C: \text{a shell correction which is needed for small velocities, and}$$

$$W_{max}: \text{the maximum energy transfer in a single collision between an electron of a silicon atom and an incident particle with mass } m:$$

$$W_{max} = \frac{2 m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma \frac{m_e}{m} + \left(\frac{m_e}{m}\right)^2}.$$

Figure 2.4(a) illustrates the characteristics of the Bethe-Bloch formula for muons and protons penetrating silicon. Density and shell corrections are neglected. Important material parameters used for calculations are itemized in table 2.1. At non-relativistic energies dE/dx is dominated by the factor $1/\beta^2$ and decreases with increasing energy until a minimum is reached at about $\beta = 0.96$. Particles with energy losses near this minimum point are called *minimum ionizing particles (MIPs)*. Beyond this minimum point the term $1/\beta^2$ becomes almost constant and a slight rise of the energy loss is observed due to the logarithmic dependence in equation 2.6. In fact, this *relativistic rise* is suppressed by density and shell corrections.

masses and the indistinguishability of the interacting particles. The description can be found in [30].

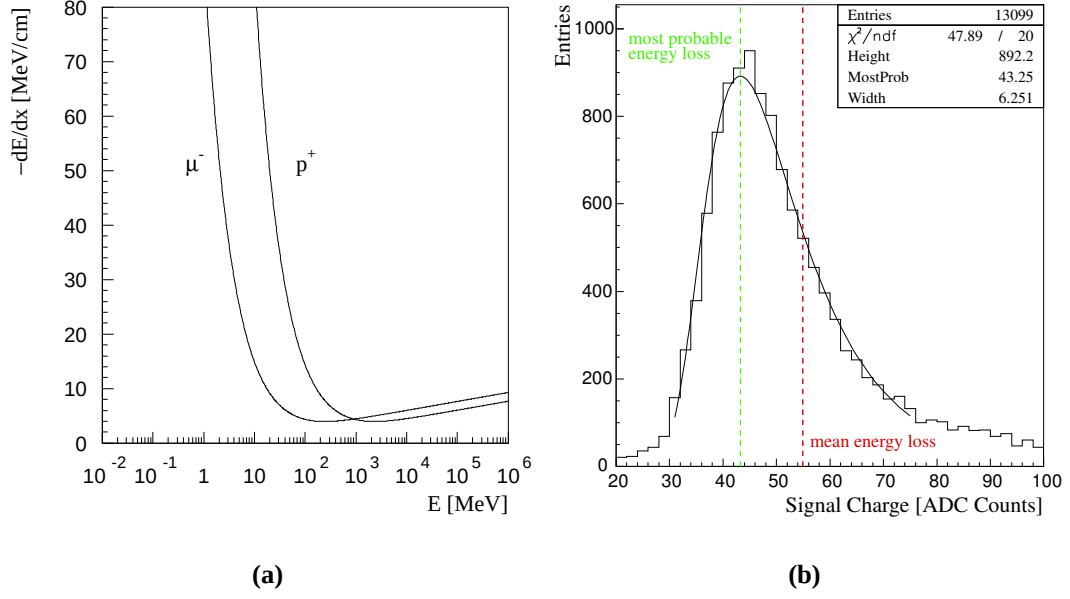


Figure 2.4: Energy loss of charged heavy particles in a 300 μm thick silicon wafer. (a) Bethe-Bloch formula calculated for muons and protons neglecting density and shell corrections. (b) Measured Landau distribution of cosmic ray muons.

The Bethe-Bloch formula describes the mean energy loss of a charged, heavy particle traversing a certain thickness of matter. In general the energy loss of a particle will not be equal to this mean value because of statistical fluctuations occurring in the number of collisions suffered and in the energy transferred in each collision. L.D. Landau [35] was the first who calculated the energy loss distribution in case of very thin absorbers. Equation 2.7 describes the *Landau distribution* $f(\lambda)$.

$$f(\lambda) = \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}(\lambda + e^{-\lambda})}, \quad (2.7)$$

where the non-dimensional, reduced energy variable λ represents the normalized deviation of the actual energy loss ΔE from the most probable energy loss $\Delta E_{MostProb}$. The parameterization of λ is expressed in equation 2.8.

$$\lambda = \frac{\Delta E - \Delta E_{MostProb}}{\xi} \quad \text{with} \quad \xi = \kappa \rho_{Dens} \frac{Z}{A} \frac{z^2}{\beta^2} l, \quad (2.8)$$

where ξ is given by the first term in the Bethe-Bloch formula 2.6 scaled by the path length l . An example for a typical Landau distribution is shown in figure 2.4(b), where a CMS silicon detector has been used to measure cosmic ray muons. It resembles a distorted normal distribution with a long tail resulting from rare, highly ionizing knock-on electrons, the δ -electrons. Due to the asymmetry, the mean energy loss is higher than the most probable energy loss.

In silicon the mean energy loss $(dE/dx)_{Mean}$ of a MIP is about 390 eV/ μm , while the mean energy $\bar{E}_{Gen}$ required to create one electron-hole pair is 3.6 eV.

Thus the number n_{e-h} of created $e-h$ pairs along a certain path length l can be approximated by equation 2.9.

$$n_{e-h} = \frac{l \, dE/dx}{\overline{E}_{Gen}}. \quad (2.9)$$

As a consequence, a traversing MIP creates about 32,500 $e-h$ pairs on average in a standard 300 μm thick silicon wafer. In practice it is more convenient to use the most probable energy loss described by the Landau distribution. The scale factor between the mean and the most probable energy loss is approximately 1.5 thus resulting in the most probable number of 22,000 $e-h$ pairs produced in a 300 μm silicon wafer. Usually the latter value is used for references or calibration purposes.

A detailed discussion of the features of the Bethe-Bloch formula and Landau's theory can be found in [30, 36].

Thermal Generation

Generally charge carriers can also be generated by thermal excitation due to the small energy gap between valence and conduction bands which is in the order of a few eV. As mentioned above, the energy required to create an $e-h$ pair in silicon is about three times larger than the band gap E_G thus suppressing the direct thermal excitation. The thermal energy at ambient temperature $T = 300 \text{ K}$ is given by

$$E_T = k_B \cdot T \approx 0.0245 \text{ eV}. \quad (2.10)$$

A comparison of this thermal energy with the mean energy required for direct band-to-band transitions $\overline{E}_{Gen} = 3.6 \text{ eV}$ demonstrates that the thermal excitation primary occurs in two steps through intermediate local states built by imperfections of the crystal or impurities. As a result, non-irradiated silicon detectors can be operated reliably at ambient temperature. Nevertheless, thermal charge carrier generation usually has a detrimental effect in a silicon detector, because it is an additional noise source superimposed to the signals.

2.1.2 Advantages of Silicon

Compared with non-semiconductor materials, silicon has unique properties with respect to its application in high energy physics that makes it suitable for the detection of ionizing particles or radiation. Some of the most important reasons for using silicon in modern high energy physics experiments are listed below:

- The small band gap E_G leads to a large number of charge carriers per unit energy loss of the ionizing particles to be detected. The average energy $\overline{E}_{Gen}$ for creating an $e-h$ pair is one order of magnitude smaller than the ionization energy in gases, for instance.
- The high density ρ_{Dens} leads to a large energy loss per traversed length of the ionizing particle thus allowing to build thin detectors that produce measurable signals.

- Electrons and holes move almost free in the silicon. Because of their mobilities μ_e and μ_h , charge can be collected rapidly, in the order of 20 ns, which is essential in high-rate environments, such as the LHC with its bunch crossing time of 25 ns.
- The mechanical rigidity allows the construction of self-supporting structures.
- Detectors and readout electronics can both be built out of silicon. Thus their integration in one device is possible.
- Large area silicon sensors can be produced in industrialized procedures. Thus a large-scale sensor production can be envisaged.

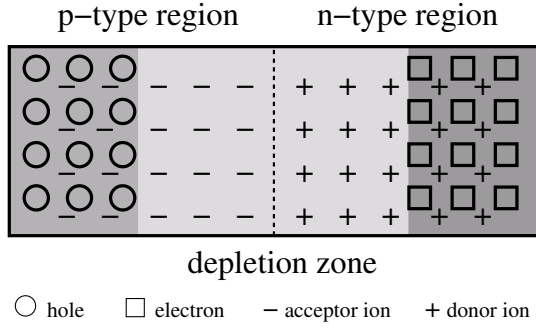
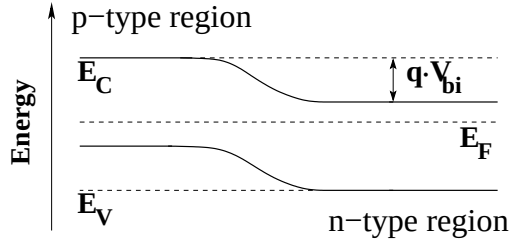
2.2 The CMS Silicon Sensor Technology

In pure silicon the intrinsic carrier density (equation 2.2) is $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$ at ambient temperature. Thus a volume of about 0.03 cm^3 of silicon would lead to 4.5×10^8 free carriers which is four orders of magnitude higher than the mean number of charge carriers created by a traversing MIP. In doped silicon the ratio is even worse, since there are additional electrons and holes from ionized donors or acceptors. Cooling is a proper strategy to lower the number of free carriers. An other way to make silicon suitable for particle detection is to deplete the silicon of free carriers through a *reverse biased pn-junction*. This method will be discussed in the following section.

2.2.1 The Reverse Biased pn-Junction

The functionality of semiconductor devices depends on the formation of a semiconductor junction. A so-called *pn-junction* is created when a single semiconductor crystal is doped with acceptors on one side and donors on the other side. For simplifying purposes a planar step junction is often used to illustrate basic processes being involved in pn-physics (see figure 2.5).

The formation of a pn-junction creates a region with important physical characteristics across the interface between the two different doped regions, the *depletion zone*. Because of the initial gradient in the electron and hole concentrations, there is a diffusion of holes towards the n-type region and a migration of electrons towards the opposite, the p-type side. As a consequence, the diffusing electrons combine with holes in the p-region while the holes capture electrons on the n-side. This recombination of e and h causes a charge constitution on either side of the junction. Since the p-type zone is injected with additional electrons this region becomes negatively charged and vice versa. Thus an electrical field gradient across the junction is created until a stationary state is reached which halts the diffusion process leaving a region of immobile space charge, the depletion zone. Due to the electric field a potential difference is present across the pn-junction, called *built-in potential* V_{bi} , which is usually in the order of a hundred mV.

**Figure 2.5:** Planar step pn-junction.**Figure 2.6:** Typical energy band structure describing a planar step pn-junction.

The energy band structure is thus deformed and the Fermi energy levels of both types line up leading to the band structure scheme as shown in figure 2.6.

The impact of the depletion zone on high energy physics detectors is given by the special property of being devoid of all mobile charge carriers. Any electron or hole created, or traversing this zone will be affected by the electric field and can be detected as a signal on either end of the junction if electrical contacts are installed there. In general, the intrinsic electrical field is not able to provide efficient charge collection. Better results can be obtained by applying an additional external *reverse bias voltage* V_{bias} to the junction, such that V_{bias} and V_{bi} are of the same sign. This enlarges the depletion zone and thus the sensitivity volume for particle and radiation detection. Moreover, the higher external voltage will provide a more efficient charge collection.

An important quantity of a reverse biased pn-junction represents the width w of the depletion zone given by equation 2.11.

$$w \approx \sqrt{\frac{2 \epsilon V_{bias}}{q |N_{eff}|}}, \quad (2.11)$$

where ϵ is the dielectric constant and N_{eff} is the effective impurity density depending on the donor density N_D and the acceptor density N_A as depicted in equation 2.12.

$$N_{eff} = N_D - N_A. \quad (2.12)$$

Equation 2.11 is deduced in appendix B.2 based on assumptions constrained by CMS demands, e.g. $N_D \gg N_A$ and $V_{bias} \gg V_{bi}$. It is evident that the depletion region increases with the applied bias voltage until all free carriers are removed from the complete silicon volume. The depletion depth can also be expressed in terms of the material resistivity ρ and the carrier mobility μ using equation 2.3.

$$w \approx \sqrt{2 \epsilon \rho \mu V_{bias}}. \quad (2.13)$$

This formula accentuates the impact of resistivity with regard to the CMS detector design. High resistivity material leads to a low bias voltage when keeping the depletion

depth constant. Since each semiconductor device is limited in its geometrical dimensions, the bias voltage V_{depl} needed to deplete the whole material with thickness w_{max} is given by

$$V_{depl} = \frac{q |N_{eff}| w_{max}^2}{2 \epsilon} = \frac{w_{max}^2}{2 \epsilon \rho \mu}. \quad (2.14)$$

A detector is called *over-depleted*, if it is biased with a voltage V_{bias} larger than V_{depl} . The maximum voltage which can be applied is limited by the resistance of the semiconductor. *Electrical breakdown* occurs when the electrical field is high enough to initiate avalanche multiplication³, for instance. In fact, the electrical field will depend on temperature, on specific geometrical layout, and on inhomogenities in the material such as doping density variations and crystal defects.

Although a reverse biased junction is ideally nonconducting, a small current, the *leakage current*, exists when an external voltage is applied. This current appears as noise in the detector (see section 4.3) and limits the smallest signal pulse height which can be observed. This current has several sources of which the thermally generated current is quite dominant. If the depletion zone is in equilibrium condition, $e-h$ pairs are thermally generated within the depleted volume. Due to the external electric field these charge carriers drift towards the corresponding electrodes giving rise to a generation current. The contribution of the generation current to the leakage current can be described in terms of the current density j_{gen} :

$$j_{gen} = \frac{1}{2} q \frac{n_i}{\tau_0} w, \quad (2.15)$$

where τ_0 is the lifetime of the minority carriers in the depletion zone with its depth w . The lifetime is inversely proportional to the density of impurities whereas w is proportional to $\sqrt{V_{bias}}$ as shown in equation 2.11. Due to the intrinsic charge carrier density n_i the leakage current depends strongly on temperature [37]:

$$I_{leak} \propto T^2 e^{-\frac{E_G}{2k_B T}}. \quad (2.16)$$

Reducing the temperature from ambient temperature to 0 °C decreases the leakage current to about a factor of 1/6 of its original value, for example. Thus the reliable operation of a semiconductor detector requires a constant temperature.

2.2.2 Radiation Damage in Silicon Sensors

The CMS silicon detector design is mainly constrained by the severe LHC radiation environment. Intense radiation may change the semiconductor material significantly thus changing some properties of the material [38]. Basically, semiconductors are affected by two radiation damage mechanisms:

- *displacement damage*: incident radiation displaces silicon atoms from their lattice sites. The resulting defects alter the electronic characteristics of the crystal.

³An avalanche multiplication occurs, if the electron-hole pairs generated due to impact ionization cause other impact ionization events thus increasing the number of charge carriers.

- *ionization damage*: energy absorbed by ionization in insulating layers, such as SiO_2 , liberates charge carriers which drift to locations where they are trapped and cause parasitic fields.

Since the properties of a large depletion zone of a semiconductor detector is determined primarily by its bulk⁴ properties, displacement damage plays the most important role. Three effects show up under strong radiation influence: The doping concentration changes, the leakage current increases, and the charge collection efficiency decreases.

The change in doping densities affects the effective impurity density N_{eff} and thus the depth of the depletion zone or the depletion voltage indicated by equation 2.14. The effective doping concentration and the corresponding depletion voltage versus 1-MeV-equivalent neutron per cm^2 fluence for several initial resistivities is depicted in figure 2.7. Obviously, the effective doping of n-type silicon initially decreases, becomes intrinsic⁵ at the *inversion point*, the minimum of the curve, and then turns p-like. The fluence Φ_{eq} required for inversion depends on the initial doping concentration defined by the resistivity of the silicon. Due to equation 2.14 high resistivity sensors have a low initial density thus reaching the inversion point with less fluence than those with low resistivity. Moreover, figure 2.7 shows that at a fluence of about 2×10^{14} particles per cm^2 , which is equivalent to ten years of LHC operation, 300 μm thick silicon detectors have to be depleted with a few hundred volts. This demands a detector technology being able to cope with bias voltages of a few hundred volts.

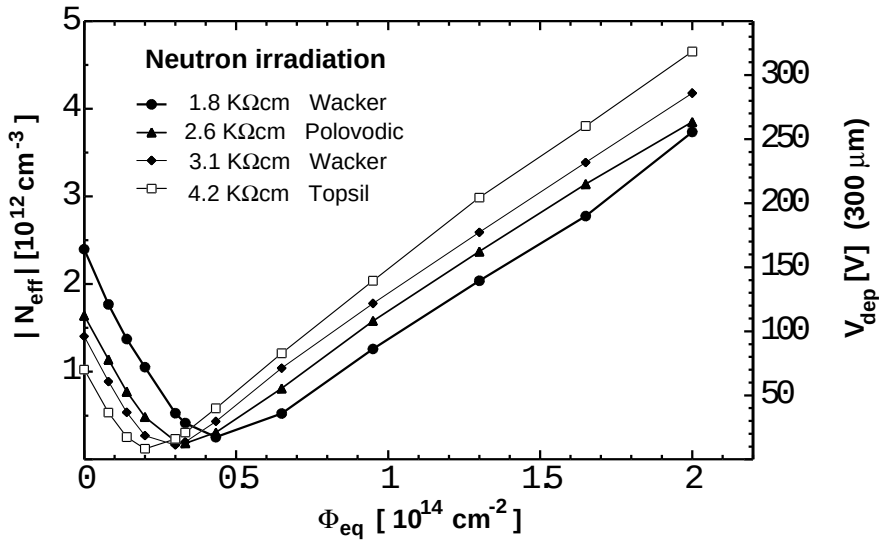


Figure 2.7: Effective doping concentration versus 1-MeV-equivalent neutrons per cm^2 fluence. The innermost layer of the CMS tracker has to deal with a total fluence of $\Phi_{tot} = 2 \times 10^{14}$ particles per cm^2 during the scheduled ten years of LHC.

Source: [39]

⁴The bulk builds the main body of a detector.

⁵This means that N_A and N_D are almost equal.

The increase of the leakage current caused by radiation damage is related to the creation of energy states within the silicon band gap. This facilitates the transition of electrons from the valence band to the conduction band thus leading to an additional generation current in the depletion zone. After irradiation the leakage current can be parameterized by equation 2.17.

$$I_{leak,rad} = I_{leak} + \alpha \Phi V, \quad (2.17)$$

where I_{leak} is the leakage current before irradiation, α is a damage coefficient, Φ is the particle fluence and V represents the detector volume. Both terms show the same strong exponential temperature dependence as indicated in equation 2.16. After irradiation the leakage current initially decreases with time. This beneficial process is called *annealing*. Unfortunately it is only a short-term effect followed by a deterioration effect called *reverse annealing*. Both processes counteract with respect to the leakage current resulting in a value which is significantly above the initial state. Due to their temperature dependence it is possible to detain the processes and keep the leakage current constant after irradiation. An environment temperature of about -10°C provides the most beneficial effect. Moreover, a powerful method to prevent a semiconductor detector from high leakage current is segmentation. For a given damage level the detector leakage current per signal channel can be reduced significantly by any kind of segmentation.

Displacement damage also causes defects in the bulk material which act as charge traps and recombination centers. As a result, charge is captured and released after a certain time. Thus the charge carrier lifetime is decreased and the charge collection efficiency is reduced. This process can be restored partially by slightly over-biasing the detector.

The basic silicon detector is insensitive to ionization effects, but this is not the case for the peripheral structures, such as insulating layers, for instance.

2.2.3 The CMS Silicon Microstrip Sensor Design

The reliable operation of silicon detectors in the LHC radiation environment depends strongly on the sensor design as well as on suitable material choices. Figure 2.8 shows a schematic view of the CMS silicon sensor design which is a result of considerable research and development efforts in close collaboration with industry.

The bulk of the CMS silicon sensors is built of n-type silicon. Heavily doped p^+ implants⁶ are processed in strips into the surface of one sensor side, the *junction side*, thus providing one dimensional information about traversing particles. The distance between two neighbouring strips is called *strip pitch* P while their width is referred to as *implant width* W . In the rectangular sensors for TOB and TIB the strip pitch is kept constant whereas in wedge-shaped sensors the strip distance changes from one end of the sensor to the opposite end. This is also true for the implant widths.

The opposite wafer side, the *ohmic side* or *backplane*, is coated with an unstructured n^+ implant. This ensures good ohmic contact to the metal electrode (aluminium

⁶To distinguish heavily doped semiconductors from normally doped materials (ratio of $\approx 100 : 1$), usually a “+” sign after the material type is used.

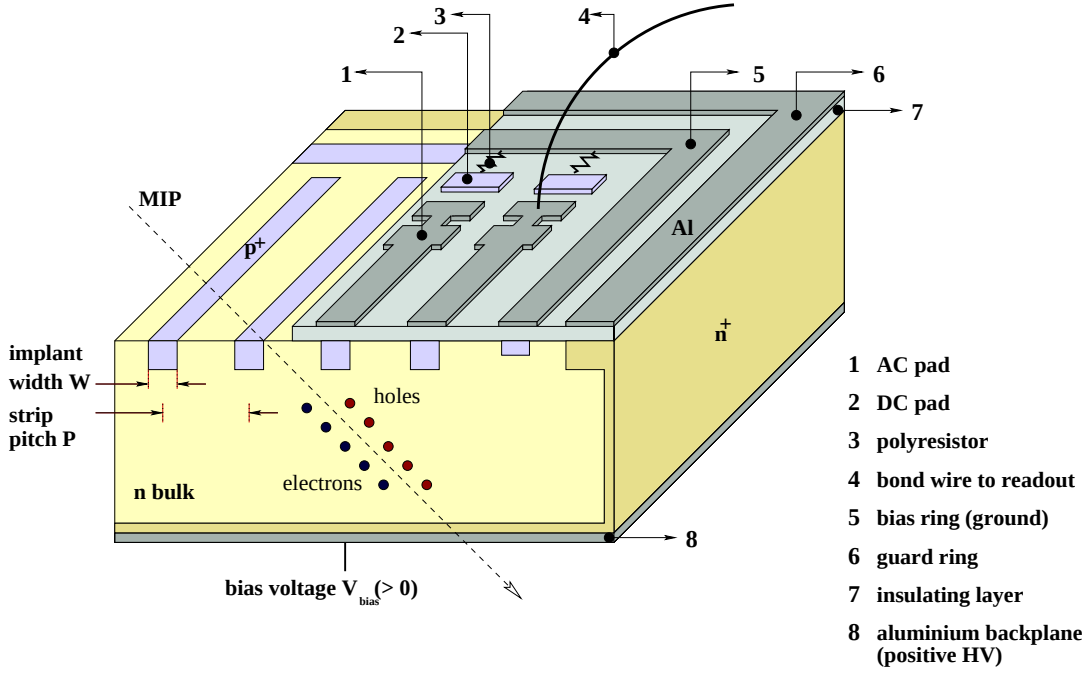


Figure 2.8: Schematic structure of a CMS silicon microstrip sensor.

backplane) and prevents the bulk from minority carriers being injected. Moreover, the n^+ implant is required over the entire cutting area of the junction side to avoid edge effects.

The biasing scheme of a silicon detector plays an important role and affects the design of the sensors. In the CMS layout, sensor integrated polysilicon bias resistors (*polyresistors*) will connect each strip via a metallized probe pad, called *DC pad*, to the grounded *bias ring* which borders the complete sensor thus providing all strips with the same potential. Realistic values for leakage currents and bias resistors (512 strips, $I_{leak} = 1 \mu A$, $R_{poly} = 1.5 M\Omega$) lead to a voltage drop across the polyresistors of the order of a few mV which is negligible with respect to the operation bias voltage.

A floating *guard ring* surrounds the strips and the bias ring to gradually degrade the electric field within the sensitive area, and to minimize edge effects. This improves the breakdown performance of the sensors. The p^+ implants are covered with multiple thin insulating layers of SiO_2 and Si_3N_4 on which aluminium strips are deposited parallel to the implants. The aluminium strips have a slight metal overhang with respect to the implants (about 15% at each side) to enhance the sensor breakdown behaviour.

The CMS sensor design provides so-called *AC coupling* as the DC leakage current is bypassed over the polyresistors while the AC part can be picked up over the capacitor built by the metal-oxide-semiconductor interface. Each strip has to be connected to its own readout channel and amplifier. This connection is made with a $25 \mu m$ thin wire welded onto the corresponding *AC pad* using an ultrasonic bonding wedge. Two rows of AC pads are used at the ends of the strips on each side of the detector thus

allowing for bonding and for testing. Examples of how the different sensor structures are arranged in the active region are shown in the figures B.3(a) to B.3(c).

Sensor Specifications

The baseline requirements for the CMS silicon strip tracker are described in [40, 41] and include the following basic properties to be accomplished by two sensor manufacturers, Hamamatsu Photonics [42] and ST Microelectronics [43]:

- bulk material: n-type silicon (phosphorus doped), float zone,
- crystal orientation: $\langle 100 \rangle$,
- sensor thickness:
 - $w_{max,thin} = 320 \pm 20 \mu\text{m}$, called *thin detectors* (produced by Hamamatsu),
 - $w_{max,thick} = 500 \pm 20 \mu\text{m}$, called *thick detectors* (produced by ST),
- material resistivity:
 - $\rho_{thin} = 1.5 - 3.25 \text{ k}\Omega \text{ cm}$ (thin detectors),
 - $\rho_{thick} = 4 - 8 \text{ k}\Omega \text{ cm}$ (thick detectors),
- strip pitch: $P = 80 - 205 \mu\text{m}$, depending on the sensor location in the tracker,
- resistivity between strip and bias line implants: $R_{poly} = 1.5 \pm 0.5 \text{ M}\Omega$,
- line resistivity of a strip: $R_S = 50 \Omega$,
- sensor surface: junction side polished and back side acid etched,
- sensor design: 15 different lay-outs based on 6'' planar wafer technology,
- number of sensors to be produced: 24,244 single sided sensors.

The electrical representation of a strip is a capacitive current source composed of the backplane capacitance and the interstrip capacitance with respect to neighbouring strips. The total strip capacitance C_{strip} depends on two geometrical sensor characteristics, the implant width W and the strip pitch P . An empirical equation is deduced in [18] and given by equation 2.18.

$$C_{strip} = \left(0.8 + 1.7 \frac{W}{P} \right) \text{ pF/cm.} \quad (2.18)$$

The relation of strip width and pitch will be kept constant at $W/P \approx 0.25$. This value is a compromise between low total strip capacitance C_{strip} and stable detector operation at high voltage.

Chapter 3

Module Readout Electronics

The front end electronics located nearest to the silicon sensors, the front end (FE) hybrid, plays an essential role in the readout chain of the CMS tracker acting as an interface between the sensors and the counting room. This means that the hybrid has to provide a bi-directional information flow. Measured data has to be transmitted to the counting room after receiving a level 1 trigger, for instance. An FE hybrid carries the readout and control chip circuits, the ASICs¹, and provides these chips with the required environment. This includes the needed chip bias voltages of +2.5 V (V250 line), +1.25 V (V125 line) and 0 V (VSS line). The following list itemizes the different types of chips mounted on the hybrids:

- **APV** – Analogue Pipeline – Voltage Mode [44]
- **APVMUX** – APV Multiplexer [45]
- **TPLL** – Tracker Phase-Locked Loop [46]
- **DCU** – Detector Control Unit [47]

In general the body of each hybrid is based on a high-density 4-metal layer board, the substrate, suited with SMD² components, and a polyimide cable providing all electrical connections except for the analogue inputs. The actual baseline layout of a TEC FE hybrid with its chip equipment is presented in figures 3.1(a) and 3.1(b).

Since each silicon module needs its own readout electronics, more than 15,000 FE hybrids have to be built and integrated in the tracker.

3.1 Layout of the Front End Hybrid

The FE hybrids have been designed and developed by a team of two laboratories in Strasbourg³. Evolving a functional FE hybrid suited for LHC requirements a lot of aspects have to be considered affecting the geometrical layout as well as the material choices, such as substrate or glue.

¹Application Specific Integrated Circuits.

²Surface Mounted Devices, e.g. resistors and capacitors, ICs, transistors, etc.

³Institut de Recherches Subatomiques IReS/CNRS.

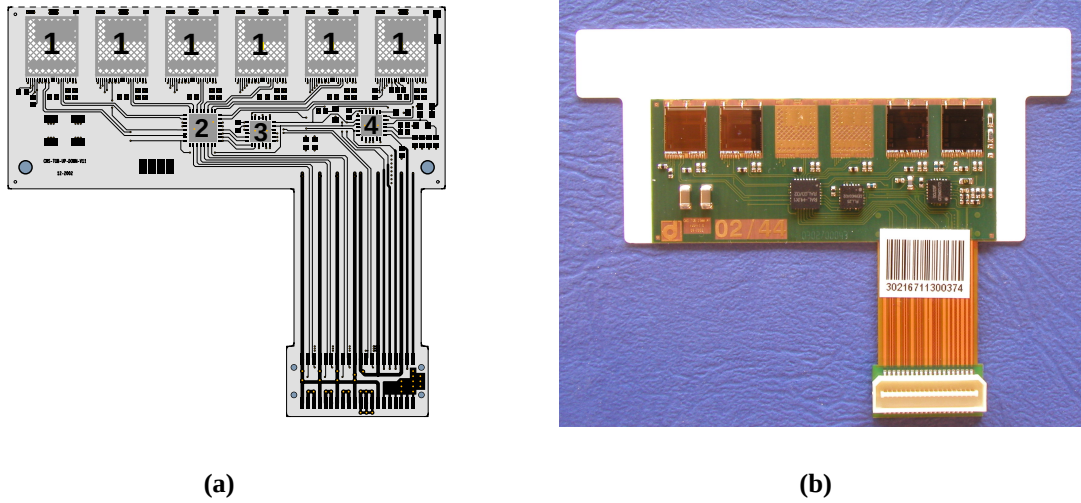


Figure 3.1: TEC hybrid layout, version 2002. (a) Hybrid schematic. The locations of the readout and control chips used are numbered as follows: 1 – APV, 2 – APVMUX, 3 – TPLL and 4 – DCU. (b) The Kapton (polyimide) substrate is laminated to a ceramic plate (white).

Essential aspects to be reviewed are radiation hardness and radiation length of the hybrids. According to automated assembly requirements, sufficient flatness and rigidity are demanded. Since the tracker will be operated at $-10\text{ }^{\circ}\text{C}$, thermal properties, such as thermo-mechanical compatibility of the chosen materials (carbon fibre, graphite, ceramic etc.) and thermal conductivity⁴, have to be considered.

Moreover, a complete industrial production is scheduled due to the enormous number of hybrids to be built. The procedure of manufacturing the hybrids includes not only the substrate production itself but also the loading with SMD components, connectors, chips, and the bonding process thus limiting the number of companies being prepared to match these requirements.

Material Choices

During the research and development phase of about three years the main focus changed from radiation length aspects towards high yield mass production facets. Thus several production technologies of FE hybrids have been developed and are still in the scope of evaluation. Some of these technologies are listed below:

- thick-film technology on ceramic substrate,
- pure FR-4⁵ circuits,
- flex-rigid FR-4 technology, and
- full-flex polyimide circuits on rigidifiers such as ceramic plates.

⁴The ASIC chips dissipate up to 3 W electrical power.

⁵FR-4 is a general grade laminate made of woven fibreglass fabric saturated with an epoxy resin [48].

Each technology has its specific merits and drawbacks concerning thermal conductivity λ and expansion CTE ⁶ as well as radiation length X_0 as shown in table 3.1. As a consequence, the mechanical processing in terms of soldering, bonding or gluing is affected strongly by the chosen technology.

Material	CTE [ppm/°C]	λ [W/mK]	X_0 [mm]
Al ₂ O ₃ (ceramic)	7.0	24.0	75.5
FR-4	12–16	0.2 – 0.3	194.0
carbon fibre	< 1.0	200 – 400 1.0 $\perp$	250.0
graphite E779	7.4	65.0	188.0
polyimide (Kapton)	45.0	0.2	286.0
Cu	17.0	390.0	14.3
Au	14.0	318.0	3.35

Table 3.1: Material parameters being relevant for hybrid technology. || means in fibre direction and $\perp$ perpendicular to the fibre direction. Source: [49]

The first hybrid prototypes were built in thick-film technology on a ceramic substrate (Al₂O₃). Ceramic is well suited to transfer the produced heat and it favours graphite as frame material for the silicon sensors. This is indicated by table 3.1. But with respect to industry mass production the layout was not suited for a large scale assembly. Especially the fact that the TPLL and APVMUX chips were merged in a single large die with very small pitch constrained the limit of that technology extremely. Moreover, all hybrid ASIC chips were naked which means that each electrical connection of the chips had to be bonded during the hybrid production. Thus the number of companies being able to assemble such hybrids decreased whereas the price increased significantly. Only Dorazil [50] and MIPOT [51] produced in total 180 of these ceramic FE hybrids so far.

Apart from the aspect of large scale production, ceramic hybrids played an essential role in the development of the diagnostic testing system as discussed later in chapter 5. Besides that, the first TEC wedge-ring-6 detector modules were built with ceramic hybrids (see chapter 7).

Since the end of 2001 the TPLL and APVMUX chips are individual dies LPCC⁷ packaged. The DCU has also been realized in LPPC package format leading to a larger pitch. Therefore additional advanced hybrid technologies could be envisaged. At present a full-flex polyimide circuit on a ceramic carrier seems to meet all specifications and is chosen to be the baseline technique for the mass production.

Geometrical Layout

Different kinds of hybrid geometries are required due to the modularity of the tracker. The inner parts of the detector (TIB and TID) demand a very high-density layout caused by spacial restrictions whereas TEC and TOB allow for the usage of larger

⁶Coefficient of Thermal Expansion.

⁷Leadless Plastic Chip Carrier.

hybrid substrates. Also the hybrid polyimide cables and connectors are affected according to their location within the tracker in terms of length and design. TIB hybrids use a split cable ending with one 30 pin NAIS [52] and one 20 pin SAMTEC connector [53] while TOB or TEC hybrids communicate via one 40 pin NAIS connector, for instance. Figures C.1 and C.2 depict some photos of different types and technologies of FE hybrids produced so far.

	TIB / TID		TOB		TEC	
Detector	single	double	single	double	single	double
6 APVs	1056	1056	1680	–	1152	1152
4 APVs	1428	–	2448	1080	4096	–
Total	2484	1056	4128	1080	5248	1152
	3540		5108		6400	
	15048					

Table 3.2: Different types of FE hybrids in the complete tracker. Each module is read out by either four or six APV chips. Source: [49]

Table 3.2 gives an overview of the different required hybrid geometries. In the design of single sided and double sided silicon detectors hybrids with identical substrate but with turned connectors are planned to reduce the number of different production masks. Each hybrid substrate is suited to house up to six APV chips. Thus a hybrid which is equipped with only four APV chips has two vacant positions, as shown in figure 3.1(b).

3.2 Components of the Front End Hybrid

The CMS tracker FE electronics uses a simple bi-directional 2-wire bus developed by Philips for efficient integrated circuit control [54]. This bus is called *Inter Integrated Circuit (I²C) bus*. Bus compatible devices incorporate an on-chip interface which allows them to communicate directly with the outer world via this serial bus. Simple master-slave relationships are used and each device connected to the I²C bus is software addressable by a unique 7-bit address. Appendix C.2 presents the most important I²C bus specifications. In the following sections the different FE hybrid components and some of their features are described.

3.2.1 The APV 25 Chip

The APV is a complex analogue pipeline ASIC developed to amplify and store signals from 128 channels of a silicon strip sensor in a 192 column deep memory with a sample rate matching the LHC bunch crossing time. Moreover, the chip contains special features required for the use in CMS including a programmable bias generator, an internal test pulse generation system and a slow control communication interface. The latter component allows to access chip configurations, bias settings, and error states via programmable command registers using the I²C interface.

The current (and final) version of the APV chip is called *APV 25-S1* and is fabricated in commercial 0.25 μm deep-submicron CMOS⁸ technology. The chip dimensions are 7.1 $\times$ 8.1 mm with an input channel pitch of 44 μm . A detailed description of the APV 25 design features is given in [44].

Communication with the APV

Within the I²C framework the APV chip may only act as a slave device and is addressed using the standard 7-bit mode where the two leading bits are “01” (“0” is called *most significant bit*). The remaining five bits are defined by bonding the corresponding address pads of the chip. The address “1111” is reserved for global addressing (*broadcast address*) where all connected APVs will respond. To determine the communication direction, which means *write* or *read* operations, an additional bit is appended representing the least significant bit. If this bit is set to “1”, a read operation is signaled whereas a “0” defines a write access.⁹

After addressing a specific chip, a command register must be programmed before data may be transferred. This 8-bit command determines which of the provided chip registers is to be accessed. Table 3.3 lists all available registers with their specific functionality and programmable ranges. These registers are both read- and writable.

Name	Value Range	Description
IPRE	$n \times 4 \mu\text{A}$	preamp input FET ¹⁰ current bias
IPCASC	$n \times 1 \mu\text{A}$	preamp cascode current bias
IPSF	$n \times 1 \mu\text{A}$	preamp source follower current bias
ISHA	$n \times 1 \mu\text{A}$	shaper input FET current bias
ISSF	$n \times 1 \mu\text{A}$	shaper source follower current bias
IPSP	$n \times 1 \mu\text{A}$	APSP current bias
IMUXIN	$n \times 1 \mu\text{A}$	multiplexer input current bias
ICAL	$n \times 625 \text{ electrons}$	calibrate edge generator current bias
VFP	$-1.25 \text{ V} + (7.5 \text{ mV} \times n)$	preamp feedback voltage bias
VFS	$-1.25 \text{ V} + (7.5 \text{ mV} \times n)$	shaper feedback voltage bias
VPSP	$+1.25 \text{ V} - (7.5 \text{ mV} \times n)$	APSP voltage level adjust
CDRV	channel 0-7	calibrate output mask
CSEL	$3.125 \text{ ns} \times m$	calibrate delay select
MODE	see table 3.4	mode of chip operation
LATENCY	$k \times 24 \text{ ns}$	write-trigger pointer delay
MUXGAIN	resistor 1-8	gain of multiplexer

Table 3.3: Command bias registers of the APV 25 (with $n = 0, \dots, 255$, $m = 0, \dots, 7$, and $k = 1, \dots, 192$). Source: [44]

⁸Complementary Metal-Oxide-Semiconductor.

⁹In the following, the presented I²C addresses always include the write condition bit. Typically the addresses are given as hexadecimal number indicated by a leading “0x”. Thus the broadcast address is 0x7E (= 01111110 in binary format), for instance.

¹⁰Field Effect Transistor.

The MODE register plays an essential role in the APV operation. As shown in table 3.4, important conditions can be selected via this register, such as *deconvolution*¹¹ or *peak mode*, *inverter on/off* or *3-sample/1-sample mode* (see the following sub-sections for detailed explanations). The analogue bias control allows the chip bias to be disabled while the registers are programmed. Enabling this control lets the programmed values become operative.

Bit	Function	Value=0	Value=1
0	analogue bias	off	on
1	trigger mode	3-sample	1-sample
2	calibration inhibit	off	on
3	readout mode	deconvolution	peak
4	readout frequency	20 MHz	40 MHz
5	preamplifier polarity	non-inverting	inverting
6	not used		
7	not used		

Table 3.4: Definition of the mode register.

Source: [44]

Data Output Format

The form of the data output is a differential current within the range of ± 4 mA. The output is cycled with 20 MHz but can be switched to 40 MHz via the MODE register. When there is no data to be read out, it is at logic low level with synchronization pulses, the *tick marks*, which show up every 70 system clock cycles or 35 cycles, respectively. After receiving a trigger which is defined as a single pulse on the trigger line (see section 3.2.2), 70 or 35 clock cycles are required for internal data processing. Then the data set, also called *frame*, is sent to the output until the start of the next clock cycle. Figure 3.2 depicts such a frame made up of four parts: a digital header, a digital address, an error bit and an analogue data set composed of measured signals of 128 channels.

The 3-bit header represents the start of a new data set and should always be at high level. The next 8-bit number defines the memory address from which the following analogue data sample has been read. A special kind of *Gray Code* which is given in appendix C.3 is used to encode this address. All APV chips housed on the same FE hybrid run with the same trigger and clock lines. Thus these chips ought to run synchronously with respect to the pipeline address. The single error bit is used to monitor *FIFO*¹² errors and *LATENCY errors*. Both failures will be explained in the next paragraph. As long as no error occurs, the bit stays at logic high level. When sensing an error in the APV logic, the specification of the error is defined in the 8-bit (read only) ERROR register. A reset can be applied to the APV to clear the error flag.

After the digital data part the analogue data set is sent in interleaved order. A tick mark follows immediately after the APV frame, if no second trigger is pending directly

¹¹In figures the deconvolution mode will be abbreviated with “dec”.

¹²First In, First Out.

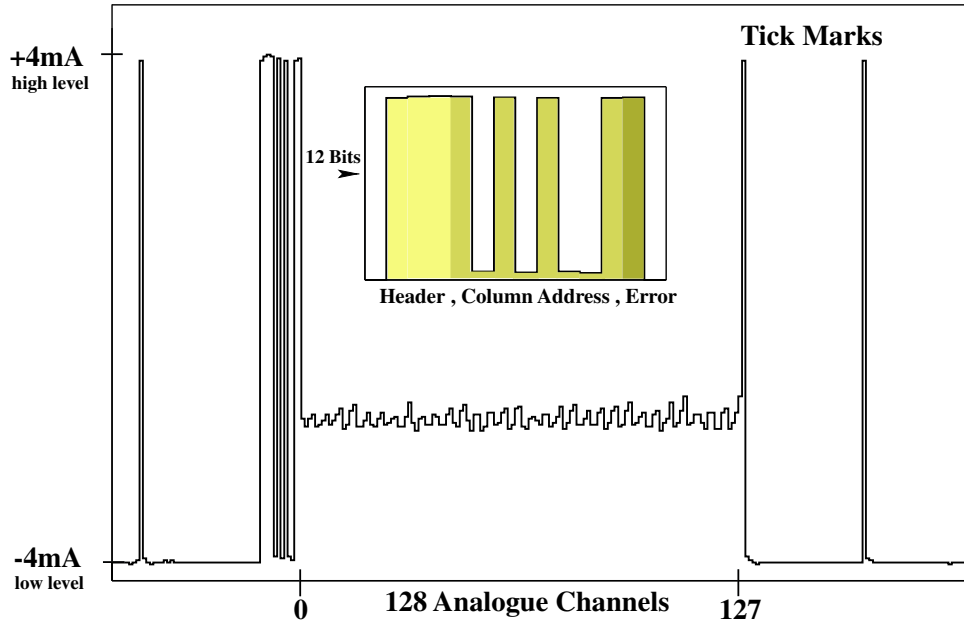


Figure 3.2: APV 25 data output format in the 1-sample mode.

or the APV is not operated in the 3-sample mode. In the 3-sample mode the first data frame is followed by two other frames with no tick marks between.

A reset sequence, called *RESET 101*, clears any pipeline pointers (see next paragraph) and adapts them with the programmed latency separation. This is done by sending two pulses separated by a gap of one clock cycle (“101”). The initialization of the pointers results in a waiting time of 11 clock cycles plus the determined latency clock cycles after a reset. During this time no trigger should be sent.

APV 25 Architecture

A schematic of the APV 25 functionality is shown in figure 3.3. Each APV input channel contains a preamplifier, a switchable unity gain inverter to permit signals of either polarity and a shaping amplifier (shaper). The shaper output of each channel is sampled with 40 MHz into the 192 cell deep pipeline. To read out the data buffer a special processor called APSP¹³ is implemented. This processor can be operated in two different modes: peak or deconvolution mode. In peak mode only one sample per channel is read from the pipeline while in deconvolution mode three samples are read sequentially and the final output is the weighted sum of all three (details concerning the weights will be presented in the next paragraph). After the APSP procedure the data is sampled/held (S/H) and fed into a 128:1 multiplexer.

¹³Analogue Pulse Shape Processor.

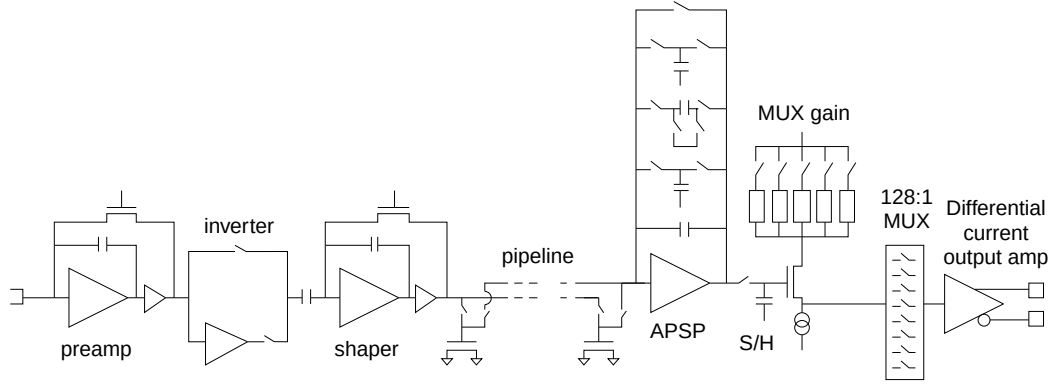


Figure 3.3: Block diagram of the APV 25 chip.

Source: [24]

Signal Processing and Buffering Scheme

The APV architecture is designed for efficient signal processing which includes signal integration, amplifying, and shaping. Signals from silicon strip detectors arrive at the inputs of the chip as single pulses of current which are integrated and amplified by charge sensitive preamplifiers. Each output pulse of the amplifier is characterised by a short rising time of a few nanoseconds, dominated by the charge carrier drift time in the detector bulk, followed by a constant tail lasting a few microseconds. Figure 3.4(a) depicts typical output pulses based on input charges equivalent to the charge deposited by 1–5 MIPs traversing the detector.

An effective CR-RC shaping filter produces a 50 ns shaped voltage pulse. The shaping is adjustable over a limited range to regulate the inevitable degradation of the pulse shape caused by irradiation, for instance. Equation 3.1 describes the parameterization of an ideal CR-RC shaping response $v(t)$ to a typical input pulse produced by the preamplifier.

$$v(t) = \frac{A Q_c t}{\tau} e^{-t/\tau} \quad (\text{for } t \geq 0), \quad (3.1)$$

with A being a constant factor determined by the preamplifier, Q_c being the collected charge and $\tau = RC = 50$ ns being the time constant of the shaping filter. Figure 3.4(b) shows simulated shaper responses to corresponding preamplifier inputs.

The shaper output is sampled at LHC clock intervals and stored in the analogue pipeline buffer realized as a ring buffer of 192 capacitor cells with cycling *write* and *read (trigger)* pointers. Their relative distance determines the latency time elapsed between the physical particle crossing and the L1 trigger decision. The optimal latency time can be adjusted via one of the APV command registers, called LATENCY. The pipeline depth allows a programmable latency of up to 4.8 μ s covering the CMS L1 trigger delay of about 3.2 μ s. The separation between read and write pointers should always be equal to the value programmed into the LATENCY register. This is checked every time the pointers complete a full cycle of the pipeline. If the latency between both pointers does not match the register value, an error is flagged in the ERROR register and in the data header immediately.

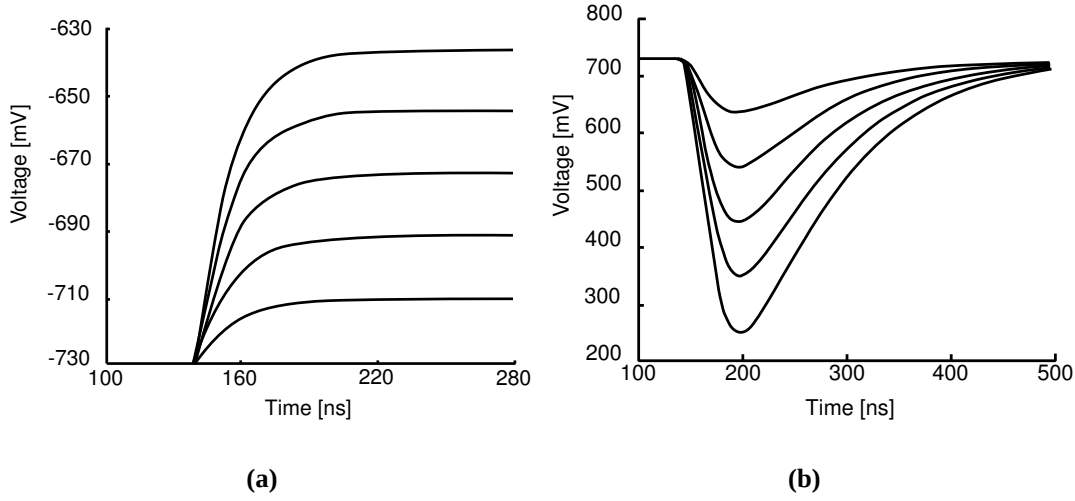


Figure 3.4: Simulation of (a) the APV 25 preamplifier response and (b) the shaper response to input charges equivalent to the charge deposited by 1–5 MIPs traversing the detector. Increasing MIP charge shows up in increasing pulse height. Source: [55]

The analogue pulse shape processor APSP provides the pipeline read out either in peak or in deconvolution mode. In peak mode one data sample is reserved in the pipeline for reading out. This corresponds to the peak voltage of the CR-RC shaped signal, if the sample time is adjusted correctly. In general, peak mode is used when data rates are sufficiently low so that the effects of pile-up of detector signals are not significant. If pile-up becomes more relevant, which is the case for LHC data rates, the CR-RC shaped signals will superimpose each other thus inhibiting the distinction of different consecutive signals. In this situation the deconvolution mode is used (see appendix C.4). Figure 3.5 illustrates the procedure of this specific mode. After an L1 trigger decision the output signal $s(channel)$ of each input channel is composed of three consecutively read pipeline columns as defined by equation 3.2.

$$\begin{aligned}
 s(channel) = & v_{pipe}(channel) \cdot w_1 \\
 & + v_{pipe+1}(channel) \cdot w_2 \\
 & + v_{pipe+2}(channel) \cdot w_3,
 \end{aligned} \tag{3.2}$$

with v_x being the buffer contents of three sequentially marked pipeline columns. For the relative weighting factors the following values are used $w_1 = 1.0$, $w_2 = -1.759$, and $w_3 = 1.457$. These values are realized by fixing the APSP capacitances to $c_1 = 1.16$ pF, $c_2 = 2.04$ pF, and $c_3 = 1.69$ pF.

As a consequence, the deconvolution operation results in a re-shaping of the analogue pulse shape characterised by a new shaping constant of $\tau = 25$ ns. Thus using the deconvolution method offers a way either to use fast or slow shaping depending on the operation conditions.

When the APV chip (running in peak mode) is triggered the appropriate pipeline column is marked for readout to prevent valuable information from being overwritten.

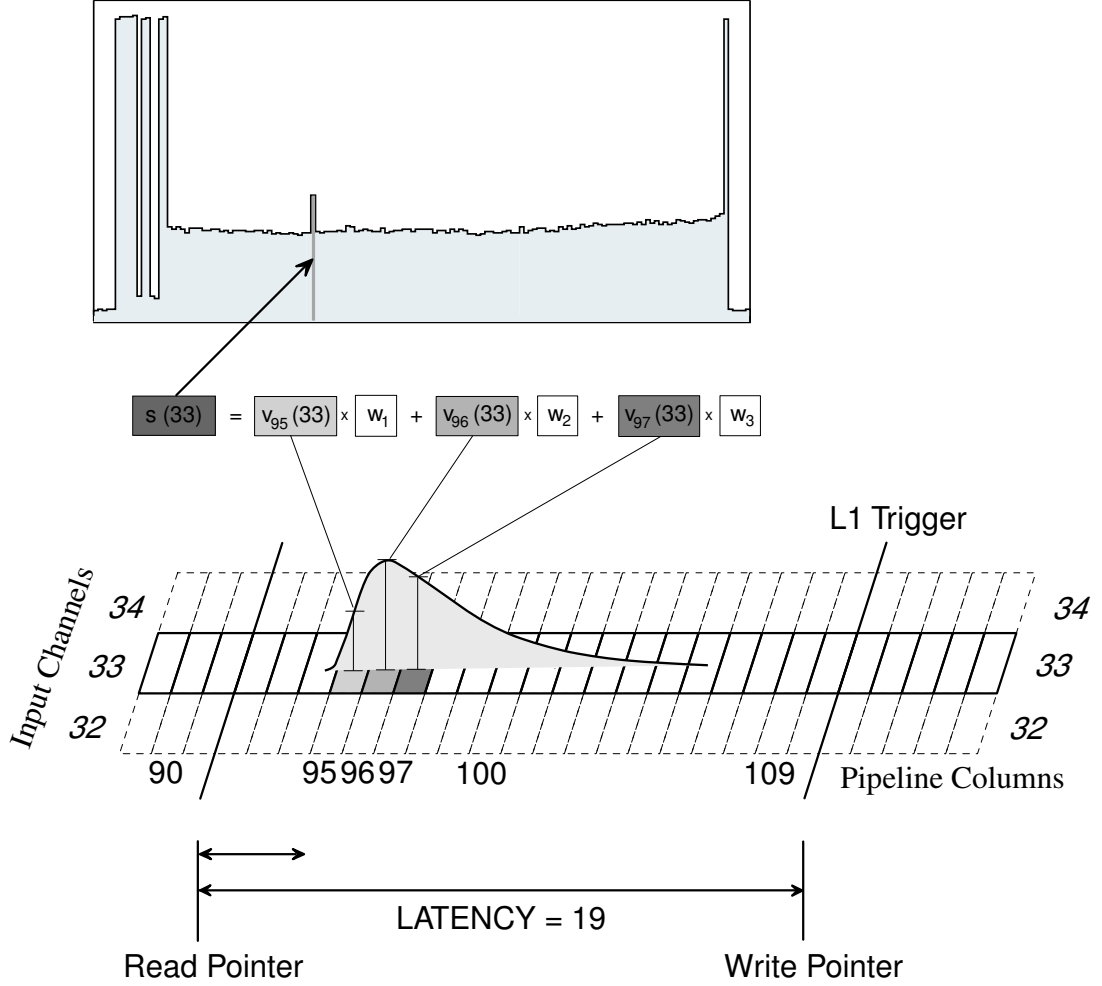


Figure 3.5: The APV 25 deconvolution mode. After an L1 trigger decision, the output signal of each channel is the linear combination of three consecutive pipeline cells. The location of the read pipelines is fixed by the LATENCY value. The column address of a data sample released to the APV output is defined by $WritePointer - ReadPointer + 3$. The three columns added correspond to the 75 ns the chip needs for the preparation of the data.

Then the corresponding address is stored in the *FIFO buffer* with a depth of 31 storage cells. In case of peak mode the FIFO buffer allows 31 triggers before a *FIFO error* is launched (bit 1 of the ERROR register is set to “0”). In deconvolution mode the number of permitted triggers is limited to ten, since for each trigger three consecutive addresses have to be stored.

A 128 to 1 multiplexer drives the only analogue output from the APV chip. In order to meet the required data rate, a nested multiplexer architecture has been chosen. It consists of three levels of multiplexing as shown in figure 3.6.

A fast 4 to 1 output multiplexing stage (level 1) drives the output buffer, each of the four inputs are driven by a second level of 4 to 1 stages (level 2). The final level of 8 to 1 multiplexing stages (level 3) results in the required total of 128 to 1. One advantage of this scheme is that only the output multiplexer needs to run at 40 MHz while the first level multiplexer runs at 2.5 MHz and the second one at 10 MHz. An other advantage concerns the lower power consumption needed. An extra input to the level 1 multiplexing stage provides external digital information (e.g. the digital header, column address and error bit) that is added to the analogue data stream.

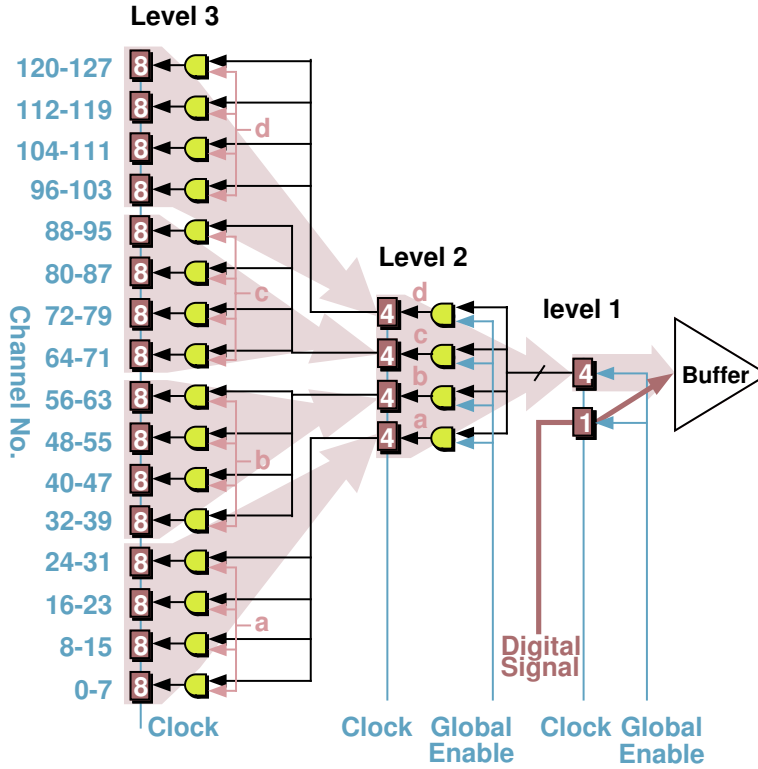


Figure 3.6: Principal structure of the APV 25 multiplexer.

Because of the staged multiplexing, the output channel order does not correspond to the physical ordering of the APV channels. But the physical channel numbering can be calculated by equation 3.3.

$$c = 32 \cdot (n \bmod 4) + 8 \cdot \text{int}(n/4) - 31 \cdot \text{int}(n/16), \quad (3.3)$$

with c being the physical channel number and n being the output channel number.

Internal Calibration

A special feature of the APV 25 chip is the internal calibration circuit which is intended to be a system for on-chip testing and measurement of the analogue pulse response [56]. Basically, the circuit generates and injects pulses of programmable charge into selected input channels. The amount of charge to be selected via the ICAL register covers a range between 0 and 25.5 fC which is equivalent to the charge deposited by 0 to 7.2 MIPs traversing a detector (assuming 1 MIP = 22,000 electrons).

The 128 analogue input channels are clustered in 8 groups, each group consisting of a set of 16 channels. In order to minimize channel cross talk, the channels belonging to one group are separated by 7 uninvolved channels. The selection of each group can be done with the CDRV mask register.

A shaped CR-RC pulse is sampled and stored in 25 ns intervals. To provide a more detailed scanning of a calibration pulse, an additional delay regulator is implemented. Thus a programmable fine delay (CSEL) of eight values in increments of 3.125 ns allows to shift the pulses between two consecutive LATENCY values. Figure 3.7 shows two calibration pulses being processed in peak and deconvolution mode respectively.

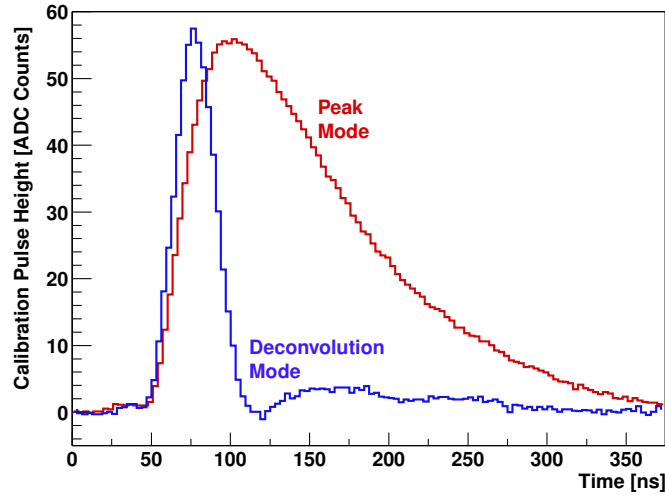


Figure 3.7: Calibration pulses in peak and deconvolution modes with VFS=75.

The calibration circuit should be inhibited under normal chip operating conditions, in order to prevent additional noise generation by the delay regulator logic. Bit 2 of the MODE register inhibits (value = 0) or activates (value = 1) this part of the APV chip.

A double pulse “11” on the trigger line is interpreted as a calibration request. The polarity of a test pulse is negative responding to the first calibration request after start-up or after a reset. But afterwards the polarity toggles between positive and negative on subsequent calibration requests. To receive unipolar signals one has to send the trigger sequence “11-*x*-1-*x*-11” periodically, with *x* being a pattern of (at least two) consecutive zeros. Consequentially, the second trigger request dumps the signal of the alternated polarity as no trigger is followed.

3.2.2 The TPLL Chip

In the CMS tracker system the LHC reference clock and the L1 trigger decisions are transmitted from the counting room to the FE hybrid via a single line to reduce the number of physical channels. Thus both the clock and the trigger information are encoded as a single signal. When the L1 accept decision is issued by the central trigger processor the coded signal stays at logic low level for the duration of a LHC clock cycle thus creating a *missing pulse*. The combined coding of the 40 MHz clock and a first level trigger is depicted in figure 3.8(a).

Combining the clock and trigger lines requires an extra circuitry in the front end system to extract from the encoded signal the exact separated information. This circuitry is represented by the Tracker Phase-Locked Loop ASIC, the TPLL¹⁴. To be more precise, two internal chip components, called PLL and trigger decoder logic, are responsible for this task. Besides clock recovering, a clock phase shifter is also implemented to provide adjustable delays for fine tuning of the timing. The selection of the output clock phase is done by the user via the internal I²C interface. The TPLL contains an autocalibration logic element that sets the optimal bias conditions at start-up. Figure 3.8(b) reveals the basic architecture of the TPLL chip.

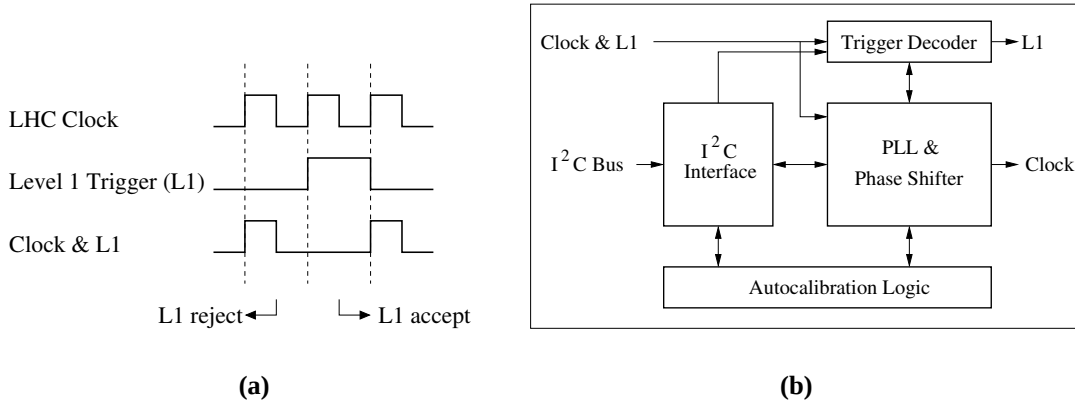


Figure 3.8: (a) Combined coding of the clock and L1 trigger. (b) TPLL architecture with its main components: PLL and trigger decoder for clock and trigger separation, phase shifter for clock phase adjustment, and autocalibration logic to determine optimal start-up settings. Source: [46]

3.2.3 The APVMUX Chip

The APVMUX chip multiplexes the data output of APV pairs onto one single line to reduce the physical readout channels (which means the number of cables) by a factor of two. The difference of the 40 MHz APV clock and the 20 MHz output clock benefits the multiplexing process. After a RESET 101 sequence, the data output starts at even or odd clock periods. This depends on whether the I²C address (in the 7-bit notation)

¹⁴The TPLL is often called PLL.

of the corresponding APV chip is even or odd. Therefore the output frame of odd chips is delayed by 25 ns with respect to even chips. The APVMUX includes fast switches to toggle between both APV data samples, and to attach the corresponding signal thus producing a single data frame with the length of 280 bits¹⁵.

The differential current outputs of the APVs are converted into voltages by internal resistors. The total resistance value R can be varied between $400\ \Omega$ and $50\ \Omega$ using eight $400\ \Omega$ resistors connected in parallel. Switches in series with each of these $400\ \Omega$ resistors allow to vary the total resistor value. An 8-bit register can be loaded to control the switches via the chip internal I²C interface. As a consequence, the total APV frame height can be adjusted to the dynamic range of a digitizing ADC¹⁶ used in the readout hardware (see section 5.1).

3.2.4 The DCU Chip

As the name DCU (detector control unit) indicates, this ASIC is used for monitoring purposes only. Seven analogue input channels provide the supervision of some embedded parameters with a 12-bit resolution. Especially the monitoring of the two low voltages V125 and V250 supplying the hybrid gives important information about the global condition of the FE electronics. Several temperatures can be monitored by the DCU, such as external detector and hybrid temperature as well as the internal DCU temperature. As discussed in section 2.2 another interesting detector parameter is represented by the leakage current I_{leak} which is also fed into the DCU. Similar to the other ASIC chips the device operation is done via an I²C interface.

¹⁵[128 bits(one bit per channel) + 12 bits(header, column, error bits)] $\times$ 2 APVs = 280 bits.

¹⁶Analogue-to-Digital Converter.

Chapter 4

CMS Silicon Microstrip Detector Modules

Based on the details concerning CMS silicon sensors and FE electronics given in the chapters 2 and 3, the construction of a CMS silicon detector module will be described in this section. In particular, known problems and flaws of these modules are of huge interest from the point of view of a large-scale production and quality control. Assembly failures can influence the performance of a module significantly. Therefore an early detection of those failures is essentially in the production chain.

4.1 Layout of the TEC Modules

The build-up of a CMS TEC silicon microstrip detector module is depicted in figure 4.1.

For TEC modules belonging to ring five to seven, two silicon sensors (WxA and WxB) and the FE hybrid have to be glued (with two-component epoxy glue [57]) onto a mechanical structure, the *frame*, in order to guarantee mechanical stability thereby using a minimum budget of material. The frame is made of three parts of carbon fibre composite which are glued together: two *frame legs* and one *cross piece*. For modules in the rings one to four, only one sensor is needed. In these cases a frame is made of single pieces of carbon fibre. Apart from stability aspects, the frame plays also an important role in the tracker cooling strategy. Since the FE electronics and the irradiated modules dissipate a large amount of heat during their operation (2.1 W per hybrid and 0.5 W per sensor after ten years of LHC operation), an efficient heat transfer to the cooling system is needed. Due to its high thermal conductivity properties (see table 3.1), the frame matches the transfer requirements.

In order to bias the module and to measure the temperatures on the sensors, a specific *Kapton foil* is glued onto both legs of the frame. The foil is a sandwich of Kapton and copper layers and carries temperature sensors. The copper layers are used to apply the high voltage to the sensors while the Kapton insulates the sensor backplane from the frame which is at ground potential. Conductive glue (Polytec EE-129-4 [58]) is used to connect the backplane and the bias part of the Kapton foil.

In the cases of ring five to seven both sensors WxA and WxB have to be contacted electrically with each other via bond wires which means that each strip pad on the first sensor has to be bonded to its corresponding pad on the second sensor. While the sensor-to-sensor bonding is done between equal pitches, the APV pad pitch does not match the sensor pitches. Thus an interface, called *pitch adapter*, has to be inserted to adapt the different pitches. A closeup view of this interface is shown in figure 4.2. The pitch adapter consists of a glass substrate with $1.5\text{ }\mu\text{m}$ thick fan-like aluminium strips and bond pads. Due to the various detector types needed in the tracker, 24 different pitch adapter designs are planned with substrate dimensions varying between $64 \times 9\text{ mm}^2$ and $123 \times 21\text{ mm}^2$ [59].

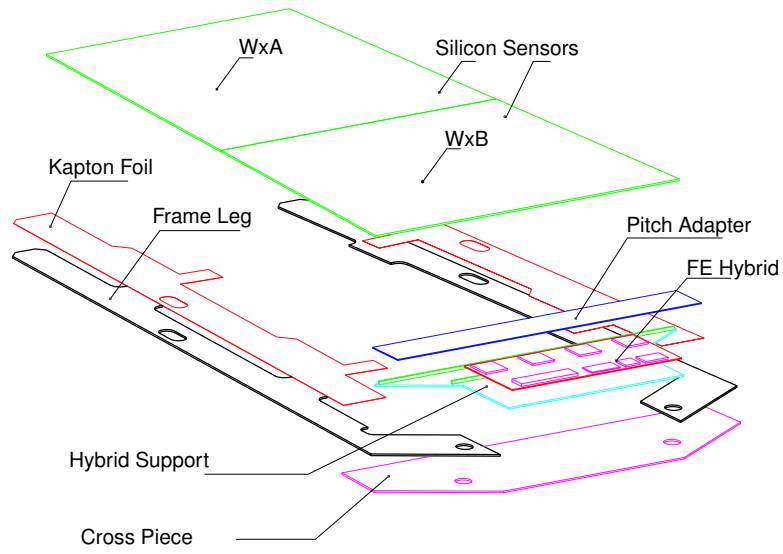


Figure 4.1: Exploded view of a TEC wedge-ring-x module. The labels WxA, WxB are used to identify the location of each sensor with respect to the module and the tracker (W6B $\equiv$ wedge-shaped sensor of ring 6 placed on the hybrid side of the module, for example).

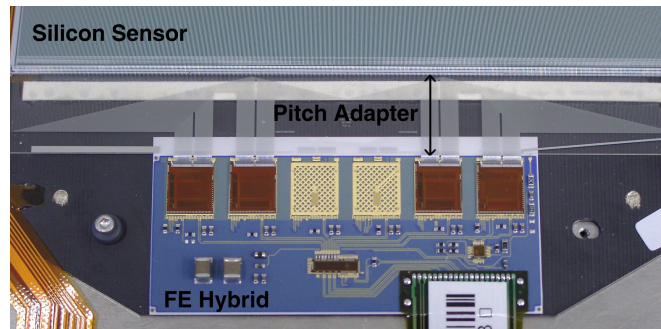


Figure 4.2: Pitch adapter between sensor and FE electronics.

Figure 4.3 shows a TEC wedge-ring-6 module belonging to the so-called *express-line 1* batch which is a pre-series production of twelve modules assembled in March 2002. The module is equipped with a ceramic hybrid housing four APV chips. Details about the modules of the pre-series and their qualification results will be given in chapter 7.

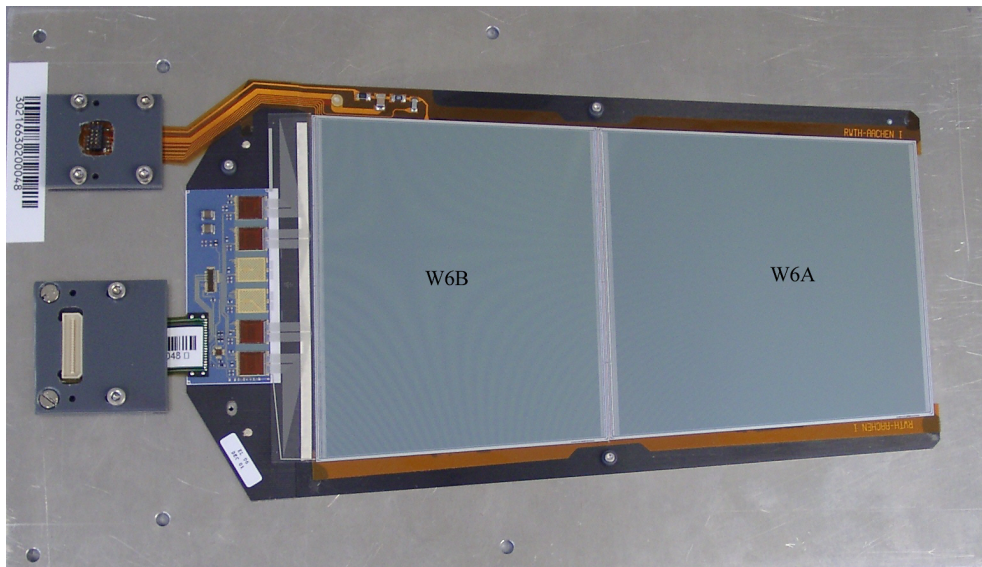


Figure 4.3: TEC wedge-ring-6 module of the express-line 1 batch.

4.2 Problems and Flaws Affecting the Module's Performance

As described in the previous sections, a CMS tracker module is composed of different materials and components demanding various sophisticated production technologies. This complexity involves a large variety of conceivable problems arising during the individual production phases. Not only assembly failures, but also the transportation and the handling of the hybrids or modules may have impacts on their functionality and performance.

Based on the experiences of former experiments using silicon detectors and on those gained by measurements with prototype hybrids and modules, typical flaws and failures of such systems can be deduced. The most important failures that play an essential role in the developed test procedures (which will be described in chapter 6) are defined below:

- **open:**
 - (a) missing or broken bond wire,
 - (b) aluminium strip breakage.

- **short:**

- (a) electrical connection of one or more neighbouring aluminium strips or p^+ implants,
- (b) shorted conductor paths such as bond wires or PCB¹ tracks.

- **pinhole:**

shorts or ohmic connections between aluminium strips and their corresponding p^+ implants.

While opens and shorts can occur at silicon modules as well as at FE hybrids, pinholes are module specific failures.

Open

An individual TEC wedge-ring-6 module needs more than 1,500 single bond wires to be welded onto bond pads. In particular, the pad pitches between pitch adapter and APV chips are very small (44 μm). During the automated bonding process, bond wires are used to connect sensor-to-sensor, sensor-to-pitch adapter and pitch adapter-to-readout chips. Non-packaged ASIC chips are also bonded to the hybrid substrate. Due to the large number of bond wires to be welded, weak or even missing bondings can occur. Although a single bond wire is designed to hold masses up to (10 ± 1.2) g, the susceptibility to careless handling and transportation is not negligible. Recent tests show that vibrations perpendicular to the module plane can have detrimental influences on the bond wires [60].

Scratches on the sensor surface can lead to breakages of the aluminium strips whereas the discontinuance of a p^+ implant originates in the sensor processing.

Strips affected by open bond wires or breaks are characterized by a lower capacitance compared to the nominal strip capacitance C_{nom} , which is given by the sum of the individual sensor and pitch adapter capacitances:

$$C_{nom} = C_{WxA} + C_{WxB} + C_{pitch}. \quad (4.1)$$

In the case of missing or open bond wires, usually a repair can be envisaged, if none of the bond pads is damaged. In general, an open is no danger to the readout chips, but it affects the noise behaviour of the corresponding strip (see section 4.3).

Short

Shorts on sensors originate mainly from the wafer processing technique. Although planar technology plays an essential role in the industrialized large-scale production of silicon sensors, it can cause some undesirable failures leading to strong electrical effects. Especially the photolithographic process or the oxide etching phase are probable sources for shorts. For a closer look at the sensor production process see appendix B.1.

¹Printed Circuit Board.

As a consequence, in most cases a repair is not possible. Shorts are characterized by higher capacitances with respect to the nominal values and cause fake multi-strip hits degrading the detector resolution.

Pinhole

Similar to the creation of shorted sensor strips, pinholes are generated during the planar wafer processing. Usually, a photolithographic defect in the processing of the insulating layer is the reason for a pinhole. A small hole in the insulation means that during the metallization phase the metal can reach close to or even touch the implanted p^+ strip. Deep scratches on the sensor surface due to careless handling or breakthroughs of bonding pads might also cause pinholes.

Pinholes are the most dangerous kind of failures, since they can disable complete readout chips. Thus the affected strip has to be disconnected from the APV input.

Miscellaneous Faults

The leakage current should be constant, at constant environment temperature and stable humidity, after reaching the depletion voltage V_{depl} . Deviations from this rule show wafer flaws due to variations in the processing phase. The leakage current should not exceed a certain limit, since this would cause additional noise. Finding the sources of a high leakage current allows the improvement of processing methods.

The reliable operation of the CMS silicon detectors requires a carefully controlled environment which includes constant temperature and humidity conditions. Especially the high voltage performance is sensitive to the environment. High voltage breakdowns originate in local high electrical fields caused by bad sensor cuts, humidity, crystal defects, bad isolation layers, etc. The breakdown voltage has to be above 500 V in order to match the CMS radiation requirements.

The module and hybrid readout depends on the functioning of the ASIC chips. Due to bad bonding or soldering of a chip, the I²C communication can fail thus inhibiting a reliable operation. A wrong low voltage power supply can cause problems with respect to the I²C bus protocol and level acknowledgment. In this case the chip communication will also fail. Usually this kind of errors is called *I²C faults*.

4.3 Noise Performance

Since the signals created in a silicon detector are very low, the signal detection and the particle reconstruction efficiency of the tracker is affected by the noise performance of the individual modules significantly. Opens, shorts, and pinholes influence the noise behaviour of a module, since these failures increase or decrease some important quantities such as capacitances or currents.

In general, the noise in electronic systems, such as silicon detectors, is defined in terms of *equivalent noise charge (ENC)* given in units of the electrical charge e . The total noise ENC_{tot} is usually the result of several contributions originating from

different components of the system. Assuming that the individual sources behave uncorrelated, ENC_{tot} is given by equation 4.2.

$$ENC_{tot}^2 = \sum_i ENC_i^2 \quad (4.2)$$

The noise consideration basically depends on the electrical parameters of a typical CMS silicon detector module. In order to quantify the noise contributions of a module, a simplified electrical scheme of noise related components has to be taken into account. Figure 4.4 illustrates the most important noise sources in the detector. They are separated in voltage and current generators. Voltage generators are connected in series with the preamplifier and the sensor, thus creating *series noise*. Contrariwise, current generators are connected in parallel with the sensor and generate *parallel noise* [61].

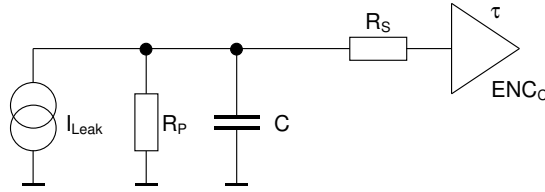


Figure 4.4: Simplified schematic of noise sources in a silicon strip detector. The physical noise sources can be identified in the leakage current I_{leak} , in the polysilicon resistor R_P , and in the series line resistor R_S to be added to the contribution of the preamplifier. Source: [24]

Mainly four noise sources contribute to the total noise ENC_{tot} :

- Shot noise $ENC_{I_{leak}}$ (parallel noise) from the detector bias current I_{leak} given in nA:

$$ENC_{I_{leak}} = 106 \cdot \sqrt{I_{leak} \cdot \tau}, \quad (4.3)$$

with τ being the time constant of the shaper given in μs .

- Polysilicon resistor (R_p , given in $M\Omega$) noise ENC_{R_p} (thermal, parallel noise):

$$ENC_{R_p} = 758 \cdot \sqrt{\tau / R_p} \quad (4.4)$$

- APV amplifier noise ENC_C being composed of a constant parallel part and a serial part scaled with the total capacitance C given in pF:

$$ENC_C = ENC_{Cp} + C \cdot ENC_{Cs} \quad (4.5)$$

- Readout line resistor (R_s , given in Ω) noise ENC_{R_s} (thermal, serial noise):

$$ENC_{R_s} = 0.395 \cdot C \cdot \sqrt{R_s / \tau}. \quad (4.6)$$

The noise depends strongly on the time constant τ of the chosen readout system. Parallel noise sources rise with increasing τ whereas series noise shows the opposite behaviour. As a consequence, noise estimations must be done for peak mode and for deconvolution mode separately. The deconvolution mode compromises the noise. Table 4.1 summarizes the resulting noise contributions based on typical CMS detector and readout parameters. The total theoretically expected equivalent noise charge ENC_{tot} reaches 1,100 electrons for peak mode whereas deconvolution mode leads to about 1,600 electrons. To give an impression of these numbers, a traversing MIP creates about 22,000 $e-h$ pairs in a standard 300 μm thick silicon wafer. Thus the ratios of a MIP signal and the estimated noise values are approximately 20 and 14, respectively. Some components within the CMS readout chain also contributing to the total noise have been neglected in the simplified estimation above. Nevertheless, although several line drivers, receivers, or transmission lines will cause additional noise in the system, the total noise is still dominated by the APV input noise.

Noise Source	Parameter	Value	
	Amplifier	APV 25	
	I_{leak}	1000 nA	
	R_p	1.5 M Ω	
	C	18 pF	
	R_s	50 Ω	
		APV MODE	
		Peak	Deconvolution
	τ	0.05 μs	0.025 μs
	ENC_{Cp}	250 e	400 e
	ENC_{Cs}	36 pF $^{-1} \cdot e$	60 pF $^{-1} \cdot e$
$ENC_{Ileak}[e]$	see eq. 4.3	530	375
$ENC_{Rp}[e]$	see eq. 4.4	138	60
$ENC_C[e]$	see eq. 4.5	898	1480
$ENC_{Rs}[e]$	see eq. 4.6	225	345
$ENC_{tot}[e]$	see eq. 4.2	1076	1566

Table 4.1: Noise related parameters and corresponding noise numbers.

Source: [24]

It has been shown [62] that the ratio between peak mode noise and deconvolution mode noise can be expressed for parallel and series noise separately called REL_p and REL_s , respectively. Both ratios are given in equations 4.7 and 4.8.

$$REL_p = \frac{ENC_{dec,p}}{ENC_{peak,p}} = \sqrt{\frac{e^{-2}}{x^2} \cdot (e^{2x} - 4x - e^{-2x})} \quad \text{and} \quad (4.7)$$

$$REL_s = \frac{ENC_{dec,s}}{ENC_{peak,s}} = \sqrt{\frac{e^{-2}}{x^2} \cdot (e^{2x} + 4x - e^{-2x})}, \quad (4.8)$$

where $x = \Delta t / \tau$ is the ratio of sampling interval to amplifier time constant. The noise values in case of deconvolution mode are referred to as $ENC_{dec,p}$ and $ENC_{dec,s}$ whereas in peak mode the noise values are named $ENC_{peak,p}$ and $ENC_{peak,s}$.

The effect of different choices of x is illustrated in figure 4.5. Assuming CMS conditions, x is equal to 0.5 (since $\Delta t = 25$ ns and $\tau = 50$ ns) which leads to following estimation:

$$ENC_{dec,p} \approx 0.44 \cdot ENC_{peak,p} \quad \text{and} \quad (4.9)$$

$$ENC_{dec,s} \approx 1.53 \cdot ENC_{peak,s}. \quad (4.10)$$

By this means the deconvolution method decreases the parallel noise while the series noise increases. It can be surmised that the measured ratio of deconvolution mode noise and peak mode noise will lie somewhere between the extremes of the series and parallel cases.

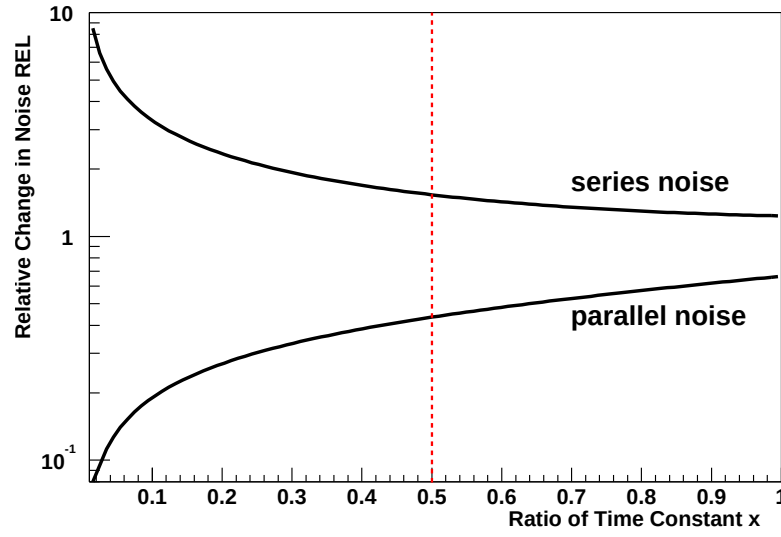


Figure 4.5: The effect of deconvolution on noise, expressed as the ratio of noise before (peak mode noise) and after the APSP filter (deconvolution noise), called REL . The solid lines show separately the consequences for parallel and series noise whereas the dashed line indicates the CMS case with $x = 0.5$ ($\Delta t = 25$ ns and $\tau = 50$ ns).

Chapter 5

Development of a Test Facility for CMS Hybrids and Modules

The construction of the CMS tracker involves a large number of industrial companies and research institutes from many different countries. The silicon module mass production period will span over one year. During this period it is essential to assure simple and reproducible assembly and testing procedures among all centres. This demands an environment for testing which is able to accompany and supervise ideally the complete production phase. A reliable diagnostic system is already mandatory during the research and development periods of specific components, such as front end hybrids.

In general, a standard test facility is composed of three units: the diagnostic and control hardware, the corresponding readout and analysis software, and the test environment (see figure 5.1). While the test hardware in combination with the software builds a system interacting directly with the test object, the test environment is required to facilitate a safe and reproducible operation of the test system and object. Each unit of a test facility needs an appropriate design in order to match all constraints set by the test object.

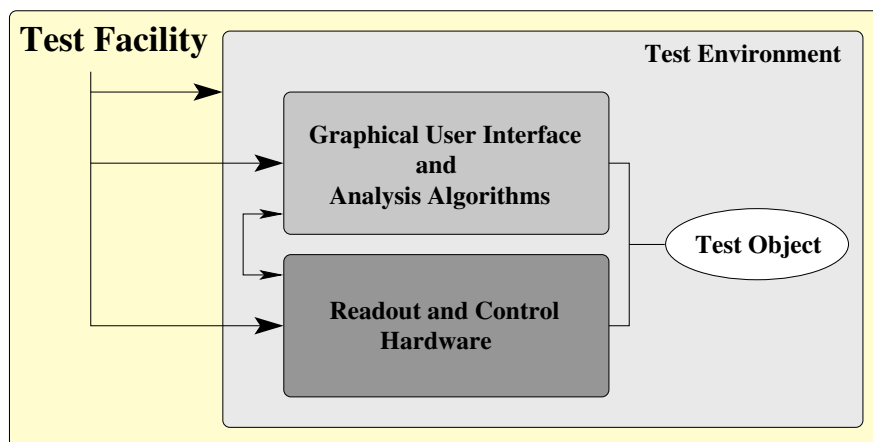


Figure 5.1: General schematic of a test facility.

The test facility introduced in this thesis is particularly intended for diagnostic purposes and quality assurance of CMS FE hybrids and silicon detector modules. This includes the reliable observation of typical failures as discussed in section 4.2. According to its main feature, the test system is called *APV Readout Controller (ARC)* [63]. The development of the ARC system started at Aachen in midyear 2000.¹

5.1 The ARC System

The minimal equipment needed to readout and control a FE hybrid is composed of only a few elements providing a compact and flexible structure. In the following sections the most important features and tasks of each component of the ARC setup will be discussed.

5.1.1 ARC Board

The fundamental device within the ARC setup is the *ARC board* [65] which is depicted in figure 5.2. It is a printed circuit board designed in Double Euro format (160 mm × 233 mm) thus fitting into a standard 19" crate. A single ARC board has to be powered by ± 5 V DC voltages requiring currents of 1.4 A / 60 mA. These voltages can be applied to the ARC board by a standard DC low voltage device.² When there is need for operating more than one ARC board at the same time, the backplane of a 19" crate can also be used to power these boards (see section 5.3). In this case the connection to each board is done via the same 64 pin connector used to link the readout bus.³ Two hybrids can be connected to the front plate of one ARC board (*HYBRID 1*, *HYBRID 2* connectors) while an expansion bus (*EX BUS*) provides the synchronized operation of several boards and FE hybrids. External trigger signals can also be applied via a Lemo socket (*TRG*). The *BUSY* Lemo socket gives information about the condition of the ARC board (busy / not busy) according to the data processing after receiving a trigger.

There are three main function blocks on the ARC board facilitating the complete operation of FE hybrids or silicon modules:

- clock and trigger generation and distribution,
- data sampling and buffering, and
- slow control and low voltage control.

The properties of these function blocks are accessible via software. Each board has a specific 8-fold DIL⁴ switch defining an individual address in order to distinguish several boards operated at the same time.

¹Basic principles of the ARC system originate in the prototype synchrotron radiation detector (PSRD) readout setup developed for the Alpha Magnetic Spectrometer AMS [64].

²The power is supplied via the D-Sub9 connector on the ARC board.

³A HI-CON connector is mounted on the ARC board for this purpose.

⁴Dual InLine.

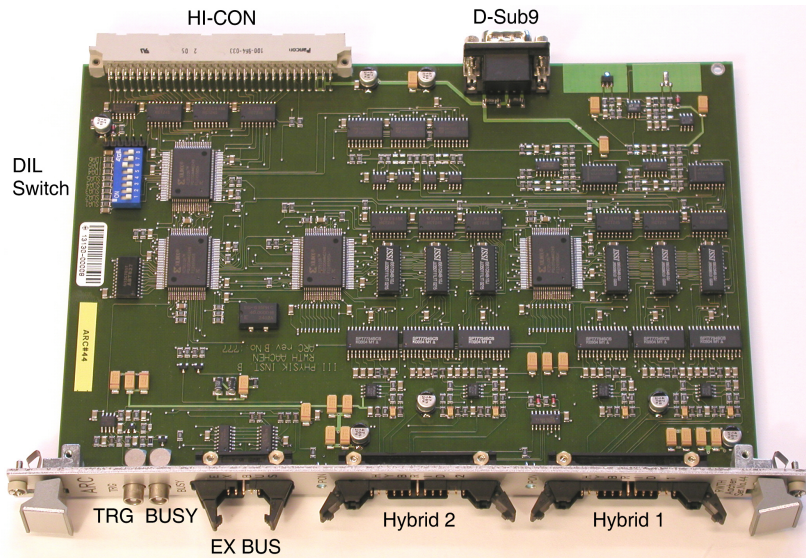


Figure 5.2: The APV Readout Controller board ARC.

Clock and Trigger

The *APV controller* located on the ARC board creates the clock and trigger signals for both hybrids connected. The clock itself is generated by a crystal oscillator, while the trigger signal can be generated by software via an ARC internal register. Optionally, an external generated asynchronous NIM⁵ or LVDS⁶ signal can be applied to the TRG Lemo connector on the front side of the ARC board. Finally, the trigger pulse is latched to and synchronized with the system clock. Initialized by this trigger, a programmable 16-bit long APV trigger sequence is send to each APV. This sequence can be composed of the APV specific patterns (event trigger, RESET 101, and calibration request) as described in section 3.2.1. In order to generate several trigger signals with varying time differences of up to 255 clock ticks, the so-called *spacer* has been implemented defining the number of clock cycles to elapse without a trigger signal. Since the spacer divides the 16-bit trigger sequence into a high and a low byte, it can be used to expand the 16-bit trigger pattern. Figure 5.3 illustrates the spacer feature by means of an example.

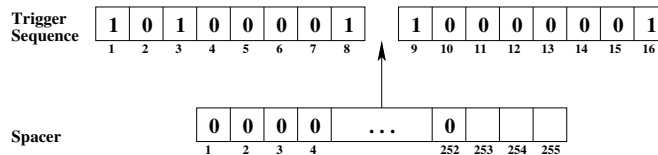


Figure 5.3: Principle of the trigger pattern sent to the APV. If the spacer is set to 252, the two event trigger at bit position 8 and 9 are separated by 252 clock cycles.

⁵Standardized Nuclear Instrument Module logic signal.

⁶Low Voltage Differential Signaling.

Data Sampling and Buffering

Two groups of three 8-bit ADCs, one group for each hybrid, sample the analogue APV data with a synchronized clock with optionally 20 or 40 MHz. In order to adjust the correct sampling time, the ADC clock phase can be shifted in ten steps of approximately 1.7 ns. Individual ADC working points can be adjusted by DACs⁷ to exploit the 8-bit resolution of the ADCs. Finally, the digitized data are stored in an 8 kByte RAM⁸ per ADC.

Slow Control and Low Voltage Control

There are three I²C controller⁹ located on the ARC board. Two of them are used for hybrid slow control purposes providing the communication between the PC and the ASICs. The third one is utilized to control and monitor the low voltage power consumptions of the hybrid. The corresponding low voltage regulators are mounted on the ARC FE adapter (see next section) which can be accessed via the ARC board.

Some ARC board specifications and features are summarized in table D.1.

5.1.2 ARC Front End Adapter

The *ARC front end adapter* [67] is an other important element in the framework of the ARC test setup. The first release of this component consists of two printed circuit boards (dimensions: 72 mm × 72 mm) which can be stacked onto each other. Figure 5.4 shows all sights of the adapter cards.

One of the two boards houses amplifiers, line drivers, and an I²C level shifter to adjust the I²C signals as needed. The voltage regulation for the hybrid is located on the second board. In order to avoid reverse currents due to hybrid failures, the hybrid power regulator is designed as a voltage tracking regulator. Thus the voltage on the V125 line is always half of the voltage on the V250 line.

An I²C controller on the ARC board provides the access to hybrid currents and voltages on the two power lines by software. The voltages can be adjusted within a range of +4% / – 15% with respect to the nominal voltages. Currents can be measured with a resolution of 4 mA, whereas the voltages are determined with a precision of 10 mV at V125 and 20 mV at V250, respectively. An over-voltage protection as well as a current limiter guarantees the safe hybrid operation with respect to its power consumption. If one voltage exceeds the nominal voltage by more than 8%, the complete hybrid voltage supply is cut off to prevent hybrid damage. The current limiter is set to 1.3 A on the V250 and to 0.9 A on the V125 power line. These values are based on experiences gained with a significant number of hybrids with four APVs and extrapolated to expected values for six APVs.

The separation of the high power dissipating part from the FE adapter facilitates the use of the ARC system for hybrid and module thermal cycling tests. Only the level

⁷Digital to Analogue Converter.

⁸Read Access Memory.

⁹The controller are of type PCF8584 [66].

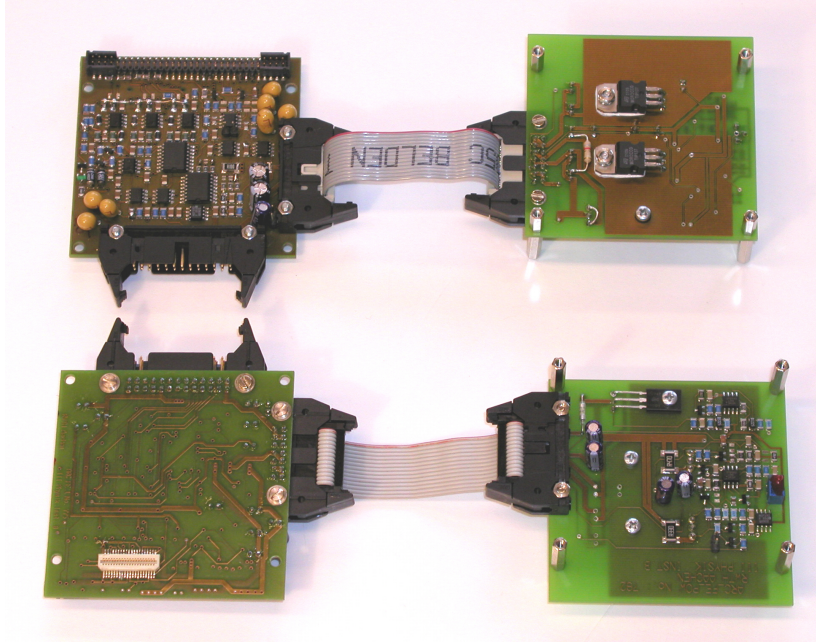


Figure 5.4: Different sights of the ARC front end adapter. The boards on the left side represent the amplifier and I²C level shifter part while the boards on the right are responsible for the voltage regulation.

shifter and the analogue buffer need to be close to the hybrid while the high power part can be located apart from the hybrid.

All test results shown in this thesis are obtained from measurements using the described version of the ARC FE adapter. Since January 2003 a modified type of FE adapter is available, called *ARC FE_M adapter*. This adapter has the same features as the old version, but is also suited to provide an appropriate operation of modules including high voltage connection, backplane pulsing, and grounding. Figure D.1 depicts the latest version of the FE adapter.

5.1.3 PC Adapter

The communication between the computer and the ARC system is realized with the *SRDPC bus*¹⁰ specifically designed for the AMS experiment. Generally, the bus protocol is a standard PC ISA bus adapted for long cable lengths. The bus is operated at about 5 MHz transferring 16 bits in parallel. Due to the bus specific *extended bus cycle* feature, the readout rate is limited to 2 MB/s.

Two different kinds of connection between the ARC board and the PC are supported. In the first case the *PCMIO card* [68] serves as an ISA bus extender which buffers and links 16 data lines, 6 address lines, as well as three control lines from the ISA bus via a 50 pin flat cable to the SRDPC bus. The card fits into a standard IBM XT ISA slot.

¹⁰Synchrotron **R**adiation **D**etector **P**C bus [64].

If no ISA slot is available, the *SRDEPPPC module* [69] can be used instead of the PCMIO interface. In this case the interface is connected to the PC printer port which has to provide the *enhanced parallel port (EPP)* protocol¹¹. Thus the usage of a notebook can be envisaged resulting in a portable test setup.

The SRDEPPPC module transforms the EPP byte transfer to the SRDPC bus protocol resulting in a significantly slower readout rate compared to the PCMIO card. Each device that acts on the SRDPC bus has a specific identity number defined by an on-board DIL switch (see figure 5.2).

5.1.4 Build-up of the Minimal ARC System

Figure 5.5 depicts all components of the minimal ARC setup configuration developed in Aachen.

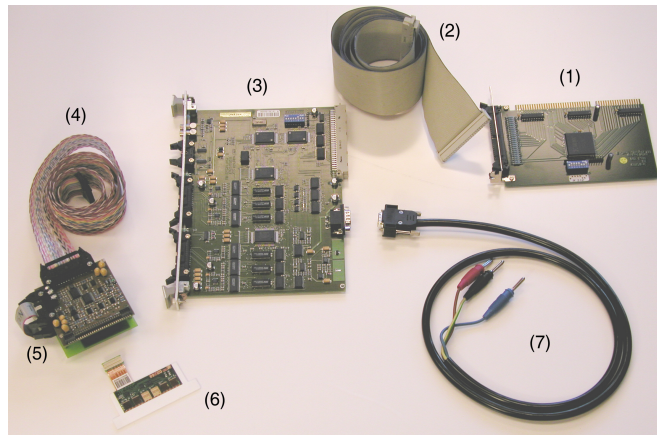


Figure 5.5: Minimal ARC system components: (1) PC adapter card, (2) 50 pin flat cable, (3) ARC board, (4) 26 pin twisted pair flat cable, (5) ARC FE adapter, (6) FE hybrid, and (7) power cable to DC low voltage supply.

The ARC board has to be connected via a 50 pin flat cable to the PC adapter which is a PCMIO card in this case. The low voltage is applied to the ARC board via a special power cable merging three pin plugs to a D-Sub9 connector. An appropriate DC low voltage supply has to provide about 3.5 A at the +5 V line and 60 mA at the -5 V line considering the hybrid load (1.4 A for the ARC board and about 0.9 A per hybrid on the positive voltage line) and optional setup extensions (see section 5.1.5). Each hybrid is connected directly to its own ARC FE adapter which is linked to the ARC board via a 26 pin twisted pair flat cable.

The main function blocks of the minimal ARC setup are depicted in figure 5.6. For the sake of lucidity, only those coherences are implemented which are essential for the operation of a single hybrid. In particular the buffering part of the scheme duplicates in case of a two-hybrid readout.

¹¹EPP allows a bi-directional parallel data transfer.

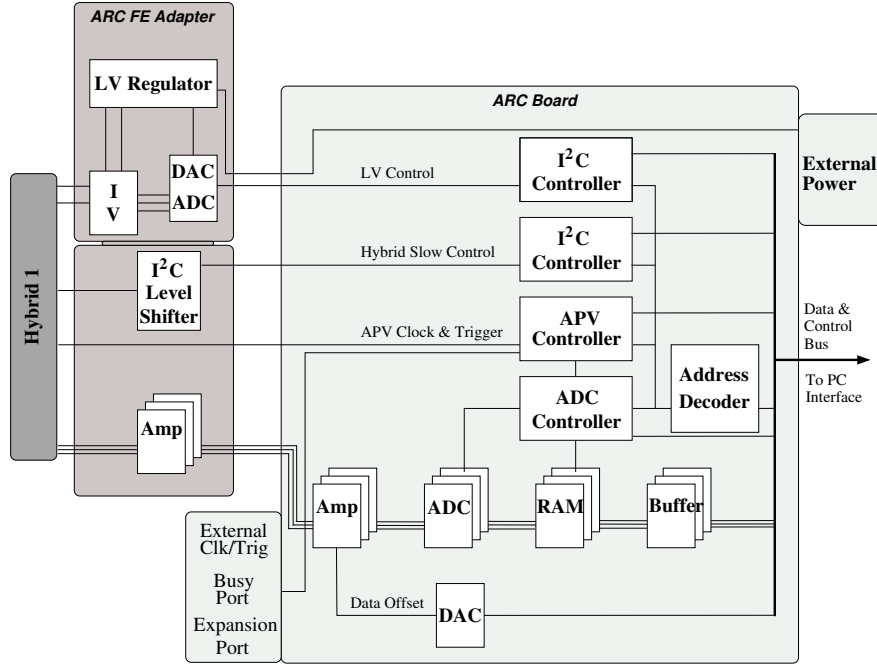


Figure 5.6: ARC board and ARC front end adapter function blocks to operate one hybrid.

The ARC system can be operated either in a *single board setup* or in a *multi board setup*. As indicated in figure 5.7, a multi board setup is composed of several ARC boards housed in a crate. In this case one ARC board acts as a master and the others act as slave devices. The external trigger is applied to the master board that forwards clock and trigger signals to the other boards via the expansion bus connection on the front side of each ARC board. By this means a multi board setup can be synchronized to one global clock and trigger.

5.1.5 Extensions of ARC

The basic concept of the minimal ARC system allows its extension to a complete stand-alone silicon detector module test setup. In particular a tool providing external source measurements and a specific high voltage supply are required to qualify a detector module.

LEP_16 Board

Since silicon is sensitive to electromagnetic radiation (see section 2.1.1), light with a certain wavelength can be used to prove the response of each readout strip on the module. Considering figure 2.3, the infrared wavelength regime corresponds to a photon penetration depths matching the thickness of a CMS module. Photons in this energy range can be produced either by a laser device or by LEDs¹².

¹²Light Emitting Diodes.

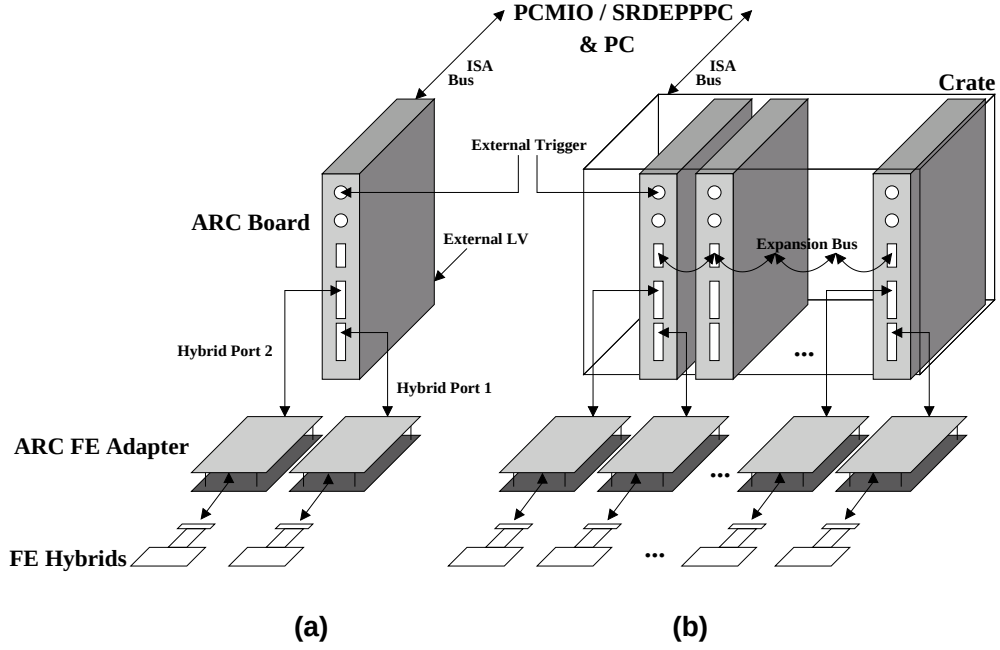


Figure 5.7: A schematic diagram of the minimal ARC setup in terms of (a) single board and (b) multi board setup.

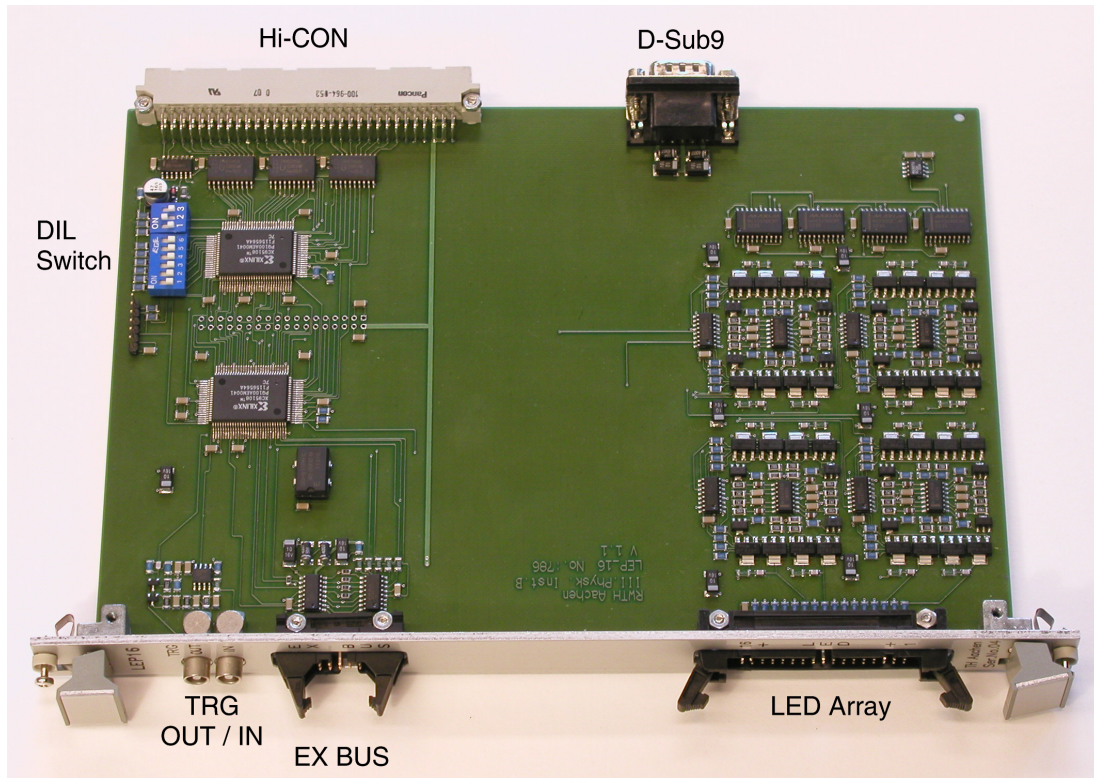
The final decision to establish a certain kind of LED controlling device was influenced by several aspects such as cost-performance ratio, availability, and appropriate features. Thus a 950 nm GaAs-LED¹³ produced by Osram was adopted to build an array of LEDs (see table D.2 for detailed LED properties). Due to the wavelength of 950 nm, the penetration depths is only about 50 nm thus creating electron-hole pairs mainly in the detector surface region. This is adequate to observe the detector failures described in section 4.2.

A specific LED controller board has been developed which is compatible to the ARC environment. In fact, this controller is of the same size as the ARC board and is called *LEP_16*¹⁴ (see figure 5.8). It is intended to perform continuous or pulsed light tests with up to 16 LEDs illuminating the depleted module sensors. Each LED can be operated individually with respect to pulse width and light intensity. The pulse repetition rate is also adjustable for the LEDs. The LED pulser can deliver a trigger signal required to be applied to the external trigger socket of the ARC board.

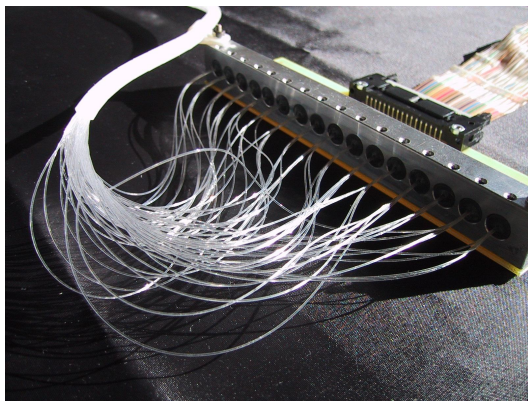
Figure 5.8(b) gives an impression of the designed LED array which consists of 16 diodes embedded within an aluminium block of 17 cm length. Each LED is coupled to four 1 m long optical fibres thus increasing the number of light spots to 64. The opposite ends of the fibres are glued in series into a mechanical support structure with a pitch of 2 mm, to cover the full width of all sensor designs planned. Thus the total width of the optical fibre array is 12.8 cm. Figure 5.8(c) illustrates the fibre array which can be mounted above the silicon wafer.

¹³Type SFH 4501 [70].

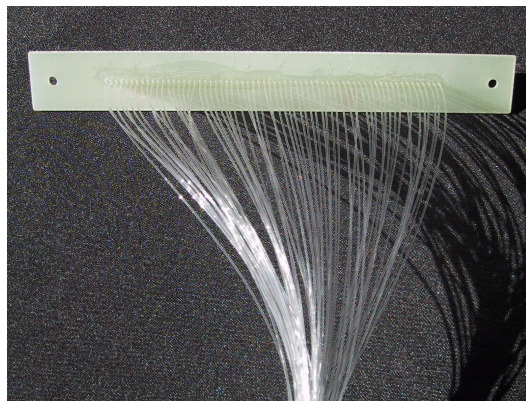
¹⁴LED Pulser that facilitates the operation of 16 LEDs.



(a) LEP_16 board.



(b) Infrared LEDs.



(c) Optical fibre array.

Figure 5.8: The LED pulser equipment: (a) The LED controller board. (b) 16 LEDs counter-sunk in an aluminium block. Each LED is coupled to four 1 m long optical fibres. (c) Mechanical structure of the fibre array.

Due to the small diameter (0.5 mm) of each optical fibre, small light spots can be achieved. The size of one light spot is equivalent to approximately 25 detector strips (see section 6.1.6) when the array is mounted 3 mm above a silicon wafer. For safety reasons, the fibres are encased in a flexible hose. In addition, the aluminium block is located within a rigid plastic box to prevent the fibres from being disconnected.

DEPP Board

Since a module needs to be operated with bias voltage, a module test facility has to provide high voltage of up to 600 V as well as a current measurement device with an appropriate resolution. As described in section 2.2, the leakage current of a detector plays an essential role in the characterization and behaviour of this semiconductor device. A specific high voltage module, called *DEPP*¹⁵, has also been developed at Aachen which is fully compatible to the ARC system. This means that it can be latched to the same SRDPC bus connected to the ARC board or the LED controller. DEPP provides a voltage range of 0 to 600 V and current measurements in three ranges with different resolutions: 0–10 μA (resolution: 2.5 nA), 0–100 μA (resolution: 25 nA) and 0–1000 μA (resolution: 250 nA). Since this power supply could not be used for the measurements presented in this thesis, it will not be described in detail here. Figure D.2 shows a photo of the DEPP board.

5.1.6 Production of the ARC System

Table 5.1 gives a summary of all ARC components produced in Aachen and distributed to various members of the CMS tracker collaboration so far.

Component	Number
PCMIO card	100
ARC board	81
FE adapter old	50
FE adapter new	80
LEP_16	22
DEPP	16

Table 5.1: ARC setup components delivered so far. The production of additional boards is envisaged.

5.2 The Front End Hybrid Industrial Tester

An industrial specific device, called *Front End Hybrid Industrial Tester (FHIT)* [71], was designed in close collaboration with UCL¹⁶ Louvain-la-Neuve and RWTH Aachen

¹⁵DEPLEtion Power.

¹⁶Université Catholique de Louvain.

to supervise the industrial hybrid manufacturing. The system is meant to perform a fast and easy test of every FE hybrid directly after its assembly.

There are three different types of FHIT systems available, the *mono-FHIT*, the *dual-FHIT*, and the *easy-FHIT*. Since the recommended test setup suited for industrial purposes is represented by the dual-FHIT, this type of system will be discussed in the following.

The dual-FHIT consists of two printed circuit boards, called *FHIT boards*, connected to one ARC board. In a sense, one FHIT board replaces the ARC FE adapter, but is suited for *connectivity tests (CT)* and *electrical tests (ET)* searching for some global hybrid failures, such as open circuits, bad connections, or wrong low voltage supplies. In addition, the FHIT board has to perform a calibration of the DCU chip.

In order to provide a compact test facility, all boards needed are enclosed in a metallic box depicted in figures 5.9(a) and 5.9(b). Two FE hybrids can be plugged onto the top of the box easily via specific transition boards allowing the connection of each type of hybrid to the FHIT system.¹⁷ On the front panel of the dual-FHIT box two START buttons (one button per hybrid) and two global result LEDs are located while the top side houses four additional LEDs intended to indicate the system and test status.

Two connections between the PC and the FHIT are required to control and monitor the test results. The RS232 serial port is used to access the FHIT boards whereas the SRDPC bus connection is needed to operate the ARC board (as described in section 5.1.3). FHIT requires a power supply providing +5 V, +12 V and –5 V DC voltages.

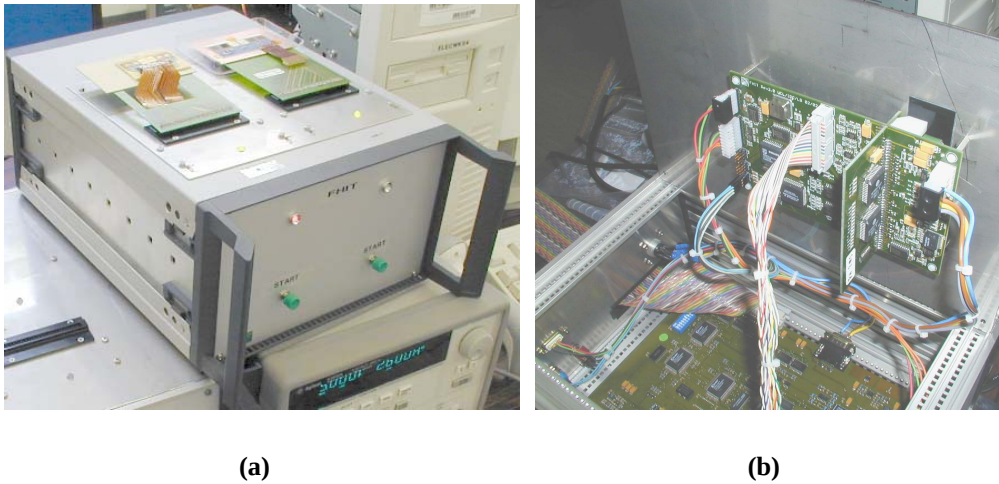


Figure 5.9: Front End Hybrid Industrial Tester FHIT. (a) Dual-FHIT with two plugged FE hybrids. (b) Mono-FHIT with a single FHIT board (top) and an ARC board (bottom).

Source: [71]

¹⁷Since the NAIS connectors of the FE hybrids allow only a few connections, specific NAIS to ERNI transition cards will be plugged to every hybrid after its assembly to provide the hybrid connector from being damaged. Thus the present connectors on the top of the FHIT box have to be changed.

5.3 Test Environment

Crate

As mentioned above, the ARC board, the LED pulser LEP_16, and the high voltage module DEPP can be pushed into a standard 19" crate being equipped with a 1-to-1 transition backplane and an appropriate DC low voltage power supply. Figure 5.10 depicts such a crate with some ARC setup components inside. The backplane is connected to the PC via the 50 pin SRDPC bus cable. The usage of a crate provides a clear and safe keeping of the readout hardware.



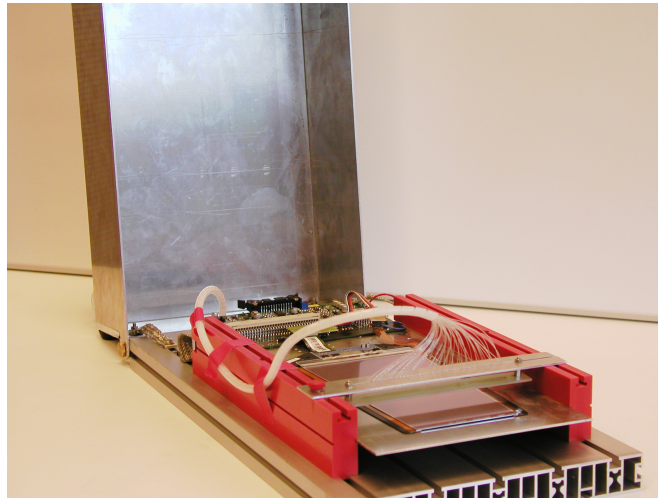
Figure 5.10: Crate equipped with one ARC board and one LED controller.

Storage and Test Box

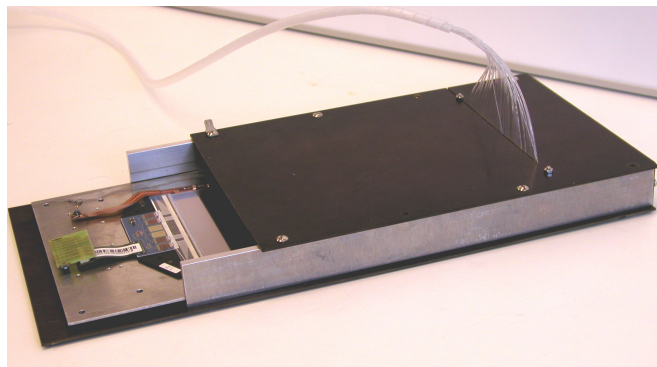
Since silicon detector modules are extremely sensitive to environmental conditions such as light, temperature, humidity, or electromagnetic fields, adequate *test boxes* had to be designed protecting the modules during the various testing procedures performed at different locations. Thus two kinds of test boxes were built to provide safe module operation on a desk at ambient temperature, the *ambient temperature test box*¹⁸, or optionally at low temperatures, the *cooling test box*. These boxes are depicted in figures 5.11(a) and 5.11(b).

¹⁸This box is designed by J. Olzem and built in the workshop of the I. Physikalisches Institut B.

Although the boxes are used for different purposes, both box layouts are based on similar principles. Modules which are mounted on a rigid aluminium plate, the *module carrier*, are pushed into a guide rail while the optical fibre array can be adjusted in a few millimeters distance to the sensor surface in order to illuminate the module. In case of the ambient temperature test box, the fibres are kept movable along the detector length. This feature is not suitable for test boxes intended to be pushed into a cooling box. Thus the fibre array has to be fixed onto the top plate of the cooling test box. Due to thermal contact aspects, the two guide rails of a cooling test box are realized in aluminium material.



(a)



(b)

Figure 5.11: Module test boxes: (a) the ambient temperature test box with the dimensions $13\text{ cm} \times 25\text{ cm} \times 48\text{ cm}$ and (b) the cooling test box with the dimensions $3.5\text{ cm} \times 19.5\text{ cm} \times 42\text{ cm}$.

Cooling Box

Even a low temperature system, such as the CMS tracker, will require maintenance at ambient temperature at some time. Thus impacts on hybrids and modules concerning warm up periods have to be simulated and reviewed very carefully. For this reason two phases of temperature cycling are planned during the tracker production at hybrid and at module level. In general, cool down and warm up phases give information about the quality of the bondings due to the mechanical stress applied to the bond wires while varying their temperature. Low temperature measurements mainly validate the electrical functionality of the ASICs or the hybrid and show the detector behaviour at simulated CMS environment conditions ($-10\text{ }^{\circ}\text{C}$).

Thus a specific temperature controlled test box has been built at Aachen [72]. This *cooling box* is suited to house up to five silicon detector modules stored in their test boxes. The basic structure is defined by an aluminium cage covered with insulating ROHACELL¹⁹ (5 cm thick) and rigid PVC²⁰ plates (0.5 cm thick) building a volume of about 60 liters. A special nitrogen inlet is used to flush the closed box, in order to provide controlled low humidity conditions. Both top and bottom plates of the cage provide 5 cm wide guide rails that facilitate the slide-in of the cooling test box shown in figure 5.11(b) as well as their thermal contact to the cooling sources.

Two *peltier elements*²¹ are mounted directly onto both plates. By this means the cooling system takes advantage of the so-called *peltier effect*²² which provides a simple way to regulate cooling systems. In general, the temperature produced by a peltier element can be affected by varying the current fed to the element while keeping the applied voltage constant. A simple change of polarity results in the change of a cooling into a heating effect or vice versa.

The chosen peltier elements can be operated at 24 V DC with a maximum nominal current of 14.2 A thus producing a large amount of heat on their warm sides. As a consequence, the dissipated heat has to be removed efficiently. For this reason the elements are realized as a so-called *direct-to-liquid system* which means that an external liquid (e.g. water) can be connected to the elements taking over the created heat. In fact, the efficiency of a peltier element depends on the difference ΔT between the liquid's temperature and its cool side's temperature thus affecting the net cooling power. Using the institute's infrastructure, a closed circuit delivering water with constant temperature of about $10\text{ }^{\circ}\text{C}$ has been chosen to flush the peltier elements. Thus an envisaged cooling temperature of $-20\text{ }^{\circ}\text{C}$ leads to a cooling power of about 160 W per peltier element. Pictures of the test box are depicted in figures 5.12(a) and 5.12(b).

Several Dallas DS1820 temperature sensors (resolution: $0.5\text{ }^{\circ}\text{C}$) [75] are positioned at various places. From the testing point of view the temperature near the silicon module is most interesting (see section 2.2.1), since it has to be used for regulation purposes. Therefore one sensor is fastened directly to the module carrier plate. Additional

¹⁹Polymethacrylimide (PMI) hard foam [73].

²⁰PolyVinyl Chloride.

²¹Type DL-290-24-00-00-00 produced by Supercool [74].

²²DC current through a junction of two different metals or semiconductors leads to a temperature difference which can be used for heating or cooling purposes (observed in 1834 by J. C. A. Peltier).

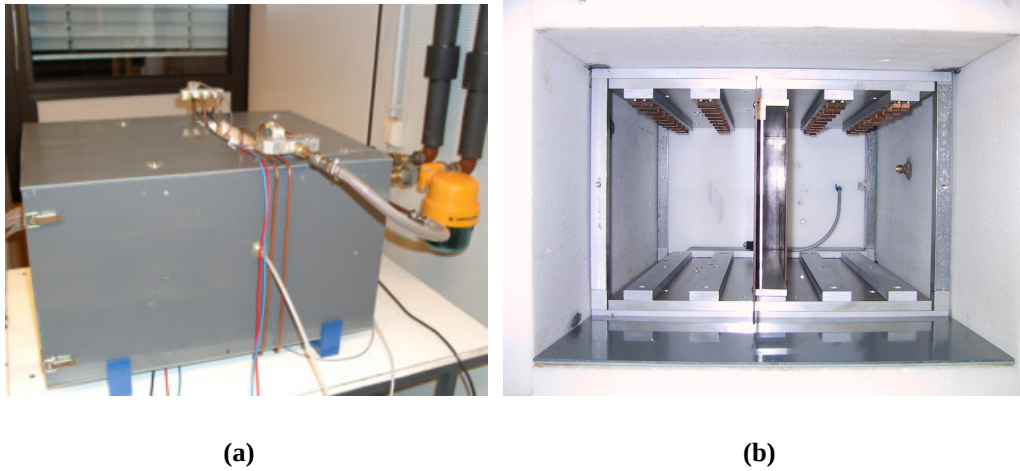


Figure 5.12: Cooling box. (a) Outer box with connection of the peltier elements to the closed water circuit. (b) Inner box with aluminium cage and empty test box inside.

temperature sensors are installed to measure the temperatures inside and outside the cooling box.

In particular the water inflow and outflow temperatures as well as the temperatures of the warm side of each peltier element give information about the box operation. Unexpected temperature increases or decreases give rise to an alarm with adequate reactions concerning peltier powering, water or N_2 flushing. It is clear that a proper *interlock system* is needed to prevent the test objects from being damaged. In addition to the mentioned software based temperature supervision, an external moisture watchdog connected to a magnetic valve is used to observe and control the water circuit. In case of a pipe burst, the water flow can be disconnected immediately by closing the valves.

Since humidity affects the electronics and the silicon part of the detector, this aspect also has to be controlled regularly. It is realized with a humidity sensor²³ which is located near the temperature sensor at the carrier plate. In practice, the cooling procedure is started after reaching a relative humidity value well below 10% at an environment temperature of about 12 °C which is slightly above the temperature of the peltier's cooling liquid. Thus the dew-point is about −19 °C.

Peripheral Devices

To provide the currents required to operate both peltier elements in parallel, a specific laboratory power supply²⁴ is used ($I_{max} = 33\text{ A}$, $V_{max} = 33\text{ V}$). Since this power supply provides an RS232 connection, a simple way of communication between the device and a PC is guaranteed. An automated temperature regulation of the cooling system can be envisaged.

In order to regulate and control the cooling box via software, a specific serial interface, called *COOLI* [78], was developed. This interface is a multitask device equipped

²³Type HIH-3610 from Honeywell [76].

²⁴Type XHR 33/33 from XANTREX [77].

with the following features:

- A serial controller provides the input/output (I/O) connection to a standard PC.
- The read out of the Dallas DS1820 temperature sensors is supported by a specific Dallas one-wire interface.
- A serial slave I/O interface is used for the remote control of the laboratory power supply. It receives echo characters from the serial controller I/O interface and forwards them to its output port.
- Devices supporting an analogue remote control (e.g. some power supplies) can be connected to an analogue output. This feature facilitates COOLI to be used in other cooling devices. With respect to the cooling box, the used humidity sensor is linked to the analogue input part.
- An additional feature of the cooling controller is represented by a digital I/O interface.²⁵ It allows to control external devices, such as a pressure controller.
- A polarity switch (30 A, 50 V) provides the change of the voltage sign applied to the peltier elements. Thus the decision about cooling or heating the box is left to the user or to the regulator, respectively.
- From the safety point of view a special hardware interlock system has been implemented. A watchdog timer controls the access of the serial controller port (each access resets the timer). If the watchdog times out after 1.5 min because of a disconnection of the data transfer, the peltier elements are switched off and the controller interface goes into idle mode. This prevents the peltier elements from being overheated while being uncontrolled due to a PC crash, for instance.

5.4 General Concept of the Readout Software

The development of a qualification software package needs an appropriate design concept. In general, the tasks of such kinds of software include the readout and control of various testing devices and their peripheral extensions as well as data handling, such as data analysis and data storage. In particular the automation of testing procedures demands a combination of these tasks requiring modular and flexible software structures. Several basic questions have to be reviewed, in order to choose a suitable strategy:

- Which object has to be tested or qualified?
- Who will use the software package?
- What kind of tests have to be done?

²⁵This feature has not been used in the Aachen cooling box environment.

5.4.1 Fields of Application

Figure 5.13 gives an impression of the main fields of application concerning the ARC system and the cooling box within the flow of the CMS module production. The usage of the ARC system starts already in industry in form of the FHIT system in order to allow a fast control of the FE hybrid manufacturing. A more detailed hybrid qualification is done at the *Hybrid Assembly and Qualification Centres* where the pitch adapters are assembled to the hybrid. This composition is then tested deeply, including extended temperature cycles. Afterwards the FE electronics is sent to the *Module Assembly Centres* which have to glue sensors and FE electronics onto the support frame. At this stage only fast hybrid tests are planned. The *Module Bonding and Qualification Centres* accomplish all electrical connections needed making a CMS silicon detector module operable. The ARC system is used to read out and test a complete module for the first time in the production chain. All hybrid and module tests mentioned are scheduled to last only a few minutes in total which is contrary to the tests during the next production step. The modules are shipped to *Long Term Test Centres* where the long term stability of each detector has to be validated. The testing time is scheduled to take one to three days based on a temperature cycled environment. At this stage the cooling box comes into operation.

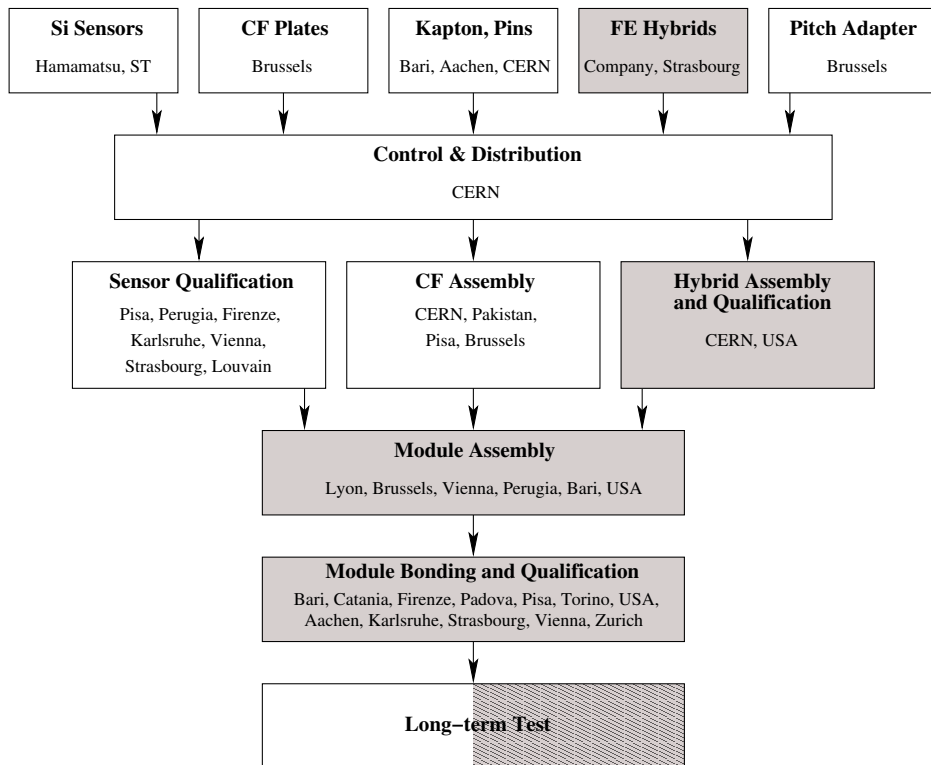


Figure 5.13: Silicon detector module production network. Gray-coloured boxes indicate fields of ARC application while the gray shaded box shows also the use of the cooling box. In some institutes an other test setup, which components are partially similar to the final CMS tracker readout system [79], is used during the long term test.

Due to the various types of production centres, the accompanying test setup has to provide compact hardware structures as well as specialized diagnostic software. In particular the software has to cope with individual requirements arising at the different production steps.

5.4.2 Operator Demands

The large number of modules to be produced involves many institutes and companies as well as many operators which have to be trained differently. This demands an automated software package which is convenient and simple to use. Thus the software has to provide a user-friendly graphical interface²⁶ guiding the operator from the beginning of the test to the final result output demanding only a few actions. In this *automated test mode* deep knowledge about the test object is not expected from the operator.

Ideally, a test software is not only suited for untrained users, but also for experts. In the case of a module or hybrid failure during the automated test, an expert should be capable of performing detailed diagnostic tests while using the same test environment. Thus individual advanced diagnostic procedures also have to be available. Moreover, the *expert mode* provides the software usage also during earlier research and development phases of the hybrids and modules.

5.4.3 Basic Elements of the ARC Software

The software package designed to operate the ARC system is called *APV Readout Controller Software (ARCS)* [80]. ARCS is built-up of two different programming languages: LabVIEW and C/C++.

LabVIEW [81] is a widespread programming tool developed and supported by National Instruments that provides an appropriate development environment for advanced graphical user interfaces. Buttons, displays, simple data conversions, or data flow structures can be implemented in an easy way. Thus LabVIEW 6.i has been chosen to evolve the GUI of ARCS. Although LabVIEW is a licensed software package, a so-called *run-time engine* is distributed by the producer without license fees which enables the use of executable files built with the LabVIEW application builder. By this means expensive license fees for each test centre are avoided. But the usage of this run-time engine limits the software platforms being suitable to WINDOWS 9x, NT/2000, or XP distributions.²⁷

Hardware access routines and calculation algorithms are realized in the C++ language. Since C++ provides flexible software structures, it can be implemented easily in different kinds of software packages. Unfortunately, C++ can not be embedded directly in LabVIEW code. Thus C++ methods have to be called from a specific C based interface. This interface includes all needed C++ methods in form of C functions.

The complete C/C++ source is compiled to a WINDOWS specific *dynamic link library (dll)* which is accessible by LabVIEW.

²⁶Graphical User Interface, GUI.

²⁷The portability of ARCS to WINDOWS NT/2000 was studied and successfully performed at Fermilab.

The integration of C++ routines into the ARC software project allows the incorporation of additional foreign C++ algorithms or libraries, such as *ROOT* [82] or *XERCES* [83]. While *ROOT* is a powerful data analysis framework providing advanced data handling tools, *XERCES* provides *XML*²⁸ parsing and generation. Some aspects of these software packages will be described in section 6.3.

Program Sequence

The ARC software is subdivided into five main parts, called *monitoring*, *fast tests*, *deep tests*, *all tests*, and *TCP/UDP*²⁹. Figure 5.14 shows the screen that appears when the primary initialization phase (including the PSRDPC bus, the I²C bus, and the readout chips) has been completed successfully.

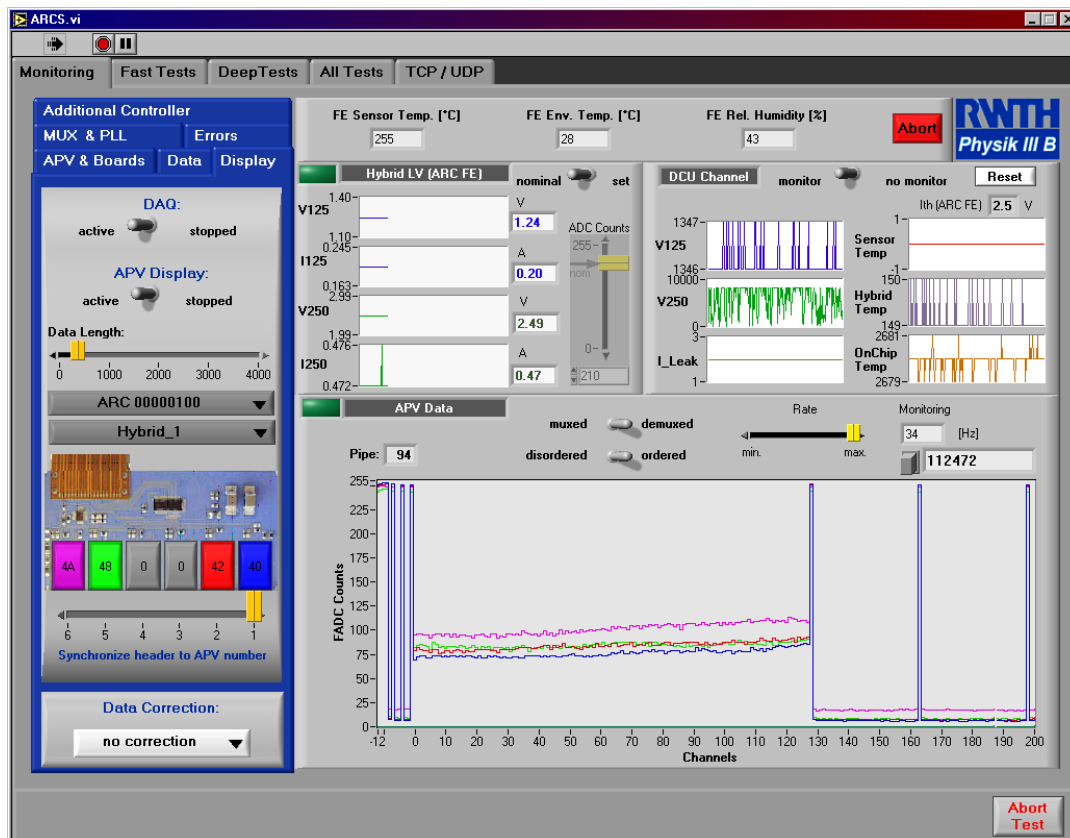


Figure 5.14: Screen-shot of the graphical user interface of ARCS during the monitoring phase. The five main parts of ARCS are accessible via separate index cards located at the upper left corner.

²⁸The EXtensible Markup Language is a simple, very flexible text format derived from SGML (ISO 8879). Originally designed to meet the challenges of large-scale electronic publishing, XML is also playing an increasingly important role in the exchange of a wide variety of data on the world wide web and elsewhere.

²⁹Transmission Control Protocol / Users Datagram Protocol.

Several functions and properties of the connected test object are displayed on-line. In particular the APV frames (bottom right window), the DCU measurements (top right), as well as the low voltage supplies and the corresponding current consumptions (top left) give a first clue about the status of the test object. Apart from the monitoring feature, advanced settings and parameters are accessible via this panel. For instance, the MUX, PLL, and APV command registers can be adjusted, the trigger pattern is selectable and some ARC properties can be fine-tuned. A detailed description can be found in [80].

The *fast tests* are meant to provide fast, standardized procedures in order to test the basic functionality of a hybrid. These tests can be performed without special knowledge about any operational aspects. The *deep test* panel enables an expert as well as a non-trained operator to do various automated tests, such as pedestal, noise, and calibration measurements. Both fast tests and deep tests will be discussed in detail in chapter 6. In order to provide full automation concerning large-scale assembly and testing, a panel called *all test* is implemented in ARCS. An individual list of test procedures defined in the deep test scenario can be composed and finally performed sequentially. By this means various production centres can use the same software package although requiring individual test procedures and settings.

Finally, a specific *TCP/UDP* software interface is incorporated in ARCS. It is intended to access external software applications in order to exchange information or data. The interface is used to connect the cooling box software *ACDC*³⁰ [84] to ARCS. Figure 5.15 presents a screen-shot of ACDC during the temperature regulation.

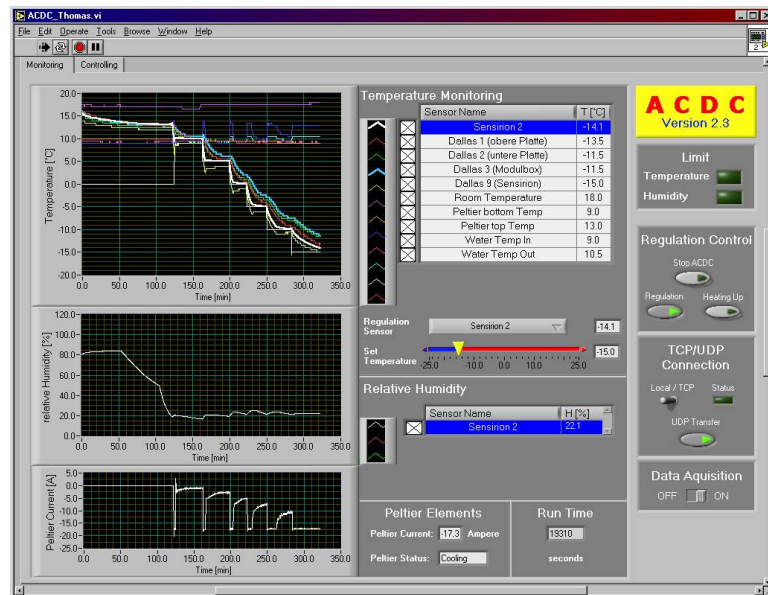


Figure 5.15: Screen-shot of the ACDC graphical user interface (version 2.3). ACDC allows the monitoring of all temperatures, the relative humidity, and the peltier element currents.

³⁰Aachen Cooling Device Control.

The TCP protocol allows the transmission of the nominal regulation temperature from ARCS to ACDC whereas the UDP protocol supports the reception of temperature and humidity data sent from ACDC to ARCS. As a result, a long term module test can be established in a simple way using the communication between both applications. In this scenario, ARCS controls only the aimed module environment temperature and receives the actual temperatures. ACDC supervises the complete cooling box parameters and accomplishes the regulation circuit³¹ independently from the ARC software. This guarantees that in case of an unexpected shutdown of the ARCS application, the cooling software keeps controlling the cooling box thus improving the operational reliability of the test facility. Figure 5.15 depicts a screen-shot of the ACDC software which is completely LabVIEW 6.i based.

³¹The implemented regulation circuit is a *Proportional-Integral-Derivative (PID)* regulation.

Chapter 6

Development and Implementation of Test Procedures

Apart from the graphical user interface and the ARC hardware access routines, most efforts were spent on the development of appropriate test procedures and their implementation into the ARC software. The test procedures presented in this section comprise the present status of measurements that are planned during the hybrid and module assembly phases [85]. Each part of the qualification assurance will be discussed in detail while special attention is paid to the following points:

- characteristics and prospects of the measured quantity,
- measurement procedure,
- interpretation of the data samples, and
- assessment criteria.

Moreover, the sensitivity of each test with respect to failure identification and the correlations of various tests is considered. Based on these aspects, appropriate fields of application within the production chain are proposed according to figure 5.13.

The various test procedures and their prospects are evaluated on the basis of measurements performed with TEC FE hybrids and wedge-ring-6 silicon detector modules using the ARC setup as described in section 5.

Object Identification

In order to keep track of the different module components assembled during the large-scale production, specific identification numbers are used to mark each object. For instance, FE hybrids are labeled with one-dimensional 14-digit *bar codes* which are composed of three parts (see figure 6.1).

The leading number 302 identifies the object as a part of the CMS tracker. The following four digits, called *part number*, define the hybrid type (see table C.1 for the numbering scheme) whereas the remaining seven digits build the unique hybrid identification number, called *part serial ID number*. To simplify matters, in this thesis the different test objects are characterized by specific abbreviations defined in table C.2.

	3	0	2	*	*	*	*	#	#	#	#	#	#	#
	CMS TK			Part Number				Part Serial ID Number						

Figure 6.1: Bar code scheme established for hybrids.

Channel Numbering Scheme

The convention for readout channel numbering follows the physical location of strips on the silicon sensors as presented in figure 6.2. This scheme is the same for all module geometries, although the sensor specific strip numbering etched on the surface (see figure B.3(a)) might be different. According to the APV manual [55], the APV readout channels are also numbered in physical order from 0 up to 127. The observance of a standardized numbering scheme is crucial to guarantee a unique diagnostic and repair procedure of faulty channels throughout the various test centres.

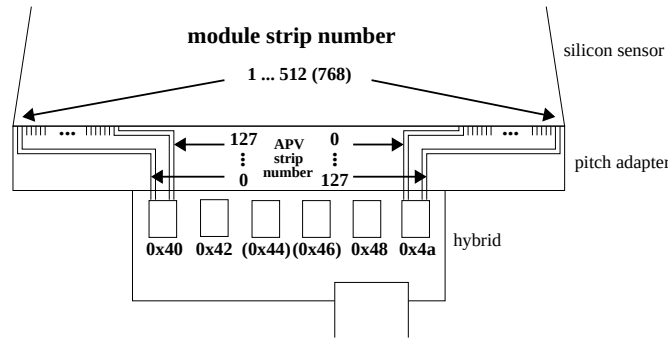


Figure 6.2: Numbering scheme for APV and module data. The assignment of the APV I²C addresses on the hybrid relative to the sensor is also shown. The parentheses indicate the vacant positions in case of hybrids equipped with four APV chips.

Assessment Strategies

The assessment of a hybrid or a module depends in particular on the behaviour of individual readout channels. A channel is denoted as a *regular channel*, if it shows the expected signature according to the measurement performed. Otherwise the channel is marked as a *bad channel*.

To simplify the automated test procedures and data interpretation, the assessment strategies should be as common as possible thereby being efficient in spotting failures. The experience of various hybrid and module measurements shows that in most cases so-called *linear thresholds* are sufficient to distinguish bad channels from regular channels. Linear thresholds are fixed values to which each measuring point DAT_i of a data sample based on N elements is compared.

The simplest strategy to assess an individual measuring point DAT_i which is assigned to channel i , for instance, is given by the comparison of the value DAT_i with *absolute thresholds*. The minimal condition is called CUT_{abs}^{min} whereas CUT_{abs}^{max} de-

defines the maximal allowed value. Thus a channel is marked as bad, if one of the following conditions is true:

- $DAT_i < CUT_{abs}^{min}$ or
- $DAT_i > CUT_{abs}^{max}$.

This type of assessment demands a sufficient knowledge about the data levels expected for regular channels. This is a tight demand on the test systems at different locations, since even slightly varying operation conditions or the usage of different peripheral devices (e.g. low and high voltage supplies) can cause different test results. Thus a reliable cross calibration throughout the various test centres has to be guaranteed in order to keep the measurements and the used thresholds as unique as possible.¹ In this sense it is recommended to use the absolute cuts in combination with conditions that depend less on the local test environments.

Assuming a data sample composed of N measuring points DAT_i , the mean value $\overline{DAT}$ is then calculated as given in equation 6.1.

$$\overline{DAT} = \frac{\sum_{i=k}^{N+k-1} DAT_i}{N}, \quad (6.1)$$

where k defines the first data point of the sample.

$\overline{DAT}$ can be used to define conditions that separate conspicuous values from normal (expected) values. A channel i is referred to as regular channel, if the following condition is true:

$$\overline{DAT} - \Delta < DAT_i < \overline{DAT} + \Delta, \quad (6.2)$$

where Δ is a constant value defining the outer limits of the tolerable value range. Typically, Δ is defined by one of these evaluations:

- $\Delta = CUT_{perc} \cdot \overline{DAT}$,
where CUT_{perc} is a number between 0 and 1. In this case Δ is a *percentage threshold* with respect to the mean value.
- $\Delta = CUT_{rms} \cdot RMS$,
where RMS is the standard deviation from the mean value $\overline{DAT}$ calculated by equation 6.3.

$$RMS = \sqrt{\frac{\sum_{i=k}^{N+k-1} (DAT_i - \overline{DAT})^2}{N - 1}}. \quad (6.3)$$

Therefore CUT_{rms} defines the number of standard deviations a measured value may differ from the mean value (*RMS threshold*).

In order to avoid undesired contributions from bad channels shifting the mean value as well as the standard deviation, a two-stage data assessment is performed. In the first step a pre-selection of probable bad channels is done on basis of the RMS threshold

¹At present a so-called *cross calibration* of all ARC setups used in the CMS tracker collaboration is under way. See [86] for details.

condition where CUT_{rms} is set to three standard deviations and the complete data set is used to calculate $\overline{DAT}$ and RMS . Those channels marked as bad are not considered in the second re-calculation procedure. Thus the received quantities are called *truncated mean* $\overline{DAT}_{trunc}$ and *truncated RMS* RMS_{trunc} , consequentially.

The adjustment of the four parameters CUT_{abs}^{min} , CUT_{abs}^{max} , CUT_{perc} , CUT_{rms} is a crucial aspect in the qualification procedures of the hybrids and modules. The determination and optimization of these cut parameters depends on a statistically significant number of measurements and therefore on an appropriate number of test objects.

Basic Operation Conditions

In order to bias the modules, a high voltage power supply from C.A.E.N.² is used. This supply provides up to 3 mA for a voltage range between 0 to 3 kV with an adjustable safety maximum of the current delivered (resolution of 1 μ A).

Since the current resolution of the high voltage power supply is limited, a specific *current monitor (CUMO)* is used [88]. The CUMO is a NIM module intended to monitor currents between 1 nA and 200 μ A at a voltage level of up to 7 kV. The current can be measured in four ranges (0 – 200 nA, 0 – 2 μ A, 0 – 20 μ A, and 0 – 200 μ A).

If not mentioned explicitly, all measurements shown in this thesis are performed at ambient temperature and with ASICs running with default values as defined in table 6.1.

Register	Default Value
IPRE	98
IPCASC	52
IPSF	34
ISHA	34
ISSF	34
IPSP	55
IMUXIN	34
ICAL	29
VFP	30
VFS	60
VPSP	40
CDRV	254
CSEL	1
LATENCY	4
MUXGAIN	4

Chip	Settings
APV	MODE=43 preamp polarity: inverting readout frequency: 20 MHz readout mode: peak calibration inhibit: off trigger mode: 1-sample analogue bias: on
APVMUX	resistor bits 0,1: on
PLL	trigger delay: 0 phase shift: 0

Table 6.1: Standard chip settings: (left) APV default settings based on [44] and (right) ARC specific standard settings.

²Type Mod. N126 [87].

6.1 The Advanced Test Procedures

The APV analogue data output is converted into ADC counts by the ARC board providing an 8-bit resolution. The ADC values obtained are called *raw data* representing the most pristine data sample within the analysis chain. For a certain channel i at event³ n the ADC level is referred to as RAW_i^n . Figure 6.3(a) shows the raw data of a single event obtained from a module equipped with four APVs whereas figure 6.3(b) presents the superposition of 10,000 raw data samples. The width of the black band indicates the fluctuation of the raw data per readout channel from event to event. This effect will be interpreted in section 6.1.3 as noise with respect to a certain mean value. Some channels are characterized by a wide spread thus being called *noisy channels*. Figure 6.3(b) illustrates that each APV owns an individual data distribution. As a result, the data assessment strategy described above is usually applied APV-wise.

In order to extract relevant information from the raw data, such as a charge signal S_i^n , distortions mainly caused by the electronics have to be considered and compensated. Those distortions are discussed in the following sections.

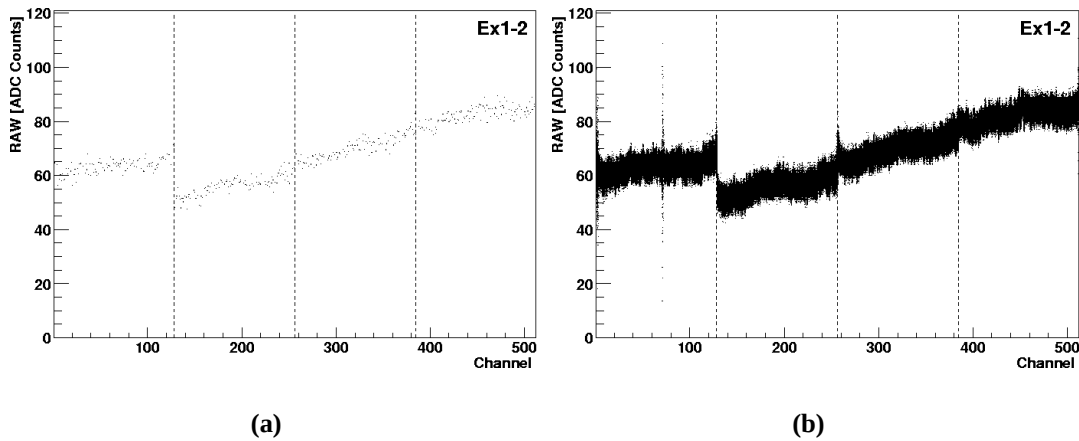


Figure 6.3: Raw data samples of module Ex1-2: (a) A single event. Each point corresponds to a certain module channel. (b) 10,000 raw data events superimposed. The dashed lines indicate the APV borders.

Test Characteristics

The typical duration of the raw data measurement and data storage is about 2 min for 10,000 events. The storage of raw data samples is not planned during any standard test program yet. Nevertheless, a raw data file contains un-corrected information about the test object and allows for a re-calculation of pedestal and noise data, for example.

³In the following “event n ” means the n^{th} event triggered.

6.1.1 Pedestal

When no signal is applied to the chip, each channel ideally should output the same ADC level. However, due to mismatching of devices inherent in any ASIC technology, variations occur. These variations are described by the *pedestal* distribution representing the data *baseline*.

The pedestal PED_i for each channel i is defined as the average strip output level if no signal, caused by external or internal charge deposition, is present. Thus PED_i can be derived from a raw data sample based on N events as described in equation 6.4.

$$PED_i = \frac{\sum_{n=1}^N RAW_i^n}{N}. \quad (6.4)$$

Figure 6.4 depicts typical pedestal distributions obtained from a TEC FE hybrid which is equipped with four APV chips operated in peak and deconvolution mode. Each chip is characterized by its individual baseline. The slight pedestal gradient within the 128 channels of an APV is likely due to a power supply drop across the chip. The absolute pedestal height can be adjusted via the VPSP register, but the pedestal structure is an individual chip property. Depending on the measurement, the baseline has to be shifted in order to exploit most of the available ADC range. To avoid saturation effects, the minimum and maximum data levels may not reach 0 or 255 ADC counts, respectively. This aspect plays an important role during the external light tests and during the calibration pulse measurements to be described later.

The APV baseline measured in deconvolution mode is typically lower than the baseline obtained in peak mode while keeping all other APV command registers constant. This is due to the positive and negative weights ($w_1 = 1.0$, $w_2 = -1.759$, and $w_3 = 1.457$) used for the linear combination in the deconvolution method (see section 3.2.1).

Data Interpretation

The pedestal data are more or less insensitive to typical hybrid or module failures. Thus in the ARC software pedestals are mainly used for data correction and noise calculation purposes.

6.1.2 Common Mode Noise

Due to electronic noise pick-up at the preamplifier inputs, an event by event baseline shift occurs that is common to groups of neighbouring channels. This effect is called *common mode*. In addition to the pedestal correction, a common mode correction has to be applied to a raw data sample before an appropriate signal identification is possible. Equation 6.5 shows the calculation of the common mode noise CMN_g^n per event n and common mode group g as it is implemented in the ARCS analysis algorithms.

$$CMN_g^n = \frac{1}{N_{ch}} \sum_{i=g \cdot N_{ch}}^{(g+1) \cdot N_{ch} - 1} (RAW_i^n - PED_i), \quad (6.5)$$

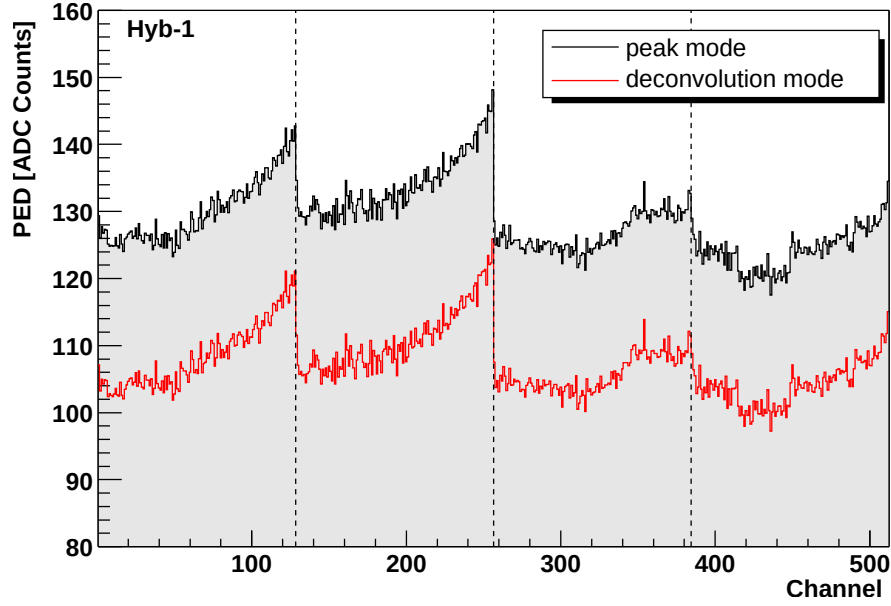


Figure 6.4: Typical pedestal data of a hybrid with four APVs (peak and deconvolution mode, inverter on). Data samples of different APV chips are separated by dashed lines.

where N_{ch} is the number of channels that are considered to be affected by the same common mode shift for each group g .

Since the analogue inputs of the APV chip are grouped in four blocks of 32 channels each, the common mode calculation in ARCS is ideally based on these four groups. This means that $g = 0, \dots, 3$ and $N_{ch} = 32$.⁴

Figure 6.5 presents the common mode distributions of a complete FE hybrid. Each sub-figure (corresponding to a certain APV chip) includes four common mode distributions according to four sub-regions corresponding to the different input groups. The sum of these distributions is also depicted in the figures. The data samples are fitted with a Gaussian function $f_{gauss}(x)$ parameterized in equation 6.6.

$$f_{gauss}(x) = \text{Constant} \cdot \exp\left(-\frac{1}{2} \cdot \frac{(x - \text{Mean})^2}{\text{Sigma}^2}\right). \quad (6.6)$$

Data Interpretation

The common mode distribution is an indicator for the actual measurement conditions. For instance, a bad grounding scheme will affect the distribution in terms of width of and deviation from the Gaussian shape. Apart from that, the common mode noise data of the four groups are used to correct the raw data samples in addition to the pedestal correction. An assessment of the common mode noise distributions is not planned yet.

Recent results on module tests show that a small common mode distribution is essential with respect to noise measurements and noise data interpretation [86]. This topic will be discussed in the next section.

⁴In early releases of ARCS (up to version 5.1) the common mode was not calculated group-wise thus using $g = 0$, $N_{ch} = 128$ (see section 7.1.2).

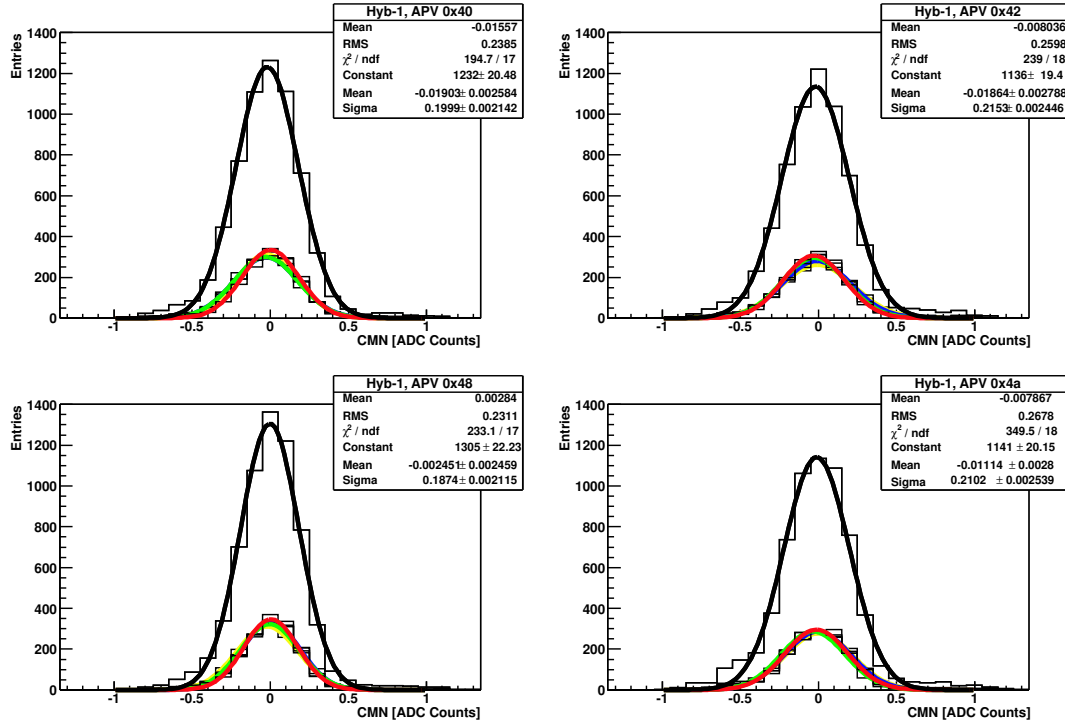


Figure 6.5: Common mode noise distributions (peak mode, inverter on). The small distributions (fitted lines in red, green, blue, yellow) indicate the four different common mode groups per chip whereas the large distribution represents the sum of those four sub-groups (the given fit parameters belong to the large distribution).

6.1.3 Raw Noise and Common Mode Subtracted Noise

The statistical fluctuation of the raw data per channel around its pedestal is named *raw noise*. Equation 6.7 defines the raw noise NOI_i^{raw} of channel i calculated on the basis of N events.

$$NOI_i^{raw} = \sqrt{\frac{\sum_{n=1}^N (RAW_i^n - PED_i)^2}{N - 1}}. \quad (6.7)$$

When the raw data is also corrected for common mode noise, the so-called *common mode subtracted noise* NOI_i is derived:

$$NOI_i = \sqrt{\frac{\sum_{n=1}^N (RAW_i^n - PED_i - CMN_{g(i)}^n)^2}{N - 1}} = \sqrt{\frac{\sum_{n=1}^N (S_i^n)^2}{N - 1}}, \quad (6.8)$$

where $g(i)$ represents the common mode of the group the channel i belongs to. S_i^n describes the *signal* of channel i at event n after the pedestal and common mode correction:

$$S_i^n = RAW_i^n - PED_i - CMN_{g(i)}^n. \quad (6.9)$$

As discussed in section 4.3, the deconvolution method implemented in the APV chips affects the noise performance of a hybrid or a module significantly. Parallel

noise is decreased after the deconvolution process while the series noise is increased. Since the parallel part of the APV amplifier noise contribute most to the total noise, a net increase of noise has to be expected when operating the chips in deconvolution mode. Compared to FE hybrids, modules suffer from additional noise sources such as leakage current and strip capacitance. Thus a slightly different behaviour of hybrids and modules should occur with respect to the noise measured.

Figure 6.6 depicts noise distributions obtained from a hybrid and a module operated in peak and deconvolution mode, respectively. Both test objects show no conspicuous readout channels. According to the Gaussian fits to the noise distributions depicted in figures 6.6(b) and 6.6(d), in peak mode the mean value of the common mode subtracted noise distribution is about 0.5 ADC counts for the hybrid and approximately 1.5 ADC counts for the module. The corresponding values when running the ASICs in deconvolution mode are 0.7 ADC counts for the hybrid and 1.9 ADC counts for the module. Thus in the present case, one measures a ratio $REL_{hybrid} \approx 1.44$ for the FE hybrid and $REL_{module} \approx 1.27$ for the module. These results represent typical observations matching the expectations described in section 4.3.

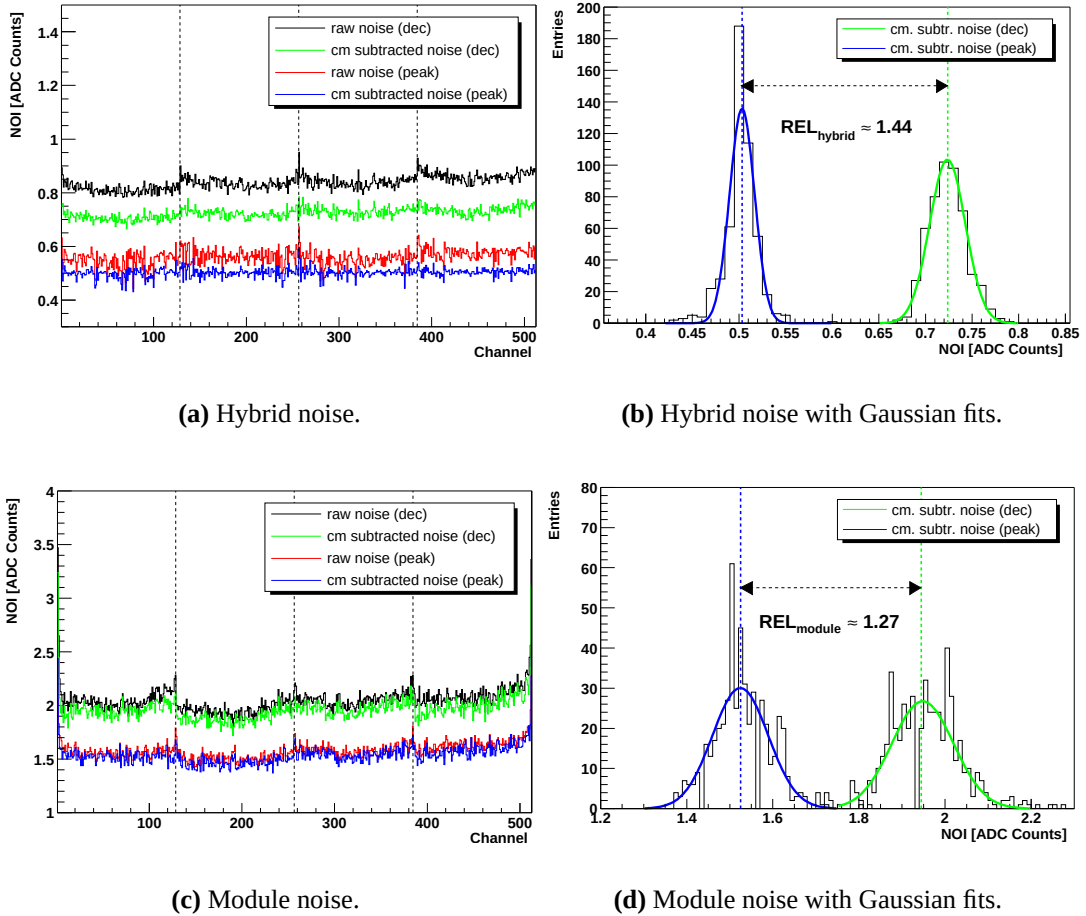


Figure 6.6: Channel noise distributions (raw noise and common mode subtracted noise) in peak and deconvolution (dec) mode obtained from a hybrid and a module.

Data Interpretation and Cut Strategies

The noise measurements are sensitive to all typical hybrid and module failures as discussed in section 4.2. Figure 6.7 depicts the results of module Mod-1 concerning raw noise and common mode subtracted noise. This module suffers from ten opens (channels 1, 65, 227, 232, and 237–242), two shorts (405/406 and 501/502/503), and one pinhole (57) distributed across the complete sensor. In the present case, opens show up with higher noise than regular channels whereas the pinhole and the shorts are characterized by lower noise values. Further conspicuous channels occur at the edges of the APVs, although these strips are not affected by any failure.

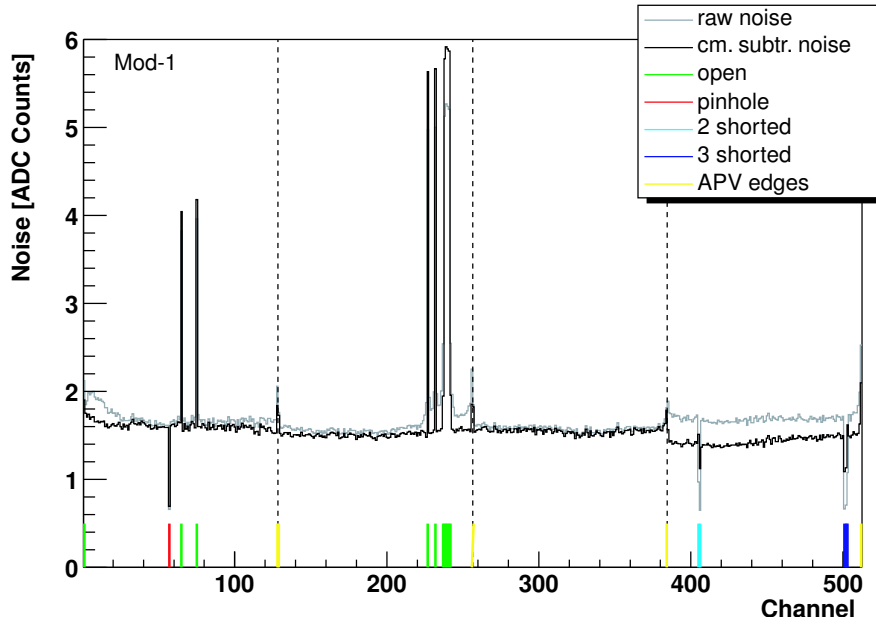


Figure 6.7: Noise distribution of a module showing all typical failures (the APVs are operated in peak mode with inverter on). Those channels deviating from the regular channel's signature are indicated by the coloured bars below the distributions.

The interpretation of noise signatures with respect to unique failure matching is complicated due to an APV on-chip common mode subtraction. This correction is caused by an external resistor $R(\text{external})$ located on the FE hybrid supplying power to the chip internal preamplifier output inverter stage (see figure 6.8). This supply is common to all 128 inverters in a single chip. As a result, a common mode signal V_{CM} appearing on the external resistor drives down the output of all channels. This kind of internal data correction affects also those channels with significantly less common mode noise than regular channels, e.g. open strips. Thus opens seem to behave noisier than regular channels.

As a consequence, the noise measurement is extremely sensitive to environmental conditions, such as grounding and external noise sources which affect the common mode noise of the detector. This indicates that there are certain levels of common mode noise that cause opens to have noise lower than, noise equal to, or noise higher than regular channels. Thus the interpretation of noise values has to be done carefully.

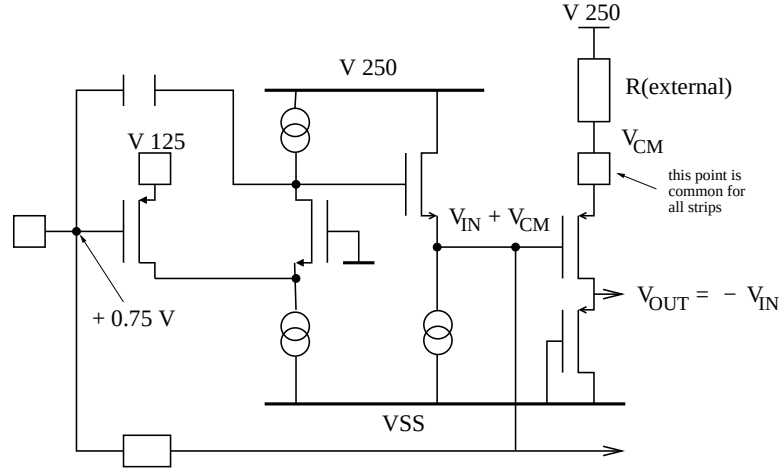


Figure 6.8: Schematic of the APV preamplifier and inverter stage ($V_{125} = 1.25$ V, $V_{250} = 2.5$ V, and $V_{SS} = \text{ground}$). Source: [89]

Recent noise measurements show that a common mode noise less than approximately 0.5 ADC counts is needed to provide the distinction of different failure types in a unique way [86]. In this case, open bonds occur always with lower noise values than regular channels. This matches the naive expectation that a lower total capacitance leads to lower noise which is based on equation 4.5 where the noise dependence from the total capacitance seen by the preamplifier is expressed.

If nearly no common mode noise is present, the APV internal common mode subtraction is negligible. In this case, the location of an open channel can be derived from the absolute noise height, since the total capacitance seen by the amplifier input is different with respect to sensor-to-sensor or sensor-to-pitch adapter failures (see equation 4.1).

In the case of low common mode noise another problem improves: the noise levels of the APV edges decrease or even equal the regular channel levels. As discussed in [90], an additional presumable explanation for the noisy APV edges is the instability of the bias ring ground. As a result, a low common mode noise along with good shielding will be important to get uniform test results over the production period.

In ARCS the common mode noise is used to determine readout channels showing conspicuous behaviour. In order to determine a bad channel with respect to its noise signature, a rather complex flagging strategy is implemented in the ARCS analysis routines⁵. In fact, the channel assessment is a combination of four different conditions checked on-line on the basis of N events. Thereby a channel i is masked as bad, if one of the following criteria is true:

$$\bullet D \cdot RMS_i^{NOI} < |NOI_i - \overline{NOI}|,$$

where D defines the number of standard deviations RMS_i^{NOI} , NOI_i may differ from the mean common mode subtracted noise $\overline{NOI}$. D is adjustable in a range

⁵For the sake of comparability of different test setups using different kinds of analysis software, the presented pedestal and noise calculations are based on C++ classes provided by V. Zhukov [79].

between 0 and 25. The calculation of RMS_i^{NOI} is given in equation 6.10.

$$RMS_i^{NOI} = \sqrt{\frac{\sum_{n=1}^N (NOI_i^n - \overline{NOI})^2}{N - 1}}, \quad (6.10)$$

with NOI_i^n being the common mode subtracted noise of event n .

- $NOI_i < NOI_{min}$ or $NOI_i > NOI_{max}$,
where NOI_{max} and NOI_{min} are cut conditions constraining the absolute noise limits accepted. The values may range between 0 and 10 and $NOI_{max} > NOI_{min}$.
- The next condition is based on event by event information where a channel i is assigned as a *noisy channel* at event n , if one of the following two criteria is true:

- $|S_i^n| > T \cdot NOI_i$,
- $|S_i^n| > T \cdot |\overline{S_i^n}|$,

where T is a cut condition adjustable between 0 and 25. $|\overline{S_i^n}|$ describes the mean signal of the corresponding APV. If $N_{noisy,i}$ is the number of events a certain channel has been flagged by one of the criteria described above, the following condition is used to assess channel i after N events:

$$\frac{N_{noisy,i}}{N} > P,$$

where P defines the fraction of the total number of events that is accepted to be flagged as noisy channel without being signed as a bad channel. The values of P may range between 0 and 1.

Test Characteristics and Cut Parameters

The pedestal, common mode, and noise data are determined in the same test procedure. The typical duration of one measurement is about 45 s for 5000 events. Every FE hybrid and module test program have to include the calculation of pedestal, common mode, and noise. The common mode noise can be used to evaluate the quality of grounding and shielding during the measurement. In ARCS, the assessment of all channels is done via the common mode subtracted noise which is sensitive to opens, shorts, and pinholes. A unique failure diagnostic depends extremely on the common mode noise. Thus a properly designed test environment used in every test centre is essential. The following cut parameters are suited to find bad channels with respect to their noise behaviour:

Noise Cut	Module	FE Hybrid
D	5.0	5.0
NOI_{min}	1.0 ADC counts	0.1 ADC counts
NOI_{max}	5.0 ADC counts	2.0 ADC counts
T	3.0	3.0
P	0.2	0.7

These cuts (and all other cuts mentioned at the end of each test procedure) were used to assess the express-line modules which will be discussed in chapter 7. The cuts represent the first attempt to characterize TEC modules. Recently, big efforts are spent on the final definition of cut strategies and thresholds to be used for TEC, TIB, TOB, and TID modules during the large-scale production [91].

6.1.4 Pipeline Test

Pedestal and noise measurements can also be used to inspect each single APV pipeline cell. Since the pipeline addresses are encoded in the APV data frames, a unique assignment of data per channel to the 192 columns is guaranteed. As a consequence, the pedestal and noise calculations given in equation 6.4 and 6.8 have to be extended by a column index j : $PED_{i,j}$, $NOI_{i,j}$. Thus 128×192 cells per APV have to be considered separately. This requires a large number of events in order to calculate the pedestal and noise values with statistical significance.

During the pipeline test procedure the LATENCY register is fixed to ten whereas the trigger pattern is defined by the sequence “10100000(spacer)00000001”. In order to access the different pipeline cells systematically, the spacer value (as introduced in section 5.1.1) is varied from 215 down to 24 in decrements of one. These values are equivalent to pipeline cell 192 and 1, respectively. N events are used to estimate pedestals and noise values per spacer setting.

Figure 6.9 presents pedestal data obtained from 1000 events per pipeline cell in form of a matrix. Each pipeline shows the typical pedestal structure with increasing values for increasing channel numbers.

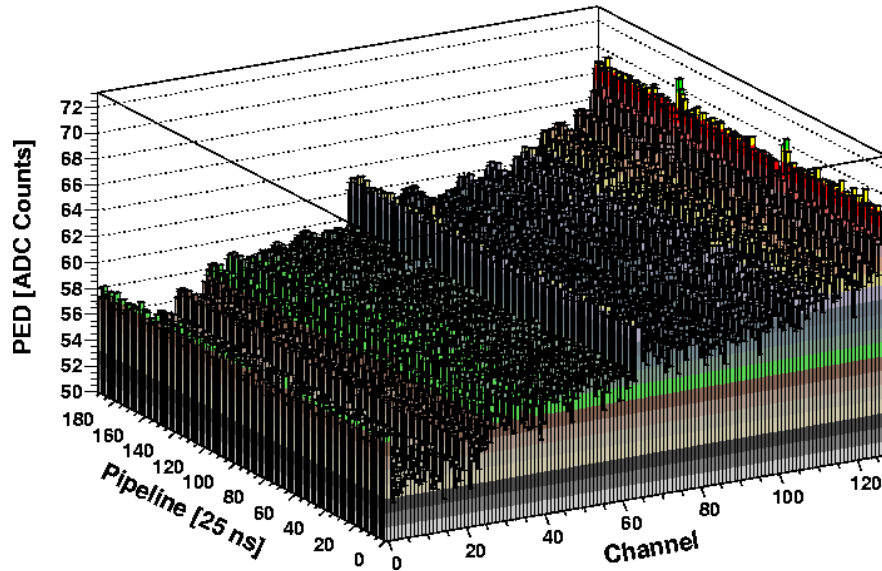


Figure 6.9: Pedestal pipeline data of a single APV. The pedestal structure along each pipeline has a typical form while the pedestal data for a certain channel show only small fluctuations along the pipeline columns.

Data Interpretation and Cut Strategies

The pedestal matrix can be used to check the uniformity of the pedestal data per pipeline column. Based on the matrix entries obtained, the mean pedestal value $\overline{PED}_j$ per column j is calculated via:

$$\overline{PED}_j = \frac{\sum_{i=0}^{127} PED_{i,j}}{128}, \quad (6.11)$$

while the corresponding standard deviation RMS_j^{Pipe} is defined by:

$$RMS_j^{Pipe} = \sqrt{\frac{\sum_{i=0}^{127} (PED_{i,j} - \overline{PED}_j)^2}{127}}. \quad (6.12)$$

Typical results for $\overline{PED}_j$ and RMS_j^{Pipe} are shown in figure 6.10. The mean standard deviation of the pedestal data along a certain pipeline is approximately 4.8 ADC counts. A faulty pipeline column f would occur with a large deviation of $\overline{PED}_f$ or RMS_f^{Pipe} from regular pipeline values.

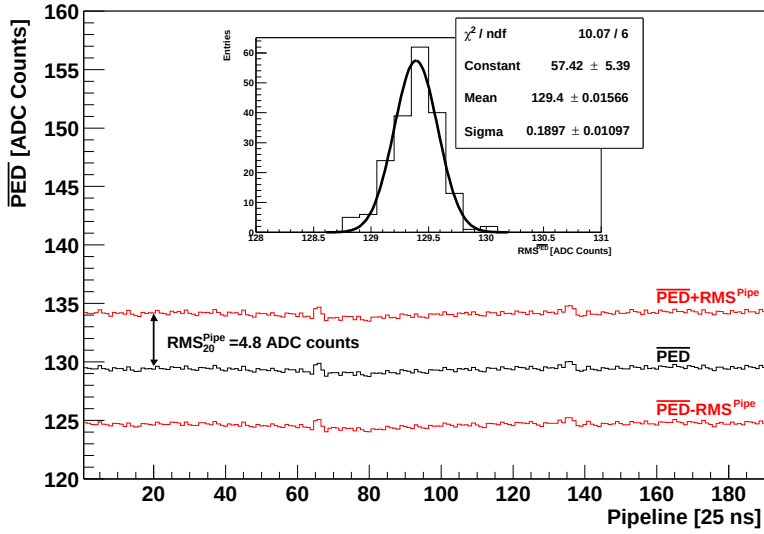


Figure 6.10: Mean pedestals $\overline{PED}_j$ per pipeline column j . The data range of one standard deviation is also shown (red lines). The sub-figure depicts the statistical distribution of the mean pedestal values revealing a small variation of about ± 0.2 ADC counts.

Since the pipeline scan uses the same analysis algorithms as described in section 6.1.3, the same advanced assessment criteria can be used. In particular the common mode subtracted noise provides the on-line assessment of every pipeline cell. Figure 6.11 shows a pipeline noise measurement revealing three bad channels. These channels are characterized by higher noise than regular channels along the complete pipeline.

The pipeline test is the most time consuming part of the measurements implemented in the ARC software. Thus this test procedure is only suitable for long-term tests where the total measurement time is a secondary aspect.

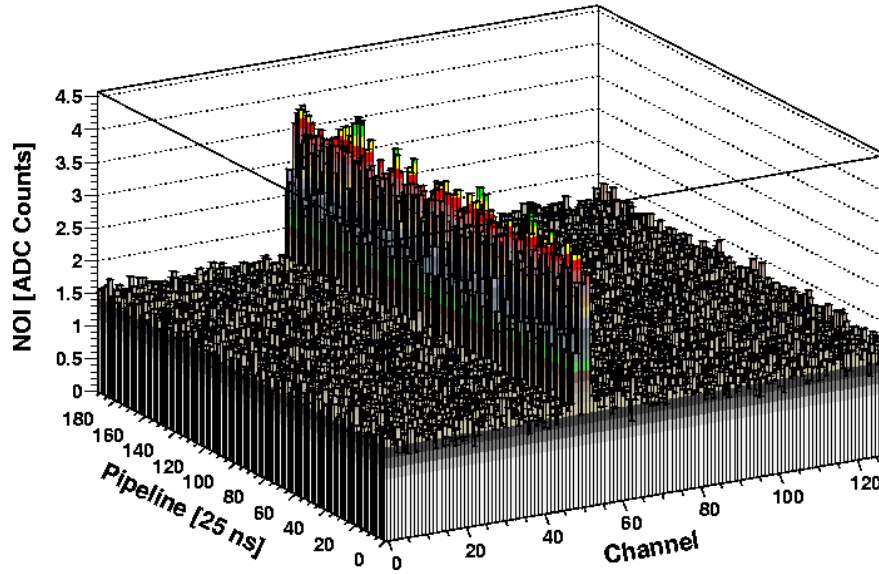


Figure 6.11: Common mode subtracted noise pipeline data. Three channels (48, 50, and 51) show significantly higher noise than regular channels. These channels were flagged as bad by the assessment procedure.

Test Characteristics

The pipeline test needs a significant number of events per pipeline cell. The duration of one measurement demanding 1000 events per cell is about 35 min. Thus the pipeline test is no official part of the planned test programs yet, but it could be incorporated in the long-term test scenario. In the case of a common mode subtracted noise measurement a bad pipeline cell has to be identified by the same advanced assessment criteria as described in section 6.1.3.

6.1.5 Calibration Pulse Shape Tests

The calibration pulse shape test makes use of the APV internal calibration circuit which is described in section 3.2. The test procedure is meant to check the following three aspects:

- functioning of the internal calibration circuit,
- observation of strip faults such as opens, pinholes, and shorts,
- deduction of the optimal sample time.

The test procedure provides a detailed scan of the calibration pulse shape, the so-called *latency scan*. The trigger pattern sent to the APV chips periodically is “11000000(spacer)00010011” while the spacer value is set to five in case of deconvolution mode or to eight otherwise. Since the measurement demands unipolar signals, two calibration requests are sent to the chips. The second request is not followed

by an event trigger. This dumps the signal of the alternated polarity (as discussed in section 3.2.1).

During the scan, the LATENCY value is increased by increments of one starting from LATENCY_{min} (the default value is one) and ending with LATENCY_{max} (the default value is 20). For each LATENCY value, eight fine delay settings with respect to the injection time of the calibration charge are adjusted consecutively in steps of 3.125 ns via the CSEL register. The CDRV register is used to access all eight calibration groups. To summarize, the following three registers are changed during the latency scan, if N is the number of events to be taken per measuring point:

- CDRV every N^{th} event,
- CSEL every $(8 \cdot N)^{\text{th}}$ event,
- LATENCY every $(64 \cdot N)^{\text{th}}$ event.

Every time the LATENCY value is changed, the actual baseline is re-calculated in order to provide a reasonable data correction.

The APV chip provides several command registers allowing modifications to the pulse shape, such as MODE, VFS, and VFP. In particular, the MODE register defines the polarity and the shape of the calibration pulse. The signal polarity depends on the chosen trigger pattern. In the automated pulse shape test implemented in ARCS, an inverter stage which is switched on is accompanied by a negative polarity. The ARC software provides the following MODE register settings affecting the signal polarity:

- MODE = 43 (peak, inverter on) $\rightarrow$ negative polarity,
- MODE = 11 (peak, inverter off) $\rightarrow$ positive polarity,
- MODE = 33 (deconvolution, inverter on) $\rightarrow$ negative polarity,
- MODE = 1 (deconvolution, inverter off) $\rightarrow$ positive polarity.

If the inverter is switched on, the VPSP register is adjusted to 25 in order to exploit the range below the baseline. On the contrary, VPSP is set to 43, if the inverter is switched off, thus enlarging the space above the baseline. To avoid overflow effects with respect to the 8-bit ADC range, the maximum injection charge allowed is $\text{ICAL} = 210$ which is equivalent to the deposited charge of approximately six MIPs.

Figures 6.12(a) and 6.12(b) show several pulse shapes for a certain APV channel while operating the chip in peak mode and in deconvolution mode, respectively. The VFS register affects the decay behaviour of the corresponding pulse significantly.

Data Interpretation

In order to extract essential information from the calibration pulses, basic shape characteristics have to be identified. The following shape properties will be used to assess the pulses (see figure 6.13 for illustration):

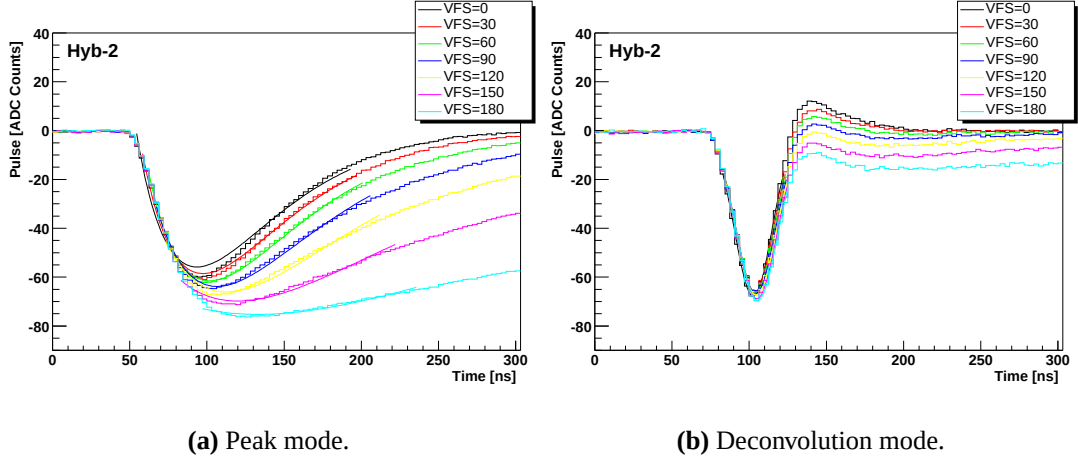


Figure 6.12: Calibration pulse shapes of a certain APV channel concerning different VFS values thereby operating the chip with the inverter stage switched on. The fit functions shown are defined in equations 6.13 and 6.14.

- *pulse baseline*: The baseline of a pulse is the level from which the pulse starts to evolve. Due to the pedestal correction applied, the calibration pulse baseline should be approximately zero.
- *pulse height* or *amplitude (PSH)* : The amplitude defines the height of the pulse measured from its extreme value to the current baseline value. In case of a signal with negative polarity, *PSH* is negative thus being the minimum value of the distribution. If the signal is positive, *PSH* is positive and represents the pulse maximum.
- *time offset (TO)*: The time offset defines the origin of the pulse with respect to the begin of the measurement.
- *peak time (PT)*: The time (with respect to the begin of the measurement) at which the pulse attains its extremal value is called peak time.
- *rise time (RT)*: The rise time is the time elapsed between the start of the pulse and the reach of its full amplitude.⁶ To simplify matters, the notation *RT* is also used for pulses with negative amplitude.

From the point of view of an automated test procedure, a robust and reliable extraction of the pulse information has to be guaranteed. Normally the determination of all pulse parameters is not necessary, since they reveal the same information. Two specific fit functions are incorporated in the ARCS analysis routines to characterize both kinds of shapes originating from peak and deconvolution mode operation.

⁶This definition is based on the fit function chosen for the measurements in peak mode (see equation 6.13). The function includes *RT* in form of a fit parameter.

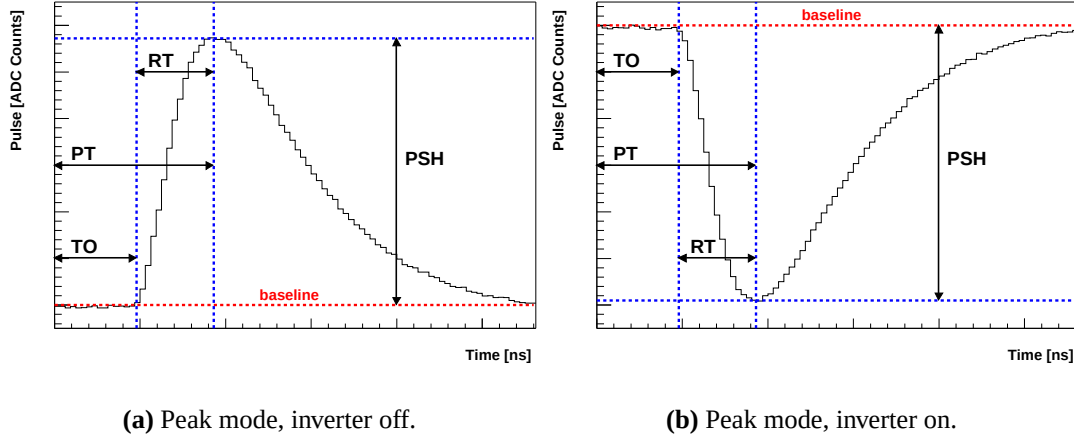


Figure 6.13: Pulse shape characteristics.

In case of peak mode, the pulse shape can be parameterized by equation 6.13.

$$f_{peak}^{shape}(t) = PSH \cdot \frac{(t - TO)}{RT} \cdot \exp\left(1 - \frac{t - TO}{RT}\right). \quad (6.13)$$

PT is deduced from TO and RT via $PT = TO + RT$.

In deconvolution mode the description of a small time range around the peak time can be done via a Gaussian function as given in equation 6.14.

$$f_{dec}^{shape}(t) = PSH \cdot \exp\left(-\frac{1}{2} \cdot \frac{(t - PT)^2}{\sigma^2}\right), \quad (6.14)$$

with σ being the standard deviation of the Gaussian function. In this case the rising time RT of the pulse is approximated by $RT \approx 2.3 \cdot \sigma$ (see figure E.1).

Figures 6.12(a) and 6.12(b) also include the fitted functions for the different pulse shapes after optimizing the parameters PSH , TO , and RT . In peak mode the fits are performed in a time range between $(PT - 40 \text{ ns})$ and $(PT + 100 \text{ ns})$ whereas in deconvolution mode the fit range is limited to $(PT \pm 20 \text{ ns})$.

Although the functions seem to fit the data well, the fit results obtained have to be assessed in terms of reliability and meaning. A detailed analysis of the VFS scan, shown in extracts in figure 6.12(a), reveals the limits of the fit procedures. Based on pulse shape information of 128 channels for seven different VFS register settings, the mean values of the fit parameters $\overline{PSH}$, $\overline{PT}$, and $\overline{RT}$ are determined. Figures 6.14(a) to 6.14(c) depict the dependencies of those values from the VFS settings. In addition, the same quantities extracted directly from the measurement are superimposed. As a result, the measured data agree with the fitted parameters at a 5% level with respect to the mean pulse heights and the mean peak times.

On the contrary, the difference between the fitted value for $\overline{RT}$ and the real rise time increases with increasing VFS values. The deviation becomes significant for $VFS \geq 120$ which is approximately 20% at $VFS = 120$ and 90% at $VFS = 180$.

Figure 6.14(d) shows two examples of fitted shapes for $VFS = 60$ and $VFS = 180$. The included fit functions are extrapolated to lower time bins. While one function

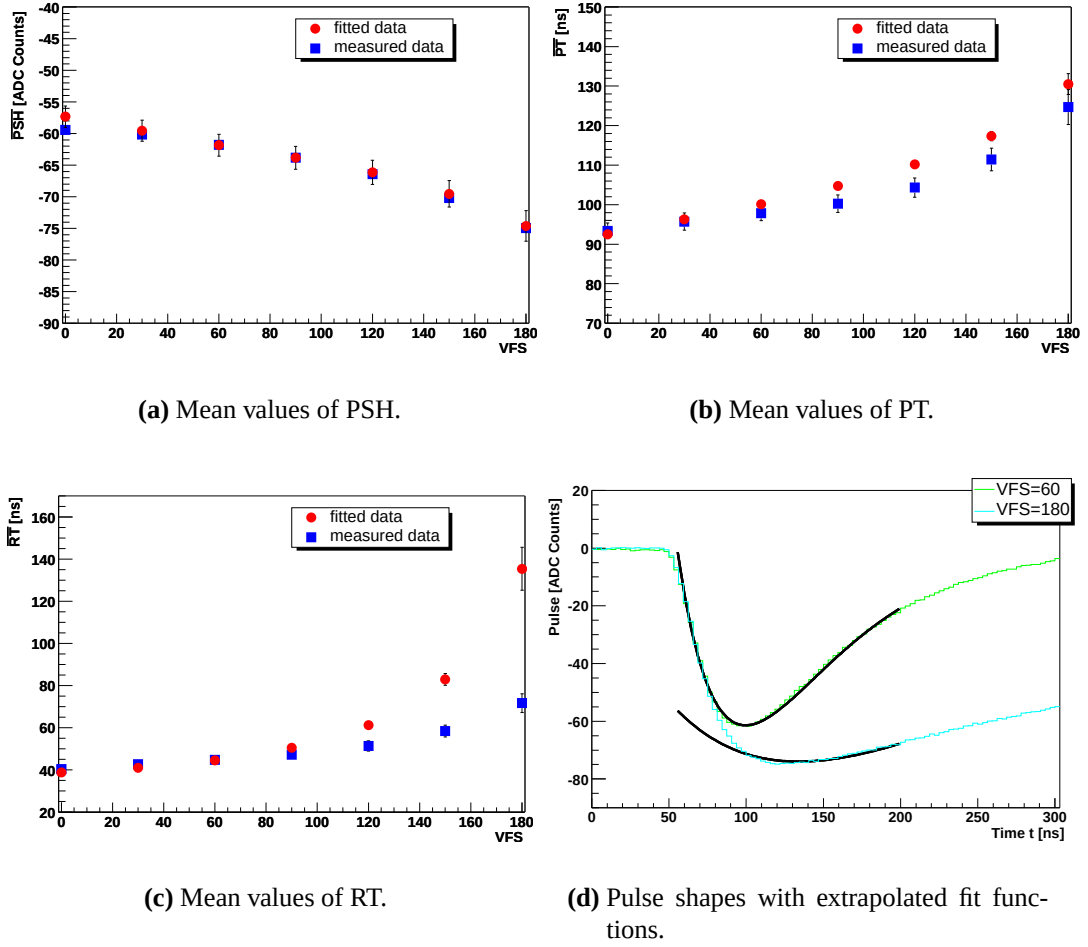


Figure 6.14: Fit parameters as functions of the VFS register. Parameters obtained from fits are compared with those values extracted directly from the measured data.

(VFS = 60) fits well to the measured data distribution, the second function (VFS = 180) only agrees with the data at higher time bins. Thus the fit parameter RT is not allowed to be interpreted as rise time of the pulse shapes for $VFS \geq 120$. Since the pulse shape test will be performed for $VFS = 60$, the chosen function describes the pulse data adequately.

In deconvolution mode similar interpretation problems do not occur, since the distribution around the extremal value is not affected significantly by the variation of VFS (see figure 6.12(b)). Thus the Gaussian fit delivers reliable results for the complete VFS range.

The power of the pulse shape test is illustrated in the figures 6.15(a) to 6.15(d). Different failures occur with different pulse shape signatures which can be compared to the behaviour of regular channels. While opens are characterized by higher amplitudes and lower peak and rise times, shorts show significantly lower PSH , PT , and RT values than regular channels. In particular the pulse amplitudes for shorts give a hint to the number of strips connected. Usually, two shorted strips divide the injected charge

thus showing pulse heights of about one-half compared to regular channels. In case of three strips connected, the amplitude is about one-third of the average height per strip. Both situations are included in the figures 6.15(a) to 6.15(d). The present pinhole shows up with nearly no response to the calibration pulse. This signature is not unique for all kinds of pinholes which will be discussed in detail in section 6.1.6. In order to avoid unreliable fit results during an automated test procedure, a fit to a certain pulse shape is not performed, if the absolute extremal value $|PSH|$ is less than 10 ADC counts. In this case the fit parameters are set to zero. As a consequence, the test procedure needs a minimal injection charge ($ICAL > 10$) to work reliably.

The peak mode distributions for PSH , PT , and RT concerning only regular channels are homogeneous. Thus a strategy following linear thresholds can be used to separate bad channels from regular channels. In deconvolution mode the measurements typically show slight slopes of maximal 10 ADC counts across a single chip (see figure E.2). This worsens the observation efficiency of errors when using linear cuts.

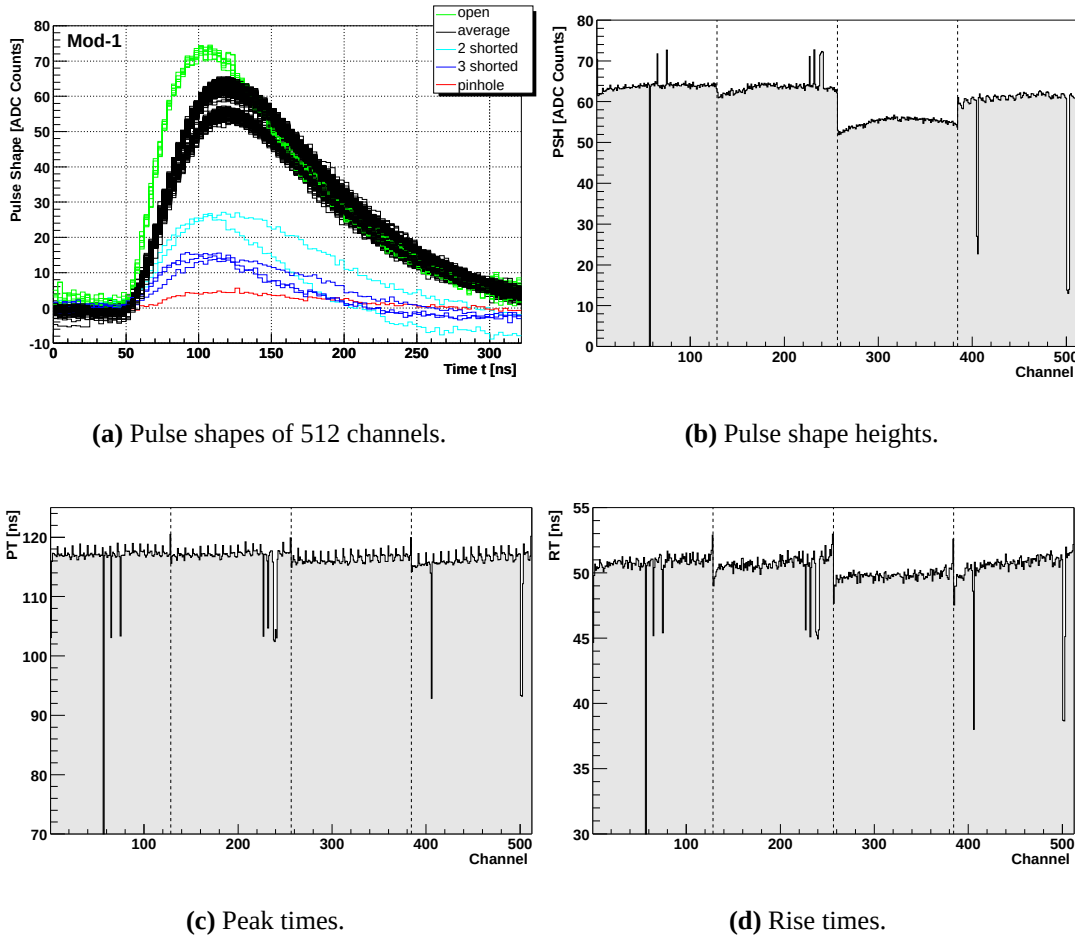


Figure 6.15: Calibration pulse test in peak mode. Different types of strip errors show up with different shape signatures.

Test Characteristics and Cut Parameters

The pulse shape test procedure is one of the most powerful tools with respect to failure diagnostics. Thus it is planned to be used in all quality assurance tests. The pulse shape measurement requires a time of about 1:30 min for ten events per measuring point including the subsequent shape fitting. Similar to the noise measurements, the pulse shape measurements are sensitive to grounding conditions. Bad grounding sometimes shows up in distorted pulse shapes at the edges of the chips particularly (see appendix E.2). Nevertheless, a stable fit procedure allows the assessment of the readout channels with respect to their pulse shape properties. The following cut parameters are suitable:

Pulse Shape Cuts	CUT_{rms}	CUT_{perc}
<i>PSH</i>	4.0	0.20
<i>PT</i>	5.0	0.03
<i>RT</i>	5.0	0.03

The cuts are independent from the type of the test object are applied APV-wise.

6.1.6 Light Tests with Light Emitting Diodes

Two kinds of infrared light tests are implemented in ARCS exploiting the features of the LEP_16 board and the optical fibre array. In principle the light measurements are meant to verify the response of a depleted silicon detector to a physical signal. In this sense the tests represent the only module specific measurements planned during the qualification chain.

One of these tests is based on *pulsed light* while the other one uses *continuous light*. Due to the AC coupling technique used to read out a CMS module, AC and DC currents generated in the bulk material cause significantly different effects in the detector. Pulsed light creates charge in the sensor periodically thus simulating traversing particles whereas continuous light increases the detector's DC leakage current without being observed by the readout strips. Thus both types of measurements can be used to determine different kinds of detector failures.

Pulsed Light Test

In this kind of test, pulsed light signals are applied to the detector's sensors at low rates (1.6 kHz) with short pulse lengths (500 ns). The light intensity is adjustable by the operator, but a medium intensity is used by default. In order to avoid saturation effects of the APV chips, the LEDs are switched on and off one by one. This procedure is called *pulsed light scan*. The fibre array is arranged at the end of the second wafer (WxA, according to figure 4.1) to spot not only un-bonded channels and shorted strips, but also breaks of the aluminium readout lines at the sensor.

Every-time one of the 16 LEDs is switched on, a statistics of N events is accumulated (default value is $N = 100$ events). These data samples are used to calculate the mean response of each channel. Afterwards the mean values are corrected by pedestal

data based on 100 events. By this means, 16 different data samples are available at the end of a complete light scan. The superposition of those samples allows to extract the maximal response LED_i of each readout channel i throughout the scan. Typically the pulsed light scan is performed at $LATENCY = 2$ thereby operating the APVs in peak mode with the inverter stage switched on.

Figure 6.16(a) shows typical channel responses to pulsed light exemplified on data from a single APV. The intensity profiles of the individual light spots are reflected by the measured wave structure depending strongly on the distance of the optical fibre array to the sensor surface. Moreover, the large variations of individual light intensities are caused by inhomogeneous fibre connections to the diodes resulting in different light injections. Figure 6.16(b) illustrates the large variations in the response of regular channels which range between 50 and 90 ADC counts. In the present case, bad channels show up for $LED_i < 20$ ADC counts whereas the entries above 100 ADC counts are caused by strip cross talk evoked by faulty neighbouring channels.

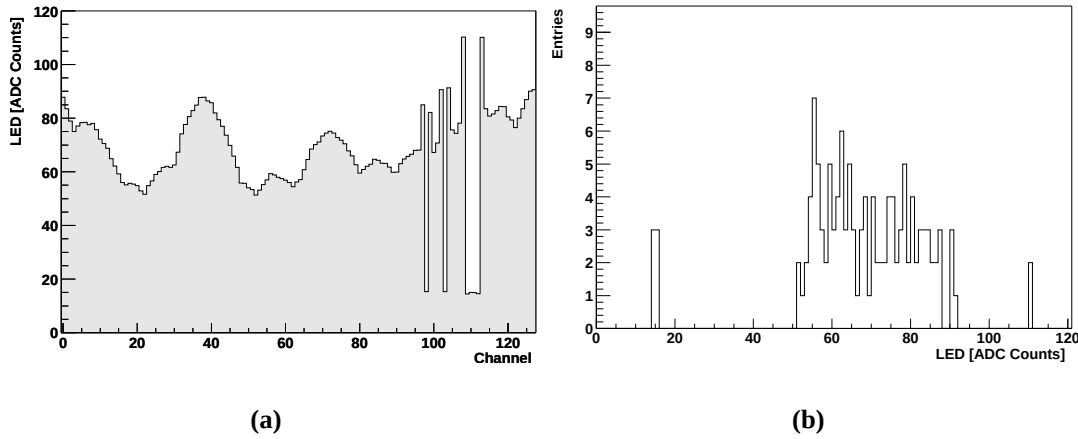


Figure 6.16: (a) Response of a module to pulsed LED light. Since strips 98, 101, and 109–112 (considering the APV numbering scheme) show only slight response to light, they are assessed as bad channels. (b) Statistical distribution of the light responses. The spread of regular channel responses is about ± 20 ADC counts.

Data Interpretation

Since each optical fibre array represents a unique device due to the inhomogeneous fibre coupling to the LEDs, it is essential to prove the reproducibility of test results using different optical fibre arrays. Appendix E.3 gives an overview of measurements performed with 16 different optical arrays produced in Aachen. The data samples are based on the same operation conditions using the same module (Ex1-7). This module was modified with artificial failures (one open at channel 101, three pinholes at 163, 183, and 203, two shorts at 223/224 and 243/244) thus providing to check the impacts of LED light on the various kinds of typical channel failures.

As a result, the 16 measurements reveal the same conspicuous channels in terms of low responses to the LED light. The individual wave structures deviate from each other

with respect to intensity heights and fluctuations significantly. Comparisons of the 16 data samples are depicted in figures 6.17(a) and 6.17(b), respectively. For each channel the mean response value $\overline{LED}_i$ is calculated as well as the corresponding standard deviation. Regular channels show fluctuations of about ± 8 ADC counts whereas the light effect on faulty channels is similar for all data samples (± 1 ADC count).

Due to the large intensity variations from one LED array to the other, a unique definition of a bad channel for automated quality evaluation is difficult. In particular, shorted strips are sometimes hidden in the wave structure, since they may give partially response to light. This case is illustrated in figure 6.17(b). The arrow indicates a known faulty strip that is difficult to be distinguished from regular channels with a linear cut strategy.

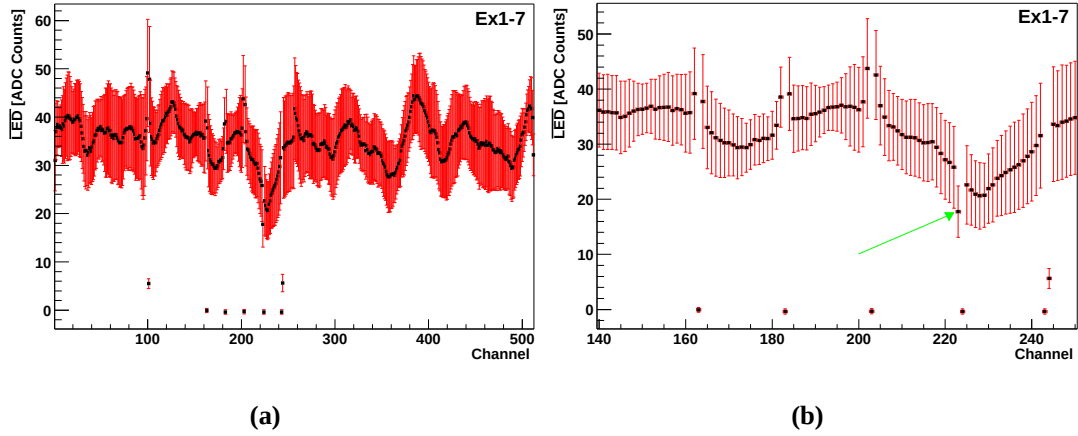


Figure 6.17: (a) Mean light response per module channel. The data and their corresponding standard deviations (assigned as error bars) are derived from the 16 measurements shown in figures E.5 and E.6. (b) Zoomed region between channels 140 and 250. The arrow indicates a known shorted strip hidden in the wave structure.

From the automation's point of view, some kind of data calibration is required, in order to improve the capability of spotting bad channels reliably when using the pulsed light test. A single initial calibration run is insufficient to correct the measurements properly, since the light spot structure varies from one array to the other. Moreover, the same positioning of an array between two consecutive module tests can not be guaranteed. Thus a sophisticated on-line calibration is incorporated in the ARCS analysis framework which is performed at the beginning of every pulsed light test.

As discussed above, the LEDs are switched on and off one by one during the test procedure. This can be used to reconstruct an ideal light profile structure from the measured light data. When switching on a single LED, the light profile on the corresponding part of the detector can be fitted. Due to the small optical fibres and their polished ends, the light shapes are usually Gaussian-like. Consequentially, a Gaussian function (see equation 6.6) is used to fit each single light profile measured. Before those fits are performed, a pre-selection of evidently conspicuous strips is done considering the uncorrected light scan information LED_i . Condition 6.2 is used to apply

a linear RMS cut to each measuring point with $CUT_{rms} = 3.0$. If a channel is flagged as bad, it will not be considered in the Gaussian fit procedure at all.

Figure 6.18(a) shows two examples of fitted light pulses. A fibre light spot that covers only regular channels leads to an undistorted Gaussian signal with a FWHM⁷ of about 24 channels (at an array distance of about 3 mm from the surface). If the spot illuminates also faulty channels, the signal is usually distorted significantly. In this case the light shape includes non responding channels that are surrounded by overshooting channels caused by cross talk effects. Nevertheless, even those pulses lead to sufficient fit results when using a Gaussian function. The fit parameters are used to calculate the ideal light response per channel in the observed enlightened region. Thus 16 Gaussian distributions are available at the end of a complete light scan describing a perfectly working detector. The superposition of those distributions is used to determine the ideal maximal response of the individual channels. The derived ideal light profile structure is shown in figures 6.18(b) and 6.18(c), respectively. The quantity used to describe the ideal light response of channel i is called LED_i^{fit} .

In the last step of the calibration procedure, the ideal wave structure is subtracted from the initial data sample thus leading to a quantity called LED_i^{diff} :

$$LED_i^{diff} = LED_i - LED_i^{fit}. \quad (6.15)$$

Figure 6.18(d) shows the results of the data subtraction. Regular channels are characterized by values for LED_i^{diff} of about zero ADC counts whereas faulty strips show up with a large negative value.

In order to prove the stability of the on-line calibration, this procedure is also applied to the 16 different LED array measurements discussed above. The individual results are shown in figures E.7 and E.8 where all distributions are flat concerning regular channels thus approving the functioning of the calibration procedure. A detailed comparison of the 16 data samples is illustrated in figure 6.19. For each channel the mean value $\overline{LED_i^{diff}}$ is calculated as well as the corresponding standard deviation. In contrast to figure 6.17(a), regular channels show the same behaviour in all measurements. Thus the separation of bad channels from regular ones is improved. Even the shorted strip, previously hidden in the wave structure, shows up in the corrected data sample (see arrow).

The data interpretation after the on-line calibration procedure is straightforward. A regular channel is characterized by a difference of $LED_i^{diff} = (0 \pm 5)$ ADC counts, since the reconstructed value is nearly equal to the initial measurement. If an open or a pinhole is present, the corresponding channel gives nearly no response to external illumination. Thus the difference between measured and ideal light response is large and negative (typically below -15 ADC counts). As shown in the example above, shorted strips are sometimes more delicate to spot due to their partial responses to light.

Cross talk effects are still present after the data subtraction, but usually they are characterized by positive deviations from zero. If several faulty channels occur at short distances, cross talk effects can also lead to data shifts into the negative direction.

⁷Full-Width Half-Maximum.

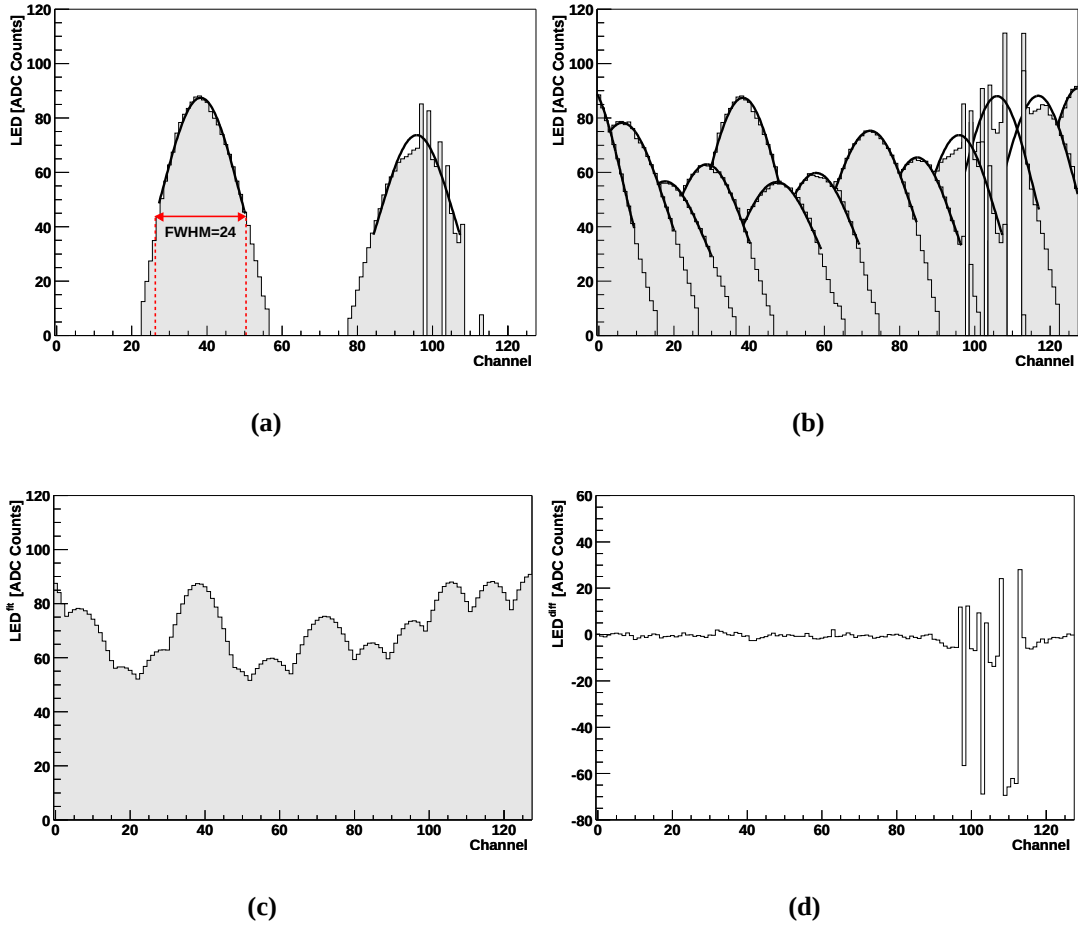


Figure 6.18: Pulsed light calibration strategy: (a) Light pulses are fitted separately with Gaussian functions, (b) several pulses covering the complete APV channel range are superimposed, (c) an ideal light profile is derived, and (d) the differences of measured and ideal light responses are calculated.

Test Characteristics and Cut Parameters

The pulsed LED light test (with the light structure correction) provides a very fast failure determination, since the typical duration of the test procedure is about 20 s using 100 events per LED that is switched on (including the fitting). It can be used for all module tests which includes the module assembly and qualification, as well as the long-term test. The pulsed light test is sensitive to opens and pinholes particularly, but it is not suited to distinguish between the different kinds of failures. For the channel assessment the following conditions (applied chip-wise) are sufficient:

Pulsed Light Cuts	CUT_{rms}	CUT_{perc}	CUT_{abs}^{min}
LED	3.5	0.6	
LED ^{diff}			-15.0 ADC counts

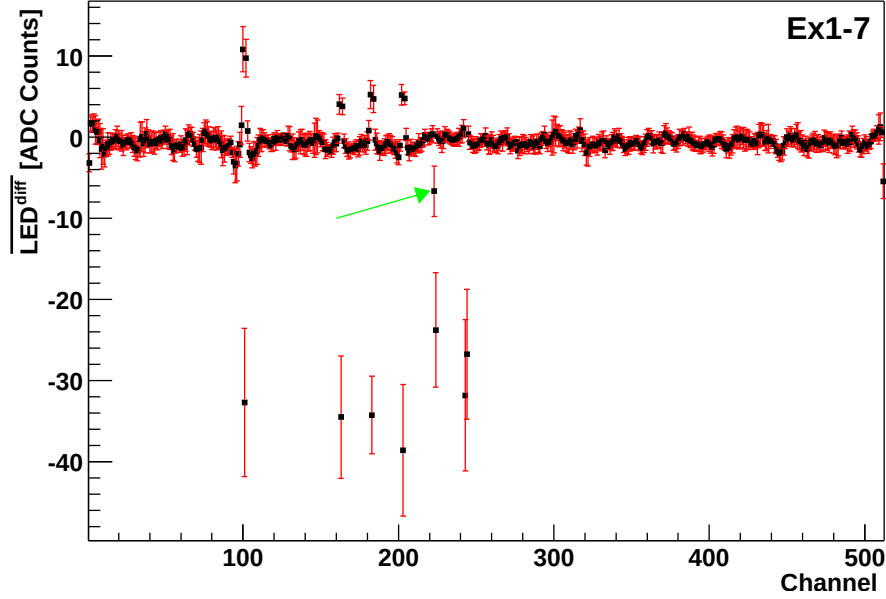


Figure 6.19: Mean difference of measured and ideal light response per module channel. The data and their corresponding standard deviations (assigned as error bars) are derived from the 16 measurements shown in figures E.7 and E.8. The array indicates the same shorted strip which was hidden in the wave structure shown in figure 6.17.

Remarks

Similar light tests can be performed with an infrared laser moving step by step across the sensor surface. In fact, laser measurements provide the possibility of studying single strips, since the laser spot can be focused down to the dimensions of a single strip. Thus an extensive data calibration is not required. The disadvantage of a laser system is its price and the huge installation effort. In addition, various production centres need to be equipped with the same portable system in order to guarantee a homogeneous test procedure. From this point of view, a cheap LED system is favoured. Another crucial aspect is the demand of a specific pinhole test which needs a continuous light illumination. This topic will be discussed in the next section.

Continuous Light: Pinhole Test

As mentioned in section 4.2, pinholes are defined as shorts or ohmic connections between aluminium strips and their corresponding p^+ implants. In order to observe this kind of failure, ARCS makes use of the internal calibration feature of the APV chip in combination with the continuous light supply of LEP_16. More precisely, in the pinhole test the calibration pulse amplitude per readout channel is determined as a function of the leakage current induced by continuous light originating from the LED array.

The test procedure includes the step-wise increase of the continuous light intensity in 86 steps. To provide safe operation of a detector with respect to the total leakage

current drawn, three different intensity ranges are available which are adjustable via an 8-bit DAC located on the LED controller board:

- 0 to 85 ADC counts in steps of one ADC count,
- 0 to 170 ADC counts in steps of two ADC counts,
- 0 to 255 ADC counts in steps of three ADC counts.

Figure 6.20 shows the correlation between the LED intensities and the DC current created in the sensor.

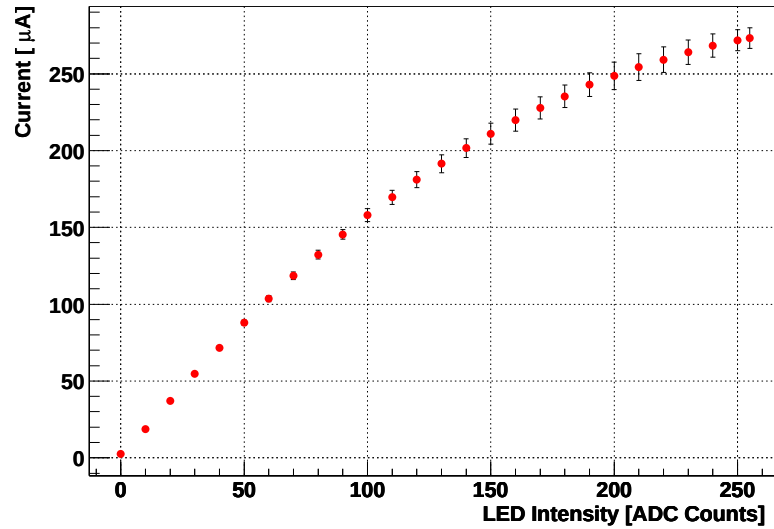


Figure 6.20: Correlation between LED intensities and created DC currents. The data points are mean values based on four measurements while the error bars indicate one standard deviation.

After changing the LED intensity, a calibration charge of 65,000 electrons selected via $ICAL = 100$ is injected to each calibration group periodically being accessible via the CDRV register. The trigger pattern used is “11000000(spacer)00010011” whereas the spacer value is set to five. The pinhole test is always performed at a fixed sample time ($LATENCY = 13$, $CSEL = 127$) and at fixed MODE register (peak mode, inverter off and calibration inhibit off $\rightarrow$ $MODE = 11$). The data samples are corrected by their pedestals which are based on 100 events.

By this means, the response of each individual channel to calibration pulses as a function of the leakage current is obtained. For a certain channel i at intensity int the response data is referred to as PIN_i^{int} . Figure 6.21 shows the results of a pinhole test performed on module Mod-1. The figure illustrates the sensitivity of the continuous light test with respect to different channel failures.

Data Interpretation

The signatures of regular channels, opens, and shorts are similar to those described in the calibration pulse shape test. Opens show significantly higher pulse response than

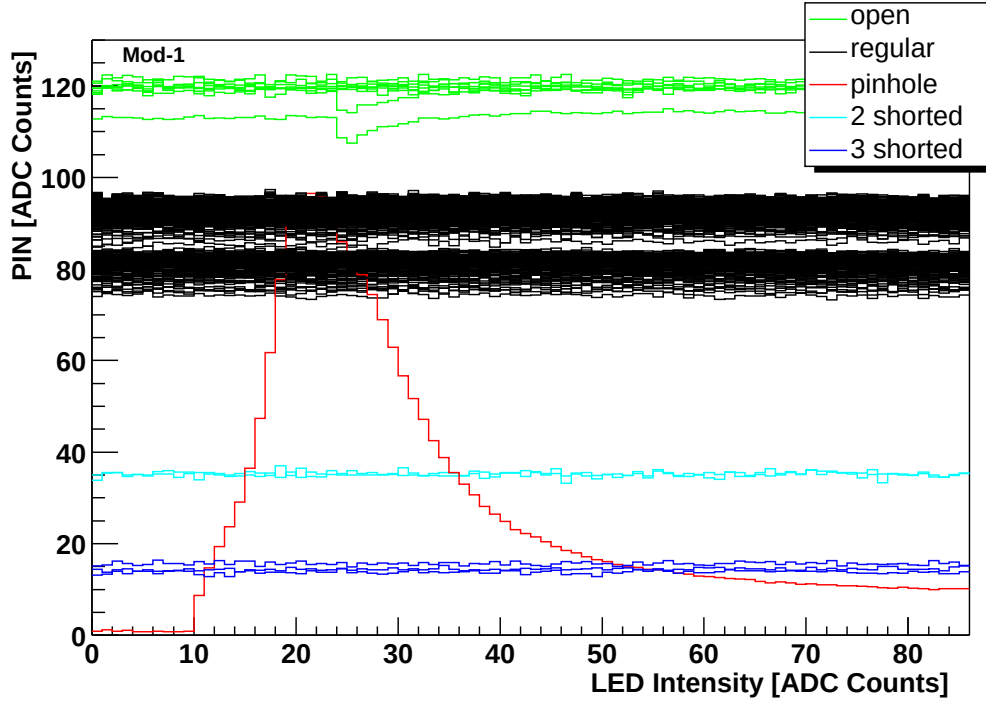


Figure 6.21: Signatures of different failures that show up in the pinhole test. The data of 512 channels are superimposed. A pinhole may cause cross talk effects on its calibration group members. In this case, the pulse shape heights are reduced slightly at certain light intensities. Obviously two of the open bond channels are affected. Source: [92]

regular channels while shorts are characterized by responses of one-half (2 shorted strips) or one-third (3 shorted strips) of the pulse heights of regular channels, respectively. Usually, the responses of opens, shorts, or regular channels to the calibration pulses are not affected by the variation of the LED intensities. In contrary, in most cases a pinhole affected channel changes its response during the intensity scan. In the present case of figure 6.21, the pinhole signature evolves from no signal response at very low LED intensities to a normal response at a certain intensity (at approximately 20 ADC counts). At higher currents the charge injection response starts to decrease again. This kind of pinhole is also called a *resistive pinhole*.

The impact of a resistive pinhole on an APV chip is illustrated in figure 6.22, where the pinhole itself is represented by an additional resistor $R_{pinhole}$ in the readout chain. A resistive pinhole causes an electric potential problem (at V_c), since the virtual ground of the APV preamplifier is shifted with the strip leakage current. The optimal working point of the preamplifier input is +0.75 V. If I_{leak} is small (which corresponds to a low LED intensity), V_c is less than +0.75 V. Thus current flows out of the chip and the APV preamplifier output (V_i). As a consequence, only the channel affected by the pinhole is dead. If I_{leak} is large ($V_c > +0.75$ V), current flows into the APV and the preamplifier output saturates. Apart from the pinhole strip being dead, the inverter output transistor turns on and draws as much current as possible thus taking away current from the remaining inverters on the chip. This is a possible mechanism for one

pinhole to disable a complete APV.

Thus only for a certain leakage current or a certain LED intensity, respectively, if the condition $V_c \approx +0.75\text{ V}$ is valid, the APV preamplifier is not saturated and shows the normal response to a calibration pulse (see figure 6.23(a)). The current value required to match this situation depends strongly on the resistance of the pinhole which can range between a few Ω and a few $\text{G}\Omega$. Therefore the LED intensity needed to un-saturate the APV preamplifier is not unique for all pinholes. Typically, low resistive pinholes become already obvious at currents of below $100\text{ }\mu\text{A}$.

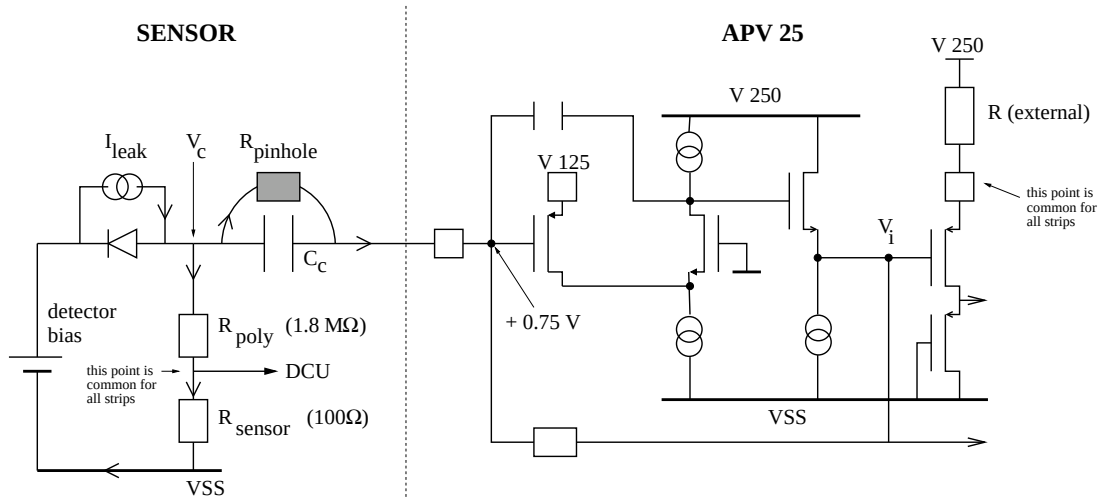


Figure 6.22: Pinhole effect. The gray shaded resistor called $R_{pinhole}$ illustrates the impact of a pinhole to the detector system. Source: [89]

A low resistive pinhole is in particular dangerous for irradiated modules, since the leakage current increases with irradiation. This can lead to a large current into the APV preamplifier. To improve this situation, the potential divider between the leakage current dependent resistance of the n-bulk below the strip R_{sensor} and the polyresistor R_{poly} can be changed by reducing both resistances (see [89] for details). Nevertheless, due to their impacts on APV chips, pinholes have to be identified as early as possible and get disconnected from the preamplifier.

Throughout the various module tests performed with the ARC system, two other effects in the continuous light test occurred also being interpreted as pinholes. One signature observed is shown in figure 6.23(b). The affected channel is characterized by the typical behaviour of an regular channel at low LED intensities and a rapid decrease of the response at a certain intensity (here at 25 ADC counts). In fact, these failures act like proper capacitors up to specific voltages where they immediately begin to conduct. Therefore those failures are called *threshold pinholes*.

Another conspicuous kind of signature shows no response at all during the complete intensity scan (see figure 6.23(c)). This case seems to be a temporary effect, since it vanishes with module operation time. Sometimes it evolved to a typical threshold pinhole, but sometimes it vanishes completely acting like a regular channel. Due to

this characteristic the affected channels will be called *temporary pinholes* in the following.⁸

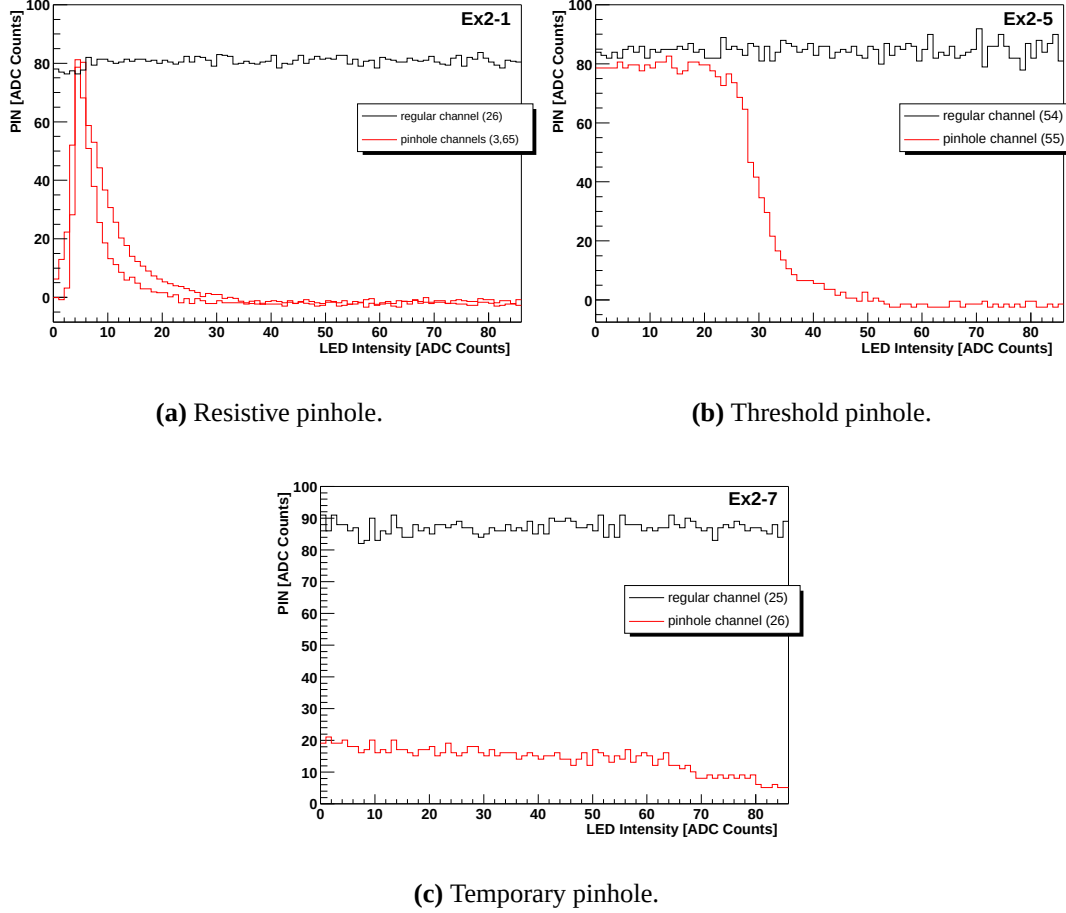


Figure 6.23: Different pinhole signatures compared to the behaviour of a regular channel.

From the point of view of an automated test procedure, decisive failure characteristics have to be extracted from the measurements explained above. In ARCS, two quantities are used to determine conspicuous channels: PIN_i^{max} and ΔPIN_i , where i defines the corresponding channel. PIN_i^{max} is the maximal response per channel occurred during the complete intensity scan. On basis of this quantity, opens, shorts, regular channels, and temporary pinholes can be distinguished efficiently. A resistive pinhole can be tagged by calculating the difference between the maximal and the minimal pulse responses throughout the scan:

$$\Delta PIN_i = PIN_i^{max} - PIN_i^{min}. \quad (6.16)$$

The distributions of PIN^{max} and ΔPIN obtained from module Mod-1 are presented in figures 6.24(a) and 6.24(b). Since the data show homogeneous distributions

⁸A channel that never shows any response to calibration pulses could also suffer from a defect APV input.

within the individual APVs, linear thresholds can be envisaged to evaluate the quality of the corresponding module. Figure 6.24(b) reveals that the pinhole (located at channel 57), which is characterized by a very large value for ΔPIN_i , causes cross talk effects on its calibration group members. Thus every eighth strip of the affected APV chip (here channel 1,9,..., 121), shows a significantly larger value for ΔPIN than regular channels do normally. The cross talk effect depends on the type of pinhole and on the number of pinholes present on the corresponding sensor region. Several pinhole measurements revealed that regular channels belonging to the same calibration group as a pinhole typically have ΔPIN values which are a factor of 2 to 5 larger than those values obtained from regular channels not being affected by cross talk effects. As a consequence, the cut threshold for ΔPIN_i has to include some margin in order to avoid generating fake bad channels due to cross talk effects.

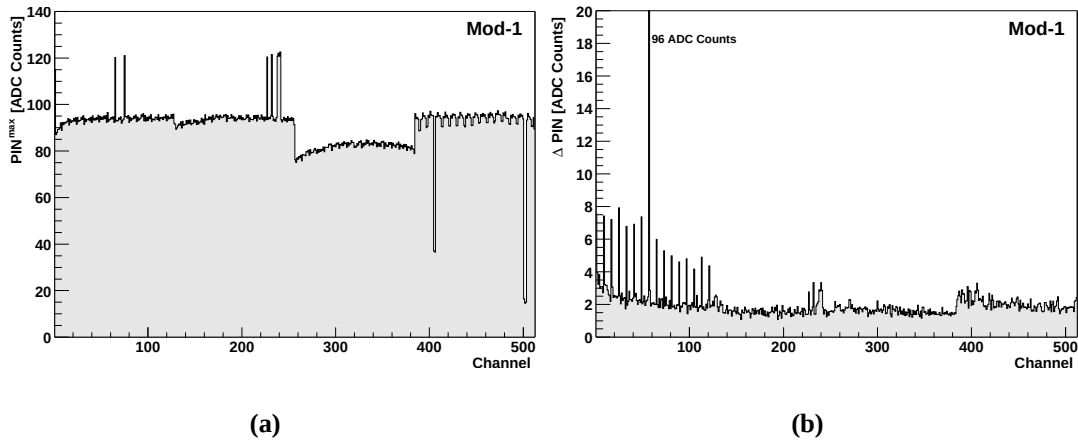


Figure 6.24: Pinhole test characteristics: (a) PIN_i^{max} and (b) ΔPIN_i . The quantities are extracted from the measurements depicted in figure 6.21.

Test Characteristics and Cut Parameters

The continuous LED light test (pinhole test) requires about 1:45 min taking five events per measuring point. This test is the most powerful tool with respect to failure diagnostics of modules. It is sensitive to all kinds of faults and allows to assign different types of signatures to different flaws uniquely. Similar to the pulsed light test, the pinhole test will be used for all module tests which includes the module assembly and qualification, as well as the long-term test. In particular, a proper pinhole search is proposed to be performed immediately after the module bonding, since wrong bond parameters may cause breakthroughs of the bond pads (see section 7.2.3). The channel assessment can be done chip-wise with the following cut conditions:

Continuous Light Cuts	CUT_{rms}	CUT_{perc}	CUT_{abs}^{max}
PIN^{max}	4.0	0.2	
ΔPIN			40.0 ADC counts

6.1.7 I-V Curve Measurements

In the *I-V curve* measurement, a correlation between the applied detector bias voltage and the measured current is determined. The obtained I-V curve typically shows the characteristic behaviour of a reverse biased diode. In general, this kind of test is meant to prove the breakdown performance of each module.

In the test procedure, the sensor bias voltage is typically ramped from 0 V up to a certain maximal voltage V_{max} thereby not exceeding a ramping rate of 10 V/s. Since the modules have to be operated at a few hundred volts after ten years of LHC running, the tested modules should thus cope with $V_{max} = 450$ V. After reaching the voltage value, the measuring point is taken when a defined waiting time is elapsed (typically 30 s). This time is essential to allow the detector to reach its new equilibrium condition.

Figure 6.25 depicts a typical I-V curve obtained. The measurement was performed at ambient temperature without humidity controlled conditions. One can see the slight rise of the leakage currents at low voltages followed by a long plateau. At the edge of the breakdown voltage the leakage current increases significantly within a few volts.

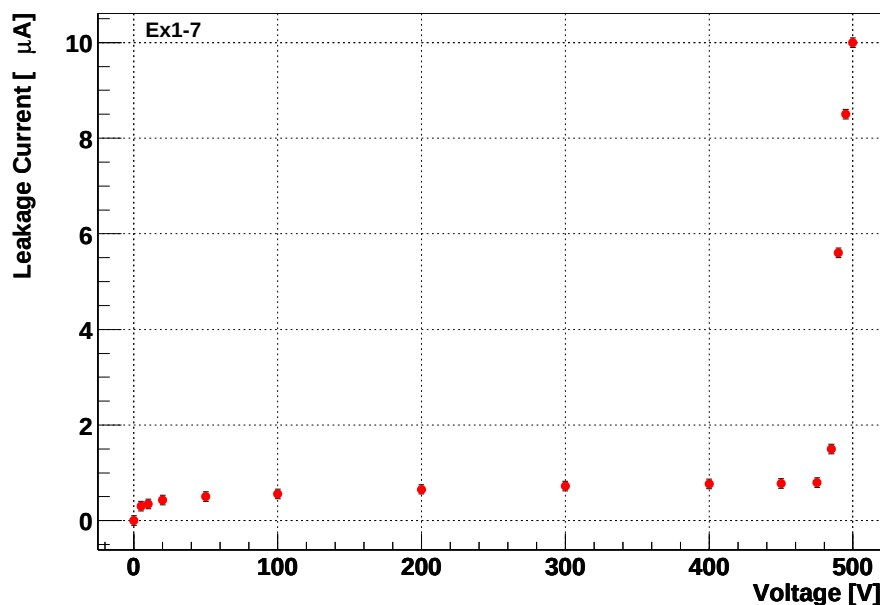


Figure 6.25: Typical I-V curve of a module.

Data Interpretation

The current-voltage measurement is extremely sensitive to the environmental conditions such as temperature, humidity, brightness, handling, and history of the module. This makes a comparison of different measurements of the same module difficult.

Nevertheless, the curves can be interpreted in terms of maximal leakage current drawn at a certain voltage. Thus a module is called bad, if the breakdown occurs before reaching the 450 V regime.

Remarks

The current-voltage measurements shown in this thesis are performed manually using the high voltage supply device mentioned at the beginning of this chapter. In this sense they were no part of the ARCS test procedures. Recently, an automated I-V curve scan has also been implemented in the ARCS environment using the DEPP high voltage board.

Test Characteristics

A non-irradiated module suffering from an electrical breakdown at low voltages will not be able to survive the ten years of LHC operation. From this point of view, the I-V curve measurement is an essential type of test to be done during the module quality assurance. Since the I-V curve measurement is extremely sensitive to several conditions (temperature, humidity, module history, etc.), a unique test procedure has to be defined to provide reasonable and comparable test results. In this thesis, a breakdown is announced if $I_{leak} > 20 \mu A$ at a voltage lower than 450 V.

6.1.8 General Remarks

A comparison of the individual test procedures presented in this thesis reveals that some of the tests yield similar failure information. Although the allowed time for testing is restricted, the accumulation of redundant information is essential from the point of view of an automated quality assurance. Since each test shows its own sensitivity to environmental influences and to different types of failures, the combination of several test results can lead to a unique failure matching. This redundancy allows to use linear threshold conditions for the channel assessment even for data distributions which are not homogeneous at all. If a faulty channel is not observed in one test due to the thresholds used, it will presumably be found in another measurement. This improves the efficiency of an automated test procedure.

6.2 The Fast Test Procedures

The *fast test* procedure includes eight standardized, basic functional tests which are intended to provide a fast characterization of FE hybrids particularly. In addition, the present status of the used ARC setup is checked. Thus the fast test should be performed at the beginning of each hybrid or module qualification procedure. To cope with the limited test time at some production centres, the test procedures are optimized to take less than one minute altogether.

Figure 6.26 shows the fast test panel as it is implemented in the ARC software. The application is designed to be operated without detailed knowledge of the test object connected. Thus all tests selected by the operator at the beginning of the fast test are performed and interpreted automatically. After each sub-test some comments and the final result are shown and then written into an ASCII log file.

At the end of the fast test procedure various lights indicate the total test results with respect to chip faults, pedestal, noise, and calibration pulse measurements, and hardware reliability. A green light flags a passed test whereas a red light indicates a problem during one of the tests. If a certain measurement is not performed, the light stays black. Since the log file includes the complete test history, it can be used for a fast failure analysis.

The combination of the fast and advanced tests allow a complex and extensive quality assurance of hybrids as well as modules. While the fast test validates the basic functioning of the hybrid and its components, the advanced test gives detailed information about the data performance of the test object.

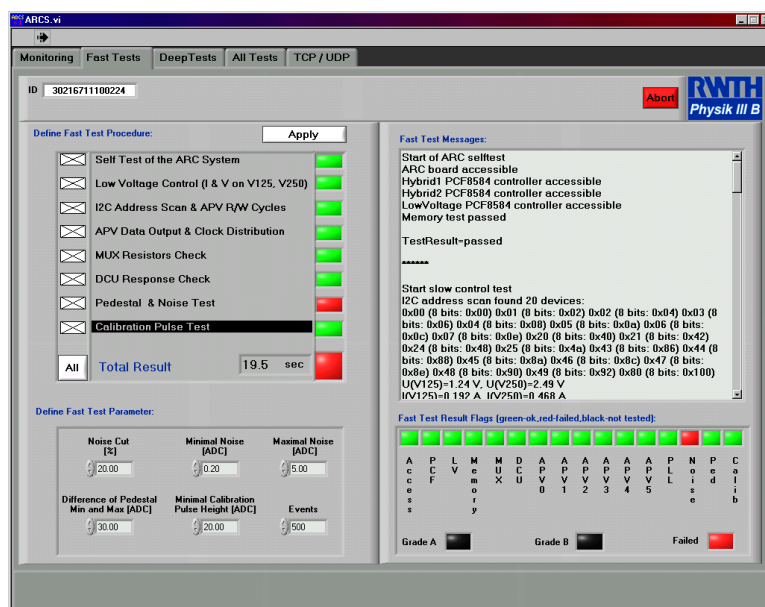


Figure 6.26: Fast test panel in ARCS. The operator is allowed to mark all sub-tests to be done thereby using the cut conditions adjusted (left side). A specific window on the right side lists comments and results of the fast test performed while several lights indicate the functionality of different hybrid components.

6.2.1 Setup Self Test

The first test incorporated in the fast test procedure is represented by the *setup self test* to verify the reliable performance of the setup. A bad operation of the diagnostic system might cause dubious test results. Thus the accessibility of the ARC board is checked at the beginning by read/write cycles of the ARC internal status register. If this test fails, the complete fast test procedure is stopped immediately. Afterwards the functioning of the three I²C controller is supervised, since these controller play an essential role in the I²C communication with the ASIC chips on the hybrid. Finally, an extensive memory test is performed by writing specific patterns into the RAMs and reading them back in order to compare the corresponding value sequences.

In case of a successful test (indicated by `TestResult=passed`), the information written into the log file after the setup self test typically reads as follows:

```
The Log-File has been written at:
Date= 30.06.2003 , Time 10:29:05
Hybrid Bar Code: 30216711100224
Test Results:
Start of ARC self test
ARC board accessible
Hybrid1 PCF8584 controller accessible
Hybrid2 PCF8584 controller accessible
LowVoltage PCF8584 controller accessible
Memory test passed
TestResult=passed
```

6.2.2 Slow Control Test

The *slow control test* includes an I²C address scan where the total number of connected I²C devices is determined. The address scan takes advantage of the standard I²C write access protocol (see appendix C.2). An I²C device gives only response to its own I²C address by setting the acknowledge bit (ACK) to one. The principally allowed address range includes all even numbers (with regard to write accesses) between 0x00 and 0xFF. Thus this range is scanned systematically to find devices responding to a certain write command.

For a hybrid equipped with four APVs, the expected number of addresses that have to be found is 19 (see log file entry at the end of this paragraph) whereas in the case of six APVs located on a hybrid two more addresses are added to the bus. In fact, two of these I²C addresses are defined by the ARC system and used for the low voltage control (0x90, 0x92). The remaining addresses belong to the chips on the hybrid.

One conceivable reason for I²C communication problems is a faulty low voltage supply. The ASIC chips behave slightly different from standard I²C devices with respect to their low and high level recognition. For instance, an APV interprets a certain voltage value as a logic “0” when being lower than 0.35 V whereas the I²C standard demands a threshold of up to 0.75 V at a supply voltage of 2.5 V. If the low voltage supply deviates from its nominal values, the level thresholds are also affected which might cause level recognition problems of different chips.

Since the ARC front end adapter facilitates the measurement of hybrid voltages and currents on the V125 and V250 lines, a low voltage check is implemented in the slow control test procedure where the following ranges have to be validated:

$$\begin{aligned} 1.22 \text{ V} &\leq V(\text{V125}) \leq 1.28 \text{ V}, \\ 2.45 \text{ V} &\leq V(\text{V250}) \leq 2.55 \text{ V}, \\ 0.10 \text{ A} &\leq I(\text{V125}) \leq 0.50 \text{ A}, \\ 0.40 \text{ A} &\leq I(\text{V250}) \leq 1.00 \text{ A}. \end{aligned}$$

These current limits chosen consider the fact, that some APV command registers affect the current consumption on the low voltage lines significantly. In addition, hybrids

equipped with four and six APVs draw different currents. Figure 6.27 shows the current consumptions of V125 and V250 at varying ISHA register settings. The ISHA register defines the current bias of the shaper input FET and can be adjusted between $0\ \mu\text{A}$ and $255\ \mu\text{A}$ in steps of $1\ \mu\text{A}$. The V125 line is not influenced by the different ISHA values, while the V250 line reveals a linear slope of about $0.56\ \text{mA}$ per ISHA step. This value matches the expected current consumption of a hybrid being equipped with four APVs ($512 \times 1\ \mu\text{A} = 0.512\ \text{mA}$ per ISHA step) within 10% .

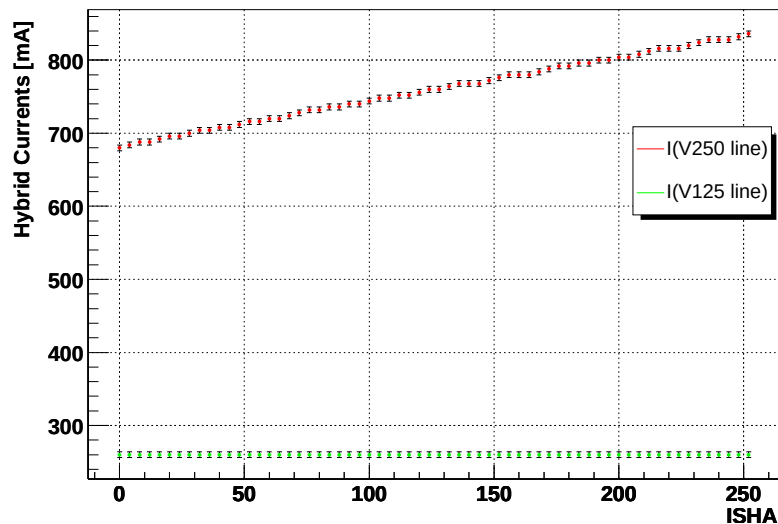


Figure 6.27: Current consumption of a FE hybrid versus ISHA register settings.

The results of the slow control test are also written into the log file. The I²C addresses found are not only given in the usual 8-bit form, but also in a 7-bit notation (without the read/write bit):

```
Start slow control test
I2C address scan found 19 devices:
0x00 (8 bits: 0x00), 0x01 (8 bits: 0x02), 0x02 (8 bits: 0x04),
0x03 (8 bits: 0x06), 0x04 (8 bits: 0x08), 0x05 (8 bits: 0x0a),
0x06 (8 bits: 0x0c), 0x07 (8 bits: 0x0e), 0x20 (8 bits: 0x40),
0x21 (8 bits: 0x42), 0x24 (8 bits: 0x48), 0x25 (8 bits: 0x4a),
0x43 (8 bits: 0x86), 0x44 (8 bits: 0x88), 0x45 (8 bits: 0x8a),
0x46 (8 bits: 0x8c), 0x47 (8 bits: 0x8e), 0x48 (8 bits: 0x90)
0x49 (8 bits: 0x92)
V(V125)=1.24 V, V(V250)=2.49 V
I(V125)=0.184 A, I(V250)=0.468 A
LV levels in expected ranges
TestResult=passed
```

6.2.3 APV I²C Access Test

During the *APV I²C access test* the communication with each of the readout chips mounted on the hybrid is verified. The addresses reserved for APV chips range between 0x40 and 0x7E. Thus four (or six) of the I²C addresses found should be in that address range. In fact, the expected APV addresses are 0x40, 0x42, (0x44, 0x46,) 0x48, and 0x4a. If a deviation from these addresses occurs, it is immediately reported in the log file.

In the next step, ten write/read (w/r) cycles per command register and APV are performed. The test procedure is composed of consecutive write and read sequences of all APV registers while the written and read values are compared with each other.

If the communication with at least one APV is established, the so-called *APV assignment* is initiated. This phase is intended to order the found APV addresses with respect to their physical location on the hybrid. Figure 6.2 depicts the expected APV addresses as well as their assignment relative to the hybrid's substrate. The ordering procedure is based on the MODE register using the 3-sample feature. One APV after the other is operated in the 3-sample mode while the remaining APVs run in the 1-sample mode. A specific frame finding algorithm is implemented in ARCS that determines whether an APV is running in the 3-sample mode or not. The RAM location in which the corresponding APV data is buffered can thus be obtained. Since each memory is correlated to the physical data lines of the different APVs in a unique way, a reliable chip assignment is provided by this means. A correct APV assignment is essential with respect to the automated failure localization on a module, since the module's numbering scheme is based on the arrangement of the APVs on the hybrid. The assignment is a basic condition to provide accurate fault detection and repair.

The APV assignment is also a powerful tool to prove the functionality of the APV-MUX chip. Sometimes the multiplexing chip on a hybrid fails in interleaving two frames originating from two different APVs, thus generating a data sample that includes data of one APV twice. As a result, the number of output frames seems to match the expected number (four in case of a hybrid with four APVs), but in fact one data frame is doubled. The only way to find those failures in automated test procedures is the operation of one APV in a different way than the remaining chips (e.g. by using the 3-sample mode or calibration pulses). An alternation of this procedure allows the determination of the missing APV data frame in an effective and fast way.

After the APV I²C access test these information are written into the log file:

```
Start APV I2C access test
Scanned APV I2C addresses:
0x20 (8 bits: 0x40)
0x21 (8 bits: 0x42)
0x24 (8 bits: 0x48)
0x25 (8 bits: 0x4a)
Perform w/r cycles on APVs:
I2C APV Address: 0x20 (8 bits: 0x40) ok
I2C APV Address: 0x21 (8 bits: 0x42) ok
I2C APV Address: 0x24 (8 bits: 0x48) ok
```

```

I2C APV Address: 0x25 (8 bits: 0x4a) ok
No errors during r/w cycles on each APV register
Perform APV assignment:
APV position on hybrid (0,1,2,3,4,5):
0x20 (8 bits: 0x40), 0x21 (0x42), 0x00 (0x00),
0x00 (0x00), 0x24 (0x48), 0x25 (0x4a)
TestResult=passed

```

6.2.4 APV Data Test

The *APV data test* is only performed on APV chips that can be assigned. Based on N events (50 to 2000 events can be selected), the frame finding algorithm is used to look for APV frames in order to extract the error bit information from the digital output part as mentioned in section 3.2.1. The test is intended particularly to inspect whether all APVs run synchronized during the observation of the specified number of events. The synchronization is determined by decoding the pipeline addresses event by event. Within one event all chips should deliver data from the same pipeline location. If this synchronization is violated, a column error is announced.

In addition, the APV data test gives indirect information about the functionality of the APVMUX and the TPLL chips. A completely missing APV frame could be caused by faulty data multiplexing or by wrong clock and trigger distribution.

The information that is written into the log file after the APV data test reads as follows:

```

Start of APV data output test
(only assigned APVs are considered)
Number of taken events: 500
Search for APV frames and column errors:
Frame of APV 0x20 (8 bits: 0x40) found
Frame of APV 0x21 (8 bits: 0x42) found
Frame of APV 0x24 (8 bits: 0x48) found
Frame of APV 0x25 (8 bits: 0x4a) found
No column error
TestResult=passed

```

6.2.5 APVMUX Test

A specific *APVMUX test* is incorporated in the fast test procedures, in order to show the functionality of the eight APVMUX resistors being adjustable via chip internal registers. If the APVMUX chip is found in the I²C address scan (0x86), the measurements are done with N events (50 to 2000 events can be selected).

The ARC system is adjusted to exploit most of the available ADC range of 256 counts, if the APVMUX chip is operated with two resistors switched on. Thus at least two resistors have to be switched on during each measurement. The effects on the data output when switching on different numbers of resistors are illustrated in figure 6.28.

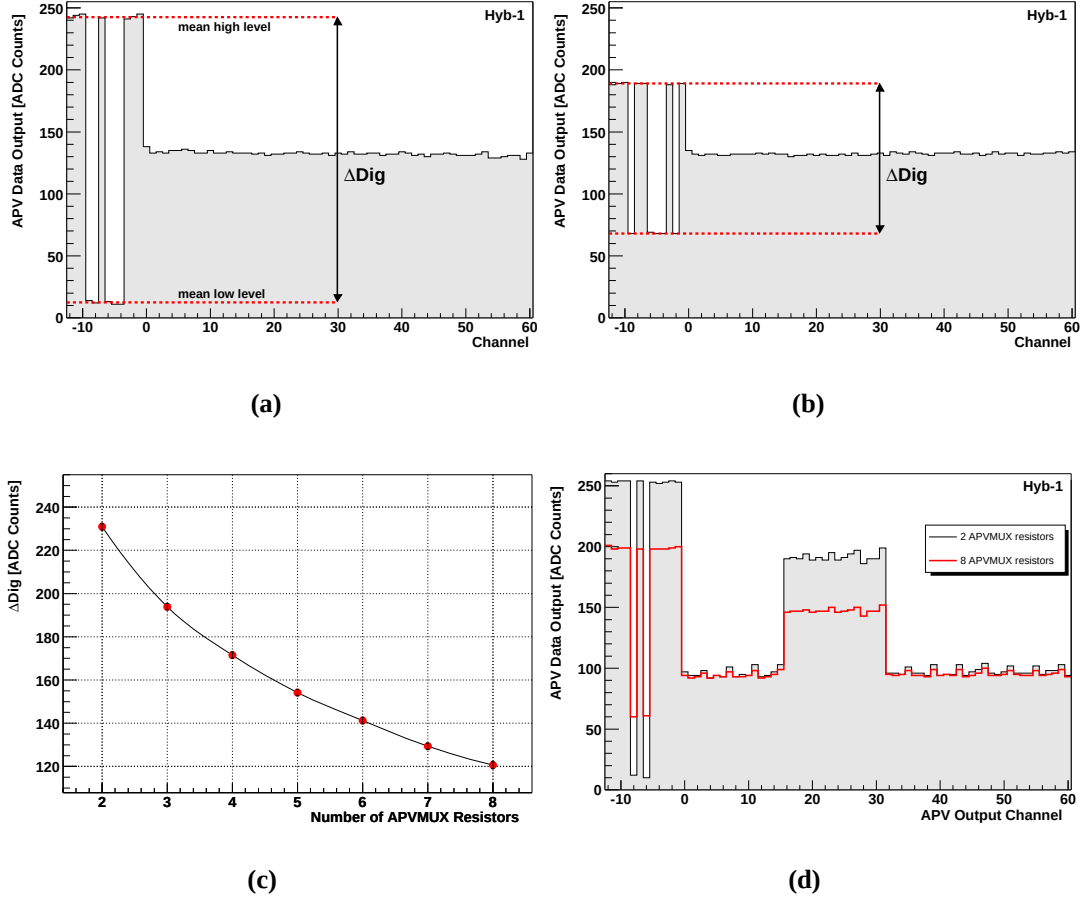


Figure 6.28: APV data frames under different operating conditions of the APVMUX chip: (a) Two resistors and (b) eight resistors are switched on. The analogue data baseline stays at the same height, but the digital data height ΔDig decreases by 50%. (c) ΔDig as a function of the number of resistors switched on. (d) Signal heights are also affected by the APVMUX resistors. In the present case, the pulse heights of a certain calibration group are shown ($CDRV = 253$ and $ICAL = 87$). For illustration purposes, the APV output channels are not ordered by equation 3.3.

The APVMUX test procedure uses an algorithm to determine the mean logic low level and the mean logic high level of the digital part of the APV output as shown in figure 6.28(a). The difference ΔDig between both levels should show significant dependencies from the total number of the resistors switched on. In fact, due to the parallel connection of the multiplexer's resistors, the difference is expected to decrease with increasing number of resistors. Figures 6.28(a) to 6.28(c) prove this expectation.

Based on the measurements presented in figure 6.28(c), specific conditions are determined to distinguish a regular APVMUX chip from a faulty chip. If the chip is operated with two resistors, ΔDig has to be within a range of 200 and 255 ADC counts. In addition, the minimal difference of two consecutive measurements may not undershoot 5 ADC counts.

The results of an APVMUX test are summarized in the following manner:

```

Start of MUX resistors test
APV #0 0x20 (8 bits: 0x40) ok
APV #1 0x21 (8 bits: 0x42) ok
APV #2 0x00 (8 bits: 0x00) not tested
APV #3 0x00 (8 bits: 0x00) not tested
APV #4 0x24 (8 bits: 0x48) ok
APV #5 0x25 (8 bits: 0x4a) ok
Expected frame height limits: [200.0,255.0]
APV 0 , frame height: 217
Minimal difference between different resistor switches: 5.0
APV 0 , differences within range ok
APV 1 , frame height: 219
Minimal difference between different resistor switches: 5.0
APV 1 , differences within range ok
APV 4 , frame height: 228
Minimal difference between different resistor switches: 5.0
APV 4 , differences within range ok
APV 5 , frame height: 225
Minimal difference between different resistor switches: 5.0
APV 5 , differences within range ok
All MUX resistors are ok
TestResult=passed

```

6.2.6 DCU Test

Since the ARC FE adapter provides the variation of the low voltages supplied to the hybrid, this feature can be used to perform a *DCU test*. Figure 6.29(a) shows the linear correlation between the adjustable low voltage DAC on the FE adapter and the low voltage measured on line V250 within a voltage range of 2.3 V and 2.6 V.

The nominal DAC value used to provide the hybrid with the required voltages is equal to 210 ADC counts. While changing the supply voltages, the ARC FE adapter allows the determination of the corresponding current consumptions. Figure 6.29(b)

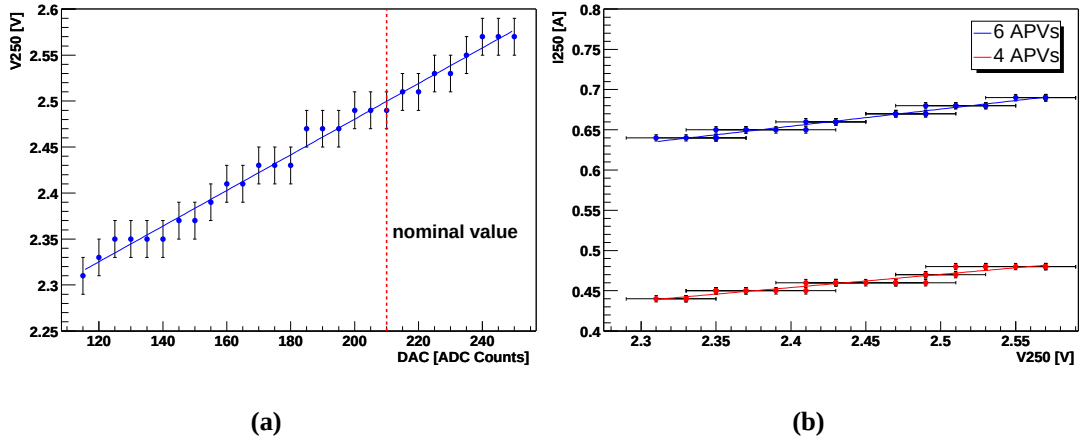


Figure 6.29: Hybrid low voltage and current measurements. (a) Adjustment of the low voltage on V250 and (b) current consumptions on line V250 based on four and six APVs, respectively.

presents two different low voltage-current scans on line V250 based on hybrids equipped with four and six APVs, respectively. Both measurements reveal similar linear slopes and a constant difference of about 0.2 A from each other.

The DCU chip is intended to monitor the hybrid low voltages among other parameters. Thus a low voltage scan can be performed to check the corresponding DCU response. Figure 6.30 shows the linear correlation between the DCU measurement of the voltage applied on line V250 and the adjusted DAC value on the ARC FE adapter.

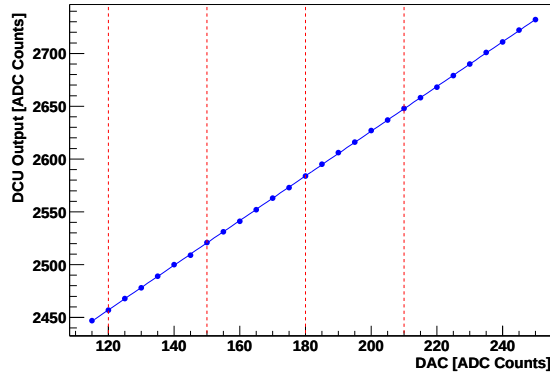


Figure 6.30: V250 voltage measurement by the DCU. The dashed (red) lines indicate the measuring points checked during the DCU test implemented in the fast test environment.

The DCU test scans the chip output of the V125 and V250 lines at four different DAC settings, namely at 120, 150, 180, and 210 ADC counts (nominal value) which are equal to 2.32 V, 2.38 V, 2.44 V, and 2.5 V. A DCU error will be announced, if the corresponding DCU measurement does not change from one applied voltage to the other. To verify the functioning of the voltage supply while changing the DAC values, the voltages as well as the current consumptions measured with the FE adapter are also

observed. All measurements rely on a functioning of the I²C communication with the DCU (I²C addresses: 0x00, 0x02, 0x04, 0x06, 0x08, 0x0a, 0x0c, and 0x0e) as well as the low voltage controller (0x90, 0x92).

At present a calibration of the DCU chips after their production in industry is not performed. Thus only the DCU output data (measured in ADC counts) can be interpreted and assessed in the fast test procedure so far. In the future it is planned to calibrate the DCU output during the FHIT tests at the hybrid manufacturer as well as during the hybrid-to-pitch adapter assembly at CERN. In this case a direct comparison between the DCU measurement and the ARC FE adapter measurement can be implemented in ARCS.

The information that is written into the log file after the DCU test reads as follows:

```
Start of DCU response test
ARC FE : I(V125)=0.184 A, I(V250)=0.464 A, V(V125)=1.24 V, V(V250)=2.49 V
DCU : V(V125)=1344 Counts, V(V250)=2687 Counts
ARC FE : I(V125)=0.180 A, I(V250)=0.448 A, V(V125)=1.22 V, V(V250)=2.43 V
DCU : V(V125)=1316 Counts, V(V250)=2631 Counts
ARC FE : I(V125)=0.176 A, I(V250)=0.432 A, V(V125)=1.19 V, V(V250)=2.37 V
DCU : V(V125)=1284 Counts, V(V250)=2569 Counts
ARC FE : I(V125)=0.176 A, I(V250)=0.412 A, V(V125)=1.16 V, V(V250)=2.33 V
DCU : V(V125)=1252 Counts, V(V250)=2506 Counts
Hybrid LV consumption reasonable
DCU output of AL1 & AL2 reasonable
TestResult=passed
```

6.2.7 Pedestal and Noise Tests

In order to provide a fast characterization of the hybrid data performance, the pedestal and noise measurements done are based on the same calculation algorithms as discussed in the sections 6.1.1 and 6.1.3. The data samples are obtained from N events (50 to 2000 events can be selected) while operating the APV chips in peak mode with the inverter switched on. In the present ARCS version, a pedestal sample is marked as bad, if the difference of the maximal and the minimal pedestal values (per APV) exceeds 30 ADC counts.

The common mode subtracted noise is assessed via absolute cuts combined with percentage thresholds. The noise thresholds are set to:

$$\begin{aligned} CUT_{abs}^{min} &= 0.2 \text{ ADC counts,} \\ CUT_{abs}^{max} &= 2.0 \text{ ADC counts, and} \\ CUT_{perc} &= 0.2. \end{aligned}$$

The noise test fails, if a hybrid has more than 0.8% bad channels (see section 6.2.10 for the grading of a hybrid). All data samples are written into a separate ASCII data file. This is also true for the calibration pulse test described in the next section.

The log file includes the following information after finishing the pedestal and noise tests:

```

Start of pedestal & noise test
(only assigned APVs are considered)
Number of taken events: 500
APV #0 0x20 (8 bits: 0x40):
Pedestals ok
Noise: number of bad channels: 0
APV #1 0x21 (8 bits: 0x42):
Pedestals ok
Noise: number of bad channels: 0
APV #4 0x24 (8 bits: 0x48):
Pedestals ok
Noise: number of bad channels: 2
APV #5 0x25 (8 bits: 0x4a):
Pedestals ok
Noise: number of bad channels: 0
Total number of bad channels: 2
TestResult=passed

```

6.2.8 Fast Calibration Pulse Test

The *fast calibration pulse test* is meant to check the APV channel response to an injected amount of charge. The requested charge is equivalent to 36,250 electrons (ICAL = 58). In contrast to the advanced pulse shape test, only the signal height per channel at a fixed sampling time (LATENCY = 16 and CSEL = 63) is measured. The trigger pattern sent to the APVs periodically is “11000000(spacer)00010011” while the spacer value is set to eight. Moreover, the MODE register is set to one (refer to section 6.1.5).

At the beginning of the test procedure, a short pedestal run is performed in order to correct the data measured with respect to the baseline. Then the calibration pulses are injected group-wise by varying the CDRV register. At each CDRV setting the mean responses of the corresponding channels to the calibration pulses are determined (N events are used). Figure 6.31 depicts the data obtained from a fast calibration test.

The assessment of the channel behaviour is done by using the absolute threshold strategy. In this sense a certain APV channel is flagged as bad, if its calibration pulse response does not exceed

$$CUT_{abs}^{min} = 40 \text{ ADC counts.}$$

In analogy to the noise measurement, the fast calibration pulse test fails, if a hybrid has more than 0.8% bad channels.

The results of the fast calibration pulse test are also written into the log file:

```

Start of calibration pulse test
(only assigned APVs are considered)
APV #0 0x20 (8 bits: 0x40): no bad channel found
APV #1 0x21 (8 bits: 0x42): no bad channel found

```

```

APV #4 0x24 (8 bits: 0x48): no bad channel found
APV #5 0x25 (8 bits: 0x4a): no bad channel found
Total number of bad channels: 0
TestResult=passed

```

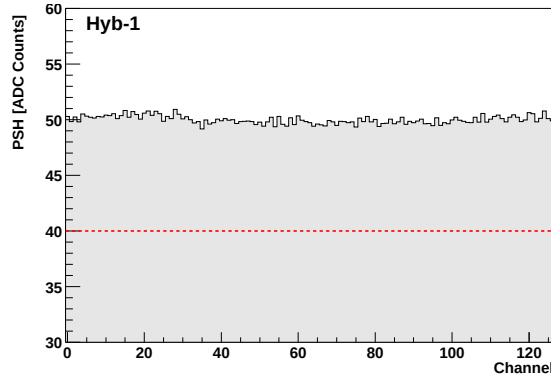


Figure 6.31: Channel responses to calibration pulses. The dashed line depicts the cut criterion.

6.2.9 General Remarks

The individual test procedures often rely on results already obtained in previous tests. For instance, the address scan is the basis for nearly all tests as it provides the chip communication. To save time, certain procedures are only done when required for the first time. This means that the APV assignment is performed only once and then the results are used in consecutive test procedures.

A specific TPLL chip test has not been implemented in the fast test procedures yet. Apart from the I²C address scan (which should reveal the addresses 0x88, 0x8a, 0x8c, and 0x8e), the functionality of this chip is solely derived indirectly from the performance of the APV chip. If clock and trigger signals are not generated correctly, the APV data output does not match the expected signature, for instance. Nevertheless, recent hybrid cooling results at CERN show temperature dependent TPLL failures with respect to the internal autocalibration circuit [93]. If the hybrid power has to be switched off at low temperatures, sometimes the TPLL can not be reset. As a consequence, an advanced test of this chip has to be defined and implemented in the fast test procedures in the future.

Test Characteristics

The fast test should be used at the beginning of all test programs, since it verifies the basic functionality of the test setup and the test object. Moreover, it is the only test that checks the I²C communication with the ASIC chips on the hybrid (APV, APVMUX, TPLL, and DCU). Any failure in the fast test (apart from the pedestal, noise, and pulse shape measurements) would indicate a gross problem for an entire chip. The duration of a complete fast test is about 50 s when using 500 events for the measurements.

6.2.10 The FHIT Test Procedures

The industrial test procedure provided by the FHIT system [71] consists of three sub-tests, called *connectivity test*, *electrical test* and *functional test*. The first two tests are performed using the FHIT board whereas the latter test is based on ARC board features and is composed of a specific configuration of the fast test procedures discussed in section 6.2. Figure 6.32 depicts the FHIT test panel which is also realized with LabVIEW 6.i and looks similar to the fast test control in ARCS.

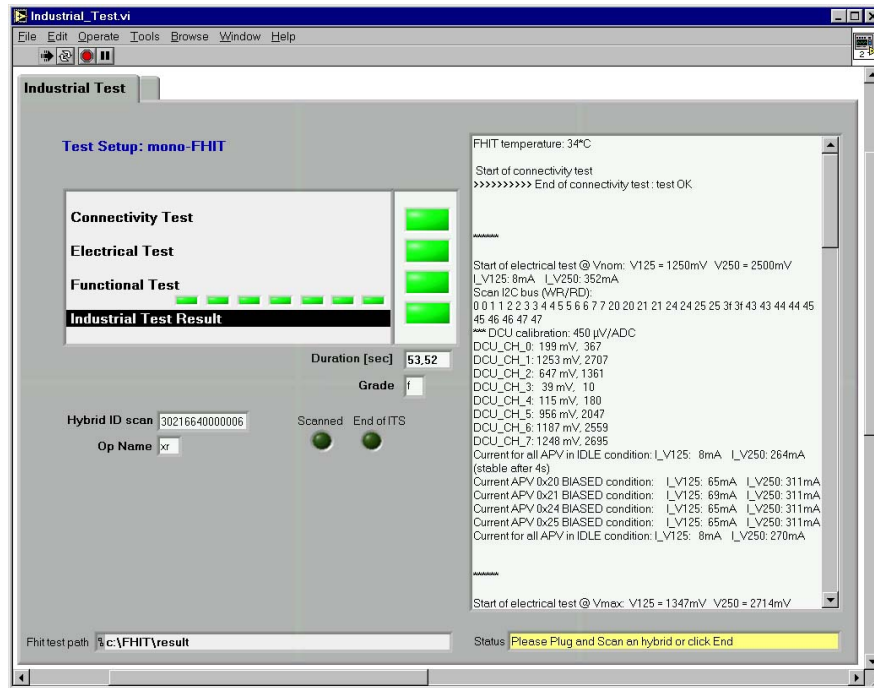


Figure 6.32: Screen-shot of the FHIT software.

All important pre-settings are defined in a specific configuration file that is read by the FHIT software. Based on this information the FHIT test can be started when pressing the START button located at the front side of the FHIT aluminium box (see figure 5.9 (a)). If all connections are done correctly, the test is performed automatically in less than 100 s. The obtained data samples and test results are monitored and written into an ASCII file. The global test results are indicated by lights on the software panel as well as by LEDs on the FHIT test box. Table 6.10 gives the definition of the used LED color codes. To grade a bare hybrid, the number of bad channels is considered as well as the functioning of the ASIC chips. In this sense, a FE hybrid is characterized as

- grade A*, if it has less than 0.4% bad channels,
- grade B*, if it shows more than 0.4%, but less than 0.8% bad channels,
- bad*, if it has more than 0.8% bad channels, or any bad functioning chip.

LED	Color	Meaning
front	green	grade A hybrid
	blinking green	grade B hybrid
	orange	grade C hybrid (if defined)
	blinking orange	grade D hybrid (if defined)
	red	bad hybrid
	blinking red	test failed (fatal error)
	off	hybrid ID performed
top	green	hybrid (un)plugging allowed
	orange	waiting for information, hybrid (un)plugging allowed
	red	hybrid powered on, hybrid unplugging not allowed
all	blinking red	FHIT powered on with hybrid connected

Table 6.10: LED color code.

Source: [71]

Connectivity Test

The connectivity test is a passive test without applying the FE hybrid with power. Each pin of the hybrid NAIS connector is checked in order to find open or short circuits. The procedure is repeated ten times if everything works well. It lasts less than five seconds in total.

Electrical Test

During the electrical test, the hybrid power consumption (voltages and currents) are observed. In addition, the I²C communication with the hybrid ASICs is proved. In particular the DCU chip is calibrated at this test stage and the DCU linearity is verified. The electrical test is performed with different hybrid supply voltages:

$$\begin{aligned}
 V_{125_{nominal}} &= 1.25 \text{ V} , & V_{250_{nominal}} &= 2.50 \text{ V}, \\
 V_{125_{maximal}} &= 1.30 \text{ V} , & V_{250_{maximal}} &= 2.70 \text{ V}, \\
 V_{125_{minimal}} &= 1.10 \text{ V} , & V_{250_{minimal}} &= 2.20 \text{ V}.
 \end{aligned}$$

Functional Test

The third part of the FHIT test is represented by the functional test procedure. The FHIT board is switched to the so-called *transparent mode* and the FE hybrid is then controlled completely by the ARC board. The tests performed during this procedure are taken from the ARCS fast test: setup self test, APV I²C access test, APV data test, APVMUX test, pedestal and noise measurement, and fast calibration pulse test. All cuts and thresholds used in the functional test are defined in the previous section.

6.3 Data Handling

Data handling and storage is a point of extraordinary interest in the quality assurance chain. Due to the large number of FE hybrids and modules to be assembled and tested, an appropriate data organization is needed. Thus all results of the different test procedures will be written into *local files (LF)* meant to retain at the local test centre. Exclusive data are taken from these local files and filled into so-called *data base files (DB)* which are transferred to the *CMS tracker data base* located at IPN⁹ Lyon [94]. The data base cumulates the most important test results obtained at the different production steps and centres. By this means a centralized assembly supervision is guaranteed providing track to the history of every produced component.

In the following sections, some details concerning LF and DB creation will be presented.

6.3.1 Creating ROOT Files

In the ARCS framework local files are based on the ROOT system [82]. ROOT provides an object oriented framework (using C++) with all the functionality needed to handle and analyse large amounts of data in a very efficient way. Having the data defined as a set of objects, specialized storage methods are used to get direct access to separate attributes of the selected objects, without having to touch the bulk of the data. Included are histogram methods, data fitting, function evaluation, graphics and visualization classes in order to allow the setup of an analysis system that can query and process the data interactively or by command lines.

Several ROOT classes of version 3.05/02 for WINDOWS are incorporated in the ARC software providing the data storage in form of histogram, vector, or string objects. All data and results obtained from a hybrid's or module's quality test are accumulated in a *ROOT file* typically named "*bar code.root*", with *barcode* the identity number of the test object (as introduced at the beginning of this chapter).

In general, a ROOT file may contain directories and objects. It is stored in machine independent format and may be compressed in several levels. A ROOT file is allowed to have a maximum size of 2 GBytes. Using the ROOT browser option, it is possible to access the different object types included in the corresponding ROOT file. In particular histograms can be displayed easily this way. Thanks to ROOT's command line interpreter and script processor *CINT*¹⁰ individual *macros* can be written to extract certain information from a ROOT file automatically. For instance, this allows a fast generation of analysis plots.

In order to provide a useful organization of the various data blocks originating from different test procedures, a specific ROOT file structure has been defined. Figure 6.33 illustrates the global arrangement of the test results and information within the storage file. A tree structure is used to allow simple navigation through the important data objects. The main directories are labeled "*Record#*", with "*#*" being an integer number. Every time a new qualification test is initiated, a new record is created. By this means

⁹Institut de Physique Nucleaire de Lyon, France.

¹⁰C++ INTerpreter

the same object can be tested several times while all information is written separately into a single file. This is an important aspect during a long-term test where tests have to be performed at different environment temperatures.

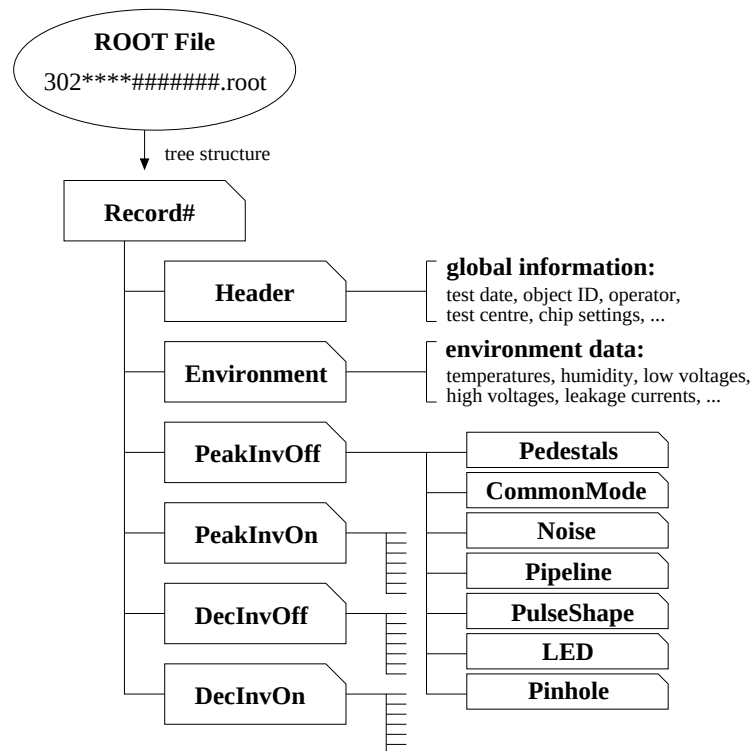


Figure 6.33: Schematic root file structure created by ARCS.

Each “Record#” folder typically includes sub-directories called “Header”, “Environment”, “PeakInvOff”, “PeakInvOn”, “DecInvOff”, and “DecInvOn”. The folder “Header” includes some global facts concerning date of the test, bar code number of the checked object, and operator’s name, for example. Environmental test conditions, such as temperatures, humidity, high and low voltage supplies, are stored in folder “Environment”. Depending on the MODE register settings (peak or deconvolution mode, inverter on or off) all tests performed are written into the corresponding directories. The results of the different test procedures discussed in section 6.1 are stored in separate sub-directories.

Figure 6.34 depicts a screen-shot of the ROOT object browser for the example of a pinhole test. The contents of each test folder includes APV specific measurements in form of histograms, summarizing hybrid results, and assessment results.

6.3.2 Creating XML Files

In order to store test results in the tracker database, specific XML files (DB) have to be generated that include the essential data and information in text form ordered in a tree

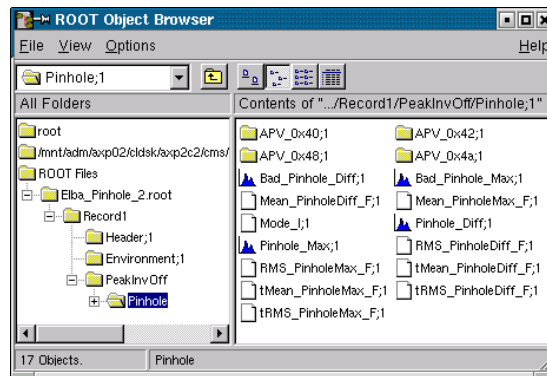


Figure 6.34: ROOT object browser. The typical contents of the “Pinhole” folder is listed in the right part of the window.

structure. The results are finally stored in database tables. The definition of an XML file in terms of module qualification can be found at [95].

The conversion of ROOT files into XML files is realized with the C++ framework of XERCES¹¹ incorporated in ARCS. A specially designed LabVIEW interface allows to select a certain ROOT file to be converted (see figure 6.35). The corresponding file structure is then read and visualized “Record”-wise. Finally, the operator has to select the data to be filled into the XML file by specifying “Record#” and the APV MODE register setting.

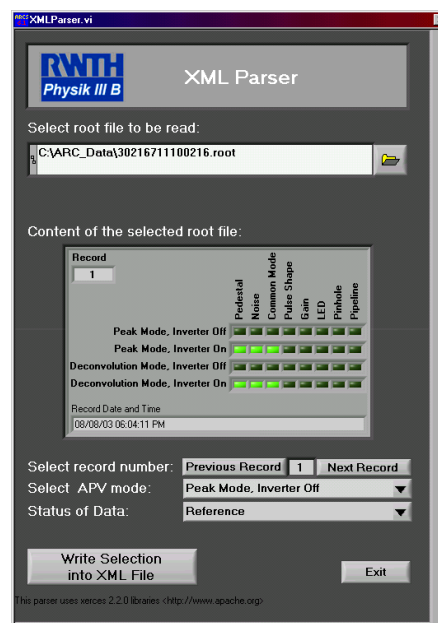


Figure 6.35: The XML file creator incorporated in ARCS.

¹¹Version c2_2_0-win32.

Chapter 7

Pre-series of TEC Wedge-Ring-6 Modules

Some of the potential future problems may be the non-homogeneity of the production between the various assembly and test centres. Thus all participating centres have to be qualified and calibrated before entering the large-scale manufacturing. Various aspects need to be verified locally:

- *production capability* → Are all required tools, gantries¹, or jigs² operational?
- *test capability* → Is the test equipment installed, understood, and operational?
- *comparability* → Is the production quality the same in all centres?

Under these considerations, two pre-series of altogether 21 TEC wedge-ring-6 modules were built by the TEC collaboration in 2002. In the first batch of modules, called *express-line 1*, twelve modules were produced in March. Based on the experiences gained with this express-line, the module assembly of a second series, the *express-line 2*, was initiated half a year later. As the name “express-line” suggests, the modules were produced in a short time period in advance of any scheduled large-scale production activity. As a consequence, the modules are not composed of final components. For example, ceramic hybrids are used to equip all modules instead of flex-rigid FR-4 hybrids. The specifications of the sensors are given in figures B.4 and B.5. The sensor’s thickness is 400 µm for the express-line 1 batch and 500 µm for the express-line 2 series. Figure 4.3 shows the mechanical layout of an express-line 1 module.

After the assembly in Karlsruhe, Lyon, or Vienna, all modules were cumulated in Aachen to be characterized in detail by the ARC system. This allowed the optimization of existing test procedures implemented in the ARC software and the development of new tests. The test procedures and the deduced quality criteria described in chapter 6 are results of the express-line measurements. In a final step, the TEC test centres were equipped with at least one express-line module to improve their test environment

¹A gantry is a tool that provides the automated module assembly.

²This includes the bonding jigs, for example.

and to prove their test capabilities. The TEC institutes that contributed to the express-line series are RWTH Aachen, UIA³ Antwerp, ULB⁴ Brussels, IEKP⁵ Karlsruhe, UCL Louvain-la-Neuve, IPN⁶ Lyon, IRES⁷ Strasbourg, HEPHY⁸ Vienna, and ETH⁹ Zurich.

In the following paragraphs the test programs performed on both express-line series and their corresponding results will be presented. For simplicity, the modules will be named “Ex1-#” or “Ex2-#” with # = 1, 2, ..., 12 or 9, respectively. The corresponding bar codes can be found in table C.2.

Module Grade Definition

The grading of a module is similar to that of a FE hybrid. In particular the number of bad channels contribute to the quality assessment of the modules. Other important aspects are the high voltage behaviour and the functioning of the hybrid’s components. Thus a module is called a

- *grade A* module, if it shows less than 1% bad channels and passes the IV test,
- *grade B* module, if it has between 1% and 2% bad channels and passes the IV test,
- *grade C* module, if the IV test reveals suspicious behaviour,
- *grade F* module, if it has more than 2% bad channels or the hybrid carries any bad ASIC.

These definitions represent the present status of module grading as described in [91].

7.1 Express-line 1

The express-line 1 module production was the first attempt to assemble more than one prototype detector in a short period using as much automated production tools as operational at that time. From the point of view of the ARC system, the main focus was laid on the following aspects:

- validation of the ARC test setup,
- improvement of test procedures implemented in the ARC software,
- deduction of new tests, and
- determination of failure signatures in different tests.

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⁴Université Libre de Bruxelles, Belgium.

⁵Institut für Experimentelle Kernphysik, Germany.

⁶Institut de Physique Nucléaire de Lyon, France.

⁷Institut de Recherches Subatomiques, France.

⁸Institut für Hochenergiephysik der Österreichischen Akademie der Wissenschaften, Austria.

⁹Eidgenössische Technische Hochschule, Switzerland.

7.1.1 Test Environment

The transportation and storage of the twelve express-line 1 modules were done in two special plastic boxes provided by IPN Lyon. Figure 7.1 depicts one of these boxes which are suited to house up to ten modules mounted on their aluminium carrier plates. The carrier plates can be pushed into styrofoam blocks meant to absorb mechanical shocks during the transportation.

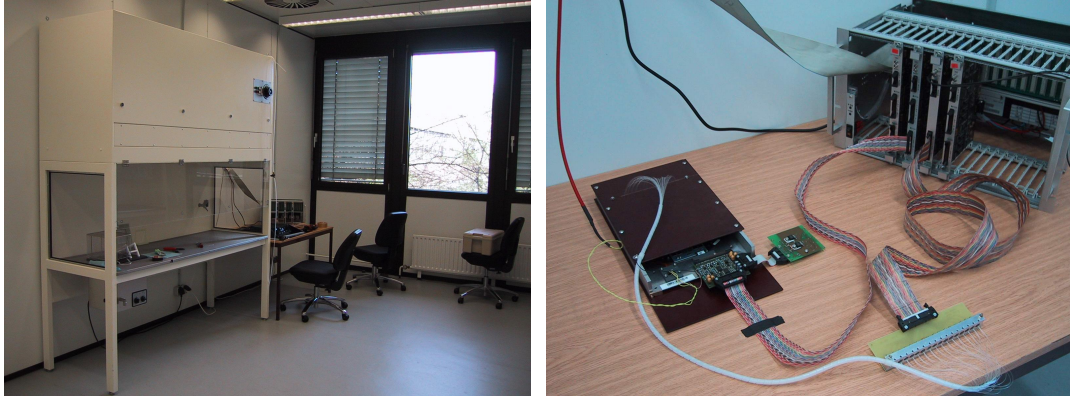


Figure 7.1: Transport box suited to hold up to ten modules mounted on their carrier plates.

The ARC test setup was operated in a clean room¹⁰ in order to guarantee an appropriate environment for measurements at stable temperature and humidity conditions. Figure 7.2(a) pictures the clean room with one of its four class 100 flow boxes. This room is also equipped with a microscope allowing a detailed *optical inspection* of the module's sensors or bond wires. Pictures of certain sensor sections are depicted in the figures B.3(a) to B.3(c).

All measurements were performed with the minimal ARC setup extended by one LEP_16 module as shown in figure 7.2(b). ARCS version 5.1 was used to operate the ARC equipment and to analyse the data. In order to bias the modules, a C.A.E.N. high voltage power supply of type Mod. N126 was used whereas the leakage currents were measured with the current monitor CUMO [88].

¹⁰Per Federal Standard 209E, the numeric classification means how many particles larger than $0.5\ \mu\text{m}$ are acceptable within a classified clean environment. Thus a class 100 environment means that no more than 100 particles larger than $0.5\ \mu\text{m}$ exist in any given cubic foot of air. The measurement of the institute's clean room revealed class 200.



(a) Clean room with one flow box.

(b) ARC test setup.

Figure 7.2: Test environment used for the express-line 1 measurements.

7.1.2 Test Procedures

The test program for express-line 1 modules was composed of test procedures discussed in chapter 6. The following measurements were done at ambient temperature:

- 1) The complete set of **fast tests** (setup self test, slow control test, APV I²C access test, APV data test, APVMUX and DCU tests, pedestal and noise measurements, as well as fast calibration pulse test) was performed using 500 events per measurement.
- 2) The **pedestal** *PED* and **common mode subtracted noise** *NOI* measurements were based on 1000 events while operating the APVs in peak mode with the inverter switched off. A group-wise common mode corrected noise calculation was not available for the express-line 1 tests (refer to section 6.1.2).
- 3) The randomly triggered APV **pipelines** were checked demanding at least 100 events per pipeline cell for pedestal and noise calculations (in peak mode).
- 4) The **calibration pulse shape tests** were done using 10 events per measuring point (in peak and deconvolution mode, with inverter off, and ICAL = 112). The implemented pulse shape fit routine provided the extraction of pulse shape heights *PSH* and rise times *RT*.
- 5) An early release of the **pulsed light test** was used to prove the channel response to external light. 100 events per measuring point were taken to evaluate the channel response *LED*. The deduced data was not corrected for the light spot structure (see section 6.1.6).
- 6) An **IV curve** was measured for each module in a voltage range between 0 V and the individual breakdown voltage (in steps of 100 V). The modules were not flushed with dry air or nitrogen during the measurements.

- 7) For each express-line 1 module, a **raw data** sample of 10,000 events was stored to allow for a re-calculation of pedestal and noise data.

7.1.3 Results of the Measurements at Ambient Temperature

A summary of the most important test results is given in table 7.1. In total, 20 different strips were identified as bad channels by at least one of the test procedures 1) to 5). Thus only 0.3% of all channels were affected by one of the three main faults introduced in section 4.2.

Nine open bonds were observed of which two open bonds belong to un-bonded pinhole defects on the modules Ex1-6 and Ex1-11. These two faults were already found during the sensor qualification procedures at the *Quality Test Centres* [41].¹¹ Open bond failures showed up in all tests with identical signatures with respect to regular channels: higher noise, higher pulse height, shorter pulse rise time, and lower responses to LED or laser sources. Every open bond was also found in an optical inspection.

Four shorts occurred on the modules Ex1-2 and Ex1-4 which could not be found optically. The noise behaviour is not unique whereas the pulse shape measurement is a powerful tool to spot this kind of failure. The pulse heights were always lower than those of regular channels thereby having shorter rise times. The LED measurement is not suited to observe all shorts, if both strips are illuminated with nearly the same intensity at the same time. A laser system is able to hit single channels thus allowing the reliable determination of all shorts.

Pinholes showed up in the test procedures for the express-line 1 series, but could not be characterized by a unique signature. The five pinholes (plus the two un-bonded pinholes) indicated in table 7.1 were already known from initial sensor qualification tests. These sensor test results were very important for the development of reliable test routines with respect to the diagnostic of a pinhole failure.

Fast test results and APV pipeline measurements are not included in the summary table, since both tests revealed no hints concerning other flaws than those observed by the tests mentioned above.

The assessment of the breakdown performance was difficult due to the detector's sensitivity to environmental conditions. Taking into account that the modules were not flushed with nitrogen, the high voltage breakdown results (if available) were though included in the grading strategy for the express-line 1 series. Only two modules suffered an electrical breakdown below or near the claimed limit of 450 V whereas five others only exceeded this value by a small amount.

From these points of view, the express-line 1 results are encouraging with respect to a large-scale production. The manufacturing methods provide robust and operational silicon detector modules.

¹¹The **Quality Test Centres** are responsible for the acceptance tests of the silicon sensors. These QTCs are capable of spotting pinholes at sensor level by measuring the current between AC and DC pads strip-by-strip. A current above 1 nA indicates a pinhole. Moreover, the coupling capacitance provides the probing of pinholes.

Defect Location		Defect Found								Grade
Module	Strip	NOI	PSH	RT	LED	Laser	Type of Defect	Breakdown		
Ex1-1	–	<	>	<	<	<	none	o	A*	
Ex1-2	303	×		×	×	×	(pinhole)		B	
	168		×	×	×	×	open			
	166		×	×	×	×	open			
	141		×	×	×	×	open			
	137		×	×	×	×	open			
	82			×	×	×	(short)			
	83		×	×	×	×	(short)			
	71	×		×	×	×	open			
	2		×	×	×	×	open			
Ex1-3	–						none	o	A*	
Ex1-4	420			×		×	(short)		C	
	419		×	×	×	×				
	71		×	×	×	×				
	70		×	×	×	×				
Ex1-5	–						none	≈ 500 V	A	
Ex1-6	164		×	×	×	×	open	≈ 610 V	A	
Ex1-7	–						none	≈ 480 V	A	
Ex1-8	33		×	×	×	×	open	≈ 800 V	A	
Ex1-9	419	×	n.s.	n.s.	×	×	(pinhole)	≈ 530 V	A	
	264		×	×	×	×	(pinhole)			
Ex1-10	505	×	n.s.	n.s.	×	×	(pinhole)	≈ 500 V	A	
	323		×	×	×	×	(pinhole)			
Ex1-11	503		×	×	×	×	open	≈ 450 V	C	
Ex1-12	–						none	≈ 500 V	A	

Table 7.1: Summary table of the express-line1 test results. The nomenclature is as follows: < (>) value smaller (larger) than values of regular channels, × defect found in this type of test, o test not done, “n.s.” no signal, (type of defect) defect not found in optical inspection, and * grading without considering the IV test. The laser measurements mentioned here were done by J. Olzem, I. Physikalisches Institut B.

A few remarks have to be added to these results. Noisy APV edge channels, which typically included the channels 0 to 2 and 125 to 127, were not taken into account with respect to the module's grading if they were not suspicious in another test than in the noise measurement. Figure 7.3 presents the noise signatures of the two outermost APV chips of one module. It can be observed that the outermost readout channels of a module, which means channel 0 on APV 0x40 and channel 127 on APV 0x4a, show even more noise than the inner chip edges. As discussed in section 6.1.3, the noise behaviour of the APV edges can be improved providing good shielding and grounding conditions.

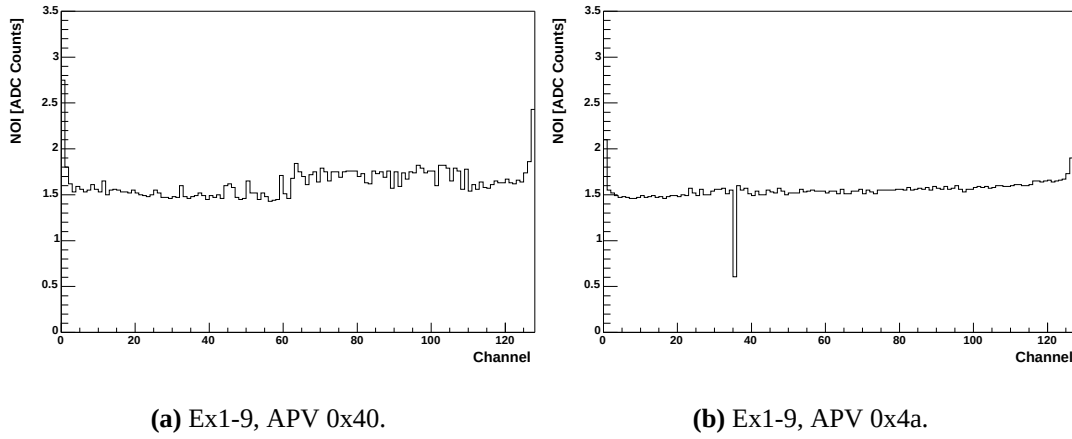


Figure 7.3: Two typical measurements of the common mode subtracted noise. The edges of both APVs are significantly noisier than the remaining channels. Since no other test procedure announced a failure at the edges, these channels were not flagged as bad. Only one real bad strip is included in the data samples shown, a pinhole on channel 35 of APV 0x4a.

Figures 7.3(a) and 7.3(b) also illustrate that the calculation method of the common mode subtracted noise used in ARCS 5.1 was not sufficient to guarantee a low number of falsely marked channels in an automated channel assessment. The measurements often revealed non-homogeneous noise distributions along the chips. These signatures were likely due to common mode effects that were not common to all channels of a chip, but only to a certain group of channels. As a consequence, the noise calculations in ARCS were modified in order to apply a group-wise common mode correction to the raw noise measured (refer to section 6.1.2).

A basic aim of the module pre-series was to prove the capability of a homogeneous module production characterized by a low failure rate. In addition to the grading of the individual modules, an overall view of the different quantities measured is useful. Figure 7.4 presents the truncated mean values¹² for common mode subtracted noise $\overline{NOI}_{trunc}$, calibration pulse heights $\overline{PSH}_{trunc}$, and rise times $\overline{RT}_{trunc}$, as well as for

¹²See the discussion of the assessment strategies in chapter 6 for the definitions of “truncated mean” and “truncated RMS”. Since the values were calculated APV-wise, the following indices were used: $i = 0$ and $N = 127$.

light responses $\overline{LED}_{trunc}$ deduced from the express-line 1 modules Ex1-1 to Ex1-12. Each module is characterized by four APV mean values. By this means, the homogeneity of an individual module can be checked and compared to the results obtained from the other modules. The global average of all values is superimposed and can be used to illustrate the uniformity of the complete production batch. The module results are very consistent with each other showing fluctuations of less than 10%. The comparability of different modules confirmed the feasibility of the module concept in terms of mechanical structure and manufacturing. Moreover, the measurements proved the stability and robustness of the test system and its software tools.

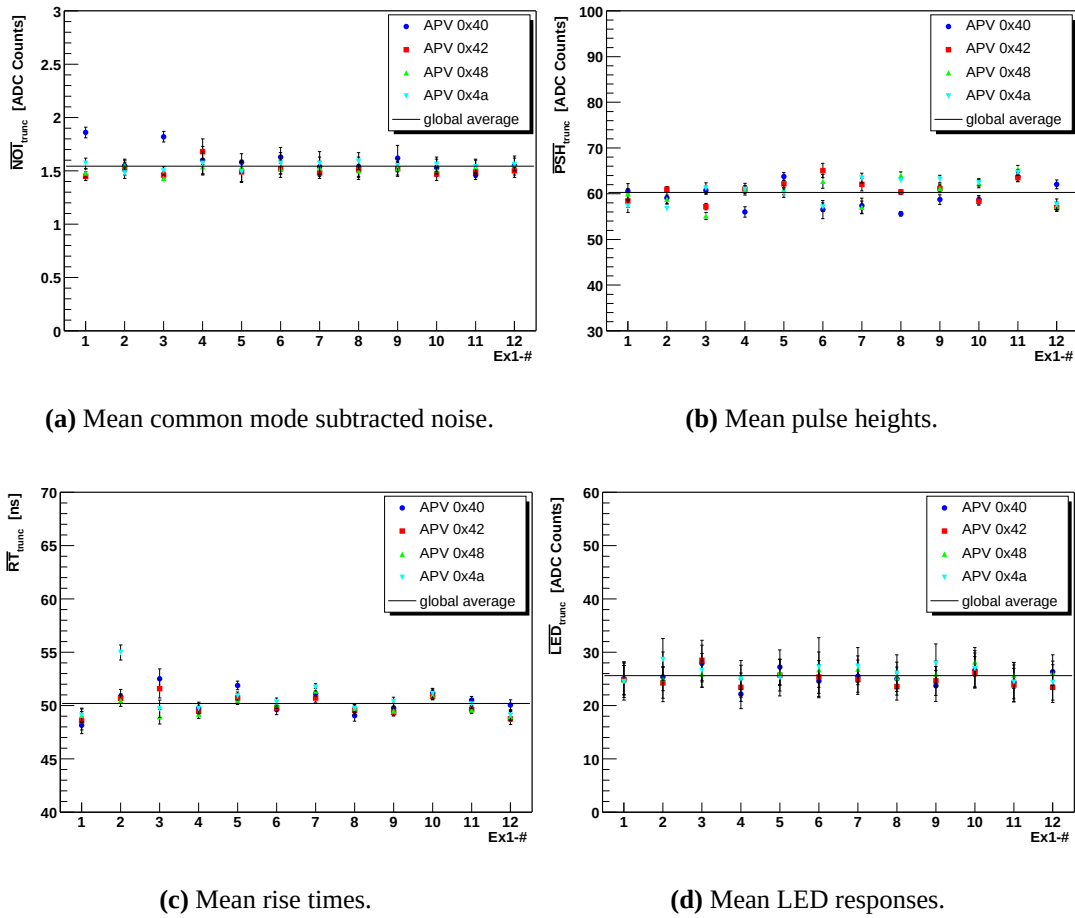


Figure 7.4: Characterization of the express-line 1 modules. All quantities were measured in peak mode and the errors indicate the corresponding standard deviations. The *global average* values are superimposed as solid lines. Table E.1 includes all data shown.

7.1.4 The Cosmic Ray Muon Test Facility

Since the energy deposited in a silicon detector translates directly into charge, particles with known initial energy can be used to determine the relation between a digitized

A crucial point with respect to a reliable signal measurement is the correct adjustment of the sampling point defined by the LATENCY register. As shown in figure 7.6, the monitoring feature of ARCS can be used to determine the optimal sampling time. When running the APV chips in the 3-sample mode and sending three consecutive event trigger (“1001001”), nine APV frames taken from neighbouring pipeline cells can be extracted and displayed. The LATENCY register setting has to be varied until a triggered muon event shows up with a maximal signal height in the first frame monitored. In the present example, the LATENCY value has to be shifted by two bunch crossing units to guarantee a reliable measurement.

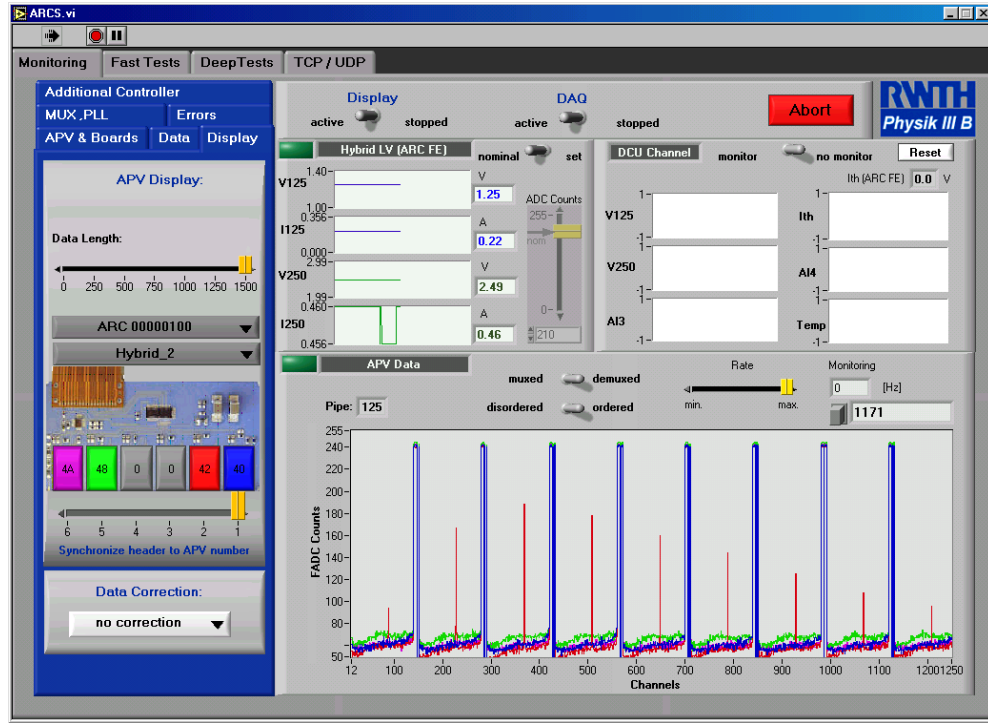


Figure 7.6: ARCS display of a triggered muon event. Nine APV frames from consecutive pipeline cells are displayed including a single muon hit (red signal) in the middle of one APV. The different signal heights illustrate the time dependent behaviour of the muon pulse. Source: [96]

In order to distinguish the signal induced by a traversed particle from normal noise, it is demanded that the signal S_i^n of channel i (see equation 6.9) exceeds a certain threshold. In the present case, a particle’s signal is identified, if $S_i^n > 3.0 \cdot NOI_i^{raw}$. Those strips meeting this condition are combined to so-called *clusters* of neighbouring channels. Thereby the width of a cluster is defined by a left border (channel l) and a right border (channel r). By this means, the *cluster charge* S^n per event n is determined by:

$$S^n = \sum_{i=l}^r S_i^n. \quad (7.1)$$

Figure 7.7(a) illustrates the cluster identification condition implemented in the IRIS environment. Four adjacent strips fulfill the threshold condition and build one cluster. A five days cosmic ray measurement, which is equivalent to about 13,000 events sampled, delivered a cluster charge distribution as shown in figure 7.7(b). The module was operated at 100 V. Due to the Landau theory on the energy loss of charged particles in case of very thin absorbers, the signal distribution can be described by the function given in equation 7.2.

$$f_{landau}(x) = p_0 \exp \left(-\frac{1}{2} \left(\frac{x - p_2}{p_1} + \exp \left(-\frac{x - p_2}{p_1} \right) - 1 \right) \right), \quad (7.2)$$

where p_0 is a scale factor defining the maximum of the distribution and p_1 determines its width. p_2 is the most probable value. Since the condition of a very thin absorber

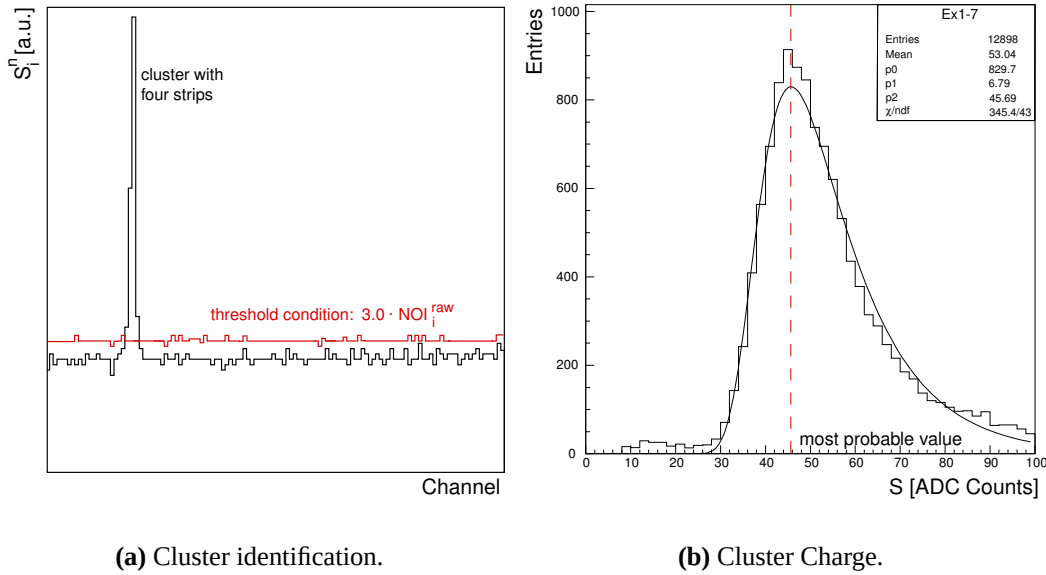


Figure 7.7: Cluster charge identification from measurements of cosmic ray muons.

Source: [96]

reaches its limit for a 400 μm thick silicon sensor, slight deviations of the fit function from the measured data occur. Nevertheless, the quality of the fit is sufficient to extract the most probable value of the distribution given by $S \approx 45$ ADC counts. This value corresponds to the most probable number of electrons a traversing MIP creates in a 400 μm thick silicon sensor which can be estimated to about 30,000 electrons due to section 2.1.1. As a result, the ARC system can be characterized by the following relation:

$1 \text{ ADC count} \equiv 670 \text{ electrons.}$

7.2 Express-line2

Based on the experience gained with the express-line 1 series some test procedures of ARCS could be optimized and one new type of test, meant to find pinholes in a unique way, was implemented in the software routines of ARCS 5.11. This software package was used to characterize the second batch of TEC wedge-ring-6 modules. During these tests, the main focus was laid on the following aspects:

- determination of failure signatures in different tests at different temperatures,
- improvement of present test procedures,
- test of the module performance at different temperatures, and
- verification of the cooling box's functionality.

7.2.1 Test Environment

The express-line 2 modules were tested in two environments, in the clean room described in section 7.1.1 at ambient temperature and in the cooling box presented in section 5.3. The cooling box was used to perform temperature cycles of the modules lasting about eight hours per test program. The temperature measured at a module carrier plate served as reference temperature for the regulation. The measurements were done in a temperature range between ambient temperature and $-10\text{ }^{\circ}\text{C}$ (on the carrier).

Figure 7.8 depicts the test setup used for the cooling tests. Four modules were installed in their small test boxes and placed into the cooling box at once thus requiring two ARC boards and four ARC FE adapter for the readout. During a temperature cycle only one module could be equipped with a LED array above the sensor providing light measurements at different temperatures. The cooling box was controlled by the COOLI module (see section 5.3) using the ACDC software package mentioned in section 5.4.3.

7.2.2 Test Procedures

The test program of the nine express-line 2 modules was divided into two parts, single measurements at ambient temperature and periodical tests during the temperature cycles. While the measurements at ambient temperature were meant to determine production flaws in particular, the cooling tests were used to check the quality of the bond wires welded. In addition, the performance of a module and its components in a cold environment was of great interest. In order to determine the production flaws at ambient temperature, the complete test program was composed of the following measurements:

- 1) The complete set of **fast tests** (setup self test, slow control test, APV I²C access test, APV data test, APVMUX and DCU tests, pedestal and noise measurements, and fast calibration pulse test) was performed using 500 events per measurement.

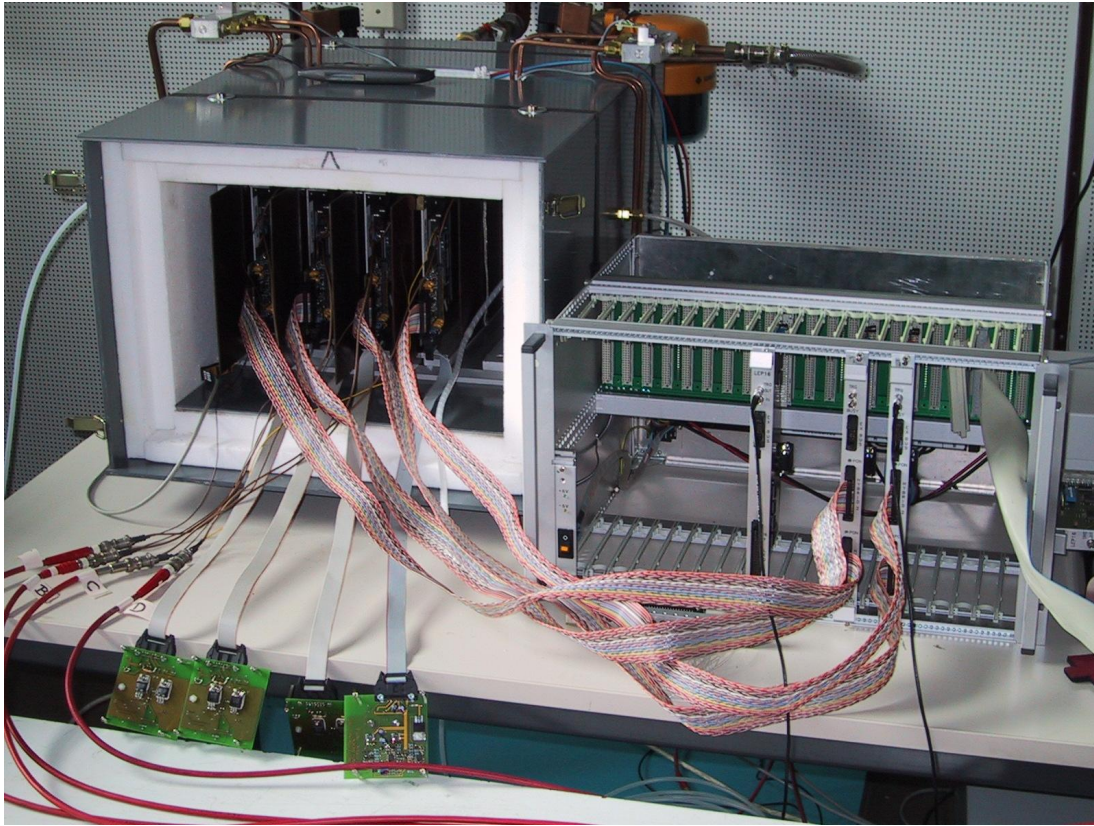


Figure 7.8: Cooling box test setup used for temperature cycles of the express-line 2 batch. Four modules were installed in the box simultaneously and the required cables were passed through the front door of the box (opened in this figure).

- 2) The **pedestal** PED , **common mode** CMN , **raw noise** NOI^{raw} , and **common mode subtracted noise** NOI measurements were based on 10000 events (in peak and deconvolution mode, with inverter on).
- 3) The randomly triggered APV **pipelines** were also checked demanding at least 100 events per pipeline cell for pedestal and noise calculations (in peak and deconvolution mode, with inverter on).
- 4) The **calibration pulse shape tests** were done for 10 events per measuring point (in peak and deconvolution mode, with inverter on, and $ICAL = 58$). The pulse shape fit routine provided the extraction of pulse shape heights PSH and rise times RT .
- 5) The **pulsed light test** was used to prove the channel response to external light (in peak mode, with inverter on). 100 events per measuring point were taken to evaluate the channel response LED . The deduced data was not corrected by the light spot structure.

- 6) The **continuous light test** was used to search for pinholes (5 events per measuring point).
- 7) An **I-V curve** was measured for each module in a voltage range between 0 V and the individual breakdown voltage (in steps of 100 V). The modules were not flushed with dry air or nitrogen during the measurements.

The program during the temperature cycles was more complex with regard to the test logistics, since the modules were tested at different locations (outside and inside the cooling box) and at various temperatures (+20 °C, 0 °C, and −10 °C):

- Before the modules were installed in the cooling box, a complete quality check (as listed above) had to be done in peak and deconvolution mode with the inverter switched on and off.
- When the modules were placed into the cooling box and connected to the readout system, only pedestal, common mode, and noise measurements, as well as pulse shape tests were performed. The same kinds of measurements were done at the temperatures mentioned above.
- In a last step, the cooling box was warmed up and the modules were finally checked completely.
- Certain modules were also used to determine important module properties at different temperatures, such as light responses or leakage currents drawn.

7.2.3 Results of the Measurements at Ambient Temperature

Table 7.2 gives a summary of the most important results of the express-line2 qualification tests at ambient temperature. In total, nine different strips were identified as bad channels by at least one of the test procedures 1) to 6). This means that only 0.2% of all channels were affected by either an open bond or a pinhole failure. Shorts were not present in that batch of modules.

The small number of open bonds (of which two bonds were removed due to pinhole faults found at sensor test level) emphasizes the accurate bonding quality of the corresponding centres. In peak and in deconvolution mode, open bonds showed higher pulse heights than regular channels. Apart from one exception (Ex2-8, peak mode), these failures also occurred with lower rise times. The common mode subtracted noise allowed no unique diagnostics statement.

The presence of six pinholes (plus two un-bonded pinholes) was an unexpected result. During the initial sensor tests at the QTCs only three of these faults (on the modules Ex2-2 and Ex2-5) were found and reported by the sensor test group in the production data base. Assuming that the sensor test procedure was able to observe all pinholes that were present at that time, the additional pinhole failures found with the ARC system were presumably created either during the module production or during the test procedures.

Module Ex1-7 of the express-line1 was used to check the impacts of different bond parameters on the number of pinholes found. As a result, the creation of a pinhole in fact depends on the selected parameters influencing the force with which a bond wire is pressed onto the bond pad. So, the oxide-layer below the pads may suffer a breakthrough. In order to exclude the possibility of producing pinholes during the light tests, where a large number of charge carriers are created in the surface region of the sensors, an extensive illumination of module Ex2-5 was performed. Pinhole tests were repeated periodically (using all intensity ranges) and pulsed light tests for a time period of more than five hours were done. The measurements revealed no creation of pinholes due to the external light illumination. Another conceivable reason for the generation of pinholes was found during the optical inspection. Deep scratches were observed on the surfaces of some sensors that were affected by pinhole faults. Presumably, careless handling of the detectors may also cause ohmic connections between the aluminium strips and the p^+ implants.

Throughout the express-line 2 measurements the pinhole test worked as designed and provided a reliable observation of pinhole faults. In combination with the fit results of the pulse shape test, even a unique determination of resistive and threshold pinholes was possible. A resistive pinhole had a significantly higher value of ΔPIN than a regular channel. Thereby it was conspicuous in the pulse shape test since it showed no signal response. On the contrary, a threshold pinhole was indicated by no failure in the pulse shape measurement but a higher value of ΔPIN than expected for a regular channel. Typically a temporary pinhole hardly gives any response to calibration pulses. Thus PIN^{max} is significantly lower (nearly zero) than for all other channels. This case was also observed during the tests (module Ex2-7). As mentioned in section 6.1.6 this failure signature is not unique, since a defect preamplifier input of an APV would reveal the same behaviour.

Fast test results and APV pipeline measurements are not included in the summary table, since both tests indicated no other flaws than those observed by the tests mentioned above. The breakdown limit of 450 V was matched by six of the nine modules. Again, the assessment of the breakdown performance was difficult due to the detector's sensitivity to environmental conditions. Thus one has to consider that the modules were not flushed with nitrogen.

As mentioned in the previous section, a group-wise common mode correction was implemented in ARCS which led to an improvement of the homogeneity of the noise distributions. In addition, special efforts were spent on a proper shielding and grounding scheme during the test procedures, but the problem of noisy APV edges could not be solved completely. Thus these edge channels were not taken into account, if they were not suspicious in another test than in the noise measurement.

As a result, six modules of the express-line 2 series passed the qualification criteria with the “grade A” whereas the three remaining detectors were graded with a “C”.

Defect Location		Defect Found												Grade	
Module	Strip	Mode	NOI	PSH	RT	LED	ΔPIN	PIN^{max}	Type of Defect	Breakdown					
Ex2-1	183	peak dec							×	○	○	○	(pinhole)	>500 V	A
	512	peak dec	×	×					×	○	○	○	(pinhole)		
Ex2-2	435	peak dec	×	n.s. n.s.	n.s. n.s.	×	○	○	×	○	○	○	(pinhole)	≈ 200 V	C
	423	peak dec		×	×	×	○	○		○	×	○	open		
Ex2-3	270	peak dec	×	×	×	×	○	○		○	×	○	(open)	>500 V	A
Ex2-4	—	peak/dec											none	>500 V	A
Ex2-5	3	peak dec	×	n.s. n.s.	n.s. n.s.	×	○	○	×	○	○	○	(pinhole)	>500 V	A
	65	peak dec	×	n.s. n.s.	n.s. n.s.	×	○	○	×	○	○	○	(pinhole)		
Ex2-6	—	peak/dec											none	≈ 300 V	C
Ex2-7	155	peak dec	×	n.s. n.s.	n.s. n.s.	×	○	○		×	○	○	(pinhole)	≈ 400 V	C
Ex2-8	495	peak dec	×	×	×	×	○	○		×	○	×	open	>500 V	A
Ex2-9	—	peak/dec											none	>500 V	A

Table 7.2: Summary table of the express-line2 test results. The nomenclature is as follows: < (>) value smaller (larger) than values of regular channels, × defect found in this type of test, ○ test not done, “n.s.” no signal, (type of defect) defect not found in optical inspection, and peak (dec) means the APV peak (deconvolution) mode.

Figure 7.9 confirms the homogeneous production of the express-line 2 modules. The four figures show the truncated mean values for common mode subtracted noise $\overline{NOI}_{trunc}$, pulse heights $\overline{PSH}_{trunc}$, pulse rise times $\overline{RT}_{trunc}$, and light responses $\overline{LED}_{trunc}$ for the modules Ex2-1 to Ex2-9.

Each module is characterized by four mean values (one per APV) in peak mode and in deconvolution mode, respectively. The data obtained are very consistent with each other. Compared to the results of the express-line 1 modules, the second pre-series production was even more homogeneous and faultless. The data fluctuation throughout the different measurements was less than 5% which was also caused by the better grounding and shielding conditions.

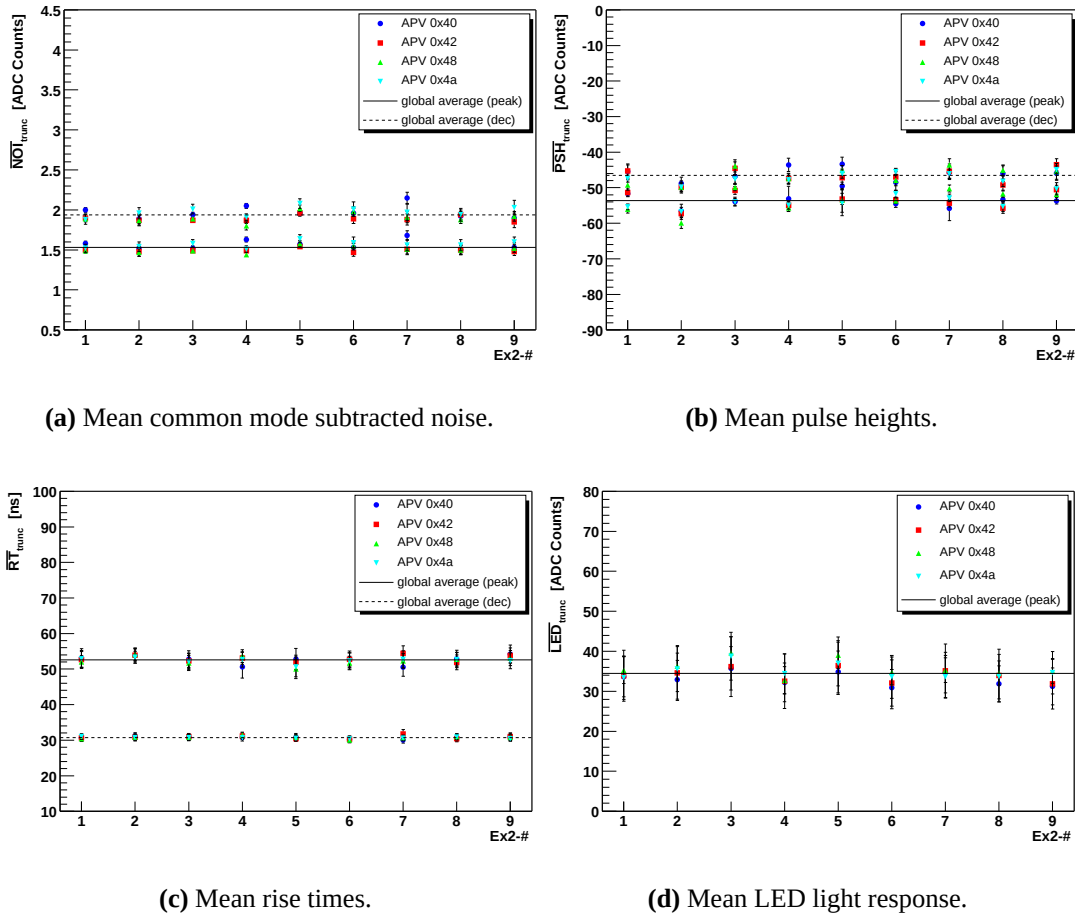


Figure 7.9: Characterization of the express-line2 modules. The errors indicate the corresponding standard deviations. The data are extracted from the results listed in the tables E.2 and E.3. The calculated *global average* values are indicated by solid lines in the case of peak mode operation and by dashed lines in the case of deconvolution mode operation.

7.2.4 Results of the Measurements with Temperature Cycling

The cooling test data were analysed from different points of view:

- What are the impacts of temperature on the mechanical stability of the modules?
- What are the effects of temperature on the performance of a module?
- Do different temperatures demand different test procedures to be implemented in ARCS?

In order to check the mechanical stability of the modules several temperature cycles between $T = +20\text{ }^{\circ}\text{C}$ and $T = -10\text{ }^{\circ}\text{C}$ were performed. By this means, mechanical stress was induced to the module's bond wires and sensors, respectively. The faults were determined before and after the cycling procedures and compared with each other finally. As a result, no additional failures occurred.¹⁴

Another important aspect was the examination of the behaviour of typical quality criteria measured at different temperatures.¹⁵ This included among other things the determination of pedestal, noise, and pulse shape properties. As discussed in [98], the impacts of the temperature on bare APV 25 chips are multi-faceted due to the large number of chip parameters affected by temperature, such as charge mobilities, transistor noise, resistances, and power consumptions. The study revealed that for a drop in temperature the current consumption increases, the data baseline increases, noise decreases, and pulse shapes, as well as calibration pulses change. Based on these results the express-line2 modules were also investigated for temperature effects which will be described in the following paragraphs.

Figures 7.10(a) to 7.10(d) show the pedestal distributions of module Ex2-6 at $+20\text{ }^{\circ}\text{C}$ (before cooling), $0\text{ }^{\circ}\text{C}$, $-10\text{ }^{\circ}\text{C}$, and $+20\text{ }^{\circ}\text{C}$ (after cooling) while operating the APV chips in peak mode with the inverter stage switched on. The mean pedestal values increased with decreasing temperature by about 5 ADC counts comparing the data measured at $+20\text{ }^{\circ}\text{C}$ and at $-10\text{ }^{\circ}\text{C}$. After the cooling cycle, the pedestal values recovered completely to the initial values.

Comparisons of pedestal data obtained from measurements done in peak and deconvolution mode (with the inverter switched on and off) are shown in figure 7.11. In deconvolution mode, the pedestal change was negligible which was also true for the impact of the inverter stage settings. The reason for the marginal influence of temperature in the case of deconvolution mode is related to the specific weights used for the deconvolution method (see section 6.1.1). Nevertheless, the pedestal results for modules approve those obtained from bare APVs.

The temperature dependence of the common mode subtracted noise is illustrated in the figures 7.12(a) to 7.12(d). While the noise values for peak mode decreased marginally in the case of low temperatures, the noise for deconvolution mode increased with a significance of approximately 0.2 ADC counts. Again, the influence of the inverter stage was negligible. The results for peak mode match the expected behaviour.

¹⁴Cooling cycles during which the modules are not read out are called *passive cooling tests*. This method can be used directly after the module assembly to check the quality of the bond wires.

¹⁵By this means, an *active cooling* test is done.

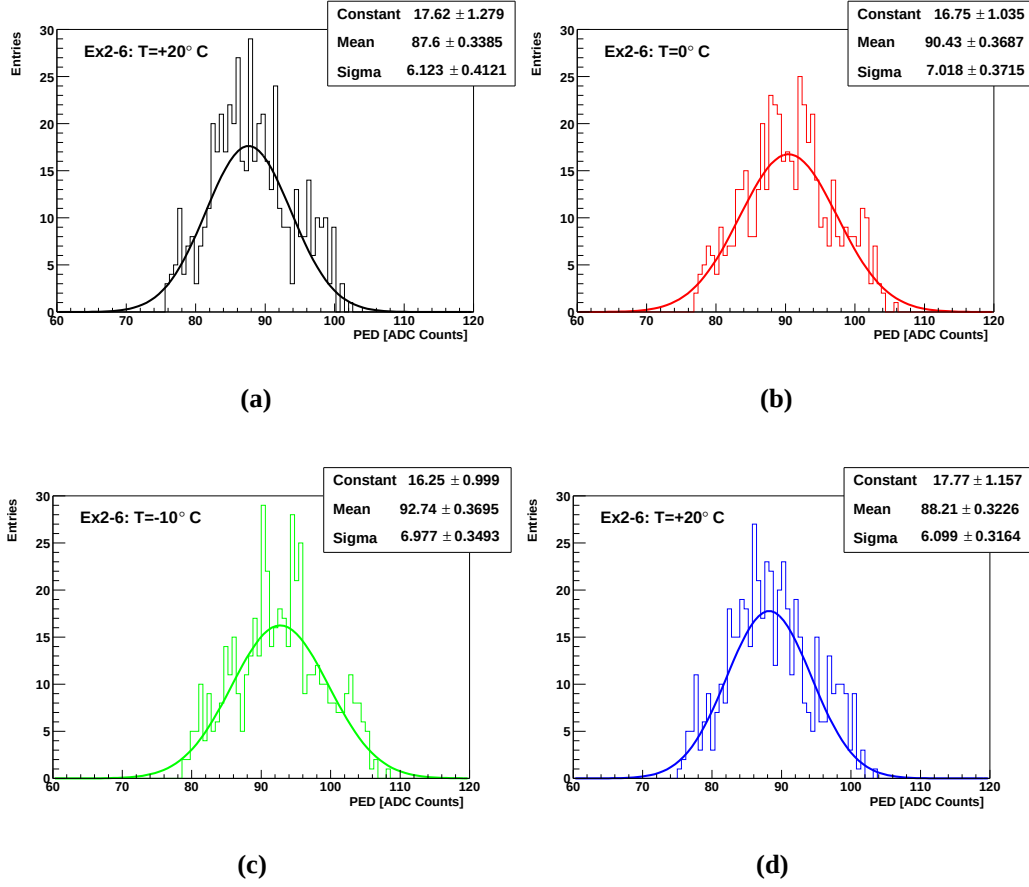


Figure 7.10: Pedestal distributions for different temperatures (512 channels of module Ex2-6, peak mode, inverter on). The module was operated at (a) $T = +20^\circ \text{C}$ (before cooling), (b) $T = 0^\circ \text{C}$, (c) $T = -10^\circ \text{C}$, and $T = +20^\circ \text{C}$ (after cooling).

In the case of a bare APV a drop in temperature means a decrease of noise. In addition, the leakage current is a typical noise source of a module but it decreases with decreasing temperatures (refer to equation 2.15 and section 4.3). On the contrary, the noise signatures for deconvolution mode are in opposition to the expectations. At present an explanation is not evident.

Figure 7.13(a) shows the temperature cycles used to determine the impacts of temperature on the calibration pulse shapes. Three temperatures were addressed (20°C , 0°C , and -10°C) during the eight hours of cooling box operation. The dashed lines indicate the time at which the pulse shape measurements were done (in peak mode, inverter on). At each point, seven different ICAL register settings ($\text{ICAL} = n \times 29$, with $n = 1, \dots, 7$) were adjusted in order to change the amount of charge injected into all input channels.

Figure 7.13(b) presents the temperature dependence of the mean pulse heights deduced from the analysis of 128 pulse shapes for different ICAL register settings (refer to the figures E.9(a) to E.9(f)). The figure illustrates that the absolute value $|PSH|$ increased significantly (by about 15%) when the temperature was decreased from $+20^\circ \text{C}$

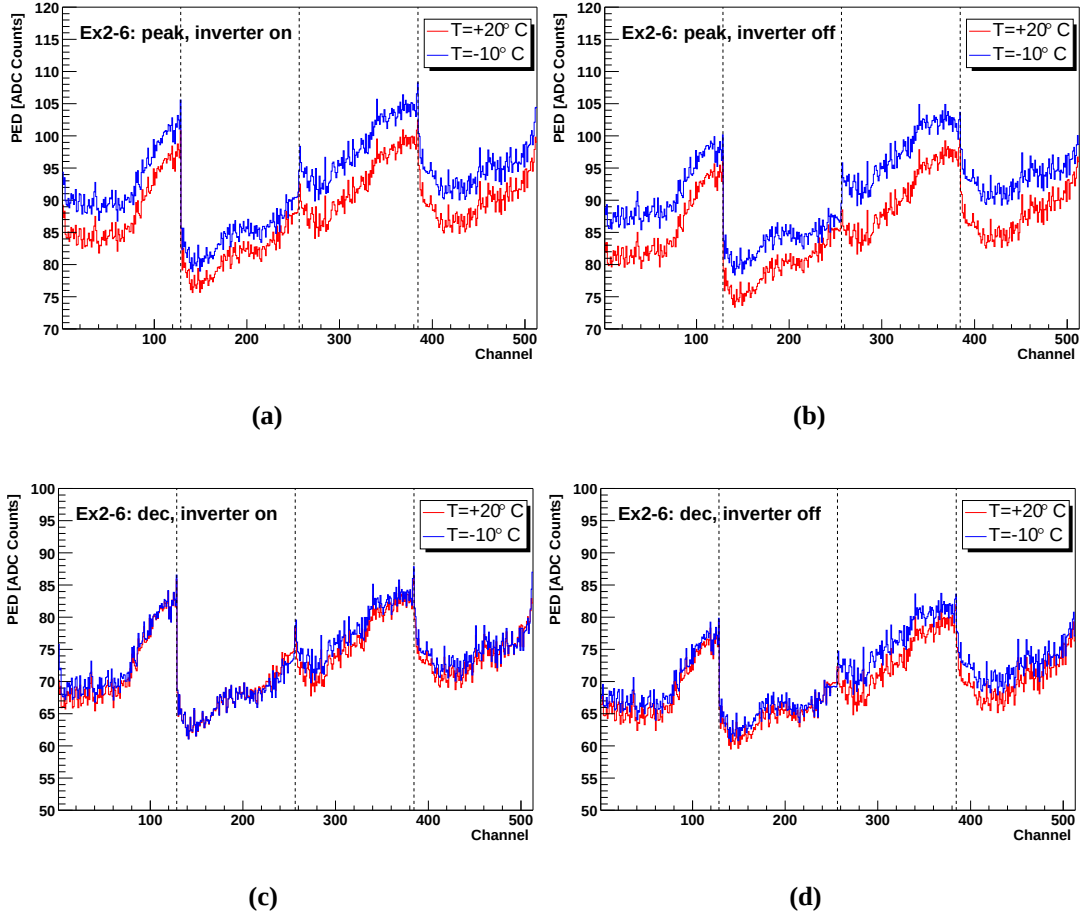


Figure 7.11: Pedestals at different temperatures and APV modes: (a) peak mode and inverter on, (b) peak mode and inverter off, (c) deconvolution mode and inverter on, and (d) deconvolution mode and inverter off.

down to -10°C .

To exemplify the development of the signal heights at three different temperatures, *PSH* values obtained from a single module channel are plotted in figure 7.13(c) as a function of ICAL register settings. For low ICAL values (< 160)¹⁶ the correlations were strictly linear for each temperature whereas the slopes of the line fits increased with decreasing temperature. Large ICAL values (> 160) led to the lost of linearity and resulted in a 10% deviation from the line fit at ICAL = 200. This is a known effect already reported in [99].

In addition to the pulse heights, the pulse rise times *RT* were extracted from the pulse shapes. Similar to *PSH*, the rise time of a pulse shape was also affected by the temperature. As depicted in figure 7.13(d), the rise times decreased with decreasing temperature (between 5% for low ICAL values and 10% for high values). Again, these results are presumably caused by the changing behaviour of some APV properties at low temperatures. Nevertheless, the modules and the APV chips kept operational

¹⁶ICAL = 160 corresponds to a charge created by about four MIPs.

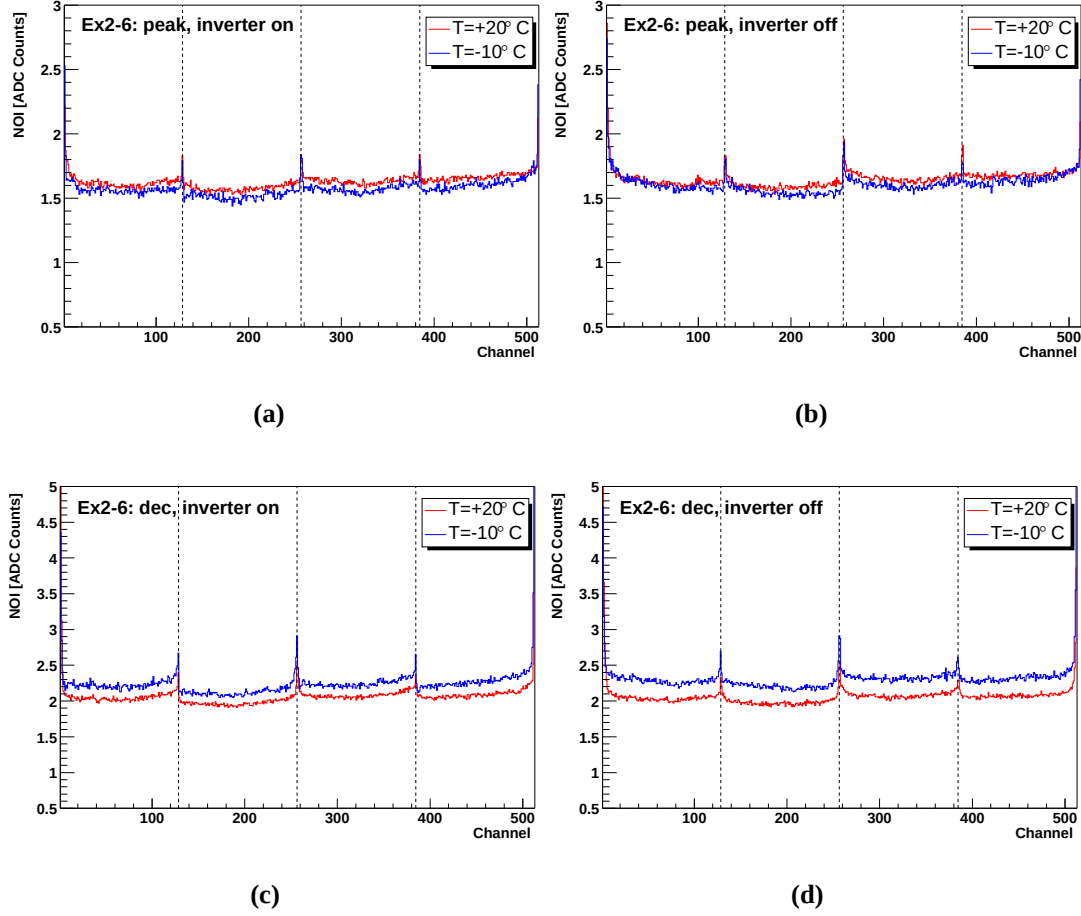


Figure 7.12: Common mode subtracted noise of module Ex2-6 at different temperatures and APV modes: (a) peak mode and inverter on, (b) peak mode and inverter off, (c) deconvolution mode and inverter on, and (d) deconvolution mode and inverter off.

at low temperatures. An appropriate adjustment of several APV command registers (ISHA and VFS for the pulse shape, ICAL for the calibration pulse, and VPSP for the data baseline) can be done to adapt the quantities measured at different temperatures.

The increase of signal heights at low temperatures could also be observed for external signals, such as LED light pulses. Due to the 1 m long optical fibres used (see section 5.1.5), the LEDs themselves could be placed outside the cooling box during the cycling procedures. Thus the diodes were not affected by the different temperatures and did not contribute to the change in the signal heights. By this means, the measurements at different temperatures were comparable with each other. The results for $T_1 = +20^\circ\text{C}$ and $T_2 = -10^\circ\text{C}$ are shown in figure 7.14(a). The differences in the light response $\Delta LED_i = LED_i(T_2) - LED_i(T_1)$ for every channel i are presented in figure 7.14(b). The mean difference was about 9 ADC counts. This result illustrates the increase of the charge collection efficiency of a cooled silicon detector with decreasing temperature.

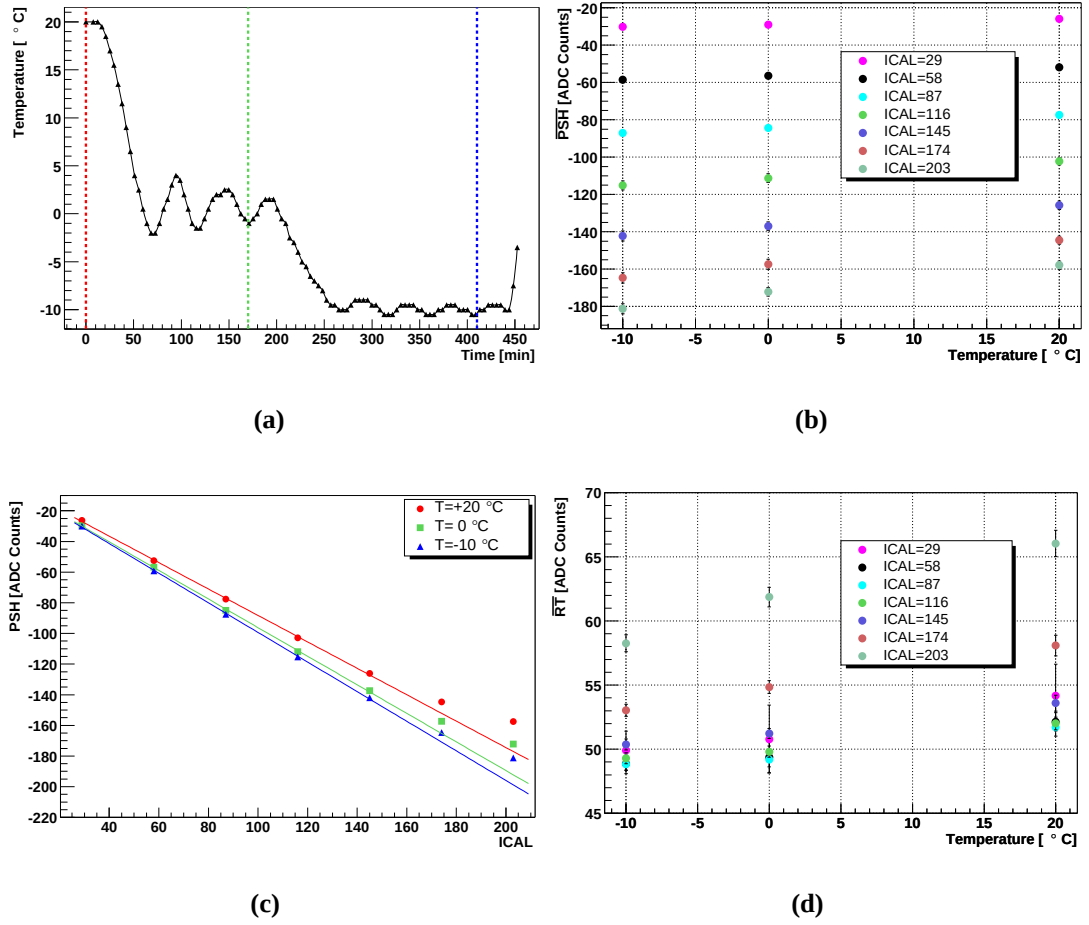


Figure 7.13: Impacts of temperature on the calibration pulse shapes. (a) Temperature cycle for about eight hours. The dashed lines indicate the time (and temperature) at which the presented data were taken. (b) Mean pulse shape heights for three temperatures and different ICAL settings. (c) Calibration pulse heights versus ICAL. (d) Mean pulse shape rise times. The data are extracted from the measurements shown in figures E.9(a) to E.9(f).

Since the long-term test of the assembled modules will presumably be composed of measurements at ambient temperature and at about -10°C , the failure signatures of open bonds, shorts, and pinholes at both temperatures were of great interest with respect to an automated quality control.

The behaviour of the two pinholes found at module Ex2-5 as well as one regular channel in dependence of the temperature are depicted in figure 7.15(a). As described above, the calibration signal heights increased with decreasing temperature which became also obvious in the pinhole test where the height difference was about 20 ADC counts. The pinhole signatures differed from each other at different temperatures. In the case of $T = -10^{\circ}\text{C}$ the heights of the calibration pulse shapes decreased much faster with increasing light intensity after reaching the signal maximum. However, this behaviour had no effect on the pinhole signature used to assess the individual channels

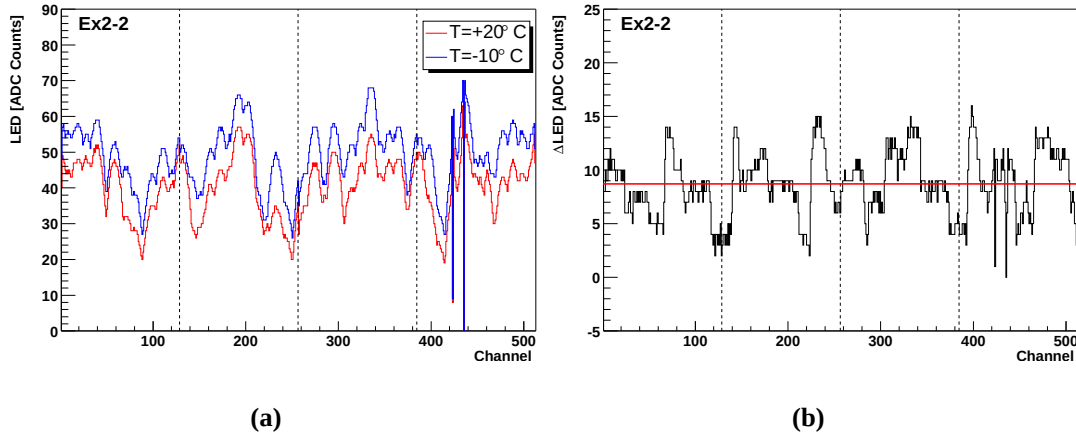


Figure 7.14: (a) Responses to pulsed LED light at $T = +20^\circ \text{C}$ and $T = -10^\circ \text{C}$. (b) Response differences between both measurements. The solid (red) line indicates the mean value.

as illustrated in figure 7.15(b). ΔPIN relies only on the maximal and minimal pulse heights which makes the pinhole test robust against temperature changes.

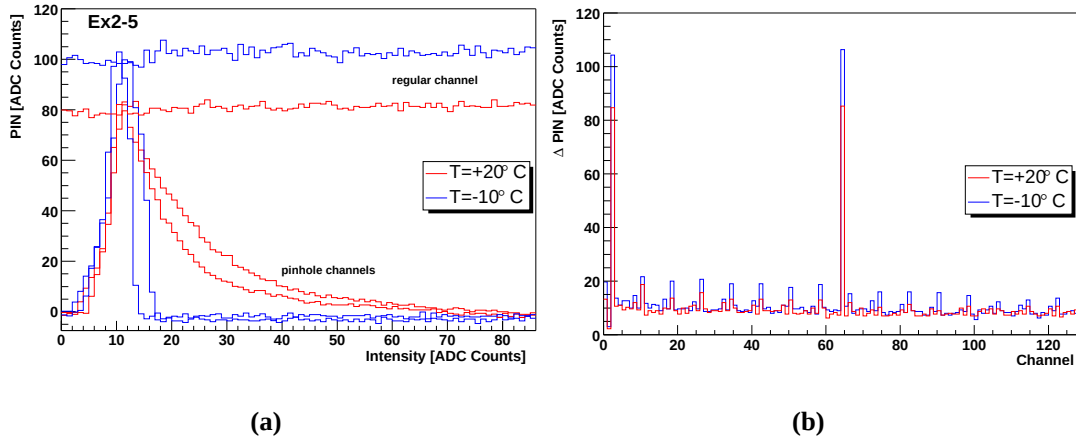


Figure 7.15: (a) Signatures of resistive pinholes at $T = +20^\circ \text{C}$ and $T = -10^\circ \text{C}$ obtained with the continuous light test. For comparison, the behaviour of a regular channel is also superimposed. (b) ΔPIN versus APV channel.

Open bonds and shorts could be characterized by the same signatures as described in the previous paragraphs. Thus the test procedures developed were suitable to observe faults at different temperatures with the same efficiency.

As discussed in section 2.2.1, the leakage current I_{leak} of a module depends on the temperature T and on the bias voltage V_{bias} . Figure 7.16 presents the measurement of I_{leak} as a function of T applying $V_{bias} = 200 \text{ V}$ to the module [96]. The errors are given

by the resolutions of the current monitor (0.01 μA) and the temperature measurement¹⁷ (1 $^{\circ}\text{C}$). Based on equation 2.16 the following fit function was used to describe the data sample:

$$f_{I_{leak}} = C \cdot (T + 273)^2 \cdot \exp\left(\frac{-E_G}{2 k_B (T + 273)}\right), \quad (7.3)$$

where C is a constant and $k_B = 8.617 \times 10^{-5} \text{ eV/K}$ is the Boltzmann constant. The unit of the temperature had to be translated from $^{\circ}\text{C}$ into K . The fit is of good quality and reveals the fit parameter E_G to be $0.98 \pm 0.06 \text{ eV}$. Compared to the expected band gap energy of a non-irradiated silicon sensor (which is 1.1 eV), the extracted result is consistent with the expectation.

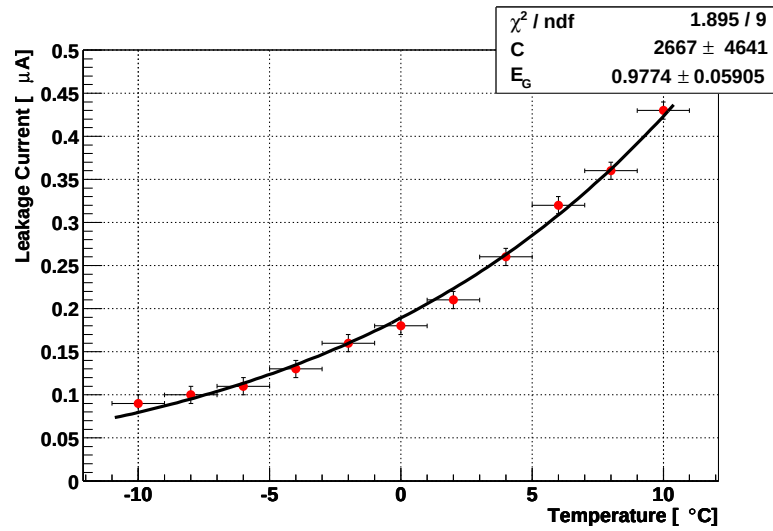


Figure 7.16: Impact of the temperature on the leakage current.

The cooling tests confirmed the functionality of the express-line2 modules at different temperatures. It could be demonstrated that the ARC system, the ARC software, as well as the test environment (e.g. the cooling box) developed and built-up at Aachen are suited to cope with the large-scale production of FE hybrids and modules.

¹⁷Due to safety reasons the Dallas sensor used was not mounted directly to the silicon surface but to the module's carrier plate.

Chapter 8

Conclusions and Future Plans

This thesis deals with the quality assurance of front end hybrids and silicon microstrip detector modules envisaged for the CMS inner tracking device. Since the tracker will be equipped with approximately 15,000 modules, a compact and inexpensive diagnostic system is needed to monitor the mass production in industry and in the various CMS tracker production centres.

To meet these requirements, a test setup called ARC system was developed and distributed among all collaborating institutes to perform full quality tests of front end hybrids and modules at each production step.

The ARC system is controlled via a C++ based readout software using LabVIEW as graphical user interface. This software package is called ARCS, and is suited to assess the functionality of hybrids and modules in a comfortable way. The various test procedures incorporated in ARCS are the results of more than three years of experience gained with various types of hybrids and modules analysed with the ARC system.

In particular, a pre-series of 21 TEC wedge-ring-6 modules built in 2002 was used to improve and establish the individual ARC software routines. This module production was divided into two batches called express-line 1 and 2. All modules of the express-lines were tested with the ARC system at ambient temperature in a clean room environment. The second pre-series could also be assessed at low temperatures (-10°C) using a specific cooling box for modules built in Aachen.

Three types of faults showed up during the different test procedures implemented in ARCS: open bonds, shorts, and pinholes. In total only 29 channels (of 21×512 channels) were identified as faulty channels affected by one of the failures mentioned above. This leads to a failure rate of less than 0.3% which stresses the good quality of the components used and the accurate bonding quality. From the ARCS point of view, the test procedures developed could be proven to be very stable throughout the measurements, thus representing a powerful tool to find and to diagnose failures based on the correlated results of different tests. Especially the reproducibility and the comparability of the test results are encouraging with respect to the enormous challenge of the large-scale production the CMS experiment is facing.

In this thesis, the physics of silicon sensors was investigated under different conditions using the ARC setup. All measurements were in agreement with the expectations, thus stressing the functionality of the test system.

Moreover, the suitability and reliability of the individual test procedures incorporated in the ARCS environment with respect to the quality assurance of hybrids and silicon modules was demonstrated. These tests have to be integrated into automated test programs needed at different test centres in the near future. Recently, big efforts are spent on the final definition of the test programs, cut strategies, and thresholds to be used during the large-scale production.

A properly designed and calibrated diagnostic system is an essential condition to guarantee a reliable and homogeneous front end hybrid and module production. The ARC system is suited to accomplish these requirements.

Appendix A

Physics

A.1 Feynman Diagrams of Standard Model Higgs Production Channels

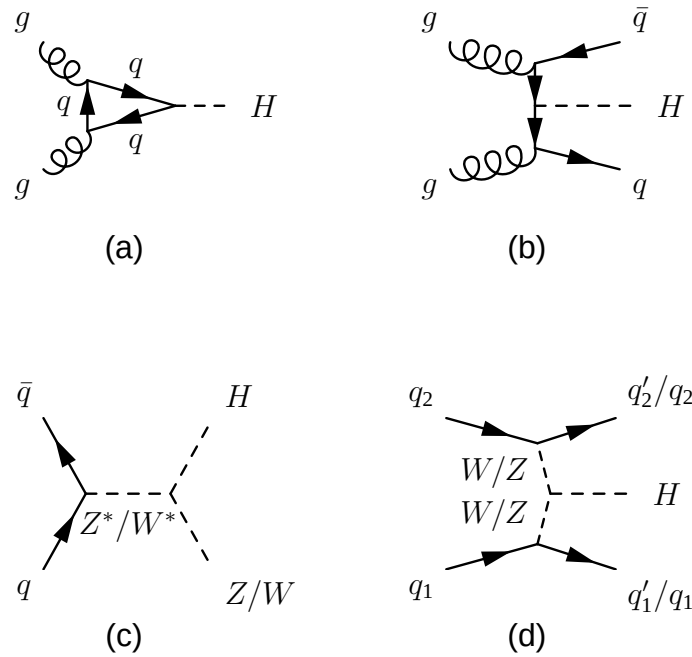


Figure A.1: Feynman diagrams of different production channels of the SM Higgs boson at LHC: (a) gluon-gluon fusion, (b) associated production with a $q\bar{q}$ pair, (c) associated production with W/Z boson (Higgs-Strahlung) and (d) vector boson (WW/ZZ) fusion.

A.2 Feynman Diagrams of Standard Model Higgs Decays

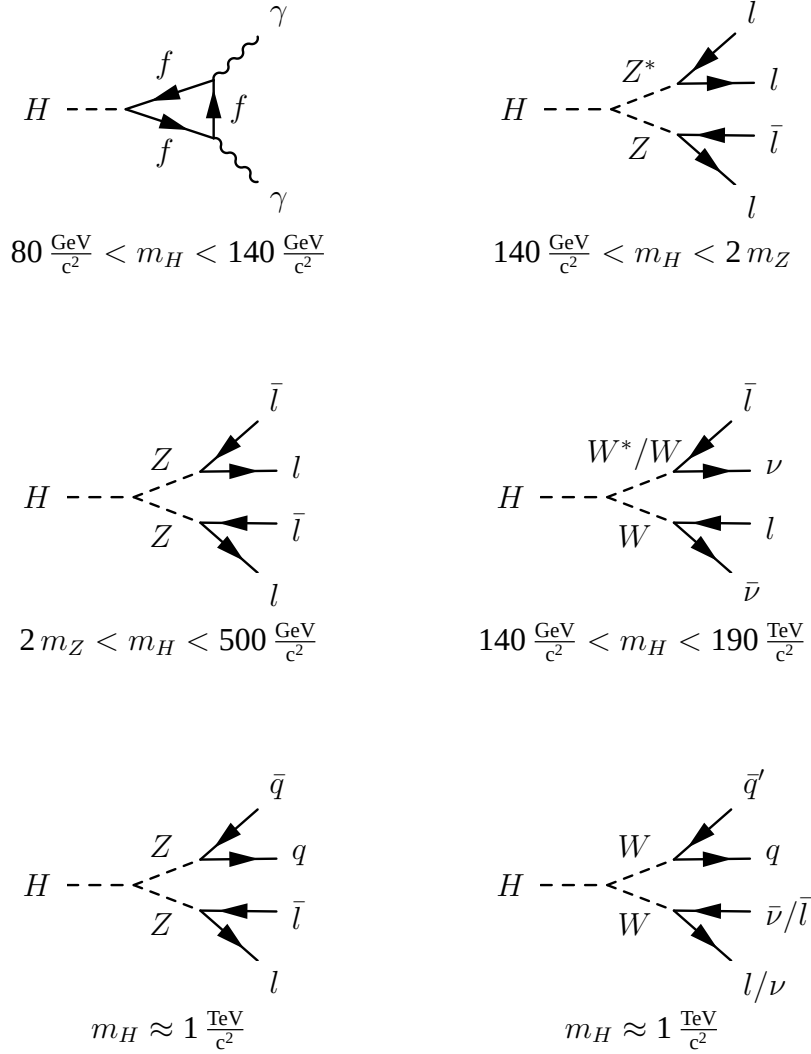


Figure A.2: Decay modes of the SM Higgs boson showing the highest sensitivity in the experimental search for different mass ranges. The indicated leptons l are either electrons or muons.

Appendix B

Silicon Specifics

B.1 Processing Sequence in Planar Technology

The planar process for detector fabrication introduced by J. Kemmer [29] includes generally the following steps:

- 1) the starting point: polished and doped bulk material (e.g. n-type silicon),
- 2) deposition of insulating layers (SiO_2 , Si_3N_4) produced by chemical reaction between gases surrounding the semiconductor surface (oxidation),
- 3) photolithographic structuring,
- 4) chemical oxide etching,
- 5) doping either by diffusion or by implantation,
- 6) oxidation, deposition and structuring of metal (e.g. aluminium) by evaporation or sputtering, afterwards thermal treatments, and passivation.

Figure B.1 illustrates the different steps needed to produce a microstrip silicon sensor via the planar technology.

B.2 The Depletion Zone of the pn-Junction

If the charge density distribution $\rho(x)$ (in a one-dimensional approximation) in the depletion zone is known, the depth of the zone can be calculated via *Poisson's equation*:

$$\frac{d^2V}{dx^2} = -\frac{\rho(x)}{\epsilon}, \quad (B.1)$$

where V is the electrical potential and ϵ the dielectric constant of silicon. In case of a pn-junction with the donor and acceptor impurity densities N_D and N_A , a uniform charge distribution can be assumed. If x_p denotes the extent of the depletion zone on the n-side and x_n the depth on the p-side, one can use equation B.2. where q is the

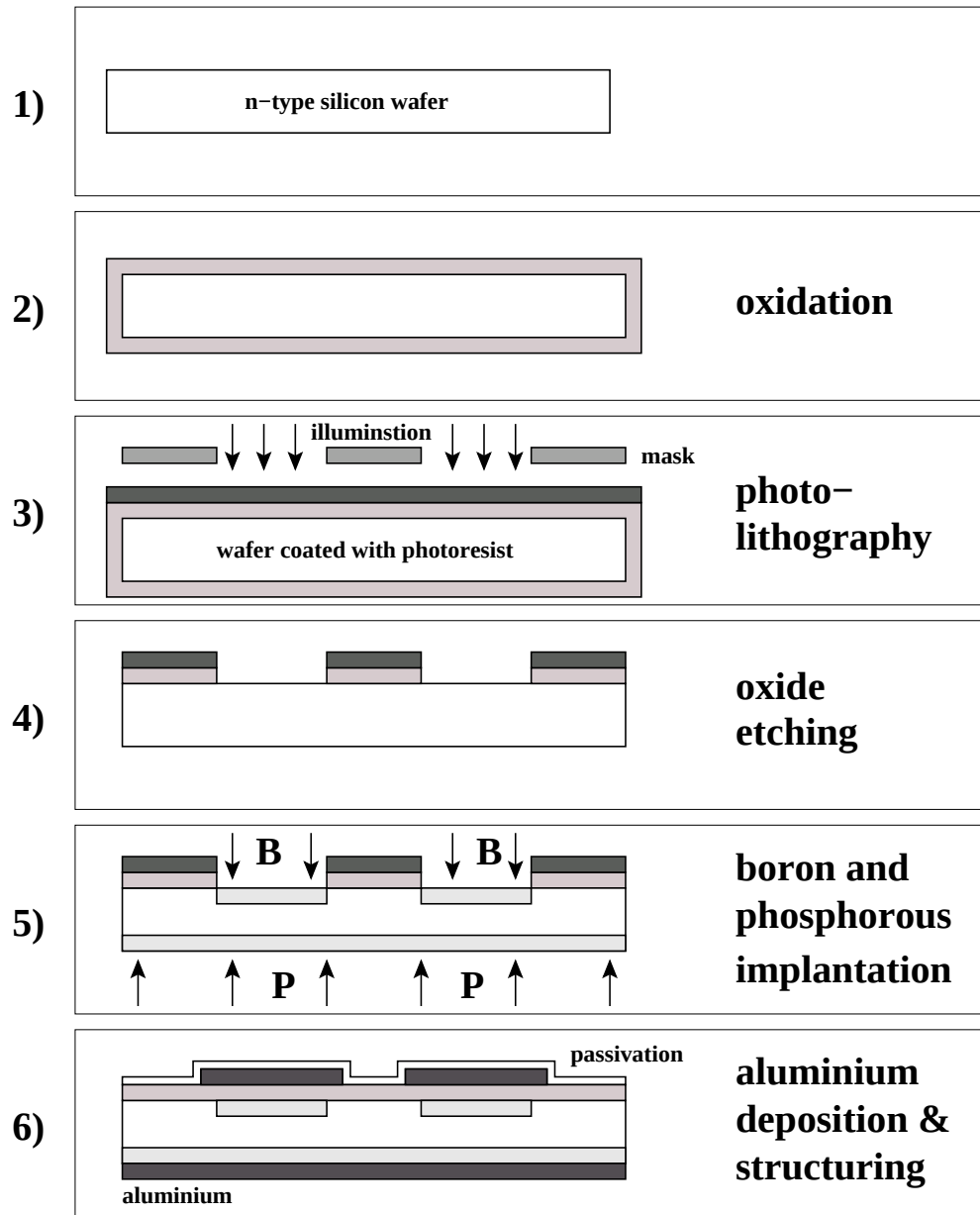
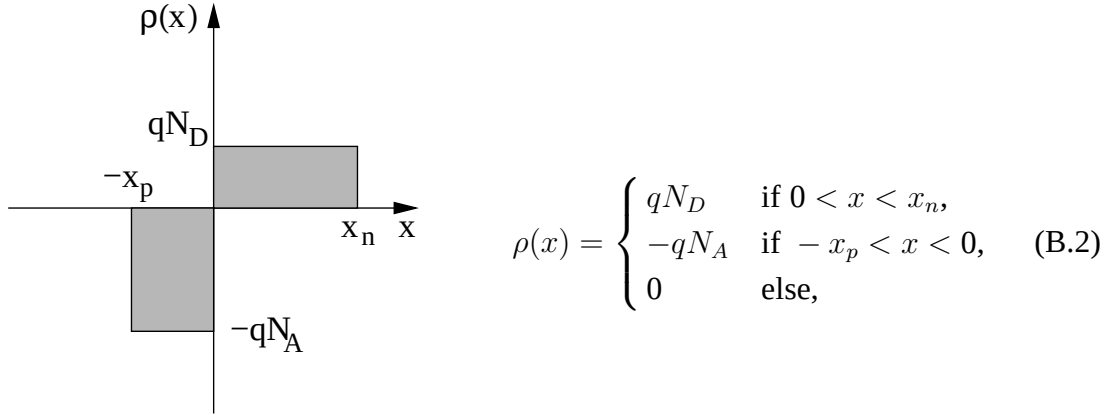


Figure B.1: Simple schematics of the planar technology.



charge of the electron. Since the total charge is conserved, the following equation is valid:

$$N_A \cdot x_p = N_D \cdot x_n. \quad (\text{B.3})$$

Using the conditions $dV/dx = 0$ at $x = x_n$ and $x = -x_p$, as well as $V(x) = V_{bi}$ at $x = x_n$ and $V(x) = 0$ at $x = -x_p$, respectively, a twofold integration of the Poisson equation delivers:

$$V(x) = \begin{cases} -\frac{qN_D}{\epsilon}(x_n - x)^2 + V_{bi} & \text{if } 0 < x < x_n, \\ +\frac{qN_A}{\epsilon}(x_p + x)^2 & \text{if } -x_p < x < 0, \end{cases} \quad (\text{B.4})$$

with V_{bi} being the so-called *built-in voltage* which is parameterized in equation B.5. It describes the height of the potential barrier without applying an external voltage (see figure B.2). V_{bi} voltage is usually of the order of a few hundred millivolts at ambient temperature.

$$V_{bi} = \frac{q}{2\epsilon}(N_D \cdot x_n^2 + N_A \cdot x_p^2). \quad (\text{B.5})$$

The combination of equations B.5 and B.3 results in the *depletion width* w :

$$w = x_n + x_p, \quad (\text{B.6})$$

with

$$x_n = \sqrt{\frac{2\epsilon V_{bi}}{qN_D(1 + N_D/N_A)}}, \quad x_p = \sqrt{\frac{2\epsilon V_{bi}}{qN_A(1 + N_A/N_D)}}. \quad (\text{B.7})$$

Both equations B.7 illustrate that the depletion zone extends into both regions in reverse proportions to the acceptor and donor densities. In particular in materials where one type of impurity atoms is dominant, e.g. $N_D \gg N_A$, which is the case for the silicon strip detectors used at CMS, then $x_n \gg x_p$. Thus the depletion region is almost entirely on the n-side of the junction. In this approximation ($x_p \rightarrow 0$) the width w is given by:

$$w \approx x_n \approx \sqrt{\frac{2\epsilon V_{bi}}{qN_D}}. \quad (\text{B.8})$$

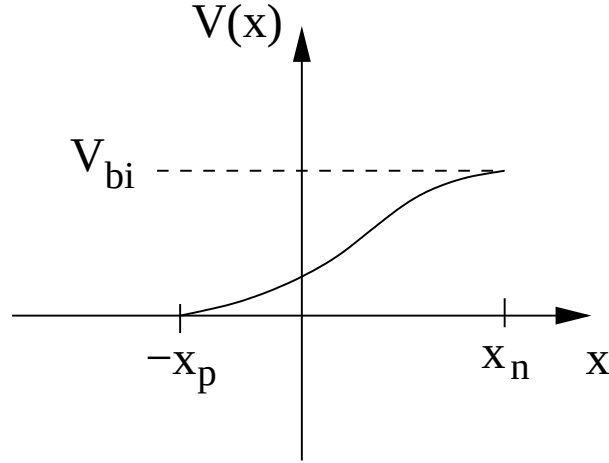


Figure B.2: Potential barrier V_{bi} .

Using equation 2.3 the resistivity ρ and the electron mobility μ_e can be included into equation B.8:

$$w \approx \sqrt{2 \epsilon \rho \mu_e V_{bi}}. \quad (\text{B.9})$$

For particle detector devices based on a pn-junction, an external voltage V_{bias} of the same sign as the built-in voltage is applied in order to increase the depletion region. In this case V_{bi} has to be replaced by $V_B = V_{bias} + V_{bi}$ in the equations B.8 and B.9:

$$w \approx \sqrt{\frac{2 \epsilon (V_{bias} + V_{bi})}{q N_D}}. \quad (\text{B.10})$$

In order to deplete a silicon sensor of thickness w_{max} completely, a bias voltage of $V_{bias} = V_{depl}$ is needed. V_{depl} is called *depletion voltage* and can be calculated by using equation B.10:

$$V_{depl} = \frac{q N_D w_{max}^2}{2 \epsilon} - V_{bi}. \quad (\text{B.11})$$

B.3 Microscopic Sensor Pictures of a TEC Wedge-Ring-6-Sensor

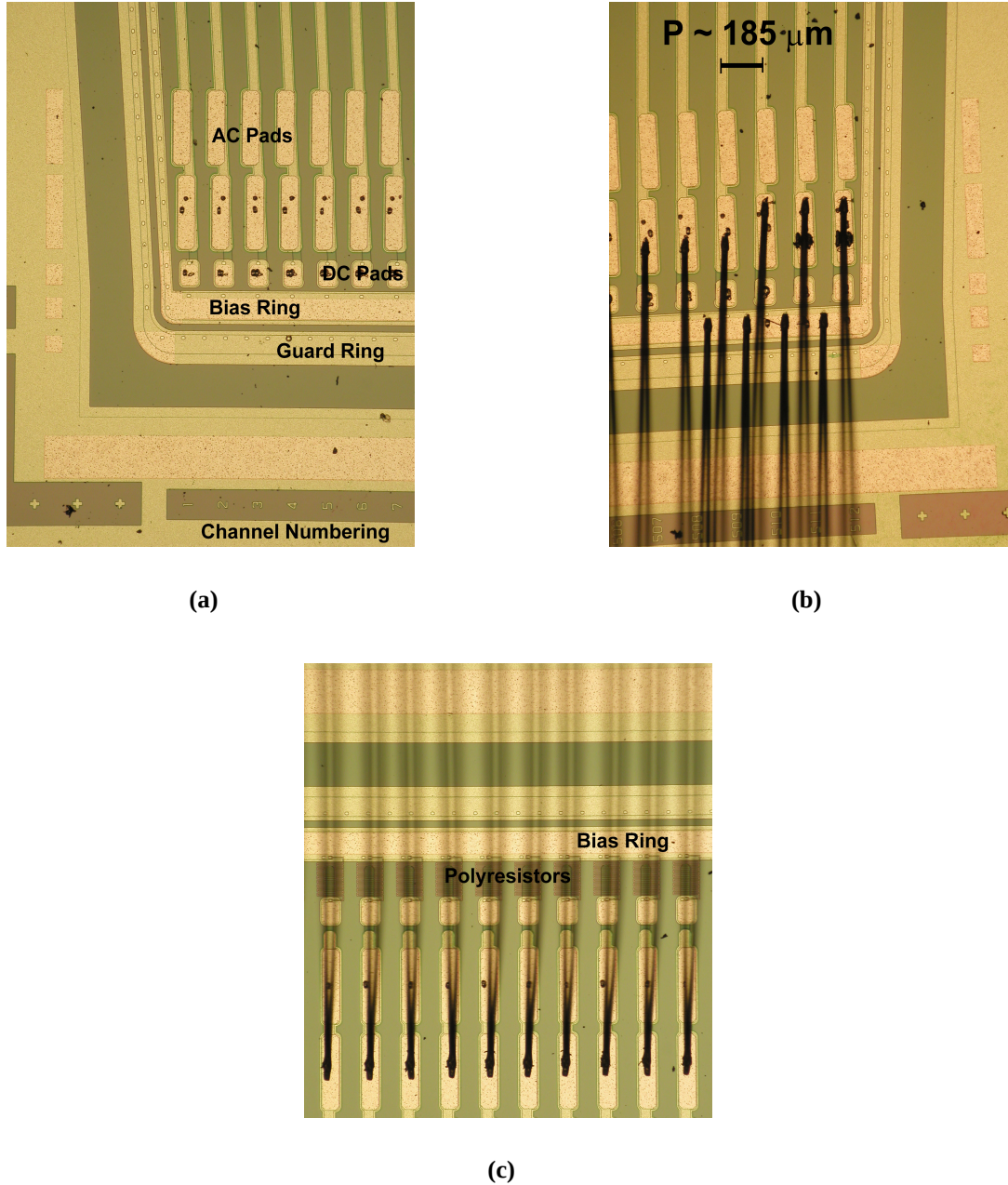


Figure B.3: Microscopic TEC sensor pictures. (a) Left edge of sensor W6B (small side). Guard ring, bias ring, AC pads and DC pads, and the strip numbering are labeled. (b) Right edge of sensor W6B (small side). The AC pads 506 to 512 are connected to the corresponding sensor W6A via bond wires. Four bond wires are used to ground the bias ring. (c) Edge of sensor W6B (readout side) with polyresistors connected to the bias ring.

B.4 Sketches of TEC Wedge-Ring-6 Sensors A and B

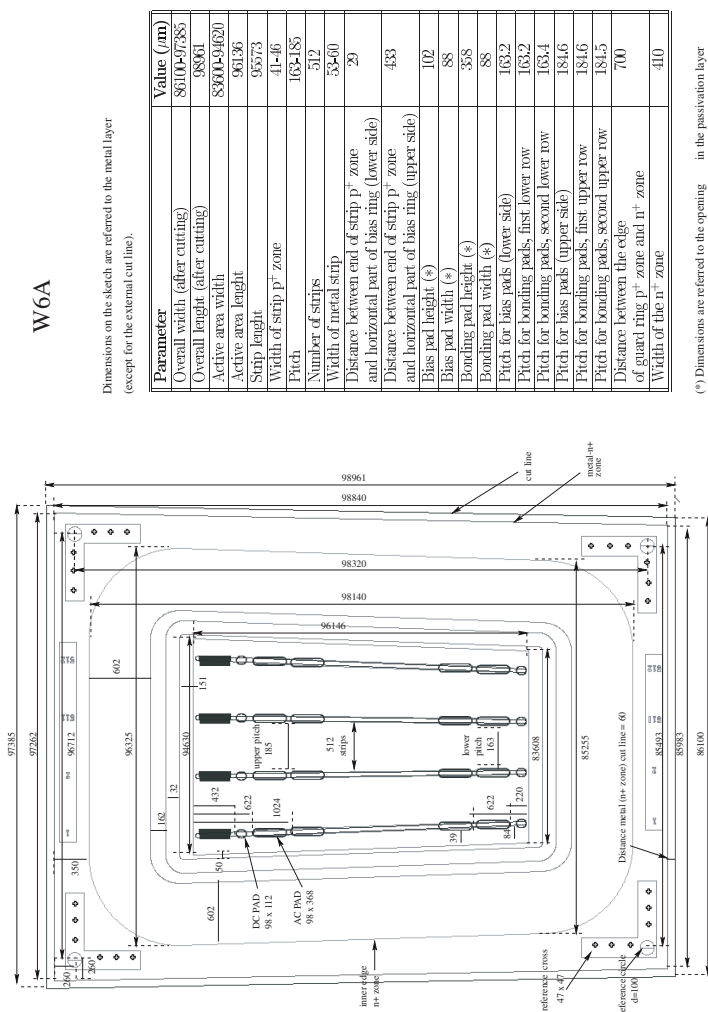


Figure B.4: Sketch of a TEC wedge-ring-6-sensor A.

Source: [100]

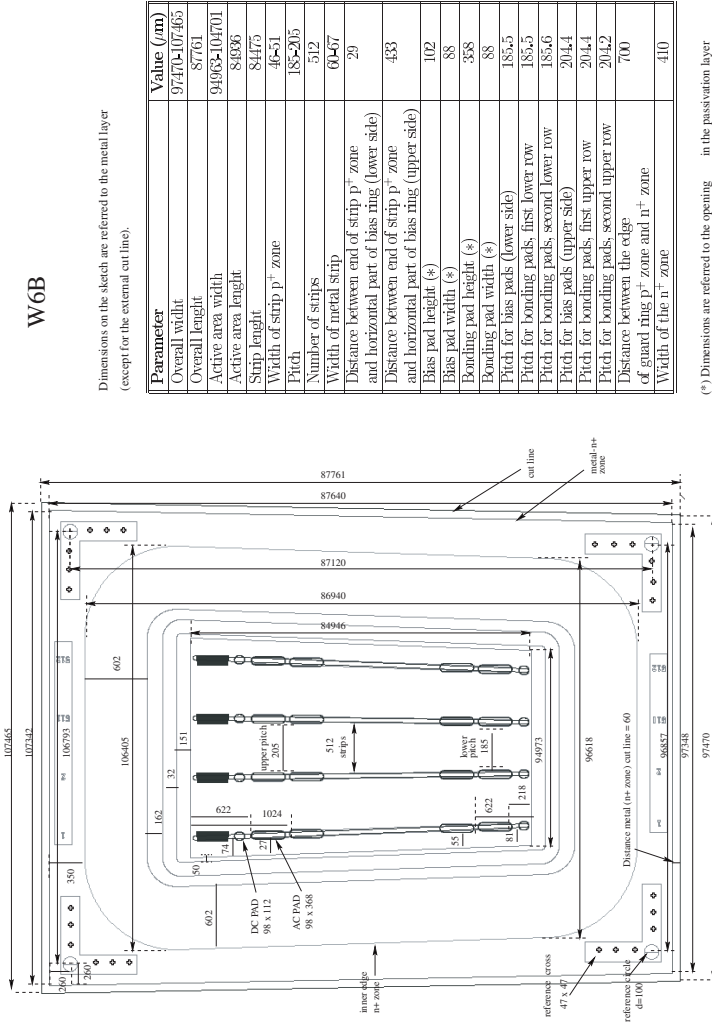


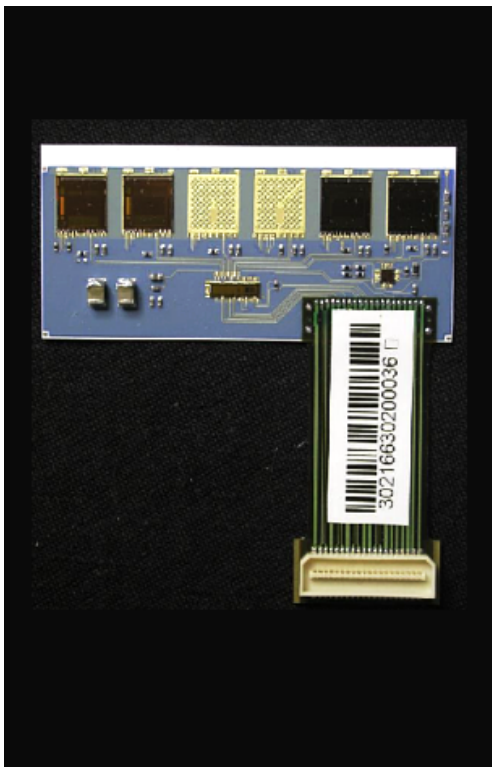
Figure B.5: Sketch of a TEC wedge-ring-6-sensor B.

Source: [100]

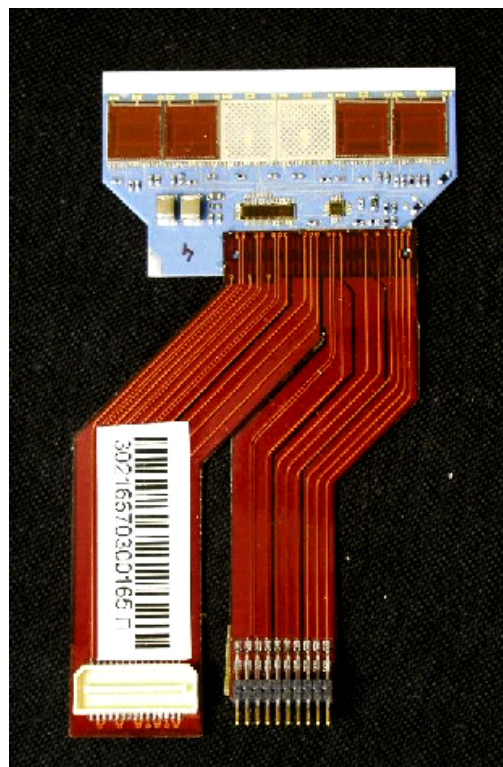
Appendix C

Hybrid Specifics

C.1 Different Types of Front End Hybrids

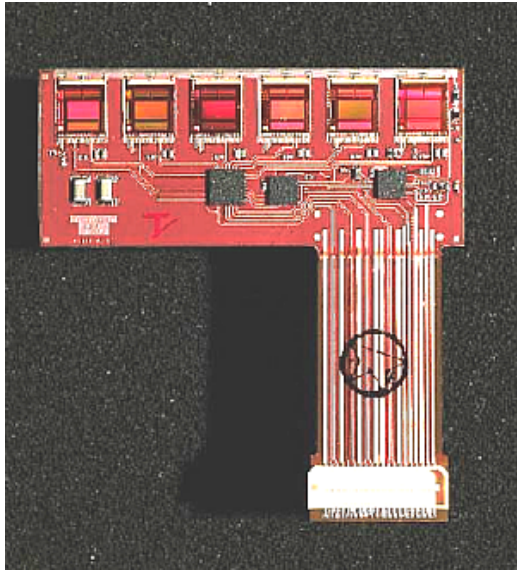


(a) Ceramic TEC FE hybrid.

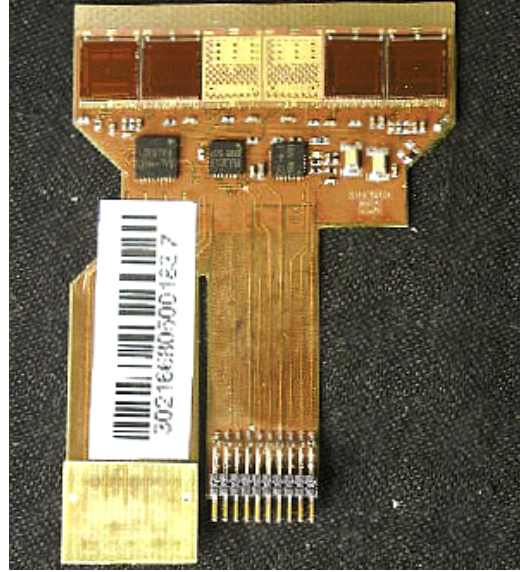


(b) Ceramic TIB FE hybrid.

Figure C.1: Ceramic FE hybrids equipped with four APVs and merged TPLL/APVMUX chips produced by Dorazil. [50]



(a) Flex-rigid polyimide-FR4 TEC FE hybrid.



(b) Flex-rigid polyimide-FR4 TIB FE hybrid.

Figure C.2: Flex-rigid polyimide-FR4 FE hybrids fabricated by Cibel [101]. Both hybrids carry packaged TPLL, APVMUX, and DCU chips.

C.2 I²C Bus Specifications

This section summarizes the most essential aspects of the I²C bus. A more detailed description can be found in [54].

The I²C bus requires only two lines for inter circuit communication which are called *serial data line (SDA)* and *serial clock line (SCL)*. Each device being connected is recognized by a unique 7-bit address and can operate either as a *transmitter* or *receiver* depending on the function of this device. Moreover, a device can be considered as a *master* or *slave* when performing a data transfer. A master is the device which initiates a data transfer on the bus and generates the clock signal to permit the transfer. At that time any other device addressed is considered as a slave.

Figure C.3 depicts the connection of standard I²C devices to the bus. SDA and SCL are connected to a positive power supply voltage via a pull-up resistors. When the bus is free both lines are at logic “1” (*HIGH* level). A logic “0” is defined as *LOW* level.

The data transfer rates are as follows:

- 100 kbit/s in standard-mode,
- 400 kbit/s in fast-mode,
- 3.4 Mbit/s in high-speed-mode.

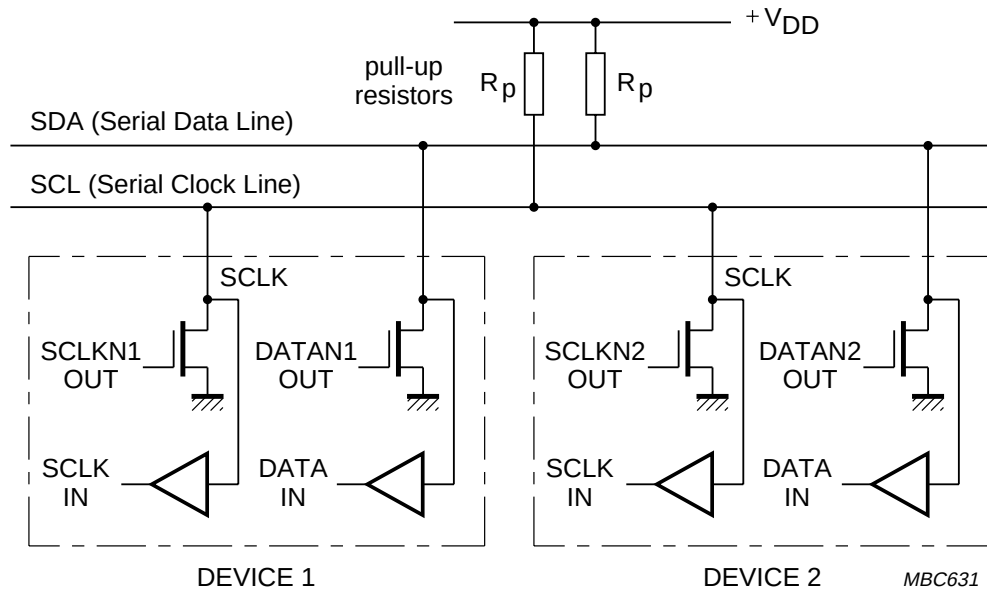


Figure C.3: Connection of standard- and fast-mode devices to the I²C bus. Source: [54]

During a HIGH period of the SCL, the data on the SDA must be stable. The HIGH and LOW state of the data line can only change when the clock signal on the clock line is LOW. Both cases are illustrated in figure C.4.

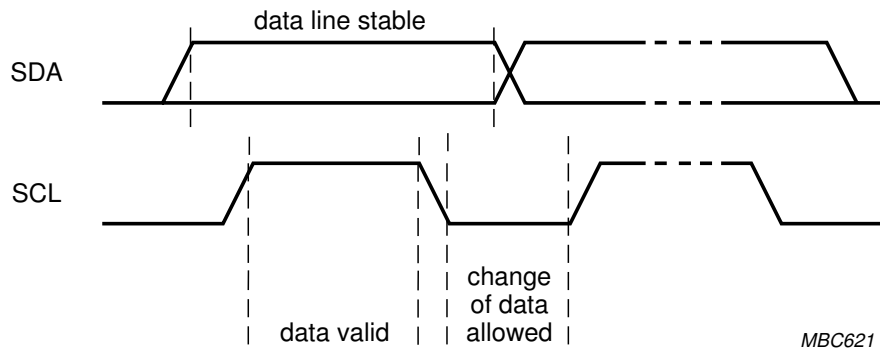


Figure C.4: Bit transfer on the I²C bus. Source: [54]

Complete data transfers follow the format shown in figure C.5. After a START condition (S), the unique 7-bit slave address is sent which is followed by an eighth bit defining the direction of the data transfer (R/W). A “0” indicates a transmission or WRITE access whereas a “1” signals a READ request. The data transfer (DATA) is always terminated by a STOP condition (P) generated by the master. Usually a receiver which has been addressed is obliged to generate an acknowledge (ACK) after each byte has been received.

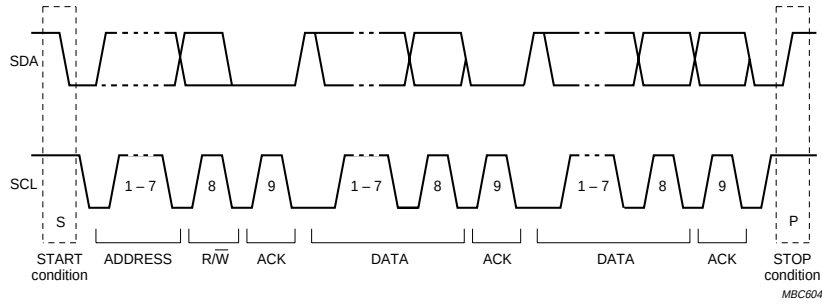


Figure C.5: A complete I²C data transfer.

Source: [54]

C.3 Gray Code

The digital part of an APV frame is composed of a 3-bit header, an 8-bit column address, and one error bit. The column address is encoded in the so-called gray code. Figure C.6 gives an example of how to interpret the column address of an APV frame in terms of digital “0” (LOW level) and digital “1” (HIGH level). In the present case the code number is “10101001”. This code can be translated into the column number 174 when using the gray code table presented in figure C.7.

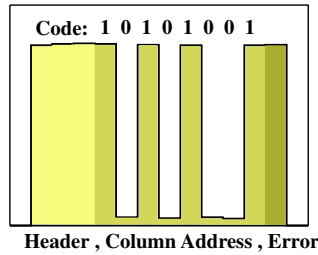


Figure C.6: Interpretation of a column address.

C.4 The Deconvolution Method of Pulse Shaping

The so-called *deconvolution method* [102] offers a way to use either fast or slow shaping depending on operation conditions. Because of the high interaction rate at the LHC the optimal time constant τ cannot be used. Fast shaping is essential to reduce signal pile-up but it worsens noise from a CMOS amplifier simultaneously. On the contrary, slow shaping leads to higher shot noise after detector radiation damage.

In a linear amplifying system the relation between the signal output $v(t)$, the initial signal $s(t)$ and the impulse response $h(t)$ is described by the convolution integral given in equation C.1.

$$v(t) = \int_{-\infty}^t h(t-t')s(t')dt'. \quad (\text{C.1})$$

APV25-S0 Pipeline Column Address Codes

COL	POS	CODE	COL	POS	CODE	COL	POS	CODE
0	0	00110000	64	128	01010000	128	127	11110000
1	2	00110001	65	130	01010001	129	125	11110001
2	4	00110011	66	132	01010011	130	123	11110011
3	6	00110010	67	134	01010010	131	121	11110010
4	8	00110110	68	136	01010110	132	119	11110110
5	10	00110111	69	138	01010111	133	117	11110111
6	12	00110101	70	140	01010101	134	115	11110101
7	14	00110100	71	142	01010100	135	113	11110100
8	16	00111100	72	144	01011100	136	111	11111100
9	18	00111101	73	146	01011101	137	109	11111101
10	20	00111111	74	148	01011111	138	107	11111111
11	22	00111110	75	150	01011110	139	105	11111110
12	24	00111010	76	152	01011010	140	103	11111010
13	26	00111011	77	154	01011011	141	101	11111011
14	28	00111001	78	156	01011001	142	99	11111001
15	30	00111000	79	158	01011000	143	97	11111000
16	32	00101000	80	160	01001000	144	95	11101000
17	34	00101001	81	162	01001001	145	93	11101001
18	36	00101011	82	164	01001011	146	91	11101011
19	38	00101010	83	166	01001010	147	89	11101010
20	40	00101110	84	168	01001110	148	87	11101110
21	42	00101111	85	170	01001111	149	85	11101111
22	44	00101101	86	172	01001101	150	83	11101101
23	46	00101100	87	174	01001100	151	81	11101100
24	48	00100100	88	176	01000100	152	79	11100100
25	50	00100101	89	178	01000101	153	77	11100101
26	52	00100111	90	180	01000111	154	75	11100111
27	54	00100110	91	182	01000110	155	73	11100110
28	56	00100010	92	184	01000010	156	71	11100010
29	58	00100011	93	186	01000011	157	69	11100011
30	60	00100001	94	188	01000001	158	67	11100001
31	62	00100000	95	190	01000000	159	65	11100000
32	64	01100000	96	191	11000000	160	63	10100000
33	66	01100001	97	189	11000001	161	61	10100001
34	68	01100011	98	187	11000011	162	59	10100011
35	70	01100010	99	185	11000010	163	57	10100010
36	72	01100110	100	183	11000110	164	55	10100110
37	74	01100111	101	181	11000111	165	53	10100111
38	76	01100101	102	179	11000101	166	51	10100101
39	78	01100100	103	177	11000100	167	49	10100100
40	80	01101100	104	175	11001100	168	47	10101100
41	82	01101101	105	173	11001101	169	45	10101101
42	84	01101111	106	171	11001111	170	43	10101111
43	86	01101110	107	169	11001110	171	41	10101110
44	88	01101010	108	167	11001010	172	39	10101010
45	90	01101011	109	165	11001011	173	37	10101011
46	92	01101001	110	163	11001001	174	35	10101001
47	94	01101000	111	161	11001000	175	33	10101000
48	96	01111000	112	159	11011000	176	31	10111000
49	98	01111001	113	157	11011001	177	29	10111001
50	100	01111011	114	155	11011011	178	27	10111011
51	102	01111010	115	153	11011010	179	25	10111010
52	104	01111110	116	151	11011110	180	23	10111110
53	106	01111111	117	149	11011111	181	21	10111111
54	108	01111101	118	147	11011101	182	19	10111101
55	110	01111100	119	145	11011100	183	17	10111100
56	112	01110100	120	143	11010100	184	15	10110100
57	114	01110101	121	141	11010101	185	13	10110101
58	116	01110111	122	139	11010111	186	11	10110111
59	118	01110110	123	137	11010110	187	9	10110110
60	120	01110010	124	135	11010010	188	7	10110010
61	122	01110011	125	133	11010011	189	5	10110011
62	124	01110001	126	131	11010001	190	3	10110001
63	126	01110000	127	129	11010000	191	1	10110000

Figure C.7: APV25-S0 Pipeline Column Address Code (Gray Code). This code is also used for the successor chip, the APV25-S1.

Source: [103]

If the amplifier output voltage is sampled at regular intervals, it is convenient to write equation C.1 in matrix form as:

$$V_i = \sum_j H_{ij} S_j \quad \text{or} \quad \mathbf{V} = \mathbf{H} \cdot \mathbf{S}. \quad (\text{C.2})$$

The original signal can be recovered by performing the inverse operation

$$\mathbf{S} = \mathbf{H}^{-1} \cdot \mathbf{H} \cdot \mathbf{S} \equiv \mathbf{W} \cdot \mathbf{V}. \quad (\text{C.3})$$

For the CR-RC filter implemented in the APV scheme, the elements of the weight matrix $\mathbf{W}$ reduce to a particularly simple form. If the system response is described by

$$v(t) = \frac{ct}{\tau} e^{-t/\tau} \quad \text{for } t \geq 0, \quad (\text{C.4})$$

there are only three non-zero weights necessary to receive the original signal (c is a constant).

$$s_k = w_1 v_k + w_2 v_{k-1} + w_3 v_{k-2}, \quad (\text{C.5})$$

with

$$w_1 = \frac{e^{\Delta t/\tau-1}}{\Delta t/\tau}, \quad w_2 = \frac{-2e^{-1}}{\Delta t/\tau}, \quad w_3 = \frac{e^{-\Delta t/\tau-1}}{\Delta t/\tau}. \quad (\text{C.6})$$

Δt is the sample interval which is 25 ns in case of LHC.

C.5 Front End Hybrid Bar Code Definition

Part Number	Tracker	APV #	Connector	Notation
1163	TEC	4	top	TEC_4_up
1165	TEC	6	top	TEC_6_up
1166	TEC	6	bottom	TEC_6_down
1168	TIB	4	bottom	TIB_4_down
1170	TIB	6	bottom	TIB_6_down
1171	TOB	4	top	TOB_4_up
1172	TOB	4	bottom	TOB_4_down
1173	TOB	6	top	TOB_6_up
1175	TOB	4	top	TOB_4_up
1176	TOB	4	bottom	TOB_4_down
1177	TIB	6	top	TIB_6_up
1178	TIB	6	bottom	TIB_6_down

Table C.1: The FE hybrid bar code scheme. In general the bar code reads as follows:
302{part number}{part serial ID number} (see figure 6.1).

C.6 Hybrid and Module Nomenclature

Name	Bar Code	Description	Object Type
Ex1-1	30216630200007	express-line 1, ceramic hybrid	module
Ex1-2	30216630200012	express-line 1, ceramic hybrid	module
Ex1-3	30216630200013	express-line 1, ceramic hybrid	module
Ex1-4	30216630200017	express-line 1, ceramic hybrid	module
Ex1-5	30216630200020	express-line 1, ceramic hybrid	module
Ex1-6	30216630200022	express-line 1, ceramic hybrid	module
Ex1-7	30216630200023	express-line 1, ceramic hybrid	module
Ex1-8	30216630200026	express-line 1, ceramic hybrid	module
Ex1-9	30216630200027	express-line 1, ceramic hybrid	module
Ex1-10	30216630200029	express-line 1, ceramic hybrid	module
Ex1-11	30216630200048	express-line 1, ceramic hybrid	module
Ex1-12	30216630200056	express-line 1, ceramic hybrid	module
Ex2-1	30216630200097	express-line 2, ceramic hybrid	module
Ex2-2	30216630200098	express-line 2, ceramic hybrid	module
Ex2-3	30216630200099	express-line 2, ceramic hybrid	module
Ex2-4	30216630200100	express-line 2, ceramic hybrid	module
Ex2-5	30216630200101	express-line 2, ceramic hybrid	module
Ex2-6	30216630200102	express-line 2, ceramic hybrid	module
Ex2-7	30216630200104	express-line 2, ceramic hybrid	module
Ex2-8	30216630200105	express-line 2, ceramic hybrid	module
Ex2-9	30216630200106	express-line 2, ceramic hybrid	module
Mod-1	30216711300238	flex-rigid, prototype	module
Hyb-1	30216711100216	flex-rigid, prototype	hybrid
Hyb-2	30216650500159	ceramic, prototype	hybrid

Table C.2: Nomenclature of FE hybrids and modules. At present modules are characterized by the corresponding hybrid bar codes. During the large-scale production a module will probably be identified by a two-dimensional dice label located on the frame.

Appendix D

Test Environment Specifics

D.1 ARC Features and Specifications

Type	Function	Comment
<i>Clock</i>	internal 40 MHz, or external clock input	software selectable LVDS up to 40 MHz
	clock output	LVDS
<i>Trigger</i>	input internal	software
	input external	NIM or LVDS
	output	LVDS
<i>Hybrid I/O</i>	analogue inputs	6 differential voltages
	impedance	50 Ohm
	slow control	3 standard buffered I ² C links
	clock/trigger	2 LVDS clock lines 2 LVDS trigger lines
<i>Expansion Port</i>	input or output	clock: LVDS trigger: LVDS synchronized trigger: LVDS APV trigger: LVDS
<i>Power Requirements</i>	1.4 A at +5 V 60 mA at −5 V	

Table D.1: Specifications of the APV Readout Controller board.

Source: [65]

D.2 New Components of the ARC System

At the beginning of the year 2003, the ARC system was modified and expanded by two components, the *ARC FE_M adapter card* (see figure D.1) and the *DEPP board* (see figure D.2). Both components were not used for the measurements presented in this thesis.

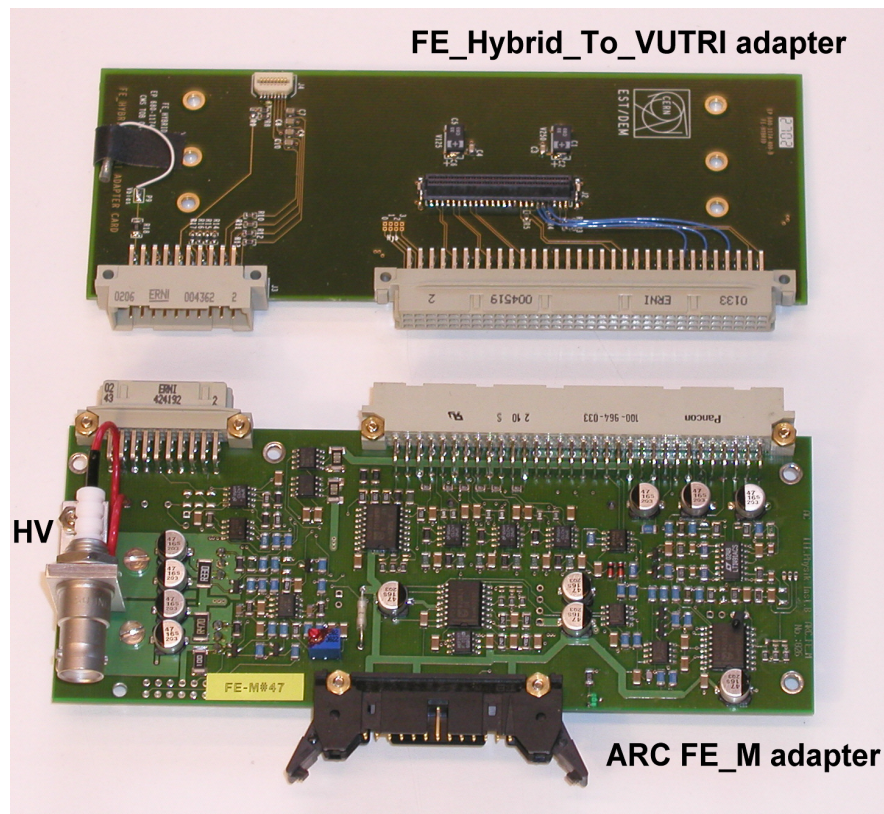


Figure D.1: The new ARC FE_M adapter card (bottom) can be connected to the so-called *FE_Hybrid_To_VUTRI* adapter (top) provided by CERN. The latter card will connect the modules to the readout system. This card is a common interface to different test setups.

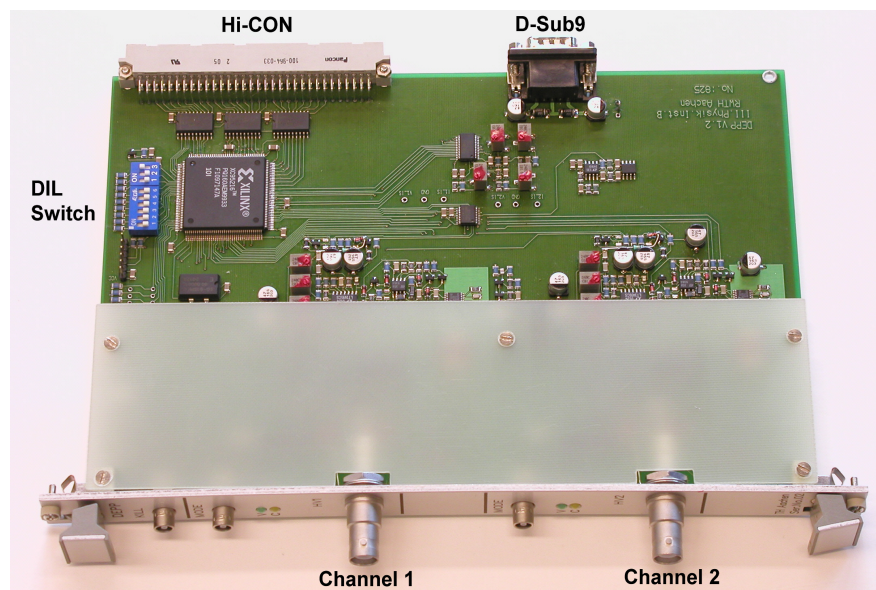


Figure D.2: The DEPP board which is suited to bias two modules (channel 1 and 2).

D.3 LED Characteristics

Parameter	Value
LED radial package	5 mm
temperature range	$-40... + 100\text{ }^{\circ}\text{C}$
reverse voltage V_R	3 V
forward current I_F	100 mA
power dissipation	180 mW
wavelength at peak emission	950 nm
half angle	$\pm 7^{\circ}$
active chip area	0.09 mm^2
switching time	10 ns
capacitance	35 pF

Table D.2: Characteristics of LED type SFH 4501.

Source: [70]

D.4 Specifications of the Peltier Element

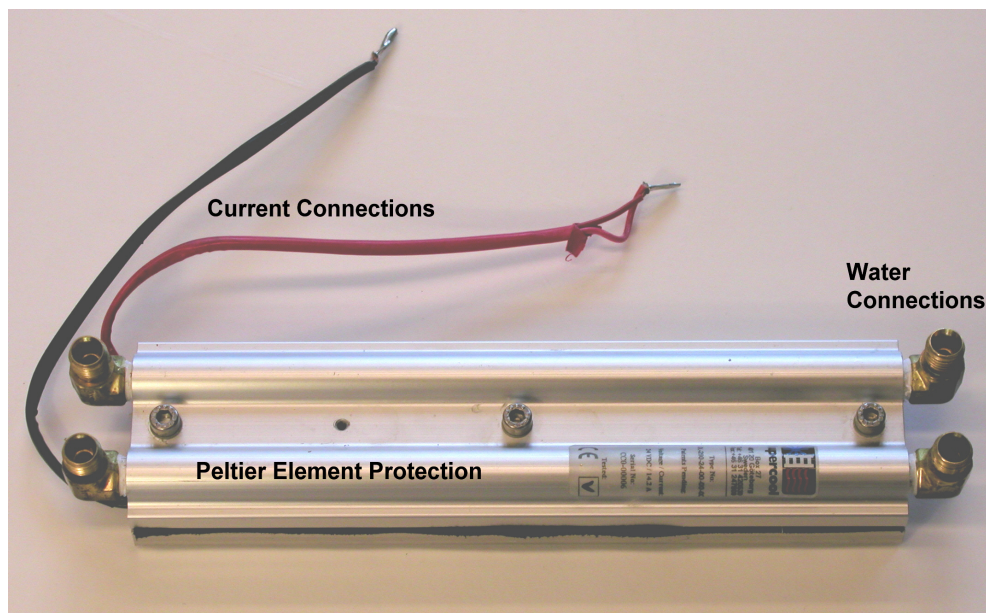


Figure D.3: Peltier element of type DL-290-24-00-00-00.

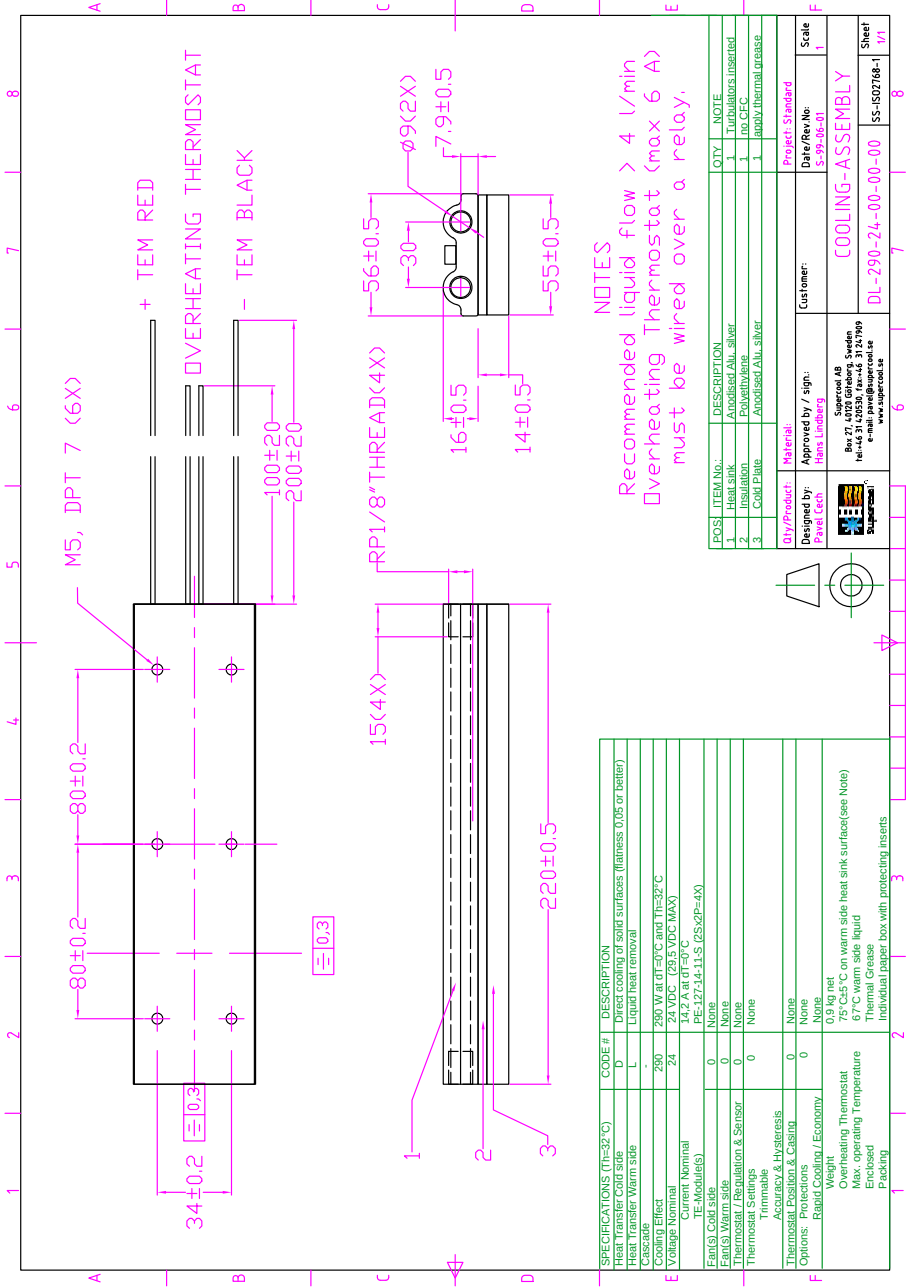


Figure D.4: Layout of the peltier element DL-290-24-00-00-00.

Source: [74]

D.5 Calculation of the Dew-point

The dew-point DP defines the temperature at which the air would become saturated (with respect to water) if cooled at constant pressure and without the addition or removal of water vapour. When the temperature cools to the dew-point, the air becomes saturated and fog, dew, or frost can occur.

The dew-point can be deduced from the relative humidity RH (given in %) and the environment temperature T (given in °C) as shown in the following equations:

$$\log Ew = 0.66077 + \frac{7.5 \cdot T}{237.5 + T} + \log RH - 2, \quad (D.1)$$

$$DP = \frac{237.3 \cdot (0.66077 - \log Ew)}{\log Ew - 8.16077}, \quad (D.2)$$

where Ew is the saturation vapour pressure over water. These formulas are commonly used approximations. They are described in [104].

Examples:

$$RH = 50\%, T = 25\text{ °C} \rightarrow DP = 13.9\text{ °C},$$

$$RH = 10\%, T = 25\text{ °C} \rightarrow DP = -8.7\text{ °C},$$

$$RH = 12\%, T = 10\text{ °C} \rightarrow DP = -18.6\text{ °C}.$$

Appendix E

Measurements with the ARC System

E.1 Calibration Pulse Shapes in Deconvolution Mode

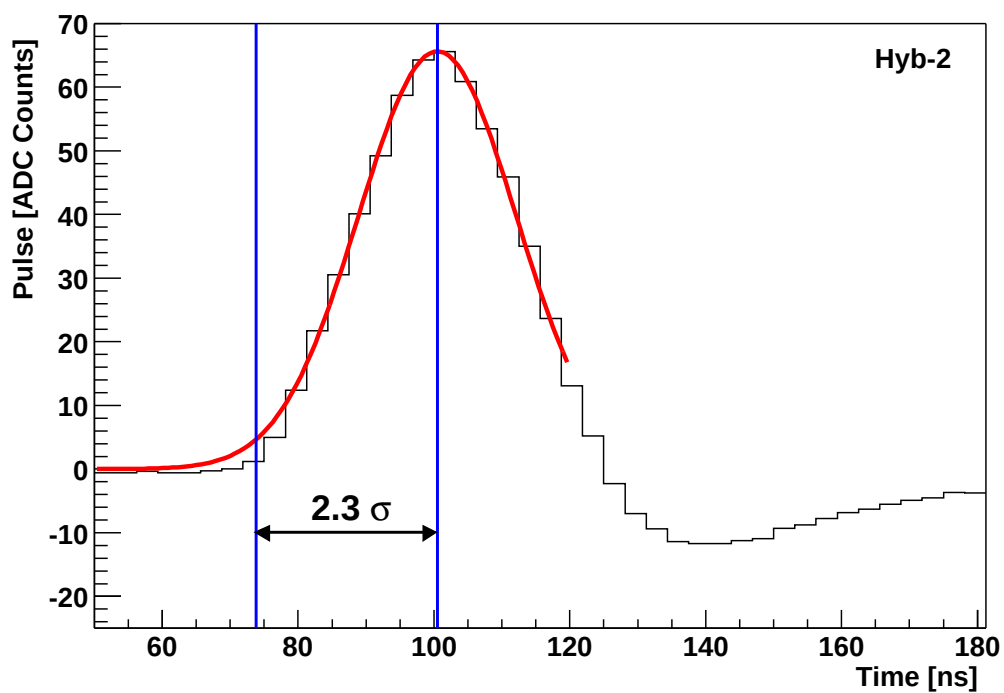


Figure E.1: Rise time definition in deconvolution mode: $2.3 \cdot \sigma \approx RT$. σ is the standard deviation of the fit function [6.14](#).

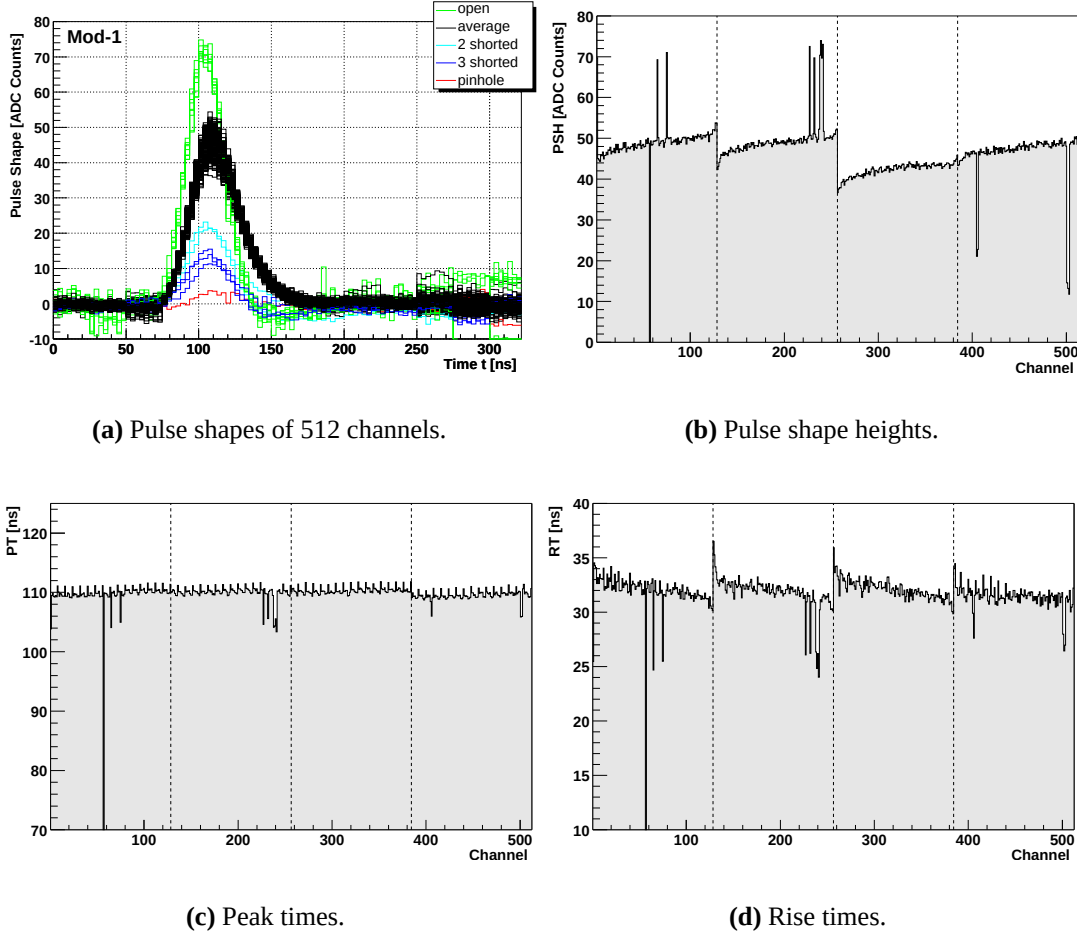
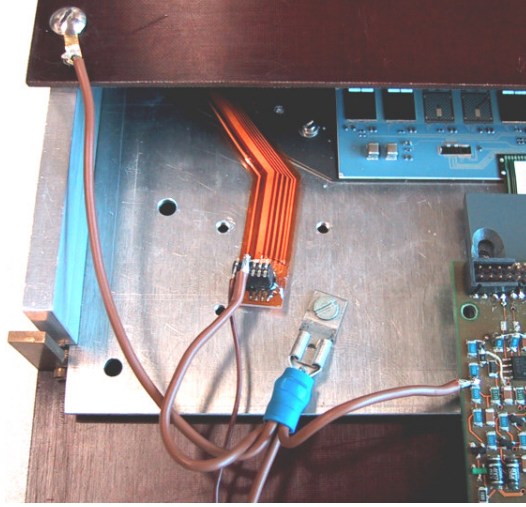


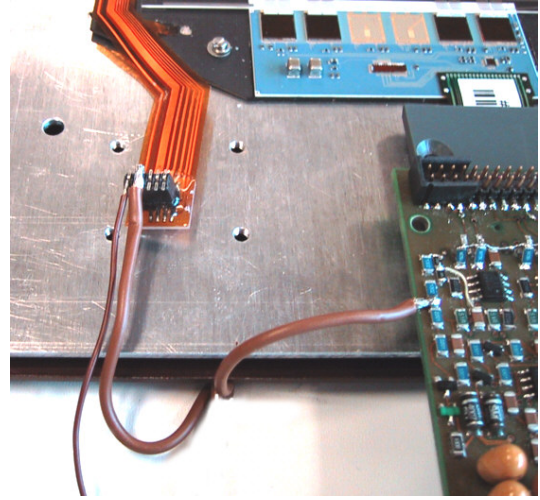
Figure E.2: Calibration pulse test in deconvolution mode. Different types of strip errors show up with different shape signatures.

E.2 Impacts of Grounding on Calibration Pulse Shapes

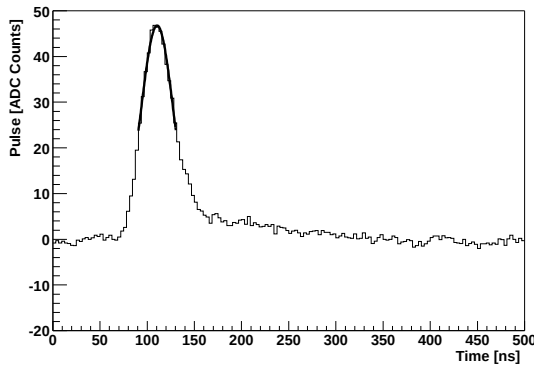
During the tests of the express-line series it became evident that a proper grounding scheme is an essential condition for reliable measurements. As an example, two different types of grounding scenarios of a module with respect to its environment are depicted in the figures E.3(a) and E.3(b). The “good” scheme is pictured in figure E.3(a) where all components (module, hybrid, carrier, FE adapter, and test box) are connected to a common ground. As a result, the calibration pulse shape measurement (in deconvolution mode, inverter off) reveals no problem (figure E.3(c)). On the contrary, in the case of a “bad” grounding scenario (only hybrid and module have the same electric potential) the calibration pulse shows a distorted shape as presented in figure E.3(d). This means that extremely bad grounding conditions may cause wrong shape fits and presumably faulty marked bad channels in an automated test procedure.



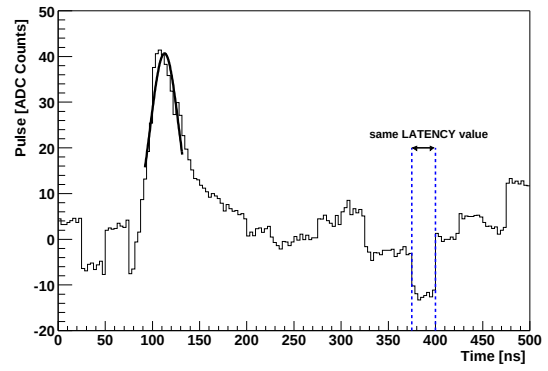
(a) Good grounding scheme.



(b) Bad grounding scheme.



(c) Good grounding.



(d) Bad grounding.

Figure E.3: Grounding effects on pulse shapes (deconvolution mode). The distortions occur for all eight CSEL settings at certain LATENCY values.

E.3 LED Calibration

Figure E.4 pictures the environment used to test the 16 different LED arrays produced in Aachen. The measurements were done at ambient temperature with the same module (Ex1-7) supplied with a bias voltage of $V_{bias} = 150$ V.

This module was modified with artificial failures (one open at channel 101, three pinholes at 163,183, and 203, two shorts at 223/224 and 243/244) which were all found in the LED tests shown in the figures E.5 and E.7.

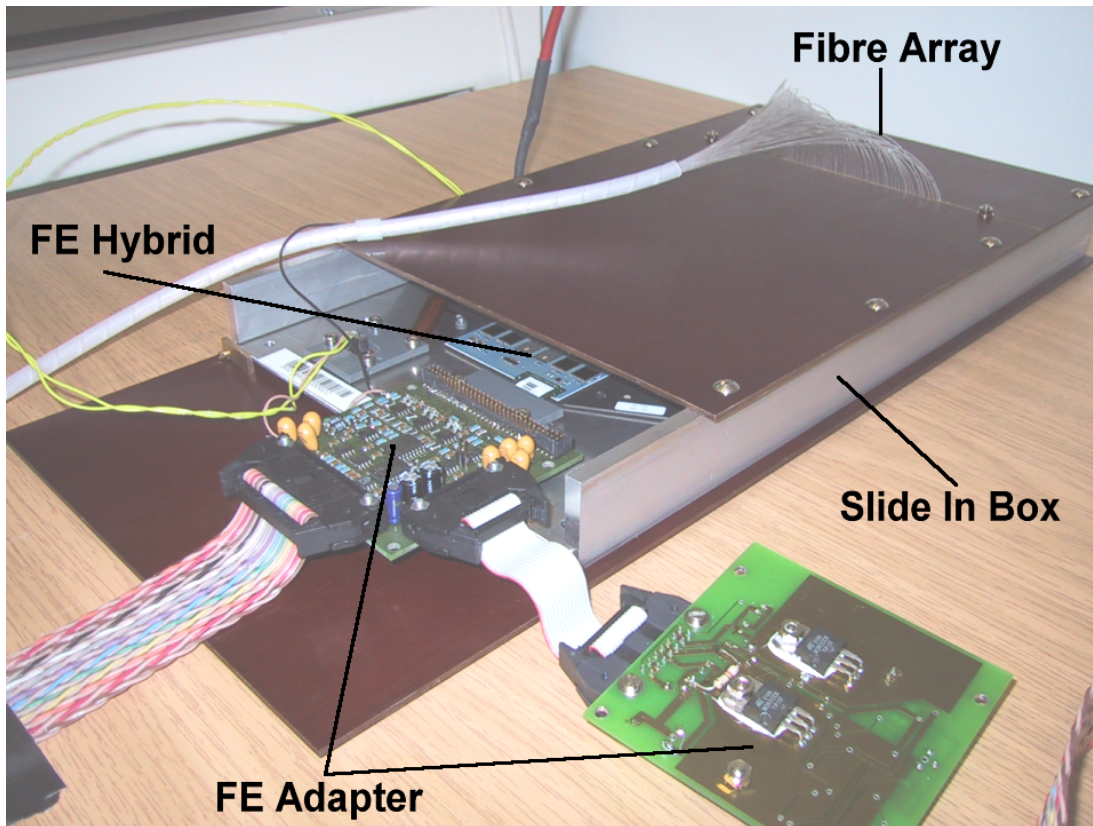


Figure E.4: Test box with an optical fibre array.

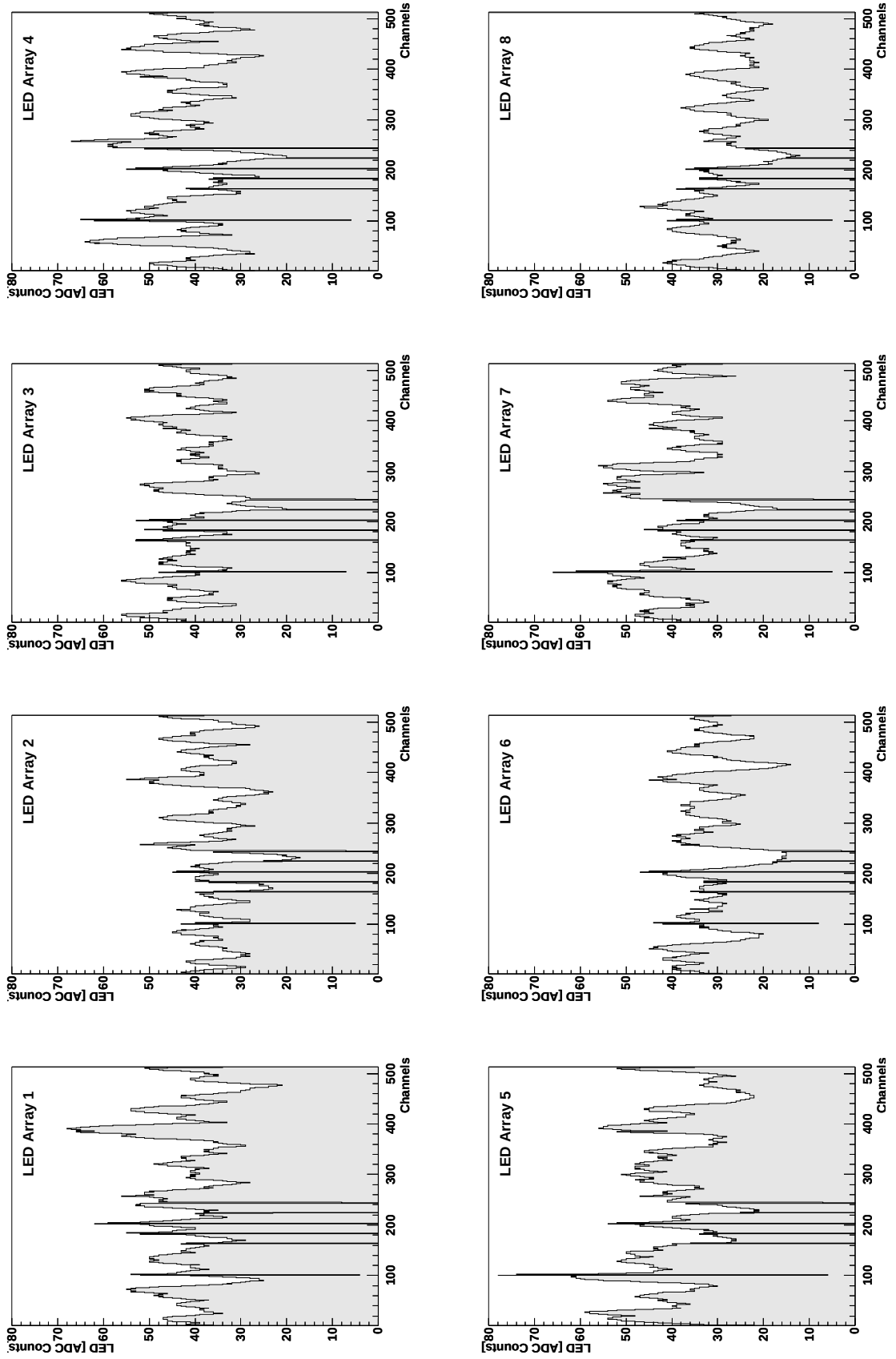


Figure E.5: Response of module Ex1-7 to pulsed light from LED array 1 to 8.

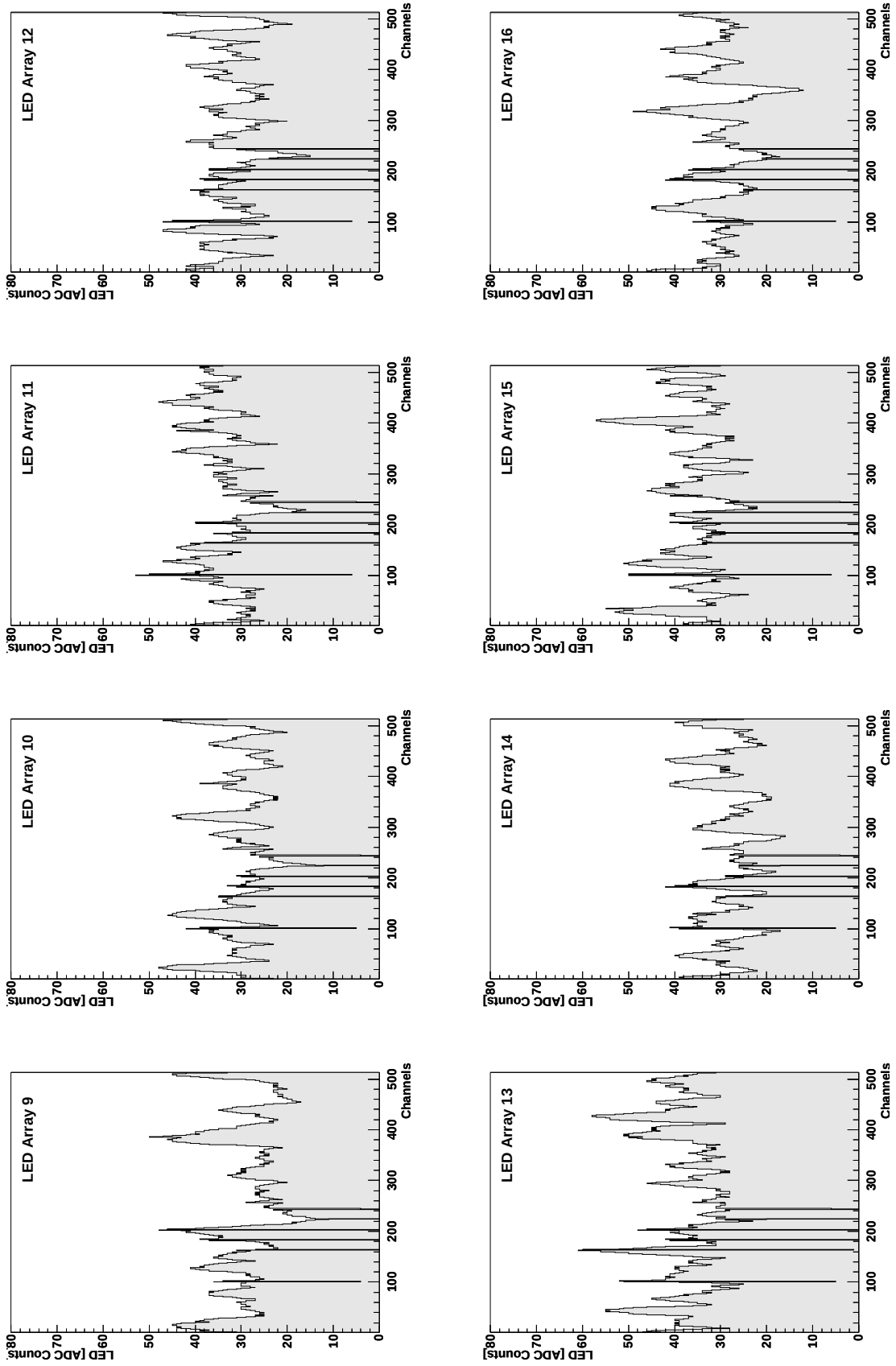


Figure E.6: Response of module Ex1-7 to pulsed light from LED array 9 to 16.

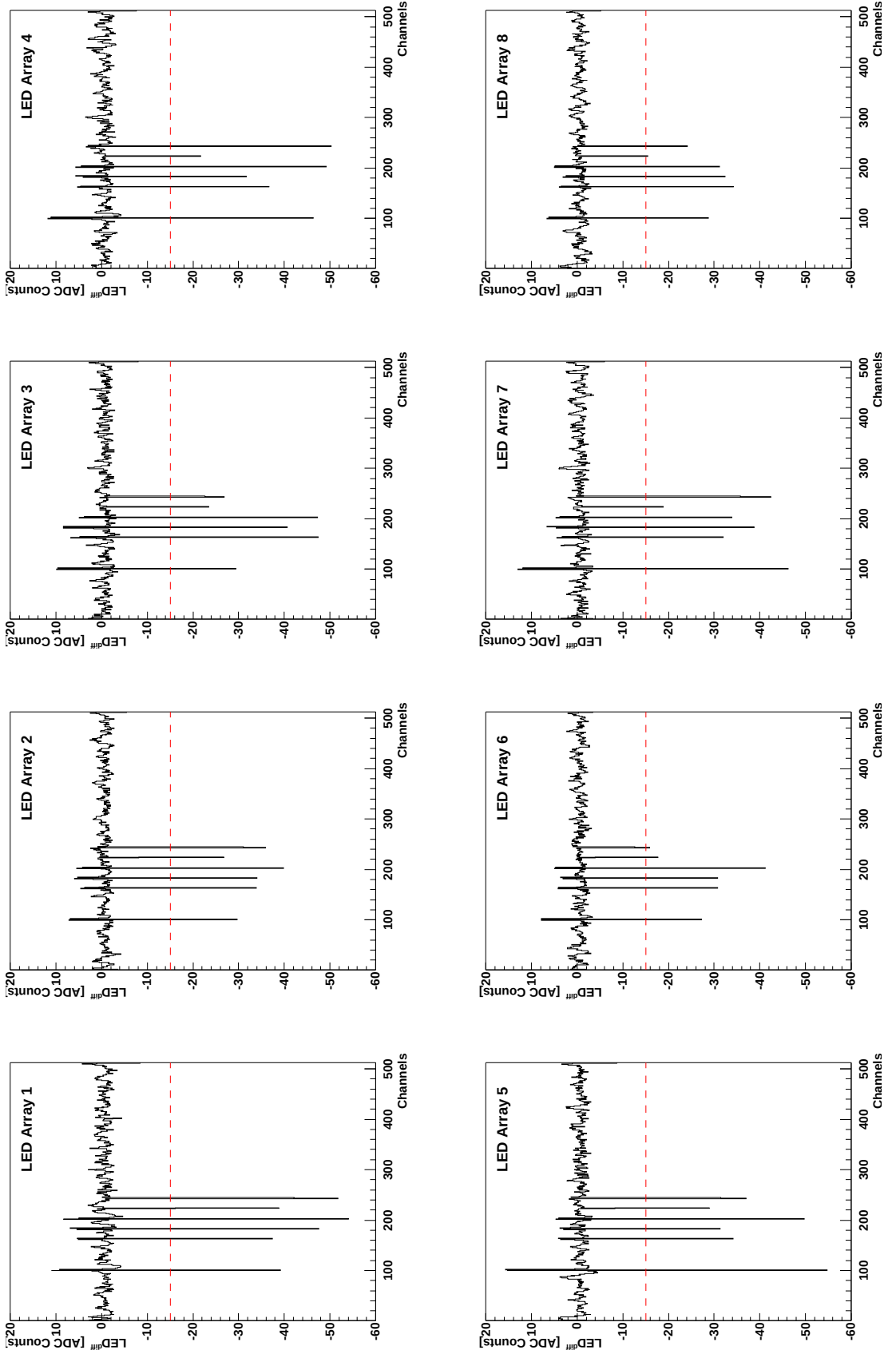


Figure E.7: Difference of measured and ideal light responses (based on measurements shown in figure E.5). The dashed lines indicate an effective cut at -15 ADC counts.

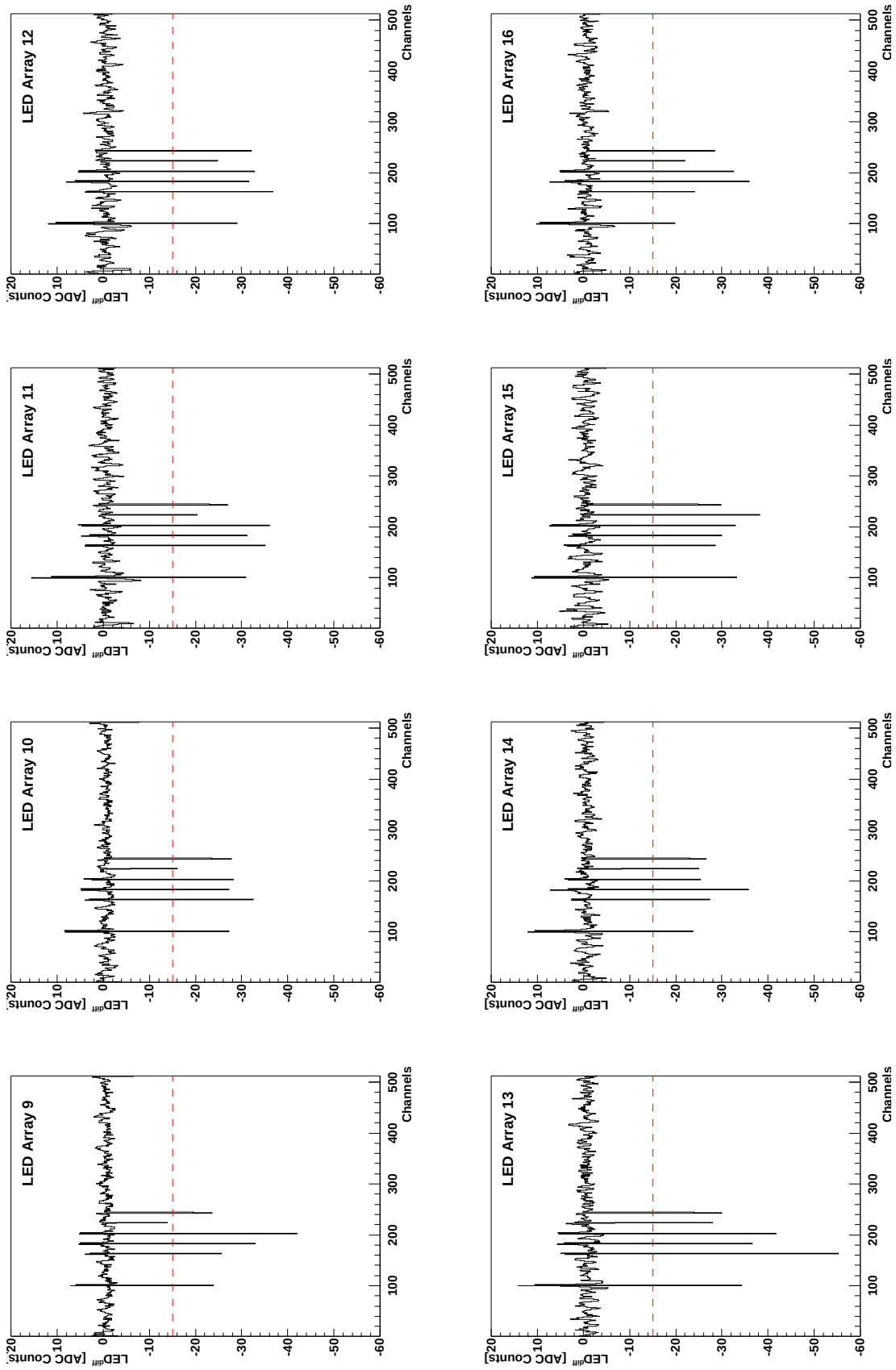


Figure E.8: Difference of measured and ideal light responses (based on measurements shown in figure E.6). The dashed lines indicate an effective cut at -15 ADC counts.

E.4 Express-line 1 Results at Ambient Temperature

Module	APV	Noise [ADC Counts]		Pulse Shape [ADC Counts]				Pulsed Light [ADC Counts]	
		$\bar{\sigma}$	RMS	$\overline{PSH}$	RMS	$\overline{RT}$	RMS	$\overline{LED}$	RMS
Ex1-1	0x40	1.86	0.05	60.55	1.68	48.18	0.78	25.04	3.09
	0x42	1.45	0.04	58.41	1.37	48.57	0.86	24.86	3.36
	0x48	1.48	0.04	59.92	1.21	49.10	0.58	24.80	2.71
	0x4a	1.57	0.05	57.26	1.37	49.07	0.68	24.48	3.47
Ex1-2	0x40	1.55	0.06	59.11	1.34	50.86	0.66	25.39	4.64
	0x42	1.52	0.06	60.96	0.63	50.68	0.42	24.26	2.89
	0x48	1.55	0.05	58.81	0.93	50.47	0.53	25.06	2.27
	0x4a	1.48	0.05	56.74	0.45	54.98	0.71	28.66	3.91
Ex1-3	0x40	1.82	0.05	60.75	0.87	52.52	0.91	27.89	3.43
	0x42	1.46	0.03	57.17	0.71	51.59	0.88	28.51	3.76
	0x48	1.43	0.02	55.14	0.75	48.95	0.69	25.93	2.46
	0x4a	1.50	0.04	61.20	1.18	49.69	0.82	26.61	3.17
Ex1-4	0x40	1.60	0.13	56.02	1.15	49.79	0.52	22.13	2.70
	0x42	1.68	0.12	61.03	0.68	49.47	0.36	23.44	2.65
	0x48	1.54	0.07	60.99	1.28	49.21	0.42	25.31	2.27
	0x4a	1.57	0.11	60.94	0.82	49.70	0.47	25.00	3.44
Ex1-5	0x40	1.58	0.08	63.74	0.85	51.89	0.40	27.20	3.26
	0x42	1.49	0.10	62.18	0.79	50.71	0.39	25.71	2.99
	0x48	1.54	0.06	60.79	1.02	50.52	0.42	26.20	2.42
	0x4a	1.49	0.09	60.13	0.93	50.90	0.38	25.24	3.43
Ex1-6	0x40	1.63	0.09	56.51	1.98	49.64	0.50	24.58	3.12
	0x42	1.52	0.08	65.08	1.57	49.79	0.36	25.37	3.06
	0x48	1.52	0.05	62.70	1.50	50.10	0.37	26.72	3.32
	0x4a	1.57	0.10	57.10	0.93	50.33	0.37	27.23	5.51
Ex1-7	0x40	1.54	0.09	57.38	1.65	51.13	0.47	25.52	3.01
	0x42	1.48	0.05	62.02	1.39	50.72	0.40	24.88	2.80
	0x48	1.53	0.06	57.01	1.37	51.38	0.47	26.85	2.46
	0x4a	1.57	0.11	63.39	1.08	51.71	0.33	27.38	3.49
Ex1-8	0x40	1.54	0.09	55.62	0.50	49.06	0.52	25.04	3.10
	0x42	1.51	0.09	60.37	0.56	49.56	0.40	23.56	2.52
	0x48	1.50	0.06	64.01	0.76	49.78	0.38	25.20	2.04
	0x4a	1.59	0.08	62.85	0.55	49.72	0.39	26.07	3.44
Ex1-9	0x40	1.62	0.12	58.73	1.06	49.75	0.46	23.70	2.91
	0x42	1.52	0.06	61.13	0.65	49.36	0.33	24.62	2.72
	0x48	1.52	0.06	61.17	0.95	49.49	0.45	25.93	2.41
	0x4a	1.55	0.06	63.21	0.85	50.36	0.42	27.89	3.67
Ex1-10	0x40	1.53	0.08	58.70	0.90	51.19	0.42	26.64	3.24
	0x42	1.47	0.06	58.36	0.87	50.87	0.31	26.22	2.94
	0x48	1.51	0.07	62.30	1.01	50.95	0.41	28.18	2.68
	0x4a	1.56	0.07	62.38	0.70	51.12	0.42	26.91	3.40
Ex1-11	0x40	1.46	0.04	63.70	1.10	50.52	0.33	24.45	3.16
	0x42	1.49	0.05	63.52	0.82	49.64	0.33	23.84	3.12
	0x48	1.49	0.04	65.42	0.75	49.60	0.36	25.64	3.44
	0x4a	1.54	0.06	64.65	0.60	50.15	0.45	24.38	3.67
Ex1-12	0x40	1.55	0.09	62.03	0.96	50.05	0.50	26.34	3.19
	0x42	1.50	0.06	56.97	0.85	48.75	0.52	23.41	2.82
	0x48	1.56	0.07	57.35	0.80	49.01	0.44	26.10	2.25
	0x4a	1.56	0.06	57.65	1.22	49.10	0.52	24.34	3.30

Table E.1: Summary table of the express-line 1 test results. The mean values are truncated values as described at the beginning of chapter 6. All tests were done in peak mode.

E.5 Express-line 2 Results at Ambient Temperature

Module	APV	Noise [ADC Counts]		Common Mode [ADC Counts]		Pulse Shape [ADC Counts]			
		$\bar{\sigma}$	RMS	$\overline{CMN}$	RMS	$\overline{PSH}$	RMS	$\overline{RT}$	RMS
Ex2-1	0x40	2.00	0.03	-0.01	0.54	-45.40	2.08	30.66	1.02
	0x42	1.90	0.05	-0.04	0.51	-45.27	1.66	30.63	0.96
	0x48	1.89	0.03	-0.01	0.49	-49.21	1.47	30.46	0.77
	0x4a	1.88	0.06	-0.02	0.53	-47.42	0.99	31.02	0.82
Ex2-2	0x40	1.89	0.06	-0.03	0.51	-48.82	1.78	31.18	0.90
	0x42	1.87	0.07	-0.01	0.52	-49.91	1.25	30.84	0.84
	0x48	1.87	0.06	-0.01	0.50	-49.91	1.25	30.84	0.84
	0x4a	1.96	0.07	-0.01	0.54	-49.79	1.72	30.73	0.98
Ex2-3	0x40	1.94	0.03	0.01	0.53	-46.82	2.23	30.80	0.94
	0x42	1.87	0.03	0.00	0.51	-44.53	1.82	31.01	0.85
	0x48	1.89	0.03	0.01	0.50	-43.87	1.73	30.79	0.88
	0x4a	2.01	0.06	0.03	0.57	-47.55	1.23	30.74	0.84
Ex2-4	0x40	2.05	0.03	-0.01	0.54	-43.57	1.83	30.77	0.98
	0x42	1.87	0.04	0.01	0.52	-47.41	1.31	31.14	0.89
	0x48	1.80	0.05	-0.01	0.49	-47.38	1.47	31.39	0.87
	0x4a	1.91	0.04	-0.01	0.54	-47.77	1.22	30.71	0.70
Ex2-5	0x40	1.96	0.03	-0.01	0.54	-43.40	1.99	30.80	1.07
	0x42	1.96	0.04	0.00	0.53	-47.19	1.88	30.42	0.74
	0x48	2.02	0.04	-0.01	0.53	-45.14	1.41	30.86	0.77
	0x4a	2.08	0.06	0.01	0.58	-46.04	1.27	30.52	0.73
Ex2-6	0x40	1.96	0.06	-0.01	0.54	-48.48	2.23	30.24	0.98
	0x42	1.89	0.06	-0.02	0.51	-46.96	1.43	30.28	0.74
	0x48	1.98	0.06	-0.01	0.52	-47.89	1.56	30.04	0.69
	0x4a	2.01	0.09	0.01	0.58	-45.53	0.94	30.37	0.62
Ex2-7	0x40	2.15	0.07	-0.03	0.56	-45.74	1.93	30.09	0.89
	0x42	1.88	0.07	-0.04	0.52	-45.36	2.02	31.72	1.27
	0x48	1.91	0.07	-0.02	0.49	-43.63	1.81	30.63	0.82
	0x4a	1.97	0.10	-0.04	0.54	-46.07	1.27	30.57	0.74
Ex2-8	0x40	1.92	0.06	-0.02	0.51	-46.04	2.22	30.69	1.03
	0x42	1.94	0.06	-0.02	0.51	-49.23	1.66	30.39	0.82
	0x48	1.88	0.05	-0.02	0.48	-45.05	1.48	31.01	0.79
	0x4a	1.94	0.08	-0.02	0.55	-48.21	1.44	30.87	0.83
Ex2-9	0x40	1.90	0.06	0.01	0.52	-45.92	1.99	30.99	1.08
	0x42	1.85	0.07	-0.02	0.50	-43.53	1.70	31.01	0.98
	0x48	1.92	0.06	-0.02	0.49	-45.40	2.25	30.76	0.93
	0x4a	2.03	0.09	0.00	0.56	-44.93	1.02	30.44	0.75

Table E.2: Summary table of the express-line 2 test results. The mean values are truncated values as described at the beginning of chapter 6. All tests were performed in deconvolution mode.

Module	APV	Noise		Common Mode		Pulse Shape			Pulsed Light		Pinhole	
		$\bar{\sigma}$	[ADC Counts] RMS	$\overline{CMN}$	[ADC Counts] RMS	$\overline{PSH}$	[ADC Counts] RMS	$\overline{RT}$	$\overline{LED}$	[ADC Counts] RMS	$\overline{\Delta PIN}$	[ADC Counts] RMS
Ex2-1	0x40	1.58	0.03	-0.02	0.38	-51.66	0.89	53.07	33.66	5.05	8.92	1.26
	0x42	1.50	0.04	-0.05	0.36	-51.34	1.01	52.64	33.90	6.37	9.39	1.85
	0x48	1.49	0.03	-0.03	0.35	-56.03	1.13	51.97	35.27	3.35	8.81	1.38
	0x4a	1.52	0.05	-0.02	0.38	-55.39	0.79	52.89	33.41	5.43	9.44	1.33
Ex2-2	0x40	1.52	0.05	0.00	0.35	-56.55	1.02	53.82	32.89	4.87	8.82	1.23
	0x42	1.48	0.06	0.01	0.35	-57.26	0.77	53.93	34.59	6.86	8.31	1.78
	0x48	1.47	0.05	0.01	0.34	-59.91	1.54	54.11	36.30	3.25	8.61	1.31
	0x4a	1.54	0.06	0.01	0.39	-56.76	2.11	53.31	35.55	5.62	9.47	1.57
Ex2-3	0x40	1.52	0.03	-0.02	0.37	-53.93	1.25	52.79	35.73	5.44	8.88	1.36
	0x42	1.49	0.03	-0.03	0.36	-50.79	1.08	52.31	36.18	7.49	8.79	1.24
	0x48	1.49	0.03	-0.02	0.34	-49.93	0.90	51.72	39.61	4.04	8.81	1.28
	0x4a	1.58	0.05	-0.01	0.40	-53.99	0.94	52.06	38.75	5.99	9.15	1.44
Ex2-4	0x40	1.63	0.03	-0.03	0.38	-53.10	3.53	50.62	32.23	4.85	6.66	0.92
	0x42	1.49	0.03	-0.02	0.36	-54.96	0.86	53.09	32.51	6.82	6.39	1.02
	0x48	1.44	0.03	-0.02	0.33	-55.67	1.00	53.67	32.75	3.39	6.09	0.74
	0x4a	1.51	0.04	-0.02	0.38	-54.96	1.05	52.64	34.38	4.95	6.39	0.91
Ex2-5	0x40	1.57	0.03	-0.02	0.37	-49.51	1.09	52.83	34.84	5.26	8.40	2.09
	0x42	1.54	0.03	-0.04	0.36	-53.17	1.56	51.90	36.41	7.18	5.28	0.71
	0x48	1.58	0.04	0.00	0.36	-53.55	3.39	50.03	39.02	3.29	5.28	0.72
	0x4a	1.64	0.05	-0.01	0.41	-54.18	3.69	50.64	37.01	5.67	5.43	0.67
Ex2-6	0x40	1.53	0.05	-0.02	0.37	-54.49	1.06	52.78	30.89	4.58	9.01	1.54
	0x42	1.47	0.05	-0.02	0.35	-53.38	0.71	52.71	32.08	6.47	9.16	1.50
	0x48	1.55	0.05	-0.03	0.35	-53.68	0.77	51.69	34.73	3.12	9.48	1.40
	0x4a	1.59	0.07	0.01	0.40	-51.70	0.95	52.30	33.61	5.36	9.86	1.61
Ex2-7	0x40	1.68	0.06	0.02	0.43	-55.83	3.41	50.56	34.66	5.06	9.87	1.59
	0x42	1.51	0.07	-0.02	0.38	-54.34	1.08	54.44	35.14	6.69	9.20	1.42
	0x48	1.51	0.06	-0.02	0.36	-50.23	0.99	52.29	35.27	3.08	9.08	1.22
	0x4a	1.56	0.07	-0.01	0.39	-52.86	1.03	52.74	33.63	5.33	9.34	1.44
Ex2-8	0x40	1.50	0.05	-0.02	0.35	-53.33	0.73	52.85	31.85	4.53	8.97	1.35
	0x42	1.50	0.06	0.00	0.34	-55.78	1.43	51.88	33.97	6.58	8.67	1.42
	0x48	1.50	0.06	-0.01	0.33	-51.70	0.99	52.77	34.56	3.04	8.97	1.32
	0x4a	1.56	0.07	-0.02	0.36	-55.28	1.41	52.65	33.67	5.57	8.93	1.43
Ex2-9	0x40	1.53	0.06	0.00	0.37	-53.67	0.89	54.23	31.23	4.59	9.02	1.23
	0x42	1.48	0.05	-0.03	0.34	-50.53	1.24	53.82	31.89	6.29	8.73	1.25
	0x48	1.52	0.05	-0.03	0.34	-51.87	1.64	53.13	34.98	2.99	8.98	1.41
	0x4a	1.60	0.06	-0.03	0.39	-50.30	1.69	52.34	34.66	5.30	9.48	1.81

Table E.3: Summary table of the express-line2 test results. The mean values are truncated values as described at the beginning of chapter 6. All tests were done in peak mode.

E.6 Express-line 2 Results at Different Temperatures

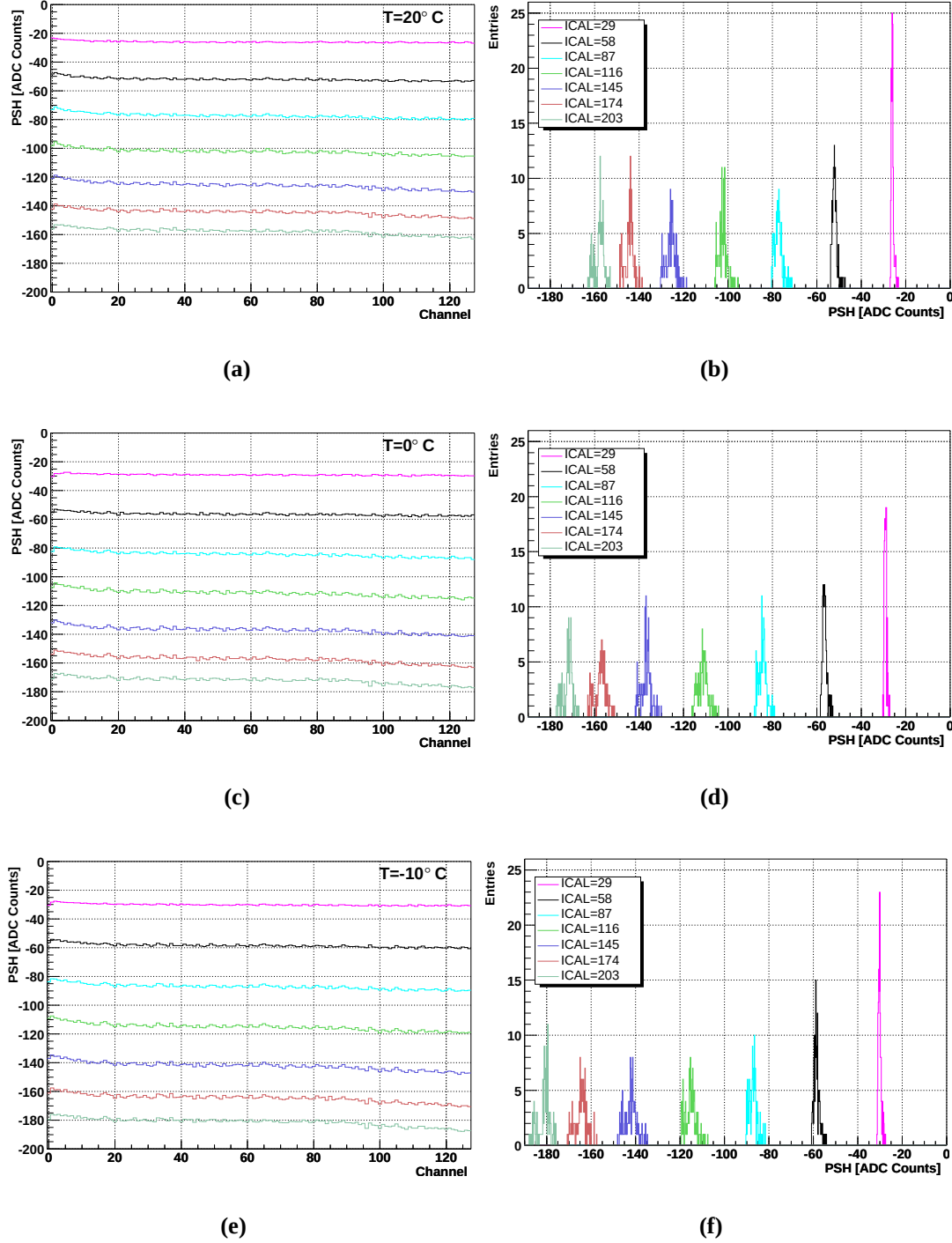


Figure E.9: Different calibration pulse shape heights at three temperatures. (a) PSH versus the channel number of APV 0x40 of module Ex2-4 and (b) PSH distributions for different ICAL values at $T = +20^\circ\text{C}$. The same measurements are shown in (c) and (d) at $T = 0^\circ\text{C}$, and in (e) and (f) at $T = -10^\circ\text{C}$.

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Glossary

ACDC	Aachen Cooling Device Control
ADC	Analogue-to-Digital Converter
ALICE	A Large Ion Collider Experiment
AMS	Alpha Magnetic Spectrometer
APSP	Analogue Pulse Shape Processor
APV	Analogue Pipeline - Voltage Mode
APVMUX	APV Multiplexer
ARC	APV Readout Controller
ASIC	Application Specific Integrated Circuit
ATLAS	A Toroidal LHC ApparatuS
CDF	Collider Detector at Fermilab
CERN	Conceil Européenne pour la Recherche Nucléaire
CINT	C++ Interpreter
CKM	Cabbibo-Kobayashi-Maskawa
CMOS	Complementary Metal-Oxide-Semiconductor
CMS	Compact Muon Solenoid
CUMO	Current Monitor
DB	Data Base File
DCU	Detector Control Unit
DEPP	DEpletion Power
DIL	Dual InLine
DLL	Dynamic Link Library
DP	Dew-point

ECAL Electromagnetic CALorimeter

ENC Equivalent Noise Charge

EPP Enhanced Parallel Port

FE Front End

FET Field Effect Transistor

FIFO First In, First Out

FWHM Full-Width Half-Maximum

GUI Graphical User Interface

HCAL Hadronic CALorimeter

HLT High Level Trigger

I²C Inter Integrated Circuit

IRIS Interactive Runfile InSpection

ISA Industrial Standard Architecture

L1 Level One Trigger

LED Light Emitting Diode

LEP Large Electron Positron Collider

LEP_16 LED Pulser

LF Local File

LHC Large Hadron Collider

LHC-b Large Hadron Collider Beauty Experiment

LINAC LINear ACcelerator

LVDS Low Voltage Differential Signaling

MIP Minimum Ionizing Particle

MSGC Micro Strip Gas Chamber

MSSM Minimal Supersymmetric Standard Model

NIM Nuclear Instrument Module

PCB Printed Circuit Board

PSH Pulse Shape Height

PSRD Prototype Synchrotron Radiation Detector

PT Peak Time

QCD Quantum ChromoDynamics

QED Quantum ElectroDynamics

QTC Quality Test Centre

RAM Read Access Memory

RF Radio Frequency

RT Rise Time

Si Silicon

SM Standard Model

SMD Surface Mounted Device

SRDEPPPC Synchrotron Radiation Detector Enhanced Parallel Port PC

SRDPC Synchrotron Radiation Detector PC

SUSY Super SYmmetry

TCP Transmission Control Protocol

TEC Tracker End Cap

TIB Tracker Inner Barrel

TID Tracker Inner Disk

TO Time Offset

TOB Tracker Outer Barrel

TPLL Tracker Phase-Locked Loop

UA1 Underground Area 1

UDP Users Datagram Protocol

XML Extensible Markup Language

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*“Wer über sich hinauswachsen will,
muss gut verwurzelt sein.”
(Gerhard Uhlenbruck)*

Lebenslauf

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