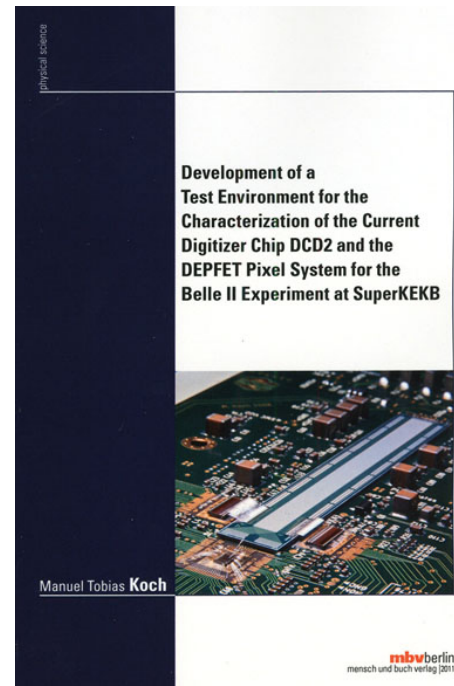


DEVELOPMENT OF A TEST ENVIRONMENT FOR
THE CHARACTERIZATION OF THE CURRENT DIGITIZER CHIP DCD2
AND THE DEPFET PIXEL SYSTEM
FOR THE BELLE II EXPERIMENT AT SUPERKEKB

MANUEL KOCH

September 2011

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DEVELOPMENT OF A TEST ENVIRONMENT FOR
THE CHARACTERIZATION OF THE CURRENT DIGITIZER CHIP DCD₂
AND THE DEPFET PIXEL SYSTEM
FOR THE BELLE II EXPERIMENT AT SUPERKEKB

Dissertation

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ABSTRACT

The future super flavor factory SuperKEKB with its detector system Belle II offers precision physics measurements to verify the Standard Model or probe undiscovered phenomena beyond its limits. A two layer vertex pixel detector is built based on the DEPFET technology. The Depleted Field Effect Transistor (DEPFET) pixel structure is an advanced type of silicon semiconductor detector, which provides simultaneously position sensitive detector capabilities and internal amplification. Fast and low noise readout of large area DEPFET sensors with row rates of 10 MHz is required. A new readout chip, the Drain Current Digitizer (DCD2), is available, which allows parallel readout of multiple channels with on-chip signal digitization. For the full characterization of this ASIC a FPGA based readout system has been designed, which also allows the operation of a prototype system including a DEPFET sensor. In this thesis, detailed measurements of the standalone performance of the DCD2 and the full system are presented; a limit on the possible readout speed of a large DEPFET sensor is established, and a switch from the slower double sampling readout scheme to a faster single sampling scheme is motivated.

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ACRONYMS

ADC	analog-to-digital converter
ADU	analog-digital unit $\equiv$ LSB
ASIC	application-specific integrated circuit
CCCG	capacitive-coupled cleargate
CCD	charge-coupled device
CDS	correlated double sampling
CMOS	complementary metal-oxide-semiconductor
DAC	digital-to-analog converter
DCD2	Drain Current Digitizer (second prototype version)
DCD-B	Drain Current Digitizer for Belle II (third prototype version)
DEPFET	Depleted Field Effect Transistor
DHP	Data Handling Processor
DNL	differential nonlinearity
D-SUB	D-subminiature, type of connector
DUT	device under test
ENC	equivalent noise charge
FPGA	field-programmable gate array
IEEE	Institute of Electrical and Electronics Engineers
I ² C	Inter-Integrated Circuit bus
ILC	international linear collider
INL	integral nonlinearity
JTAG	IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture

LSB	least significant bit $\equiv$ ADU
MOSFET	metal-oxide-semiconductor field-effect transistor
MSB	most significant bit
OCP	over-current-protection
OVP	over-voltage-protection
PCB	printed circuit board
PDN	power distribution network
PXD5	DEPFET pixel sensor production, batch 5, 2006
PXD6	DEPFET pixel sensor production, batch 6, 2010–11
RBR	redundant binary representation
RMS	root mean square
RSD	redundant signed digit
SMA	SubMiniature version A, type of connector
TLU	trigger logic unit
UMC	United Microelectronics Corporation, semiconductor company
USB	Universal Serial Bus, communication standard for peripheral devices

INTRODUCTION

Over 2500 years ago philosophers and scholars began to build a model of the smallest constituents of matter, which probably started the modern age of science as we know it. Since then, scientists set out to find and answer the deepest and most fundamental questions of nature. What are the fundamental forces? What is the fate of the universe, how was it created? What is the origin of mass and matter? Based on these and many more questions, a never ending story of success and discoveries in the natural sciences started. Today, particle physics is one of the disciplines making an important contribution to solving the mysteries of the universe.

In the beginning of the twenty-first century scientists base their research on the well-established Standard Model of particle physics. This model lists the fundamental particles that have been found so far: the three families of quarks and leptons, and the four bosons responsible for the fundamental forces of nature. Even more, the ingredients of the Standard Model — quantum electrodynamics, quantum chromodynamics and the electroweak theory — precisely describe the interactions of all the particles. It also requires the existence of the yet undiscovered “God particle”, the Higgs boson, which is required to give all other particles mass.

Driven by the hope of new discoveries, scientists keep pushing the limits. On the one hand, discovery machines are built, like the Large Hadron Collider at CERN. In proton-proton collisions with a center-of-mass energy of up to 14 TeV new particles are produced, hopefully including the Higgs boson.

On the other hand, one tries to increase the understanding of existing measurements at lower energies with high statistics, to further constrain the parameters of the Standard Model, and to find unexpected phenomena beyond its predictions. This frontier of precision and rare decay physics has been enabled through the study of B meson systems at asymmetric positron/electron (e^+/e^-) colliders, running primarily at a center-of-mass energy of the $\Upsilon(4S)$ resonance with 10.58 GeV, e. g. the experiments BaBar[14] at the PEP-II collider and the Belle detector[1] at the KEKB collider[60].

The Belle detector ceased its successful operation for over a decade in 2010. Experimental results provided insight into the flavor structure of elementary particles, and established the CKM model of quark mixing and CP violation[51]. With their rich decay spectrum, B mesons further open the opportunity for many interesting measurements[2–5, 7, 8, 15, 22, 23, 43, 62, 95, 106, 110]. Flavor factories have also the potential to discover new physics beyond the Standard Model, if measurements show discrepancies to the theory. This requires however a significant increase in collected data volume, which cannot be accomplished in reasonable time with the existing experiments.

A next generation collider, the super flavor factory SuperKEKB, will go into operation at KEK in the late 2010's. This asymmetric e^+/e^- accelerator operates with energies of 4 GeV/7 GeV per beam, and beam currents of 3.6 A/2.6 A; the instantaneous luminosity of $8 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$ is about a factor 40 higher compared to the previous machine KEKB. A new detector, Belle II as an upgrade of Belle, is required to deal with the increased interaction rates and higher background processes.

The Belle II detector[6, 27] is a hermetic detector system which allows the reconstruction of particle tracks after a collision, and performs the measurement of energy, momentum and charge of the produced particles. Track reconstruction requires detectors placed closely to the interaction point, which can deal with a high track multiplicity, perform well in an environment with high radiation levels, and offer an intrinsic position resolution in the order of a few micrometers. Additionally, by keeping the material budget of the vertex detectors very low, Coulomb scattering of the particles at the detector planes and thus a degradation of the track reconstruction has to be kept to a minimum. A new addition to the Belle II detector suited for this is a two layer silicon pixel detector based on the DEPFET technology.

The Depleted Field Effect Transistor (DEPFET) is an advanced semiconductor detector which integrates the first amplification stage directly into the pixelated sensor material by the use of a FET, resulting in a significant signal-to-noise advantage. Thin ($75 \mu\text{m}$), large area all-silicon modules with $\approx 50 \mu\text{m} \times 75 \mu\text{m}$ pixels will be produced for the Belle II pixel detector. At the edges of the DEPFET detector modules, outside of the acceptance region where the material budget can be higher and effective active cooling is possible, dedicated readout and steering ASICs are located. The DEPFET sensors are integrating devices, which require a continuous, un-triggered, full-analog and full-frame readout; zero-suppression and hit selection is performed in the ASICs and signal processing chain.

To keep the hit occupancy low, short frame times are preferred. In the scope of this thesis a limit on the possible readout speed for large scale DEPFET devices could be established for the first time by measurements. A FPGA based readout system was designed, for the full characterization of a new readout ASIC, the DCD2, and for dedicated operation of a newly designed prototype system including said ASIC and a DEPFET sensor.

In this thesis, the DEPFET technology is introduced in the first chapter, followed by an overview of the Belle II DEPFET sensor modules. The third chapter introduces the hardware design efforts necessary for this thesis. In chapter four, the DCD2 readout chip is described, which is followed by dedicated measurements in the next chapter. The fifth chapter shows all measurements which include a DEPFET sensor, here the readout time limits are established, source measurements are presented and a limit on the digital signal resolution is discussed.

The Depleted Field Effect Transistor (DEPFET) pixel structure (see [Figure 2](#)) is an advanced type of silicon semiconductor detector, which provides simultaneously position sensitive detector capabilities and internal amplification. A p -channel metal-oxide-semiconductor field-effect transistor (MOSFET) structure is combined with a high-resistivity, n -type substrate. Using a principle called sideways depletion, the bulk can be fully depleted. A potential minimum for electrons is created by an additional n -implant underneath the transistor channel and called internal gate. Signal charge generated by absorbed ionizing radiation is separated

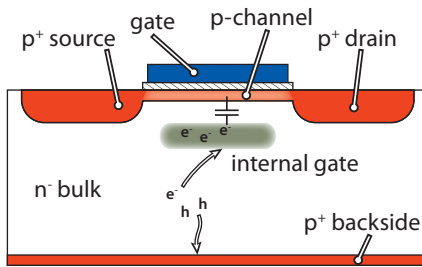


Figure 2: The DEPFET structure is based on a p -channel MOSFET on a fully depleted bulk. Signal charge is collected in the internal gate and modulates the transistor current.

by the electric field in the active volume. While holes drift to the backside p^+ -contact, electrons are transported to and stored in the internal gate. The collected charge changes the potential of the internal gate, and further influences mirror charges in the transistor channel. As a result, the channel current is modulated, and the collected signal charge can be externally measured. A special clear process is introduced which removes charge from the internal gate to allow continuous detector operation.

The DEPFET principle has first been proposed by Kemmer and Lutz [47] in 1987, and was experimentally confirmed in 1990 [48].

2.1 DEPFET OPERATION

The DEPFET operation can be separated into three stages which will be described in the following sections. First, the charge collection principle based on sideways depletion and the internal gate is reviewed; secondly, the readout of a DEPFET is presented including the electrical properties; and last, the clear process is explained. An equivalent circuit of the DEPFET, the choice of optimal operating voltages, and further details are outlined in the closing section.

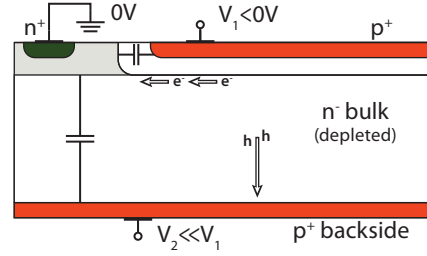
2.1.1 Charge collection

2.1.1.1 Sideways depletion and vertical potential minimum

The DEPFET substrate is a double diode structure that shares many similarities with semiconductor drift chambers [35, 36]. On both sides of a

n -type silicon wafer p^+ -implants form diodes. A n^+ -substrate contact is placed somewhere outside of the active area, typically close to the detector edge for simplified connectivity. Reverse biasing of the diodes is achieved by applying appropriate voltages to all contacts (bulk, back- and frontside; illustrated in Figure 3). At small voltages two independent space charge regions form around the p^+ -contacts leaving a part of the conducting bulk undepleted in between. With increasing voltage the depletion regions touch each other and form a potential minimum for majority carriers (electrons in the case of a n -type bulk). By applying different voltages to the surface contacts the position of this potential minimum can be moved vertically. This depletion method is called *sideways depletion*¹. Compared to a typical n - p -structure full depletion can be achieved at lower biasing voltage and with less detector capacitance. It is important

Figure 3: Sideways depletion at full asymmetric biasing. The depletion regions from front- and backside just touch each other, forming a potential minimum close to the top.



to note that electrons in the potential minimum will move slowly to the n^+ -contact by means of diffusion whereas the minority carriers (holes) can drift fast in the electric field to the back or front side contact. At this point it is possible to structure the front or back contacts and introduce an additional electric field component by applying a voltage gradient — this has led to the invention of the semiconductor drift detector.

For DEPFET structures the front side p^+ -implants are formed by the source and drain regions of a MOSFET, whereas the source is on higher potential. The vertical potential minimum is pinned to a position directly underneath the surface by applying asymmetric voltages and by using an additional n -type doping close to the surface.

2.1.1.2 Internal gate and local potential minimum

To provide a local potential minimum for electrons an extra n -type doping is added, directly underneath² the external gate of the MOSFET. This *internal gate* has a relatively low doping concentration of $\approx 1 \times 10^{16} \text{ cm}^{-3}$ [39] compared to the front side implantations. After depletion, the excessive free electrons of this area are removed and a positive space charge remains — which is now highly attractive for electrons. The capacity of the internal gate of a typical³ DEPFET device has been measured by Schmieden [92] and is reported to be in the order of $\approx 58\,000 \text{ e}^-$.

During charge collection the DEPFET transistor is typically switched off. The floating potential region of the internal gate is then capacitively

¹ sometimes *sideways depletion*

² The position of the internal gate is illustrated in Figure 2, Figure 4 and Figure 11.

³ Device used: DEPFET PXD5 COCG L B, wafer S90, sensor I00; for applications in high energy physics (ILC); drawn dimensions of external gate $W \times L = 10.8 \mu\text{m} \times 6.4 \mu\text{m}$

coupled to the external gate. By changing the voltage of the external gate in the off-state ($V_{\text{gate, off}}$) the internal gate can be shifted to a more positive potential and thus be made more attractive for charge collection. (This does no longer hold during clear or readout, where the internal gate couples to the then existing hole channel of the transistor, resulting in a lower, less attractive, potential.)

The DEPFET is a highly dynamic device; the internal gate forms only a potential minimum if it is repeatedly cleared. Even without the presence of ionizing radiation, the internal gate quickly fills up due to leakage current (in ≈ 100 ms at room temperature, cf. [92]), preventing further charge collection. Sideways depletion is a good concept to understand a static state of the DEPFET, however it will not restore the internal gate to a charge collecting state. The *depletedness* of the internal gate is a dynamic result of the clear process.

2.1.2 Readout

To quantify the collected charge the DEPFET needs to be read out. The external gate is switched on; electrons in the internal gate influence a mirror charge in the channel of the MOSFET, with a similar effect like a voltage change on the external gate. The DEPFET is typically used in the *integration and sample mode*⁴ suitable for imaging devices.

2.1.2.1 Drain or source based readout

The DEPFET can be read out in two different configurations, depending on the terminal which is connected to the readout chip (or discrete amplifier). In a *source follower configuration*, a current is forced through the DEPFET transistor using an external current source, the drain is connected to ground. The voltage change at the source can then be measured. This configuration has severe speed limits influenced by the load capacitance of the source line C_L , since this capacitance has to be charged or discharged to the final measured voltage. The risetime t_r can be calculated (small signal model of a source follower, [see 72]):

$$t_r = 2.2 \frac{1}{g_m} \left(C_L \left(1 + \frac{C_{gs}}{C_{gd}} \right) + C_{gs} \right) \quad (2.1)$$

The settling time can reach several μs which makes the source follower configuration unsuited for a high speed readout as required for the Belle II DEPFET pixel detector, where a readout time for a single DEPFET pixel of ≈ 100 ns is required.

In a *drain based readout* a current has to be measured. The voltage of the common drain line can be held constant by the readout chip, therefore

⁴ *Integration and sample mode*: During charge collection (integration) the external gate is turned off, and only turned on for readout. Allows multiple DEPFET transistors to be connected to the same readout bus.

A *real time mode* as described by Lutz [64] is also possible, where the DEPFET is continuously conducting (always turned on). Applications are drift detectors or CCDs.

the speed does ideally not depend on the load capacitance C_L . As a disadvantage, drain based readout is more sensitive to irradiation damage⁵ or process variations, which causes changing pedestal (i. e. baseline without signal) currents. (cf. thoughts on pedestal variations in [Section 7.6](#)).

2.1.2.2 Electrical characteristics

The internal amplification g_q of the DEPFET — the figure of merit so to speak — is expressed in drain current I_d change per collected signal charge in the internal gate (typically pA/e⁻). To derive the current/voltage characteristics of the DEPFET, a model working with influenced mirror charges in the transistor channel can be assumed. A detailed derivation of the DEPFET characteristics can be found in the works of Klein [49], Lutz [63], and Rummel [89]; the results are briefly given here.

A charge q present in the internal gate is equivalent to a gate-source voltage change of $\partial V_{gs} = f \cdot \frac{\partial q}{C_{ox}}$, with a reduction factor f accounting for parasitic coupling of the internal gate to other regions. The drain current can be modeled⁶ as:

$$I_d = \frac{1}{2} \frac{W}{L} C'_{ox} \left(f \frac{q}{C_{ox}} + V_{gs} - V_{th} \right)^2$$

After calculation of $g_m = \partial I_d / \partial V_{gs}$ and $g_q = \partial I_d / \partial q$, and substituting resulting terms, one finds the following scaling rules for a DEPFET device. The internal amplification g_q is proportional to the transconductance g_m :

$$g_q = \frac{g_m}{C_{ox}} \quad (2.5)$$

⁵ Radiation damage causes a threshold voltage V_{th} shift towards higher V_{gs} due to trapped charges in the gate oxide. In the source follower configuration, the threshold voltage shift leads to an equal shift of the source voltage. In drain based readout, the transistor characteristics change according to [Equation 2.2](#), either reducing I_d and g_q (see [Equation 2.8](#)), or requiring a readjustment of the gate source voltage V_{gs} .

⁶ The metal-oxide-semiconductor field-effect transistor (MOSFET) has become the most important device for integrated high density electric circuits since its invention in the 1960s. It is described extensively in literature, see for example Sze [96], Tsividis [103], and Lutz [63]. For the operation of a DEPFET device, which is working in the saturation region, the following relations are of relevance.

The drain current I_d and transconductance g_m of a p-channel device in the saturation region are given as:

$$I_d = -\frac{1}{2} \frac{W}{L} \mu_p C'_{ox} (V_{gs} - V_{th})^2 \quad (2.2)$$

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = -\frac{W}{L} \mu_p C'_{ox} (V_{gs} - V_{th}) \quad (2.3)$$

g_m can also be expressed as:

$$g_m = \sqrt{2 \mu_p C'_{ox} \frac{W}{L} I_d} \quad (2.4)$$

with the width and length of the gate W and L , the charge carrier mobility μ_p , the gate source voltage V_{gs} , the transistor threshold voltage V_{th} , and the sheet capacitance C'_{ox} . The gate capacitance can be calculated as $C_{ox} = C'_{ox} WL$.

With respect to the external gate length L and width W the the internal amplification g_q scales as:

$$g_q \Big|_{I_d, \text{const.}} \propto \frac{1}{L^{3/2}} \quad \text{and} \quad g_q \Big|_{I_d, \text{const.}} \propto \frac{1}{W^{1/2}} \quad (2.6)$$

A reduction of the oxide thickness t_{ox} (required to achieve radiation hardness [see 111, and references therein]) and therefore increasing of the oxide capacitance C_{ox} will reduce g_q with a square root dependence:

$$g_q \Big|_{I_d, \text{const.}} \propto \sqrt{t_{ox}} \quad (2.7)$$

The internal amplification also depends on the drain current. Changing the operating point of the DEPFET transistor using the gate voltage ($V_{\text{gate, on}}$ during on-state) is therefore the only practical way to influence g_q of a given device. Neglecting short channel effects, one finds:

$$g_q \Big|_{W, L, \text{const.}} \propto \sqrt{I_d} \quad (2.8)$$

2.1.3 Clear process

A clear process is introduced to remove the collected charge from the internal gate. This is realized by providing an additional terminal close to the internal gate, which can then perform a localized, on-demand depletion operation. The relevant structures and implants for the clear

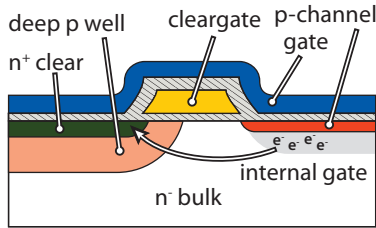


Figure 4: Relevant structures for the clear process. A high positive voltage is applied to the n^+ -clear contact; connection to the internal gate is made via punch-through assisted by the cleargate. The collected charge is completely removed.

process are illustrated in Figure 4 (which is a cut through Figure 11). The clear contact is a n^+ -implantation, self-aligned⁷ to the poly-silicon clear gate. Charge loss into the clear contact during signal integration is avoided by a shielding implantation: beneath the clear region a negative space charge is provided by a deep boron implantation, often called p -well or deep- p . This implantation gives rise to a potential barrier which has to be overcome during the clear process. During the clear process, a high positive potential is applied to the clear contact. Via punch-through [24, 58], the potential of the clear contact can reach through the shielding p -well. Underneath the cleargate⁸ a n -channel forms, which connects the

⁷ In a complementary metal-oxide-semiconductor (CMOS) process, *self-alignment* refers to a technique [20] where a polysilicon gate is used as a mask for the doping of surrounding implantation, thus preventing any misalignment.

⁸ There exists also an overlap of the deep p -well with the cleargate. With increasing overlap the potential barrier and the needed clear voltage rise. Devices with different p -well/cleargate overlap are present on the PXD5 production; a designator A (as in COCG SA) is used for 1.5 μm overlap, devices with designator E (as in COCG LE) feature 1.2 μm overlap.

internal gate with the clear contact. Now the collected charge electrons can flow to the clear contact, the internal gate is emptied. As a final step the clear potential is lowered again.

To avoid reset noise a complete clear process is beneficial, resulting in the same pedestal current I_{ped} after each clear process. Then the sampled signal value can be referred to a stored pedestal offline, or a direct correlated double sampling (CDS) in the analog domain is made possible. All electrons collected in the internal gate can be removed in ≈ 10 ns by using a clear voltage pulse of 14 V ($V_{\text{clear, high}} - V_{\text{clear, low}}$) as was shown by Sandow et al. [90].

2.1.3.1 Cleargate

A clear voltage reduction is possible by using the cleargate to lower the potential barrier between the internal gate and the clear contact, as shown in device simulations by Richter et al. [85]. The clear process can be improved by dynamically raising the cleargate voltage during the clear process. The cleargate can be clocked; or a capacitive coupling between the cleargate and clear contact can be implemented. This capacitive-coupled cleargate (CCCG) requires an explicit capacitance — e. g. visible in Figure 11. An operation with a static cleargate is also possible.⁹

One further use of the cleargate is technology¹⁰ specific. The cleargate, as the first poly-silicon layer, forms a lateral isolation frame around the MOSFET structure to suppress parasitic currents flowing from source to drain. Normal MOSFET processes would provide this isolation using oxide filled shallow trenches or local field oxide.

2.2 DETAILS

This section introduces further details of DEPFET devices. An equivalent circuit for a DEPFET device is given, optimal operating parameters are discussed, a typical readout sequence is shown, and the spectral performance is reviewed.

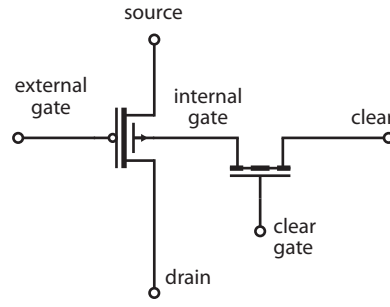
2.2.1 Equivalent circuit

The equivalent circuit for a single DEPFET transistor is illustrated in Figure 5. Parasitic elements, made up by the resistance of connecting lines and coupling capacitances, form RC-networks that exhibit low pass characteristics. Capacitive coupling leads to unintended charge injections, especially when operating with high (≈ 10 V) switching voltages. All these

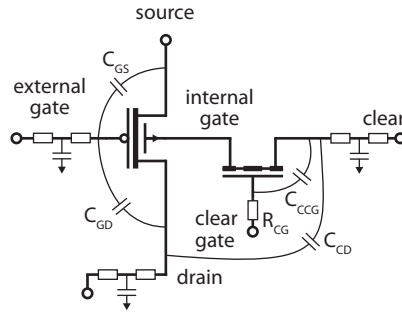
⁹ The devices used in this thesis work with a static, or common, cleargate. This is reflected in the designation of the device, e. g. COCGLE where COCG stands for common cleargate.

¹⁰ The DEPFET is produced at the *Halbleiterlabor, Max-Planck-Institut, München*. The technology available is based on direct writing laser photolithography and conventional proximity exposure, which allows the implementation of wafer scale sensors without the need for photoretic stitching. A minimum feature size of ≈ 2 μm can be implemented. Points differing from standard MOSFET processes can be found in the articles from Richter et al. [85] and Gärtner and Richter [39].

effects have an influence on the achievable readout speed as is shown in measurements in [Section 7.1](#) and [Section 7.3](#).



(a) DEPFET equivalent circuit...



(b) ...including parasitics.

Figure 5: A single DEPFET equivalent circuit. Relevant parasitics include the gate-drain capacitance C_{GD} , the gate-source capacitance C_{GS} , and the clear-drain capacitance C_{CD} . The low pass characteristics on the gate, clear, and drain lines are due to distributed RC, and indicated in the schematic with a small RCR combination. If a device with a capacitive-coupled cleargate (CCCG) is used, the coupling capacitance C_{ccg} and the resistor R_{cg} are implemented intentionally.

2.2.2 Optimal operating region — choice of voltages

The DEPFET is supplied with several voltages, typically referred to the source of the transistor. The bulk contact is supplied with a voltage V_{bulk} (≈ 10 V higher than V_{source}), to prevent any pn -junctions from being forward biased. The gate voltages $V_{\text{gate, on}}$ and $V_{\text{gate, off}}$ have an influence on the charge collection and internal amplification, as discussed in [Section 2.1.1.2](#) and [Equation 2.8](#). Remaining are the cleargate voltage V_{cg} , and the clear voltages $V_{\text{clear, low}}$ and $V_{\text{clear, high}}$, which determine largely the optimal operating conditions of a DEPFET device.

With a parametric scan over these voltages and by measuring the signal, e. g. produced by a radioactive source, an optimization to maximize the signal (or better: signal-to-noise ratio) can be performed; such a measurement is shown in [Figure 6](#). The limiting ranges for $V_{\text{clear, low}}$ and V_{cg} are given by the following effects [39]:

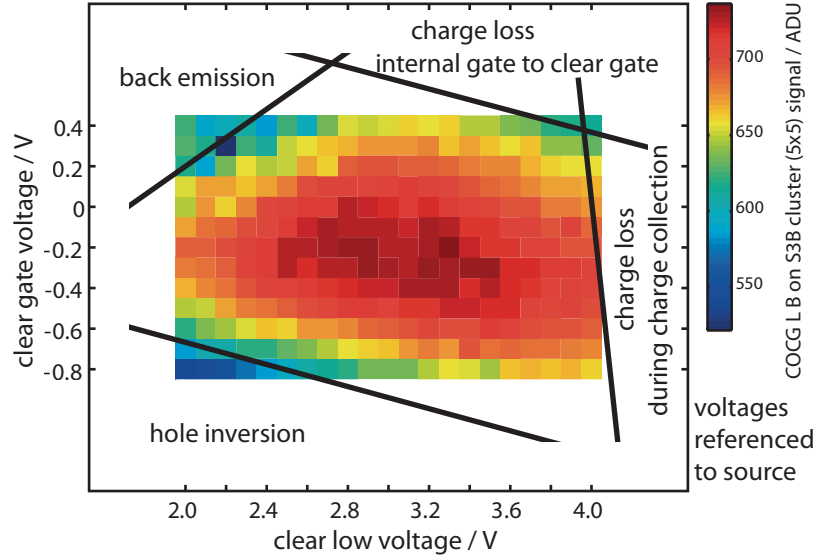


Figure 6: Determination of optimal operating voltages for a DEPFET device. A parametric scan over $V_{\text{clear,low}}$ and V_{cg} is performed, while measuring the signal of a radioactive source [provided by 29].

BACK EMISSION: If the clear low voltage $V_{\text{clear,low}}$ is chosen too negative, back emission of electrons from the clear implantation to the internal gate will occur.

HOLE INVERSION: The cleargate voltage V_{cg} has to be chosen positive enough to suppress a parasitic hole channel in the insulation structure along the cleargate. This can lead to the development of shorts between source and drain, or between source and the deep p -well.

CHARGE LOSS: If the clear low voltage $V_{\text{clear,low}}$ is chosen too high, the clear contact becomes attractive for signal charge during the charge collection — charge is lost. A similar process can develop when V_{cg} is chosen too high; charge then accumulates underneath the cleargate region leading to very long (μs) charge collection times.

The voltages used for DEPFET devices in this thesis are given in [Figure 40](#) on [page 51](#).

2.2.3 Readout sequence

Reading out a single or a larger array of DEPFET pixels requires sequencing of the control signals (i. e. steering voltages for gate and clear) and the definition of a sampling point for the drain current I_d . Various readout concepts were studied before in detail by Fischer et al. [31] and Lutz [64], a more recent summary can be found from Rummel [89, chap. 18]. Excluding special cases, two (rather canonical) readout sequences are favored which differ primarily in the number of samples taken.

SINGLE SAMPLING The drain current I_d is measured once after each integration period, before the clear process. The measured current

then equals the sum of the pedestal current I_{ped} , the signal current I_{sig} , leakage current¹¹ and a contribution from electronic noise.

$$I_d = I_{\text{ped}} + I_{\text{sig}}$$

To extract the signal value, the measured I_d is referenced to a stored pedestal value offline. Pedestal currents are individual to each DEPFET transistor (due to process, voltage, temperature, and irradiation variations), so an efficient storage and subtraction mechanism for pedestal values is obligatory.

DOUBLE SAMPLING After the clear process a second sample is taken, directly measuring I_{ped} ; the signal current I_{sig} can then be extracted in the analog domain of the readout chip.

$$I_{\text{sig}} = (I_{\text{ped}} + I_{\text{sig}}) - I_{\text{ped}}$$

This readout mode is also called correlated double sampling (CDS). Additional features are the suppression of low frequency noise components¹², and the demands on the dynamic input range of the readout chip are reduced if the pedestal current subtraction is handled in the analog domain.

Both readout sequences are illustrated in [Figure 7](#). Double sampling is the standard method for readout due to its many advantages, and it is implemented as such on the previously available readout chip [101]. However, if fast row times are required, and the readout speed turns out to be a major issue, the feasibility of a sample-clear-sample sequence needs to be reevaluated.

2.2.4 Spectral performance and electronic noise

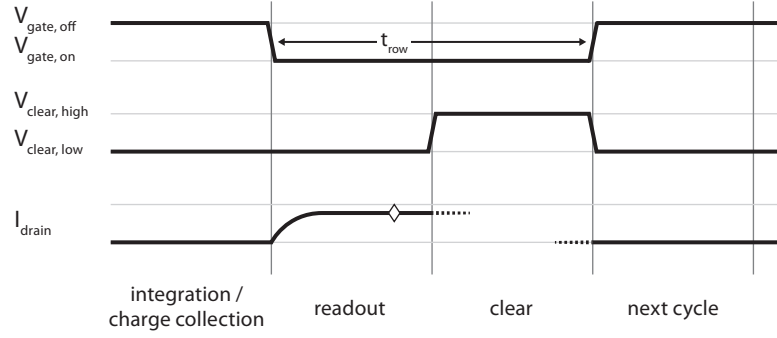
The DEPFET, as any other semiconductor detector, is affected by electronic noise [see standard literature, e. g. 63, 87, 94, 96]. Electronic noise is usually given as input referred noise, and expressed by the equivalent noise charge (ENC) in e^- . The overall intrinsic noise of a DEPFET pixel with high bandwidth readout (50 MHz) was demonstrated to be better than 50 e^- by Rummel [89], with white noise being the dominant contribution.

In an environment where the readout chips present the dominant noise source, the noise from the DEPFET can be safely ignored since uncorrelated noise contributions add in quadrature. For a target total noise of 200 e^- , as stated in the Belle II Technical Design Report[27], the contribution of the DEPFET is merely $\left(\frac{50}{200}\right)^2 \approx 6.3\%$.

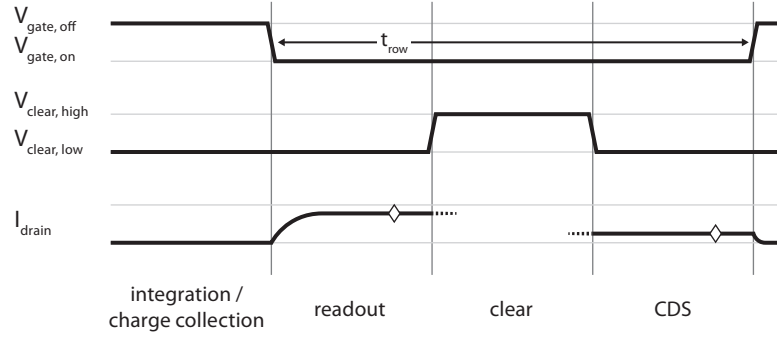
If a low bandwidth readout of the DEPFET is possible (shaping times $\approx 10 \mu\text{s}$) in a specific application, the total noise of the device can be reduced to a few e^- , yielding a remarkable spectroscopic performance. This

¹¹ The *leakage current* (excluding its shot noise) will present itself as a contribution to the pedestal, as long as the integration time is constant and there are no fast temperature or biasing changes.

¹² *Low frequency noise components* not only include contributions from the DEPFET, but also from the surrounding system, e. g. power supplies.



(a) Single sampling



(b) Double sampling

Figure 7: Illustration of DEPFET readout sequences for single (a) and double (b) sampling. For the drain current I_d sampling points are indicated by $\diamond$. During the clear process the drain current is dominated by parasitic coupling effects and not shown here. The sequence of events is:

INTEGRATION: The external gate is switched off ($V_{\text{gate, off}}$). Charge is collected in the internal gate, the device consumes no power, no drain current is flowing.

READOUT: The external gate is switched on ($V_{\text{gate, on}}$), drain current starts to flow. After settling of the current, the readout chip takes one sample.

CLEAR: The clear process is performed ($V_{\text{clear, high}}$).

OPTIONAL CDS: A second sample can be taken after the clear process.

NEXT CYCLE: The device is switched off again. Typically the readout of the next pixel row would take place now.

has been studied in multiple measurements, e. g. with different filtering techniques by Porro et al. [81], or single devices by Andricek et al. [10] (see Figure 8), Lutz [64], Ulrici et al. [105] and Treis et al. [100]. Measurements with ^{55}Fe at 5.9 keV using either a source follower configuration or drain based readout give a spectral resolution in the range of 130 eV to 150 eV with a noise peak of 2.2 e^- to 4.8 e^- .

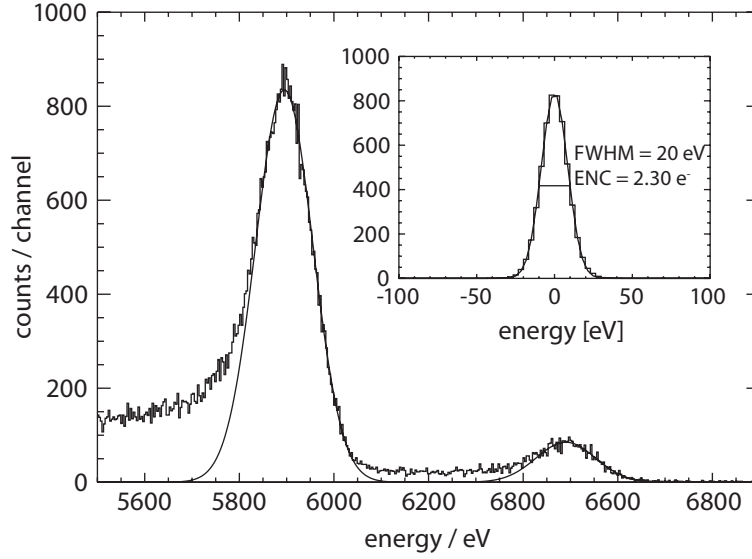


Figure 8: Measurement from [10, fig. 5]. ^{55}Fe spectrum taken with a linear DEPFET, gate $W \times L = 25\text{ }\mu\text{m} \times 7\text{ }\mu\text{m}$, in drain current readout at room temperature with a shaping time of $6\text{ }\mu\text{s}$. The noise peak is measured to an $\text{ENC}(\text{rms})$ of 2.3 e^- .

3.1 INTRODUCTION

SuperKEKB is a positron/electron collider specifically designed for the production of B mesons (B factory). The asymmetric e^+/e^- beam energies of 4 GeV/7 GeV correspond to a center-of-mass energy of the $\Upsilon(4S)$ resonance (10.58 GeV), which decays by strong interaction into B meson pairs ($\approx 50\% B^0\bar{B}^0$, $\approx 50\% B^+B^-$). The center-of-mass system moves in the direction of the electron beam, and the B mesons are boosted by this motion with a Lorentz boost factor $\beta = \frac{7-4}{10.58} = 0.283$. This boost is essential to provide a spatial separation of the two decay vertices of the B mesons. The decay time difference can be reconstructed, which allows the observation of time dependent CP -violating asymmetries [18, 50].

The Belle II detector follows an onion-like, hermetic design typical for collider experiments (see Figure 9). The innermost part of the detector

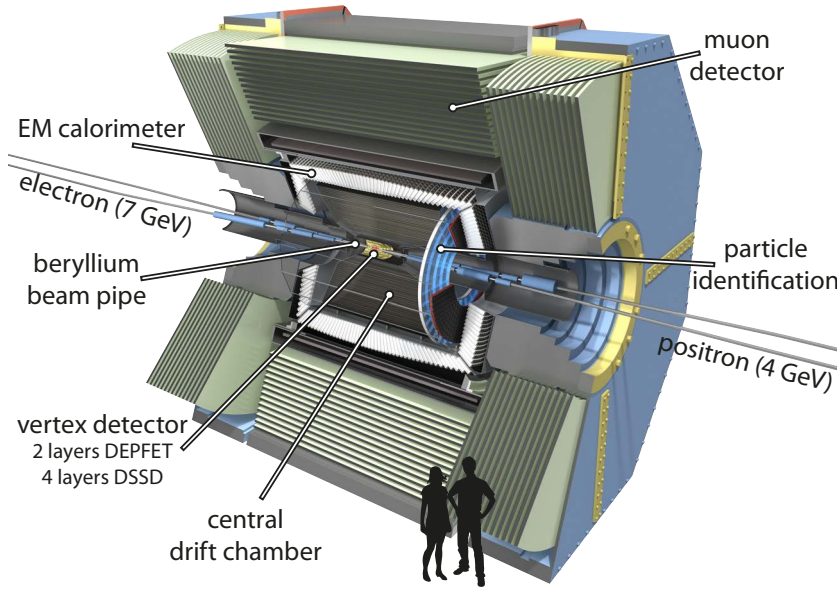


Figure 9: The Belle II detector. Picture from the Belle II Collaboration.

is the interaction region [27, ch. 3], where the e^+/e^- beams collide at a crossing angle of 83 mrad with beam currents of 3.6 A/2.6 A and an instantaneous luminosity of $8 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$. Directly outside of the beam pipe the vertex detector for track reconstruction is located, consisting of a two layer pixel detector[27, ch. 4] and a four layer silicon double-sided strip detector[27, ch. 5]. The following gas-filled central drift chamber (CDC)[27, ch. 6] reconstructs charged particle tracks and measures particle momenta, it provides particle identification by measuring energy loss in this gas volume, and it provides fast trigger signals for charged

particles. The CDC is surrounded by a particle identification system[27, ch. 7] consisting of an array of quartz bars. Here, the time-of-propagation of Cherenkov light created by charged particles is measured. The next detector layer is the electromagnetic calorimeter[27, ch. 9] made of CsI(Tl) crystals, which provides photon detection, photon energy measurement, and electron identification. The outermost detector layer is the muon detector[27, ch. 10], consisting of alternating iron plates and active detector elements.

The Belle II detector is an upgrade of the original Belle detector[1], and the addition of a two layer pixel detector close to the interaction region is one of the most important changes. The main task of the pixel detector is vertex reconstruction, and the figure of merit here is the *impact parameter resolution* σ_{d_0} (i. e. how good can a particle decay position close to the interaction region be reconstructed). The impact parameter resolution is the combined error of a geometric term and a Coulomb scattering term. The geometric term is the resulting error of a track-fit, and depends only on the position of the pixel layers (r_1 and r_2) and the intrinsic position resolution σ_{SP} of the detector itself. The Coulomb scattering term depends on the particle momenta p , the incident angle θ , and the detector radiation length $\frac{x}{X_0}$.

$$\sigma_{d_0} = \sqrt{\frac{r_2^2 + r_1^2}{(r_2 - r_1)^2}} \sigma_{\text{SP}} \oplus \frac{r_1 \cdot 13.6 \text{ MeV}}{p \sin^{\frac{3}{2}} \theta} \sqrt{\frac{x}{X_0}}$$

It can be seen that the best σ_{d_0} is achieved for spaced detector planes located as close as possible to the interaction point and for thin detectors. There are several points motivating the use of a thin pixel detector with high intrinsic position resolution:

- ♦ Compared to KEKB/Belle, the Lorentz boost of the center-of-mass-frame is reduced due to changed machine parameters from $\beta_{\text{KEKB}} = 0.425$ to $\beta_{\text{SuperKEKB}} = 0.283$. This reduces the flight distance $z = \beta\gamma c\tau$ of a particle with lifetime τ by one third, which requires an equal increase of vertex position resolution for the same experimental accuracy.
- ♦ The beam pipe radius is 10mm, two-thirds of that in KEKB, which allows the detector planes to move closer to the interaction point. However, the rate of background events increase roughly with the inverse square of the radius, causing higher hit occupancy [27, ch. 4]. To avoid ambiguities, a pixelated detector is preferred over strips.
- ♦ Low momentum particles suffer from excessive Coulomb scattering, which mandates a low material budget for the pixel detector ($\ll 100 \mu\text{m}$ of silicon thickness per layer).

3.2 THE DEPFET PIXEL DETECTOR

The DEPFET pixel detector for Belle II consists of two layers of DEPFET sensors, arranged in a cylindrical shape around the beam pipe. The inner

layer has 8 planar all-silicon sensors located at a radius of 14 mm, each module has a sensitive length of 90 mm and a width of 12.5 mm. The outer layer at a distance of 22 mm to the beam pipe is made out of 12 modules with a sensitive length of 124 mm and the same width as the inner modules. Modules are split in half¹ in the middle, thus a total of 40 half-modules are required. The modules are mounted and fixed by screws on an integrated metallic support and cooling structure. The layout of the pixel detector is shown in Figure 10. A detailed description of the joint efforts of the *DEPFET Collaboration* towards the design of the DEPFET pixel detector for Belle II can be found in the *Belle II Technical Design Report*[27] and the references therein.

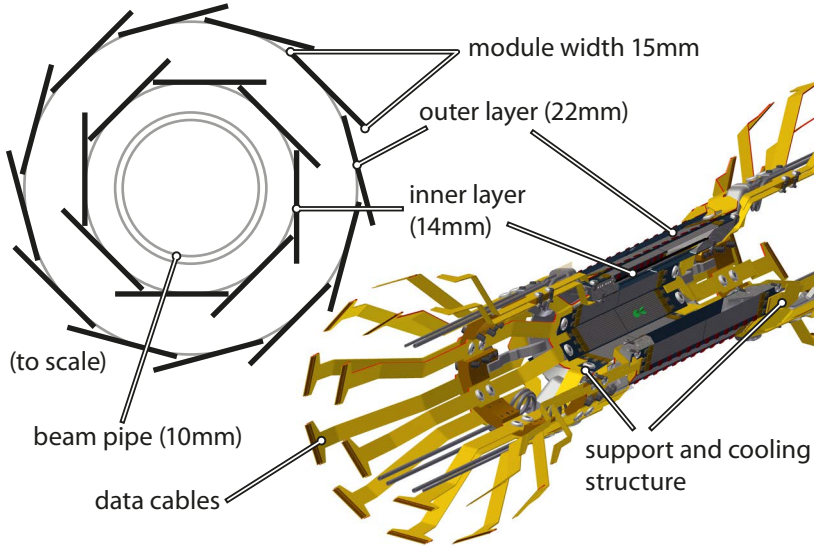


Figure 10: Schematic illustration of the Belle II DEPFET pixel detector, showing two layers of modules, and the mechanical support structure with cooling and electrical cabling.

3.3 MODULE LAYOUT

The DEPFET detectors for the Belle II pixel detector are all-silicon modules that combine an active area of DEPFET pixels, the readout and steering chips, and a landing area for a flexible interconnect cable. The module, along with some highlights on key areas, is illustrated in figure 11–16.

The pixel array (matrix) itself is made on 75 μm thin detector grade silicon, directly bonded on a thicker ($\approx 400 \mu\text{m}$) silicon handling wafer. Thinning is accomplished using deep anisotropic etching [9, 32], which opens windows in the supporting handling wafer. The active area is then completely exposed; in the frame around the module underneath the application-specific integrated circuits (ASICs) grooves are etched. These grooves allow a further material reduction by roughly 30 %, and additionally provide a rigid frame.

¹ Splitting the modules in half is necessary due to size limitations of the sensor wafers for production; it further increases the production yield and simplifies the assembly.

The readout ASICs, the Drain Current Digitizer for Belle II (DCD-B) and the Data Handling Processor (DHP), are placed at the end of the active area. There is 23 mm space left, outside the acceptance region, which will not contribute to the multiple Coulomb scattering material budget; proximity to the mechanical support structure makes active cooling of the ASICs possible. The SWITCHER chips, however, have to be placed on the long side of the active area on a thick, 2 mm wide balcony. For a compact module design all ASICs are flipped and connected via bump bonds. The DEPFET module is therefore equipped with an under-bump (copper) metalization, which makes the surface suitable for soldering.

The electrical interconnect to electronics outside of the detector is realized with a multi-layer polyimide flexible printed circuit board (PCB) (see Figure 15). This cable implements all power and ground connections, slow control, and impedance-controlled high-speed differential lines for data transmission. The connection to the DEPFET module can be made by a combination of glue, traditional wire bonds, and bump bonds.

3.4 DEPFET PIXELS FOR BELLE II

The development of DEPFET structures for the Belle II vertex detector is, due to similar requirements, based on previous experience in ILC type pixels [85]. The pixels themselves² are enlarged to $50\text{ }\mu\text{m} \times 58\text{ }\mu\text{m}$ for the inner and $50\text{ }\mu\text{m} \times 80\text{ }\mu\text{m}$ ($\varphi \times z$) for the outer detector layer. Even though multiple design and layout options are implemented in the PXD6 production, a baseline design for the DEPFET pixels has been chosen.

The DEPFET structure, as shown in Figure 11, has individual source and drain regions embedded in clear and drift implantations. The size of the active elements in a pixel is small compared to the pixel size, since the DEPFET transistor itself stays small. The transistor size is effectively given by the external gate length, which is favorably small for higher gain (cf. Equation 2.6), and for a fast clear process. Empty space³ between the pixels is filled with a shared clear contact and a p^+ -drift implant.

² A (realistic) note on the given geometries and sizes:

The length of the active area is given by the distance to the beam pipe and the polar angular acceptance range from 17° to 150° , which is defined by the silicon vertex tracker, the next detector at a radius of 38 mm. (The asymmetry of the angular acceptance accounts for the forward boost of the center-of-mass frame.)

The inner (outer) layer has an active area length of 44.80 mm (61.44 mm) for a half module. The pixel sizes are influenced by multiple constraints, foremost the physics requirements for position resolution define the overall size, while practical considerations influence the digits after the decimal point. Given a fourfold readout (see Figure 12) and the spacing constraints of the DEPFET technology, a pixel size of $50\text{ }\mu\text{m}$ in φ -direction naturally accommodates 4 parallel drain readout lines and supply lines for the source potential. For the z -direction, constraints are given by the achievable readout speed (and are a result of measurements done in this thesis), and the desire to use the SWITCHER chips efficiently. Using 6 SWITCHER chips with 32 channels each yields a total of $6 \times 32 \times 4 = 3 \times 2^8 = 768$ pixels with a z -length of $58.3\text{ }\mu\text{m}$ ($80\text{ }\mu\text{m}$). Further options are discussed to keep pixel coordinates on a $5\text{ }\mu\text{m}$ grid spacing; it is also possible to have different pixel sizes depending on the angular position (inner layer: $256 \times 55\text{ }\mu\text{m}$ and $512 \times 60\text{ }\mu\text{m}$, outer layer: $256 \times 70\text{ }\mu\text{m}$ and $512 \times 85\text{ }\mu\text{m}$).

³ The ILC pixels were tightly packed for the smallest pixel size possible with no empty space in between; pixels even featured a shared source to save additional space.

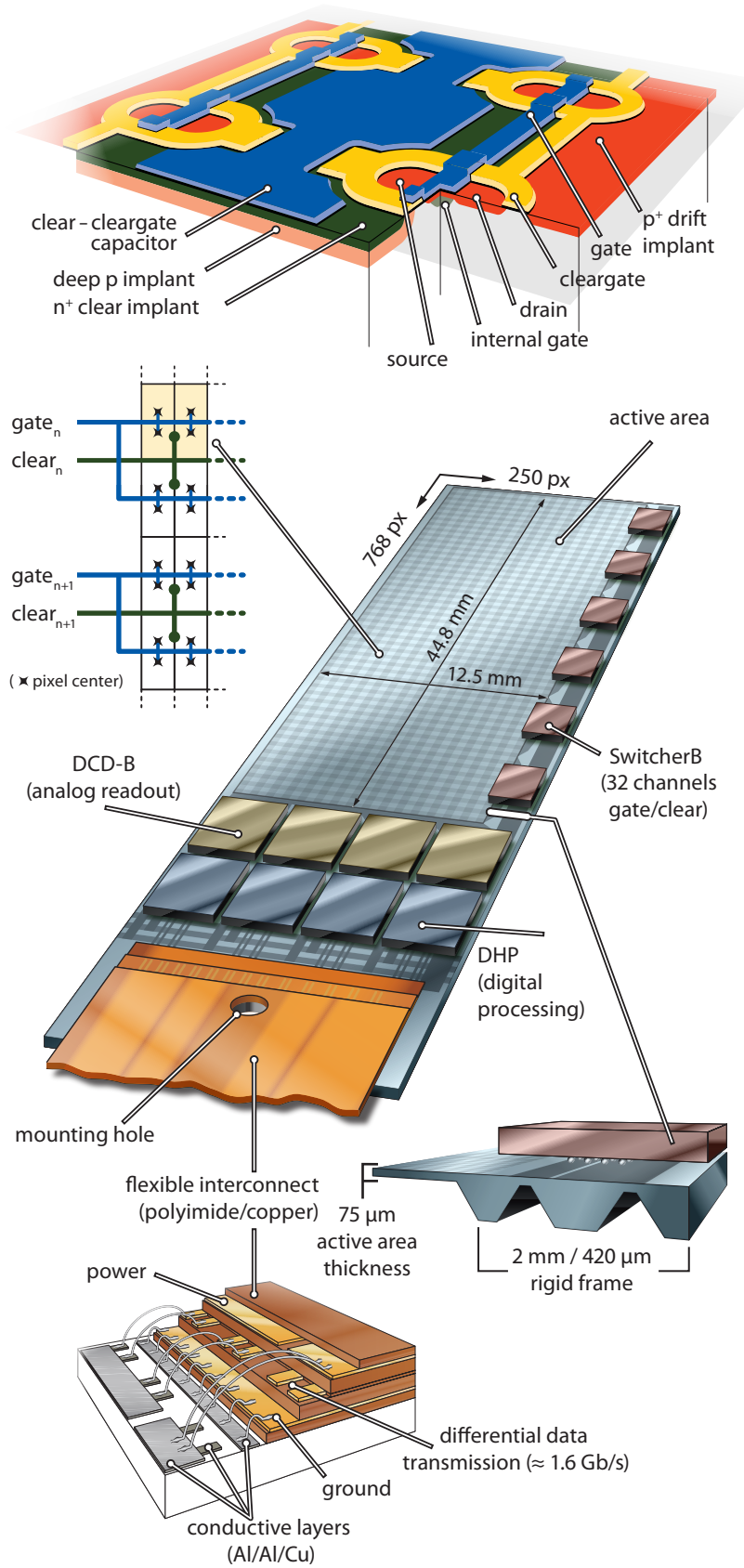


Figure 16: A DEPFET module for the Belle II pixel detector.

Figure 11:
DEPFET pixels for Belle II, layouted as single transistors with capacitive coupled clear gate (metal / contacts not shown), with a size of $50\text{ }\mu\text{m} \times 58\text{ }\mu\text{m}$ ($\phi \times z$) for the inner layer.

Figure 12:
To achieve a frame time of $20\text{ }\mu\text{s}$ a fourfold arrangement of pixels is chosen.

Figure 13:
A half-length all-silicon module combines on a total size of $15\text{ mm} \times 68\text{ mm}$ (inner layer) all readout and steering chips. The active area with 192×10^3 pixels is made on thin ($75\text{ }\mu\text{m}$) detector grade silicon. The power consumption is less than 9 W per half-module.

Figure 14:
For rigidity and bondability, all sections outside of the active region have a thickness of $420\text{ }\mu\text{m}$. Deep anisotropic etching is used to reduce the material in the supporting frame.

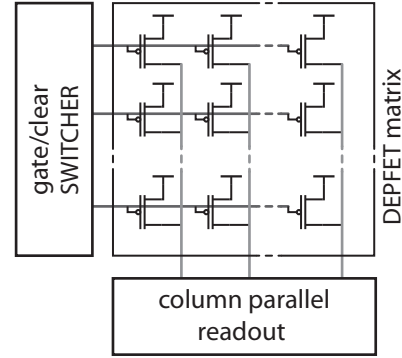
Figure 15:
A three layer flexible PCB facilitates all electrical connections.

This drift implant prevents the existence of areas with undefined surface potential, and thus avoids penalties in charge collection times. Advanced features, like a capacitive-coupled cleargate, can be implemented as well. The arrangement of individual pixels in a matrix is asymmetric. Every second DEPFET transistor is mirrored: the sources of individual pixels face each other, likewise do the drains. Additionally, the distance between the sources is kept short, while the drift region between the drains is allowed to expand, adjusting for the desired pixel size. This allows a simplified layout with less routing (and higher production yield), since now the clear contacts can be shared. Another reason is increased charge collection efficiency: The source is connected to the highest potential and is thus more attractive for signal charge. Signal electrons on their way to the internal gate are less impeded while drifting underneath the drain regions compared to the source regions. By pairing the sources of the transistors close together the drift fields within the sensor are further optimized.

3.5 READOUT CONCEPT

The DEPFET pixels are arranged in a matrix (see [Figure 17](#)) which is operated row wise, in the so called *rolling shutter mode*. One horizontal pixel row at a time is activated by a SWITCHER chip; the drain currents of all those pixels are then transmitted in parallel to the readout chip for further processing. This mode of operation not only allows the shared usage of the vertical drain lines for all pixels in the same column, it also keeps the power consumption⁴ of the sensor's active area to a minimum. The detailed operation of a DEPFET device is explained in [Section 2.1](#).

Figure 17: DEPFET matrix operated in rolling shutter mode. The SWITCHER steers the gate and clear of an array of DEPFET pixels, row by row. The current is read out column parallel using shared drain lines.



READOUT TIMING The most challenging aspect is the frame readout time of $20 \mu\text{s}$ ⁵, which would translate on a full module with 1536 pixels to a row time of only 13 ns. This timing is impossible to achieve (cf. measurements in [Section 7.1](#)) due to intrinsic settling times of the DEPFET sensor and the readout chips. The time constraint is however relaxed by splitting

⁴ A pixel consumes only power while being read out, not while integrating signal charge. The power consumption of the DEPFET active area for a half module is given by $N_{\text{pixels on}} \times V_{\text{ds}} \times I_{\text{d}}$, which amounts only to $1000 \times 5 \text{ V} \times \approx 100 \mu\text{A} = \approx 500 \text{ mW}$

⁵ The readout of the DEPFET pixel detector is synchronized to the operation of the SuperKEKB machine. The exact frame time is only approximately $20 \mu\text{s}$ and based on the RF frequency of 508.887 MHz and the revolution frequency of the beam.

the module in half, using readout chips at both sides, and implementing a high degree of parallelization by using a fourfold pixel arrangement (Figure 12). This results in a factor of eight gained in speed, translating to a row time of 104.2 ns (9.6 MHz). To gain additional time, the DEPFET typical sample-clear-sample (double sampling, see Section 2.2.3) readout operation has been abandoned in favor of the faster sample-clear (single sampling) sequence.

3.5.1 Readout electronics

Three distinct ASICs are needed to operate a DEPFET module. Steering of the gate and clear lines is accomplished by the SWITCHER chips. The drain currents of selected DEPFET pixels are digitized using the analog frontend chip DCD-B, while digital processing is handled by the DHP chip. These ASICs and their functionality will be briefly described in the following sections.

THE SWITCHER CHIP (described in [27, 80]) facilitates steering of the gate and clear lines of the DEPFET module by providing fast (10 ns rise time with ≈ 50 pF load capacitance) output signals up to 20 V. Six chips with 32 channels each are mounted on the 2 mm wide lateral frame of the DEPFET module. The operation is rather simple: DEPFET channels are selected via a shift register which can be daisy-chained to the next SWITCHER chip, this way individual control of all 6 chips is avoided. As a special feature, the output steering signals for the DEPFET gates can be operated in an overlapping mode which could improve settling times of the drain currents, (cf. Section 7.1.3.1). This ASIC is produced in the AMS HV 0.35 μ m technology using special design techniques for radiation hardness. The chip size is 2.1 mm $\times$ 3.6 mm, with a total of 96 bump-bondable input / output pads.

THE DCD-B CHIP digitizes incoming DEPFET drain currents. Current receivers (based either on transimpedance amplifiers or regulated cascodes) hold the drain line potentials constant, thus canceling the effect of the large drain line load capacitance (≈ 50 pF). Two current mode algorithmic analog-to-digital converters (ADCs) with eight bit resolution work interleaved in each of the 256 channels to digitize the currents. The output data is then transmitted to the DHP for further processing. The DCD-B chip, and its predecessor the DCD2, are described in Section 4.7 and Section 4, and in their corresponding documentation [27, 78, 79].

THE DHP CHIP is the digital backend ASIC for data storage and further digital processing. Its main task is to reduce the data provided by the DCD-B chip, using zero-suppression on the incoming data and only transmitting triggered data to the outputs. Efficient zero suppression requires an algorithmic preprocessing of the data: First, a common offset (mean value) is calculated and subtracted from the input values. This allows the suppression of low frequency noise components that are common to a whole DEPFET row. As a second step, the pedestal values individual to

each DEPFET pixel are subtracted; pedestal storage memory of equal size to the DEPFET matrix is required. As a last step, zero suppression is performed by discarding all data that falls below a selectable threshold. The DHP provides storage memory (hit buffers) for several full frames of data. Upon reception of a trigger signal, this data is transferred to the outside of the detector using high speed data links. On the DEPFET module one DHP chip acts as a master, controlling the timing of the SWITCHER outputs; furthermore, each DHP provides data to the DCD-B chips facilitating pedestal current compression in the analog domain (see [Section 7.6.2.1](#)). The current DHP prototype chips are implemented in a IBM 90 nm technology (and a future switch to a 65 nm technology is planned), which provides a high memory density per chip area.

THE DCD2 READOUT ASIC

The Drain Current Digitizer (DCD2) is a current-mode prototype chip for readout of DEPFET pixel sensors. It has been designed in 2007 by Perić et al. [76], and its stand-alone characterization and use in a DEPFET readout system is the focus of this thesis. The key features, building blocks (see also Figure 18) and operating principle of this ASIC are:

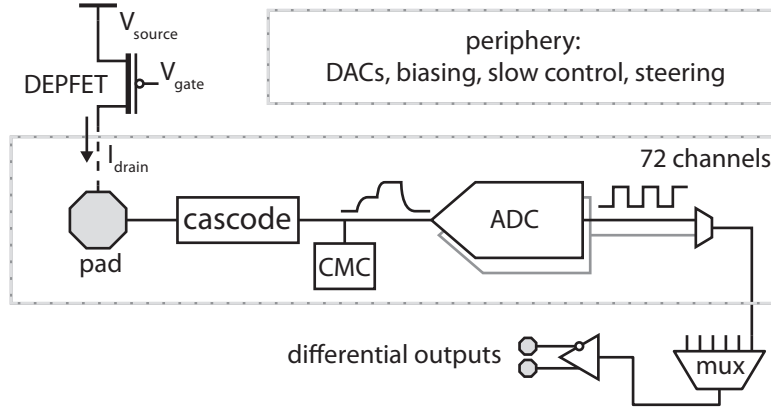


Figure 18: The Drain Current Digitizer (DCD2) prototype chip has 72 individual channels to receive the DEPFET drain current. Each channel has a regulated cascode to keep the input voltage constant, an additional current memory cell (CMC) for optional correlated double sampling (CDS) to subtract DEPFET pedestal currents and two current-mode ADCs with 8-bit resolution. The digital output codes of 6 channels are multiplexed and transmitted off-chip by high speed differential lines.

- ♦ 72 input channels are available, arranged as a 6×12 matrix on a total chip area of $\approx 1.5 \text{ mm} \times 3 \text{ mm}$, to digitize input currents coming either from a DEPFET transistor, an external precision current source, or internal test current sources.
- ♦ The potential of each DCD2 input channel is held constant by a *regulated cascode*, which cancels the effects of large input capacitances and speeds up the reception of currents.
- ♦ The current can optionally be fed into a presampling *current memory cell* that allows subtraction of a DEPFET pedestal current I_{ped} in a CDS sampling mode, leaving only the signal current I_{sig} to be digitized.
- ♦ A cyclic ADC digitizes I_{sig} with 8 bit resolution in a conversion time as fast as 160 ns.
- ♦ For increased conversion speed, two cyclic ADCs work interleaved in each channel.

- ♦ The data of six input channels is multiplexed and serialized, and transmitted off-chip using high speed differential links with up to 600 MHz. Thus one such link contains the data of twelve individual ADCs; there is a total of twelve high speed outputs on the chip.
- ♦ In order to provide high radiation tolerance, the chip has been implemented in a 180 nm CMOS technology using enclosed NMOS transistors [38] and novel radiation hard circuits [76].

The ADC, memory cells, and regulated cascode will be described in the following sections. A detailed description of the chip, including rather technical aspects of digital communication and configuration, can be found in [12, 76, 78].

4.1 ANALOG INPUT PATH

The analog input circuits are outlined in Figure 19. After the pad, which connects to the DEPFET sensor using wire bonds, several static and switchable current sources are present. Test signals can be produced on-chip using two current sources, *InjBias* for a pedestal current and *InjSignal* for a switchable, dynamic signal. The current flowing through the regulated cascode and a global current baseline adjustment is set with *MainOffset* and *MainSub*, two current sinks. A monitor bus is present on the chip, and allows a single, direct external connection to a selectable inspection point; signal injection or monitoring is possible either before or after the cascode in each pixel.

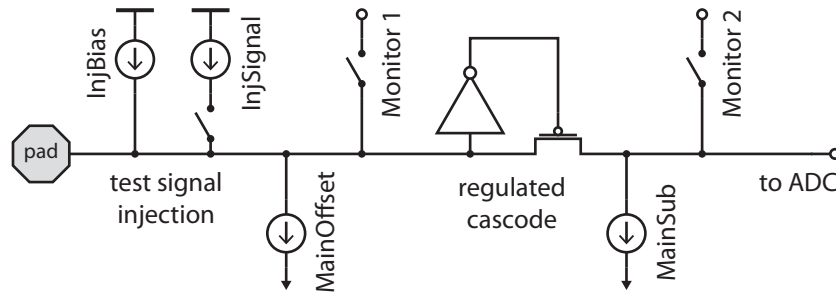


Figure 19: Schematic of the analog input stage of the DCD2. Test signals (or parametric current sweeps) can be produced by three static (*InjBias*, *MainOffset*, *MainSub*) and one switchable (*InjSignal*) current source. External connections are possible at two monitoring points. The block diagram of the ADC is given in Figure 24.

4.2 REGULATED CASCODE

The schematic of the regulated cascode and the biasing parameters are given in Figure 20. It is based on a folded cascode amplifier topology, using a NMOS input transistor with an additional power supply *VCAVSS*. The power consumption per pixel is ≈ 1.7 mW (cf. data in Figure 39 on page 50), influenced mainly by the biasing current *CascAmpBias*. The main

task of the cascode is to compensate for the DEPFET drain capacitance, where values of up to 50 pF are expected for large sensors. The cascode holds the input potential constant, thus preventing the charging and discharging of the parasitic input capacitance with the signal current, leading to improved readout speed. The settling time can be further adjusted with a feedback amplifier (CascAmpSF) between damped oscillation and over-damped behavior, see Figure 21. Settling time and noise measurements under various capacitive loads are presented in Section 6.2.

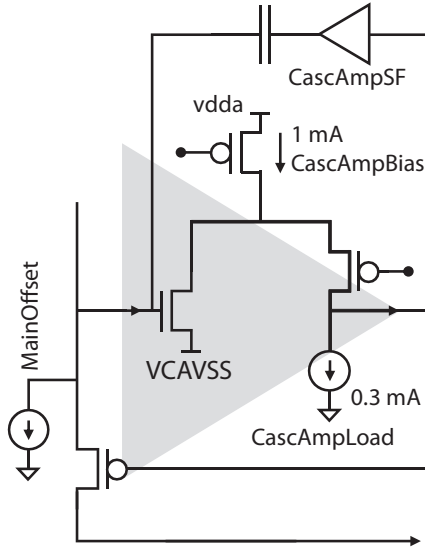


Figure 20: The DCD2 regulated cascode is implemented using a folded cascode topology amplifier. The main biasing of the amplifier is set with CascAmpBias and CascAmpLoad, while the input potential can be directly influenced by changing the amplifiers ground voltage VCAVSS. The cascode provides no additional signal gain and introduces no current offsets.

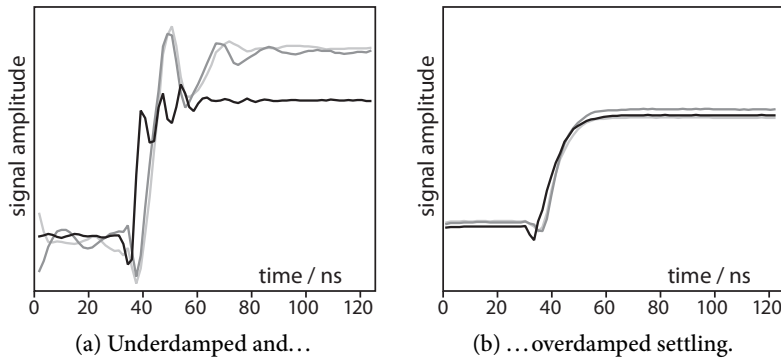


Figure 21: DCD2 cascode settling behavior as a response to a current step function at the input, measured with the DCD2 as described in Section 6.2.1.

(a) CascAmpSF = 0 (DAC units). Even though the response of the cascode is a sharp step, damped oscillations over ≈ 60 ns prevent settling. The channels for the gray curves have an additional input capacitance attached.

(b) With CascAmpSF = 250 (DAC units) oscillations are suppressed and settling is achieved in ≈ 20 ns.

4.3 CURRENT MEMORY CELLS

Current memory cells are analog memory elements that store and duplicate currents. In the DCD2 they are used as building blocks for the ADC and as a standalone element to provide optional double sampling. The

Figure 22: The DCD2 current memory cell [76] uses an amplifier and a trans-conductor to provide signal and voltage independent current storage capabilities. This design is a modified zero- (constant-) voltage switching memory cell based on [71].

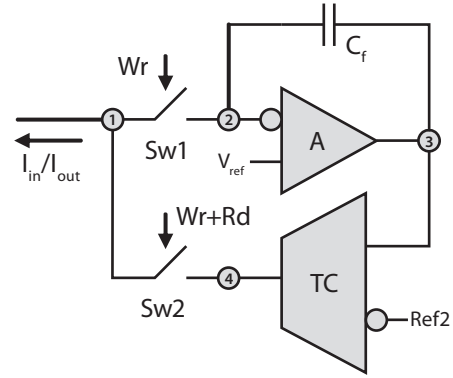
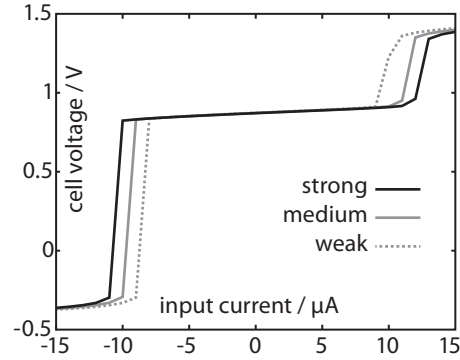


Figure 23: The transfer characteristics of the current memory cell has been measured as a function of the input current. Depending on the biasing of the cell, the current range where the input voltage stays constant ($= V_{ref}$) is up to $\pm 12 \mu A$.



design of the current memory cell is shown in Figure 22 [see 76, II.B]. The cell has a bidirectional input / output node ① for currents, the capacitor C_f is used as a memory element. The trans-conductor TC converts the voltage across C_f (at node ③) into a current, which then flows into node ④. An inverting amplifier A is used, which is for the following explanation assumed to be ideal.

IN WRITE STATE both switches Sw1 and Sw2 are conducting, and due to negative feedback the voltages at nodes ①, ② and ④ are equal to V_{ref} . Node ③ settles to a voltage that forces the transconductor to compensate the input current exactly, since no current can flow into the amplifier inputs or C_f .

IN READ STATE switch Sw1 is opened, the voltage across C_f is frozen, and the previously sampled current keeps flowing to node ④. If the current is fed to another cell of the same type, the voltage seen at node ① will again be V_{ref} , which avoids voltage dependent higher order effects of these cells. Over a wide range of input currents the memory cell input voltage remains constant, while the biasing of the active elements can be changed to adjust the total input range. A measurement for three different biasing settings is shown in Figure 23. Stored currents can also easily be duplicated by feeding the input voltage ③ of the trans-conductor to another, identical, trans-conductor outside of the memory cell.

4.4 CURRENT DIGITIZATION ADC

Digitization of DEPFET drain currents is performed directly in the DCD2 readout chip (hence the name). A cyclic (or algorithmic) ADC implementation has been chosen which is known to achieve high resolution within a small¹ silicon area [61]. The DCD2 ADC operates in current mode and is explained in detail in the corresponding paper by Perić et al. [76] and the thesis by Armbruster [12]. A short description, including the conversion algorithm and its benefits, will be presented here.

A simple approach to digitize a signal starts with the comparison of the input current with a reference current I_{ref} (threshold). If the current is higher than the reference, the most significant bit (MSB) is set to one and the reference current is subtracted from the input. Otherwise the MSB is set to zero and no subtraction is performed. The remainder (residue) is then multiplied by a factor of two and the whole process is repeated. This repetition can be performed by the same ADC stage in a cyclic fashion (resulting in a cyclic ADC), or in a serial, pipelined fashion using multiple, cascaded stages (resulting in a pipeline ADC).

The implementation on the DCD2 follows a slightly different approach, using redundant signed digit (RSD) cyclic conversion, which is based on the SRT division algorithm [86, 99]. Instead of one threshold two thresholds are used. This introduction of one extra decision level allows this ADC stage to resolve 1.5 bit of information². The extra half bit is used as redundancy and provides automatic error correction, making the ADC stage less sensitive to non-idealities like noisy comparator thresholds.

4.4.1 Realization of the cyclic ADC

The ADC consists of 4 current memory cells, two current mode comparators (each with two thresholds), and digital logic for redundant binary representation (RBR) decoding. The block diagram is shown in Figure 24. Two memory cells and one comparator work as a (cyclic) unit, which either performs a single operation consisting of comparison/subtraction/gain as in Equation 4.1a, or this unit operates as a receiver to store the result from the other one. The comparator is connected only to one of the two memory cells, which are additionally equipped with switchable current sources to perform the subtraction/addition of the reference current I_{ref} . The ADC operates with the following repeating steps, alternating between memory cell pairs 1,2 and 3,4:

STATE 1 The input signal³ is stored in memory cell 1.

¹ On a Belle II half-module 2048 individual ADCs have to be integrated on an area of $\approx 13 \text{ mm} \times 5 \text{ mm}$

² More precise, $\log_2(3) = 1.58 \text{ bit}$

³ The input signal, coming from the regulated cascode, is first stored in a single pre-sampling current memory cell (not shown in the block diagrams here), effectively pipelining the operation. This not only ensures that the current duplication in STATE 2 acts on the same input current (i. e. ensuring that $x + x = 2 \cdot x$), it also shortens the hold time of the input current by one clock cycle ($\frac{1}{8}$ times the row time)

STATE 2 A copy of the input signal is stored in cell 2. The comparator, connected to cell 1, performs the comparison.

STATE 3 Based on the comparison result in the previous steps current sources in cells 1 and 2 are activated to add/subtract I_{ref} . Both cells have now the same output current; adding these currents effectively performs a multiplication with 2 (stage gain).

STAGE 4 The sum of the output currents of cells 1 and 2 is stored in cell 3.

The comparator results of each step are stored in a shift register and further processed (see [Section 4.4.3](#)) to provide the final binary digitization result. The ADC performs 8 cyclic steps, resulting in 8 bit resolution. The conversion time for each cycle is ≈ 20 ns, leading to a total time of ≈ 160 ns. To meet the specifications for a high speed DEPFET sensor readout, which demand a row time of ≈ 100 ns, two identical ADCs work interleaved in parallel.

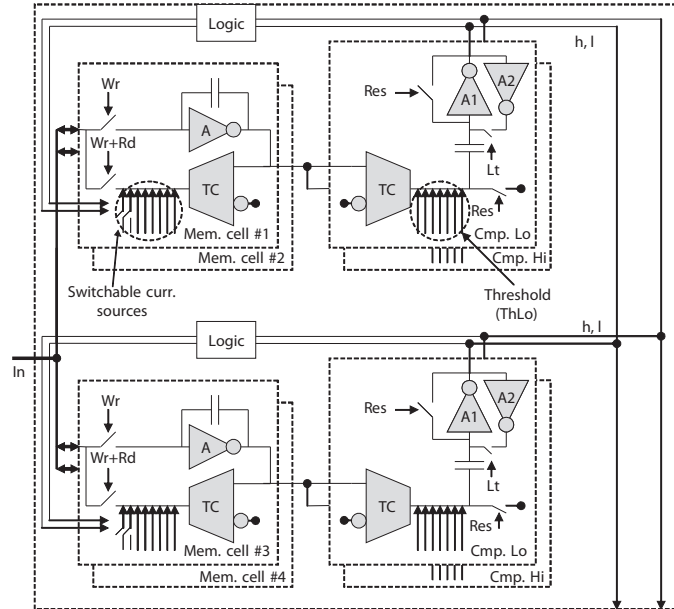


Figure 24: DCD2 ADC block diagram (from [76, 79]). The ADC has 2 units, consisting of 2 current memory cells (left) and one current mode comparator (right).

4.4.2 Conversion algorithm

The conversion principle is based on a recursive binary search algorithm [see 82, ch. 8] to approximate the analog input current:

$$I_{\text{out}_{i+1}} = 2 \left(I_{\text{in}_i} - d_i I_{\text{ref}} \right) \quad (4.1a)$$

$$\text{with} \quad I_{\text{in}_i} = \begin{cases} I_{\text{out}_i} & \forall i \neq 0 \\ I_{\text{input}} & i = 0 \end{cases} \quad (4.1b)$$

$$\text{and} \quad d_i = \begin{cases} 1 & I_{\text{in}_i} > +\frac{I_{\text{ref}}}{2} \\ 0 & -\frac{I_{\text{ref}}}{2} \leq I_{\text{in}_i} \leq +\frac{I_{\text{ref}}}{2} \\ -1 & -\frac{I_{\text{ref}}}{2} > I_{\text{in}_i} \end{cases} \quad (4.1c)$$

$$\text{for all} \quad i = 0, 1, \dots, N-1 \quad (4.1d)$$

The resolvable analog current input range⁴ is determined by I_{ref} , where $I_{\text{input}} \in [-2I_{\text{ref}}, +2I_{\text{ref}}]$. The output digits $d_i \in D = [-1, 0, 1]$ of the conversion process are given in redundant binary coding and are later mapped to a true binary representation (see [Section 4.4.3](#)).

The analog residue current after the i -th iteration is given by I_{out_i} . Solving the recursion [Equation 4.1a](#) for I_{input} gives:

$$I_{\text{input}} = \frac{I_{\text{out}_N}}{2^N} + \frac{2I_{\text{ref}}}{2^N} \prod_{k=0}^{N-1} 2^{N-1-k} d_k \quad (4.2)$$

The least significant bit (LSB) value is given by the full range and the quantization steps as $\text{LSB} = I_{\text{ref}} 2^{2-N}$. Since each residue current I_{out_i} lies within the input boundaries of the following stage, limits for the final quantization error $\text{Err}_{Q,N}$ can be found:

$$\text{Err}_{Q,N} \equiv \frac{I_{\text{out}_N}}{2^N} \in \left[-\frac{2I_{\text{ref}}}{2^N}, +\frac{2I_{\text{ref}}}{2^N} \right] \quad (4.3)$$

The operation of the ADC and the influence of errors can be explained with the help of a Robertson diagram [13, 41] in [Figure 25a](#). Here for one ADC stage the residue current I_{out} is plotted as a function of the input current I_{in} , normalized to I_{ref} . Comparator thresholds can be identified by the steps with a height of I_{ref} in the diagram.

The diagram is framed by a box of dimensions equal to the input range of the ADC stages, thus an out-of-range condition causing subsequent errors can easily be seen. Should the output (y-axis) exceed the input range of the next stage (x-axis), clipping will occur.

SAMPLING ERRORS AND THRESHOLD SHIFTS A constant sampling error in each ADC cycle has an impact on the conversion algorithm. Adding a constant sampling error dx to each conversion step leads to the following operation, modified from [Equation 4.1a](#):

$$I_{\text{out}_{i+1}} = 2 \left(I_{\text{in}_i} - d_i I_{\text{ref}} + \Delta x \right) \quad (4.4a)$$

⁴ In the case of the DCD2 ADC, the nominal value is $I_{\text{ref}} = 4 \mu\text{A}$ yielding a total range of $16 \mu\text{A}$. With biasing changes a total range of $24 \mu\text{A}$ is possible.

which yields after resolving the recursion:

$$I_{\text{input}} = \frac{I_{\text{out}N}}{2^N} + \frac{2I_{\text{ref}}}{2^N} \prod_{k=0}^{N-1} 2^{N-1-k} d_k + \frac{2^N - 1}{2^{N-1}} \Delta x \quad (4.4b)$$

$$\text{with} \quad \frac{2^N - 1}{2^{N-1}} \Delta x \approx 2\Delta x \quad (4.4c)$$

It can be seen that the total input range is shifted by $\approx 2\Delta x$ (see Figure 25b), which is uncritical for digitizing DEPFET drain currents, since varying pedestal currents of the device are expected to be much higher than $2\Delta x$.

Comparator threshold shifts are uncritical (see Figure 25c), as long as the thresholds are, respectively, between $[0, -I_{\text{ref}}]$ and $[0, +I_{\text{ref}}]$. Setting the thresholds at $\pm \frac{I_{\text{ref}}}{2}$ leaves the maximum margin for inaccuracy, thus allowing high levels of noise, offset and even hysteresis [37]. When threshold shifts and offset exceed this safety area, the residue current I_{out} after a conversion step will exceed the valid input range for the next stage. Consequently, the ADC characteristics then shows areas with wide codes or missing codes (see Figure 25d).

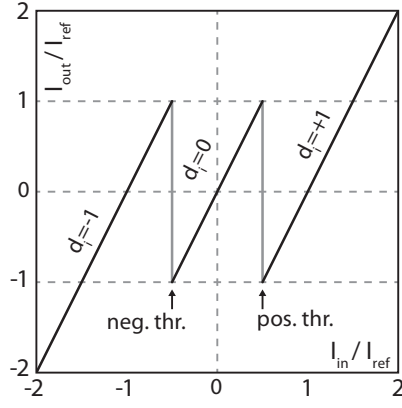
4.4.3 Redundant binary representation

Any number can be represented as a radix polynomial. Given an integer base or radix r , $r \geq 2$, and digits $d_i \in \mathbb{Z}$ which belong to some digit set D , then any (integer) number p can be written as:

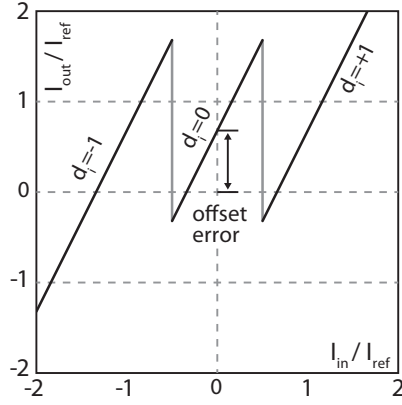
$$p = \sum_{k=1}^m d_i r^i \quad (4.5)$$

For a fixed base, several digit set representations are possible. Well known binary numbers use the base $r = 2$ with a digit set $D = \{0, 1\}$ whereas a radix 2 redundant binary representation (RBR) uses the digit set $D = \{-1, 0, 1\}$; here are more digits in the digit set than necessary, hence the term redundant. RBRs allow addition and subtraction operations without carry propagation which can significantly speed up arithmetic operations with high bit widths. A standard approach for the conversion of a RBR to a binary number is to simply perform the summing operations as in Equation 4.5., which can be implemented by separation of the digit vector into the positive and the negative digits and then perform a carry-propagating addition.

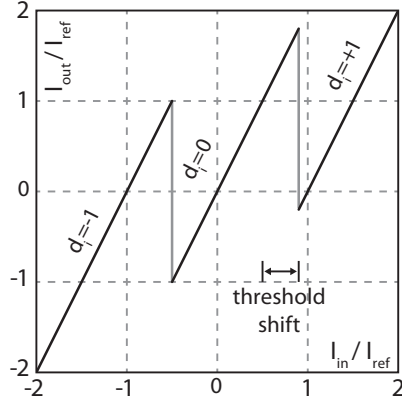
The natural output of the DCD2 ADC is a RBR, so a conversion process is necessary. The sequentially produced bits, most significant digit first, are stored in a shift register. After the ADC finished the conversion process, the shift register is latched and fed to a binary adder. With each clock cycle a single bit addition with carry is performed. This choice of implementation adds significant latency to the digital output, which however has no impact on the DEPFET system. Many arithmetic algorithms which work with redundant representations of a number system produce results most significant digit first, e. g. the SRT division algorithm [see also 40]. Converting these RBRs on-line presents a problem, since carry propagation in any addition or subtraction operation is from least significant to most significant bit. On-the-fly algorithms (i. e. most significant digit first) to



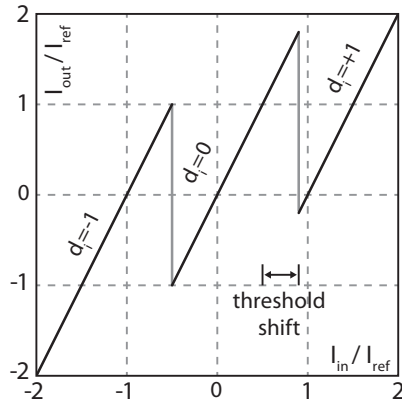
(a) Normal operation



(b) Constant sampling offset



(c) Comparator threshold shift



(d) Excessive errors

Figure 25: Robertson diagrams of the ADC, using RSD conversion. The residue current I_{out} is plotted as a function of the input current I_{in} , normalized to I_{ref} . These plots include the gain of 2 from Equation 4.1a [cf. 76, fig. 6].

(a) In normal operation the comparator thresholds lie at $\pm \frac{I_{\text{ref}}}{2}$, dividing the input current into three regions.

(b) Introducing a constant sampling offset error causes a global shift of the

solve these problems have been proposed by Ercegovac and Lang [28] and generalized by Kornerup [57] and Frougny [33]. With the expense of a few more registers and combinatorial logic, on-the-fly conversion of RBRs to a normal binary representation is possible. On-the-fly conversion is also easy to implement in a hardware description language with a two-state state machine, this is one of the reasons why it is used for the successor DCD-B chip.

4.5 ADC PERFORMANCE SPECIFICATION

The quality of an ADC is specified by its static and dynamic⁵ performance. In our case — sampling of a stable and settled DEPFET drain current — static performance specification is of higher importance. Static errors can be quantified by comparison of the ideal ADC transfer function with the measured, real, characteristics. The following forms of static errors are of importance.

OFFSET AND GAIN ERRORS The transfer characteristic of an ADC follows the straight line equation $D = O + G \times A$, where D is the digital output, A the analog input, and O , G are offset and gain. Ideally, the offset O is zero while the gain G is identical in all channels. Offset and gain errors are, however, of minor importance when reading out DEPFET drain currents. Offsets act identical as pedestal currents I_{ped} , offline analysis software pedestal correction will pick up both. The same is true if DEPFET gain variations are corrected offline. Excessive offset errors (see [Figure 79b](#) on [page 92](#)) or gain errors (see [Figure 79a](#)) have, however, an effect on the total dynamic range as explained in [Section 7.6.2.2](#).

DIFFERENTIAL NONLINEARITY The differential nonlinearity (DNL) is defined as the difference between an actual, measured, code width and the ideal value of 1 LSB. The definition of the instantaneous DNL [42, 66] is:

$$\text{DNL}_i = \frac{Q_{i+1} - Q_i}{\text{LSB}} - 1, \quad i = 1, 2, \dots, 2^N - 2 \quad (4.6)$$

where $Q_{i+1} - Q_i$ is the width of code bin i . Note that the width of the top and bottom bins $i = 0$ and $i = 2^N - 1$ are undefined, since these serve as overflow bins for out-of-range input signals. Referring to the DNL of an ADC usually implies the maximum instantaneous DNL:

$$\text{DNL} = \max_i (|\text{DNL}_i|) \quad (4.7)$$

⁵ Dynamic performance is usually measured with a sine wave input (which can be challenging for a current mode ADC). Specifications include signal-to-noise ratio (SNR), total harmonic distortion (THD), signal to noise and distortion ratio (SINAD), spurious free dynamic range (SFDR), effective number of bits (ENOB), and intermodulation distortion (IMD).

An example is shown in Figure 26. Monotonic behavior is only guaranteed if the ADC produces no missing codes, implying that the DNL error must be always less than one. The RMS value of the DNL can be defined:

$$\text{DNL}_{\text{RMS}} = \left(\frac{1}{2^N - 1} \sum_{i=1}^{2^N - 2} (\text{DNL}_i)^2 \right)^{\frac{1}{2}} \quad (4.8)$$

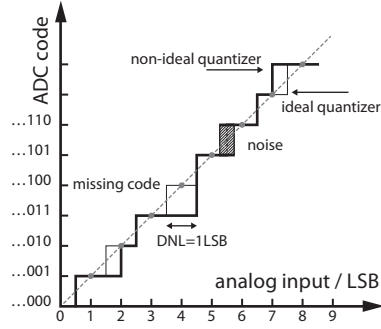


Figure 26: The transfer function of an ideal quantizer (ADC) is compared with a realistic one, where wide or short codes are the cause of DNL. Noise dynamically widens the transition steps.

INTEGRAL NONLINEARITY The integral nonlinearity (INL) is defined as the maximum deviation of the transfer characteristics from a straight line (see Figure 80a on page 93). Two common definitions are used:

BEST STRAIGHT LINE INL is the result of a straight line fit to the ADC characteristics, which also is the closest linear approximation of the actual transfer function. From the fit, gain (slope) and offset can be extracted.

END-POINT INL uses a straight line through the end points of the ADC transfer curve after correcting for gain and offset errors. This often gives a more pessimistic result than the straight line fit.

The INL can also be defined as the accumulation of all DNL errors over the full ADC range [42]:

$$\text{INL} = \sum_{i=1}^{2^N - 2} |\text{DNL}_i| \quad (4.9)$$

QUANTIZATION ERROR An irreversible conversion error is produced during quantization, where a range of analog input values is mapped to a finite set of digital codes. A limit to the quantization error was found in Equation 4.3. The minimum quantization noise can be calculated, assuming that all quantization levels are uniformly distributed and separated by one LSB, yielding :

$$\sigma_{Q(\text{uniform})} = \frac{\text{LSB}}{\sqrt{12}} \quad (4.10)$$

For a real ADC quantization bins have unequal lengths due to DNL. Using the *alternate coding model* [82, ch. 7.5.1], which assumes that the ADC transfer characteristic can be divided into ranges of short and long codes, the total quantization noise related to the DNL becomes:

$$\sigma_{Q(\text{alternate})} = \frac{\text{LSB}}{\sqrt{12}} \times \sqrt{1 + 3 \cdot \text{DNL}^2} \quad (4.11)$$

4.6 BIASING PARAMETERS

The DCD2 design includes multiple biasing parameters that define vital operating points, e. g. gain and speed for amplifiers, the range of the ADC and current memory cells, or the power consumption of the regulated cascode. In many cases such parameters are meant to be *user adjustable*, to adapt to different working scenarios that deviate from the default settings chosen by the ASIC designer. Some parameters even require adjustment to counteract the effects of process, voltage, and temperature variations. Typically programmable digital-to-analog converters (DACs) are included on-chip to handle these tasks — the DCD2 includes 12 current mode DACs with 12-bit resolution and 3 voltage mode DACs with 5-bit resolution. The current mode DACs produce a full scale output of 256 μA , adjustable in 4096 steps. This output current is then scaled using current mirrors^[114] and distributed to the target circuit blocks. All DACs are listed in [Table 1](#) including their used settings and maximum ranges, with their corresponding current values. A description of the parameters is given in the following paragraphs.

INPUT CURRENT SOURCES The input current sources *InjSignal*, *InjBias*, *MainOffset*, and *MainSub* allow test current injection and subtraction of the DEPFET pedestal current. *MainOffset* is the main current source to subtract up to 100 μA of input current. *MainSub* is used to further adjust the input current to the ADC range; since the ADC has a bipolar input and the current flowing through the regulated cascode has to be always positive this cannot be accomplished by *MainOffset* alone. *InjSignal* is a switchable test current source which can be steered by a FPGA generated external strobe signal. The total current I_{in} flowing into the ADC in a channel can be calculated⁶ with given DAC settings of the 4 currents by:

$$I_{\text{in}} = \frac{1 \mu\text{A}}{4096} \left(213 \cdot (\text{InjBias} + \text{InjSignal}) - 256 \cdot (\text{MainOffset} + \text{MainSub}) \right) \quad (4.12)$$

REGULATED CASCODE BIASING The usage of *CascAmpBias*, *CascAmpLoad*, and *CascAmpSF* is shown in [Figure 20](#) and [Figure 21](#). Measurements with varying *CascAmpBias* are presented in [Section 6.2.2](#).

CURRENT MEMORY CELL BIASING The transfer characteristics of the current memory cells can be adjusted using *VPFB*, *VPLoadFB2*, and *VPLoadFB*. Optimal settings (for operating range and speed) are achieved if the input range of the memory cell is symmetric to zero current and as large as possible, see [Figure 23](#). A good starting point is to increase all three values simultaneously; *VPLoadFB* defines the whole range, while symmetry adjustments are done with *VPLoadFB2* (positive range) and *VPFB* (negative range)^[75].

⁶ This calculation is an approximation, assuming that all current mirrors match exactly, neglecting second order effects, and that the on-chip DACs show perfect linear outputs. For measurements an external precision current source is used instead, since deviations are expected between the channels.

Table 1: DCD2 internal bias settings.

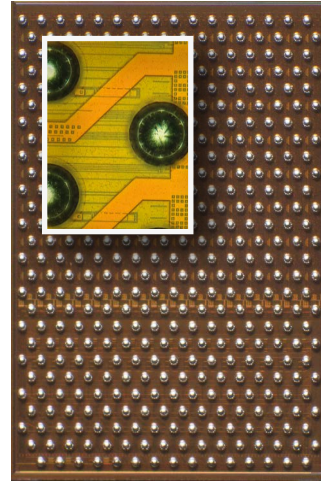
name	default setting		used setting		DAC range
	LSB	μA	LSB	μA	μA
test current sources					
InjSignal	0	0	variable		213
InjBias	480	25	variable		213
MainOffset	320	20	1600	100 ^a	256
MainSub	160	10	280	17.5	256
regulated cascode					
CascAmpBias	528	1017	700	1350	7890
CascAmpLoad	320	308	250	241	3950
CascAmpSF	212	41	250	49	800
current memory cells					
VPampBias ^b	384	20	384	20	213
VPFB	192	20	400	41.7	427
VPLoadFB2	192	10	320	16.7	213
VPLoadFB	210	10.9	360	18.7	213
misc.					
VNDelay	400	25	800	50	256
VPCascFB	5		5		
VNCascFB	21		21		
RefFB	13		13		

^a used up to 100 μA to sink the DEPFET drain current^b memory cell amplifier bias, see A in [Figure 22](#)

4.7 THE NEXT GENERATION DCD-B READOUT CHIP

A successor to the DCD2 chip has been commissioned [see 79]. The design of the DCD-B is focused on providing a close to final analog readout solution for Belle II DEPFET devices. The geometry is rescaled to approximately $3\text{ mm} \times 5\text{ mm}$ to accommodate 256 input channels. Connectivity of all inputs and outputs is achieved by commercially placed solder bump-bonds. The digital output multiplexing scheme is relaxed to reduce the required input / output frequency from 600 MHz to 400 MHz by choosing a four-fold instead of a six-fold multiplexer. The digital output pads are implemented as non-standard single-ended signals to facilitate the communication with the DHP chip (see [Section 3.5.1](#)); for test-systems, however, an additional signal transmission chip[59] adapting from these single-ended signals to differential signaling is required. The digital readout and control block for processing of the ADC codes and generation

Figure 27: Picture of the DCD-B. The chip is implemented in UMC 180 nm technology with an area of $3240\text{ }\mu\text{m} \times 4969\text{ }\mu\text{m}$. Bump bonds with a minimum distance of $200\text{ }\mu\text{m}$ are used for all connections. Picture courtesy of ZITI, University Heidelberg.



of fast steering signals is now fully synthesized. A standardized JTAG-Interface for slow control is provided.

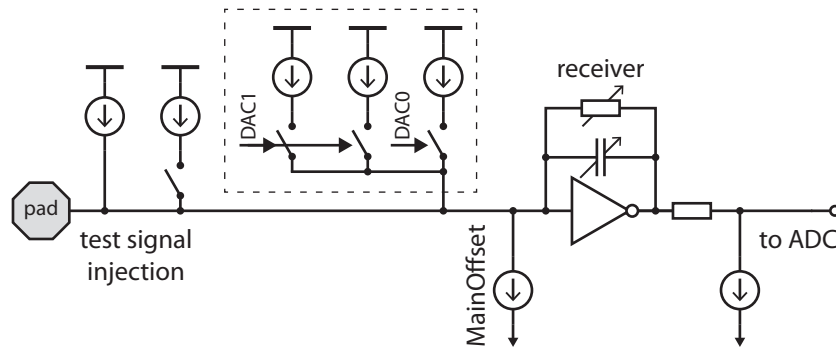


Figure 28: Schematic of the analog input stage of the DCD-B. Compared to the DCD2 (cf. Figure 19) a 2-bit DAC is added to extend the input dynamic range. The regulated cascode is replaced with a resistive current receiver with adjustable gain.

The analog part (see Figure 28) is improved to provide better noise performance and a higher dynamic range. The two major changes are:

CURRENT RECEIVER: A resistive current receiver (trans-impedance amplifier) replaces the regulated cascode, yet it is equivalent in terms of transfer function and small signal model. The current receiver is expected to work more linear and the input potential can be chosen freely which in turn eliminates the additional power supply voltage V_{CAVSS} ⁷. It features a selectable gain (by a factor of 1, 2, 3 and 4) and an adjustable settling time. Since the main source of electronic noise in the DCD-B is the input transistor of the current receiver, choosing slower settling times will improve the noise performance.

⁷ However one important feature of the regulated cascode is lost: the input current equals exactly the output current and no additional offset and gain errors are introduced. In case of the resistive current receiver channel-to-channel transistor mismatch and biasing differences can introduce further errors.

DYNAMIC RANGE EXTENSION: Newly included is a 2-bit DAC to improve the dynamic range of the ADC. It is implemented by two switchable current sources⁸ in front of the current receiver. The 2-bit data for each channel has to be supplied dynamically by either the DHP or the test-system and can be different for every DEPFET pixel. This DAC can be understood as a low-noise range extension to the ADC: the setting of the DAC bits require previous knowledge (based on measurements of pedestal currents I_{ped}) and therefore during digitization of the DEPFET drain current no additional decision making process (e. g. comparison to thresholds) is introduced. This concept is further illustrated in [Section 7.6](#).

⁸ The two bit DAC has been designed in a way to add current. Although this seems counter-intuitive, in this way the design can be realized with *p*-channel MOSFET current sources instead of *n*-channel current sinks, which provides advantages when following a radiation hard design strategy.

A test system for any Belle II readout chip has to fulfill multiple requirements. It needs to be able to connect to all relevant inputs / outputs of the device under test (DUT), the output data rate needs to be manageable, storage space (i. e. memory) with sufficient bandwidth and depth needs to be present, and communication with a computer is mandatory. The test system (see [Section 5.1](#)) needs to be flexible to adapt to different test scenarios, which can be achieved by employing a field-programmable gate array (FPGA) as the central component. A FPGA allows free assignment of its inputs / outputs, functionality can be implemented using some higher hardware description language (e. g. Verilog or VHDL), it provides numerous specialized internal resources and — most importantly — it can be reprogrammed. The particular choice of FPGA is further detailed in [Section 5.1.1.1](#).

Moreover, the test system should not only act as a test bench for the readout chip, but it should also be capable to interface to a full DEPFET hybrid PCB (see [Section 5.2](#)), which includes steering of the SWITCHER chips, and further increases the demand for storage space and precise timing. A design approach that yields a stable, low noise, working, accessible for testability, and reusable system is needed; some of the used components and design techniques are outlined in the following sections and figures.

Once all the components are assembled (see [Section 5.3](#)), the hybrid PCB is populated with a DCD2 and a DEPFET sensor (two types are available, see [Section 5.3.1](#)). A very brief review of the developed software and firmware is given in [Section 5.3.2](#). The powering scheme of the full system, due to its complex nature, is reviewed in [Section 5.3.3](#).

5.1 DEVELOPMENT OF A FPGA READOUT SYSTEM

The development of a FPGA based readout solution was driven by the finalized specifications of the DCD2 readout chip. When developing such a system, it is a reasonable approach to look at past developments (e. g. the S3B system [88] with older hybrids) and include their benefits and omit the mistakes made; but one should also dare a speculative look into the future and include provisions for plans to come. From the specifications given in [27, 77–79] of the DCD2 and the SWITCHER₃ chips, the Belle II module concept which foresees a larger successor of the DCD2 chip, and lessons learned from beam test efforts and older systems, the following list of requirements to an FPGA based readout system arises:

CONNECTIVITY describes the number and type of inputs / outputs available at the FPGA, and connections to other components (e. g. memory, computer, DUT)

- ♦ provide up to 32 differential inputs / outputs to a DUT (although the DCD2 only uses 14)
- ♦ provide 25 single ended inputs / outputs to the DUT
- ♦ 32 single ended and 4 differential inputs / outputs, all electrically isolated, to connect two SWITCHER₃
- ♦ interface to a trigger logic unit (TLU)[25] for future beam test operation
- ♦ interface to a computer for data transfer and configuration (60 inputs / outputs)
- ♦ interface to a logic analyzer for debugging (32 inputs / outputs)
- ♦ high speed interface to memory (75+41 inputs / outputs)
- ♦ use high quality, high-speed capable, rigid connectors

SPEED REQUIREMENTS include data rates, timing¹ precision, expected bandwidths, and are mainly driven by the maximum input / output frequency of the DCD2 ($v_{\max} = 600 \text{ MHz}$)

- ♦ all differential inputs / outputs should work at $v_{\max}$
- ♦ all single ended inputs / outputs should work at $\frac{1}{2} \cdot v_{\max}$
- ♦ all high speed inputs / outputs need impedance controlled routing, length and phase matching
- ♦ provide digitally controlled impedance² for the inputs / outputs
- ♦ memory bandwidth of $\approx 2 \cdot 12 \cdot 600 \text{ MHz} = 14.4 \text{ Gbit s}^{-1}$, which would be enough to read out two DCD2 at full speed, or a future larger chip
- ♦ precise time shifting of SWITCHER signals in the order of 1 ns, to allow an exact definition of DEPFET clear and sampling points
- ♦ FPGA input / output clock speed of $v_{\max}$ needed
- ♦ interface to a logic analyzer with at least 400 MHz
- ♦ FPGA needs to provide programmable, fine grained, clock management

¹ Depending on the context, *timing* refers to the time relationship between two or more digital signals, or the act of measuring elapsed time; it can also implicitly include secondary effects such as jitter. In digital system design, *timing* (see *static timing analysis*) refers to the ability of a particular circuit to operate with a given clock frequency.

² *Digitally Controlled Impedance* (DCI) is a form of on-die termination for input / output signals. DCI automatically adjusts the impedance of the inputs / outputs by selectively turning transistors on or off. Reference resistors external to the FPGA matching the characteristic line impedance have to be provided. During device operation, continuous recalibration is performed to counter process, voltage and temperature variations. [see

MEMORY for storing read out frames of a DEPFET matrix (e. g. in a beam test) or just data from the DUT

- ♦ use a FPGA with internal memory resources for a few full DEPFET matrix frames
- ♦ provide (slow) external memory identical to the S3B system
- ♦ provide high bandwidth, synchronous external memory with larger capacity

SAFETY, STABILITY AND TESTABILITY is essential for system operation, and should include a low noise design approach

- ♦ the system needs to detect if power is supplied to the DUT
- ♦ temperature measurement of the DUT
- ♦ provide the standardized Inter-Integrated Circuit bus (I²C) to the DUT
- ♦ test points and clear labels for all voltages and relevant signals
- ♦ use a system monitor for controlled power up sequencing, voltage control (margining) and power failure detection

5.1.1.1 Design overview and features

A functional overview is given in the block level diagram of the FPGA readout system shown in Figure 29, a photograph of the final design is shown in Figure 30. The readout system is implemented on a 12-layer 100 mm × 160 mm sized PCB using 580 passive and active components with a total of 3600 pins, 3000 drilled holes, and a combined routed trace length of 34 000 mm. The maximum power consumption is ≈ 10 W with a supply voltage in the range of 4.5 V to 5.5 V.

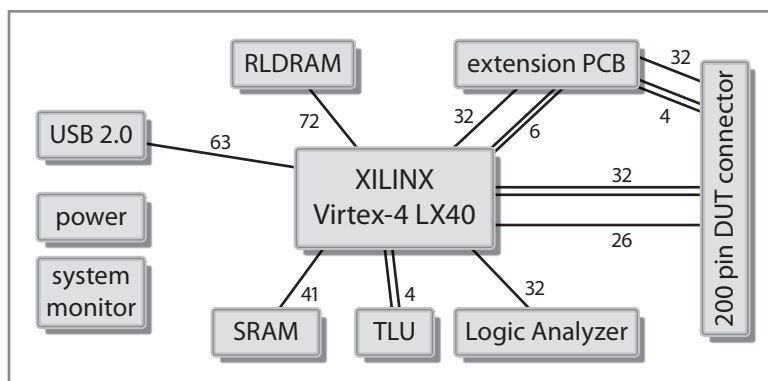


Figure 29: Component based block level diagram of the readout FPGA system. The central component — a XILINX Virtex 4 LX40 FG1148 FPGA — connects to all periphery. Numbers given in the diagram indicate the amount of single ended or differential connections needed.

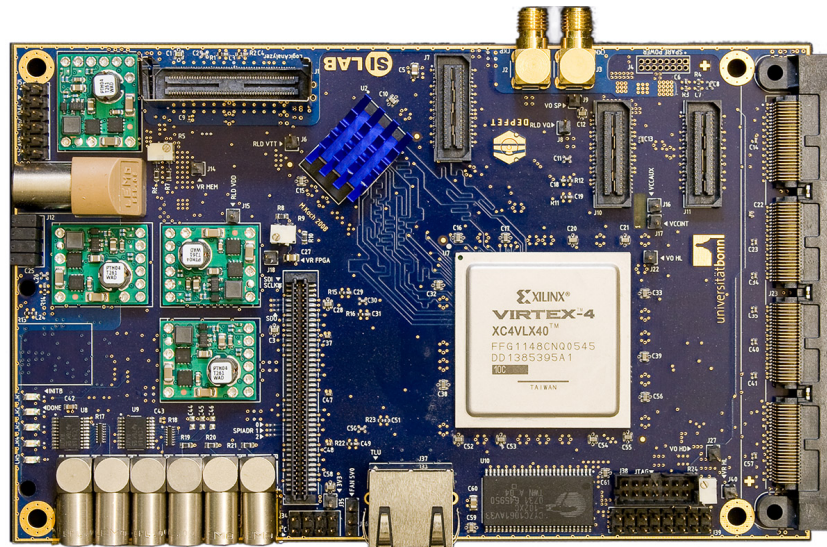


Figure 30: A custom DEPFET FPGA based readout solution PCB has been developed. Based on a XILINX Virtex 4 LX40, it offers 36 high speed differential and 58 single ended input/outputs for operating a DUT, fast storage memory with a capacity of 288 Mbit, connectivity to a TLU, multiple high speed connectors for extensions, and a well designed power distribution network (PDN) for all components. The outer dimensions of this 12-layer PCB are 160 mm $\times$ 100 mm, maximum power consumption is ≈ 10 W. Connectivity to a computer is possible with an add-on USB interface.

5.1.1.1 FPGA and memory selection

A XILINX Virtex 4 LX40 FPGA in a FG1148 package has been selected as the central component for the design. This device offers high performance for logic applications, 288 kbit distributed memory, 1728 kbit block memory, more than 40000 configurable logic blocks, memory interface support for RLDRAM-II, and a total of 640 user inputs / outputs with numerous options for input / output standards and impedance control. A large package with 34×34 pins was chosen to simplify routing during the PCB design. Many of the inputs / outputs can be used in differential mode and support speeds up to 1 Gbit/s; internally dedicated logic exists to serialize and de-serialize incoming and outgoing data, which allows an adaption of the data rate to a slower clock within the FPGA. All FPGA features, specifications and design guidelines can be found in the documentation from XILINX [117].

An external surface-acoustic-wave (SAW) oscillator provides a precision, low jitter, and low drift 200 MHz reference clock to the FPGA. Multiple reprogrammable digital clock managers (DCM) integrated to the FPGA allow a variable output clock speed from 24 MHz to 600 MHz.

As an external memory component, a 288 Mbit RLDRAM³ device has been chosen for reasons of simplicity: it is directly supported by the FPGA and provides the needed bandwidth for the readout system.

³ RLDRAM: reduced latency dynamic memory, optimized for high speeds and peak bandwidths; component used MT49H8M36BM-33 from Micron Technology, Inc.

5.1.1.2 *High speed and low noise design*

For a DUT that is potentially sensitive to electronic pickup and noise, a careful design of the FPGA system to reduce electronic switching noise or reflected energy on transmission lines is necessary. This is especially true when dealing in parallel with high speed designs⁴. It is the responsibility of the designer to assure that all aspects of a low-noise and high-speed design harmonize with each other. Standard literature on signal integrity is available [21, 44, 45, 74] and resources from industry experts can be consulted [see e. g. 93, 98]. It is further advisable to develop a design strategy for an optimal power distribution network (PDN), which includes simulations and a careful decoupling capacitor selection [112, 113, 115, 116]. The design is further optimized using dedicated electromagnetic design software [see 109] for optimal decoupling capacitor placement. This allows to minimize switching noise on power and ground planes, to eliminate resonances on these planes by using dissipative edge termination [see 19, 70, 73], and to optimize power supply output impedance over a wide frequency range.

A very important design issue is the choice of layer stackup⁵ used. It influences directly the geometry constraints for impedance controlled transmission lines, signal integrity and the effectiveness of the PDN. For this design a total of 12 layers are used, 6 of those are used for routing of signals while 3 layer pairs with 50 μm distance serve as embedded capacitance for the PDN. For increased manufacturing yield and reduced cost, all dielectric thicknesses have been chosen so that no trace needs to be thinner than 150 μm and impedance control is still possible.

5.1.1.3 *Safety features*

The supply voltages of the DUT can be connected to the readout system, where a programmable-delay supervisory circuit compares these voltages to an adjustable threshold and consecutively signals the FPGA if these voltages are present and stable. This helps the user to ensure that logic-high signals are never applied to a powered-down or malfunctioning DUT, otherwise damage could occur to the DUT by overloading the input / output protection diodes.

A system monitor⁶ has been included in the design. It facilitates programmable sequencing, monitoring and margining of all 10 board supply voltages. In case of component failures, over voltages, startup issues, or a more common short circuit somewhere in the setup due to human error, the whole system is safely shut down and the error is indicated to the user.

⁴ As an example, the momentary change of current flow of the RLDRAM memory component in case of simultaneous switching of 60 lines is $\approx 2\text{ A}$ in 1 ns.

⁵ *Stackup* refers to the sequential buildup of a PCB, and includes information about the conducting materials used (type, thickness, galvanic and chemical processes involved) and isolators (type, thickness, relative permittivity $\epsilon_r(\omega)$, resin content), as well as via pairs and allowed drill sizes.

⁶ Analog Devices ADM1062 super Sequencer with Margining Control and Temperature Monitoring

5.1.2 Outlook and alternative uses

The FPGA system proved to be a very reliable, multi-purpose and stable readout solution. A second larger batch with minor cosmetic changes of this PCB has been produced. It is successfully used for laboratory and beam tests by the *DEPFET Collaboration* for a successor system based on the DCD-B readout chip and the PXD6 sensor generation; prototyping and emulation for the DHP chip has also been implemented on this board.

As the system has been designed with a multi-purpose approach in mind, other uses outside of the *DEPFET Collaboration* are possible and welcome. So far the system has been used for bit error rate tests on cables, and serves as an emulation platform for future pixel detector development within the *ATLAS Collaboration*.

5.2 DEVELOPMENT OF A HYBRID FOR THE DCD2 AND A DEPFET SENSOR

To connect a DUT to the FPGA system (see [Section 5.1](#)), a PCB is needed to house the ASICs and include their needed periphery. This PCB is called *hybrid*, since more than one distinct device type is combined (i. e. silicon sensors, ASICs, and other active, passive and mechanical components). Hence a dedicated hybrid was designed to house a DCD2, two SWITCHER₃ and a DEPFET sensor.

5.2.1 Design overview

The hybrid is implemented on a 10-layer 100 mm × 125 mm sized PCB, with more than 300 mainly passive components to ensure signal and power integrity. A picture of the final design is shown in [Figure 31](#), and a simplified block diagram is given in [Figure 32](#). Two distinct features have been combined in the design: to provide a test platform for the DCD2 chip, and to operate a full DEPFET system including SWITCHER₃ and the sensor itself.

DCD2 TESTS require access to all input / output pads of the chip. A connection to the monitor bus (see connections in [Figure 19](#)) is possible using a SMA connector, all on-chip DACs are accessible as well. Input pads can be wire bonded to some adapter (e. g. see [Figure 55](#) on [page 64](#)) for direct measurements. All high speed output lines are length matched to ensure correct data sampling inside the FPGA.

DEPFET SENSORS can be glued to the PCB and wire bonded to the ASICs. The keep-out region for the sensor has been designed in a way that two different sensor geometries can be fitted. A standard sized 128 × 128 PXD5 sensor as well as long 256 × 1024 PXD5 sensor can be used; however for the long sensor only 1/8 of the total SWITCHER channels closest to the readout chip are connectable. The DCD2 chip has no matching wire bond pattern, input channels on this test chip have been laid out as bump bond pads spread over the chip area. Therefore only a limited amount

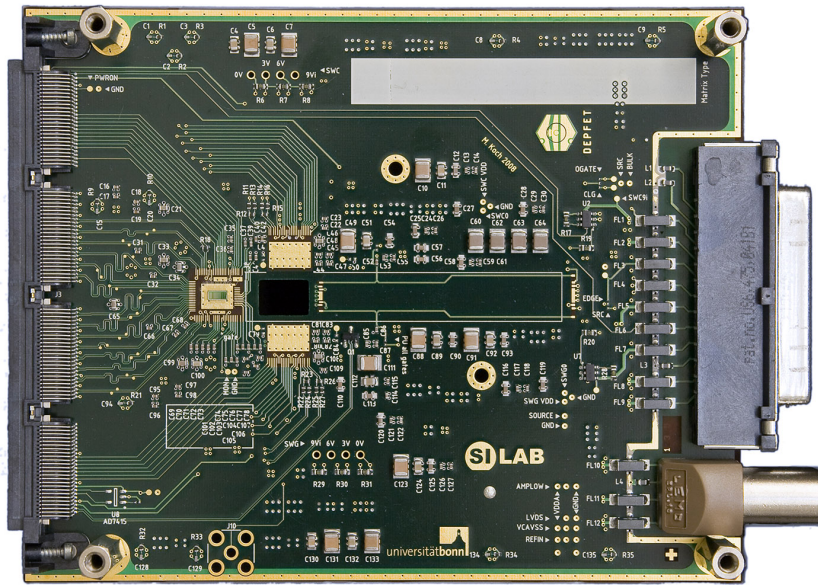


Figure 31: A hybrid PCB has been developed to provide a test platform for the DCD2 chip, and to allow the assembly of a full system with a DEPFET device and two SWITCHER₃ chips. Either a short or a long DEPFET matrix can be connected. A 200-pin rigid connector (left) interfaces with a FPGA-PCB, while power is supplied using a D-SUB connector (right). The breakout region (hole) underneath the DEPFET allows laser based measurements from the back side.

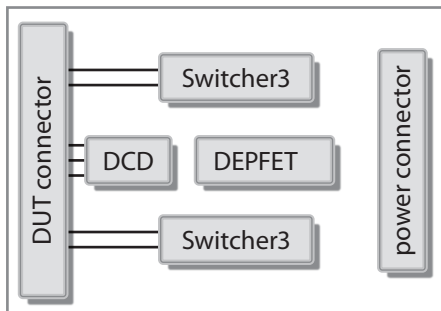


Figure 32: Component based block level diagram of the hybrid.

of DEPFET channels can connect to the read out chip (before crossing of wires would cause shorts).

THE SWITCHER₃ chips are used similarly to the older S3B system [88]. The required electrical isolation is implemented using an extension PCB which connects to the FPGA board. The power up sequence of the SWITCHER₃ requires the chip to be digitally configured before the (high) switching voltages are applied to the chip; for added safety and convenience an active, FPGA-controllable switch⁷ has been included.

CONNECTIVITY to the FPGA system is ensured with a mating 200-pin rigid, high speed connector. Power can be supplied to the system using a 25-pin D-subminiature (D-SUB) connector; the DCD2 can also be powered stand-alone using a specialized 5-pin connector.

⁷ Fairchild Semiconductor FDC6330L Integrated Load Switch

POWER AND SIGNAL INTEGRITY is an important design directive for high speed components which have a sensitive analog input stage. All traces have been routed with impedance control with improved spacing for reduced crosstalk. The inner 4×2 layers of the PCB are exclusively used as embedded capacitance to provide low inductance power supplies to the system. In [Figure 33](#) options chosen for filtering and decoupling are explained. Furthermore, test points are provided for all relevant digital signals and power nets to simplify initial debugging.

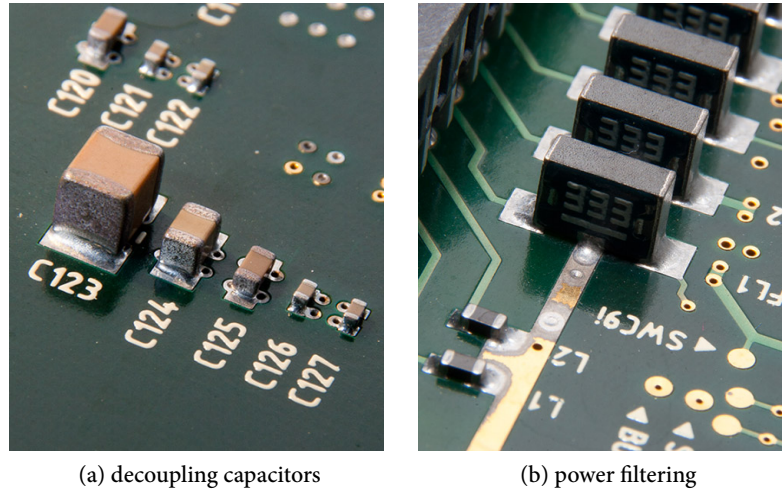


Figure 33: Two examples for the power integrity on the hybrid PCB. This considerably improves the noise immunity if unshielded long cables for power supply in a laboratory environment are used. The effectiveness was measured with a spectrum analyzer; on the PCB very low noise on supply rails was observed while beyond the filters significant disturbances from civilization sources (e. g. radio) were present. (a) Quality capacitors with various values and parasitic inductances are combined to provide a low power supply output impedance over a wide frequency range. Using simulations, cross-resonances between the different values have been reduced. (b) All incoming supply voltages are filtered using either LCL filters or ferrites [see 30, 65]. Power planes have been completely removed in the area between the connector and the filters to avoid parasitic capacitive coupling to noisy inputs.

5.3 TEST SYSTEM ASSEMBLY

This section contains a summary of additional components to complete the test system. Even though these efforts and developments consumed the lion's share of time, only the final accomplishments are presented here in pictures.

The full test system is based on the the FPGA-PCB ([Section 5.1](#)) and the hybrid ([Section 5.2](#)), which in turn is populated with the DCD2 ([Section 4](#)), the SWITCHER₃ chips, and DEPFET sensors. A power supply PCB has been added to allow easy cabling in a laboratory environment. The full system is shown in [Figure 34](#).

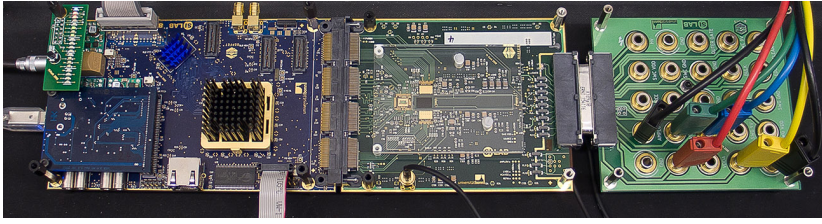


Figure 34: The full test system consists of the FPGA-PCB (left), a hybrid (middle) for testing the DCD2 chip and/or a DEPFET device, and power supply PCB (right). The power supply PCB is a connectivity solution to adapt the D-SUB connector to 4 mm plugs, thus allowing flexible cabling to laboratory power supplies.

5.3.1 Chip assembly

The assembly of all ASICs involves gluing the silicon die with a thermally and electrically conductive epoxy glue to the corresponding gold-plated copper surface on the hybrid PCB. Electrical connections are then made using aluminum wire bonds directly from pads on the chips (passivation openings) to the PCB. The wire bonded DCD2 is shown in Figure 35. The assembly proved to be particularly challenging since a total of 108 pads with a pitch of only 80 μm needed to be connected (including six different supply voltages on multiple pads, which should not connect to long break-out traces).

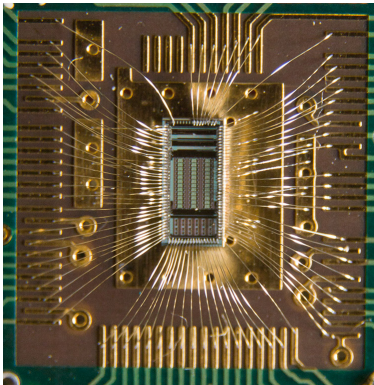


Figure 35: Wire bonded DCD2, glued to the hybrid PCB. Three overlapping levels of ≈ 100 wires connect to ground, supply voltages, and all other inputs/outputs. The solid ground-plane underneath the chip provides good heat dissipation to inner PCB-layers.

Two hybrids have been equipped with DEPFET sensors. A short COCGL DEPFET device is shown in Figure 37 and Figure 36, a long DEPFET COCGL SA device is shown in Figure 38. Connections to the DCD2 are made with long wire bonds directly to input pads spread over the chip area. Care has been taken to connect neighboring DEPFET channels to allow clustering for measurements.

5.3.2 Software / firmware development

A software suite has been developed (using C++/Qt) to interface to the FPGA system, communicate with the ASICs, automate parametric measurements and preprocess data for further analysis. A corresponding firmware for the FPGA was developed alongside, which facilitates the slow control and configuration of the ASICs, decodes the raw DCD2 data, and

Figure 36: A short COGGLE DEPFET device with a DCD2 and two SWITCHER₃ chips assembled on a hybrid. The planar view allows better size comparison (see Figure 37 for a different view).

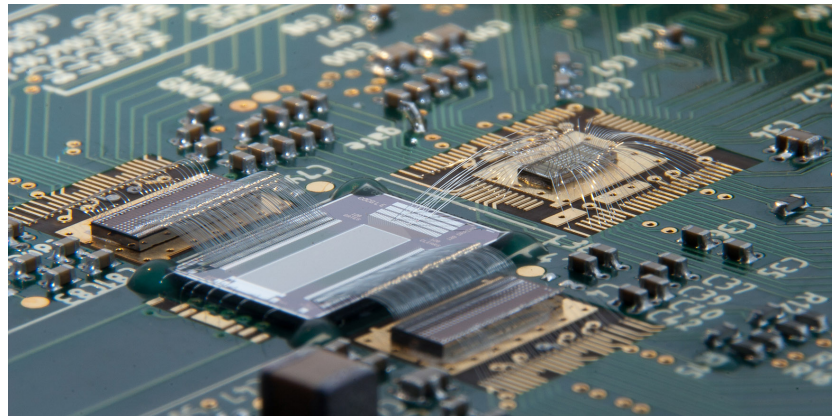
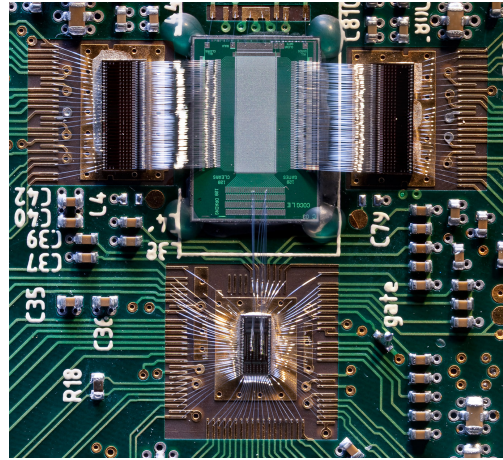


Figure 37: A short (6 mm) DEPFET COGGLE device is assembled on the hybrid, with two SWITCHER₃ and one DCD2 chip. The same device size is used on the previous S3B system, devices of the same designation COGGLE have been extensively characterized and used in beam test efforts before. This photograph particularly shows the artistic bond wire connections from twelve neighboring drain-lines to the DCD2.

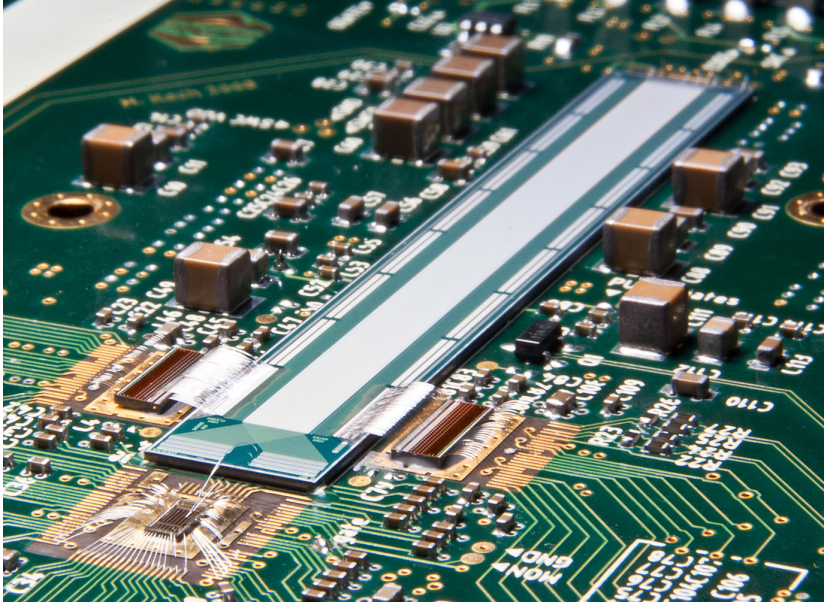


Figure 38: A long (50 mm) DEPFET COCG SA device is assembled on the hybrid, with two SWITCHER₃ and one DCD2 chip. Long wire bonds are used to connect few drain-lines to input channels of the readout chip. Only the lower 128 of 1024 SWITCHER channels are connected. The long COCG SA device provides ≈ 60 pF of input load capacitance to the DCD2.

prepares the data for transmission. The following notable features were implemented:

- ◆ The operating frequency ν of the DCD2 is adjustable from 24 MHz to 600 MHz in about 500 individual steps given by $\nu = m/n \times 200$ MHz with $m, n \in [1..32]$.
- ◆ A programmable sequencer has been implemented to allow a free adjustment of all relevant steering signals relative to each other (e. g. strobes for the gate- and clear- SWITCHER, DCD2 sampling, test signal injection). The sequencer is referenced to the row clock row_{CK} of the DEPFET matrix and allows a granularity of 96 steps with $\frac{1}{96} \times T_{\text{row}}$. Example: In case of a row frequency of $\text{row}_{\text{CK}} = 12.5$ MHz with a corresponding $T_{\text{row}} = 80$ ns the ability to adjust the signals is ≈ 830 ps.

5.3.3 Powering scheme

Powering the test system with a DEPFET sensor connected is a complicated matter. In total 15 independent supply voltages are needed, the DCD2 needs 5 alone, the DEPFET including the SWITCHER₃ needs an additional 9 voltages. The FPGA PCB, on the other hand, is self-sufficient: From a single input voltage (4.5 V to 5.5 V) all needed voltages (a total of 10) are generated. All voltages supplied to the system were generated with typical

laboratory power supplies⁸. No special power up/down sequence was performed, the system performed stable in multiple scenarios. However, for operational safety the following points were strictly enforced:

- ♦ Current limit is mandatory for all supply voltages
- ♦ over-voltage-protection (OVP) and over-current-protection (OCP) is used when provided by the power supply
- ♦ The FPGA is configured first, before any of the ASICs are powered
- ♦ The high switching voltages for the SWITCHER 3 are applied only after configuration of the chips (controlled by the FPGA)
- ♦ The FPGA detects (see [Section 5.1.1.3](#)) applied voltage to the DCD2 and performs configuration immediately

The voltages for the DCD2 are summarized in [Figure 39](#), including current consumption for two different supply voltages. In [Figure 40](#) the DEPFET voltages are given as used for measurements.

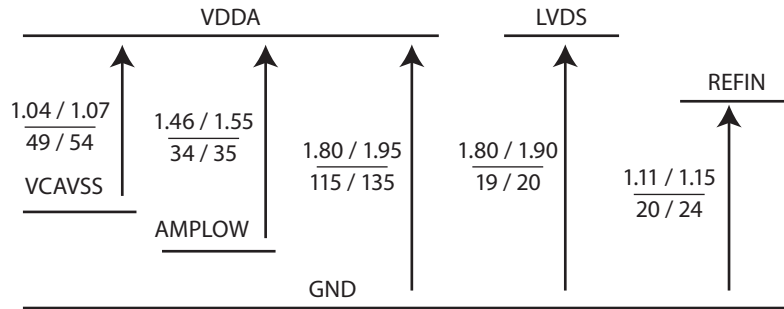


Figure 39: DCD2 supply voltages. Each arrow indicates one needed supply. The numbers given are voltage (above bar) and current consumption in mA (below bar) for two different scenarios. The numbers on the left are the suggested design values from [78], the numbers on the right are the used working set. The most prominent change is the increase of the supply voltage VDDA from 1.8 V to 1.95 V.

⁸ For the DCD2: Agilent E3631A Triple Output DC Power Supply,
Agilent E3646A Dual Output DC Power Supply
For the DEPFET: Thurlby Thandar Instruments QL355TP

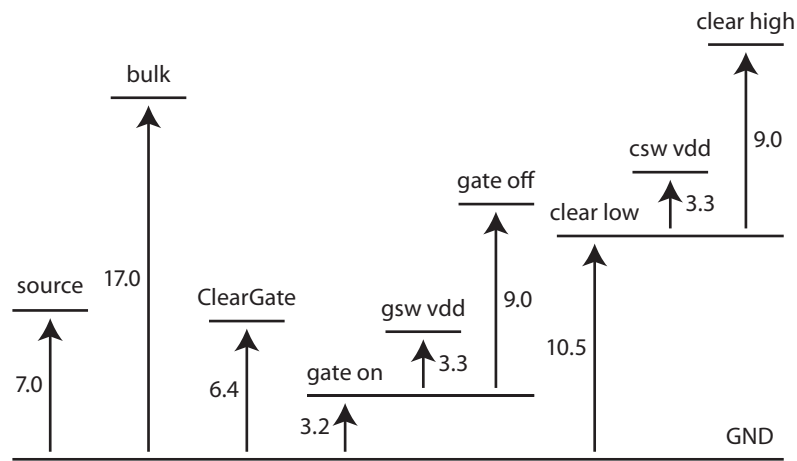


Figure 40: DEPFET supply voltages. Each arrow indicates one needed supply. The numbers given are the set voltages. Two 3.3 V supplies (gsw vdd, csw vdd) are used for the SWITCHER₃. Additionally for depletion of the sensor a high voltage of ≈ -180 V is needed.

DCD2 MEASUREMENTS

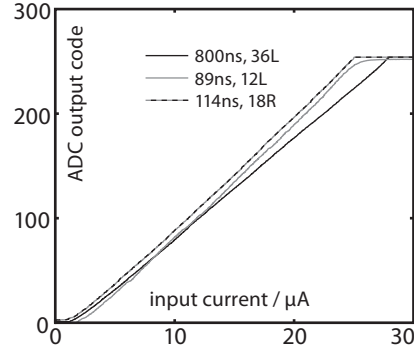
The DCD2 readout chip is characterized in detail in the following sections. Static measurements, which do not involve a changing input signal, and dynamic measurements are presented. Typical ADCs performance specifications are established, involving gain, range and offsets; these are followed by measurements of INL, DNL, noise, and effective error. The section on the dynamic measurements focuses on the performance of the input stage of the DCD2, the regulated cascode, where the rise time of input signals under capacitive load is shown. Throughout this chapter, a focus is put on the performance under typical Belle II readout scenarios.

6.1 STATIC MEASUREMENTS

For 24 individual DCD2 channels¹ — with two individual ADCs each — the gain, offset, DNL, INL, noise, noise under capacitive load, and effective error are measured. An input current is generated using a precision external current source², and swept from 0 μA to 30 μA in 25 nA steps. This current is filtered³ for additional noise suppression, and fed into the DCD2 using the *monitor bus* through the regulated cascode (see Monitor 1 in Figure 19). On chip, the MainSub current sink⁴ is set to $-17.5 \mu\text{A}$ (DAC 280) in each channel to fully utilize the ADC range. All other input current sources (cf. Figure 19 and Table 1) are turned off. For each input current 1000 samples are taken, yielding a total of 1.2×10^6 samples over the full ADC range. The two individual ADCs per channel are treated strictly separate⁵. The recorded transfer curves (see example in Figure 41) are further processed using offline analysis software to extract the static ADC performance characteristics — the results and methods used are summarized in the following sections. Recording of the transfer curves

- 1 Even though the prototype chip DCD2 has a total of 72 channels, only 24 of those (ch. 36–59) have been designed in a way to work at the maximum speed required, they are used exclusively. Multiple assemblies with DCD2s have been produced (two stand-alone setups, one with bonded capacitors, two with DEPFET devices) and are used where applicable.
- 2 Keithley 2400 SourceMeter [46]: specified current measurement accuracy in the 100 μA range of $\pm(0.025\% + 6 \text{ nA})$; noise (peak-peak) in the 100 μA range, within 0.1 Hz to 10 Hz, of 500 pA.
- 3 An additional series R-C-R filter (100 k Ω -100 nF-100 k Ω) was used for noise suppression. Internal regulation loops of the Keithley 2400 cause excessive noise in the kHz-range when used as a current source. (Confirmed by email, Keithley Instruments support, 01/2009)
- 4 The measurements therefore include offsets due to mismatch of the MainSub current sinks. Feeding the input current directly into the ADC, thus bypassing the regulated cascode, proved to be unreliable due to dynamically changing input potentials of the current memory cells. One alternative could be to turn off MainSub, and use only half of the ADC range for measurements.
- 5 The two ADCs in each channel are usually labeled *L* and *R*. Unambiguous mapping of output data to the L or R ADC is always possible.

Figure 41: (example) Three transfer curves of different DCD2 ADC channels and sampling time, where the ADC output code is measured as a function of the input current, showing visible differences in gain, offset, and linearity.



happens one channel at a time, since the calibration current over the monitor bus can only be fed into one selected channel.

Two biasing scenarios are used for these measurements, differing essentially in the analog supply voltage V_{DDA} . While the nominal supply voltage is 1.8 V, it had to be increased⁶ to 1.95 V in order to maintain reliable operation at higher readout speeds (see Figure 39 on page 50) and to compensate for on-chip voltage drops. The following graphs and measurements show a selection of both biasing schemes.

The measured data is often displayed using boxplots [68, 104]. On each box, the central line marks the median, the edges mark the lower and upper quartile (or 25th and 75th percentile), and the whiskers cover a 99.3 % range ($\pm 2.7\sigma$ in case of a Gaussian distribution); outliers are plotted individually. This is a convenient way to display multiple distributions which are not necessary of Gaussian shape; it is specifically less visual biased than similar attempts with varying shades of color and less cluttered than multiple histograms. Additionally, since the full range of the data is visible, engineering requirements for dynamic range or worst case scenarios can be spotted easier.

6.1.1 Gain, range and offset

THE DYNAMIC RANGE of the ADCs is an important parameter for digitizing DEPFET drain currents and is linked⁷ directly to the gain of the ADCs. The range of the ADCs is defined as the difference between the maximum and minimum current that can be digitized without clipping. It should be noted that the gain and range are strongly influenced by user-selectable biasing parameters (see Section 4.6); the parameters used here are optimized primarily for reliable operation at high readout speeds and secondarily for a maximum dynamic ADC range. For the targeted Belle II readout speed of ≈ 100 ns per row an ADC range of 24.37(35) μA can be set, which corresponds (assuming a DEPFET $g_q = 500$ pA/ e^- as a target for the Belle II sensors) to a input signal range of 48 740(700) e^- . The spread of the ADC ranges is ≈ 1.8 μA and is consistent for sampling speeds faster than

⁶ The UMC180 technology is specified to work with 1.8 V + 10 % maximum supply voltage. Increasing the voltage beyond that point can lead to permanent damage.

⁷ Given the gain g in LSB/ μA , the range r could be calculated simply by $r = 2^{-8} g$. Some channels, however, do not work over the full range and clipping to some minimum/maximum value occurs; in fact, no channel ever outputs the maximum digital code 0xFF. For this reason the range is treated as a separate measurement.

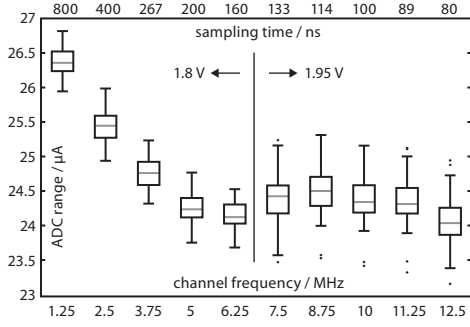


Figure 42: DCD2 ADC ranges measured vs. sampling time. A range of $24.37(35) \mu\text{A}$ can be set for typical Belle II readout speeds of $\approx 100 \text{ ns}$ per row.

160 ns. The measurements are summarized in Figure 42; a dependence of the range on the readout speed can be seen for the scenario with lower biasing voltage VDDA.

THE GAIN of the ADC corresponds to the slope of the transfer curve and is specified in $\text{LSB}/\mu\text{A}$. The slope is taken from a straight line fit ($D = O + G \times A$, with Digital code, Analog input, Gain and Offset) to the central 95 % of the full ADC range; the measurements are shown in Figure 43. For the Belle II readout speed of $\approx 100 \text{ ns}$ per row and optimized biasing a gain of $10.18(4) \text{ LSB}/\mu\text{A}$ is found, while the total spread is $0.2 \text{ LSB}/\mu\text{A}$. This corresponds to a total gain variation over all channels of $\approx 2 \%$. The size of one LSB can be calculated to $98.2(4) \text{ nA}$.

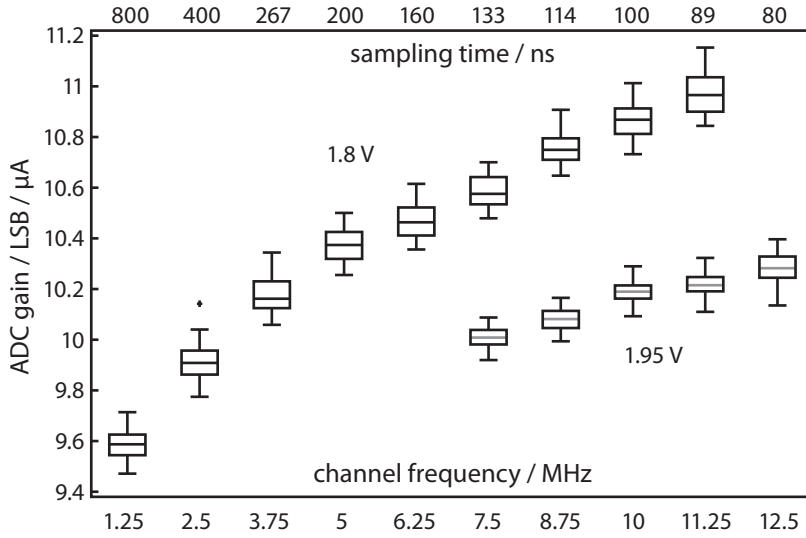


Figure 43: DCD2 ADC gain measured vs. sampling time.

THE IMPACT OF GAIN VARIATIONS is mainly on position reconstruction, where intrinsic DEPFET variations or variations caused by the readout chips act similarly. Intrinsic gain variations over DEPFET matrices have been measured previously: Esch [29] reports variations of 5 % to 10 % with source measurements, Kodyš et al. [52] finds up to 6 % in beam-test data and up to 4 % with source measurements. The impact on the position resolution of a gain error E_g can be estimated by $E_{\text{pos.res.}} \approx 0.5 E_g \times \text{pixel-pitch}$ (using a center-of-gravity calculation, from

[52]). For a gain error of 5 % and a pixel pitch of $50\text{ }\mu\text{m}$ an error on position reconstruction of $\approx 1.2\text{ }\mu\text{m}$ can be expected. Compared to the gain variations of the DEPFET devices, the variations of 2 % from the DCD2 are almost negligible. However, it is expected that future offline analysis software will implement gain corrections to improve the position reconstruction, and these corrections will also pick up any gain variations from the DCD-B channels.

OFFSET VARIATIONS are extracted from the straight line fits to the ADC transfer curves at mid-range, corresponding to an input current of $15\text{ }\mu\text{A}$, and are given in LSB. The offsets are mostly independent of the sampling time and biasing parameters (see Figure 44). Even though half (50 %) of the channels exhibit a total offset range of only ≈ 4 LSB, the distribution is dominated by outliers, resulting in a worst-case offset range of ≈ 18 LSB. This corresponds to $\approx 7\%$ of the full ADC range or to an input current variation of $\approx 1.8\text{ }\mu\text{A}$, which should be taken into account when the full dynamic range of a DCD2-based DEPFET system is under consideration (see Section 7.6). The offsets have been examined for any visible patterns corresponding to the chip geometry to exclude effects caused by IR-drop, however no such patterns could be found.

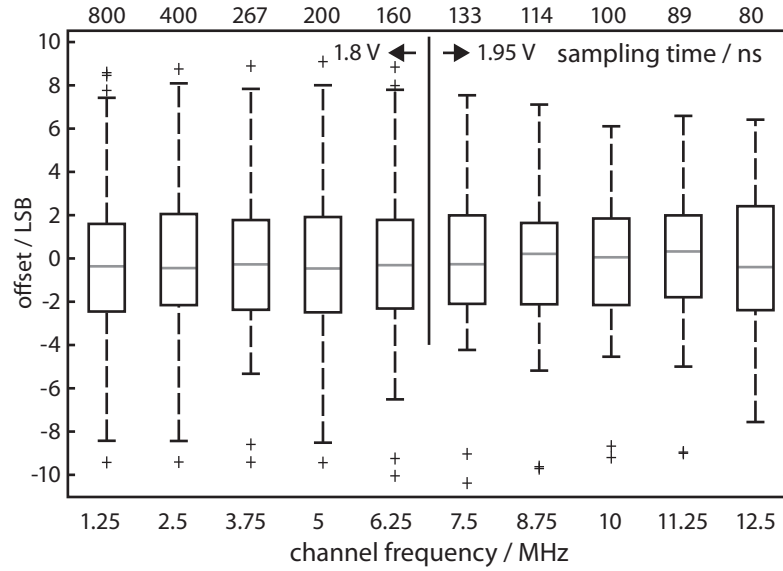


Figure 44: DCD2 ADC offsets measured vs. sampling time.

6.1.2 DNL

The differential nonlinearity (DNL) of the DCD2 ADC channels is measured as a function of the sampling time under two different biasing scenarios. A method called code density testing (also: histogram testing) [26, 67] is used and adopted for static measurements. A known input signal (current ramp as described above) is applied to the ADC, and the distribution of digital output codes is recorded in a histogram. The relative number of occurrences of the digital output codes is called *code density*. For an ideal ADC an equal number of codes are expected in each bin, as long as

the input signal is uniformly distributed. The instantaneous DNL_i (see Equation 4.6) is then related to the ratio of the measured bin width $H(i)$ to the ideal bin width Δ :

$$\text{DNL}_i = \frac{H(i)}{\Delta} - 1 \quad (6.1)$$

The ideal bin width Δ is determined by taking the average number of counts $\Delta = \frac{1}{n} \sum_i H(i)$, after a cut on the central 95 % range of the ADC transfer curve. This conveniently removes all edge effects (e. g. overflow bins, bins larger due to noise) and makes this method independent of the channel's individual gain and offset. To avoid aliasing (binning) effects the input current signal has to be applied in small steps — it can be argued that Gaussian noise present on the input actually helps this measurement by smoothing the input signal, leading to a more uniform signal distribution.

Two examples for the code density testing are shown in Figure 45, where two distinctly different bin width distributions lead to different instantaneous DNL histograms. The total dataset of the instantaneous DNL measurements is visualized in a boxplot in Figure 46, which provides a more comprehensive overview of the ADC performance than just stating the maximum DNL of each channel. The maximum values (cf. Equation 4.7) are summarized in Figure 47, where the mean maximum DNL value and the 1σ range of all 48 ADC channels are plotted. To summarize, the instantaneous DNL over all frequencies is generally — ignoring a few outliers — less than one, which guarantees a monotonic transfer characteristic.

The reasons for the high DNL values at short sampling times are easily identified when looking at the transfer characteristics of individual channels. Figure 48 shows as an example a step extending over current input ranges several LSBs wide, causing a higher code density in some bins. An explanation for these areas where wide codes are dominant can be found by comparison with Figure 25d. These issues can be mitigated for individual channels by changing biasing parameters, especially the RefIn supply voltage. It is however not possible to find an operating point at which all channels show perfect behavior.

6.1.3 INL

The integral nonlinearity (INL) of the DCD2 ADC channels is extracted from the measured transfer characteristics using the *best straight line INL* approach. As an example, the residuals from a single channel after subtracting the fitted line are shown in Figure 49 (see also Figure 80 on page 93). The residuals typically follow shapes that can be approximated by second or third order polynomials; some show larger steps corresponding to wide codes causing large DNL values (see Figure 48). The maximum (absolute) residual defines the INL, and is plotted in Figure 50. Since the INL gives a worst case scenario, this plot does not readily give any information about the average error and thus the average impact on the reconstruction of the incoming signal current. Especially in cases where the ADCs show singular areas with wide codes the INL might be

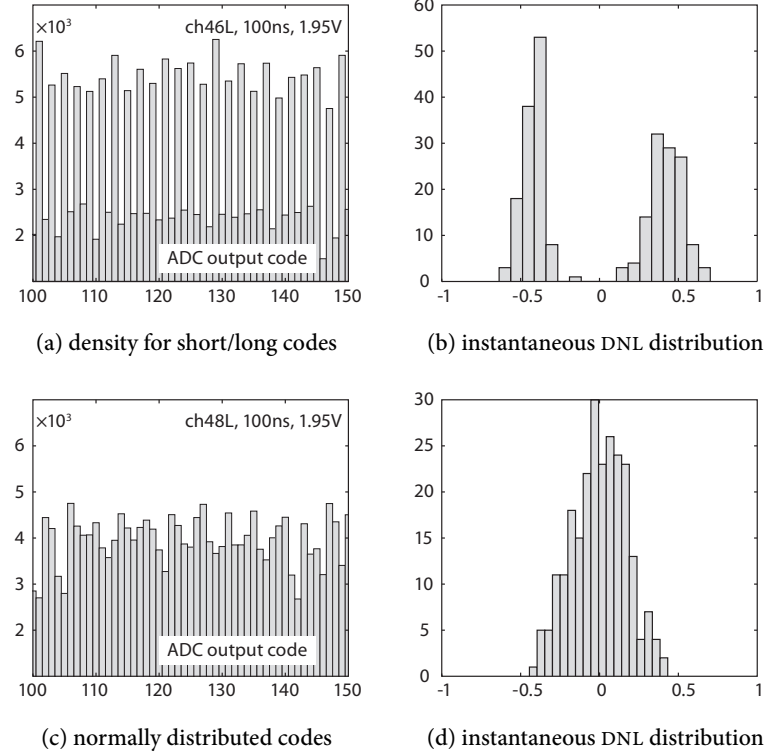


Figure 45: Two examples for code density (histogram) testing [26, 67] for DNL errors. The DCD2 has been operated with a sampling time of 100 ns and 1.95 V supply voltage. A linear input current ramp was provided and a total of 1.2×10^6 samples were recorded over the full ADC range.

(a) shows a histogram of one channel (46L, in the range of 100–150 for display) where short and long codes are alternating (see Equation 4.11). The instantaneous DNL distribution (b) shows two typical peaks at $\approx \pm \text{DNL}$.

(c) shows a different channel (48L) where the code bin widths follow a normal distribution resulting in the instantaneous DNL as shown in histogram (d).

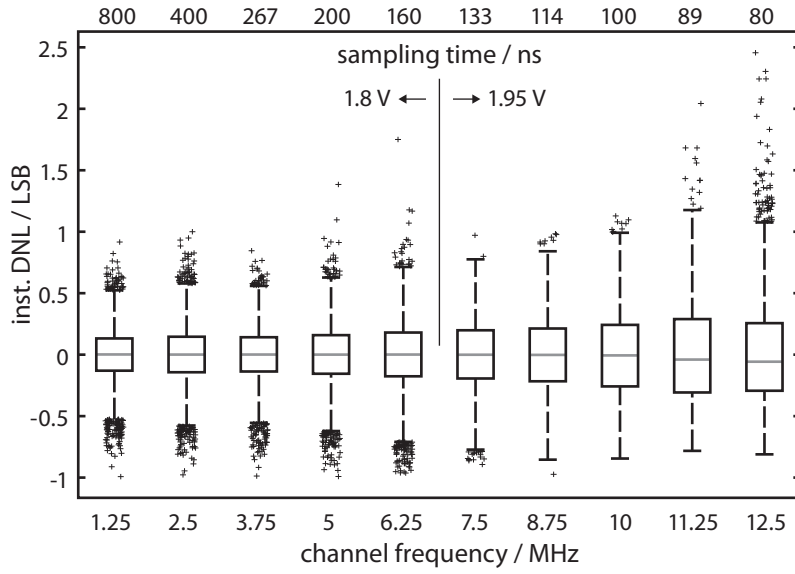


Figure 46: A boxplot visualizing the instantaneous DNL distributions for 48 DCD2 ADC channels vs. sampling time. For sampling times ≤ 133 ns the supply voltage of the DCD2 has been increased. The performance is almost stable over the whole frequency range, however an increasing amount of outliers for shorter sampling times lead to increased (maximum) DNL values.

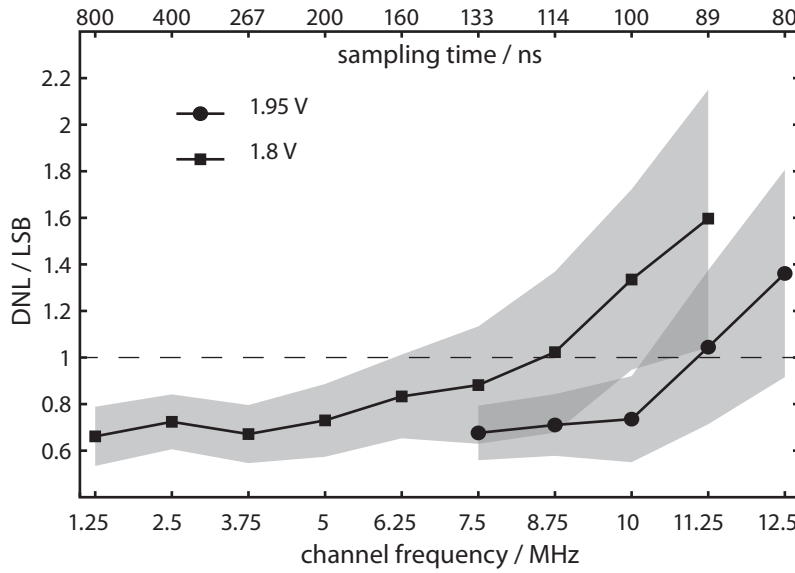


Figure 47: Summary of the maximum DNL values, extracted from [Figure 46](#). Plotted are the mean maximum DNL and a 1σ range from 48 individual ADC channels vs. sampling time. For a typical Belle II read out speed of ≈ 100 ns a $\text{DNL} \leq 1 \text{ LSB}$ is possible.

Figure 48: (example) Step in the transfer characteristics of channel 49L at a sampling time of 80 ns, causing a wide code and subsequently a large DNL error.

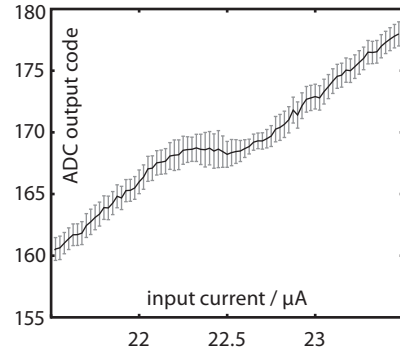
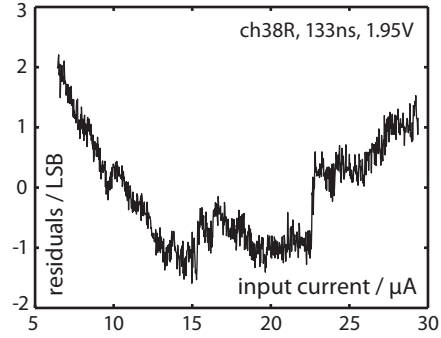


Figure 49: (example) Residuals after subtracting the best straight line fit from the ADC transfer curves, showing typical second or third order polynomial behavior, and a singular large step.



misleading. In [Figure 51](#) the combined (absolute) residual distributions of 48 ADCs are plotted as a function of the sampling time. The INL can again be identified by the outliers, while the residuals for the majority of the data points are much smaller. For a readout speed of 100 ns per row the mean (indicated by diamonds in the plot) and median of the residuals are ≈ 0.75 LSB, while the INL-defining outliers can be found in a range of 2.3 LSB to 3.4 LSB.

6.1.4 Static ADC noise

The noise of 48 individual ADCs is extracted over the central 95 % of the full ADC range as a function of the sampling time. All channels were operated with the same biasing settings; no additional cuts on the data were made. The noise is specified in nA, calculated by taking the channels' individual gain into account. All individual noise values⁸ are recorded in [Figure 52](#). Except for the fastest readout speed the mean noise is in the order of ≈ 50 nA (≈ 0.5 LSB) with few outliers extending beyond 1 LSB of noise. For a typical Belle II readout speed (100 ns) a mean noise of 54 nA is observed, corresponding to a DEPFET ENC of $\approx 108 e^-$ (assuming a

⁸ A note on calculated noise values:

Calculating the standard deviation of data points $s = \left(\frac{1}{n-1} \sum_{i=1}^n (x_i - \bar{x})^2 \right)^{\frac{1}{2}}$ when strong binning effects are expected (which is the case with our ADCs) can lead to interesting numerical results in special cases. (Valid for large n .) If the data points are equally distributed in two neighboring bins b and $b+1$, a standard deviation of $s = 0.5$ is expected. A symmetric distribution over three bins with a fraction f of the counts in the central bin b and the remaining $\frac{1}{2}(1-f)$ counts each in the bins $b-1$ and $b+1$ results in $s = \sqrt{1-f}$. An equal distribution over two bins $b-1$ and $b+1$, where the middle bin b is empty (missing ADC code), results in $s = 1$. A detailed look at noise values and their statistics can thus help identify problems.

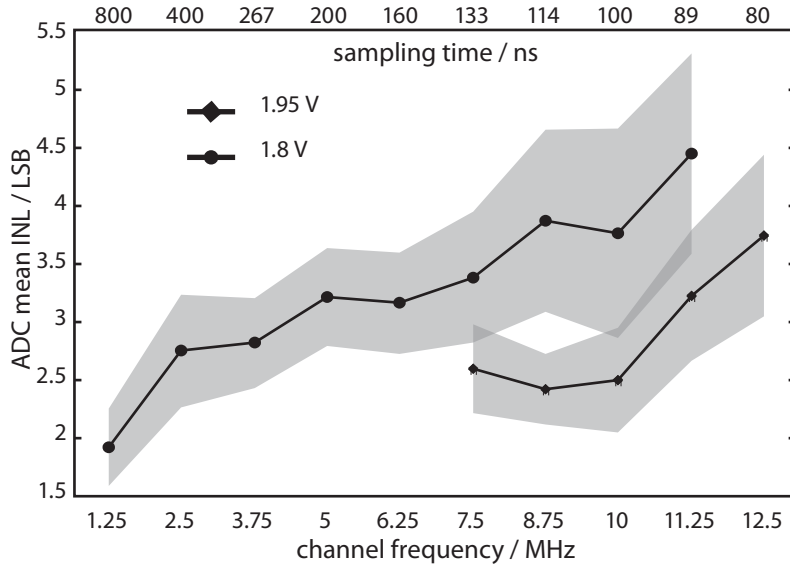


Figure 50: Measured INL of DCD2 ADC channels vs. sampling time for two different biasing scenarios (1.8 V: ●, 1.95 V: ◆). The average INL and the 1 σ -range of 48 channels is shown. An increase of the INL is observed for decreasing sampling time, which can be slightly improved by changed bias settings (more power consumption).

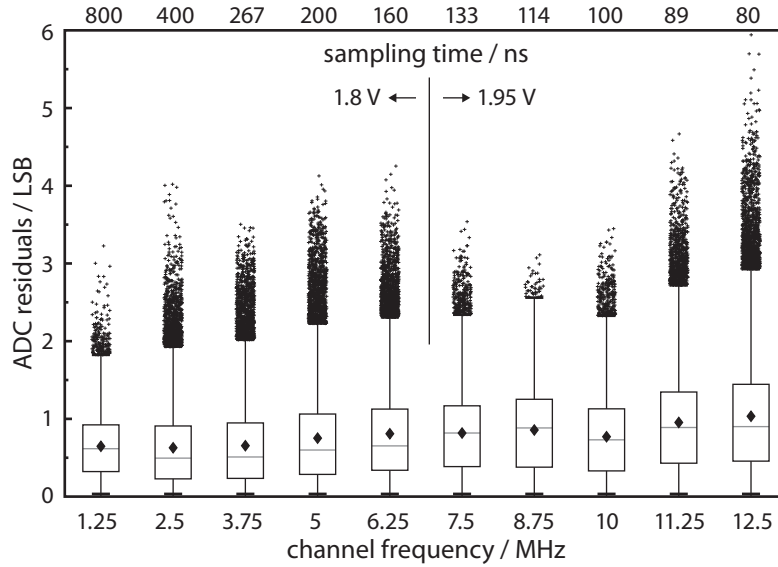


Figure 51: Measured ADC residual distributions vs. sampling time. The mean of the distributions is marked with a black diamond (◆). The mean residuals are, consistent over the operating frequency, less than 1 LSB, while $\approx 99\%$ of all residuals are less than 2 LSB. The INL-defining outliers, however, extend to extreme regions. Each boxplot contains $\approx 55 \times 10^3$ data points.

DEPFET $g_q = 500 \text{ pA/e-}$). An increase in noise, however, is expected once external capacitive loads (e. g. DEPFET drain lines) are connected to the DCD2 inputs.

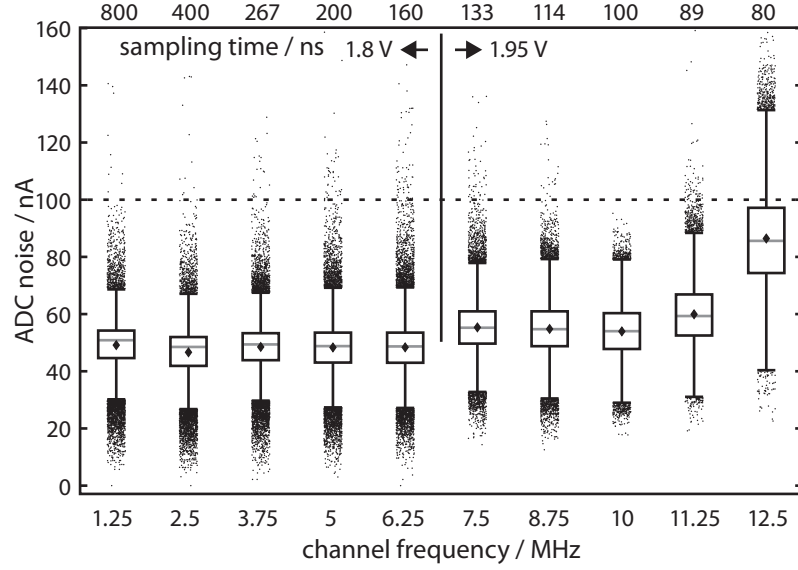


Figure 52: Measured DCD2 ADC noise distributions vs. sampling time, specified in nA after division of LSB values by individual channel gains. The mean of the distributions is marked with a black diamond ($\blacklozenge$), a dashed line (— —) indicates the value of ≈ 1 LSB. Each boxplot contains $\approx 45 \times 10^3$ data points; a few outliers for sampling times ≤ 89 ns are clipped to 160 nA for improved display. Note that if the noise is expressed in LSB and the readout speed dependent gain is not considered, the noise shows a stronger monotonic rise with faster sampling speeds (cf. Figure 43).

6.1.5 Effective ADC error

How good can an incoming current signal be reconstructed after it has been digitized by the ADC? This question summarizes the effects of all measurements shown in the previous section, and includes all systematic and statistical errors. Based on the recorded datasets a reconstruction is performed: For each digital ADC output code the corresponding input current is reconstructed using the inverse of the straight line fit function, and the difference (i. e. the error) of the result and the real input current is recorded. Data is taken within the central 95 % of the ADC range, yielding $\approx 1 \times 10^6$ data points per ADC, and $\approx 48 \times 10^6$ for all channels per readout speed. The resulting error distributions are shown as an example for one readout speed as a histogram in Figure 53, and as boxplots for all readout speeds in Figure 54. The root mean square (RMS) of these distributions is recorded in Table 2, and specified both in nA and LSB by taking the channel's individual gain into account. For typical Belle II readout speeds the total 1σ error is in the range of 110 nA (1.1 LSB), which is in good agreement with a quadratic sum of the noise and mean residuals as shown above. For the final use of these ADCs the question arises if it is worthwhile to keep the LSB for data transmission or storage since it

has no real information content, unless more sophisticated methods for calibration and reconstruction are used (e. g. a cubic fit function instead of linear).

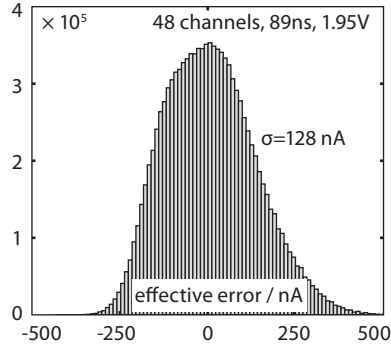


Figure 53: Example histogram of current reconstruction errors in nA, for all channels at 89 ns sampling time. The shape depends on the ADC transfer function and is not necessarily Gaussian.

Table 2: Effective ADC errors, given as 1σ values from Gaussian fits to the distributions shown in Figure 54.

sampling time ns	effective 1σ error	
	nA	LSB
800	94	0.9
400	92	0.9
267	96	1
200	104	1.1
160	109	1.1
133	111	1.1
114	113	1.1
100	106	1.1
89	128	1.3
80	152	1.6

6.1.6 Regulated cascode noise with input capacitance

Connecting a large DEPFET sensor to DCD2 inputs will introduce an additional capacitive load in the order of 50 pF. This will have an impact on the noise performance of the DCD2 and also on dynamic aspects, like readout speed and signal rise times. A special setup has been created (see Figure 55) which allows the connection of various input capacitors⁹ to the DCD2. The used capacitor values are 4 pF, 7 pF, 10 pF, 15 pF, 18 pF, 22 pF, 30 pF, 43 pF, 47 pF, 68 pF and 82 pF which are connected to one DCD2 channel each, which allows averaging over only two ADCs in this case. Unconnected DCD2 channels provide a reference for zero input capacitance. The noise vs. connected capacitance has been measured for

⁹ Used capacitors: MURATA MLCC capacitors, C0G-dielectric, GRM15 series, specified tolerance $\pm 5\%$.

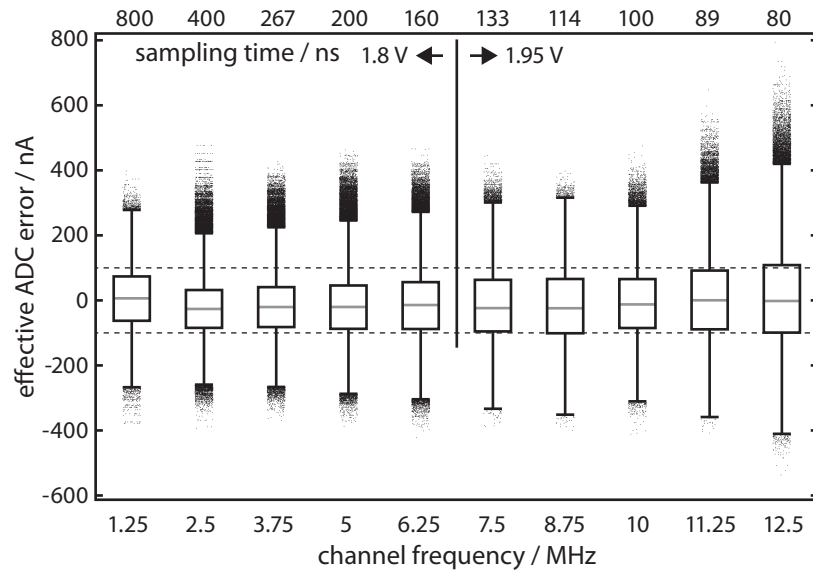
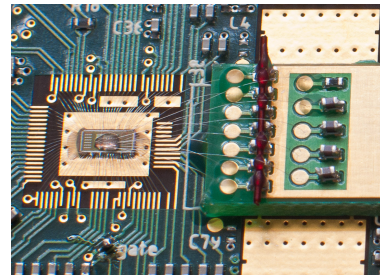


Figure 54: Boxplots of current reconstruction distributions vs. readout speed, specified in nA. This plot combines the noise and non-linearity of the ADC, showing the *effective errors* which are expected if real measurements are taken. This scenario assumes a straight line fit to the ADC transfer curve and can possibly be improved further by fit functions of higher order. (Due to the discretization of the ADC some banding effects can be seen in the outliers.) Dashed lines (---) indicate the value of $\approx \pm 1$ LSB.

Figure 55: Capacitive loads have been bonded to DCD2 input channels to allow parametric noise and speed measurements. A total of 11 capacitors with C0G-dielectric from 4 pF to 82 pF are used.



several readout speeds (800 ns, 160 ns and 89 ns), and as in the previous measurement (Figure 52) no significant readout speed dependency was found. The data for a sampling time of 160 ns is plotted in Figure 56 as a function of the attached capacitance. For values up to ≈ 30 pF the measured noise increases to ≈ 75 nA ($\approx 150 e^-$), and stays constant for higher values.

The question if a DEPFET device with a given drain capacitance can be read out at these noise values is, however, still pending further investigations for *dynamic* behavior of the DCD2 chip — specifically the settings of the regulated cascode need to be adjusted for the required input bandwidth. Comparable measurements with a dynamic input signal can be found in Section 6.2.

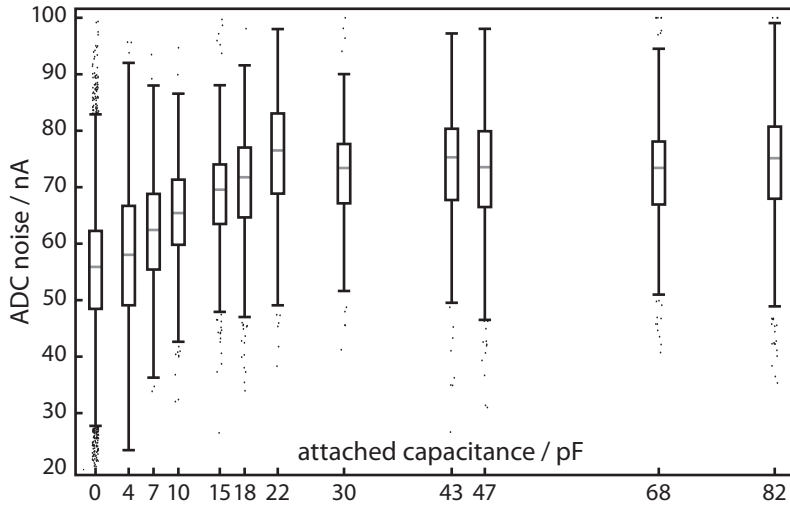


Figure 56: Measured DCD2 regulated cascode noise distributions vs. attached input capacitance, for a sampling time of 160 ns, specified in nA, data taken with the on-chip ADCs. The regulated cascode was operated with default biasing settings for these measurements (1.95 V supply, see also Table 1).

6.2 DYNAMIC MEASUREMENTS

Reading out a DEPFET matrix in ≈ 100 ns per row requires the DCD2 to fulfill also dynamic performance specifications. The settling time of the changing input signal needs to be significantly shorter than the sampling time, including the case where a large (≈ 50 pF) capacitance is present at the inputs. The performance of the regulated cascode (see Section 4.2) can be tuned to achieve the required settling time without overshoots or oscillations, and to optimize noise and power consumption. For the following measurements, a $5 \mu\text{A}$ current step is generated using the on-chip test current sources¹⁰ and fed into the ADC channels through the regulated cascode. A special sampling technique outlined in the following Section 6.2.1 is used to record detailed current waveforms (see Figure 21 on page 25 for an example); offline analysis software is used to extract rise

¹⁰ An external current step supplied over the monitor bus cannot achieve a steep enough rise time due to parasitic capacitive loads.

time and electronic noise of the signals. The 48 used ADCs are usually operated at their mid-point, by adjusting the static on-chip current sources, to prevent clipping or distortion of the applied current step.

6.2.1 Time resolved measurements with the DCD

The DCD2 can, at its peak performance, take one data sample every 80 ns which is then converted to an 8-bit digital value by two cyclic ADCs working interleaved with a conversion time of 160 ns each. Achieving a better *real time* resolution for random input signals, as e. g. a high bandwidth oscilloscope would provide, is not possible. However, if the input signal is periodic and stable, a technique called *sequential sampling* [97] can be used to record continuous time waveforms with improved *equivalent time* resolution. The basic idea is shown in Figure 57 and follows these steps:

- ◆ from a repetitive input a single sample is taken
- ◆ the sampling point is shifted in time by a step Δt
- ◆ individual samples are assembled to form a composite waveform
- ◆ averaging can be used to suppress electronic noise

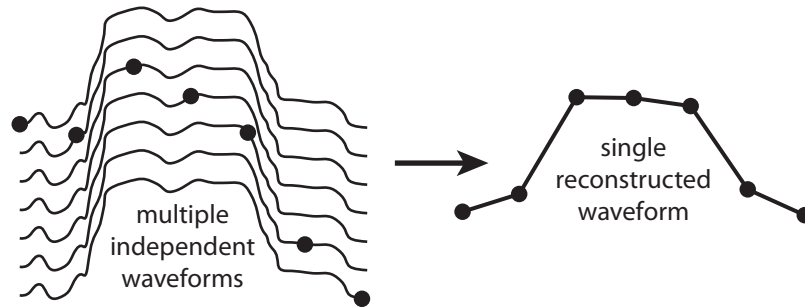


Figure 57: Sequential sampling with the DCD2. Multiple repetitive, independent waveforms and time-shifted sampling points are used to reconstruct a signal with good timing resolution.

The time resolution can be as good as ≈ 830 ps and depends on the DCD2 speed, the intrinsic DCD2 risetime, and the software/firmware implementation (see Section 5.3.2). This technique is used for rise time measurements, time resolved DEPFET drain current measurements, investigation of capacitive charge injection, and has become an invaluable tool for setting optimal sampling points in high speed DEPFET sensor readout.

6.2.2 Regulated cascode performance

The dynamic performance of the cascode is directly influenced by the power given to the cascode amplifier. The user-adjustable parameters are the amplifier supply voltage VCAVSS, the main biasing currents CascAmpBias and CascAmpLoad, and CascAmpSF to fine tune the settling behavior. A multi-dimensional parametric scan has been performed over these parameters, varying the DAC-values of CascAmpBias and CascAmpLoad

each from 100 to 1000 in steps of 25, for two VCAVSS supply voltages 0.95 V and 1.05 V. For the selected measurements shown here an optimal operating point with both CascAmpSF and CascAmpLoad adjusted to 250 is chosen. The DCD2 is operated with a supply voltage of 1.95 V at a sampling speed of 160 ns. This sampling speed has been chosen to provide small enough time steps for the sampling procedure described above, but also a large enough time window to allow complete settling of the incoming current step. The static measurements in [Section 6.1](#) show that no significant increase in noise or effective error is expected when increasing the readout speed to 100 ns.

The rise time¹¹ of the input current signal is measured as a function of cascode power consumption (CascAmpBias) and as a function of the connected input capacitance. Waveforms are recorded with a time step precision of 1.66 ns, each point is an average of 1000 individual ADC samples. The fall time of the input signal is measured as well, and resulting values are averages from two ADCs connected to each capacitor. The measurements are shown in [Figure 58](#) for selected capacitance values (0 pF, 22 pF, 43 pF and 68 pF).

For a large input capacitance of 68 pF a rise time of ≤ 25 ns can be achieved with a cascode power consumption of ≈ 1 mW per channel, corresponding to a CascAmpBias current of ≈ 900 μ A. Complete settling of the signal happens after multiple time constants, depending on the precision¹² required. The rise time approaches a lower limit of 20 ns for high power which is given by the intrinsic rise time of the current memory cells.

The same data set is used to extract the noise performance, as a RMS of the ADC output after the input signal has settled. As shown in [Figure 59](#), the noise increases both with cascode power and input capacitance. A comparison with the static measurements in [Figure 52](#) shows that an increase in noise from ≈ 70 nA to ≈ 110 nA has to be tolerated if settling times ≤ 25 ns are required.

To summarize, complete settling of an input signal to 1 % with a capacitive load of ≈ 60 pF can be achieved in ≤ 50 ns with a per-channel power consumption of the regulated cascode of ≈ 1.2 mW and a noise of ≈ 110 nA (≈ 1.15 LSB, ≈ 220 e⁻).

¹¹ The *rise time* t_r refers to the time required for the signal to change from the lower 10 % to the upper 90 % of the total step height. For a one stage RC network with an exponential response the rise time is proportional to the time constant $\tau = RC$, with $t_r = \tau \cdot \ln 9 = \tau \cdot 2.197$.

¹² A note on *complete settling*, assuming a one stage RC behavior, and $t_r = 25$ ns: The signal settles to 10 % of the final value in 2.3τ ($\equiv 1.05t_r = 26$ ns), to 5 % in 3τ ($\equiv 1.36t_r = 34$ ns), to 1 % in 4.6τ ($\equiv 2.09t_r = 52$ ns), and to 0.1 % in 6.9τ ($\equiv 3.13t_r = 78$ ns).

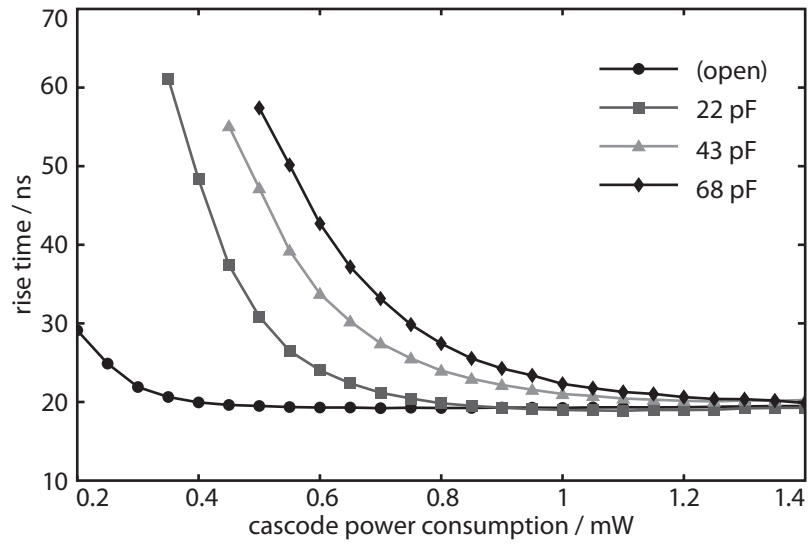


Figure 58: The rise time of a $5\ \mu\text{A}$ input current step function is measured as a function of the regulated cascode biasing (power consumption) and of the connected input capacitance. Data points are omitted for high capacitance and low power if complete settling could not be achieved in $\leq 80\ \text{ns}$. The measurement errors are $\pm 1.8\ \text{ns}$ for channels with capacitors, $\pm 1.0\ \text{ns}$ for the combined results of 12 open channels.

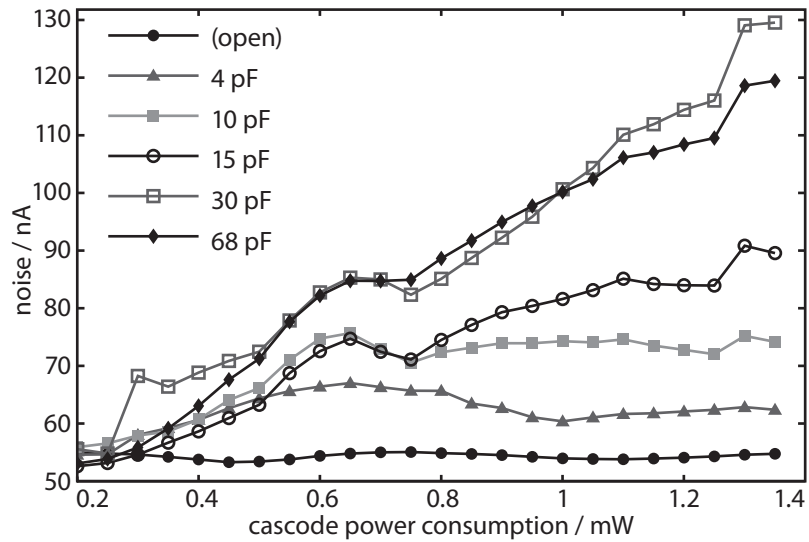


Figure 59: The ADC RMS noise of a $5\ \mu\text{A}$ input current step after complete settling is measured as a function of the regulated cascode biasing (power consumption) and of the connected input capacitance. For capacitances $\geq 30\ \text{pF}$ no further noise increase is observed, consistent with [Figure 52](#).

DEPFET PERFORMANCE MEASUREMENTS

A successful operation of a DEPFET sensor connected to a DCD2 readout chip is an important step towards a functional Belle II system. The DCD2 based readout system has been connected to two different DEPFET sensor assemblies (see [Figure 37](#) and [Figure 38](#) on [page 49](#)), which are used for the following measurements. Even though only a limited number of connected channels are available in this prototype system, all important performance verifications can be done: The maximum readout speed of a sensor is established, limiting factors and technical pitfalls are explained, and a source measurement with ^{241}Am is shown to prove the functionality of the whole system. As a result of the readout speed measurements, switching from double sampling to the faster single sampling readout mode is motivated, which can cope with the speed requirements for Belle II. Furthermore, the DCD2 allows for a first time a detailed look at unmodified¹ DEPFET drain currents with high statistics; a direct look at pixel pedestals and noise statistics can be taken. This chapter closes with an estimate of the digital resolution limits of the readout chain.

7.1 DEPFET READOUT TIMING

What is the maximum achievable readout speed of a large DEPFET sensor? Since this question (or rather its answer) has far reaching consequences for the DEPFET module layouts, the frame time, and the hit occupancy, a detailed investigation is needed. A typical readout sequence (see [Figure 7](#) on [page 12](#)) in double sampling mode requires time for sampling I_d twice and for the clear process. A minimum sampling time limit of ≈ 35 ns could be established with the previously shown DCD2 measurements, where an input signal rise time of ≈ 25 ns was measured. Given a minimum clear time of ≈ 20 ns (cf. [90], and including some safety margin for lower clear voltages), an approximate minimum readout time of 90 ns could be expected for a double sampling sequence. Also no further dependence on the input capacitance is expected, if enough power is spent in the regulated cascode circuit (shown in [Figure 58](#)). On top of this minimum timing budget of ≈ 90 ns further effects need to be added. Should the DEPFET output current I_d not behave like an ideal step function the required settling time will increase. Uncorrelated jitter present on the SWITCHER or DCD2 clocks further increases the required error margins. Last but not least, the drain lines of a long DEPFET device exhibit their own signal rise time² of ≈ 10 ns.

- ¹ The previously used readout chip, the CURO [101, 102], performed a mandatory on-chip CDS, which made the direct inspection of DEPFET drain currents impossible.
- ² Extraction of parasitic resistance and capacitance of a Belle II DEPFET module done by Koffmane [54] show a resistance of a drain line of $215\ \Omega$ with a total capacitance of 50 pF, yielding a rise time of ≈ 10 ns. (In case of a distributed RC-line the rise time is $\approx RC$ [see 16].)

7.1.1.1 Measurement procedure

A direct look at the DEPFET drain currents is possible with the DCD2 readout chip, using the sequential sampling technique outlined in [Section 6.2.1](#). The settling behavior of I_d includes the input rise time of the DCD2, therefore the measured signals are perceived as through a low pass filter. A complementary measurement has been done with a high bandwidth transimpedance amplifier without the use of the DCD2 and is shown in [Appendix A](#).

THE WAVEFORMS in the following plots show the recorded drain current I_d of a DEPFET matrix under normal operating conditions centered on the full sequence for a single pixel; the waveforms of the previous and next pixel are shown partially at the sides. Each waveform is recorded with 128 equidistantly spaced time points, the sequence for a single pixel fills $\frac{3}{4}$ of this range. The time resolution can be calculated to $\text{row-time}/96$. Each point is sampled 1000 times (i. e. the SWITCHER has to cycle 1000 times through the matrix) and averaged. Obviously, single signals (e. g. from a radioactive source) cannot be visualized with this method; leakage current and continuous signals (e. g. from a well triggered laser, or ambient light) can be seen. The zero points for the time axis and the measured currents are arbitrary. To provide a consistent display in the following plots, the time zero point is shifted to the gate-on position (i. e. activation of the displayed pixel). For the measured DEPFET output current, the zero point is shifted to the latest sampling point³ for all displayed pixels. The recorded waveform of a randomly chosen single pixel is displayed as a single black line, where the width of the line indicates the RMS of 1000 individual samples. In all but the first plot, the waveforms of all other⁴ read out pixels are shown in a gray scale density plot in the background. This gives additional information for worst case settling times, and also shows differences and similarities between the DEPFET pixels.

7.1.2 Results

A very slow readout with $t_{\text{row}} = 1.5 \mu\text{s}$ is shown in [Figure 60](#), where also the SWITCHER operations are added as a visual aid. Already a few notable things happen: During the clear operation I_d is reduced due to the internal gate of the DEPFET transistor becoming more positive after coupling to the $V_{\text{clear, high}}$ voltage. Also, while switching from one row to the next, a sudden drop in I_d is visible; the SWITCHER uses non-overlapping gate signals and causes a situation in which the DEPFET transistor in one pixel is already off while the next transistor is not yet conducting.

Switching to a faster readout allows the direct measurement of I_d settling times. A readout sequence with $t_{\text{row}} = 200 \text{ ns}$ is shown in [Figure 61](#), where settling times (after switching the gate of the DEPFET transistor

³ The latest sampling point is the second sample after clearing for double sampling, or the first sample for single sampling.

⁴ For these measurements, 768 pixels on the COG LE and 394 pixels on the COG SA device were used.

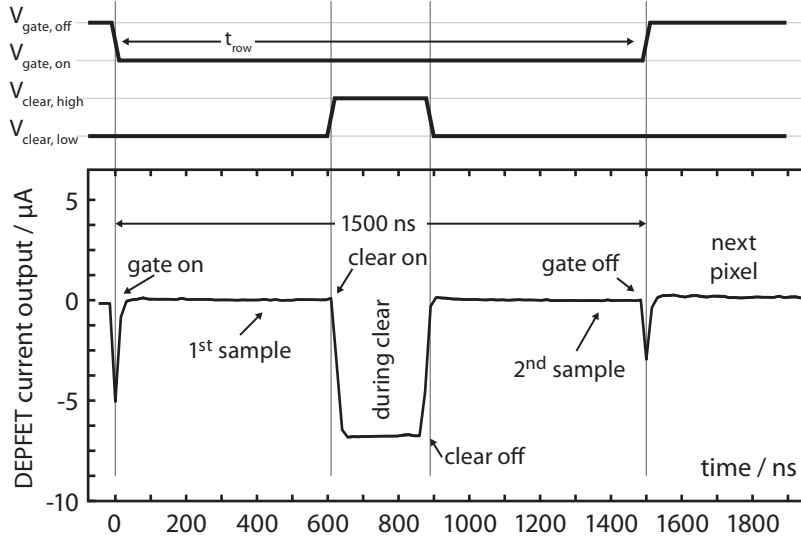


Figure 60: A slow (1500 ns per row) measurement of DEPFET drain output current in a double sampling scenario for a COG LE device, recorded with the DCD2 using sequential sampling. A single, random pixel has been chosen for this plot. The steering signals of gate and clear SWITCHER are shown on top, see also Figure 7 on page 12. During the clear operation, the internal gate of the DEPFET transistor couples to the $V_{\text{clear, high}}$ voltage, becomes more positive, and I_d is reduced. Switching from one row to the next is done with non-overlapping gate signals and causes a situation in which the DEPFET transistor in one pixel is already off while the next transistor is not yet conducting — a drop in I_d is visible.

on or after switching the clear process off) of ≈ 50 ns can be extracted. This gives a limit on t_{row} of ≈ 120 ns for double sampling readout, which is shown in Figure 62. Further noticeable are over- and undershoots in the measured current at the start and the end of the clear process, these can be explained by capacitive charge injection while switching (see Section 7.3.2).

If the readout time is reduced to ≈ 90 ns (see Figure 63) I_d no longer settles completely⁵. A solution to speed up the DEPFET readout and decrease the minimum t_{row} even further is a switch to single sampling. In Figure 64 the second sampling point is omitted and the clear strobe is moved to the end of the cycle. The benefits of CDS like $1/f$ noise suppression and dynamic range reduction are sacrificed for a faster readout; pedestal corrections need to be implemented offline now, either in software, or in the proposed zero-suppression chip DHP for the readout of the Belle II DEPFET modules. With single sampling the readout speed could be increased even further to $t_{\text{row}} = 60$ ns for this COG LE device.

The measurements have been extended to a large COG SA DEPFET device. From an electrical point of view, the larger matrix geometry leads to higher capacitive loads at the DCD2 inputs and on the SWITCHER outputs, which will slow down gate and clear switching. A different pixel geome-

⁵ It could however be possible to sample on the rising edge of the signal, and perform an offline correction for this incomplete settling, if the behavior of the output current remains stable over longer timescales.

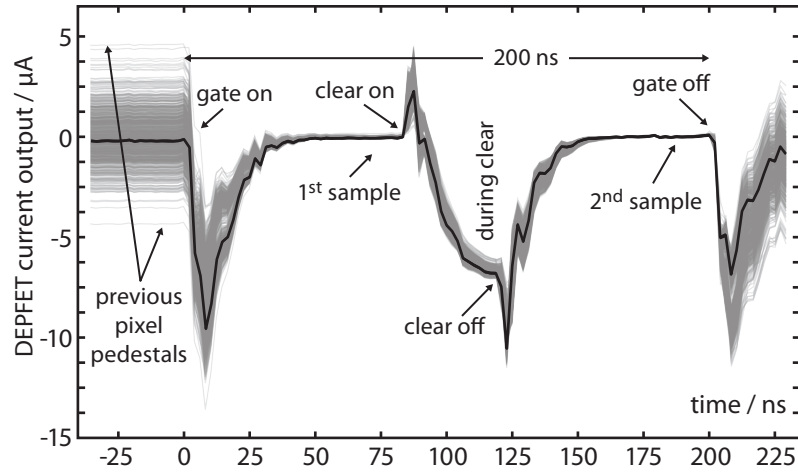


Figure 61: Measurement of DEPFET drain output current in a double sampling scenario with a row time of 200 ns, where a clear time of 40 ns has been chosen. The drain current drops by $\approx 10 \mu\text{A}$ directly after gate switching. Settling is achieved after gate switching or switching the clear off in 50 ns for all visible channels. This gives a direct limit on the row time in double sampling mode for this small COG LE DEPFET device: $t_{\text{row}} \geq 100 \text{ ns} + t_{\text{clear}} + \Delta \approx 120 \text{ ns}$, where Δ accounts for additional safety margins needed.

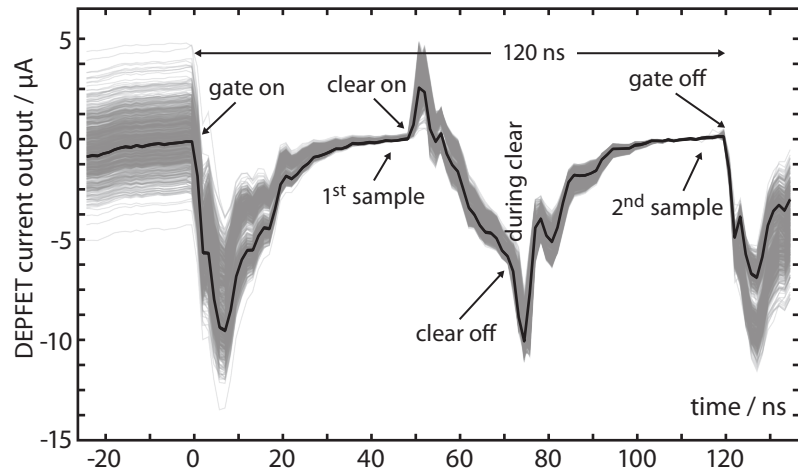


Figure 62: Measurement of DEPFET drain output current of a small COG LE device in a double sampling scenario; the minimum possible row time of 120 ns for complete settling has been chosen according to Figure 61, with a minimum clear time of $\approx 20 \text{ ns}$ (cf. [90]). The noticeable over- and undershoots at the start and the end of the clear operation are due to capacitive charge injection and explained in Section 7.3.2.

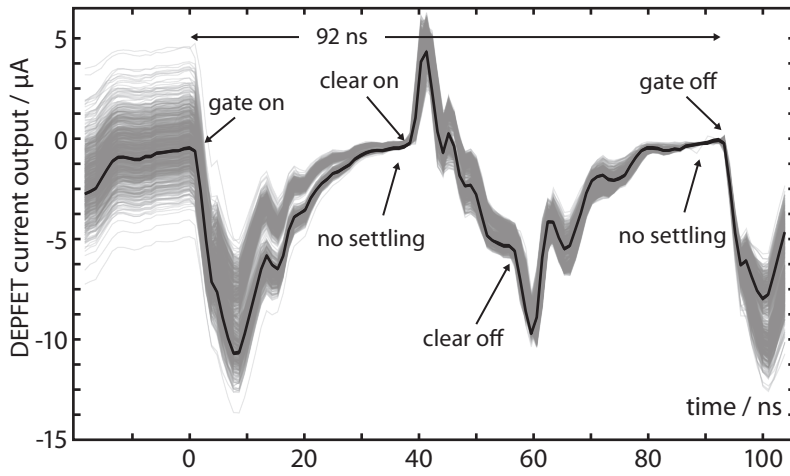


Figure 63: Measurement of DEPFET drain output current of a small COGGL device in a double sampling scenario, the row time has been further reduced to 92 ns. Complete settling is not achieved (remaining slope at sampling points).

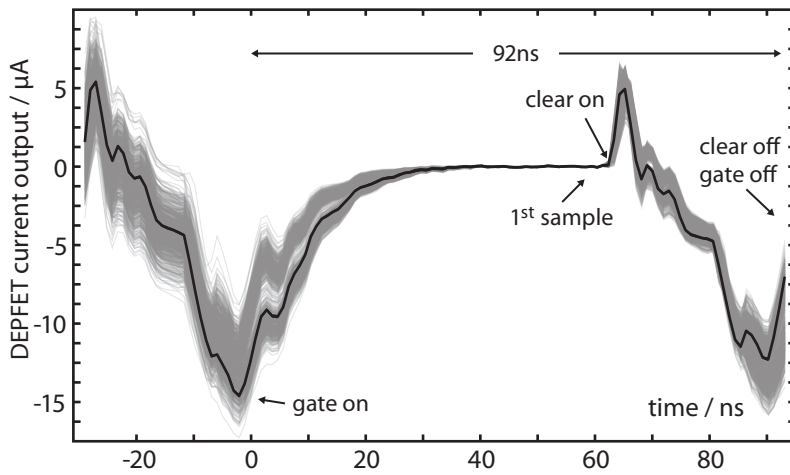


Figure 64: Measurement of DEPFET drain output current of a small COGGL device in a *single* sampling scenario, with a row time of 92 ns. The clear strobe is moved to the end of the sequence, only a single sample is taken. In this operating mode — given a faster readout chip — the frame time could be reduced further by ≈ 30 ns to ≈ 60 ns without compromising signal settling.

try compared to the COGGLE device leads to different capacitive charge injections. For $t_{\text{row}} = 160$ ns the I_d waveforms are shown in Figure 65, and as expected, the switching and charge injection artifacts are more pronounced. Settling of the drain current happens, similar to the small device, within 50 ns for all channels. For $t_{\text{row}} = 90$ ns in Figure 66 settling is no longer achieved, and here also changing to a single sampling readout helps as shown in Figure 67.

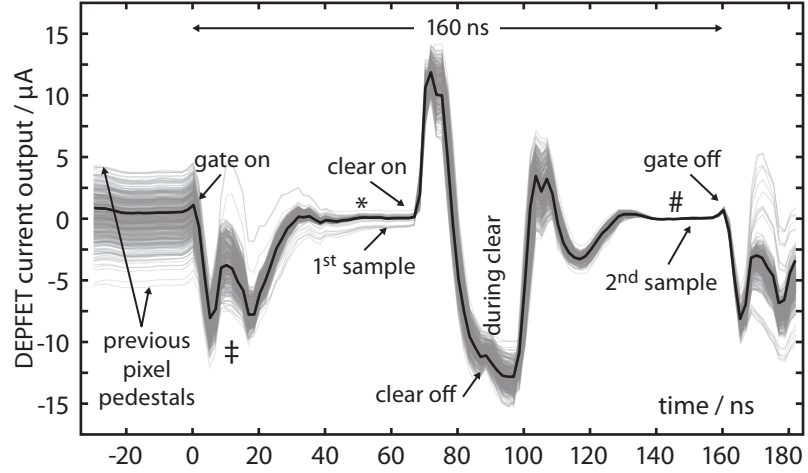


Figure 65: Measurement of DEPFET drain output current of a long COGSA device, double sampling, with a row time of 160 ns and clear time of 20 ns. Even though the current drop and capacitive charge injections are more pronounced compared to the COGGLE matrix, the settling times are almost the same. After gate-on or clear-off, settling (to points marked with * and #) is achieved within 50 ns, setting a similar row time limit of ≥ 120 ns for readout. At the point ‡ the drain current drops (twice) due to gate switching.

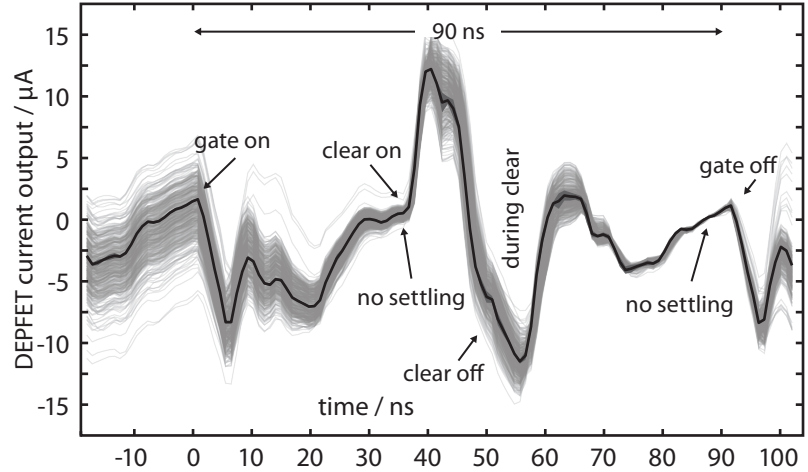


Figure 66: Measurement of DEPFET drain output current of a long COGSA device, double sampling, with a row time of 90 ns. Settling is no longer achieved.

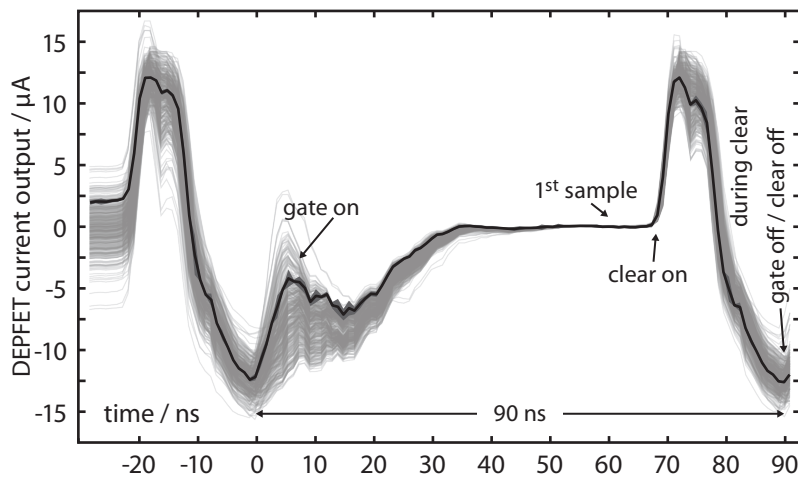


Figure 67: Switching to single sampling for the fast readout of the COGSA device produces a ≈ 30 ns time window for sampling in case of a 90 ns row time. For a Belle II scenario with a row time of 105 ns, the power consumption of the regulated cascode (or resistive current receiver, see [Section 4.7](#)) can be reduced significantly.

7.1.3 Consequences

Let us recapitulate the key differences between single sampling and double sampling readout of a DEPFET sensor, considering the measurements above; and the consequences for the proposed readout scheme of a Belle II DEPFET module, and the timing requirements for the Belle II readout.

READOUT SPEED The achievable row time is limited by signal settling times and the clear process:

- ♦ single sampling allows row times ≤ 105 ns down to ≈ 60 ns, including a ≈ 20 ns clear. The current DCD2 implementation can handle speeds up to ≈ 90 ns, limited by the ADC performance.
- ♦ double sampling limits row times to ≥ 120 ns with twice complete settling of I_d , including a ≈ 20 ns clear.

The proposed⁶ row time for the Belle II DEPFET modules is ≈ 105 ns, which makes a single sampling readout mandatory. Considering that the readout performance of the final Belle II DEPFET modules is yet unknown, it is wise to include some safety factor for the row time.

NOISE The suppression of various noise sources differ:

- ♦ double sampling suppresses low frequency ($1/f$) noise of *individual* DEPFET pixels and *individual* DCD2 channels. The $1/f$ noise of the DEPFET is very low [89] and can be ignored.
- ♦ double sampling can cope with unstable (over time) pixel pedestals, although stable pedestals are expected.
- ♦ single sampling can reduce the noise of the readout chip by a factor of $\approx \sqrt{2}$, since only one current memory cell (instead of two) contribute to the ADC input.
- ♦ in single sampling there is still time to spare: the power consumption of the regulated cascode can be reduced from 1 mW to 0.5 mW per channel, resulting in a reduced input bandwidth and less noise (see Figure 59). The total power consumption of a Belle II half-module would reduce by ≈ 0.5 W.

Low frequency noise components *common* to all read out pixels or DCD2 channels will be corrected for by the common mode correction either in the DHP or offline; this includes noise sources on the DEPFET power supplies or due to electromagnetic pick-up. In total the gain in noise performance due to double sampling will be insignificant compared to the noise of the readout chip; a well-designed input stage with a single current memory cell will even provide a better total noise performance in single sampling mode.

⁶ While earlier proposals assumed a possible row time of ≈ 80 ns, measurements done in this thesis and limits to the DCD2 ADC performance lead finally to an increased readout time target of ≈ 105 ns as specified in the Belle II Technical Design Report.

DYNAMIC RANGE The required input range for the DCD-B readout chip differs significantly:

- ♦ In single sampling the required input range of the digitization stage is maximal, and given by the maximum sum of pedestal spread, signal, and noise. A range of up to $\approx 75 \mu\text{A}$ should be considered for the design.
- ♦ In double sampling mode, the pedestals are removed before digitization, and the remaining signal and noise contributions fit comfortably within a $16 \mu\text{A}$ range of the ADC.

The consequences for single sampling are severe, since the pedestals need to be subtracted before any zero suppression. The DCD-B and DHP implementations become more complex to accommodate extra circuitry for pedestal subtraction and pedestal range compression (cf. [Section 7.6.2.1](#)). With the current concept, the number of inputs / outputs required between these chips increases by 25 %, the DHP needs additional memory (2 bit per pixel), power, and area. Even more importantly, the signal resolution in single sampling is notably lower than in double sampling mode, since the ADC range is used inefficiently.

PROCESSING Data processing and offline corrections:

- ♦ Single sampling requires extra pedestal processing and storage memory in the DHP.

However, both single sampling and double sampling modes need further online/offline processing and corrections of the data. A common mode correction removes the common part of integrated leakage current, pickup, or noise on power supplies. A pedestal correction is needed for individual DEPFET pixel leakage currents, and for individual DCD-B channel sampling offsets. Gain corrections are to be implemented for gain differences of DEPFET pixels and DCD-B channels. Finally, an offline non-linearity correction for the ADCs can be performed based on calibration data.

TO SUMMARIZE, single sampling readout is required due to the timing requirements; the consequences regarding dynamic range and required processing steps of the data are dealt with using special circuits and algorithms in the DCD-B and the DHP.

7.1.3.1 *Options to save double sampling*

There are two obvious ways to keep double sampling operational: First, increase the row time to $\approx 120 \text{ ns}$ which is considered safe for double sampling under similar conditions as the measurements done here, which would require either less pixels or larger pixels in z -direction; secondly, find a way to gain additional time for the second sampling during the 105 ns readout. Since the pixel sizes are largely defined by the necessary detector acceptance region and required particle position reconstruction, geometrical changes on this scale are impossible. However, the latter option can be addressed in multiple promising ways:

- ♦ The upcoming SWITCHER chips for Belle II implement a concept of overlapping gate switching, where two gate-on signals of consecutive pixels stay both on for a fine-grain-adjustable time. The basic idea is to keep the drain current from dropping severely, thus gaining some settling time. (see § in [Figure 65](#)).
- ♦ Sampling of the current can happen without complete settling, possibly requiring an offline correction later and increasing the sampling error.
- ♦ The clear time can be reduced to the bare minimum. Since the clear process is assisted by the capacitive-coupled cleargate (CCCG), a complete clear in less than 20 ns should be possible.

At the current state, since only ≈ 15 ns are missing, a clear answer cannot be given. Further unknown are parameters of the future Belle II-type DEPFET sensors, like the real capacitance of the drain lines, the rise time of the gate- and clear strobes, the pedestal spread of an irradiated sensor with a possible temperature gradient, or the contributions of common mode noise and pickup to the dynamic range. Further investigations with future readout systems based on the DCD-B, the SWITCHER for Belle II, and large Belle II-type DEPFET sensors are needed for a deeper insight.

7.2 PIXEL NOISE

The noise of the read out data can be extracted from the time resolved measurements shown above. This has been done for both the COCG LE and the COCG SA device, operated at a t_{row} of ≈ 90 ns in single sampling mode. At the points labeled 1st sample in [Figure 67](#) and [Figure 64](#) the noise is calculated as the RMS for 1000 readout cycles, and histograms showing this pixel noise for all connected pixels are plotted in [Figure 68](#). For the short DEPFET COCG LE matrix a pixel noise of 87.6(99) nA is found (corresponding to an equivalent noise charge (ENC) of 175(20) e^- for a $g_d = 500$ pA/ e^-), the pixel noise for the longer COCG SA device with higher capacitive load is slightly higher at 98.9(126) nA (ENC of 198(25) e^-). A comparison with stand-alone DCD2 measurements in [Figure 59](#) shows that these results are expected (with a regulated cascode power consumption of 1 mW): for the long COCG SA with a drain capacitance ≥ 30 pF a noise of ≈ 95 nA was expected; the short COCG LE device with an estimated drain capacitance of ≈ 10 pF should show ≈ 75 nA of noise.

7.3 CAPACITIVE CHARGE INJECTION

Time resolved measurements of the DEPFET drain current using the DCD2 show multiple overshoots and undershoots directly after switching the gate and clear steering signals (see e. g. [Figure 62](#), and [Section 6.2.1](#) for the measurement method). These effects impose a time penalty on the read-out cycle, effectively rendering a CDS based readout impossible. The origin of these effects needs to be investigated, especially to exclude sources that are not related to the DEPFET system development, like malfunctioning

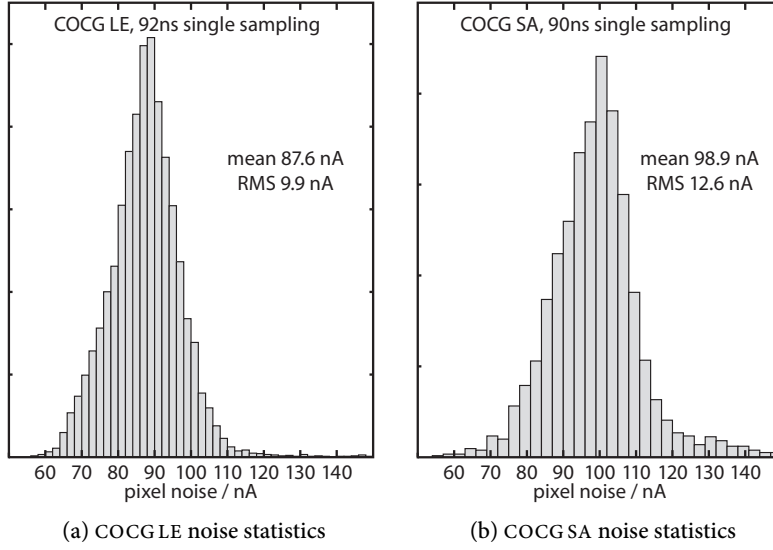


Figure 68: Histogram of single pixel noise values, for both (a) COCG LE and (b) COCG SA devices, read out in single sampling mode with a row time of ≈ 90 ns. Data is taken at as RMS values from points labeled 1st sample in Figure 67 and Figure 64.

system components, externally induced crosstalk, or simple measurement errors.

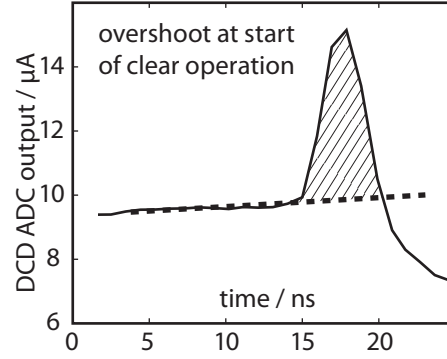
Under the presence of parasitic capacitances in the DEPFET pixel itself (see Figure 5 on page 9), between the SWITCHER steering lines and the drain line the overshoots can be explained. With a given coupling capacitance C and a voltage change ΔU , a charge $\Delta Q = C \times \Delta U$ is displaced during the switching operation. This charge ΔQ is seen as a fake signal by the DCD2 chip. The signal current I can be calculated if the rise time t_r of the SWITCHER signal is known, $I = C \times \Delta U / t_r$. Note that once the switching cycle is reversed, a charge of $-\Delta Q$ is delivered, which is evident in the following pictures.

7.3.1 Measurement procedure

To prove the assumption of capacitive charge injection a parametric series of measurements is performed. The fake signal charge is extracted as a function of either the clear or gate voltage. Current waveforms of all read out pixels are recorded around the overshoots of interest, a baseline is fitted and subtracted, and the charge ΔQ is extracted by simply integrating the measured current I over time. For noise reduction each sampling point of the waveforms is recorded 1000 times and averaged.

7 As an example, with a risetime of 10 ns, a capacitance of 1 fF and a voltage of 10 V a current flow of 1 μ A is expected.

Figure 69: The capacitively injected charge corresponds to the area of these overshoots and is extracted by subtracting a fitted baseline and then integration over time. The results are averaged over all connected DEPFET pixels.



7.3.2 Clear strobe charge injection

The drain injected charge as a function of the clear voltage has been measured for the short DEPFET COCG LE device, shown in Figure 70. A linear relationship is observed which directly links the switching operation to the overshoots. The coupling capacitance can be extracted to ≈ 2.3 fF, although it is not expected that this value matches the present parasitic capacitances exactly, since the clear operation itself causes a change in drain current and consequently cuts the overshoots short.

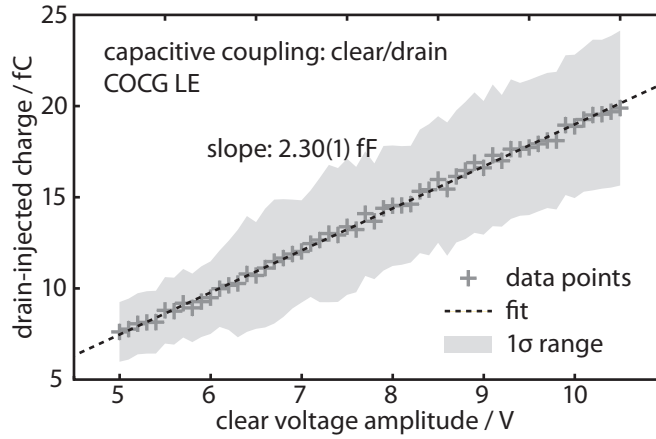


Figure 70: A linear relationship is found between clear voltage amplitude and drain injected charge, measured with a short COCG LE device.

7.3.3 Gate strobe charge injection

Measuring the effects of charge injection due to the gate voltage switching is more difficult since several effects overlap when switching from row $N - 1$ to row N :

- ◆ gate $N - 1$ turns off, charge $+\Delta Q$ is injected
- ◆ DEPFET transistor $N - 1$ turns off, the drain current I_d shuts down
- ◆ gate N turns on, charge $-\Delta Q$ is injected
- ◆ transistor N turns on and I_d rises again

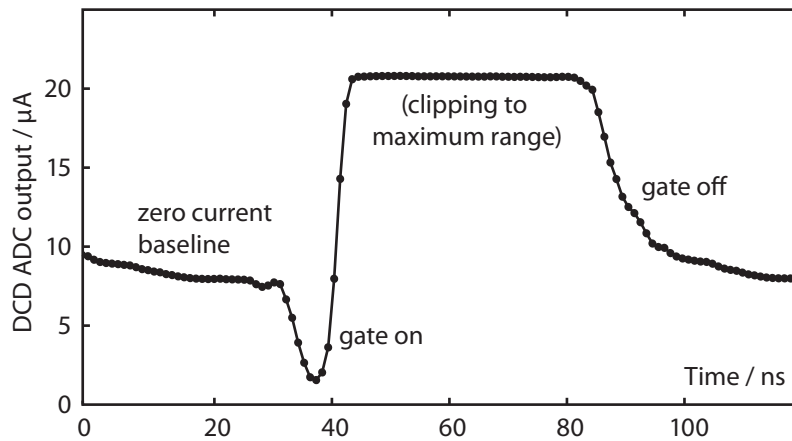
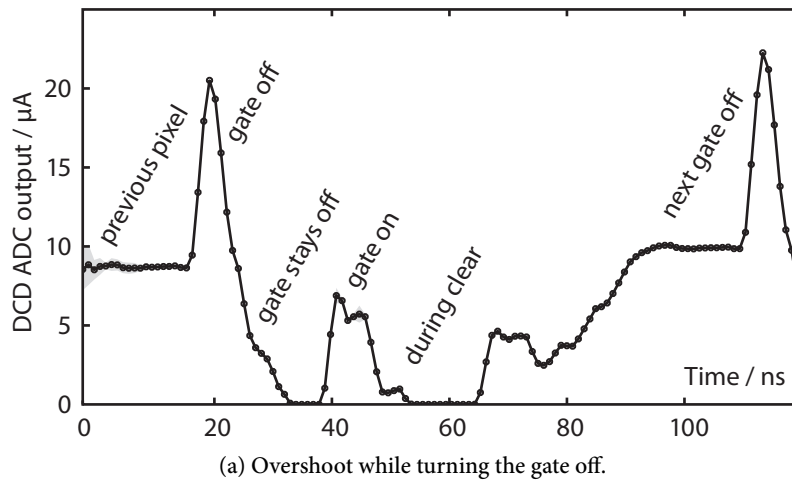


Figure 71: Current waveforms for measuring capacitive charge injection into the drain due to switching the gate lines on a long COGSA DEPFET device. The row time is 96 ns corresponding to a line frequency of 10.4 MHz.

The charge injection from both switching events should ideally cancel each other, unless there is a delay between the switching. Delays can be caused by RC delays on the connecting gate lines or by a deliberate break-before-make design chosen for the SWITCHER. To separate the above mentioned effects the operating sequence of the DEPFET is changed; after switching off gate $N - 1$ the next gate N is kept off and the drain current goes to zero. Now the $+\Delta Q$ charge injection is clearly visible, as shown in Figure 71a. Now the charge injection can be measured as a function of the gate voltage, and again a linear relationship with a coupling capacitance of ≈ 8 fF can be found (see Figure 72 for a COCG SA DEPFET device). The charge injection due to switching a gate on also exists, yet it is more difficult to observe. When starting with a turned off DEPFET, a negative spike on a zero current baseline is expected. The DCD2 can be biased with an additional current flowing into each channel (instead of subtracting the pedestal current), thereby shifting the zero baseline to an arbitrary input level. This undershoot is shown in Figure 71b.

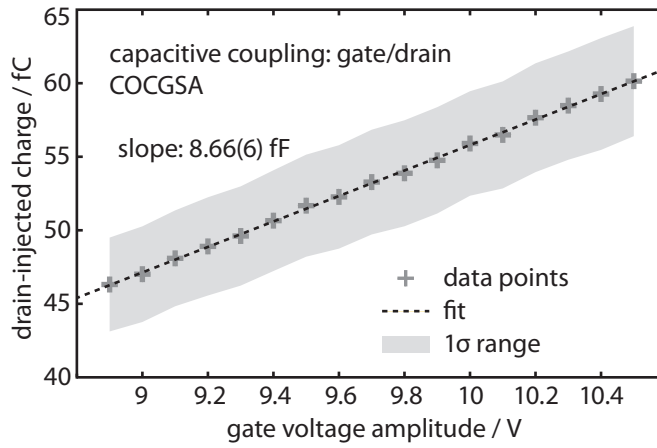


Figure 72: A linear relationship is found between gate voltage amplitude and drain injected charge, measured with a long COCG SA device.

7.3.4 Results and consequences

Parasitic capacitances between drain and the gate and clear lines could be identified as the source of the observed overshoots and undershoots. Although the capacitances are only a few fF each, fast switching with high voltages of ≈ 10 V causes a significant displacement charge to flow and a current is delivered to the readout chip DCD2. The total time penalty for a readout cycle is ≈ 20 ns. Statistics on these measurements, when several pixels are combined, can also provide an insight to process related variations.

Detailed studies are conducted to extract these parasitic capacitances directly from the layout of DEPFET pixels before production [53, 54], to improve the pixel geometries and to generate a comprehensive simulation model for a DEPFET.

7.4 PEDESTAL CURRENT SPREAD

The pedestal current spread of the COGGLE DEPFET sensor has been measured as a function of the gate source voltage V_{gs} with the DCD2. A detailed knowledge of the pedestal currents is important for a correct sizing of the dynamic input range of future readout chips; even though final Belle II DEPFET devices are not available yet, the possibility to do these measurements automatically — with high statistics over all connected pixels using the DCD2 — is demonstrated here. The drain current I_d vs. the gate source voltage V_{gs} is shown in [Figure 73a](#), where V_{gs} is varied from 2.9 V to 4.9 V in 100 mV steps by adjusting $V_{gate, on}$ of the gate-SWITCHER. The drain current has been measured after the clear process and does not include differences in leakage current spread. The dynamic input range of the DCD2 was piecewise adjusted by changing MainOffset from 500 to 1700 in 8 steps; a complete ADC calibration using an external precision current source was performed for each step and for each DCD2 channel. This procedure guarantees that no clipping of the input signals occurs, and that for each ADC output code the input current can be calculated.

The drain current characteristics follow [Equation 2.2](#):

$$I_d = \frac{1}{2} \frac{W}{L} \mu_p C'_{ox} (V_{gs} - V_{th})^2 \quad (7.1)$$

Drain current variations can be attributed to process variations during manufacturing. Typically, during etching $\frac{W}{L}$ can vary by $\pm \Delta \frac{W}{L}$; doping variations of the transistor channel and internal gate lead to a variation of V_{th} with $\pm \Delta V_{th}$ (possible oxide thickness variations act similarly to $\Delta \frac{W}{L}$). For I_d follows:

$$\begin{aligned} I_d \left(\Delta \frac{W}{L}, \Delta V_{th} \right) &= \frac{1}{2} C'_{ox} \mu_p \left[\left(\frac{W}{L} \pm \Delta \frac{W}{L} \right) (V_{gs} - (V_{th} \pm \Delta V_{th}))^2 \right] \\ &= \frac{1}{2} C'_{ox} \mu_p \left[\frac{W}{L} (V_{gs} - V_{th})^2 \right. \\ &\quad \mp 2 \frac{W}{L} \Delta V_{th} (V_{gs} - V_{th}) \\ &\quad \left. \pm \Delta \frac{W}{L} (V_{gs} - V_{th})^2 \right] + \mathcal{O}(\Delta^2) \end{aligned} \quad (7.2)$$

It can be seen that under these simple assumptions variations of the geometry of the external gate should show a quadratic dependence on V_{gs} while variations affecting the threshold voltage will show a linear relationship with V_{gs} .

The distribution of I_d variations is shown in the boxplots in [Figure 73c](#) for a larger selection of drain currents, and as a histogram in [Figure 73b](#) for a selected I_d of $\approx 100 \mu A$ (corresponding to $V_{gs} = 4.6$ V). If all single outliers are included, variations of up to $12 \mu A$ were recorded, including only 99 % of the pixels still leaves $\approx 9 \mu A$ (≈ 10 %) of variations. In [Figure 73d](#) the I_d variations are again plotted vs. V_{gs} , given with simplified

inclusion ranges. To test Equation 7.2, a second order polynomial can⁸ be fitted to the data shown in Figure 73d.

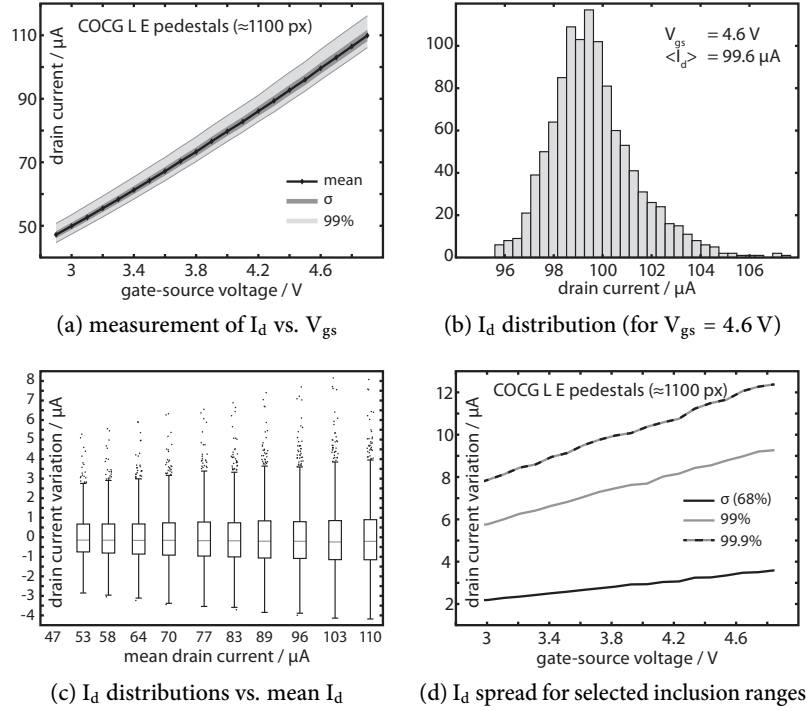


Figure 73: The DEPFET drain current I_d has been measured as a function of the gate source voltage V_{gs} for ≈ 1100 pixels of a COG L E device. Currents are measured with the DCD2, which has been calibrated for multiple I_d ranges. The main interest is in the pixel to pixel I_d variations.

(a) shows the quadratic dependence of I_d vs. V_{gs} according to Equation 2.2, the spread of the currents is plotted.

(b) shows the distribution of the drain currents for $V_{gs} = 4.6$ V.

(c) shows the distributions as a function of the mean drain current I_d .

(d) summarizes plot (c) by providing a few typical inclusion ranges for the output currents. Including all outliers, variations increase to ≈ 12 %.

7.5 RADIOACTIVE SOURCE MEASUREMENTS

A measurement with a radioactive ^{241}Am source has been performed, using the small COG L E DEPFET device. The ^{241}Am source shows characteristic lines⁹ at 59.5 keV ($\approx 16\,481\,e^-$ in Si) and 26.3 keV ($\approx 7285\,e^-$ in Si). Due to the relatively small pixel size of $32\,\mu\text{m} \times 24\,\mu\text{m}$ and diffusion of the charge carriers, charge sharing between neighboring pixels is expected, and the total charge in pixel clusters has to be considered. For this measurement only, ten neighboring drain lines of the COG L E DEPFET matrix have been connected to the DCD2, which allows (with the given double-pixel structure) to create 5×5 and 3×3 clusters. A source measurement

⁸ The fitting results in a linear relationship, indicating stronger variations in the threshold voltages. These measurements should however be performed with precision measurements using dedicated equipment in a controlled environment, and not with the DCD2.

⁹ The 13.9 keV line of ^{241}Am cannot be seen clearly due to the present noise.

with the long COCGSA device was impossible due to wire bonding limitations.

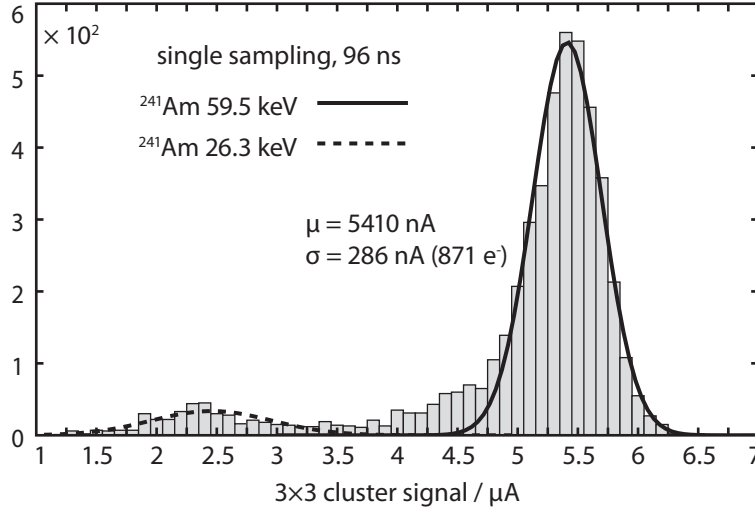


Figure 74: ^{241}Am source measurement with a small COCG LE DEPFET device using the DCD2, single sampling, 3×3 clusters, with a row time of 96 ns. The 59.5 keV line produces $\approx 16\,481\,e^-$ in Si, and is measured to 5410(286) nA. This yields a $g_q = 328(17)\,\text{pA}/e^-$, and an energy resolution of $\sigma_E/E = 871/16481 = 5.3\%$. The performed non-linearity corrections for the DCD2 ADC channels provided a small improvement to the σ -width from 310 nA ($\sigma_E/E = 5.7\%$) to 268 nA.

Data has been taken in single sampling mode, for two different readout speeds of 800 ns and 96 ns per row. Several offline data processing and correction steps were applied¹⁰ to the data:

1. A nonlinearity correction of the DCD2 ADC data is performed. To the ADC transfer curves, measured previously for calibration, a 9th order polynomial is fitted to smooth DNL related effects. The difference of this fit function to the best-straight-line fit is used for data correction.
2. To suppress low frequency noise a common mode correction is performed, where the mean value of the full frame (5×256 pixels) is subtracted from each read out pixel. A row-wise common mode correction is not possible due to the small number of pixels per row.
3. Individual pixel pedestals are subtracted. The pedestal values are calculated as a running average over a window of the last 64 frames.
4. Finally clusters are identified: a 3×3 cluster is created if the central pixel (seed) has an entry $\geq 1.2\,\mu\text{A}$ (seed-cut), pixels within this cluster are allowed to contribute only if their entry is 200 nA (noise-cut). The total cluster energies are recorded in a histogram.

The energy spectrum of ^{241}Am for $t_{\text{row}} = 800\,\text{ns}$ is shown in Figure 75, and for $t_{\text{row}} = 96\,\text{ns}$ in Figure 74. For the fast measurement, the 59.5 keV-

¹⁰ A detailed description of typical steps for data correction can be found e. g. in publications by Reuen [83] and Esch [29].

peak results in a signal of 5410(286) nA, which allows to calculate the DEPFET internal amplification to $g_q = 328(17)$ pA/e⁻.

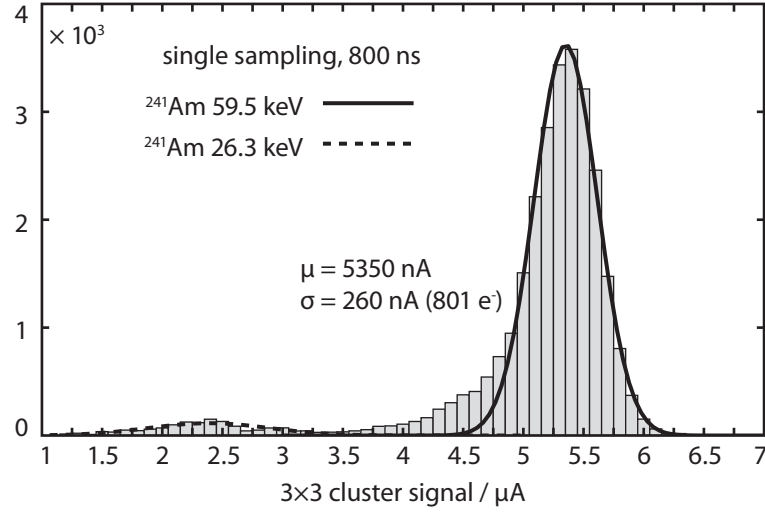


Figure 75: ^{241}Am source measurement with a small COCGLB DEPFET device using the DCD2, single sampling, 3×3 clusters, with a row time of 800 ns. This slower measurement shows a peak of 5350(260) nA for the 59.5 keV line, yielding a $g_q = 324(15)$ pA/e⁻, and an energy resolution of $\sigma_E/E = 801/16481 = 4.9\%$. Although the noise is minimally smaller, the results match the faster measurement in Figure 74.

Even though the noise¹¹ of 286 nA ($\equiv 871\text{ e}^- \equiv 3.15\text{ keV}$, $\sigma_E/E = 5.2\%$) is high, it is consistent with noise measurements presented here before. Note that for a 3×3 cluster the noise of all contributing pixels adds in quadrature, and a maximum factor of $\sqrt{9} = 3$ has to be taken into account. The measurements could be further improved by implementing DEPFET gain corrections; a more effective row-wise common mode correction will be possible in future setups where $\gg 5$ neighboring pixels are connected. Nevertheless, these measurements show a significant improvement in noise and energy resolution compared to the previously used readout system. This system, based on the CURO [101] readout chip and several generations of SWITCHER chips, was used extensively for beam test campaigns [11, 55, 56, 83, 84, 107, 108].

Source measurements are reported¹² by Furlotov [34] and Esch [29] for two devices: For a COCGLB DEPFET device ($g_q = 642(12)$ pA/e⁻) the σ -width of the 59.5 keV line of ^{241}Am is $\approx 1365\text{ e}^-$ ($\sigma_E/E = 8.2\%$), for a COCGLB device ($g_q = 355(7)$ pA/e⁻) a σ -width of $\approx 1580\text{ e}^-$ ($\sigma_E/E = 9.6\%$) is found. Earlier measurements done by Schmieden [92] with the same system, but with a COCGLB device from the PXD4 production show a σ -width of $\approx 1280\text{ e}^-$ ($\sigma_E/E = 7.8\%$, $g_q = 361(7)$ pA/e⁻).

¹¹ The numbers should be understood as a total energy resolution; including noise, systematic errors, missing gain corrections, and sub-optimal common mode noise suppression.

¹² Energy resolution values are extracted from [92, fig. 6.3], [34, fig. 6] and [29, fig. 4.3 and fig. 4.4], g_q values can be found in [29, tab. 5.3].

Further, a more comprehensive study is found in an internal report by Schmieden [91], where five COG LB devices were studied, resulting¹³ in an energy resolution of $\sigma_E/E = 10\% \text{ to } 10.6\%$.

A direct comparison with the used COG LB devices, which have almost the same internal amplification as the used COG LE, show an improvement in signal-to-noise and energy resolution by a factor of 1.5 to 2 for the DCD2-based readout system, while additionally reading out much faster and working in single sampling mode.

7.6 DIGITAL RESOLUTION LIMITS OF THE READOUT CHAIN

The digital signal resolution is an important quantity which influences the quality of position reconstruction algorithms and ultimately the spatial resolution of the detector. In the digital processing chain, the number of required bits has an impact on signal transmission bandwidths and other system aspects, e. g. the required area to implement algorithms or storage memories, and power consumption. It would be too simple to assume that the 8-bit resolution of the DCD-B-ADC equals the achievable signal resolution. What are the limiting effects for the signal resolution? To answer this question, a more realistic approach is needed, and effects and error sources from the DEPFET, the DCD2, and further digital processing (e. g. the DHP) have to be included. Key points are the dynamic ranges of the devices, like DEPFET pedestal current I_{ped} spread and the dynamic input range of the DCD-B. Error sources include electronic noise, nonlinearity of the ADC and numerical calculation errors. The following sections review the dynamic ranges and these error sources and their effect on the signal resolution.

7.6.1 *Dynamic range of the DEPFET*

The output current of the DEPFET-sensor is a sum of the static¹⁴ pedestal current I_{ped} , the signal current and dynamic contributions like common mode noise. The dynamic output range is then given by the DEPFET pixel with the lowest pedestal current I_{ped} minus the maximum expected common mode noise ($I_{\text{ped,min}} - I_{\text{CM}}$) up to the highest output value which is the sum of all possible constituents ($I_{\text{ped,max}} + I_{\text{CM}} + I_{\text{sig}}$).

7.6.1.1 *Signal current I_{sig} range*

For the following calculations a maximum signal in the sensor of 1×10^4 e⁻ is assumed (this is twice the most probable value of charge deposition from minimum ionizing particles in 75 μm of silicon, see [Figure 76](#)). This is less than the maximum energy deposited in a pixel by low energy particles, so in the following readout chain clipping to the highest possible

¹³ Schmieden [91] measures the signal-to-noise ratio as the mean cluster signal divided by the width of the cluster signal; the energy resolution given here are reciprocal values.

¹⁴ Static pedestal current I_{ped} is assumed after thermal equilibrium has been reached. Changes due to deliberate biasing changes, irradiation over time or aging effects are considered to happen slowly and can require readjustments of the DEPFET or DCD-B biasing.

ADC value might occur for some pixels. The internal amplification g_q of the DEPFET is expected to be $\approx 0.5 \text{ nA/e}^-$. This leads to a maximum signal current I_{sig} of $5 \mu\text{A}$. The calculations can, however, be adjusted easily to a different signal current.

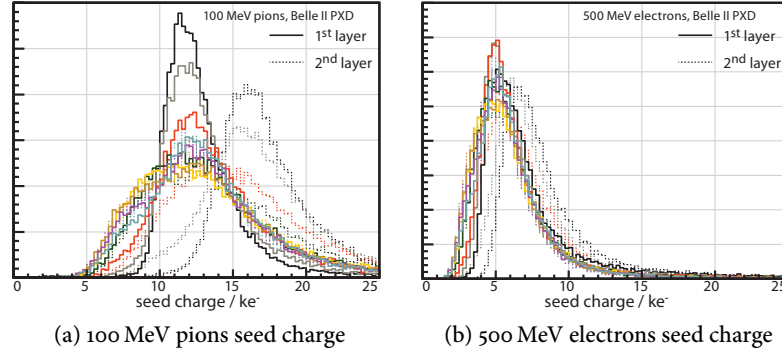


Figure 76: Expected seed pixel (pixel of a cluster with highest entry) charge for the two layer Belle II DEPFET pixel detector, assuming $75 \mu\text{m}$ thick silicon, for different incident angles (colored curves, from 20° to 90°). The highest deposited energy is roughly for 45° , where the particle has the longest trajectory in the silicon. Simulation data kindly provided by Z. Drasal, Charles University, Prague, Oct. 2010.

(a) shows the seed charge for low momentum 100 MeV charged pions, which deposit energy according to the Bethe-Bloch formula[17].

(b) shows the seed charge for 500 MeV electrons, the most probable value is $\approx 5000 \text{ e}^-$

7.6.1.2 Pedestal current I_{ped} range

The expected pedestal current I_{ped} variations can be attributed to two main factors, statistical process variations and ionizing radiation damage. The mean pedestal current (i. e. the operating point of the DEPFET) needs to be chosen so that all DEPFET pixels turn on and provide a reasonable gain (see Equation 2.8).

PROCESS VARIATIONS During the production of the DEPFET sensors various processing steps, including implantations and etching, are subject to statistical fluctuations and changing conditions. Doping concentrations of the internal gate and transistor channel are not perfectly uniform, wet-etching¹⁵ of polysilicon will cause small external gate length differences. The DEPFET transistors will thus show variations in transconductance g_m , threshold voltage, and internal amplification g_q . Measurements shown in Section 7.4 display a pedestal current variation of $\approx 10 \%$ based on these effects.

IONIZING RADIATION DAMAGE The effects of ionizing radiation damage on DEPFET-devices have been studied extensively by Wei [111] and are summarized in the Belle II Technical Design Report [27, chap. 4.5].

¹⁵ *wet-etching*: a chemical etching process where a wafer is usually immersed in a bath of liquid, cf. plasma etching

The DEPFET is a MOSFET device and thus suffers mainly from threshold voltage shifts — and an increase in threshold voltage spread — due to an increase of oxide charges in the gate oxide; a typical remedy is the reduction of the oxide thickness. With thin (100 nm) oxides threshold shifts in the order of 2 V have been observed after irradiation up to 100 kGy, these voltage shifts can be easily compensated with the SWITCHER chips. A problem however arises in case of inhomogeneous irradiation across one module: Different DEPFET pixels now operate under different biasing conditions. For a typical transconductance g_m of 50 μS and 1 V of threshold dispersion the DEPFET drain current will show a 50 μA variation. A safe assumption is 50 % pedestal current I_{ped} spread after inhomogeneous irradiation, as was shown in more recent measurements by Müller and Ritter [69]. The final answer though can only be obtained once irradiated Belle II-type devices are available and have been measured with reasonable statistics over several wafers.

COMMON MODE NOISE All unintended effects inducing a common change in signal can be summarized as common mode noise. This can happen due to electro-magnetic pickup, noise on power supply voltages or digital switching in readout chips. As such, it is mostly a system aspect and can be reduced if not totally avoided by careful design. The sensitivity to common mode effects can be quite high, e. g. a change of either V_{Source} or V_{Gate} by merely 2 mV will cause 1 LSB of signal (with $g_m = 50 \mu\text{S}$ and an ADC gain of 100 nA LSB⁻¹).

7.6.2 Dynamic range and error sources of the readout chips

7.6.2.1 DCD-B dynamic range concept

The design of the DCD-B readout chip ideally needs to adapt to the dynamic output range of a DEPFET sensor, on the other hand the DCD-B can only implement what is reasonable under various design constraints. The dynamic range for digitization is directly given by the range of the 8-bit ADC, the design value is 16 μA [see 79], however with the measurements of the DCD2 chip shown in [Section 6.1.1](#) a range of 24 μA is considered possible. The pedestal range can be compressed by a factor of four using a 2-bit DAC (see [Figure 28](#)). However, this does not simply extend the total range to $8 + 2 = 10$ bits, since the 2-bit DAC performs a fixed subtraction and only acts on compressing the pedestals and not the signal. The required ADC range is then

$$\text{ADC-range} = \frac{1}{4} \cdot \text{pedestal-range} + \text{signal}$$

with the signal only occupying a fractional part of the total range. The signal current is then digitized with

$$\text{signal-resolution [bits]} = \log_2 (\text{signal}/\text{ADC-range} \cdot 256) \quad (7.3)$$

An example is illustrated in [Figure 77](#) with typical numbers from [Section 7.6.1](#). The required ADC range as a function of DEPFET pedestal current spread is shown in [Figure 78](#), including a future scenario where a 3-bit

DAC might be used. With a signal of $5\ \mu\text{A}$ and a total ADC range of $17.5\ \mu\text{A}$ the signal will be digitized with ≈ 6.2 LSB.

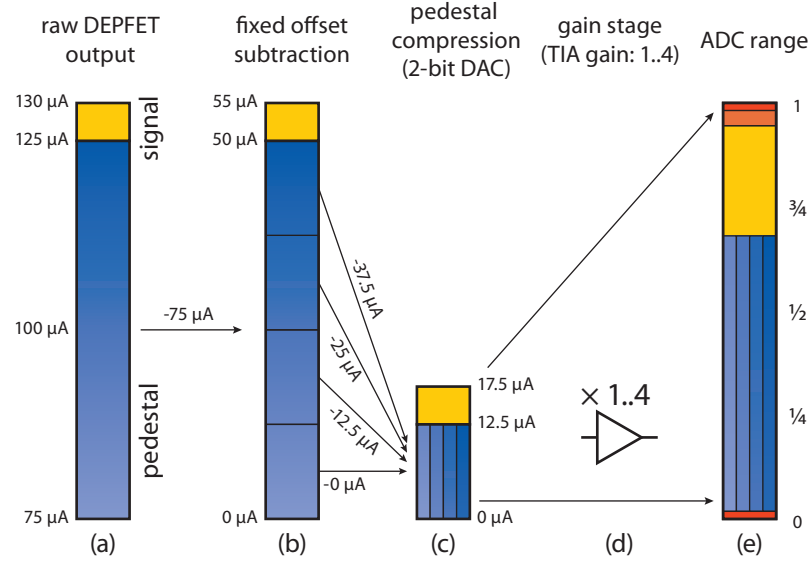


Figure 77: The pedestal range compression in the DCD-B is explained using cumulative bar charts with realistic numbers as outlined in [Section 7.6.1](#).

(a) The DEPFET is expected to operate with $50\ \mu\text{A}$ pedestal variations (■), a mean pedestal current of $100\ \mu\text{A}$ and a maximum signal (■) of $5\ \mu\text{A}$. This basically defines the input range of the DCD-B from $75\ \mu\text{A}$ to $130\ \mu\text{A}$.

(b) As a first step, $75\ \mu\text{A}$ is subtracted for all input channels with a global current source (cf. [Figure 28](#)).

(c) The biasing of the 2-bit pedestal compression DAC is set to match the total pedestal spread: one bit equals one quarter ($12.5\ \mu\text{A}$ per bit). This leaves a total range of $17.5\ \mu\text{A}$ to be digitized by the ADC.

(d) The optional gain by the current receiver is set to unity gain for this example.

(e) The input current of $17.5\ \mu\text{A}$ is mapped to the ADC range. Some headroom needs to be reserved for offset and gain errors (■), and common mode noise (■).

7.6.2.2 Typical dynamic range reducing errors of the ADCs

When dealing with a large number (i. e. 2×256 in case of the DCD-B) of ADCs, different behavior between individual channels might occur. This is due to statistical transistor mismatch and systematic errors, like voltage drops and as a result biasing changes over a large chip area. A simple definition of the operating range of the whole readout chip is the common operating range of all individual channels, which is also a guaranteed-to-work approach when interfacing the DEPFET with the readout chip. Various biasing parameters can then be iteratively changed to optimize the interaction between the dynamic output range of the DEPFET and the dynamic input range of the DCD-B. The effect of gain and offset variations of ADCs is illustrated in [Figure 79](#).

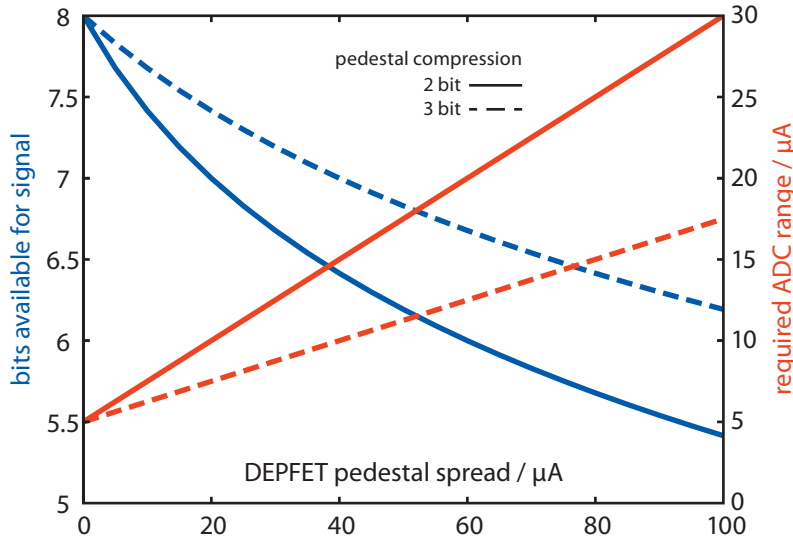


Figure 78: The effect of DEPFET pedestal current spread on the required ADC range is shown for a scenario with a 2-bit pedestal compression DAC (—) and a 3-bit DAC (- - -). Assuming $5\ \mu\text{A}$ of signal current, the signal resolution can be calculated (— resp. - - -).

In both scenarios a 8-bit ADC is assumed. For a 7-bit ADC the signal resolution is exactly one bit less (cf. Equation 7.3, $\log_2 \frac{1}{2} = -1$).

7.6.2.3 Effect of the ADC nonlinearity

Nonlinearity is the deviation of the ADC transfer curve from a straight line, reducing the effective resolution and sometimes the dynamic range. These errors can be mitigated by calibration, if the real transfer characteristic *and* the original digitized value is known. In case of the DEPFET readout, the situation is further complicated:

- ♦ Both pedestal current I_{ped} and signal current $I_{\text{ped}} + I_{\text{sig}}$ suffer from the nonlinear characteristics. Since only the real signal I_{sig} is of interest, a subtraction is performed; therefore not only the position on the transfer function is important, but also the value of the signal (see illustration in Figure 80a). In other words: The nonlinearity correction needs to be applied to both pedestals and signals. For a reasonable smooth transfer function and small signals the total error is less than expected because now only the local slope of the transfer function counts.
- ♦ Due to common mode corrections and possibly dynamic pedestal subtractions done in the DHP chip the original ADC value remains unknown, which makes it unlikely that a correction for the nonlinearity can be implemented offline.

The nonlinearity introduces a systematic error. For a typical signal of $5\ \mu\text{A}$ (≈ 70 LSB) an error of ≈ 1.5 LSB is expected, assuming an integral nonlinearity similar to the DCD2 as shown in Figure 80c and Section 6.1.3.

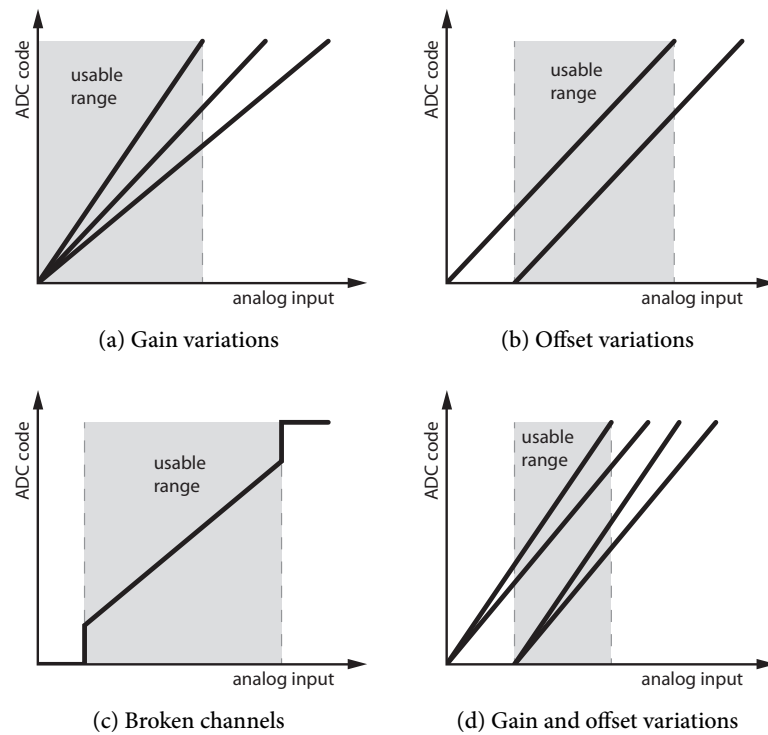


Figure 79: Typical dynamic range reducing errors of the ADCs. The usable range can be defined as the common operating range of all individual channels. Most common are gain and offset differences between channels due to statistical transistor mismatch and systematic errors, like voltage drops. Partially broken channels (c) show a reduced digitization range and also a larger DNL.

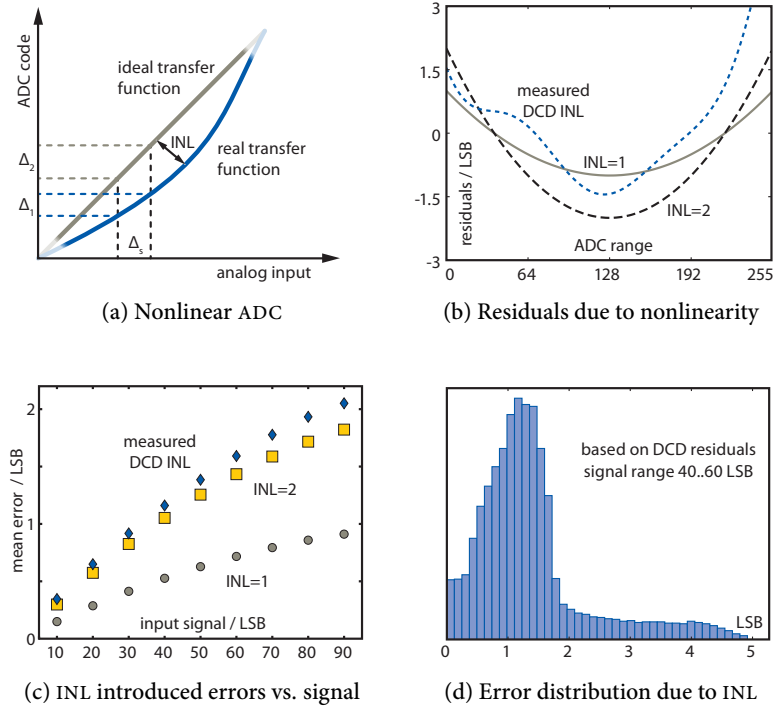


Figure 80: (a) The INL is the maximum deviation from the real transfer function of an ADC to a straight line fit. In single sampling readout mode for the DEPFET, a signal current I_{sig} is always referenced to the individual pedestal current I_{ped} of the pixel which has been sampled earlier with the same ADC. The local slope of the transfer function counts: For a given input signal Δ_s the ideal ADC output would be Δ_2 whereas in reality Δ_1 is measured.

(b) The residuals (difference between the real and the ideal transfer function) are shown for a second order polynomial function with $INL=1$ (—) resp. $INL=2$ (- - -) and for the measured INL of the DCD2 (- · - ·).

(c) The mean error depends on the transfer function and input signal range (cf. (a)). For a given input signal (± 5 LSB) all possible positions on the transfer function have been evaluated and the mean error calculated. ($INL=1$ ●, $INL=2$ ■, DCD2 ◆)

(d) The error distribution for a input signal of 40 LSB to 60 LSB based on the measured (average over 24 channels, smoothed) DCD2 residuals is shown.

7.6.2.4 Noise and numerical errors

The electronic noise component of the signal after the DCD-B is assumed to be roughly 1 LSB. Similar slightly lower values have been measured with the DCD2 (see [Section 6.1](#)) under optimized external conditions, i. e. a test system with an optimal power distribution network and limited additional noise sources. Although a better stand-alone noise performance is expected for the DCD-B compared to the DCD2, a final system on a silicon hybrid with limited decoupling in an unshielded environment is likely to show higher noise.

The numerical errors of the following digital processing chain (e. g. the DHP) can be estimated easily, without deeper knowledge of the algorithms¹⁶ used or calculations performed. If all internal calculations are performed with optimal numerical precision, truncating the result to an integer number will result in an error of 0.288 LSB ($\sqrt{1/12}$), if rounding is used then one more bit of information is considered and the error is reduced by a factor of two to 0.144 LSB ($\frac{1}{2} \cdot \sqrt{1/12}$). Even in a conservative scenario with three internal calculation steps and no extra precision the error is still rather small with 0.5 LSB ($\sqrt{3/12}$).

7.6.3 Summary

Limiting factors to the signal digitizing resolution have been explained in the sections above within a realistic scenario for the dynamic ranges of the DEPFET and the readout chip. The DCD-B will digitize DEPFET signal currents only with ≈ 6.2 LSB resolution due to the way the pedestal currents are handled. The signal is further impaired by ADC nonlinearity (1.5 LSB), electronic noise (1 LSB), and numerical errors (0.14 LSB). This leaves a final signal resolution of ≈ 4.4 LSB ($6.2 - \sqrt{1.5^2 + 1 + 0.14^2}$) which is significantly less than the 8-bit design value resolution of the ADC. There is however room for improvement:

- ♦ A reduction of the pedestal current spread could be achieved by fabrication improvements (reduce implantation dispersion); it might also be possible to supply SWITCHER chips with different voltages to counter inhomogeneous irradiation effects.
- ♦ The DCD-B concept should be reconsidered as to include a 3-bit pedestal compression DAC and only transmit seven bits of ADC data. The least significant bit of the ADC output is currently dispensable due to noise and nonlinearity. This scenario would keep the total number of connections required between the DHP and the DCD-B which is an important constraint.
- ♦ Further studies are needed to check if the nonlinearity can be compensated by calibration.

¹⁶ It is assumed that the algorithms used do either not deteriorate the signal or are offline correctable.

SUMMARY

The new Belle II detector at the SuperKEKB flavor factory requires a vertex detector of unprecedented performance to take advantage of the high beam luminosity and provide an increase in experimental precision. A pixel detector is foreseen, based on the DEPFET technology. The Depleted Field Effect Transistor (DEPFET) pixel structure is an advanced semiconductor detector, which delivers besides position sensitive detector capabilities additional features: Low-noise, internal amplification, small pixels, non-destructive readout, low power, and thinned detectors are the main advantages.

The pixel detector consists of two layers of DEPFET modules, arranged cylindrically around the beam pipe at radii of 14 mm and 22 mm. The all-silicon modules combine an active sensor area of $75\text{ }\mu\text{m}$ thin DEPFET pixels, the readout and steering chips, and an area for electrical, mechanical, and active cooling interconnect. During a frame time of $20\text{ }\mu\text{s}$, 192 rows of pixels are read out with a row time of $\approx 105\text{ ns}$. The signal currents are digitized directly on the module, further processing in the digital domain provides zero suppression and triggered data readout. A particular challenge is the fast readout of signal currents in 100 ns or less, given large scale detectors with high capacitive loads and intrinsic signal RC times.

A new prototype generation of an analog-frontend current-mode readout ASIC is available, the Drain Current Digitizer (DCD2), which is suited for the task of digitizing signal current from large DEPFET sensors fast. The DCD2 compensates input capacitances of the DEPFET sensor with a regulated cascode, and digitizes the signal currents of all input channels in parallel using cyclic algorithmic ADCs with 8 bit resolution and an effective conversion time as low as 80 ns .

A new custom FPGA based readout system was designed, which interfaces to the DCD2 readout chip located on a dedicated hybrid. This FPGA system effortlessly handles the maximum data rate of 7.2 Gbit s^{-1} of the DCD2, provides storage memory and interfaces to a computer for data processing. Substantial effort was devoted to PCB design, the development of FPGA firmware, software development, data acquisition, and data analysis. Since the DCD2 is the first prototype readout chip of its kind, most design efforts started from scratch and special problems (e. g. high speed design, high component integration density) had to be addressed.

A detailed characterization of the DCD2 — standalone and connected to a DEPFET matrix — is one major aspect of this thesis. For typical Belle II operating conditions with optimized settings at a readout speed of $\approx 105\text{ ns}$ an ADC range of $\approx 24\text{ }\mu\text{A}$ can be set, corresponding to a gain of $\approx 10.2\text{ LSB}/\mu\text{A}$ with an exceptionally low total spread over 48 channels of only $0.2\text{ LSB}/\mu\text{A}$. The static mean ADC noise is found to be 54 nA , corresponding to a DEPFET ENC of $\approx 108\text{ e}^-$ (assuming a DEPFET $g_d = 500\text{ pA/e}^-$).

Studies on the effective ADC error, including all effects of noise, INL, and DNL, result in a twice larger error in the range of 110 nA.

Dynamic measurements with fast changing input signals and attached capacitive loads were conducted. A complete settling of an input signal to 1 % with a capacitive load of ≈ 60 pF can be achieved in ≤ 50 ns with a per-channel power consumption of the regulated cascode of ≈ 1.2 mW and a noise of ≈ 110 nA (≈ 1.15 LSB, ≈ 220 e⁻).

A new hybrid has been developed, combining a DEPFET sensor, a DCD2 readout chip and two SWITCHER steering chips. Two different assemblies were used for measurements, one with a small COG LE and one with a large COG SA DEPFET sensor.

The maximum achievable readout speed of a large DEPFET sensor has far reaching consequences for the DEPFET pixel detector module layouts, the frame time, and thus the hit occupancy. A detailed study of readout sequences was made possible for the first time with the DCD2 operating in sequential sampling mode. A settling time requirement of ≈ 50 ns for the DEPFET drain current was found after switching gate or clear of the DEPFET transistor. These measurements motivate a transition from a traditional double sampling sequence to a faster single sampling readout operation for Belle II. Furthermore, limiting effects on the settling times were studied, and identified as capacitive charge injections happening within the DEPFET pixel cell itself.

Single sampling operation with the DCD2 allows a detailed look at pedestal current statistics of DEPFET devices. A relative pedestal current spread of the COG LE device was measured to be ≈ 10 %.

The consequences for the digital signal resolution limits of the readout chain with respect to pedestal current spread, DCD2 dynamic range and DCD2 non-idealities have been studied. The cumulative effects shown here should be recognized for future design improvements.

Source measurements with ^{241}Am demonstrate the performance of the new DCD2 readout chip. Compared to previous measurements with similar DEPFET devices, the signal-to-noise ratio and the energy resolution increased by a factor of ≈ 2 , while reading out with the fast Belle II target speed in single sampling mode.

All in all, the DCD2 prototype chip performs exceedingly well: its new concepts for digitizing DEPFET signal currents are proven to work at the required specifications, and it already outperforms previously available readout solutions in terms of noise, readout speed and flexibility. Future production versions of this readout ASIC will, hopefully, continue its success story. The measurements and studies done with DEPFET devices provided important input to finalize the readout specifications as stated in the Belle II Technical Design Report. The *DEPFET Collaboration* continues to use the developed FPGA readout system for current and future development efforts.

DIRECT DEPFET I_D MEASUREMENT

The output current of a DEPFET device has been measured as function of time during a normal switching sequence with a trans-impedance amplifier. This provides a complementary measurement to the waveforms recorded with the DCD2, as shown in [Section 7.1](#). A single drain of the COGGLE DEPFET sensor is wire bonded directly to the amplifier¹, the output voltage is then measured with an oscilloscope. For a slow row time of $2\ \mu\text{s}$ the resulting waveform is shown in [Figure 81](#) and should be directly compared to the DCD2-based measurement in [Figure 60](#) on [page 71](#). For a faster readout of $160\ \text{ns}$ as shown in [Figure 82](#) (cf. [Figure 61](#)) the dips due to capacitive charge injection and rise time effects are visible.

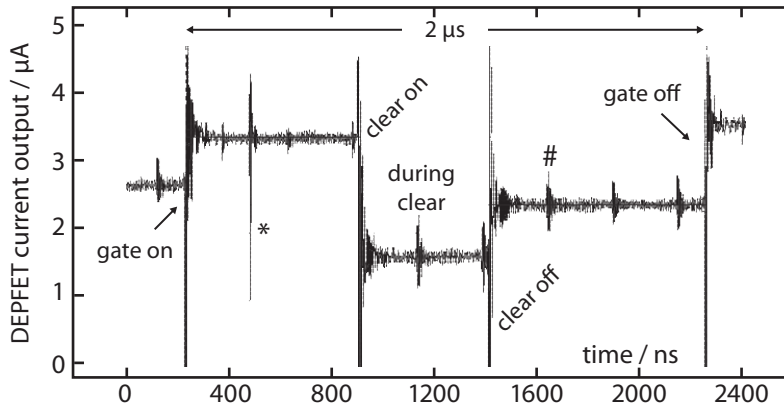


Figure 81: DEPFET COGGLE single channel readout with a transimpedance amplifier and oscilloscope, as an independent confirmation of the DCD2 based measurements. A slow readout sequence with $2\ \mu\text{s}$ row time is shown. Signal is accumulated due to leakage current and ambient light. The long spikes are the result of capacitive charge injection within the DEPFET pixel due to parasitic capacitances and high ($\approx 10\ \text{V}$) switching voltages of the SWITCHER. Other spikes can be traced back to crosstalk on the system: * is related to the falling clock edge of both SWITCHER chips (the rising edge is coincident with *gate on*); # is the internal clock of the DCD2, and occurs eight times in equidistant spacing (The DCD2 was running but not used).

¹ Analog Devices AD8015ACHIPS, wideband / differential output transimpedance amplifier, transresistance $20\ \text{k}\Omega$, bandwidth $240\ \text{MHz}$

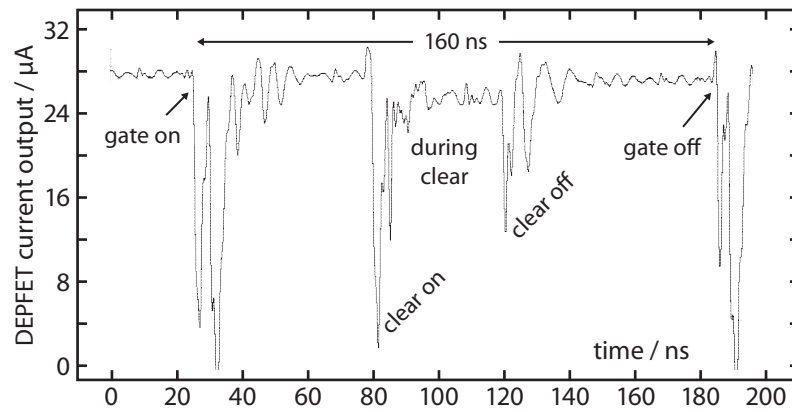


Figure 82: DEPFET COG LE single channel readout with a transimpedance amplifier and oscilloscope, with a fast readout sequence of 160 ns. The DEPFET related charge injections are easier seen compared to [Figure 81](#). The high bandwidth of the transimpedance amplifier causes excessive ringing and noise.

BIBLIOGRAPHY

- [1] A. Abashian et al. The Belle detector. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 479(1):117–232, 2002. doi: [10.1016/S0168-9002\(01\)02013-7](https://doi.org/10.1016/S0168-9002(01)02013-7).
- [2] K. Abe et al. Observation of mixing-induced CP violation in the neutral B meson system. *Phys. Rev. D*, 66(3):032007, Aug 2002. doi: [10.1103/PhysRevD.66.032007](https://doi.org/10.1103/PhysRevD.66.032007).
- [3] K. Abe et al. Evidence for CP -violating asymmetries in $B^0 \rightarrow \pi^+ \pi^-$ decays and constraints on the CKM angle φ_2 . *Phys. Rev. D*, 68(1):012001, Jul 2003. doi: [10.1103/PhysRevD.68.012001](https://doi.org/10.1103/PhysRevD.68.012001).
- [4] K. Abe et al. Measurement of time-dependent CP -violating asymmetries in $B^0 \rightarrow \phi K_S^0$, $K^+ K^- K_S^0$, and $\eta' K_S^0$ decays. *Phys. Rev. Lett.*, 91(26):261602, Dec 2003. doi: [10.1103/PhysRevLett.91.261602](https://doi.org/10.1103/PhysRevLett.91.261602).
- [5] K. Abe et al. Measurement of $\phi(3)$ with Dalitz plot analysis of $B^{+-} \rightarrow D^{(*)} K^{+-}$ decay at Belle. *Belle-Conf-0476*, 2004.
- [6] K. Abe et al. Letter of intent for KEK Super B factory. Technical report, KEK report 2004-04, 2004.
- [7] K. Abe et al. Observation of large CP violation and evidence for direct CP violation in $B^0 \rightarrow \pi^+ \pi^-$ decays. *Phys. Rev. Lett.*, 93(2):021601, Jul 2004. doi: [10.1103/PhysRevLett.93.021601](https://doi.org/10.1103/PhysRevLett.93.021601).
- [8] K. Abe et al. Improved measurement of inclusive radiative B-meson decays. *AIP Conference Proceedings*, 1078(1):342–344, 2008. doi: [10.1063/1.3051954](https://doi.org/10.1063/1.3051954).
- [9] L. Andricsek, G. Lutz, M. Reiche, and R. Richter. Processing of ultra thin silicon sensors for future e+e- linear collider experiments. In *IEEE Nuclear Science Symposium Conference Record*, volume 3, pages 1655–1658, Oct. 2003. doi: [10.1109/NSSMIC.2003.1352196](https://doi.org/10.1109/NSSMIC.2003.1352196).
- [10] L. Andricsek et al. The MOS-type DEPFET pixel sensor for the ILC environment. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 565:165–171, 2006. doi: [10.1016/j.nima.2006.05.045](https://doi.org/10.1016/j.nima.2006.05.045).
- [11] L. Andricsek et al. Intrinsic resolutions of DEPFET detector prototypes measured at beam tests. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 2011. ISSN 0168-9002. doi: [10.1016/j.nima.2011.02.015](https://doi.org/10.1016/j.nima.2011.02.015).
- [12] T. Armbruster. Algorithmischer ADC mit geschalteten Strömen. Master’s thesis, Universität Mannheim, Sept. 2009.
- [13] D. Atkins. Higher-radix division using estimates of the divisor and partial remainders. *IEEE Trans. Comput.*, C-17:925–934, Oct. 1968. doi: [10.1109/TC.1968.226439](https://doi.org/10.1109/TC.1968.226439).
- [14] B. Aubert et al. The BaBar detector. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 479(1):1–116, 2002. doi: [10.1016/S0168-9002\(01\)02012-5](https://doi.org/10.1016/S0168-9002(01)02012-5).

- [15] B. Aubert et al. Measurement of $B \rightarrow K^*(892)\gamma$ branching fractions and CP and isospin asymmetries. *Phys. Rev. Lett.*, 103(21): 211802, Nov 2009. doi: [10.1103/PhysRevLett.103.211802](https://doi.org/10.1103/PhysRevLett.103.211802).
- [16] R. J. Baker. *CMOS: Circuit Design, Layout, and Simulation*. Wiley-IEEE Press, 2010. doi: [10.1002/9780470891179](https://doi.org/10.1002/9780470891179).
- [17] H. Bethe. Zur Theorie des Durchgangs schneller Korpuskularstrahlen durch Materie. *Annalen d. Phys.*, 397, 1930.
- [18] D. Blaschke, M. A. Ivanov, and T. Mannel. *Heavy quark physics*. Springer, 2004. doi: [10.1007/b97728](https://doi.org/10.1007/b97728).
- [19] S. Bokhari and I. Novak. Effect of dissipative edge terminations on the radiation from power/ground planes. In *IEEE Symposium on Electromagnetic Compatibility*, volume 2, pages 735–737, 2000. doi: [10.1109/ISEMC.2000.874712](https://doi.org/10.1109/ISEMC.2000.874712).
- [20] R. W. Bower. Field-effect device with insulated gate; self aligned gate MOSFET. US patent 3,472,712, 1969.
- [21] D. Brooks. *Signal Integrity Issues and Printed Circuit Board Design*. Prentice Hall, July 2003.
- [22] Y. Chao et al. Evidence for direct CP violation in $B^0 \rightarrow K^+\pi^-$ decays. *Phys. Rev. Lett.*, 93(19):191802, Nov 2004. doi: [10.1103/PhysRevLett.93.191802](https://doi.org/10.1103/PhysRevLett.93.191802).
- [23] S.-K. Choi et al. Observation of a narrow charmoniumlike state in exclusive $B^\pm \rightarrow K^\pm \pi^+ \pi^- J/\psi$ decays. *Phys. Rev. Lett.*, 91(26): 262001, Dec 2003. doi: [10.1103/PhysRevLett.91.262001](https://doi.org/10.1103/PhysRevLett.91.262001).
- [24] J. Chu, G. Persky, and S. Sze. Thermionic injection and space-charge-limited current in reach-through p^+np^+ structures. *Journal of Applied Physics*, 43(8):3510 – 3515, 1972. doi: [10.1063/1.1661745](https://doi.org/10.1063/1.1661745).
- [25] D. Cussans. Description of the JRA1 trigger logic unit (TLU). EUDET-Memo-2009-4, Sept. 2009.
- [26] J. Doernberg, H.-S. Lee, and D. Hodges. Full-speed testing of A/D converters. *IEEE J. Solid-State Circuits*, 19(6):820–827, Dec. 1984. doi: [10.1109/JSSC.1984.1052232](https://doi.org/10.1109/JSSC.1984.1052232).
- [27] Z. Doležal (editor) et al. Belle II technical design report. Technical Report 2010-1, KEK, Nov. 2010. URL [arXiv:1011.0352v1](https://arxiv.org/abs/1011.0352v1).
- [28] M. Ercegovac and T. Lang. On-the-fly conversion of redundant into conventional representations. *IEEE Trans. Comput.*, C-36: 895–897, July 1987. doi: [10.1109/TC.1987.1676986](https://doi.org/10.1109/TC.1987.1676986).
- [29] S. Esch. Auslese neuer DEPFET-Sensoren mit verbesserter Ansteuerung und charakterisierenden Messungen zu Antwortverhalten und Homogenität. Master’s thesis, University of Bonn, 2010.
- [30] M. Evans and A. Moore. EMI filters fact and fiction. In *IEE Seminar on EMC - It’s Nearly All About the Cabling*, pages 12/1–12/3, Jan. 2003.
- [31] P. Fischer et al. Readout concepts for DEPFET pixel arrays. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 512:318–325, 2003. doi:

- [10.1016/S0168-9002\(03\)01909-0](https://doi.org/10.1016/S0168-9002(03)01909-0).
- [32] P. Fischer et al. Progress towards a large area, thin DEPFET detector module. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 582(3):843 – 848, 2007. doi: [10.1016/j.nima.2007.07.108](https://doi.org/10.1016/j.nima.2007.07.108).
 - [33] C. Frougny. On-the-fly algorithms and sequential machines. *IEEE Trans. Comput.*, 49:859–863, Aug. 2000. doi: [10.1109/12.868030](https://doi.org/10.1109/12.868030).
 - [34] S. Furletov. A system for characterization of DEPFET silicon pixel matrices and test beam results. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 628:221 – 225, 2011. ISSN 0168-9002. doi: [10.1016/j.nima.2010.06.322](https://doi.org/10.1016/j.nima.2010.06.322).
 - [35] E. Gatti and P. Rehak. Semiconductor drift chamber — an application of a novel charge transport scheme. *Nucl. Instrum. Methods Phys. Res.*, 225:608–614, 1984. doi: [10.1016/0167-5087\(84\)90113-3](https://doi.org/10.1016/0167-5087(84)90113-3).
 - [36] E. Gatti, P. Rehak, and J. T. Walton. Silicon drift chambers — first results and optimum processing of signals. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 226:129–141, 1984. doi: [10.1016/0168-9002\(84\)90181-5](https://doi.org/10.1016/0168-9002(84)90181-5).
 - [37] B. Ginetti, P. Jespers, and A. Vandemeulebroecke. A CMOS 13-b cyclic RSD A/D converter. *IEEE J. Solid-State Circuits*, 27:957–964, July 1992. doi: [10.1109/JSSC.1992.854935](https://doi.org/10.1109/JSSC.1992.854935).
 - [38] A. Giraldo. *Evaluation of deep submicron technologies with radiation tolerant layout for electronics in LHC environments*. PhD thesis, University of Padova, 1998.
 - [39] K. Gärtner and R. Richter. DEPFET sensor design using an experimental 3D device simulator. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 568:12–17, 2006. doi: [10.1016/j.nima.2006.07.038](https://doi.org/10.1016/j.nima.2006.07.038).
 - [40] D. Harris, S. Oberman, and M. Horowitz. SRT division architectures and implementations. In *13th IEEE Symposium on Computer Arithmetic*, pages 18–25, July 1997. doi: [10.1109/ARITH.1997.614875](https://doi.org/10.1109/ARITH.1997.614875).
 - [41] K. Hwang. *Computer arithmetic: principles, architecture, and design*. Wiley, 1979.
 - [42] IEEE. Standard for terminology and test methods for analog-to-digital converters. *IEEE Std 1241-2000*, 2001. doi: [10.1109/IEEESTD.2001.92771](https://doi.org/10.1109/IEEESTD.2001.92771).
 - [43] K. Ikado et al. Evidence of the purely leptonic decay $B^- \rightarrow \tau^- \bar{\nu}_\tau$. *Phys. Rev. Lett.*, 97(25):251802, Dec 2006. doi: [10.1103/PhysRevLett.97.251802](https://doi.org/10.1103/PhysRevLett.97.251802).
 - [44] H. Johnson. *High Speed Signal Propagation: Advanced Black Magic*. Prentice Hall, Mar. 2003.
 - [45] H. Johnson and M. Graham. *High Speed Digital Design: A Handbook of Black Magic*. Prentice Hall, Apr. 1993.
 - [46] Keithley Instruments, Inc. SPEC-2400 Model 2400 SourceMeter Specifications, June 2010.

- [47] J. Kemmer and G. Lutz. New detector concepts. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 253:356–377, 1987. doi: [10.1016/0168-9002\(87\)90518-3](https://doi.org/10.1016/0168-9002(87)90518-3).
- [48] J. Kemmer, G. Lutz, U. Prectel, K. Schuster, M. Sterzik, L. Strüder, and T. Ziemann. Experimental confirmation of a new semiconductor detector principle. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 288:92–98, 1990. doi: [10.1016/0168-9002\(90\)90470-Q](https://doi.org/10.1016/0168-9002(90)90470-Q).
- [49] P. Klein. *Entwicklung, Bau und Test eines Halbleiter-Bildzellen-detektors für den Einsatz in der Teilchenphysik*. PhD thesis, Ludwig-Maximilian Universität München, Sept. 1996.
- [50] K. Kleinknecht. *Uncovering CP Violation*. Springer Tracts in Modern Physics, 2003. doi: [10.1007/b13589](https://doi.org/10.1007/b13589).
- [51] M. Kobayashi and T. Maskawa. CP-violation in the renormalizable theory of weak interaction. *Prog. Theor. Phys.*, 49(2):652–657, 1973. doi: [10.1143/PTP.49.652](https://doi.org/10.1143/PTP.49.652).
- [52] P. Kodyš, Z. Doležal, Z. Drásal, and P. Kvasnička. Data pre-processing for the prague analysis of TB 2009. In *4th International Workshop on DEPFET Detectors and Applications*, 2010.
- [53] C. Koffmane. Extraction of parasitic RC parameters of a DEPFET pixel matrix. In *5th International Workshop on DEPFET Detectors and Applications*, 2010.
- [54] C. Koffmane. Electrical simulation of a DEPFET pixel matrix. In *DPG*, 2011.
- [55] R. Kohrs. *Development and Characterization of a DEPFET Pixel Prototype System for the ILC Vertex Detector*. PhD thesis, University of Bonn, 2008. urn: [nbn:de:hbz:5N-15375](https://nbn-resolving.org/urn:nbn:de:hbz:5N-15375).
- [56] R. Kohrs et al. First test beam results on DEPFET pixels for the ILC. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 565:172–177, 2006. doi: [10.1016/j.nima.2006.05.073](https://doi.org/10.1016/j.nima.2006.05.073).
- [57] P. Kornerup. Digit-set conversions: generalizations and applications. *IEEE Trans. Comput.*, 43:622–629, May 1994. doi: [10.1109/12.280811](https://doi.org/10.1109/12.280811).
- [58] N. Kotani and S. Kawazu. Computer analysis of punch-through in MOSFETs. *Solid-State Electronics*, 22(1):63 – 70, 1979. doi: [10.1016/0038-1101\(79\)90172-2](https://doi.org/10.1016/0038-1101(79)90172-2).
- [59] C. Kreidl et al. *DCD-RO Reference Manual*, June 2010.
- [60] S. Kurokawa and E. Kikutani. Overview of the KEKB accelerators. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 499(1):1–7, 2003. doi: [10.1016/S0168-9002\(02\)01771-0](https://doi.org/10.1016/S0168-9002(02)01771-0).
- [61] P. Li, M. Chin, P. Gray, and R. Castello. A ratio-independent algorithmic analog-to-digital conversion technique. *IEEE J. Solid-State Circuits*, 19:828–836, Dec. 1984. doi: [10.1109/JSSC.1984.1052233](https://doi.org/10.1109/JSSC.1984.1052233).
- [62] S.-W. Lin et al. Difference in direct charge-parity violation between charged and neutral B meson decays. *Nature*, 452:332–335, 2008.

- doi: [10.1038/nature06827](https://doi.org/10.1038/nature06827).
- [63] G. Lutz. *Semiconductor Radiation Detectors*. Springer Verlag, Berlin, 1999. doi: [10.1007/978-3-540-71679-2](https://doi.org/10.1007/978-3-540-71679-2).
 - [64] G. Lutz. DEPFET development at the MPI semiconductor laboratory. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 549:103–111, 2005. doi: [10.1016/j.nima.2005.04.034](https://doi.org/10.1016/j.nima.2005.04.034).
 - [65] R. Marshall. A cable can be an effective antenna - so you add ferrite. In *IEE Seminar on EMC - It's Nearly All About the Cabling*, pages 1/1–1/4, Jan. 2003.
 - [66] Maxim Integrated Products. *INL/DNL Measurements for High-Speed Analog-to-Digital Converters (ADCs)*, Application Note 283, Sept. 2000.
 - [67] Maxim Integrated Products. *Histogram Testing Determines DNL and INL Errors*, Application Note 2085, June 2003.
 - [68] R. McGill, J. W. Tukey, and W. A. Larsen. Variations of box plots. *The American Statistician*, 32:12–16, 1978. doi: [10.2307/2683468](https://doi.org/10.2307/2683468).
 - [69] P. Müller and A. Ritter. Irradiations of thin oxides – status and plans. In *5th Int. Workshop on DEPFET Detectors and Applications*, 10 2010.
 - [70] M. I. Montrose, L. Enxiao, and E.-P. Li. Analysis on the effectiveness of printed circuit board edge termination using discrete components instead of implementing the 20-h rule. In *International Symposium on Electromagnetic Compatibility*, volume 1, pages 45–50, Aug. 2004. doi: [10.1109/ISEMC.2004.1349994](https://doi.org/10.1109/ISEMC.2004.1349994).
 - [71] D. Nairn. Zero-voltage switching in switched current circuits. In *IEEE International Symposium on Circuits and Systems*, volume 5, pages 289–292, June 1994. doi: [10.1109/ISCAS.1994.409364](https://doi.org/10.1109/ISCAS.1994.409364).
 - [72] W. Neeser et al. Study of a DEPFET pixel matrix with continuous clear mechanism. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 392: 254–259, 1997. doi: [10.1016/S0168-9002\(97\)00299-4](https://doi.org/10.1016/S0168-9002(97)00299-4).
 - [73] I. Novak. Reducing simultaneous switching noise and EMI on ground/power planes by dissipative edge termination. *IEEE Trans. Adv. Packag.*, 22, 1999. doi: [10.1109/6040.784475](https://doi.org/10.1109/6040.784475).
 - [74] H. W. Ott. *Electromagnetic Compatibility Engineering*. John Wiley and Sons, Aug. 2009. doi: [10.1002/9780470508510](https://doi.org/10.1002/9780470508510).
 - [75] I. Perić. private communication, on measurements of static transfer characteristics of current memory cells, Oct. 2008.
 - [76] I. Perić, T. Armbruster, M. Koch, C. Kreidl, and P. Fischer. DCD - the multi-channel current-mode ADC chip for the readout of DEPFET pixel detectors. *IEEE Trans. Nucl. Sci.*, 57:743–753, Apr. 2010. doi: [10.1109/TNS.2010.2040487](https://doi.org/10.1109/TNS.2010.2040487).
 - [77] I. Perić et al. *Switcher 3 Reference Manual*, Mar. 2007.
 - [78] I. Perić et al. *DCD2 Reference Manual*, 2008.

- [79] I. Perić et al. *DCD-B Reference Manual*, 2010.
- [80] I. Perić et al. *Switcher-B Reference Manual*, Nov. 2010.
- [81] M. Porro et al. Spectroscopic performance of the DePMOS detector/amplifier device with respect to different filtering techniques and operating conditions. *IEEE Trans. Nucl. Sci.*, 53:401–408, 2006. doi: [10.1109/TNS.2006.869850](https://doi.org/10.1109/TNS.2006.869850).
- [82] P. Quinn and A. van Roermund. *Switched-capacitor techniques for high-accuracy filter and ADC design*. Analog Circuits and Signal Processing Series. Springer Netherlands, 2007. doi: [10.1007/978-1-4020-6258-2](https://doi.org/10.1007/978-1-4020-6258-2).
- [83] L. Reuen. *Analysis of pixel systematics and space point reconstruction with DEPFET PXD5 matrices using high energy beam test data*. PhD thesis, University of Bonn, 2011. urn: [nbn:de:hbz:5N-24431](https://nbn-resolving.org/nbn:de:hbz:5N-24431).
- [84] L. Reuen et al. Performance of a DEPFET prototype module for the ILC vertex detector. *IEEE Trans. Nucl. Sci.*, 53:1719–1725, 2006. doi: [10.1109/TNS.2006.873079](https://doi.org/10.1109/TNS.2006.873079).
- [85] R. H. Richter et al. Design and technology of DEPFET pixel sensors for linear collider applications. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 511:250–256, 2003. doi: [10.1016/S0168-9002\(03\)01802-3](https://doi.org/10.1016/S0168-9002(03)01802-3).
- [86] J. E. Robertson. A new class of digital division methods. *IRE Transactions on Electronic Computers*, EC-7:218–222, Sept. 1958. doi: [10.1109/TEC.1958.5222579](https://doi.org/10.1109/TEC.1958.5222579).
- [87] L. Rossi, P. Fischer, T. Rohe, and N. Wermes. *Pixel Detectors: From Fundamentals to Applications*. Springer, Mar. 2006. doi: [10.1007/3-540-28333-1](https://doi.org/10.1007/3-540-28333-1).
- [88] S. Rummel. Design review hybrid 3.0 for the S3B system, 2007.
- [89] S. Rummel. *Investigation of DEPFET as Vertex Detector at ILC — Intrinsic properties, radiation hardness and alternative readout schemes*. PhD thesis, Technische Universität München, 2009. urn: [nbn:de:bvb:91-diss-20090721-795284-1-1](https://nbn-resolving.org/nbn:de:bvb:91-diss-20090721-795284-1-1).
- [90] C. Sadow et al. Clear-performance of linear DEPFET devices. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 568:176–180, 2006. doi: [10.1016/j.nima.2006.05.267](https://doi.org/10.1016/j.nima.2006.05.267).
- [91] K. Schmieden. *Characterisation of Telescope Hybrids (internal report)*, July 2008.
- [92] K. Schmieden. Charakterisierung einer neuen Generation von DEPFET-Sensoren mit Hilfe eines Lasermesssystems. Master's thesis, University of Bonn, 2008.
- [93] Sigrity, Inc. Technical publications, 1995–2010. URL www.sigrity.com.
- [94] H. Spieler. *Semiconductor Detector Systems*. Oxford University Press, USA, Oct. 2005. doi: [10.1093/acprof:oso/9780198527848.001.0001](https://doi.org/10.1093/acprof:oso/9780198527848.001.0001).

- [95] M. Starič et al. Evidence for $D^0 - \bar{D}^0$ mixing. *Phys. Rev. Lett.*, 98 (21):211803, May 2007. doi: [10.1103/PhysRevLett.98.211803](https://doi.org/10.1103/PhysRevLett.98.211803).
- [96] S. M. Sze. *Physics of semiconductor devices*. John Wiley and Sons, third edition, 2007. doi: [10.1002/0470068329](https://doi.org/10.1002/0470068329).
- [97] Tektronix, Inc. *Sampling Oscilloscope Techniques, Application Note 47W-7209-0*, Oct. 1989.
- [98] The EMC Journal. Technical publications and Keith Armstrong portfolio on advanced PCB techniques, 2001–2009. URL www.compliance-club.com.
- [99] K. D. Tocher. Techniques of multiplication and division for automatic binary computers. *The Quarterly Journal of Mechanics and Applied Mathematics*, 11:364–384, 1958. doi: [10.1093/qj-mam/11.3.364](https://doi.org/10.1093/qj-mam/11.3.364).
- [100] J. Treis et al. Study of noise and spectroscopic performance of DEPMOSFET matrix prototypes for XEUS. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 568:191–200, 2006. doi: [10.1016/j.nima.2006.05.237](https://doi.org/10.1016/j.nima.2006.05.237).
- [101] M. Trimpl. *Design of a current based readout chip and development of a DEPFET pixel prototype system for the ILC vertex detector*. PhD thesis, University of Bonn, 2005. urn: [nbn:de:hbz:5N-06585](https://nbn-resolving.org/urn:nbn:de:hbz:5N-06585).
- [102] M. Trimpl et al. Performance of a DEPFET pixel system for particle detection. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 568:201–206, 2006. doi: [10.1016/j.nima.2006.05.278](https://doi.org/10.1016/j.nima.2006.05.278).
- [103] Y. Tsividis. *Operation and Modeling of the MOS Transistor*. Oxford University Press, 1999.
- [104] J. W. Tukey. *Exploratory Data Analysis*. Addison-Wesley, 1977.
- [105] J. Ulrici et al. Spectroscopic and imaging performance of DEPFET pixel sensors. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 465:247–252, 2001. doi: [10.1016/S0168-9002\(01\)00401-6](https://doi.org/10.1016/S0168-9002(01)00401-6).
- [106] Y. Ushiroda et al. Measurement of the time-dependent CP-violating asymmetry in $B^0 \rightarrow K_S^0 \pi^0 \gamma$ decays. *Phys. Rev. Lett.*, 94(23):231601, Jun 2005. doi: [10.1103/PhysRevLett.94.231601](https://doi.org/10.1103/PhysRevLett.94.231601).
- [107] J. Velthuis et al. Status of DEPFET. *Nucl. Instrum. Methods Phys. Res., Sect. A*, 569(1):57 – 60, 2006. ISSN 0168-9002. doi: [DOI: 10.1016/j.nima.2006.09.012](https://doi.org/10.1016/j.nima.2006.09.012).
- [108] J. J. Velthuis et al. A DEPFET based beam telescope with submicron precision capability. *IEEE Trans. Nucl. Sci.*, 55:662–666, 2008. doi: [10.1109/TNS.2007.914031](https://doi.org/10.1109/TNS.2007.914031).
- [109] M. Vogel and B. Cole. Power-integrity and ground-bounce simulation of high-speed pc boards. *EDN*, pages 83–88, Sept. 2003.
- [110] J.-T. Wei et al. Measurement of the differential branching fraction and forward-backward asymmetry for $B \rightarrow K^{(*)} l^+ l^-$. *Phys. Rev. Lett.*, 103(17):171801, Oct 2009. doi: [10.1103/PhysRevLett.103.171801](https://doi.org/10.1103/PhysRevLett.103.171801).

- [111] Q. Wei. *Studies of Radiation Hardness of MOS Devices for Application in a Linear Collider Vertex Detector*. PhD thesis, Technische Universität München, 2008. urn: [nbn:de:bvb:91-diss-20080725-668264-1-4](https://nbn-resolving.org/urn:nbn:de:bvb:91-diss-20080725-668264-1-4).
- [112] S. Weir. *Considerations for Capacitor Selection in FPGA Designs*. Teraspeed Consulting Group, 2005.
- [113] S. Weir. *High Performance FPGA Bypass Networks*. DesignCon 2005. Teraspeed Consulting Group, 2005.
- [114] R. J. Widlar. Biasing scheme especially suited for integrated circuits. US patent 3,364,434, Jan. 1968.
- [115] X2Y Attenuators, LLC. *X2Y Capacitors for FPGA Decoupling*. Application Note 3007, 2004.
- [116] X2Y Attenuators, LLC. *Understanding Capacitor Inductance and Measurement in Power Bypass Applications*. Application Note 3009, 2006.
- [117] XILINX. Virtex-4 documentation. Family overview (DS112), Data sheet DC and switching characteristics (DS302), FPGA user guide (UG070), Packaging and pinout specification (UG075), FPGA configuration user guide (UG071), PCB designer's guide (UG072), 2004–2010. URL www.xilinx.com.