

System Tests and Qualification of Pixel Modules and DC-DC Converters for the Phase-1 Upgrade of the CMS Pixel Detector

Von der Fakultät für Mathematik, Informatik und Naturwissenschaften
der RWTH Aachen University zur Erlangung des akademischen Grades
eines Doktors der Naturwissenschaften genehmigte Dissertation

vorgelegt von

M.Sc. Martin Lipinski

aus

Lübz

Berichter: Univ.-Prof. Dr. rer. nat. Lutz Feld

Univ.-Prof. Dr. rer. nat. Jörg Pretz

Tag der mündlichen Prüfung: 01.02.2019

Diese Dissertation ist auf den Internetseiten der Universitätsbibliothek verfügbar.



Zusammenfassung

Das CMS Experiment am Large Hadron Collider (LHC) verfügt über einen Silizium-Pixeldetektor, mit dem Spuren von geladenen Teilchen gemessen werden. Durch stetige Verbesserungen des LHC erreichte die instantane Luminosität während des sogenannten Run 2 bereits das doppelte des ursprünglichen Designwerts von $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Um von den zusätzlichen Daten profitieren zu können, hat die CMS Kollaboration im Rahmen des Phase-1 Upgrades einen neuen Pixeldetektor entwickelt, der über eine zusätzliche vierte Lage von Pixelmodulen im Zentralbereich und eine zusätzliche dritte Lage in den Endkappen verfügt. Durch eine verbesserte Ausleseelektronik wurde die Effizienz der Datennahme erhöht. Der neue Detektor wurde im März 2017 in das Experiment eingebaut.

Im Rahmen dieser Arbeit wurde die Qualitätssicherung von Pixelmodulen, die vom Karlsruher Institut für Technologie für einen Teil des Zentraldetektors produziert wurden, durchgeführt. Dafür wurden ein Setup für zyklische Temperaturwechsel und für elektrische Tests sowie ein Röntgensetup für Hochratentests und eine Energiekalibration entwickelt. In dieser Dissertation werden die Setups und die Testprozeduren dargestellt und die Ergebnisse der Pixelmodulqualifikation diskutiert. Von insgesamt 409 produzierten Pixelmodulen wurden 343 Stück (84%) als für den Detektor verwendbar klassifiziert. Ein Großteil der letztlich aussortierten Pixelmodule (43 von 48) bestand den Test im Röntgensetup nicht.

Der im Vergleich zum ursprünglichen Detektor etwa verdoppelte Stromverbrauch des Phase-1 Pixeldetektors hat die Entwicklung eines neuen Konzepts zur Spannungsversorgung nötig gemacht. Um Spannungsabfälle und Leistungsverluste auf den Versorgungskabeln zu reduzieren, werden strahlungstolerante und magnetfeldresistente DC-DC Konverter innerhalb von CMS eingesetzt, welche die Versorgungsspannungen der Auslesechips bereitstellen. In dieser Dissertation wird die ordnungsgemäße Funktion der neuen Spannungsversorgung demonstriert. Die dafür durchgeführten Integrations- und Systemtests werden beschrieben. Die Spannungsversorgung mit DC-DC Konvertern verschlechterte die Leistungsfähigkeit der Pixelmodule nicht. Es konnte beispielsweise gezeigt werden, dass die Detektionseffizienz bei einer Bestrahlung mit Photonen mit einer Rate von 120 MHz cm^{-2} auch bei einer Spannungsversorgung mit DC-DC Konvertern bei etwa 99.2% liegt. Neben den Tests wurden auch die Prozeduren für den Betrieb der DC-DC Konverter im Pixeldetektor entwickelt und optimale Betriebsparameter ermittelt.

Im Oktober und November 2017 fielen während des Betriebes des Pixeldetektors etwa 5% der DC-DC Konverter aus. Im Winter 2017/2018 wurden alle DC-DC Konverter aus dem Pixeldetektor extrahiert und untersucht. Bei etwa weiteren 30% der Baugruppen wurden Schädigungen festgestellt. In dieser Arbeit werden Tests zur Problemsuche beschrieben und die Ursache der Defekte diskutiert. Alle DC-DC Konverter wurden durch neu produzierte ausgetauscht. Die durchgeführten Tests zur Qualitätssicherung der neuen Baugruppen werden in dieser Dissertation beschrieben und die Ergebnisse vorgestellt. Bis zum Zeitpunkt der Niederschrift dieser Arbeit im Oktober 2018 sind keine DC-DC Konverter mehr ausgefallen. Es wurden etwa 109 fb^{-1} an Kollisionsdaten mit dem neuen Pixeldetektor aufgezeichnet. Dies übersteigt bereits die mit dem ursprünglichen Pixeldetektor während seiner gesamten Lebenszeit gesammelte Datenmenge.

Abstract

The CMS experiment at the Large Hadron Collider (LHC) features a silicon pixel detector that measures tracks of charged particles. Due to continuous improvements of the LHC, the instantaneous luminosity already reached twice the original design value of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ during the so-called Run 2. In order to benefit from the additional data, the CMS collaboration has developed a new pixel detector, which has an additional fourth layer of pixel modules in the central area and an additional third layer in the endcaps, as part of the Phase-1 upgrade. Improved readout electronics increased the data acquisition efficiency. The new detector was installed in the experiment in March 2017.

Within the scope of this work, the quality assurance of pixel modules, which were built by the Karlsruhe Institute of Technology for a part of the central detector, was performed. A setup for thermal cycling and electrical testing, as well as an X-ray setup for high-rate tests and an energy calibration, were developed for this purpose. In this thesis, the setups and test procedures are presented, and the results of the pixel module qualification are discussed. Out of 409 pixel modules produced, 343 (84%) were classified usable for the detector. A large part of the pixel modules (43 of 48) that were ultimately rejected did not pass the test in the X-ray setup.

The power consumption of the Phase-1 pixel detector has approximately doubled compared to the original detector, making a new powering scheme necessary. In order to reduce voltage drops and power losses on the supply cables, radiation tolerant and magnetic field resistant DC-DC converters are used within CMS to provide the supply voltages for the readout chips. In this thesis, the proper function of the novel powering scheme is demonstrated. The integration tests and system tests that were performed for this purpose are described. The powering with DC-DC converters did not impair the performance of the pixel modules. For example, it was demonstrated that the detection efficiency during irradiation with photons at a rate of 120 MHz cm^{-2} is about 99.2 %, even when DC-DC converters power the pixel module. In addition to the performed tests, the procedures for operating the DC-DC converters in the pixel detector were developed and optimal operating parameters determined.

In October and November 2017, about 5% of the installed DC-DC converters failed during operation of the pixel detector. All DC-DC converters were extracted from the pixel detector and examined in winter 2017/2018. Damage was found in about 30% additional devices. In this thesis, the troubleshooting is described, and the cause of the defects is discussed. All DC-DC converters have been replaced by newly produced ones. This thesis describes the quality assurance tests that were performed and presents the results. By the time of writing of this work in October 2018, no DC-DC converters have failed. About 109 fb^{-1} of collision data have been recorded with the new pixel detector. This already exceeds the amount of data collected by the original pixel detector during its entire lifetime.

Contents

Introduction	1
1. The CMS Experiment at the Large Hadron Collider	5
1.1. The Large Hadron Collider	5
1.2. The CMS Experiment	8
1.2.1. Silicon Tracker	9
1.2.2. Calorimetry System	11
1.2.3. Muon System	12
1.2.4. Trigger System	13
1.2.5. Upgrades of the CMS Detector	13
2. The CMS Phase-1 Pixel Detector	17
2.1. Overview	17
2.2. Pixel Module	18
2.2.1. Design	19
2.2.2. Sensor	21
2.2.3. Readout Chips	21
2.2.4. Token Bit Manager	25
2.3. Detector Control and Readout	26
2.3.1. Data Acquisition	26
2.3.2. Detector Control	27
2.4. Power System	28
2.4.1. Buck Converters	29
2.4.2. PixV13 DC-DC Converter	31
2.4.3. Power Distribution within the Pixel Detector	33
2.4.4. Power Supplies	35
2.5. Detector Geometry	37
2.6. Supply Tubes and Service Cylinders	40
2.7. Cooling	42
3. Qualification of Pixel Modules	43
3.1. Module Production at KIT	44
3.2. Quality Assurance at RWTH Aachen	47
3.3. Cold Tests	51
3.3.1. Description of the Setup	51
3.3.2. Test Procedure	56

3.4.	X-Ray Tests	69
3.4.1.	The X-Ray Setup	71
3.4.2.	High Rate Test	74
3.4.3.	Energy Calibration	83
3.5.	Course of the Series Production	85
3.5.1.	Results of Cold Box Tests	87
3.5.2.	Results of High Rate X-ray Tests	89
3.5.3.	Results of the Energy Calibration	92
3.6.	Reception Test	94
4.	Integration Tests and System Tests of the Power System	99
4.1.	The System Test Setup	99
4.2.	Expected Front-End Currents of the Phase-1 Pixel Detector	102
4.3.	Voltage Drops	103
4.4.	Transient Response	109
4.4.1.	Power-on Procedure without Load	109
4.4.2.	Power-on Procedure with nominal Loads and enabled DC-DC Converters	111
4.4.3.	Power-on Procedure with nominal Loads and disabled DC-DC Converters	112
4.4.4.	Validation of the Remote Sensing Functionality	113
4.4.5.	Power-off Procedure	116
4.4.6.	Overcurrent Protection	118
4.4.7.	Implications of Power Cycles on the Fuses	119
4.5.	Tests with Pixel Modules	120
4.5.1.	Noise Measurements	121
4.5.2.	X-Ray Measurements	123
4.6.	The long-term Test Setup	127
5.	Detector Commissioning	133
5.1.	Commissioning of the Barrel Pixel Detector	133
5.1.1.	Overview	133
5.1.2.	Test Procedures	135
5.1.3.	Results	140
5.2.	Investigation of blown Fuses	142
5.2.1.	Optimization of the Power Supply Voltage	142
5.2.2.	Calculation of the Trip Limits	148
5.2.3.	Operation of the Power System in 2017	149
5.2.4.	Operation of the Power System in 2018	150
6.	Investigation and Replacement of defective DC-DC Converters	153
6.1.	Failure Investigation	154
6.1.1.	Measurements in the System Test Setup	156
6.1.2.	Controlled Damaging of DC-DC Converters	160

6.2.	Extraction of DC-DC Converters from CMS	164
6.2.1.	The DC-DC Converter Test Setup	164
6.2.2.	Investigation of defective DC-DC Converters	166
6.2.3.	Investigation of working DC-DC converters	168
6.2.4.	A Model for the Damage	170
6.3.	Production of PixV14 DC-DC Converters	172
6.3.1.	Overview of the Qualification Tests	173
6.3.2.	Electrical Test before the Mounting of the Shield	174
6.3.3.	Thermal Cycling	176
6.4.	Results	180
7.	Summary and Outlook	183
A.	Appendix	189
A.1.	DC-DC Converters	189
A.2.	Photographs of Supply Tube Boards	192
A.3.	Pixel Module Qualification	193
A.4.	Optimization of the Power Supply Output Voltages	195
	Bibliography	197
	Acknowledgements	205

List of Figures

1.1.	Schematic view of the LHC complex.	6
1.2.	Foreseen LHC luminosity until 2037.	7
1.3.	Schematic view of the CMS detector.	8
1.4.	Schematic view of the CMS silicon tracker.	10
2.1.	Exploded view of the Phase-1 pixel detector.	18
2.2.	Schematic view of the Phase-1 pixel modules	20
2.3.	Simplified schematic of the pixel unit cell.	22
2.4.	Readout scheme of the PSI46dig chip.	24
2.5.	Readout scheme of the Phase-1 pixel modules.	26
2.6.	Overview of the data acquisition system of the Phase-1 pixel detector.	27
2.7.	Working principle of a buck converter.	30
2.8.	Photographs of PixV13 DC-DC converters	33
2.9.	Schematic view of the power distribution in the barrel pixel detector.	34
2.10.	Photograph of the bus board.	34
2.11.	Powering scheme of the Phase-1 pixel detector.	37
2.12.	Comparison of the Phase-1 and the Phase-0 detector layouts.	38
2.13.	Schematic view and photograph of the barrel detector.	39
2.14.	CAD model of a FPix half disk.	39
2.15.	CAD model of a BPix supply tube.	41
2.16.	CAD model of the FPix service cylinder.	41
3.1.	Pixel module production workflow within the KIT/RWTH Aachen consortium.	45
3.2.	Photographs of a layer 4 pixel module.	46
3.3.	Testboard and software used for the pixel module readout.	48
3.4.	Webpage created by MoReWeb.	50
3.5.	Photograph of the cold box setup.	52
3.6.	CAD drawing of the different layers of the cooling system.	53
3.7.	Photograph of the cold box with opened lid.	54
3.8.	User interface of the control software of the cold box setup.	55
3.9.	Cooling block temperature profile of a complete test sequence.	56
3.10.	Optimization of the calibration pulse time delay.	57
3.11.	Result of the PixelAlive test.	58
3.12.	Measurement of the electronic noise with so-called S-curves.	60
3.13.	Results of the threshold optimization.	62

3.14. Two-dimensional scans of PHScale vs. PHOffset.	64
3.15. Pulse height calibration of two pixels.	66
3.16. Results from the readback calibration of one readout chip.	67
3.17. Current-voltage characteristics of five pixel module sensors.	69
3.18. Energy spectra measured in the X-ray setup.	70
3.19. Photograph of the X-ray setup.	72
3.20. Photographs of the measurement chamber.	73
3.21. User interface of the control software of the X-ray setup.	74
3.22. X-ray hit map of a pixel module.	77
3.23. Results from two modules that failed the readout uniformity tests. . . .	78
3.24. Noise and signal thresholds in the cold box and the X-ray setup.	79
3.25. Efficiency of a psi46digV2 ROC vs. hit rate.	81
3.26. Efficiency map of module M4634.	82
3.27. Energy calibration of the Vcal DAC.	84
3.28. Progress of the pixel module production of the KIT/RWTH Aachen consortium.	85
3.29. Numbers of useable and rejected or damaged pixel modules.	86
3.30. Results of the I-V measurement in the cold box.	88
3.31. Difference in the number of bump bond defects before and after thermal cycling.	88
3.32. Number of defective pixels per module.	90
3.33. Comparison of results from the bump bond test in the cold box and the X-ray test.	90
3.34. Module map of missing bump bonds.	91
3.35. Number of defective or disconnected pixel cells.	91
3.36. X-ray hit detection efficiencies at 120 MHz cm^{-2}	92
3.37. Distribution of Vcal conversion factors.	93
3.38. Average Vcal-electron conversion factor per pixel module.	93
3.39. Photograph of the protective cover of a pixel module.	95
3.40. Comparison of sensor leakage currents before and after mounting of the protective covers.	96
3.41. Examples of I-V curves that had significantly changed between the full qualification and the reception test.	97
4.1. Photograph of the system test setup.	100
4.2. Photograph of the PCBs used in the system test setup.	101
4.3. Expected pixel module currents at $L_{\text{inst}} = 2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$	103
4.4. Voltage drops across V+ and return of the supply tube boards.	105
4.5. Measured and calculated voltage drops in several supply tube sections. . . .	107
4.6. DC-DC converter input voltage margin.	108
4.7. Power-on procedure without loads.	110
4.8. Power-on procedure with nominal module currents drawn from all DC-DC converters.	112
4.9. Enabling of all DC-DC converters.	113

4.10. Comparison of disabled and enabled remote sensing.	115
4.11. Output voltage of the DC-DC converters with enabled remote sensing.	115
4.12. Power-off procedure with nominal loads.	117
4.13. Power-off by disabling DC-DC converters.	117
4.14. Evolution of the power supply current during a power trip.	118
4.15. Photograph of a pixel module in the system test setup.	121
4.16. S-curve measurements with module M4558 in the system test setup.	122
4.17. S-curve measurements during X-ray illumination.	124
4.18. Hit detection efficiencies at X-ray hit rates of 50 MHz cm^{-2} and 120 MHz cm^{-2}	125
4.19. Results from the Vcal calibration with X-rays.	126
4.20. Photograph of the long-term test setup.	127
4.21. Voltage drop across the fuse on the DC-DC converters.	129
4.22. Voltage drops across the fuses of two DC-DC converters over time.	131
5.1. Photograph of one half of the barrel pixel detector.	134
5.2. Result of a POH bias scan.	135
5.3. SDA scan with layer 1 and layer 2 pixel modules of one BPix sector.	136
5.4. Two-dimensional scan of the TBM PLL delays of one pixel module.	138
5.5. PixelAlive test with sensor bias voltage turned on and off.	139
5.6. Electronic noise of pixel modules with sensor bias voltage turned on and off.	139
5.7. Reconstructed hit clusters during a data taking period in June 2017.	141
5.8. Analog and digital power supply currents before and after programming.	143
5.9. Largest possible voltage drops across the supply cables.	146
5.10. Lowest allowed output voltage of the power supplies.	146
5.11. Input voltage of the DC-DC converters in the event that the activity of the readout chips suddenly drops to zero.	148
5.12. Output currents of all digital power supply channels at $L_{\text{inst}} = 2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$	149
6.1. Input currents of one FPix power group during a powercycle.	156
6.2. Total input current of several DC-DC converters connected in parallel.	158
6.3. Input current as a function of the input voltage in the FPix detector.	159
6.4. I-V curves of one DC-DC converter, which was repeatedly subjected to overvoltage at the input.	161
6.5. I-V curve of one damaged and three working DC-DC converters.	162
6.6. Measurement of the capacitance as a function of the bias voltage and the frequency.	164
6.7. Photograph of the setup for testing DC-DC converters.	165
6.8. User interface of the control software of the DC-DC converter test setup.	166
6.9. Characterization of DC-DC converters that were extracted from CMS.	169
6.10. Distribution of the defective and high-current DC-DC converters in the BPix supply tubes.	169

6.11. Test sequence of the electrical test at the assembly company.	175
6.12. Distributions of the output voltages and the measured conversion efficiencies.	176
6.13. Photograph of the setups used for thermal cycling of DC-DC converters.	177
6.14. Photograph of DC-DC converters in the thermal cycling setup.	178
6.15. Data measured during the thermal cycling.	179
6.16. X-ray images of DC-DC converters	180
6.17. Hit efficiency as a function of the instantaneous luminosity.	181

List of Tables

2.1.	DC-DC converter pairs per layer and number of pixel modules connected.	35
3.1.	Grading criteria for the pulse height calibration.	66
3.2.	K_α -transition energies of targets used for the energy calibration.	84
3.3.	Final results of the pixel module qualification at RWTH Aachen and the reception test.	97
4.1.	Effects considered for the calculation of the minimum input voltage. . .	108
4.2.	Temperature scaling factors of the voltage drop across fuses.	131
5.1.	Estimated output currents of digital DC-DC converters at $L_{\text{inst}} = 2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$	144
6.1.	Input currents of a DC-DC converter at different input voltages.	157
6.2.	Numbers of tested, defective, and high-current DC-DC converters. . . .	170

Introduction

Since its development in the 1960s and 1970s, the Standard Model of particle physics has proven to be an outstanding theory that precisely predicts many observables from the smallest scales up to astrophysical observations. The last missing piece of the Standard Model, the Higgs boson, was observed in 2012 [1, 2] by the CMS and ATLAS experiments at the European Organization for Nuclear Research (CERN) [3]. However, the Standard Model is considered an incomplete theory because it cannot, for example, describe gravity or explain the constituents of dark matter, which makes up about 25 % of the universe. New models such as supersymmetric theories and theories with extra dimensions could answer these questions. They predict new effects and particles, which may be detected by experiments at particle accelerators.

The Large Hadron Collider (LHC) [4] at CERN is designed to collide protons with a center-of-mass energy of 14 TeV at an instantaneous luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The properties of particles that are created in these collisions are measured, amongst others, by the CMS detector (Compact Muon Solenoid). With a size of $21 \times 15 \times 18 \text{ m}^3$ and a weight of about 14 000 t, it is one of the largest particle detectors built to date.

The LHC is undergoing a continuous upgrade program. The center-of-mass energy was increased in two steps from an initial 7 TeV to the current 13 TeV. The instantaneous luminosity has reached a peak value of $2.13 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ in 2018. At the time of writing this thesis, an integrated luminosity of 190 fb^{-1} has been delivered to CMS [5].

A high instantaneous luminosity makes it possible to find rare events more quickly. However, this also increases the number of particles traversing CMS simultaneously. In order to benefit from the additional data, the granularity and the readout bandwidth of the detector have to be improved. The CMS collaboration, therefore, foresees two major upgrades. The Phase-1 upgrade, which is expected to be completed by the end of 2019, is intended to ensure an efficient operation at an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The most significant change within this upgrade is the development of a new pixel detector, which was installed in CMS in March 2017. The number of readout channels of the Phase-1 pixel detector almost doubled compared to the original pixel detector. Upgraded readout chips and new readout electronics ensure that inefficiencies, which are caused by a limited readout bandwidth, remain small. A novel powering scheme involving radiation tolerant DC-DC converters was developed to reduce power losses on the supply cables. Voltages of approximately 10 V are transmitted to DC-DC converters located within CMS, which convert them to voltages of 2.4 V to 3.5 V. On-detector DC-DC converters are used for the first time in a high-energy physics

detector. The experience gained during the development, installation, and operation of the power system is important for many other experiments as well.

From 2024 onwards, the LHC will be upgraded to the High-Luminosity LHC (HL-LHC), which will provide an instantaneous luminosity of at least $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The high rate of particle collisions and progressing radiation damage make the CMS Phase-2 upgrade necessary. Almost all subsystems of the CMS detector will be improved. For example, the entire CMS silicon tracking system will be replaced.

Within the scope of this work, important contributions to the construction and commissioning of the CMS Phase-1 pixel detector were made. The new pixel detector comprises 1856 pixel modules which were produced by several institutes. A consortium of the Karlsruhe Institute of Technology (KIT) and RWTH Aachen University was responsible for the production and testing of a portion of the pixel modules. They were built at KIT and were qualified at RWTH Aachen University. These tests ensured that only perfectly functioning pixel modules were installed in the detector. Within the scope of this work, the required test setups were developed. The functionality of the qualification procedures was verified with prototypes of the pixel modules. Subsequently, 389 pixel modules from the final production were tested, and the data were analyzed. A cold box setup was developed based on preliminary work [6]. A control software was developed, with which the tests were carried out automatically. An X-ray setup, which was built in a preceding work [7], was further optimized. The test procedure for high rate tests was developed, and grading criteria were defined. The procedure was adopted by all institutes involved in the pixel module production.

Several parts of the power system were developed at RWTH Aachen University. These include the DC-DC converters as well as several electrical boards, which are used for distributing voltages in the central area of the pixel detector (which is called BPix). One aim of this work was to validate the proper functioning of the new power system. Therefore, integration tests and system tests were carried out. A system test setup was developed, which accurately replicates the situation in the BPix detector. The setup was built with prototypes of the components and was continuously expanded when final components were available. Among other things, voltage drops and the transient behavior of the power system were examined. Recommendations for the output voltage of the DC-DC converters were derived from the results. Furthermore, the influence of DC-DC converters on the electronic noise and the efficiency of pixel modules was measured. Additionally, the aging of fuses on the DC-DC converters was investigated.

The entire BPix detector was tested at Paul Scherrer Institute (PSI) after assembly and again after the transport to CERN. As part of this work, contributions were made to the commissioning tests. The output voltages of the power supplies were optimized. Furthermore, new operating procedures for the turn-on and turn-off of the power system were developed.

After the pixel detector was operated in 2017 for about half a year, about 5 % of the DC-DC converters broke. Because the DC-DC converters are located inside CMS and

are thus not accessible, the cause of the failure was not known. As part of this work, it was tried to reproduce the failure mode in laboratory experiments. New DC-DC converters had to be produced and tested on a very tight schedule. Therefore, the previously mentioned setup for testing pixel modules was modified, to duplicate an existing setup for thermal cycling of DC-DC converters. Furthermore, a setup was developed with which DC-DC converters were tested at the assembly company.

The pixel detector was extracted from CMS in the year-end technical stop in winter 2017, and the DC-DC converters were replaced. In the context of this work, the extracted DC-DC converters were examined to find the cause of the defects.

This thesis is structured as follows: The first chapter gives a short overview of the design of the LHC and the CMS experiment, and the planned and already implemented upgrades. Chapter 2 describes the design of the Phase-1 pixel detector. A particular focus lies on the design of the pixel modules, the DC-DC converters, and the BPix power system. Chapter 3 describes the tests of 389 pixel modules, which were built at KIT and qualified at RWTH Aachen University. Pixel modules were electrically tested and thermally cycled in a cold box setup (Section 3.2). High rate tests and an energy calibration were performed in an X-ray setup (Section 3.3). Chapter 4 is dedicated to system tests with the Phase-1 BPix power system. Chapter 5 describes the commissioning of the pixel detector. After assembly, the entire BPix detector was tested, and optimal operating parameters were determined that are required for data acquisition in CMS. Section 5.1 explains the test procedures and summarizes the results. Section 5.2 is dedicated to the optimization of output voltages and current limits of the power supplies. Chapter 6 deals with the failure of DC-DC converters in 2017. The tests that were performed to reproduce the failure mode observed in CMS are described. The production of new DC-DC converters is summarized.

1. The CMS Experiment at the Large Hadron Collider

1.1. The Large Hadron Collider

The Large Hadron Collider is the most powerful particle accelerator ever built. It is operated by the European Organization for Nuclear Research (CERN) and is located in a tunnel at the France-Switzerland border close to Geneva, about 45 m to 175 m below ground level. The LHC is a synchrotron with 27 km circumference, designed to collide two counter-rotating proton beams at a center-of-mass energy of 14 TeV. The design luminosity is $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ at a bunch spacing (the time between collisions) of 25 ns. For some weeks of the year, there are also special runs in which heavy ions are brought into collision.

A large pre-accelerator complex is used to fill the LHC, as shown in Figure 1.1. As a first step, hydrogen atoms are ionized to create protons, which are then accelerated by a linear accelerator (LINAC2). Multiple circular accelerators, namely the Proton Synchrotron Booster (PSB), the Proton Synchrotron (PS), and the Super Proton Synchrotron, accelerate bunches of protons to energies of 450 GeV. Up to 2802 bunches circulate in the LHC. Superconducting magnets with a field strength of up to 8 T keep the particles on orbit and radio frequency cavities accelerate the particles to their final energy.

There are four interaction points where beams are crossed, and particles collide. Four large experiments record the collisions. Two general purpose experiments, ATLAS [9] and CMS [10], investigate a broad range of physics. These include precision measurements of Standard Model parameters, search for the Higgs boson and search for new physics beyond the Standard Model, e.g., Supersymmetry. The LHCb [11] experiment is specialized on b-hadron measurements, to investigate CP-violation and rare decays. The fourth experiment, ALICE [12], focuses on heavy ion physics.

More than two decades of research, development, and construction were required to build the LHC. It was installed in the tunnel of the Large Electron-Positron Collider (LEP), which had been operated from 1989 to 2000. The CERN Council approved construction of the LHC with four associated experiments in 1994 [13, 14]. The original plan foresaw a two-stage construction with the first commissioning of the LHC starting in 2002. However, in the following years, these plans were revised, because the funding

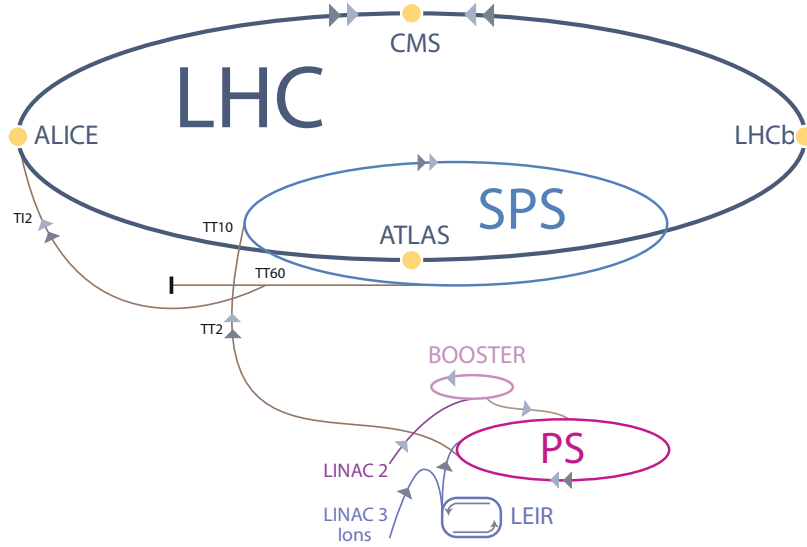


Figure 1.1.: Schematic view of the LHC, the pre-accelerators, and the four interaction points with the experiments ALICE, ATLAS, LHCb, and CMS. Modified from [8].

situation and also the overall cost estimate changed [15]. The LHC was built for the foreseen center-of-mass energy of 14 TeV in a single step. The commissioning started in 2008.

In September 2008, the first beam circulated in the LHC. Only a few days later, an electrical arc developed in one of the magnets due to a faulty electrical connection, resulting in a leak of the helium cooling system. The rapidly expanding helium damaged 53 magnets, which had to be repaired. Thus, the first collisions were delayed about one year until November 2009. For safety reasons the LHC was operated with a center-of-mass energy of 7 TeV in 2010 and 2011, which was then raised to 8 TeV in 2012. The bunch spacing was 50 ns at that time. During this so-called Run 1, an integrated luminosity of about 6.1 fb^{-1} was delivered at 7 TeV and 23.1 fb^{-1} at 8 TeV, respectively. The main achievement during this run was the discovery of the Higgs boson by the ATLAS and CMS collaborations.

The LHC complex, including the pre-accelerators, is undergoing a continuous upgrade program to improve the overall performance, especially to increase the instantaneous luminosity. The machine was shut down in early 2013 for a two-year long upgrade in which the pre-accelerators were upgraded, and the connections of all 1232 superconducting magnets were improved to allow the operation at the design energy. In 2015, the LHC was restarted for Run 2 with a center-of-mass energy of 13 TeV. The bunch spacing was reduced to 25 ns. This improvement reduces the number of interactions per bunch-crossing, known as pileup, by a factor of two. The instantaneous luminosity could be increased continuously, reaching the design value of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ for

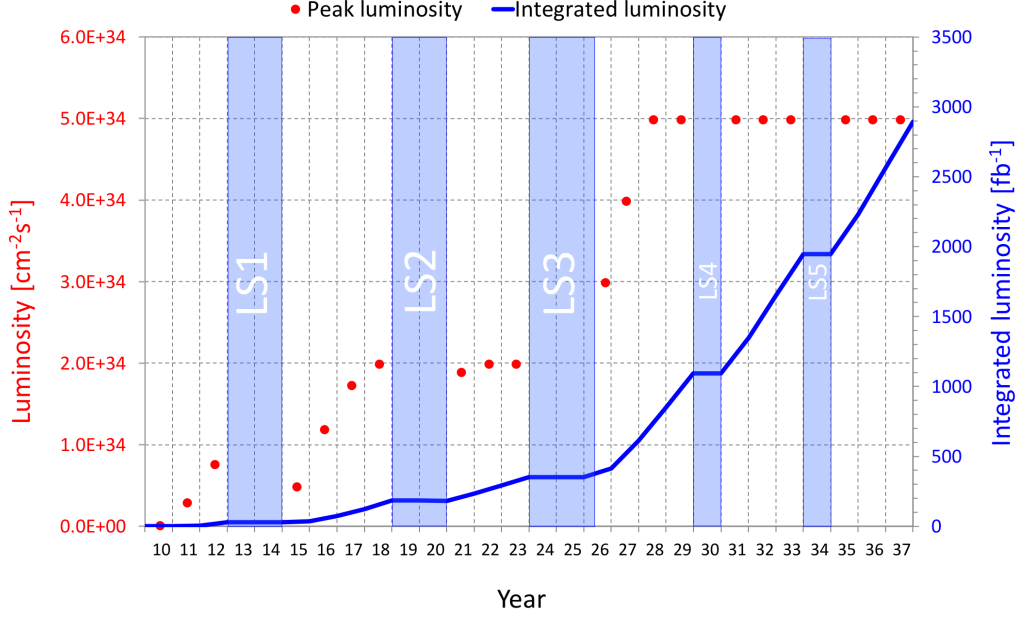


Figure 1.2.: Foreseen instantaneous luminosity (red dots) and integrated luminosity (blue line) of the LHC for the next two decades. Long shutdown periods are indicated [18].

the first time in 2016. This value already doubled in 2017, with the peak instantaneous luminosity reaching up to $2.06 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ in a few runs. About 190 fb^{-1} of proton-proton collision data have been delivered [16] to CMS until the time of this writing.

Within the next ten years, two major upgrades are foreseen to increase the luminosity further, as depicted in Figure 1.2. During the Phase-1, which is currently ongoing and extends until 2023, the instantaneous luminosity is increased to at least $2.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. This goal has already been achieved. Nevertheless, large parts of the injector chain will be improved in a technical stop in 2019 and 2020, which is called Long Shutdown 2 (LS2)¹. For example, a new linear accelerator (LINAC4) will replace LINAC2 to reduce the beam emittance. It is anticipated that until the end of Phase-1 an integrated luminosity of 300 fb^{-1} will be delivered by the LHC to ATLAS and CMS.

Phase-2 starts in 2026, after the Long Shutdown 3 (LS3). Within the scope of the High-Luminosity LHC project (HL-LHC) [17], the LHC will be upgraded during LS3 to reach an instantaneous luminosity of at least $5.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and the design energy of 14 TeV. The current plan foresees that the HL-LHC will deliver at least a further 2500 fb^{-1} .

¹During a technical stop, the LHC is shut down for maintenance.

1.2. The CMS Experiment

The CMS detector (Compact Muon Solenoid) measures the properties of particles emerging from high energy collisions at the LHC. The detector is located on the French side of the LHC ring in the village Cessy, at the so-called Point 5, in a cavern about 100 m underground. It has a length of 21 m, a diameter of 15 m and a weight of about 14 000 t. The symmetric detector consists of a barrel part and two endcaps. The interaction point (IP) lies in the center of the detector.

A central feature of CMS is the superconducting solenoid with a field strength of 3.8 T and an inner diameter of 6 m. In the magnetic field charged particles move in a circular motion. The bending radius and the bending direction are used to estimate the particle momentum and charge. Within the field volume, there are multiple subsystems, as shown in Figure 1.3. The innermost parts are the high-granularity silicon pixel detector and the silicon microstrip tracker. These subdetectors provide space point measurements of charged particle trajectories and thus allow the estimation of the particle momentum. The energies of particles that pass through the tracker are measured with a crystal electromagnetic calorimeter and a brass-scintillator hadron calorimeter.

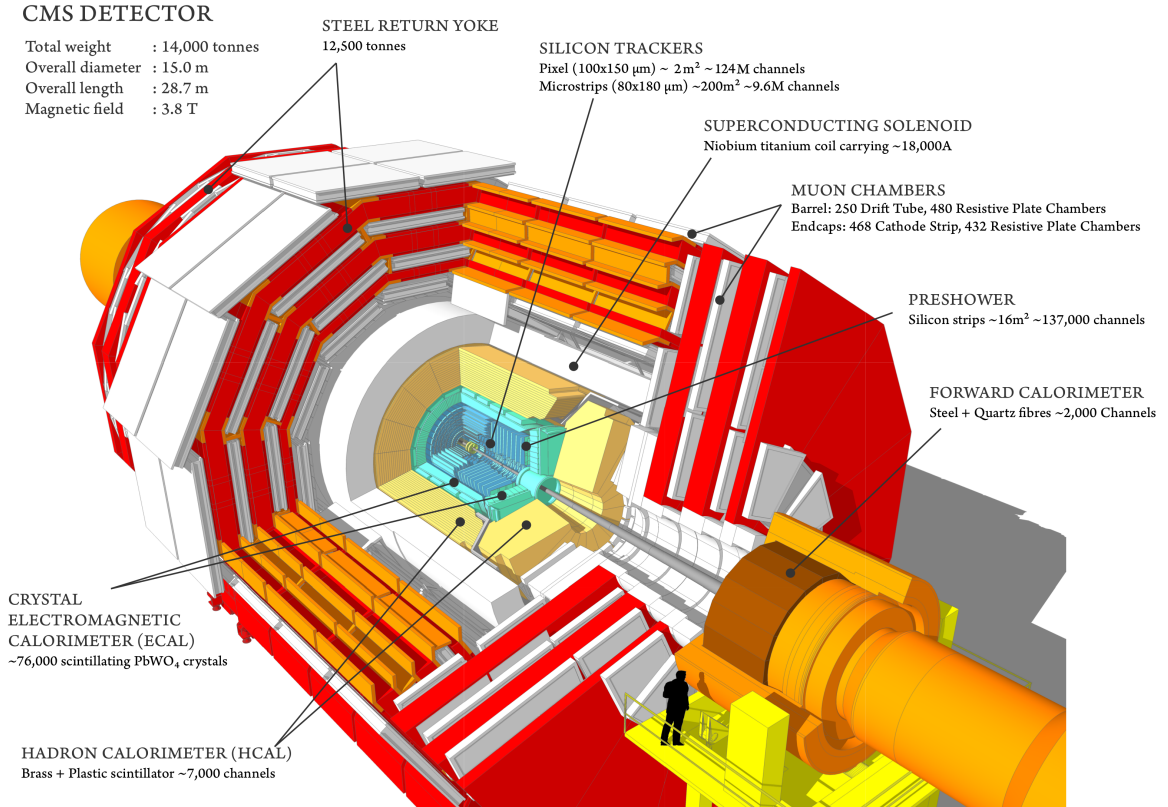


Figure 1.3.: Schematic view of the CMS detector. Modified from [19].

calorimeter. The magnet is surrounded by a steel return yoke that guides the field lines and also contains the muon chambers. While most particles are stopped within the calorimeters, muons interact only little with the material and can thus travel through the whole detector. The muon system, which is made of gaseous detectors, is used to measure their momentum.

CMS uses a right-handed coordinate system, which has its origin in the center of the detector. The coordinate system is oriented such that the x -axis points towards the center of the LHC ring, the y -axis points upwards and the z -axis points along the anticlockwise-beam direction. The azimuthal angle ϕ is measured from the positive x -axis in the xy -plane. The polar angle θ is measured from the positive z -axis. Instead of the polar angle the pseudorapidity η is widely used, which is defined as $\eta = -\ln[\tan(\theta/2)]$.

1.2.1. Silicon Tracker

The CMS experiment comprises a large silicon tracker [20, 21] to measure the momenta and the trajectories of charged particles. The transverse momentum resolution is 0.7 % at 1 GeV and 5.0 % at 1000 GeV. The transverse impact parameter resolution for high-momentum tracks is about 10 μm [22]. The latter is important especially for the reconstruction of scattering processes involving heavy particles like bottom quarks, τ -leptons or other possible non-standard model particles emerging from the proton-proton collisions. These can travel a short distance (typically a few μm to a few mm) through the detector before decaying, hence creating a displaced secondary vertex. A good spatial resolution is required to be able to attribute tracks to the correct vertices. Another challenge is the so-called pileup, which is caused by multiple proton-proton interactions in the same bunch crossing. At the CMS design luminosity of $1.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and a bunch spacing of 25 ns about 25 inelastic proton-proton interactions occur on average per bunch crossing, creating about 1000 charged particle tracks in the detector. Hence a low occupancy is required to avoid matching ambiguities. On the other hand, a large number of active channels requires more electrical power and cooling, increasing the mass of the detector. The tracking detector, however, has to be lightweight to reduce interactions with the detector material, which worsen the overall momentum and energy resolution. The CMS tracker is split into two subsystems, a high-granularity pixel detector very close to the interaction point and a large microstrip detector with an active area of 200 m^2 . The cylindrical tracking volume measures 2.6 m in diameter and is 5.8 m long. The geometry of the tracker is shown in Figure 1.4.

The pixel detector consists of a 53 cm long cylindrical barrel part (BPix) and a forward detector (FPix) with two endcaps at each side of the barrel, allowing the tracking of particles up to a pseudorapidity of $|\eta| < 2.5$. In BPix, individual pixel modules are aligned in several layers at different radii parallel to the beam axis. In the FPix detector, pixel modules are oriented perpendicular to the beam axis to reduce the material the particles have to traverse.

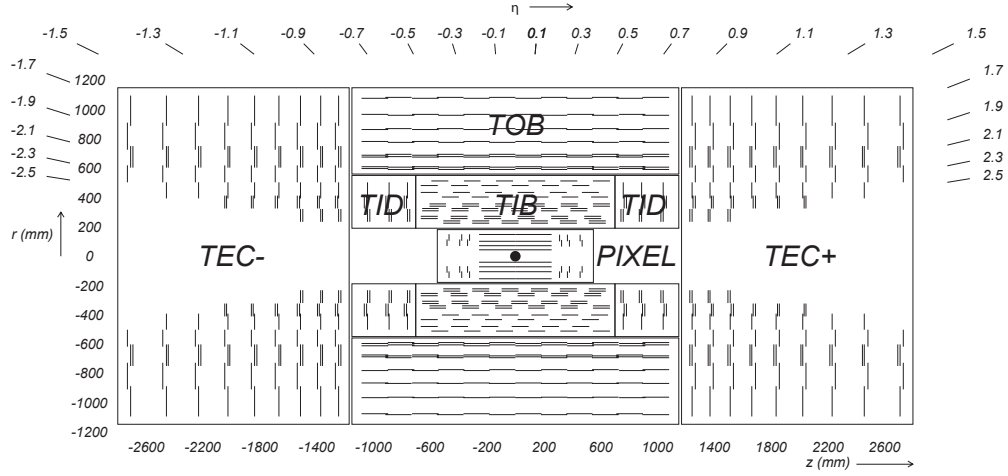


Figure 1.4.: Schematic view of the CMS silicon tracker in the rz -view. Each line represents a module. Modified from [10].

The original pixel detector that was installed in CMS featured three layers of pixel modules in the barrel and two layers in each endcap, allowing a full 3-hit coverage in the whole tracking region. Hereafter, this detector is referred to as the Phase-0 pixel detector. A new pixel detector was installed in 2017 as a part of the CMS Phase-1 upgrade to maintain a high tracking efficiency at the increased instantaneous LHC luminosity. It is thus called the Phase-1 pixel detector. This new detector, which is described in more detail in Chapter 2, features an additional fourth layer of modules in the barrel and an additional third layer in the endcaps.

The Phase-1 pixel detector is constructed from 1856 individual pixel modules. Each has 66 560 pixels, resulting in a total of about 124 million active channels. The pixel size is $100 \times 150 \mu\text{m}^2$. The modules follow a hybrid design, meaning they consist of a sensor and readout chips, which are connected in a flip-chip process. A $285 \mu\text{m}$ thick n^+ -in- n silicon sensor is connected with 16 readout chips (ROC). In principle, a silicon sensor consists of a bulk material and implants, which are doped differently from the bulk material. At the so-called p-n-junction, a charge carrier-free zone is formed, which can be enlarged by applying an external depletion voltage. In this zone, traversing particles generate charge carriers that drift to the electrodes. The readout chips in the Phase-1 pixel detector measure the analog signal height to make use of the charge sharing between neighboring pixels, which improves the position resolution. Particles usually create signal clusters several pixels wide. By considering the pulse height information of individual pixels, the location of the cluster can be determined more precisely than the spatial resolution of an individual pixel would allow. The single hit resolution of a pixel module is about $9 \mu\text{m}$ in $r\phi$ -direction and about $23 \mu\text{m}$ in z -direction [23]. The electrons generated in the sensor move in the magnetic field of CMS and are therefore subjected to a Lorentz force. Thus, charge sharing in the $r\phi$ -direction is enhanced.

The Phase-1 pixel detector features a new two-phase CO₂ cooling system. It is operated at a temperature of -20°C , to mitigate effects of radiation damage in the silicon sensors.

The silicon strip tracker expands the tracking volume up to a radius of 116 cm and has a length of 5.8 m. It is divided into four parts, which differ in design and orientation of the strip modules. The Tracker Inner Barrel (TIB) and the Tracker Outer Barrel (TOB) are composed of four and six layers of modules, respectively, which are oriented parallel to the beam axis. A three-layer Tracker Inner Disk (TID) and a nine-layer Tracker Endcap (TEC) are installed at each side of the barrel. This design allows a coverage with at least 9 hits up to $|\eta| < 2.4$. In total 15 148 modules provide 9.3 million readout channels.

The strip modules have p-in-n-sensors with a thickness of 320 μm at radii smaller than 60 cm and 500 μm at larger radii. The strip pitch ranges from 80 μm in the inner layer of the TIB to 205 μm in layer 6 of the TEC [24]. The length of the strips varies from 10 cm to 20 cm. Four layers of the barrel and three rings of the endcaps are constructed from double-sided modules, which consist of two strip modules mounted back-to-back with a stereo angle of 100 mrad.

1.2.2. Calorimetry System

The purpose of the electromagnetic calorimeter (ECAL) [10] is to measure the energies of electrons and photons. It consists of 75 848 lead tungstate (PbWO₄) crystals that are distributed in a cylindrical barrel ($|\eta| < 1.48$) and two endcaps that cover a pseudorapidity range up to $|\eta| < 3.0$. The crystals have a tapered geometry and are oriented towards the interaction point. Their small front face of $2.2 \times 2.2 \text{ cm}^2$ in the barrel and $2.86 \times 2.86 \text{ cm}^2$ in the endcaps ensures a fine granularity, which is important for the identification of individual particles. Crystals in the barrel have a length of 23 cm, corresponding to about 26 radiation lengths, while in the endcaps crystals have a length of 22 cm, which corresponds to 25 radiation lengths.

Electrons and photons interact with the crystal material and create electromagnetic showers through bremsstrahlung and pair production. Scintillation light emitted in the crystals is captured by photodetectors. The choice of PbWO₄ was motivated by its radiation hardness, fast signal response, short radiation length, and small Molière radius. On the other hand, this material has a low light yield, which requires the use of photodetectors with internal amplification. Light is collected with avalanche photodiodes in the barrel part. In the endcaps, vacuum phototriodes are used because they are more radiation resistant. The energy resolution for electrons created in Z-boson decays was measured to be about 2 % to 5 %, depending on $|\eta|$. The energy resolution for photons from Higgs-boson decays varies between 1.1 % and 5.0 % [25].

A preshower detector made from two layers of lead and silicon strip sensors is placed in front of the calorimeter endcaps. The preshower has a thickness corresponding to 3 radiation lengths and a strip pitch of 2 mm. The much finer granularity compared to

the ECAL crystals helps to distinguish between single photons and photons produced in pairs in pion decays.

The hadronic calorimeter (HCAL) [10] complements the energy measurement. A large geometrical acceptance is required to prevent particles from escaping the detector without being detected. The HCAL is thus composed of a barrel part (HB) ($|\eta| < 1.3$), two endcaps ($1.3 < |\eta| < 3.0$) (HE) and forward calorimeters ($|\eta| < 5.2$) (HF). A few additional layers (HO) are installed as a so-called tail catcher between the solenoid and the first layer of the muon system because the inner diameter of the magnet coil limits the size of the cylindrical barrel. The HB and HO are a sampling calorimeter built from alternating brass absorber plates and plastic scintillator tiles. Incoming particles interact with the absorbers and create particle showers, which in turn make the plastic emit scintillation light. Wavelength shifting fibers are used to collect and send the light to hybrid photodiodes. The forward calorimeters are located outside the magnetic field, about 11 m away from the interaction point. They are built from steel absorbers and quartz fibers, which are read out with photomultipliers.

HCAL is segmented in so-called towers that cover different active areas, depending on the pseudorapidity. The most common tower sizes are 0.087×0.087 ($|\eta| < 2.5$) and 0.17×0.17 ($2.5 < |\eta| < 4.7$) in η and ϕ . Their thickness depends on the pseudorapidity and varies between 7 to 11 nuclear interaction lengths. The use of the CMS coil as an additional absorber in front of the outer calorimeter ensures that more than 10 nuclear interaction lengths are achieved in the whole calorimeter.

1.2.3. Muon System

Muons can traverse the calorimeters without significant energy loss. These particles are identified by gaseous tracking detectors, which are installed in the iron return yoke. The detectors consist of separate electrodes that are surrounded by a gas volume. Traversing particles ionize the gas, resulting in a current flow between the electrodes that can be measured.

Like the other subsystems, the muon system [26] consists of a barrel part ($|\eta| < 1.2$) and is complemented by two endcaps ($0.9 < |\eta| < 2.4$). The barrel region is composed of four layers of drift tube (DT) modules with a size of about $2.0 \times 2.5 \text{ m}^2$ each. A module comprises twelve layers of gas-filled drift tubes, of which eight layers measure the ϕ -coordinate and four perpendicular oriented layers measure the z -coordinate. The transverse size of a drift tube is $42 \times 13 \text{ mm}^2$; the spatial resolution has been measured to be about $80 \mu\text{m}$ to $120 \mu\text{m}$ [27]. In the endcaps, where the particle flux is larger, four layers of cathode strip chambers (CSCs) are used instead. They offer a higher granularity and a faster signal response due to a shorter drift path. Cathode strip chambers consist of six anode wires and seven perpendicularly oriented copper cathode strips. The muon system is supplemented by resistive plate chambers (RPCs) in the barrel and the endcaps. RPCs are made of two plastic plates that are separated by a

gas-filled gap of 2 mm thickness. Readout strips mounted on the backside of one of the plastic plates are used for signal readout. RPCs offer a good time resolution of about 1 ns but have a spatial resolution of about 1 cm only. They are mainly used for the trigger system.

1.2.4. Trigger System

At 40 million proton bunch crossings taking place every second in the LHC the amount of data collected by the CMS detector is too large to store all events. Most of the scattering processes are elastic or quasi-elastic and therefore uninteresting for most physics analyses. The rate of stored events is reduced by about five orders of magnitude with the trigger system [28], which selects only potentially interesting events.

CMS employs a two-stage trigger system. The first level (L1) reduces the event rate from 40 MHz to about 100 kHz. Coarse data from the muon system and the calorimeters are used to decide whether the entire detector should be read out or whether the event is discarded. The trigger algorithms are implemented on FPGAs and ASICs to provide a fast decision within a latency of 4 μ s. During this time the full event data has to be buffered in the detector front-end electronics. Only if the L1 trigger has accepted the event will all subdetectors send their data to the CMS data acquisition (DAQ) system.

The second trigger stage, the so-called high level trigger (HLT), is software-based and runs on a server farm. It uses additional information from the tracking system and employs more complex reconstruction algorithms. The HLT reduces the event rate to a few hundred Hertz. Events that are accepted by the HLT are stored for offline analysis.

1.2.5. Upgrades of the CMS Detector

Due to constant improvements of the LHC and its pre-accelerators, the design instantaneous luminosity was reached in 2016 for the first time. It was envisaged that during Phase-1 of the LHC upgrade the instantaneous luminosity would be further increased and eventually reach twice the nominal value, i.e., $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. This value was reached already in 2017.

At a bunch-spacing of 25 ns this instantaneous luminosity leads to on average about 50 simultaneous proton-proton interactions in the CMS detector. The current plan foresees to operate the LHC in this configuration until Long Shutdown 2 in 2024, resulting in at least 300 fb^{-1} delivered to the CMS experiment. The LHC will be upgraded to the HL-LHC during LS3, and the instantaneous luminosity will be increased to at least $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$.

The larger particle flux and ongoing radiation damage pose new challenges for the operation of the CMS detector. To fully benefit from the increased luminosity, upgrades of several subsystems are necessary. A higher detector granularity is required to cope

with the increased pileup and to keep the occupancy low to avoid, for example, mismatching of hits to fake tracks. Faster readout electronics are required to account for larger hit rates, and the back-end electronics have to be upgraded to be compatible with increased bandwidth demands. Furthermore, the trigger system has to be modified to keep event rates at acceptable levels. Finally, subsystems that would suffer from severe radiation damage have to be replaced with more radiation tolerant ones. CMS foresees two major detector upgrades, which are referred to as Phase-1 and Phase-2 upgrades.

Phase-1 Upgrade

The CMS Phase-1 upgrade [29] started during LS1 (2013-2015). In the muon system, additional RPC and CSC stations were installed to provide additional input for the trigger. The trigger system itself was rebuilt [30] with hardware based on the MicroTCA system, which allows to increase the bandwidth and to employ more sophisticated trigger algorithms. Finally, the bandwidth of the DAQ system was increased to handle the larger data volume caused by the increased particle flux at larger luminosities and the increased number of readout channels. A new beampipe with a diameter reduced from 58 mm to 45 mm was installed to allow a reduction of the diameter of the innermost pixel layer.

The hadron calorimeter was also upgraded [31]. New multi-anode phototubes with thinner optical windows replaced the existing photomultiplier tubes of the forward calorimeter to reduce the rate of anomalous signals, which are created by Cherenkov light inside the tubes. In the HO calorimeter, the hybrid photodetectors were replaced by silicon photomultipliers (SiPMs), which offer a better photon detection efficiency and a higher gain. In a year-end technical stop in 2017/2018, SiPMs were also installed in the endcaps. During LS2 (2019-2020), SiPMs will be installed in the barrel of the hadronic calorimeter. The implementation of SiPMs allows to increase the longitudinal readout segmentation of the calorimeter towers. As a benefit further information about the hadronic shower shape can be obtained, and the signal-to-noise ratio is increased.

The most significant change within the scope of the Phase-1 upgrade is the installation of a new pixel detector during the extended year-end technical stop (YETS) in 2016/2017. The short timescale for the installation and the desire to minimize the impact on subsequent data taking were main design drivers for the new pixel detector. It was installed before LS2, because already during the 2016 data taking period the instantaneous luminosity exceeded the nominal value. Furthermore, the pixel system is designed to be extracted rather easily for refurbishment during longer technical stops. Through the replacement during a YETS, it was possible to benefit from the new system as early as possible.

The operation of the original pixel detector at Phase-1 luminosities would have lead to unacceptable inefficiencies, arising from overflowing buffers in the readout chips. The Phase-0 pixel detector was designed for an instantaneous luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$

and a bunch spacing of 25 ns. At the design value, the hit efficiency for all layers was better than 99 %, except for the innermost barrel layer, where the hit efficiency was about 98 % [23]. Simulations showed that inefficiencies in the innermost layer would have reached up to 16 % at Phase-1 luminosities. Also, the larger pileup would have either resulted in an increased rate of fake tracks (due to matching ambiguities), or a reduced tracking efficiency (if stricter track requirements were applied). Finally, the hit resolution would have deteriorated by a factor of two [32]. The reason is that radiation damage in the silicon sensors reduces the charge collection efficiency, leading to a lower signal height. As a result, fewer signals are above the detection threshold of the readout chip, which would, in turn, reduce the effect of charge sharing between adjacent pixels.

The Phase-1 pixel detector has been developed to maintain and even improve the tracking performance during the next few years. It features an additional layer of pixel modules in the barrel and the endcaps, and the radius of the innermost barrel layer has been reduced to 2.9 cm. New readout chips with increased buffer sizes and a digital data format have been developed to decrease inefficiencies arising at high instantaneous luminosities. Despite the larger number of active channels, the material budget could be significantly reduced. The new detector is built with an ultra-light carbon fiber support structure, services have been shifted out of the tracking volume, and an evaporative CO₂ cooling system replaced the mono-phase liquid cooling system. Furthermore, a new powering scheme involving DC-DC converters has been developed. It fulfills the increased power requirements of the upgraded detector with existing power supplies and the existing cable plant.

It is foreseen to replace the innermost layer of the new barrel pixel detector during LS2 in 2019 to mitigate the performance deterioration induced by radiation damage.

Phase-2 Upgrade

The changes introduced with the Phase-1 upgrade are not sufficient to cope with the increased instantaneous luminosity that the HL-LHC will deliver. Furthermore, the strip tracker will have reached the end of its lifetime by the time of LS3 and has to be replaced. Both the pixel detector and the strip tracker will be exchanged within the scope of the Phase-2 upgrade [33]. Both subdetectors will have a higher granularity to cope with the further increased pileup. A new design concept will allow the Phase-2 strip tracker to contribute to the L1 trigger decision. Modules are equipped with two silicon strip sensors (so-called 2S-modules) or a strip and a macro-pixel sensor (so-called PS-modules). The 2S-sensors, for example, will have a spacing of 1.6 mm to 4.0 mm, depending on the distance of the module from the interaction point. The readout chips will be able to compare the offset between hits in both sensors. Because the bending radius of charged particles in the magnetic field of CMS depends on their momentum, the offset can be used to discriminate between tracks with low transverse momentum and large transverse momentum. This discrimination will be done on the modules directly and will serve as an input to the trigger decision. Like in the Phase-1 pixel

detector a powering scheme involving DC-DC converters will be used for the Phase-2 strip tracker. For the Phase-2 pixel detector, a serial powering scheme will be used to minimize the material of the power cables inside the detector while keeping the voltage drops at acceptable levels.

Both endcap calorimeters (electromagnetic and hadronic) will have reached the end of their expected lifetime by the start of LS3. They will be replaced by a high granularity calorimeter (HGCAL). The electromagnetic part will use steel-clad lead as absorbers and silicon sensors for the detection of shower particles. The fine segmentation in all three dimensions enables precise measurements of the shower shape, which can be used to resolve individual particles for an improved pileup rejection. The hadronic part will use a combination of silicon sensors and scintillator tiles with mounted SiPMs. In the barrel ECAL, the existing crystals and APDs will be kept, but the readout electronics will be replaced entirely. The Phase-1 upgrades of the barrel HCAL front-end electronics are sufficient for operation under HL-LHC conditions. The scintillators, fibers, and SiPMs will be kept. However, the back-end electronics have to be replaced to cope with increased trigger rates.

The readout electronics of the DTs and CSCs in the muon system will be exchanged in order to handle a higher L1 trigger rate of 750 kHz and an increased trigger latency of 12.5 μ s. In the endcaps, a new layer of Gas Electron Multipliers (GEMs), which covers a pseudorapidity of $1.6 < |\eta| < 2.2$, will be installed during LS2. Further information about the Phase-2 upgrades of the muon system can be found in references [34, 35].

2. The CMS Phase-1 Pixel Detector

In the following chapter, the design of the CMS Phase-1 pixel detector is described in detail. First, a short overview of the detector design is given. Then the concept of the pixel modules and the detector readout architecture is described. A particular focus lies on the working principle of the readout chip because it has significantly determined the structure of the test sequences, with which pixel modules were tested during series production (Chapter 3). Furthermore, the design of the power system is described and motivated. The DC-DC converters are described in detail because they were used in system tests (Chapter 4).

2.1. Overview

The CMS pixel detector consists of a barrel part (BPix) and a forward detector (FPix), which extends the geometrical coverage up to $|\eta| < 2.5$. On both sides of the pixel detector, there are service structures on which components necessary for the operation of the pixel modules are located. Figure 2.1 shows an exploded view of the Phase-1 pixel detector.

The mechanical support structure of the pixel detector is designed in a manner that the detector can be relatively easily installed into and extracted from the CMS experiment. This allows servicing the detector during longer maintenance periods. The FPix and the BPix detectors are split in the vertical direction. They are built from half-cylinders, which are pushed together around the beam pipe during the installation in CMS. The services and auxiliary electronics are integrated on both ends of the pixel detector, inside CMS, on so-called supply tubes (BPix detector) and in service cylinders (FPix detector). Like the detector itself, the supply tubes and service cylinders are made of two half-cylinders that wrap around the beam pipe. The BPix supply tubes have a larger radius and enclose the FPix service cylinders.

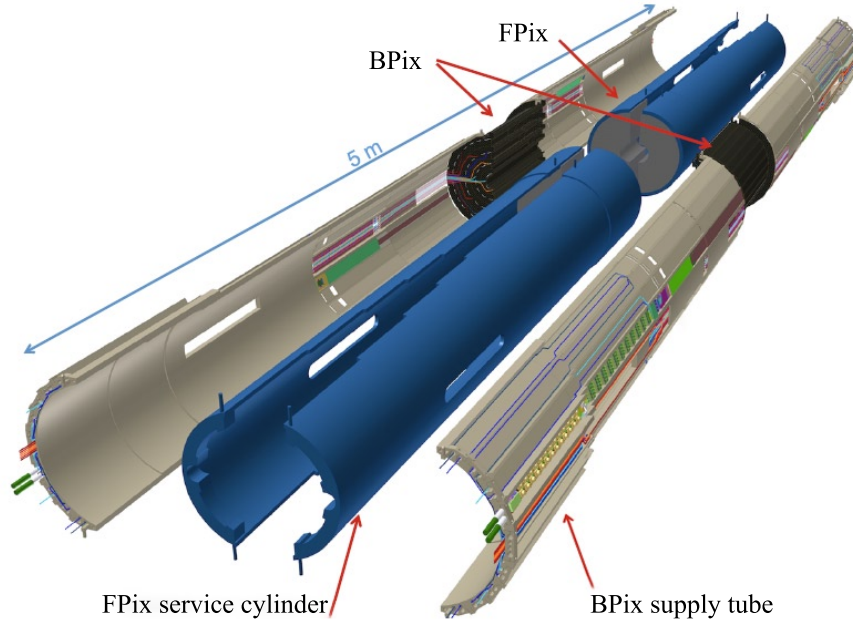


Figure 2.1.: Exploded view of the Phase-1 pixel detector. Electronics that are required to operate the pixel modules are mounted on the BPix supply tubes and in the FPix service cylinders. The FPix detector is located within the service cylinders. Modified from [32].

2.2. Pixel Module

The basic concept of the pixel modules was not changed for the Phase-1 upgrade, to introduce as little changes as possible. It is a hybrid pixel module with a highly segmented silicon sensor connected to readout chips. The sensor design remained the same, while new readout chips were developed to increase the hit detection efficiency at larger instantaneous luminosities. Barrel modules of layer 2-4 and forward pixel modules are read out with the PSI46dig ROC [36], which is an upgraded version of the original psi46V2 ROC [37]. For the innermost layer of BPix (layer 1), where the particle flux is largest, a new ROC with a different readout architecture was developed. This ROC is called PROC600 [38].

In the Phase-1 detector, the number of different module types was reduced to simplify the production as well as the maintenance procedures. In the Phase-0 detector, five different types of modules with two to ten readout chips were used in FPix and modules with eight or 16 readout chips were used in BPix. In contrast, there are only four types of modules in the upgraded detector, all of them comprising 16 readout chips. In FPix all modules are the same. In BPix there are three separate types, one for layer 1, one for layer 2 and one for layers 3 and 4.

2.2.1. Design

Schematic views of the pixel modules for barrel layers 2-4, barrel layer 1, and FPix are shown in Figure 2.2. Photons or charged particles traversing the detector create a signal in the silicon sensor. Readout chips collect the electrons and generate a hit information. A readout chip has 4160 pixels with a size corresponding to the sensor pixel size. In a flip chip process 16 ROCs (2×8) are connected to the sensor via approximately $40\text{ }\mu\text{m}$ large solder bumps.

A separate control chip, the Token Bit Manager (TBM) [39], is used to distribute the clock and the L1 trigger signals to the readout chips and to establish the communication with off-detector electronics. Three different types of TBMs have been developed for the Phase-1 detector. Pixel modules in BPix layers 3 and 4 and FPix use a single TBM, which is connected to the readout electronics by one data link (TBM08). In layer 2 of the barrel, a TBM with two data links (TBM09) is used to cope with the higher occupancy. In the first layer of the barrel, where the hit rate is about five times larger compared to layer 2, the pixel modules are equipped with two TBMs (TBM10), which also have two data links each.

The High Density Interconnect (HDI) distributes signals and supply voltages across the module. It is a thin and low-mass PCB, which is glued to the backside of the sensor. Wire bonds, which wrap around the sensor, connect bond pads of the ROCs to the HDI. The TBMs are glued to the HDI and are also connected with wire bonds. Two types of HDIs are used in BPix, which accommodate either one or two TBMs. The HDI design in FPix is similar to the BPix layers 2-4 design, but the PCB was produced by a different company.

In the barrel detector, the pixel modules are connected to the supply tube electronics with an approximately 1 m long twisted pair cable. The cable comprises six pairs of $125\text{ }\mu\text{m}$ thick wires for data transmission (nine pairs for layer 1) and eight individual wires of $360\text{ }\mu\text{m}$ diameter for powering [32]. Copper-clad aluminum wires are used for powering, to reduce the mass of the cable. In FPix, 75 cm long flexible flat cables connect the pixel modules to the electronics in the service cylinder.

Cables from BPix modules are routed outwards along the z -direction on top of other pixel modules. A thin cover made from Kapton is glued to resistances on top of the HDI to prevent damage to wire bonds of modules lying below the rather stiff cables.

The mounting of the modules in the detector is realized in three ways. In the barrel detector, $250\text{ }\mu\text{m}$ thick parts (so-called base strips) of silicon nitride (Si_3N_4) are glued to the back of the readout chips along the long edge of the module. The module is fixed on the support structure with six screws. The small radius of the innermost barrel layer prevents the use of base strips. Instead, the modules are clamped to the support structure with a small piece of carbon fiber along the short edge. In the FPix detector, a pair of module holders is glued to the HDI on each side. The modules are screwed onto the support structure.

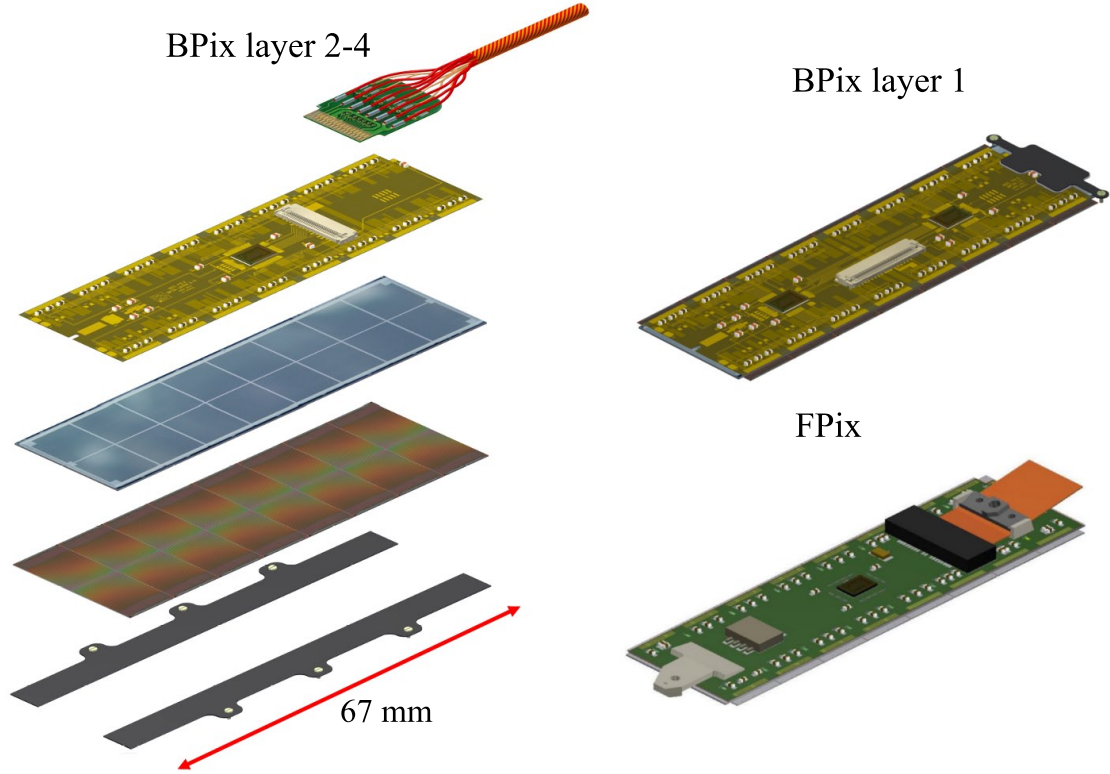


Figure 2.2.: Schematic view of the Phase-1 pixel modules [32]. Left: exploded view of a layer 2-4 module. The components shown are (from top to bottom) the cable, the High Density Interconnect with Token Bit Manager, the sensor, readout chips and base strips. Right: Module for BPix layer 1 with two TBMs (top) and FPix module (bottom).

2.2.2. Sensor

The sensor has an active area of $16.2 \times 64.8 \text{ mm}^2$ and features 66 560 pixels. It is made from an n-type silicon substrate with a thickness of $285 \mu\text{m}$ and highly doped n^+ pixel implants. The pixel size is $100 \mu\text{m}$ in $r\phi$ -direction and $150 \mu\text{m}$ in z -direction. Minimum ionizing particles create about 20 000 to 40 000 electron-hole-pairs in the sensor, depending on the incident angle.

Before irradiation, full depletion of the sensor is achieved with a bias voltage of about 100 V. With ongoing radiation damage the bias voltage has to be increased; up to 600 V are foreseen in the pixel system. A benefit of the n^+ -in-n design is that depletion always starts from the implants, allowing a charge collection even if the sensor is not fully depleted. At the end of the detector lifetime, some sensors will be operated in this mode.

2.2.3. Readout Chips

The psi46dig readout chip is manufactured in a 250 nm CMOS process. It has a size of $10.3 \times 7.9 \text{ mm}^2$ and features 4160 pixels, which are organized in 80 rows and 52 columns. Several parameters, such as timings, gain, and voltages, are adjusted with 16 programmable digital-to-analog converters (DACs). The chip has an analog domain for signal processing and a digital domain for creating hit information and for communication with other electronics. The layout of the readout chip can be divided into three functional blocks: pixel unit cells, double column periphery, and a controller & interface block. Below the design of the readout architecture of the psi46digV2 ROC is described. The differences to the psi46V2 readout chip are mentioned at the appropriate places. Further information about the ROCs can be found in references [36, 37, 40–44].

Pixel Unit Cell

A block diagram of a pixel unit cell (PUC) is shown in Figure 2.3. Each pixel of the silicon sensor is connected to the bump pad of a PUC. Signals can either be created by a charge deposition in the sensor, or by injecting calibration pulses through a 4.8 fF capacitor on the ROC. The test pulse can either be injected into the amplifier directly or into a metal pad, which is capacitively coupled to the sensor. A switch, which is controlled by the CalS register, selects the injection mechanism. The height of test pulses is adjusted by the 8-bit Vcal DAC. An additional control register (named CtrlReg) is used to increase the test range. If the register is enabled, the charge corresponding to a specific Vcal value is multiplied by a factor of 7. The CalDel DAC delays the calibration pulse by a programmable amount of time. Calibration pulses are

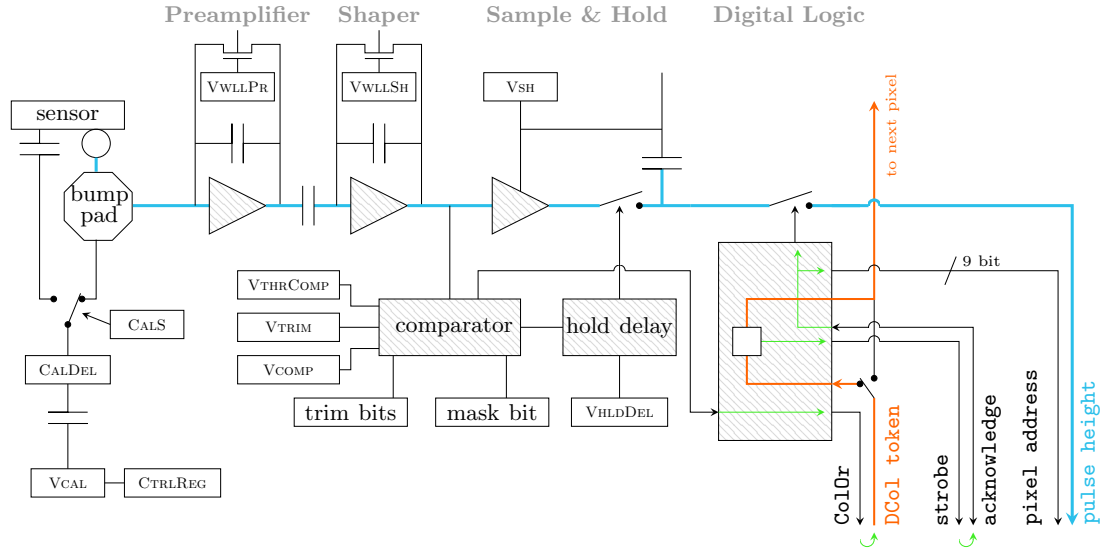


Figure 2.3.: Simplified schematic of the pixel unit cell. Some of the DACs and registers that can be programmed are indicated [43].

a viable tool to test the functionality of the pixel cell and the bump bond connection and to optimize the DAC parameters of a readout chip.

Signals are amplified and shaped in the PUC before they are passed to a comparator, which rejects pulses below a programmable threshold. The threshold is adjusted with several DACs. A global threshold, which is common to all pixels, is set with the $V_{thrComp}$ DAC. Each pixel unit cell also has four individual trim bits, which reduce the global threshold by a programmable amount. The trim bits allow compensating for inhomogeneous thresholds across the ROC. A mask bit can be used in order to switch off the comparator output to disable noisy pixels, which could potentially disturb the readout. If a signal passes the threshold, the pulse height is sampled after a programmable time delay, and the signal height is stored in the sample and hold circuit. In this case, the PUC requests a readout from the double column periphery by sending a signal on the $CoLoR$ line. The PUC becomes insensitive until the readout is finished.

The principle design of the analog chip domain of the $\psi46digV2$ remained almost unchanged compared to the $\psi46V2$ ROC. However, the crosstalk between pixels could be significantly lowered, allowing the operation with a threshold of about 1500 electrons instead of 3500 electrons. Lower thresholds usually increase the hit detection efficiency and the single hit resolution. Lower thresholds also increase the detector longevity as the sensor's reduced charge collection efficiency after irradiation can be compensated.

Double Column Periphery

The readout of pixel unit cells is realized in a so-called column drain mechanism. The psi46dig ROC has 26 double columns (DCs) that work independently from each other. Every double column consists of 2×80 daisy-chained pixels and a periphery with 24 timestamp buffer cells and 80 hit buffer cells. Once the double column periphery is notified about a hit in a PUC, a timestamp in the form of an 8-bit counter value is stored in the timestamp buffer, to associate the hit to a certain bunch crossing. The periphery sends out a readout token (DCol token), which is passed from one PUC to another. Pixels without a hit directly pass the token to the next pixel; pixels with a hit transfer their address and the analog pulse height to the data buffer and then pass the token. A second counter, which is delayed by the L1 trigger latency, is compared to the oldest timestamp in the buffer. If they match and a trigger signal is present, the double column stops data taking and goes into readout mode. Otherwise, the timestamp and data buffers associated to that event are cleared.

ROC Controller & Interface Block

All double columns transfer their hits independently from each other to their buffers. The readout of the double column buffers is controlled by the ROC controller & interface block (RCI). The readout scheme is depicted in Figure 2.4. Two readout tokens are required. As soon as the ROC receives an L1 trigger, it sends out a ROC-internal readout token to the first double column. The token is passed one after the other to all double columns, which transfer all their data to the global readout buffer. Once the ROC receives an external readout token (which is sent by the Token Bit Manager), it sends out all data from the readout buffer.

The RCI integrates circuits that are shared between all double columns. The data serializer merges pixel address and pulse height information. In the Phase-0 detector, the analog pulse height was transmitted to the detector back-end electronics. The main design change of the new psi46digV2 readout chip is a transition from a 40 MHz analog data encoding with 6 discrete levels to a 160 Mbit/s digital data encoding. The psi46V2 ROC is therefore referred to as the analog ROC, while the psi46digV2 is referred to as the digital ROC. Due to the new digital readout format, it is necessary to digitize the pulse height of the analog signal on the chip. This is realized by an 8-bit successive approximation analog-to-digital converter (ADC).

The RCI also features a phase-locked loop (PLL) block, which generates 160 MHz and 80 MHz clocks from the 40 MHz LHC clock. The DACs and registers of the ROC can be programmed via a modified I²C protocol.

The readout chip requires two supply voltages, one for the analog domain (> 1.6 V) and one for the digital domain (> 2.4 V). The ROC has low-dropout (LDO) voltage regulators, which provide stable voltages to the circuitry as long as the input voltage

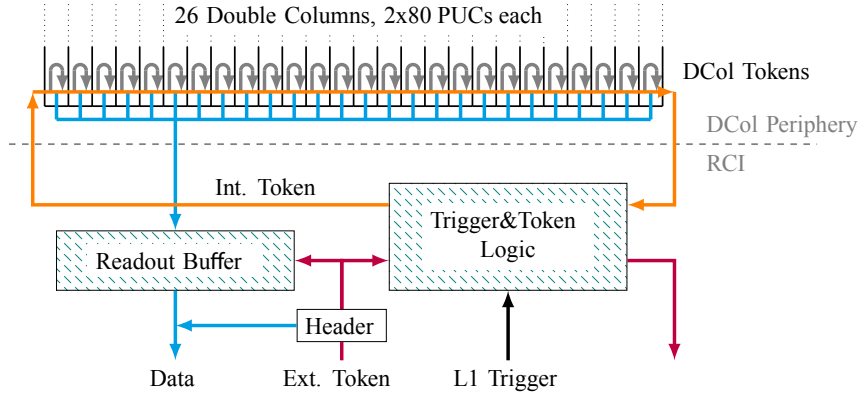


Figure 2.4.: Readout scheme of the PSI46dig chip, modified from [45]. Pixel hits are transferred to buffers in 26 independent double columns. When the readout chip receives the L1 trigger signal, an internal token is sent to the double columns. Hits are then sent to the new readout buffer stage. Upon arrival of the TBM readout token, all hit information is sent to the TBM.

is above the minimum allowed value. The current in the analog part of the ROC can be adjusted by programming the so-called Vana DAC. The current is typically set to 24 mA. The value of the regulated digital voltage can be set with the Vdig DAC. The digital current I_{dig} depends on the activity in the readout chip [43]:

$$I_{\text{dig}} = (27.0 \pm 0.4) \text{ mA} + (0.121 \pm 0.004) \frac{\text{mA cm}^2}{\text{MHz}} \times R_{\text{H}} \quad . \quad (2.1)$$

R_{H} denotes the rate of pixel hits.

The psi46digV2 ROC has a low power startup mode implemented. When input voltages are supplied to the ROC, but the DACs have not yet been programmed, the analog and digital input currents are about 5 mA and 25 mA, respectively.

Dynamic Data Losses

Several data loss mechanisms can lead to inefficiencies at large instantaneous luminosities. The inefficiencies are dynamic, meaning that they depend on the particle fluence. For example, a pixel unit cell is insensitive to new hits if the previous hit has not yet been read out. The entire double column is insensitive while it is in the readout mode, to prevent overwriting of valid data. Severe data losses also occur if one of the buffers is filled. Hits are buffered in the readout chip for the time corresponding to the trigger latency (4 ps) because only events that have a valid L1 trigger are read out and sent to the DAQ system. When the timestamp buffer is filled, no further readout tokens are

sent to the pixels, and no new events can be recorded. When the data buffer overflows, the whole double column needs to be reset and all events in a time window corresponding to the trigger latency are lost. The timestamp buffer cells of the psi46digV2 ROC have been doubled with respect to the psi46V2 ROC from 12 to 24, and the data buffer cells have been increased from 32 to 80 to overcome these issues.

The global readout buffer and the ROC-internal readout token are new features of the psi46digV2 chip. They reduce dead times caused by double columns waiting to be read out. A double column becomes insensitive after receiving a trigger signal. In the psi46digV2 ROC, a DC can resume data taking as soon as the hit information has been transferred to the global buffer. The psi46V2 chip does not have an internal readout token. Therefore, a DC must wait until the external readout token of the TBM arrives at the ROC. After the data has been sent out, the double column is reset. Only then it can take new data. As a result, all possible hits within the trigger latency are lost.

The transition from an analog coding scheme with 6 levels at 40 MHz to the 160 Mbit/s digital readout has effectively doubled the bandwidth. With these changes, the psi46dig chip can operate at a hit rate of 120 MHz/cm² with an efficiency above 99 %. This hit rate is expected in layer 2 of the barrel pixel detector at the design instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$.

The changes are however not sufficient to cope with the hit rate of about 600 MHz/cm² that is expected for layer 1 of the detector. The PROC600 was developed, which has a different readout architecture. It features the same 80×52 pixel matrix as the psi46digV2 and is also fabricated in a 250 nm CMOS process. This chip employs a new Dynamic Cluster Column Drain architecture, which reads out clusters of 2×2 pixels instead of single pixels. The double columns are continuously read out. The buffers were redesigned so that a reset after a readout is no longer required. In a test beam the efficiency at 580 MHz/cm² was measured to be about 98 % [38].

2.2.4. Token Bit Manager

The Token Bit Manager controls the readout of several ROCs on a pixel module. This is illustrated in Figure 2.5. Several ROCs are combined in a so-called token chain. Once the TBM receives a trigger signal, it sends a readout token to the first ROC in the chain. The ROC then sends out its data with a rate of 160 Mbit/s. Afterward, it passes the token to the next chip in the chain. After all ROCs have been read out, the token is returned to the TBM. The TBM multiplexes the ROC data from two readout chains into a single 400 Mbit/s data stream with a 4b/5b encoding. Furthermore, it adds header and trailer information, which is used by the off-detector electronics to assign the hit information to the correct bunch crossing. The TBM08 controls two token chains consisting of eight ROCs each. The TBM09 has four token chains with four ROCs each and requires two data links. The TBM10 (used in BPix layer 1) also has two readout links and four token chains, but only two ROCs are in a token chain.

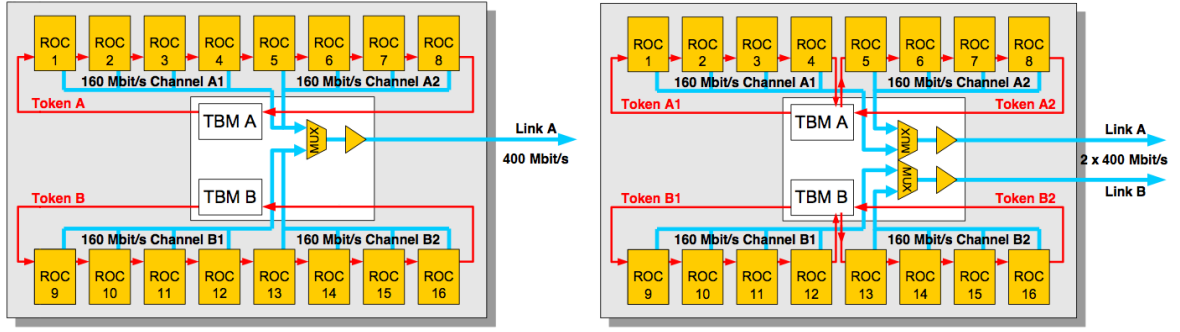


Figure 2.5.: Readout scheme of the Phase-1 pixel modules. The TBM08 (left) has two token chains and one readout link. The TBM09 (right) has four token chains and two readout links [41].

2.3. Detector Control and Readout

2.3.1. Data Acquisition

The communication of pixel modules (also called detector front-end) with the detector readout electronics (also called detector back-end) is realized via optical links. Figure 2.6 shows a schematic view of the data acquisition (DAQ) system of the Phase-1 pixel detector. The TBM data stream, which is encoded at 400 Mbit/s, is output as a low current differential signal (LCDS). A Pixel Opto Hybrid (POH) converts the electrical signals into optical signals. The POH comprises four (BPix) or seven (FPix) Fabry-Perot lasers operating at a wavelength of 1310 nm, laser drivers, and digital level translators [32, 46]. A total of 14 POHs are mounted on a so-called POH motherboard, of which 32 are used in BPix. In FPix, they are mounted on so-called port cards. The signals are transmitted to the back-end via optical fibers with a length of about 65 m. The detector back-end is located outside of the CMS experimental cavern, in the so-called service cavern.

The signals are received by Front-End Drivers (FEDs). A FED decodes the data streams from several pixel modules, buffers the hit information, and sends partial event information with a rate of 10 Gbit/s to the central CMS DAQ system. The LHC clock and the L1 trigger signal are distributed between several FEDs by a so-called AMC13. A completely new detector back-end based on the μ TCA standard [47] was developed to replace the old VME-based system of the Phase-0 detector. FEDs for the Phase-1 detector consist of an FC7 FPGA board [48] and a mezzanine card with inputs for 24 fibers.

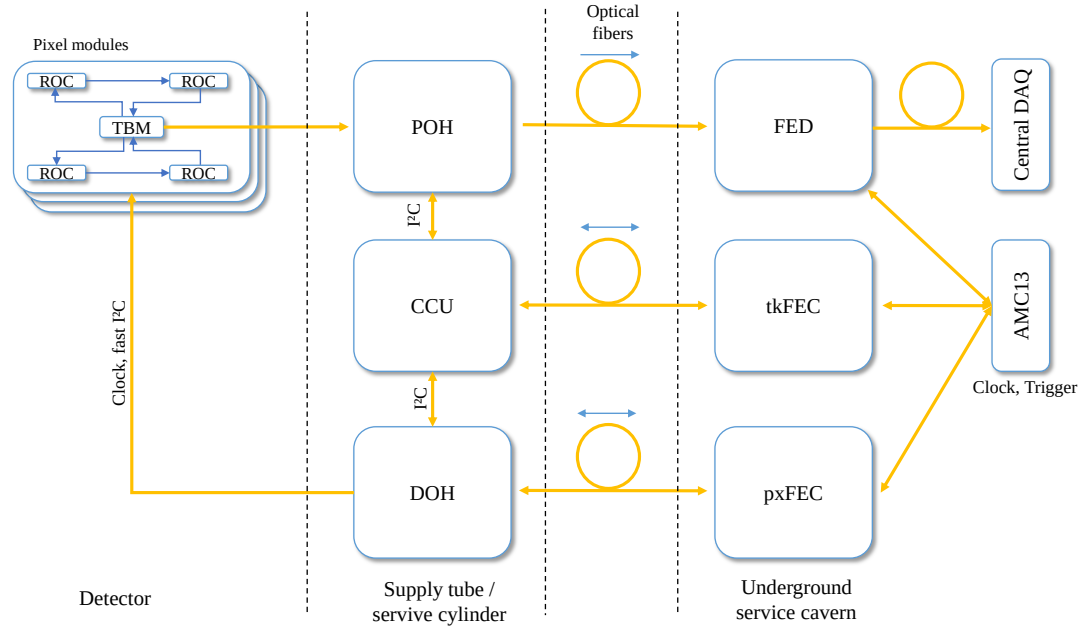


Figure 2.6.: Overview of the data acquisition system of the Phase-1 pixel detector.

2.3.2. Detector Control

The pixel detector is controlled with Front-End Controllers (FECs). FECs are also based on the FC7 FPGA board but use different mezzanine cards and firmware. Two types of FECs are used in the Phase-1 pixel detector. The so-called fast control system is driven by so-called Pixel FECs, while the slow control system is driven by so-called Tracker FECs.

The Pixel FEC sends the LHC clock signal (named CLK) and Calibrate/Trigger/Reset signals (named CTR), as well as commands for programming (named SDA), to the pixel modules. CTR signals are encoded in the clock signal, to reduce the number of fibers required to transmit the data. Various components located on service structures near the pixel detector convert the optical signals into electrical signals and process them further. The optical signals are converted to electrical low voltage differential signals (LVDS) by so-called digital opto-hybrids (DOH). CTR and CLK signals are separated on-detector by TPLL (Tracker Phase Locked Loop) and QPLL (Quartz Phase Locked Loop) chips. The relative phases of the clock and control signals are adjusted by a DELAY25 chip. The signals are converted to LCDS signals by a GateKeeper chip and LCDS driver chips and are sent to the pixel modules. So-called DOH motherboards house DOHs, PLLs, DELAY25 and GateKeeper chips in the barrel pixel detector. The DOH motherboards are plugged into the POH motherboards. In the FPix detector, all components are integrated in the port cards.

The Control and Communication Unit (CCU) is the core part of the slow control system. It programs the DOHs, PLLs, and DELAY25 chips via an I²C protocol. In the BPix detector, nine CCU25 [49] chips are integrated in a ring architecture on a so-called CCU board. Eight CCUs control a part of the pixel detector, while the last CCU is used for redundancy. The CCU ring board is connected to the Tracker FEC with optical fibers via two DOHs. Four CCU ring boards are used in total. In FPix, five CCU25 chips are mounted together with two DOHs on a CCU board.

2.4. Power System

The power consumption of the Phase-1 pixel detector is about twice as high as that of the Phase-0 pixel detector. The reason is that the number of readout channels in the Phase-1 pixel detector has increased by a factor of 1.9, while at the same time the currents drawn by a single pixel module are almost unchanged. Since the supply voltages of the pixel modules remained the same, the supply currents have approximately doubled.

The Phase-0 pixel detector used a direct powering scheme, in which several pixel modules were connected in parallel to power supplies. In the Phase-1 detector, this powering scheme would have led to a factor of about 4 increased power losses on the supply cables, because the power loss scales quadratically with the current ($P_{\text{loss}} \propto I^2$).

The output power of the power supplies would not have been sufficient to cover the increased power consumption of the pixel modules and the power losses on the cables. If only the power supplies had been replaced while the powering scheme would have stayed the same, this would have led to overheating of the cables. Due to space constraints in the cable channels and the patch panels inside CMS, the installation of additional or thicker cables was not considered feasible, especially in the short time frame of an extended technical stop.

The most cost-effective and time-saving solution was to supply a larger voltage on the existing cables and to step down to the required voltages in the detector, using radiation tolerant DC-DC converters. By increasing the supply voltage by a factor of r and by using a down-conversion with an efficiency of ϵ , voltage drops along the cables can be reduced by a factor of $r \cdot \epsilon$ and power losses can be reduced by $(r \cdot \epsilon)^2$. For the power system of the Phase-1 pixel detector design values of 10 V for the converter input voltage and 2.4 V, 3.3 V, and 3.5 V for the output voltages were chosen. Therefore, the conversion ratios range from 2.9 to 4.2. With a typical conversion efficiency between 80 % and 85 % this leads to a reduction of the power losses by factors 6 to 11. Not only the existing cable plant was kept, but also the power supplies could be reused after a modification.

2.4.1. Buck Converters

Buck converters are used in the Phase-1 pixel detector. This type of DC-DC converters reduces the output voltage by periodically connecting and disconnecting the load and the power supply. An inductor is used to store energy in a magnetic field to preserve a constant current flow, and capacitors are used to reduce voltage ripple at the input and output. The basic principle is shown in Figure 2.7. The transistors T_1 and T_2 are switched with a fixed frequency f_s . In the on-state, T_1 is conducting and T_2 is open, allowing a current flow from the power supply to the load (Figure 2.7 (top)). In this state the inductor builds up a magnetic field, resulting in a voltage drop across the coil and a reduced voltage at the load. In the next step, both transistors are switched, such that in the off-state (Figure 2.7 (bottom)) T_1 is open and T_2 is closed. In this state, the inductor is discharged to maintain the current through the load.

The conversion ratio r of a lossless DC-DC converter corresponds to the inverse of the duty cycle D , which is defined as the fraction of the time the device resides in the on-state (t_{on}):

$$T = \frac{1}{f_s} = t_{\text{on}} + t_{\text{off}} \quad , \quad (2.2)$$

$$D = \frac{t_{\text{on}}}{T} \quad , \quad (2.3)$$

$$r = \frac{V_{\text{in}}}{V_{\text{out}}} = \frac{1}{D} = \frac{1}{t_{\text{on}} \cdot f_s} \quad . \quad (2.4)$$

A control circuit is required to drive the transistors and to regulate the output voltage. Pulse width modulation is a commonly used control technique. A feedback loop adjusts the duty cycle to keep the output voltage at the set value, independently of the input voltage.

The switching frequency of buck converters can range from a few kHz to several MHz. Large frequencies lead to a lower output ripple and allow the use of smaller coils and capacitors. On the other hand, lower switching frequencies reduce losses in the transistors and increase the overall efficiency of the DC-DC converter. A compromise has to be found in this respect.

The efficiency ϵ is defined as

$$\epsilon = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{\text{out}} \cdot I_{\text{out}}}{V_{\text{in}} \cdot I_{\text{in}}} \quad , \quad (2.5)$$

where V_{out} is the output voltage of the DC-DC converter, I_{out} is the output current, V_{in} is the supply voltage, and I_{in} is the input current drawn by the DC-DC converter.

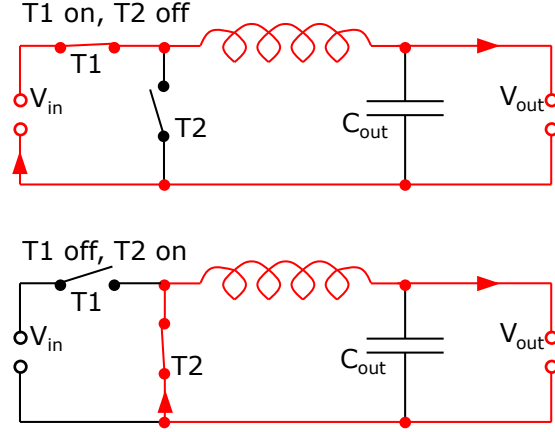


Figure 2.7.: Working principle of a buck converter [50]. The red color indicates the current path. In the enabled state (top), the load is connected to the input (T_1 closed, T_2 open). In the disabled state (bottom), the inductor is discharged to maintain the current through the load (T_1 open, T_2 closed). A control circuit (not shown) drives the switches.

When the efficiency is known, the input current of a DC-DC converter can be calculated:

$$I_{in} = I_{out} \cdot \frac{V_{out}}{V_{in}} \cdot \frac{1}{\epsilon} \quad . \quad (2.6)$$

A DC-DC converter has a negative input resistance because larger supply voltages result in lower input currents.

The operation within CMS places special demands on the DC-DC converters. Main requirements are:

- Robustness against single event upsets (SEUs).
- Tolerating a total ionizing dose of at least 10 Mrad and an integrated fluence¹ of $2 \times 10^{14} \text{ n}_{eq}/\text{cm}^2$ [32].
- Operation in the magnetic field of 3.8 T.
- Low mass and a small volume.
- Well shielded to keep electromagnetic emissions as low as reasonably possible.

¹The radiation damage caused in silicon depends on the type of particle and its energy. The equivalent fluence of neutrons with a kinetic energy of 1 MeV is used as a reference.

Devices that fulfill these requirements are not commercially available and hence had to be developed for the Phase-1 pixel detector. A buck converter design was chosen because typical output currents are in the order of 1 A to 2 A.

2.4.2. PixV13 DC-DC Converter

A magnetic field and radiation tolerant buck converter, the so-called PixV13, has been developed by the I. Institute of Physics (IB) at the RWTH Aachen University. The DC-DC converter consists of a PCB that is optimized for the use on the pixel supply tube and carries a FEAST2 ASIC [51], which has been designed by the CERN Group for Electronics Systems for Experiments (PH-ESE).

FEAST2 ASIC

FEAST2 features the two power transistors, a control circuit, and linear regulators, which provide power for the control circuit. It is produced in the $0.35\,\mu\text{m}$ I3T80 process [52] by ON Semiconductor, which has proven to be radiation tolerant while still allowing high input voltages of up to 14 V. The chip can sustain a total ionizing dose of at least 500 MRad and an integrated fluence of about $5 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$ [53]. This is about 2.5 times larger than what is required for the operation in the Phase-1 pixel detector. The ASIC is rated for input voltages of 5 V to 12 V and continuous output currents of up to 4 A or an output power of 10 W, whatever is lower. The output voltage is selectable between 0.9 V and 5 V. A schematic diagram of the FEAST2 ASIC can be found in Figure A.3 in the Appendix.

The output voltage of the converter can be disabled during detector operation by applying a voltage on a specific pin. The ASIC outputs a fixed voltage status signal (so-called PowerGood) when it is switched on and its output voltage is within $\pm 6.5\%$ of the nominal value. To prevent large inrush currents when the converter is enabled, a soft start procedure is used to slowly (within about 500 μs) increase the output voltage to the nominal value. Several other protection mechanisms are implemented in the control circuit. An over-current protection limits the peak current in the high-side transistor (T_1 in Figure 2.7), effectively reducing the output voltage of the converter for output currents above a specific value. The maximum output current depends on several factors (input and output voltage, switching frequency and inductor value) and is about 4 A for the DC-DC converters used in CMS. An over-temperature protection disables the output completely when a temperature of 103°C is reached, and enables the converter again if the temperature falls below 73°C . An under-voltage lockout (UVLO) is implemented to avoid operation at very low input voltages, which could lead to instabilities and large currents. The UVLO consists of two stages: the first stage prevents the linear regulators, which provide 3.3 V for the drivers of the power transistors and the control circuit, from switching on at input voltages below about

4.2 V. The second stage keeps the output of the converter disabled until an input voltage of about 4.8 V is present. The UVLO has a hysteresis of a few hundred mV. Thus, the converter is disabled if the input voltage falls below 4.5 V and the regulators are disabled if the voltage falls below 3.6 V.

DC-DC converter module

The FEAST2 ASIC is soldered to a $28 \times 16 \text{ mm}^2$ large 2-layer PCB, which is shown in Figure 2.8. A resistor is used to set the switching frequency to a value of 1.5 MHz. The output voltage is set via a voltage divider network and thus cannot be changed after the components have been assembled. In the Phase-1 pixel detector, three types of DC-DC converters with output voltages of 2.4 V, 3.3 V, and 3.5 V are used. The coil is a 450 nH toroid with a plastic core. The magnetic field of 3.8 T in CMS would lead to saturation of a coil with a ferrite core, causing the ferrite core to become ineffective. The board is equipped with two identical filters at the input and the output. A 32-pin connector for mounting the converters in the pixel detector is soldered to the back of the PCB. The large ground pad at the backside serves as a cooling contact and is connected to the ASIC with thermal vias. In order to reduce electromagnetic emissions, which are in the nature of switching electrical components, a shield is mounted on the converter. It is made from deep-drawn plastic and has one layer of 60 μm thick copper at the outside, which is deposited by electroplating. The shield also acts as a cooling contact for the coil. Therefore the volume between the coil and the shield is filled with thermal paste. The shield is soldered to five GND pads on the PCB, which are in turn connected to the large cooling pad on the backside of the DC-DC converter. The weight of an assembled DC-DC converter is about 3 g. The circuit diagram and the PCB layout are shown in Figure A.1 and Figure A.2 in the Appendix. In total, 1216 DC-DC converters are installed in the Phase-1 pixel detector.

The efficiency of the PixV13 DC-DC converter at an input voltage of 10 V and with typical output currents in the range of 1 A to 2 A has been measured to be about 80 % for analog converters and 85 % for digital converters. The naming scheme analog and digital refers to the output voltages supplied by the converters ($V_{\text{out}} = 2.4 \text{ V}$ for the analog domain of the pixel modules and $V_{\text{out}} = 3.3 \text{ V}$ or 3.5 V for the digital domain). The output voltages are larger than what is required by the pixel modules to account for voltage drops on the supply tubes and the service cylinders. Two digital voltages are required because the voltage drops differ between several parts of the detector. For BPix layers 1, 3, and 4, an output voltage of 3.3 V is used. In BPix layer 2 and FPix, 3.5 V are used.

The input of the DC-DC converter is equipped with a fuse connected in series. The fuse avoids a situation in which other DC-DC converters, which are connected in parallel to the same power supply, could no longer be powered because of a short circuit at the input of a single DC-DC converter. The fuses of DC-DC converters that were initially installed in CMS were rated for a current of 1.5 A. In the year-end technical

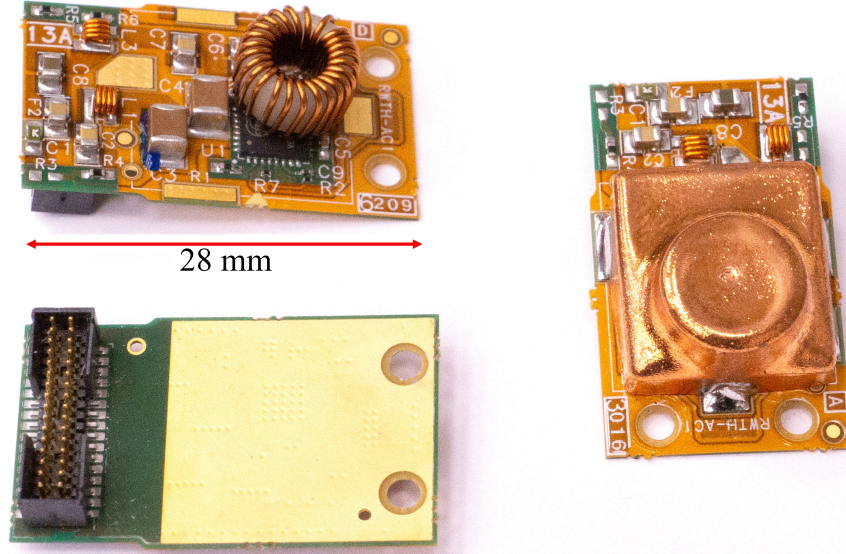


Figure 2.8.: Photographs of PixV13 DC-DC converters without shield (left) and with mounted shield (right).

stop in 2017/2018, new DC-DC converters were installed in the pixel detector. They have fuses rated to 3 A (analog DC-DC converters) and 4 A (digital DC-DC converters), respectively. This is discussed in detail in Chapter 6. Furthermore, the new DC-DC converters use a revised version of the FEAST2 ASIC (FEAST2.1). This version features a minor modification of the circuit creating the PowerGood signal. The modified DC-DC converters are named PixV14.

2.4.3. Power Distribution within the Pixel Detector

DC-DC converters of the barrel pixel detector are located on the supply tubes at $|\eta| \approx 4$ and $|z| = 2.0\text{-}2.3\text{ m}$. Figure 2.9 shows how the voltages are distributed to the pixel modules. The DC-DC converters are mounted on so-called bus boards (Figure 2.10). These PCBs consist of eight layers and have dimensions of $45.2 \times 4.1\text{ cm}^2$. A bus board houses 13 analog and 13 digital DC-DC converters, which serve up to 39 pixel modules. The DC-DC converters are screwed onto low mass cooling blocks. A cooling block consists of two anodized aluminum parts. The lower part is glued to the bus board, while the upper part is screwed onto the lower part. Cooling tubes are embedded in two notches between both parts. The cooling block is in contact with the large copper pad on the backside of the DC-DC converter and thus ensures good heat dissipation.

Up to four pixel modules are connected in parallel to a DC-DC converter. The number depends on the layer, as Table 2.1 shows. Three pairs of DC-DC converters each serve pixel modules in layers 1 to layer 3, and four pairs serve pixel modules in layer 4.

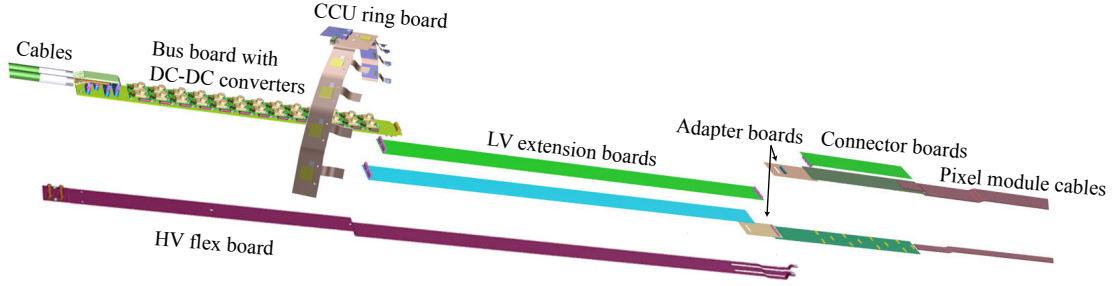


Figure 2.9.: Schematic view of the power distribution in the barrel pixel detector.

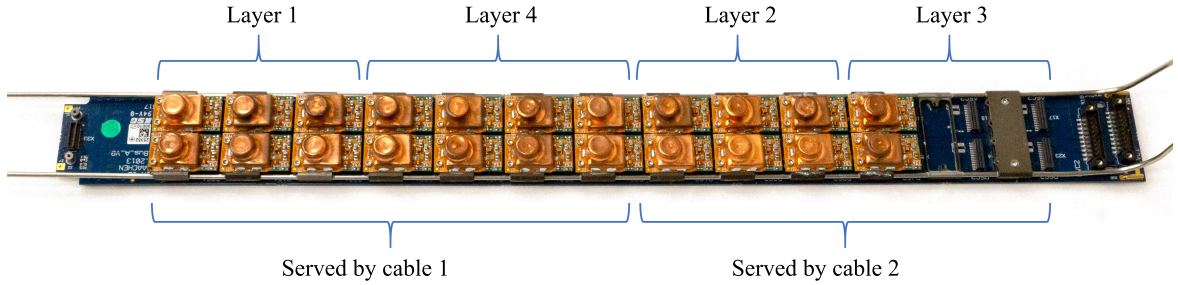


Figure 2.10.: Photograph of the bus board. Four DC-DC converters at the right end are not mounted for illustration purposes. Two cooling blocks are visible. One is completely assembled, of the other one only the lower half is visible. The layers of pixel modules, which are powered by the corresponding DC-DC converters, and the two power groups, are indicated.

A series of PCBs routes the voltages of the DC-DC converters, which are also called low voltages (LV), to the pixel modules. In the direction towards the pixel detector, the bus board is connected to two extension boards. Two adapter boards connect the extension boards to three connector boards, one of which is used for layer 4, one for layer 3 and one for layers 2 and 1. The cables of the pixel modules are plugged into the connector boards. The high voltage (HV) for the silicon sensors of the pixel modules is fed to the adapter boards with a so-called HV flex board. The HV board consists of flexible Kapton with two copper layers.

The bus board and the HV flex board are connected to power supplies via cables in the direction facing away from the detector. The same power supplies provide the input voltage for the DC-DC converters as well as the high voltage. A short pigtail cable is used to connect the bus board and the HV flex board to a common supply cable. Each bus board is connected to two power supplies and can therefore be divided into two so-called power groups. The inputs of all DC-DC converters in the same power group

Table 2.1.: Number of DC-DC converter pairs per layer and number of pixel modules that are powered from the same pair. The values are given for one BPix bus board.

	Number of DC-DC converter pairs	Modules per DC-DC converter pair
Layer 1	3	1
Layer 2	3	3 or 2
Layer 3	3	4
Layer 4	4	4

are connected in parallel. The DC-DC converters for layers 1 and 4 form a power group and DC-DC converters for layers 2 and 3 form another power group.

The CCU ring board, which is explained in Section 2.3.2, is plugged into the bus board. Single pairs of DC-DC converters (one analog and one digital) can be switched off by the CCU. The CCU has programmable PIA (Peripheral Interface Adapter) channels, which can generate a voltage of 2.5 V. These voltages are used as disable voltages for the DC-DC converters and are routed across the bus board to the corresponding devices. Furthermore, the CCU can read back whether the PowerGood signal of a DC-DC converter pair is low or high.

The DC-DC bus board, the extension boards, the HV flex board, and the CCU ring board, as well as the DC-DC converters, were developed at the RWTH Aachen University.

DC-DC converters of the FPix detector are mounted on so-called DC-DC motherboards. One board carries four pairs of DC-DC converters, each powering either three or four pixel modules. One DC-DC motherboard serves a single port card, to which it is connected with an approximately 0.4 m long twisted pair cable. The FPix system employs additional filter cards between the power supply and the DC-DC converters. The input voltage of the DC-DC converters is transmitted from the filter cards to the DC-DC motherboards via 0.95 m long twisted pair cables.

2.4.4. Power Supplies

The Phase-1 pixel detector integrates the modular SY1527 power supply system [54] developed by CAEN. The system is divided into two parts: The SY1527 mainframe, which is located in the detector control room, and five EASY4000 power supply crates [55], which are located in the experimental cavern in the proximity of the detector. The mainframe is used to control the system via a network. It houses three A1676A cards, known as Branch Controllers, that connect the mainframe with the power boards in the

experimental cavern via approximately 100 m long cables. All electronic boards used in the experimental cavern are suited for the operation in hostile environments, as they are magnetic field and radiation tolerant. Six A3468H power supplies that transform 400 VAC to 48 VDC are used to feed the EASY4000 crates. These host 16 A4602 and 56 A4603 power supplies, which generate the required voltages for the pixel detector.

Figure 2.11 illustrates the powering scheme of the Phase-1 pixel detector. The auxiliary electronics is powered from A4602 power supplies, which were already used in the Phase-0 detector. They could be reused because the auxiliary power consumption is comparable. Each power supply of this type provides four individual channels that have a maximum output rating of 56 W.

Power for the pixel modules is provided by CAEN A4603 power supplies. Software and hardware modifications were implemented in the A4603H power supplies, which have been used in the Phase-0 detector, to make them compatible with the DC-DC conversion scheme. The modifications were implemented by CAEN technicians during the technical stop in Winter 2016/2017.

The modified power supplies, which are named A4603D, deliver an increased output voltage of up to 13 V for the analog and the digital channel². In return, the maximum output current is reduced from 13 A to 9 A (digital) and from 6 A to 5 A (analog). The power supply consists of two independent power supply units (PSU). A PSU has two channels that deliver the analog and digital voltages. The voltage can be programmed for each channel individually between 8.0 V and 12.5 V, with an accuracy of 0.1 V. Furthermore, a PSU has two channels that deliver the high voltage for the pixel sensors. The bias voltage can be set between 0 V to -600 V, and a maximum current of 20 mA can be drawn per channel.

The power supplies are connected to the detector with so-called multi-service (MS) cables and auxiliary power cables. About 30 m to 40 m long cables run from the power supplies to a patch panel (named PP1) inside CMS. From there, 5 m long cables connect to a second patch panel (named PP0, also known as tracker bulkhead), and further 0.5 m long cables connect PP0 to the supply tubes and service cylinders.

In the Phase-0 detector, the power supplies compensated for voltage drops on supply cables by increasing the actual output voltage. Voltage drops depend on the current drawn by the pixel modules and therefore on the instantaneous luminosity. A fast regulation was implemented in the A4603H, which reacted to load changes within 200 μ s. The fast remote sensing has been removed in the A4603D power supplies, to avoid oscillations, which could occur due to interference with the regulation of the DC-DC converters. Instead, a slow remote sensing feature with a reaction time of about 0.6 s has been implemented. If enabled, remote sensing compensates voltage drops along the multi-service cable by increasing the output voltage of the power supply. The actual voltage at the input of the DC-DC converters is sensed at the supply tubes and the service cylinders, inside CMS.

²The original power supplies could only provide voltages up to 5.8 V (analog) and 7 V (digital).

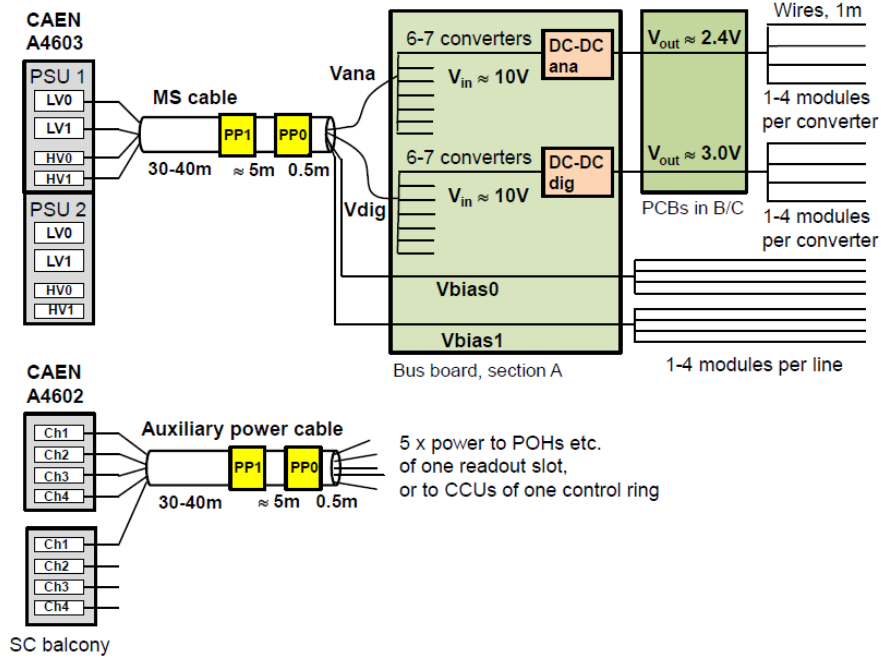


Figure 2.11.: Powering scheme of the Phase-1 pixel detector [32].

2.5. Detector Geometry

In the following, the mechanical construction of the pixel detector is described. The pixel modules are mounted in parallel to the beam axis in the BPix detector, while in the FPix detector all pixel modules are mounted perpendicular to the beam axis. A schematic layout of the Phase-1 pixel detector and a comparison with the Phase-0 design is shown in Figure 2.12. The Phase-1 pixel detector features an additional layer of modules in the barrel and the endcaps. In total 1856 pixel modules with 124 million readout channels are installed in the upgraded detector. The additional layers make a full four-point coverage in the whole tracking region possible and also reduce the interpolation distance between the last pixel layer and the first strip tracker layer. The radius of the innermost layer has been reduced from 44 mm to 29 mm to improve the vertex resolution and the b-tagging efficiency.

A BPix half cylinder consists of four layers at radii of 29 mm, 68 mm, 102 mm, and 160 mm. Each layer is composed of so-called ladders, which are made from carbon fiber. The ladders are aligned along the beam pipe. They are 56 cm long and only 550 μm thick. Each ladder carries eight pixel modules. Grooves are milled into the back of the ladders, into which cooling tubes are glued. Ladders are arranged next to each other in the ϕ -plane, as shown in Figure 2.13. The pixel modules are mounted either on the inside of the ladder or on the outside of the ladder. Adjacent pixel modules overlap in the ϕ -plane by 0.5 mm to 1.0 mm, depending on the layer. The layers are connected to

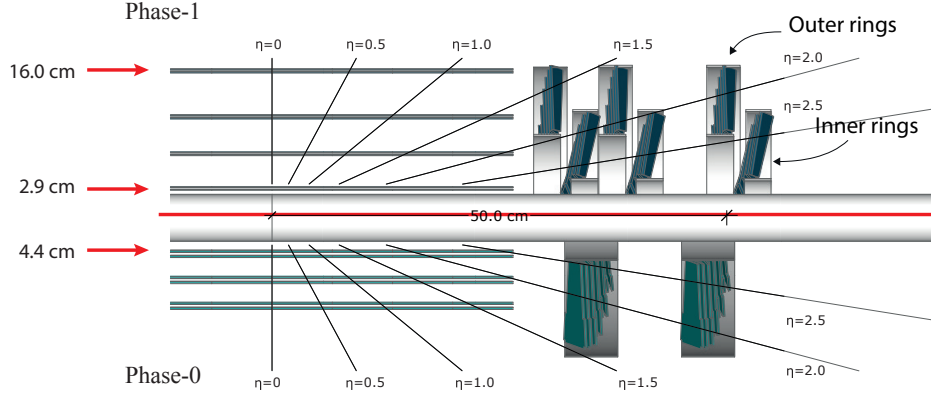


Figure 2.12.: Comparison of the Phase-1 detector layout (top) and the Phase-0 detector layout (bottom). One quarter of the detector is shown. Modified from [32].

an end flange at each side of the half-shell to stabilize the mechanical structure. The lightweight flange is made of 4 mm thick Airex foam, which is stiffened by thin carbon fiber sheets. The mechanical structure is designed such that the innermost layer can be exchanged rather easily. Increased sensor leakage currents and a degraded readout chip performance due to radiation damage may make at least one exchange of layer 1 during the LHC Run 2 necessary. At the moment, it is planned to exchange layer 1 in LS2 in 2019.

Each FPix half cylinder holds three half disks with pixel modules. The disks are further divided into an inner ring with 22 modules and an outer ring with 34 modules, as shown in Figure 2.14 (left). Rings are made from a carbon-fiber-reinforced carbon frame and support panels, so-called blades, which are made from Thermal Pyrolytic Graphite. The blades are bonded in a turbine-like geometry to the rings. They hold the modules in position and provide the cooling contact. Heat is transferred through the blades to the cooling tubes, which are integrated in the carbon frame.

Pixel modules are screwed to the blades, as illustrated in Figure 2.14 (right). A module is mounted on each side of the blade to have an overlap in ϕ . In both rings, the modules are rotated by 20° with respect to the radial axis. In the inner rings they are additionally tilted by 12° with respect to the interaction point (illustrated in Figure 2.12). This geometry enhances the effect of charge sharing between neighboring pixels, leading to an improved position resolution.

Five different types of pixel modules with different sensor geometries and different numbers of readout chips were used in the Phase-0 FPix detector. In contrast, all pixel modules are from the same type in the upgraded FPix detector.

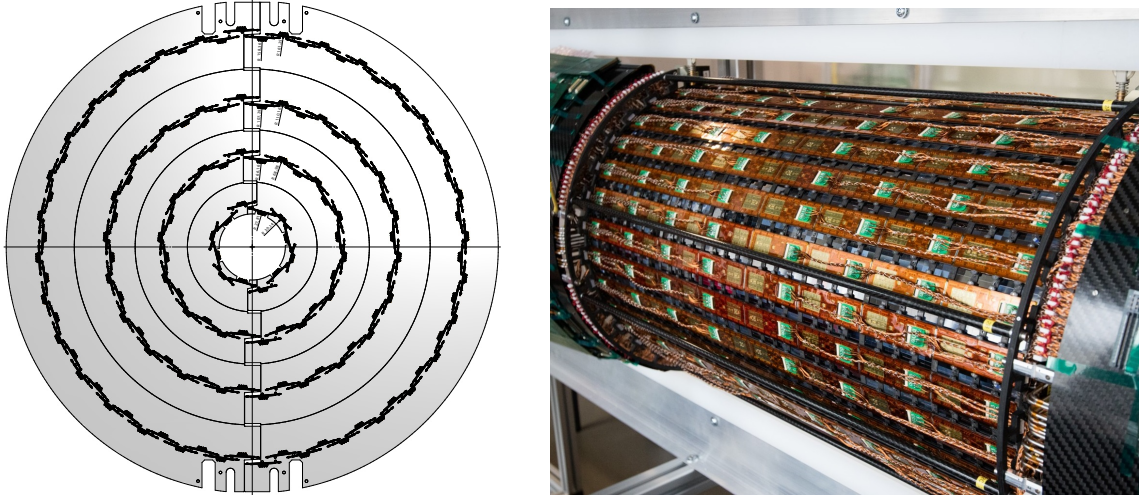


Figure 2.13.: Left: schematic view of the barrel detector in the $r\phi$ -plane [32]. Right: photograph of the outermost layer of the barrel detector.

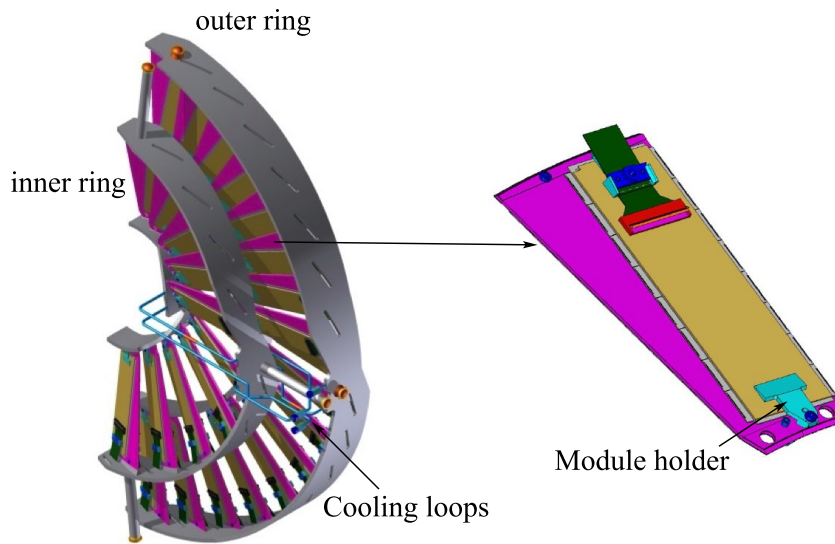


Figure 2.14.: CAD model of a FPix half disk. The pixel modules (brown) are mounted on blades (purple), which are connected to a carbon frame (gray) that has integrated cooling loops. Modified from [32].

2.6. Supply Tubes and Service Cylinders

The auxiliary electronics, which are required to operate the pixel modules, and the DC-DC converters for the barrel pixel detector are integrated on the supply tubes. There are four half cylinders, each of which is referred to as a supply tube in the following. They are named according to their position in the CMS coordinate system. Since the pixel modules are each connected to one of the four supply tubes, the BPix detector is also logically divided into four parts. There is a minus side ($z < 0$) and a plus side ($z > 0$). Furthermore, a distinction is made between inner ($x > 0$) and outer ($x < 0$). The four quadrants are named BmO ($z < 0, x < 0$), BmI ($z < 0, x > 0$), BpO ($z > 0, x < 0$), and BpI ($z > 0, x > 0$), accordingly.

The supply tubes are made from lightweight Airex foam, which is covered by carbon fiber plates. End flanges made of aluminum and glass-fiber reinforced plastic are used to stiffen the structure. The end of the supply tube that is close to the pixel detector lies within the CMS tracking volume. Therefore, it is solely made of carbon fiber plates to reduce the material budget further. After all components were mounted, the supply tube was covered in shielding foils to prevent electromagnet interference with other detector systems.

Figure 2.15 shows the layout of one BPix supply tube. In ϕ -direction, each supply tube is divided into nine sectors. The central sector contains return cooling lines and the DOHs of the CCU ring. The other eight sectors contain cooling pipes as well as the power, control and readout electronics for up to 39 pixel modules, respectively. Individual sectors are separated from each other. Only the CCU ring board spans across all sectors. In z -direction, the supply tube can be divided into four sections, A to D, with section D being closest to the detector. Section A of each sector holds the bus board with 13 pairs of DC-DC converters. Section B contains the low voltage extension boards as well as the POH motherboard, which is mounted on top of the power boards. Section C contains the connector boards, into which the pixel module cables are plugged. The optical fibers are routed out of the detector on top of the DC-DC converters in section A.

The four FPix half cylinders are made from carbon fiber. A CAD model of the FPix service cylinder is shown in Figure 2.16. The pixel modules are connected to the port cards, which host all electronic components required for the control and readout. Each port card drives 14 pixel modules, which corresponds to one quarter of a half disk. A half cylinder contains 12 port cards, 12 DC-DC motherboards, and one CCU motherboard.

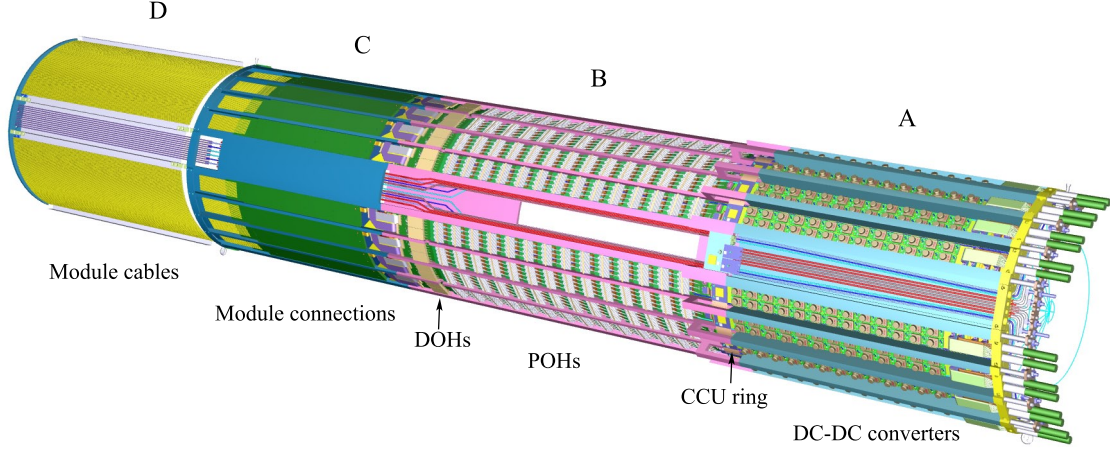


Figure 2.15.: CAD model of a BPix supply tube. In ϕ -direction, the supply tube is divided into eight equally equipped sectors and a central sector. In z -direction, the supply tube is divided into four sections. The power boards in section B are installed below the POHs and are therefore not visible.

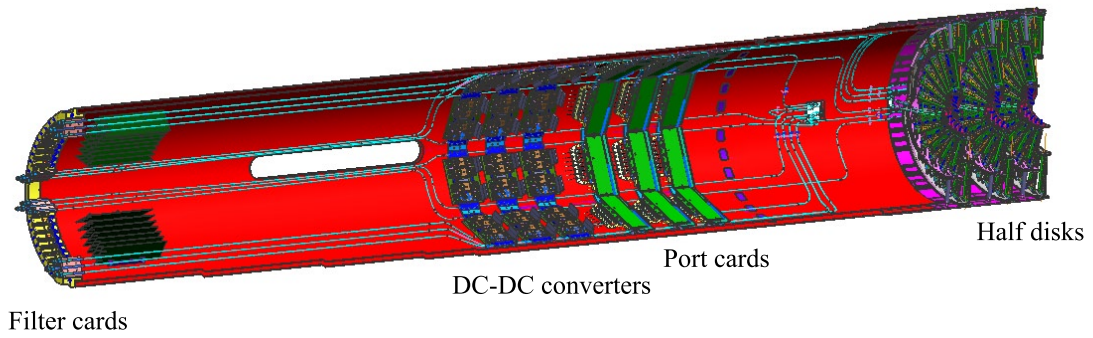


Figure 2.16.: CAD model of the FPix service cylinder [56].

2.7. Cooling

A new two-phase CO_2 cooling system was developed for the Phase-1 pixel detector. It replaces the original cooling system with liquid C_6F_{14} . Conventional mono-phase liquid cooling systems dissipate heat from the detector by warming up the liquid. In contrast, the coolant is evaporated in a two-phase cooling system. Therefore, the temperature is almost constant along a cooling pipe, and the latent heat also contributes to the heat transfer. Considerably less coolant has to be used, which reduces the total mass of the cooling system. The latent heat of CO_2 at the design temperature of the Phase-1 pixel detector of -20°C is about two orders of magnitude larger than the heat capacity.

Two-phase cooling with CO_2 allows the use of thin cooling pipes, resulting in a significant mass reduction compared to the original system. Parallel cooling pipes made of stainless steel are routed through the supply tubes and the service cylinders to the pixel modules. The outer diameter of the pipes is 2.2 mm along the supply tubes and 1.8 mm in the tracking volume. The wall thickness is 50 μm . The same pipes cool DC-DC converters, POHs, and the pixel modules. The CO_2 enters the detector in the liquid mono-phase state. Active components on the supply tubes and service cylinders provide a so-called pre-heating and bring the CO_2 in the two-phase state before it reaches the pixel modules.

Two identical cooling plants provide a cooling power of about 30 kW, whereas about 10 kW to 11 kW are required [32]. The system is based on the so-called 2-Phase Accumulator Controlled Loop (2PACL) method, which is described in references [57, 58].

3. Qualification of Pixel Modules

The Phase-1 barrel pixel detector was mainly built by European institutes, whereas a US consortium built the forward detector. In total, 1184 pixel modules are mounted in the barrel detector. It was necessary to distribute and parallel the module production across several institutes to ensure compliance with the strict schedule of the Phase-1 upgrade. A Swiss consortium, consisting of the Paul Scherrer Institute (PSI) and the ETH Zürich, was responsible for the construction of layer 1 and layer 2 pixel modules. Layer 3 modules were produced by CERN, the Helsinki Institute of Physics (HIP), and the Italian Institute for Nuclear Physics (INFN). Two German consortia produced modules for layer 4. Half of the 512 required modules (plus about 20 % of additional spares) were built by the Karlsruhe Institute of Technology (KIT) and tested at RWTH Aachen University. The other half was produced and tested by the University of Hamburg and Deutsches Elektronen-Synchrotron (DESY).

This chapter is dedicated to the module qualification tests that were performed during series production at RWTH Aachen University. In the first part, the assembly of the pixel modules in Karlsruhe is briefly described. The readout electronics and software used in the qualification procedure are presented. Two test setups were used to qualify the pixel modules. In a cold box setup (Section 3.3), the modules were tested for electrical function and were thermally cycled. In an X-ray setup (Section 3.4), high-rate tests with photons and an energy calibration of the on-chip charge injection mechanism were performed. The two test setups are presented, and the test routines are explained in detail. Section 3.5 summarizes the results from both setups and describes the course of the module production. The pixel modules of all production centers were collected at ETH Zurich. After transport, a reception test was carried out for each module. This test is described in Section 3.6.

Within the scope of this work, the cold box setup was developed based on preliminary work [6]. The procedure for testing the modules is similar to the one used to test pixel modules of the Phase-0 pixel detector [59]. The procedure was developed mainly by the Swiss consortium. It was implemented in the cold box setup presented here. For this purpose, a control software was developed with the National Instruments LabVIEW development environment [60]. The qualification tests were carried out automatically with this software. Before the series production, the function of the routines was verified with prototypes of the Phase-1 pixel modules.

An X-ray setup was improved and prepared for the testing of Phase-1 pixel modules. The results of a master thesis [7] submitted in 2014 were incorporated. The setup was

modified to test two pixel modules simultaneously. The control software was adapted to new software that was used to read out pixel modules. Prototypes of the pixel modules were used to develop the test routines for the high-rate test and to develop the grading criteria. Furthermore, requirements for the global database, to which the test results of all production centers were uploaded, were defined. The test routines developed in this work were adopted by the other production centers involved in the module production.

Furthermore, the infrastructure required for the tests during series production was set up. In both setups, 389 modules produced at KIT were tested, partly with the help of two student assistants. Within the scope of this work, the tests were coordinated, and all results were analyzed.

3.1. Module Production at KIT

Most of the parts required for the pixel modules were produced in industry. The pixel modules were then assembled at KIT. The assembly procedure summarized here is described in detail in references [61–64]. The sequence of the different production steps is shown in Figure 3.1. Sensors were made by CiS Forschungsinstitut für Mikrosensorik GmbH in Germany. This company had already made the sensors for the Phase-0 pixel detector. This choice was a cost-effective and time-saving solution, because the original sensor design for the Phase-1 upgrade remained unchanged. Qualification of a new sensor technology or the manufacturer was not required.

The flip-chip assembly of the readout chips requires an Under Bump Metallization (UBM) of the aluminum pads on the silicon sensor. The UBM consists of several layers of palladium, nickel and gold [64]. It ensures a good electrical and mechanical connection between the aluminum pads and the solder bumps and also prevents diffusion from the bump to the silicon die [65]. The UBM deposition on the sensor wafers and the wafer dicing were done by PacTech in Germany.

The readout chips were produced on 8-inch wafers by IBM. All ROCs were tested on the wafer at PSI before further processing [66]. The wafers were sent to RTI International, a company based in the USA, which was responsible for the preparation of ROCs for flip-chip mounting. The preparation included deposition of a UBM, deposition of the solder bumps, as well as thinning and dicing of the wafers. The spherical bumps are composed of tin (63 %) and lead (37 %). They have a diameter of 30 μm . The ROC wafers were thinned down to 175 μm to reduce the material budget.

Sensor and readout chips were sent to KIT for further processing. The leakage current of every silicon sensor was measured as a function of the depletion voltage. The currents were compared to a measurement at CiS to verify that the sensor was not damaged during processing. The readout chips were cleaned, and remaining photoresist from the ROC processing was removed. Every readout chip underwent a semi-automated optical inspection under a microscope. A pattern recognition software was used to find

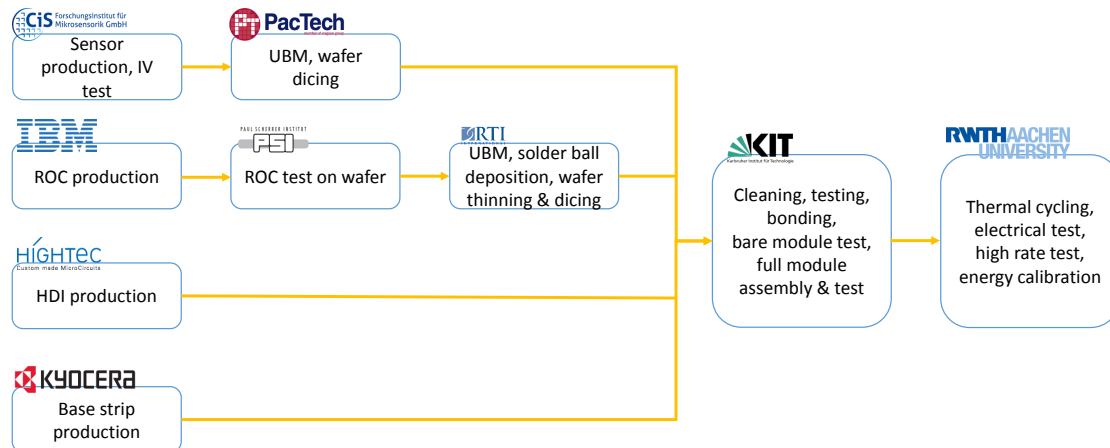


Figure 3.1.: Overview of the pixel module production workflow within the KIT/RWTH Aachen consortium.

ROCs with several missing solder balls, to detect contaminants, and to monitor the dicing quality.

The flip-chip bonding was done with a FINEPLACER femto built by Finetech GmbH. After placing a ROC on the sensor, the machine applies a bond force and heats the ROC to 140 °C to melt the solder balls. All ROCs are connected to the sensor sequentially. The assembly of a sensor with 16 mounted ROCs is called a bare module. All bare modules were tested electrically before proceeding with further steps, to avoid mounting expensive components on defective bare modules. Electrical contact with each ROC was established for this test with a probe card. It was verified that each ROC could be programmed, and the number of missing bump bonds was measured (the procedure to determine the number of missing bump bonds will be described in Section 3.3.2). Furthermore, the I-V characteristic of the sensor was measured again.

If a ROC was found defective, it was removed from the module and replaced by a new one. Bare modules that passed the test were put in an oven at 240 °C for about 30 minutes to reflow the solder. This step was required to connect the ROCs to the module permanently. Thereafter a rework was not possible anymore.

Base strips and the HDI have to be glued to the bare module to assemble a full module. Kyocera Corporation produced the silicon nitride base strips. Hightec MC AG in Switzerland produced the HDIs. The Token Bit Manager chips were glued onto the HDIs and connected by wire bonding. Optical inspections were carried out before and after assembly, and an electrical test was performed to verify the functionality of the TBM. In the last step of the production, all ROCs were wire bonded to the HDI. Figure 3.2 shows a photograph of a fully assembled module.

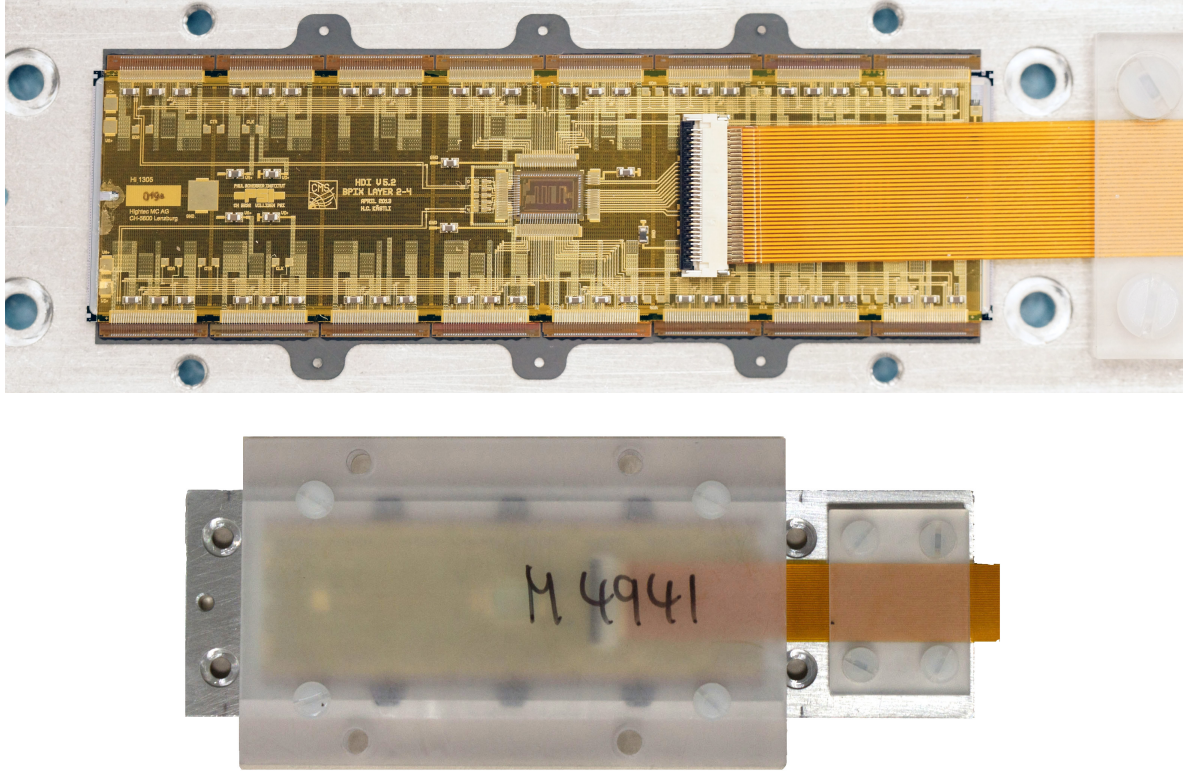


Figure 3.2.: Photographs of a layer 4 pixel module. Top: assembled full module with attached sacrificial cable. Bottom: the pixel module is mounted on an aluminum handle for transport and testing. A plastic cover is screwed to the handle to fix and protect the module.

A 25 cm long flexible cable, which is hereafter called sacrificial cable, was connected to each module for further testing of the assembled modules. The micro twisted pair cable, which is used in the detector, was not mounted at that point to ease the handling during testing. The micro twisted pair cable has a length of about 100 cm, it is quite stiff, and there is a significant risk of breaking the cable by bending. The sacrificial cable was used throughout the whole qualification procedure. It was exchanged with the final cable only before mounting in the detector. To protect the modules during handling and testing, they were mounted on a thin aluminum handle, as illustrated in Figure 3.2. The module was held in position by two dowel pins that were inserted in the screw holes of the base strips. A plastic cover was screwed to the handle to press the base strips of the module against the aluminum. As a benefit, the cooling contact between the module and the aluminum is enhanced.

3.2. Quality Assurance at RWTH Aachen

Each module was subjected to a series of tests, to ensure that only reliably working modules were installed in the pixel detector. One of the reasons was to speed up the mounting of modules on the support structure because the removal of defective modules is risky and time-consuming. In addition, most pixel modules are unreachable once the various layers of the detector are joined. Furthermore, it is not possible to repair the detector during LHC operation. Therefore, the functionality of the modules must be ensured for several years. The tests would also enable the detection and elimination of systematic sources of error during production. For this purpose, the qualification at RWTH Aachen University had to be carried out shortly after modules were produced at KIT. In the electrical tests also optimal values for the programmable digital-to-analog converters of the readout chips were determined. These values were used during the checkout of the detector and also during data taking in 2017, and some of them are still used today.

Since more pixel modules than needed were produced, not all of them were installed in the detector. To ensure that preferably the best modules were installed, they were divided into four classes (A, B, C, C*). The criteria for the classification were based for example on the number of defective pixels or pixels not connected to the sensor, the electrical performance (noise, data encoding errors, efficiency) and the sensor leakage current. For example, a high number of defective pixels reduces the detection efficiency of the module and would lead to a downgrading in this scheme. A more detailed specification of the criteria can be found in the respective section of the individual tests below. The classification followed a general scheme: an individual grade was given to each ROC and the sensor. The worst of any grades corresponded to the module grade. In the best chips (grade A), less than 1 % of the pixels (41 of 4160) had any defects, and the function of the chips was not degraded in any way. If there were more than 1 % but less than 4 % pixels (166 of 4160) with defects, the chip received the B grade. In this case, the module could also be used for the detector. If more than 4 % of the pixels were defective or the function of the ROC was otherwise compromised (for example, if the efficiency was reduced or data encoding errors occurred frequently), the module was graded C and was not used for the detector. Because the pixel modules were qualified in two independent setups (cold box and X-ray setup), the grading was also determined independently. The worst of both grades was used as the final grade. In the course of the production, an additional fourth grade (C*) was introduced. This grade was assigned to ROCs in which a whole double column was broken (80 broken neighboring pixels), which would otherwise result in grade B. It was planned to install these modules only in case there were not enough grade A and B modules available. However, this was not the case, and no C* modules were installed in the Phase-1 pixel detector.

3. Qualification of Pixel Modules

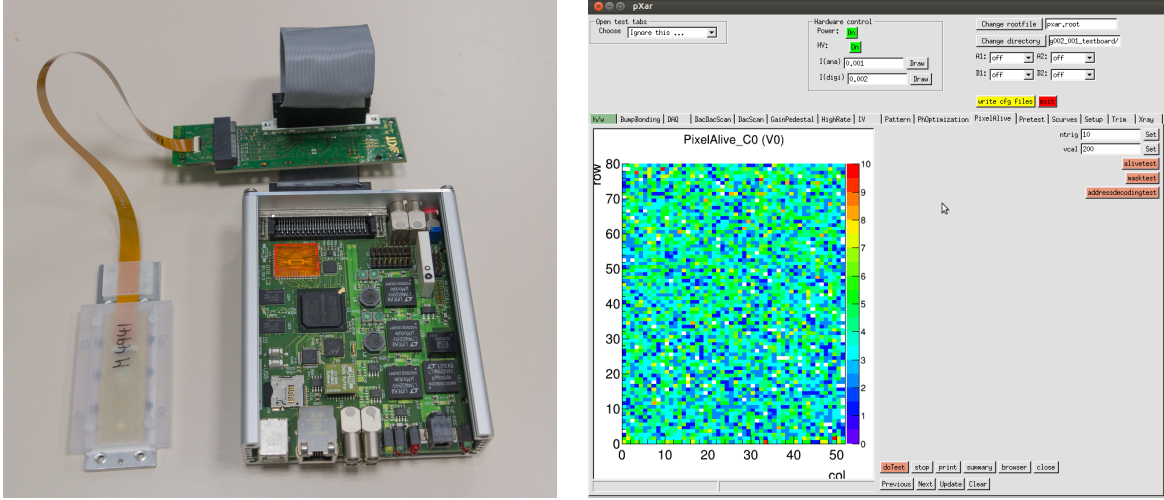


Figure 3.3.: Left: pixel modules are read out with the digital testboard (DTB). Right: GUI of the pXar software, which was used to run the test procedures in all production centers.

The qualification of pixel modules was similar in all production centers. In particular, the same hardware and software were used to read out the pixel modules and to analyze the data, to ensure comparability of results between the different centers. The pixel modules were read out with a so-called Digital testboard (DTB) [42], which is shown in Figure 3.3. Digital refers to the digital data format of the psi46dig readout chip, for which the board was designed. Module cables are connected with an adapter card. The DTB generates the required analog and digital voltages for the ROCs and the TBM and passes the high voltage, which has to be provided by an external power supply, to the sensor. The testboard features an Altera FPGA (Field Programmable Gate Array), a 128 MB large memory, and is connected to a computer via a USB 2.0 interface or ethernet. The DTB generated all signals that are required for the operation of a pixel module (clock, trigger, control signals). Deserializers are implemented in the firmware to decode the data sent by the TBM. Since the data transfer rate of the USB connection is too low for a direct readout, the events are buffered in the memory of the DTB before being sent out to the computer.

Various test routines were started from a computer. These were implemented in the C++ based software package called pXar [67]. It is possible to control the software via a graphical user interface (GUI) or to run it from a command line. The GUI, which is shown in Figure 3.3, is useful for debugging problems, while the command-line was mainly used to automate the testing. The DAC parameters and trim bits for each ROC of a module are stored in text-based configuration files. The results of the various test routines are usually saved as ROOT [68] files. These can be further processed and analyzed in other software. During the series production, several test routines were run in a predefined order. The entire procedure is called FullTest.

A software called MoReWeb, which was used for the analysis of the test results, was developed at ETH Zürich. The software is written in the Python programming language. It summarizes the results of the individual test routines and visualizes them in the form of web pages. An example result is shown in Figure 3.4. The previously defined grading criteria are applied, and the resulting module grade is calculated. Because the qualification of the modules was done in two different setups, the analysis of the data was also split into electrical tests in the ColdBox, the energy calibration with X-ray photons, and the high-rate test. A global overview page displays the results of each of these three tests for all tested modules. For the module qualification in Aachen, a local server was set up, on which two instances of MoReWeb were executed (one instance for each of the two setups).

A global database was used to collect the results from all production centers. For each pixel module the ROOT files, which were created by the pXar software, and the DAC parameter files were packed in an archive file. The archive files for all modules were uploaded onto a server. The back-end of the database used MoReWeb to process and evaluate the data and to grade the modules. The results of other tests that were carried out during module production were uploaded as well (e.g., I-V measurements of the sensors before processing, results of the bare module test). Furthermore, the status and the location of all parts (ROCs, sensors, HDIs, bare modules, full modules) were tracked. Thus, the database provided an overview of the overall status of the production and the testing at any time. A screenshot of the database GUI can be found in Figure A.7 in the Appendix.

3. Qualification of Pixel Modules

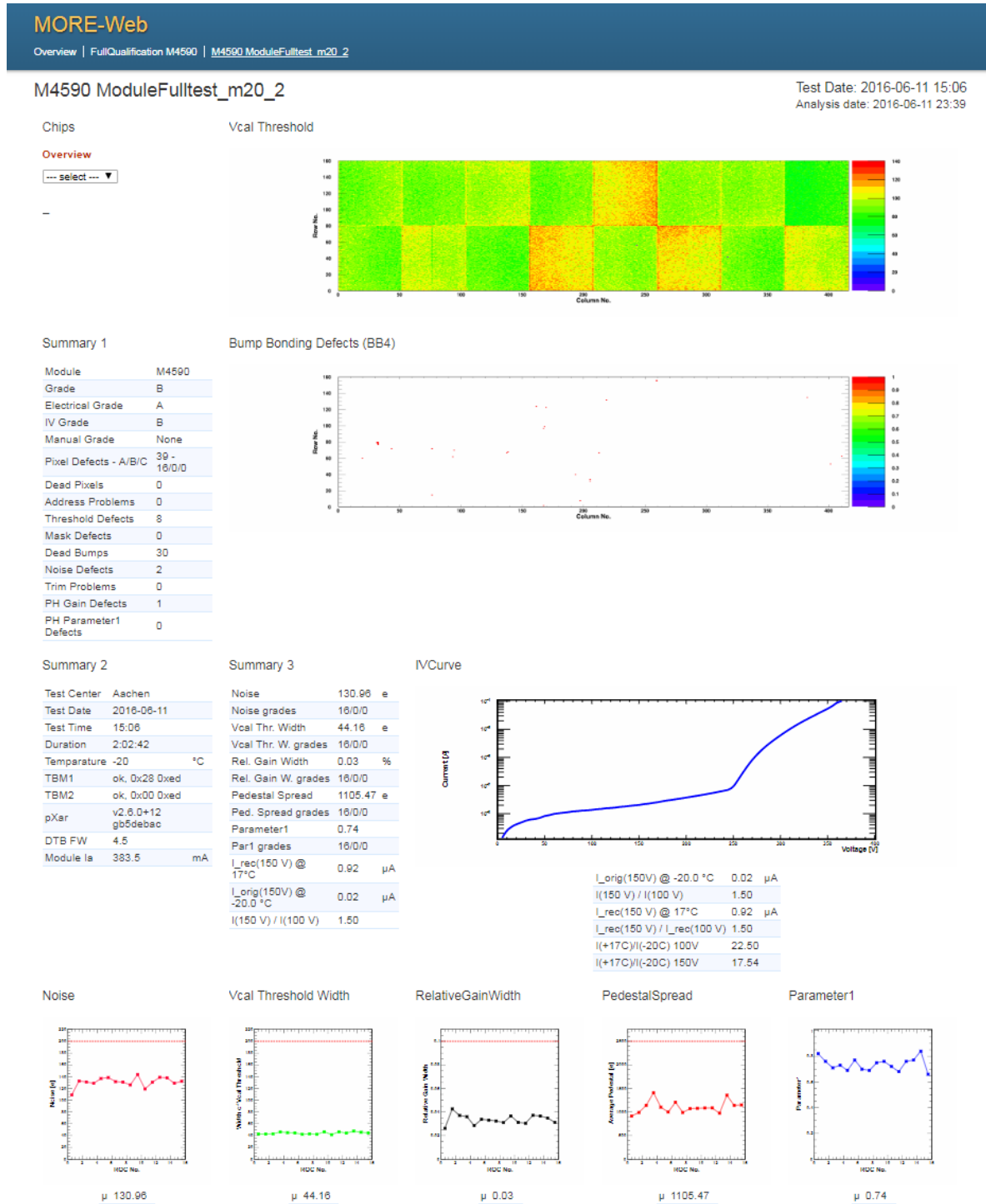


Figure 3.4.: Web page that summarizes the results of a so-called FullTest of a single pixel module, created by MoReWeb.

3.3. Cold Tests

It was planned to operate the Phase-1 pixel detector at a coolant temperature of about -20°C , but operation at warmer temperatures is also possible during technical stops of the LHC and detector checkout. The optimal values of some DAC parameters of the readout chips depend on the temperature and therefore have to be adjusted accordingly. The electrical tests, in which the DAC settings were optimized, were therefore performed at the foreseen operating temperature of -20°C and at $+17^{\circ}\text{C}$. Furthermore, a thermal cycling was performed to ensure the long-term reliability of the pixel modules. Temperature cycles in the detector are caused, for example, by on/off cycles that occur during regular operation. A mismatch in the coefficient of thermal expansion (CTE) between silicon and the solder material leads to mechanical stress in the bump bond connections. In the worst case the connection breaks. Cracks can also be initiated from contaminated pads, contaminated solder materials, voids and from flaws introduced in the dicing process [69, 70]. Every pixel module underwent at least 10 active thermal cycles between -25°C and $+17^{\circ}\text{C}$ to spot such defects. Active in this respect means that the low and the high voltages were turned on during the cycling. It was assumed that if a pixel module is not damaged in this test, it can sustain thermal cycles that occur during detector operation.

3.3.1. Description of the Setup

The electrical tests were performed in a cold box, which was designed and built in-house. Figure 3.5 shows a photograph of the setup, in which up to four pixel modules can be tested simultaneously. The cold box is made of pieces of extruded polystyrene foam and has a lid that can be opened. A two-stage cooling system, which is illustrated in Figure 3.6, regulates the temperature inside the box. The top layer consists of a $19 \times 25 \text{ cm}^2$ wide aluminum plate, on which up to four pixel modules can be placed. Four Peltier elements are connected to the backside of this plate to ensure a fast temperature stabilization. They are driven by a temperature controller, which has an embedded control loop that keeps the plate at the set temperature. The Peltier elements are operated with a maximum cooling power of about 170 W. Depending on the operation mode (cooling or heating), the Peltier elements transport heat to or away from their backside. A second aluminum plate with integrated cooling loops is used as a heat reservoir and is attached to the backside of the Peltier elements. The second plate is connected to an external recirculating chiller (Huber Unichiller 020Tw [71]), which is running with silicone oil and has a maximum cooling power of 800 W at a temperature of -20°C .

Several temperatures in the setup are measured with Pt-100 type RTDs (resistance temperature detectors). Two such temperature sensors are attached to the upper cold plate, close to the pixel modules. The measured temperature of these sensors is referred to as the cooling block temperature in the following. A third sensor measures the

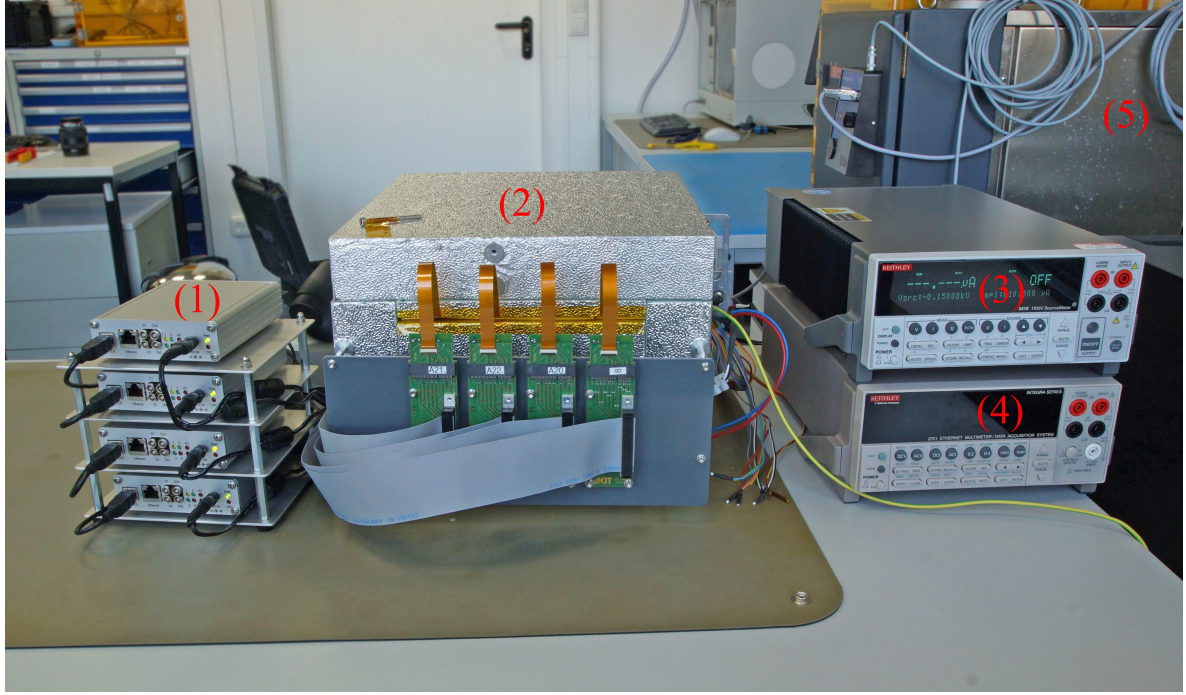


Figure 3.5.: Photograph of the cold box setup. The image shows the four digital test-boards (1), the cold box (2), the high voltage power supply (3), the multimeter (4) and the liquid chiller (5). The controller for the Peltier elements is located below the table and is not shown.

air temperature in the box. Furthermore, the relative humidity is measured with a Honeywell HIH-4000-001 humidity sensor [72]. The cold box is continuously flushed with dry air to avoid condensation. A switch can also be used to check whether the lid of the box is open or closed. The resistances of the temperature sensors, the output voltage of the humidity sensor, and the status of the switch are read out with a Keithley 2700 multimeter [73].

The Peltier controller has its own temperature sensor, which is also mounted on the upper cooling plate. Two additional temperature sensors are integrated into the lower cooling plate. One sensor measures the temperature on the back side of the Peltier elements. It is connected to and read out by the Peltier controller. The second sensor is mounted close to the inlet of the cooling fluid. This sensor is used for the temperature regulation of the chiller.

Figure 3.7 shows a photograph of the opened cold box. The pixel modules are held in position by aluminum frames, which are screwed to the upper plate. The frames push the module handles down against the plate. Furthermore, a vacuum can be applied through small channels, which are drilled in the cold plate. The vacuum increases the contact pressure. Therefore, the heat flow from the module handles to the cold plate is improved. The flat module cables are routed outside the box at the front and connect

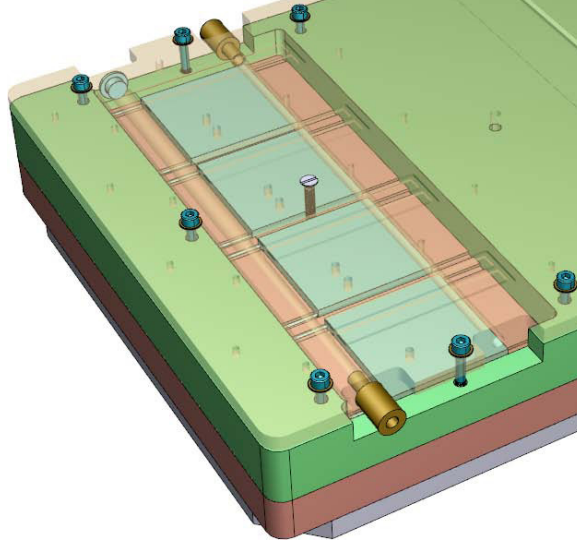


Figure 3.6.: CAD drawing of the different layers of the cooling system [6]. It shows the lower plate (red), four Peltier elements (light blue) and the upper cooling plate (semi-transparent), as well as the connections for dry air and vacuum. The vacuum channels in the upper plate are indicated. The thermal insulation is shown in green.

to adapter cards, from which the signals are sent to four digital testboards. The DTBs are used to read out and power the pixel modules. The sensor bias voltage is provided by a Keithley 2410 high voltage power supply [74]. All pixel modules were tested with a bias voltage of 150 V.

Within the scope of this work, the National Instruments LabVIEW software was used to create a program to control and monitor the setup. The so-called VI (virtual instrument) steers all devices in the setup, interacts with the DTBs and the pXar software, and prepares result data to be analyzed with MoReWeb. A graphical user interface summarizes the status of the setup. The program was designed to be easily adaptable to changes in the test routines, as the final test procedures were not yet defined when the program was developed.

The front panel¹ of the application is shown in Figure 3.8. It is possible to run any combination of predefined commands by inserting the command name and optional parameters in the list on the top left. Therefore, new tests can be added to the standard qualification procedure easily. The setup can also be used for debugging problems by running only specific commands, or it can be used for module DAC parameter variation studies or temperature variation studies. Each device can be controlled manually, or the tests can be automated by the operator, without requiring a change of the source

¹In LabVIEW terminology, the GUI is referred to as the front panel.

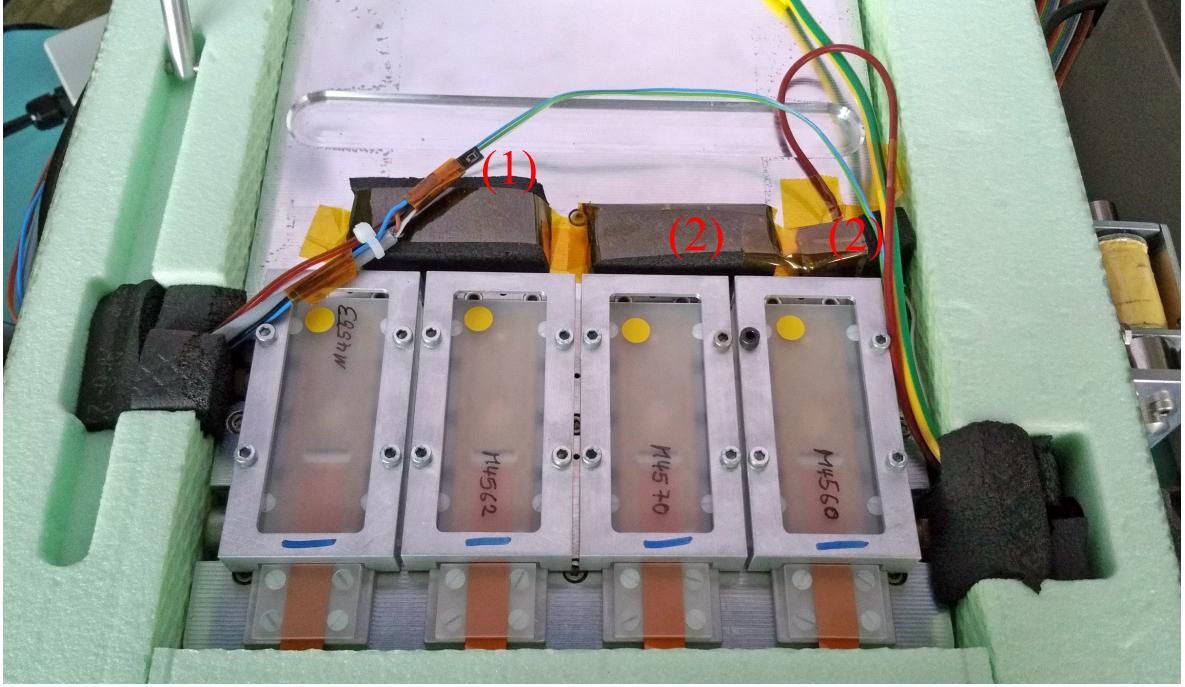


Figure 3.7.: Photograph of the cold box with opened lid. Up to four pixel modules can be tested in parallel. The module holders are clamped against the cooling plate with aluminum frames and are additionally sucked down by vacuum channels (not visible). A humidity sensor (1) and several temperature sensors (2) monitor the environmental conditions.

code. It is possible to test one to four modules by adding the module ID² and the position in the cold box to the second table. On the right side of the front panel, several parameters are shown over time (e.g., temperatures, humidity, Peltier controller voltage and current, sensor bias current). All values are logged in text files for later use. Multiple log windows in the lower part of the front panel show the status of the whole setup and the output from the pXar test routines.

An interlock system was implemented to prevent damage to the modules due to wrong operation parameters. The main risks are condensation of water on the modules while they are powered, and too large leakage currents that occur if a sensor is operated above its breakdown voltage or if it is exposed to light. Before any of the tests can be started, the operator has to acknowledge on the GUI that the system is in a safe state. In case the interlock is triggered, the low and high voltages of the pixel modules are switched off, and the whole system heats up to +17°C. The system is automatically interlocked if the dew point is less than 10 K below the temperature of the upper plate or if the box

²Each module was assigned an individual ID after assembly. The ID consists of the detector layer, in which the module is used, and a consecutive number. The modules produced at the KIT have numbers M4550 to M4958.

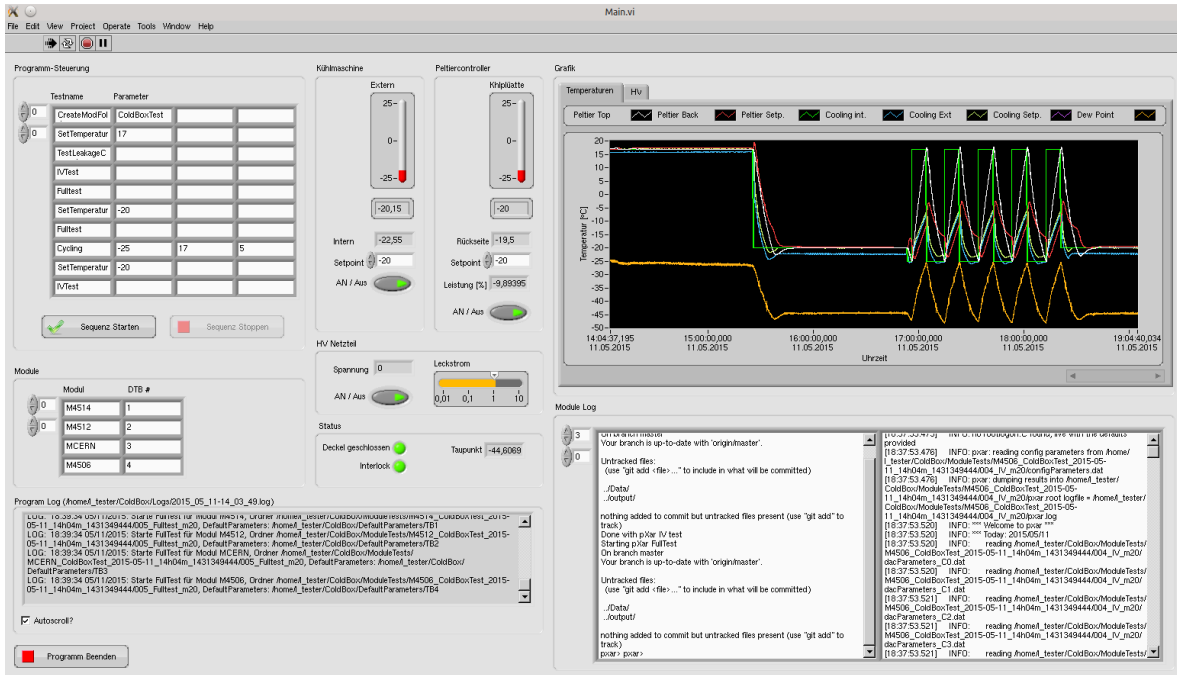


Figure 3.8.: User interface of the control software of the cold box setup. The test sequence (top left) is composed of individual commands and can be modified quickly. The current status of all devices is summarized (center) and shown over time (top right). The status log of the whole setup (bottom left) and the text output of the module test routines (bottom right) are shown.

is opened during operation. It is also interlocked if the leakage current of all modules together is above $100\mu\text{A}$. There is an additional check if the deviation between the redundant temperature sensors or the temperature difference between both sides of the Peltier elements is too large.

The program is multi-threaded and executes different tasks independently at the same time. It follows a Master/Slave design pattern [75]. Several threads control the instruments and acquire their sensor values, control the pXar software, monitor the interlock system, and log the data. The main thread collects data from all other threads and reacts on user inputs. The benefit of this implementation is that in case one of these processes crashes, the other processes can continue and bring the setup to a safe state. Another benefit is that it would be easy to replace any of the hardware, as only the code of the specific device has to be changed while the rest of the program is completely independent. Additionally, the pXar software is started as a command line process from within the LabVIEW program. Thus, it would be easy to adopt the cold box setup to a completely different test software suite, making it possible to use the setup for other future projects as well.

3.3.2. Test Procedure

The electrical tests and the test sequence for the qualification of the pixel modules in the cold box are described in the following sections. Because the design of the Phase-1 pixel modules has not changed compared to the Phase-0 pixel modules and the readout chip is an upgraded version of the original psi46V2 ROC, the tests were similar to the tests that had been performed during the construction of the original CMS pixel detector, which is described in reference [59].

Test Sequence

The Swiss consortium took a leading role in the implementation of the tests in the pXar software and every institute involved in the module qualification adopted the procedure with only minor modifications. All tests were done at the foreseen cooling loop temperature of -20°C . The modules were additionally tested at $+17^{\circ}\text{C}$ to obtain DAC parameters that were used in the X-Ray tests (Section 3.4). Figure 3.9 shows the measured cooling block temperature over time for a full qualification of four pixel modules in the test setup. The first full series of qualification tests was performed after the initial cool down to -20°C . When these tests were finished, the modules were thermally cycled between -25°C to $+17^{\circ}\text{C}$ for 10 times. All qualification tests were repeated to check for new failures. In the last step of the procedure, the pixel modules were warmed up to $+17^{\circ}\text{C}$, and all tests were performed for the third time. The complete qualification procedure required about 9 h. The thermal cycling contributed with about 160 minutes and each series of electrical tests contributed with about 120 minutes to the total test time. With up to four module tests running in parallel, up to eight modules could be tested per day. Below the individual electrical tests are described.

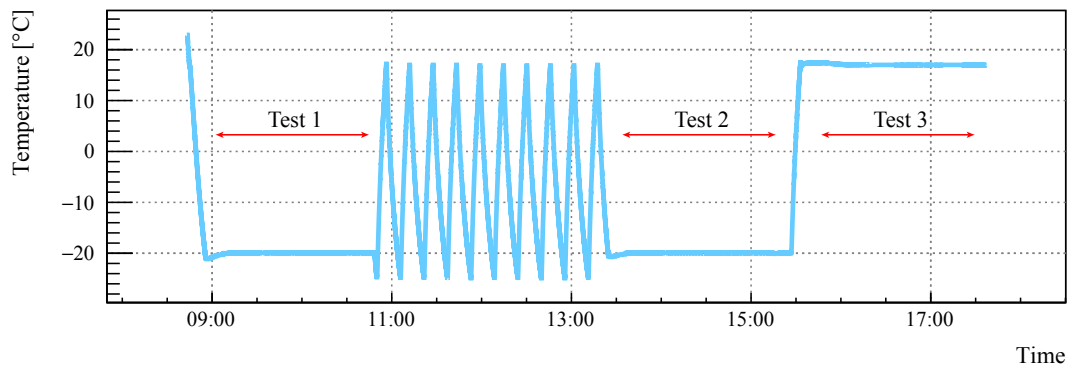


Figure 3.9.: Cooling block temperature profile of a complete test sequence. First, an electrical test is performed at -20°C . Modules undergo 10 active thermal cycles between -25°C to $+17^{\circ}\text{C}$ afterward. The electrical test is repeated at -20°C and $+17^{\circ}\text{C}$. The whole sequence takes about 9 hours.

Pretest

As a first step, it is verified that the communication with the readout chips can be established. This is done by programming the Vana DACs of all ROCs, which adjust the analog ROC currents. The analog output current of the DTB is monitored for changes at the same time. If a ROC cannot be programmed, the analog current does not change. Only if all ROCs pass this test, the procedure is continued. If not, the testing sequence is stopped completely, and the module must be manually examined to find the reason. In the next step, the Vana DAC of each readout chip is adjusted until the target current of 24 mA is reached.

All of the following tests make use of the chip internal charge injection mechanism. Thus, the timing of the calibration pulse has to be optimized. This is done by setting the CalDel DAC, which is used to shift the calibration pulse with respect to the clock signal, to a proper value. Because the analog part of the readout chip is operated with a clock of 40 MHz, the active time window corresponding to a trigger signal is 25 ns long. If the delay of the calibration pulse is not appropriately set, an injected signal is measured in the wrong clock cycle and is thus not triggered. A two-dimensional scan of CalDel vs. VThrComp (global ROC threshold) is performed, and at each step, 5 pulses are injected into a single pixel unit cell. All pulses are registered by the readout chip for a certain range of CalDel, as shown in Figure 3.10. The chip is flooded with noise hits at very low thresholds (large VThrComp values). Thus, injected pulses are not recognized anymore. A CalDel value in the center of the valid region (50 %-value) is chosen as the working point.

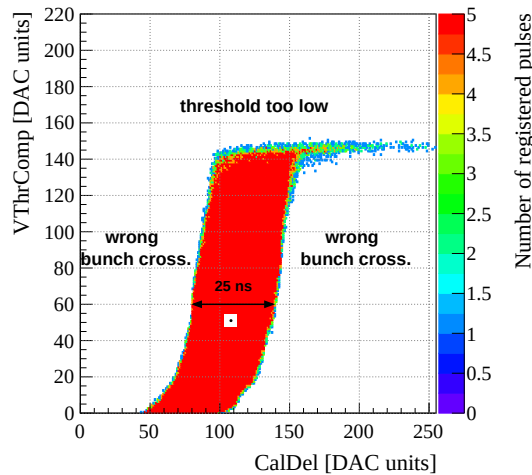


Figure 3.10.: Optimization of the calibration pulse time delay. A two-dimensional scan of CalDel (delay of the pulse) versus VThrComp (global ROC threshold) is performed. The number of registered hits is color-coded. Note that VThrComp is an inverted DAC, i.e., a low value corresponds to a large threshold. The optimized value is indicated.

PixelAlive Test

It may happen that single pixel unit cells in a readout chip do not send any signals, either because they were broken already on the silicon wafer or because they were damaged during assembly of the pixel module. The number of defective pixels was thus determined for each readout chip. In the so-called PixelAlive test, ten calibration pulses are injected in every pixel unit cell, and the number of registered hits is counted. Defective pixels show no hits at all. An example result is shown in Figure 3.11. The test is repeated with all pixels disabled to verify the functionality of the mask bit. If a hit signal is created by a masked pixel, the mask bit is defective. In a third step, the PixelAlive test is repeated with the additional requirement that the pixel address is decoded correctly, i.e., the position of the injected signal and the pixel address of the registered hit are correlated. Almost no defective pixels were observed during the module qualification because the ROCs had been tested on wafer level before assembly.

Problematic pixels are added to a list, which is used to determine the grade for each ROC. The criteria mentioned above apply, i.e., grade A for less than 1 % defective pixels, grade B for 1 % to 4 % defective pixels and grade C for more than 4 % defective pixels. The ROC is graded C as soon as a single pixel with a defective mask bit is found. The reason is that pixels with a large electrical noise can disturb the readout of the ROC. Therefore, it must be ensured that masking is possible in any case.

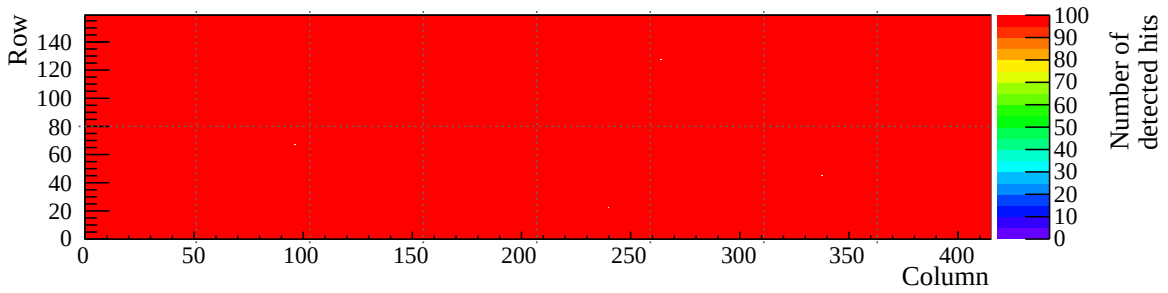


Figure 3.11.: Result of the PixelAlive test. The picture shows a schematic view of the pixel module, the 16 readout chips are indicated. The number of registered pulses is color-coded. Five defective pixels show no hits.

Bump Bond Test

The flip-chip assembly, which is used to connect the readout chips with the silicon sensor, is prone to errors. Sometimes a fraction of pixels is not properly connected to the silicon sensor. Such pixels show no anomalies in the PixelAlive test but generate no or only little signals in the detector. The bump bond test is used to find such pixels. In this test, the mechanism to inject calibration pulses capacitively into the sensor is used. Calibration pulses are injected into each pixel on the sensor, and it is checked whether the corresponding pixel unit cell registers a hit. If it does not register a hit, the bump bond connection is missing.

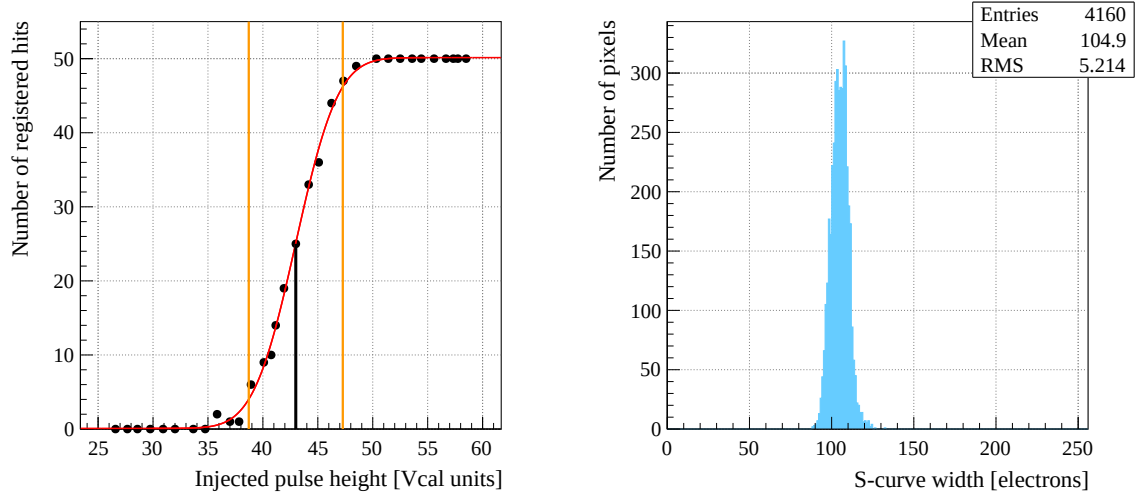
Different implementations of this test exist, because the flip-chip process differed in details among several production centers (used solder material, the height of the bump balls), and no test routine was found which could deliver valid results for all production centers. Below the implementation for the KIT modules is described [61].

In the first step, the sensitivity of the measurement is increased. Triggers are sent to the readout chips without injecting a calibration pulse. The signal threshold of all readout chips is reduced individually (i.e., the VthrComp DAC is increased by 5 units) until more than 5 noise hits are generated in the specific ROC. The lowest possible signal threshold of each ROC is used for further testing.

In the second step, 100 signals with the maximum pulse height (255 high range Vcal units) are injected into each pixel of the sensor, and the number of hits in the readout chip is counted. If a pixel registers less than 50 % of the injected signals, it is considered defective. This test is repeated for different values of CalDel because it has been observed that calibration pulses are injected at different locations of the readout chip with small time differences. This effect is taken into account by varying CalDel in steps of 10 DAC units from 80 to 200. If for any value of CalDel more than half of the injected pulses are detected, the bump bond connection is assumed to be functional. The number of pixels that have a missing or bad bump bond is counted and added to the total number of defective pixels for the grading.

S-Curves

The electronic noise of a ROC can be determined by the measurement of so-called S-curves. A zero suppression is implemented in every pixel unit cell. In an ideal case, every signal below the threshold would be ignored, while for every signal above the threshold a hit information would be created. In reality, the signal is smeared by electronic noise, and as a result, small signals can eventually pass the threshold or valid signals can be ignored. One method to measure S-curves is to inject calibration pulses with different charges, at a fixed threshold. At every pulse height step, the same number of pulses is injected, and the number of hits is counted. An example measurement is shown in Figure 3.12(a).



(a) S-curve of a single pixel. Orange lines indicate the width of the S-curve, which is a measure of the electronic noise. The black line indicates the 50 % value, which corresponds to the threshold.

(b) Histogram of the S-curve widths of all pixels of a readout chip, converted to electrons. A conversion factor of $45 \text{ e}^-/\text{Vcal}$ was used.

Figure 3.12.: Measurement of the electronic noise with so-called S-curves.

Under the assumption of Gaussian noise, the measured curve can be described by an error function:

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-\tau^2} d\tau \quad , \quad (3.1)$$

$$f(x) = p_0 \cdot \text{erf}((x - p_1)/p_2) + p_3 \quad . \quad (3.2)$$

The function $f(x)$ is fitted to the measured data. Parameter p_0 is a scaling factor and p_3 is an offset. Parameter p_2 corresponds to the width of this curve and is a measure of the electronic noise. The 50 % value (p_1) corresponds to the threshold. This method was used in the qualification procedure because it also allows the determination of the signal thresholds. An alternative way to measure the noise is to keep the injected pulse height constant and change the threshold instead. The measured curve can again be

described by an error function with a width corresponding to the electronic noise, but the 50 % value equals the height of the injected pulses.

The Vcal DAC of the psi46dig readout chip controls the pulse height of the injected calibration signals. Thus, the noise and the thresholds were obtained in Vcal units. One Vcal unit corresponds to a signal of about 45 electrons created in the sensor. The calibration factor was obtained from X-ray tests, which are described in Section 3.4.3. If the noise of a pixel is larger than 400 electrons or the fit of the S-curve failed, the pixel is added to the list of defective pixels. The typical noise measured in the cold box setup is in the order of 120 electrons at -20°C and 135 electrons at $+17^{\circ}\text{C}$. An example noise distribution for all pixels of one readout chip is shown in Figure 3.12(b). If the mean noise of the readout chip is above 200 electrons (400 electrons) it is graded B (C).

Threshold Optimization

It is desired to operate the pixel modules with a threshold that is uniform across all pixels. The threshold should be as low as possible to benefit from the charge sharing effect between neighboring pixels, which significantly improves the hit resolution. The minimum threshold at which the chip can be operated is limited by crosstalk and not by the pure electronic noise. Due to optimizations in the chip layout, the Phase-1 ROCs can be operated with a threshold as low as 1300 electrons, while for the Phase-0 detector the minimum possible threshold was about 2500 electrons. During the qualification procedure, the thresholds of the individual pixels were set to a target value of 35 Vcal units (about 1600 electrons). This procedure is called threshold trimming.

The readout chip has a global threshold for all pixels (set by the VthrComp DAC). Each pixel has four trim bits that reduce the global threshold, if enabled, to correct for variations between different pixels. The threshold reduction depends on the setting of the global Vtrim DAC. The optimization is performed in three steps:

1. Adjustment of VThrComp such that the pixel with the lowest threshold is at the target value.
2. All trim bits are enabled, and Vtrim is adjusted such that the pixel with the highest threshold is at the target value.
3. The trim bits of all other pixels are adjusted to obtain a uniform threshold distribution.

The adjustment is similar to the S-curve measurement. The Vcal DAC is kept at the target threshold value of 35 Vcal units. In the first step, VthrComp is varied. Calibration pulses are injected for each value. The value at which 50 % of the pulses are registered is the optimal setting. The procedure is repeated in step 2, but Vtrim is varied instead. The value of the trim bits is varied in step 3. Figure 3.13(a) shows the thresholds of all pixels of one module before and after the optimization. The width

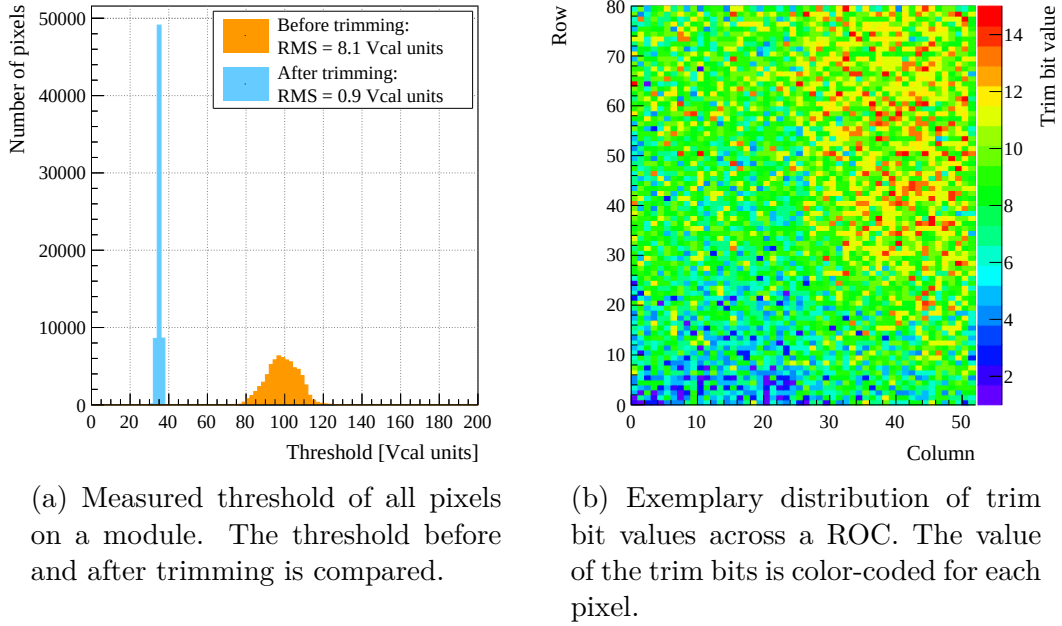


Figure 3.13.: Results of the threshold optimization.

of the threshold distribution changed from 8.1 Vcal units to 0.9 Vcal units after the trimming. Figure 3.13(b) shows an exemplary distribution of trim bit values across a single readout chip. A dependence of the trim bits on the location of the pixel in the readout chip is visible.

At every step, the actual threshold of each pixel is checked individually by a rough measurement of the S-curve. The trimming test takes about 40 minutes. Therefore, it was the most time-consuming subtest in the qualification procedure. The trim settings obtained were stored in the production database and were used for the detector operation in 2017.

Additionally, the functionality of each trim bit was tested. This was done by measuring the difference in threshold with enabled and disabled trim bit. If no significant difference was observed, a trim bit was not working and the pixel was added to the list of defective pixels.

Pulse Height Optimization

The analog signals are digitized by an 8-bit analog-to-digital converter (ADC) directly on the readout chip. The optimal energy resolution is obtained if the signals from the pixel cell exploit the full ADC range. For this reason, two global DACs, which adjust the dynamic range of the ADC, have been implemented in the readout chip. The PHScale DAC adjusts the gain, and the PHOffset DAC is used to add a constant

offset to the pulse height. Both DACs are optimized during the electrical test such that on the one hand even the lowest signals that pass the threshold are digitized with a pulse height greater than zero, and on the other hand, only signals above a target value saturate the ADC. Because the charge deposited in the sensor is about 20 000 electrons to 40 000 electrons and is divided between multiple pixels, a target saturation value of 31 500 electrons was chosen.

The optimization is done with two pixels of which one has a low and one has a high gain. These pixels have to be determined in the first step. Calibration pulses with the maximum possible height of 255 high range³ Vcal units (corresponding to 1785 low range Vcal units) are injected into every PUC to find the high gain pixel. The PHScale DAC is increased until the first pixel measures the maximum pulse height of 255 ADC units. The pixel corresponding to the 98-percentile is selected from the pulse height distribution to avoid running the optimization algorithm on anomalous pixels. The procedure for selecting the low gain pixel is similar. Pulses with a height of 60 low range Vcal units are injected, and the PHOffset DAC is increased until every pixel measures a pulse height greater than 10 ADC units. The pixel corresponding to the 2-percentile in the pulse height histogram is used for the optimization.

Once both pixels are determined, a two-dimensional scan over PHScale and PHOffset is performed. Example results for one readout chip are shown in Figure 3.14. Pulses are injected for each DAC combination, and the resulting pulse height is measured. In the high gain pixel, pulses are injected with 100 high range Vcal units, corresponding to a signal of about 31 500 electrons. For this pixel, the combinations of PHScale and PHOffset that result in a pulse height of 255 ADC units are the optimal settings. In the low gain pixel, pulses with the minimum Vcal that can still be detected are injected. The combinations of PHScale and PHOffset that result in a pulse height higher than a safety margin (20 ADC units) are the optimal settings for this pixel.

The optimized values that are finally obtained correspond to the overlap between the optimum value for both pixels. Values of ± 1 DAC unit around the optimal value are also considered to increase the stability of the algorithm. If multiple valid combinations are found, the one with the lowest value of PHOffset is preferred. If no combination is found, the ROC is graded C.

³When the CtrlReg register of the ROC is enabled, the charge corresponding to one Vcal unit is multiplied by a factor of seven. High range Vcal units refers to the state with the register switched on.

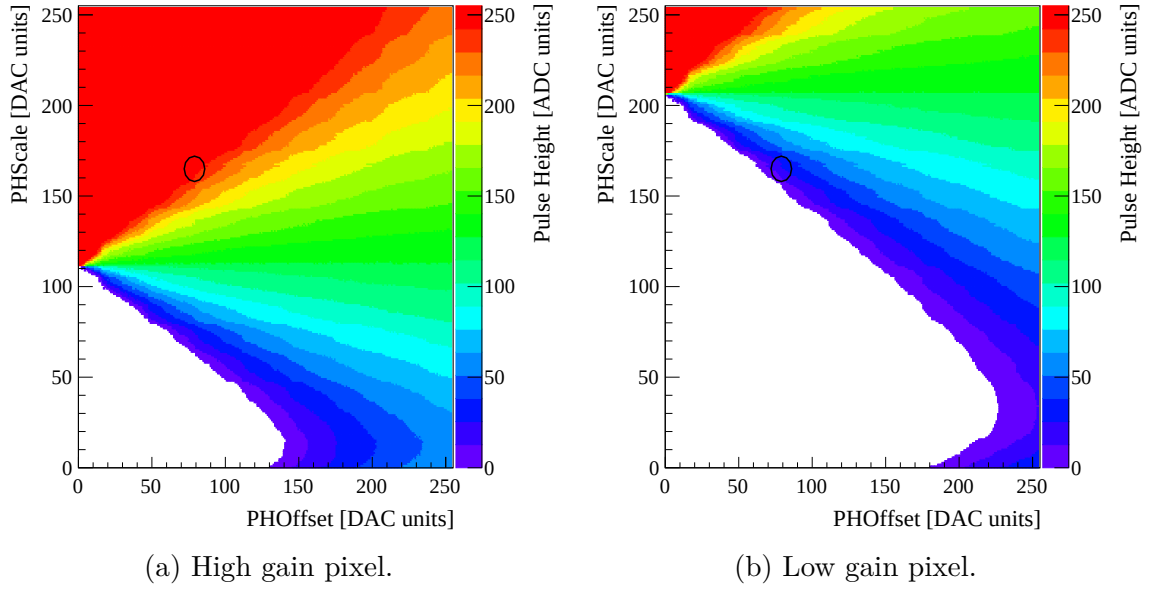


Figure 3.14.: Two-dimensional scans of PHScale vs. PHOffset. The measured pulse height is color-coded. Pulses with 100 high range Vcal units were injected in the high gain pixel. For the low gain pixel, Vcal was set to 60 low range Vcal units. The combination of settings, for which both pixels fulfill the requirements mentioned in the text, is indicated.

Pulse Height Calibration

There is no direct correlation between the measured pulse height (in ADC units) and the charge created in the sensor due to inter-pixel variations in gain. In order to conclude the physical signal height, the raw ADC values have to be converted into units of the Vcal DAC. Vcal units are the same for all pixels on a readout chip. The conversion requires an individual pulse height calibration for each pixel.

The ADC output is measured as a function of the injected calibration charge for 30 different Vcal settings for each pixel. An example measurement for two pixels of the same readout chip is shown in Figure 3.15. Three different functions are fitted to the measured curves:

1. a hyperbolic tangent function, as shown in Figure 3.15 (left):

$$PH_{\text{ADC}} = p_3 + p_2 \cdot \tanh(p_0 \cdot PH_{\text{Vcal}} - p_1) \quad , \quad (3.3)$$

where PH_{ADC} is the measured pulse height in ADC units, PH_{Vcal} is the injected pulse height in Vcal units, and p_0 , p_1 , p_2 , and p_3 are free parameters;

2. an error function (Equation 3.2), as shown in Figure 3.15 (right);
3. a linear function:

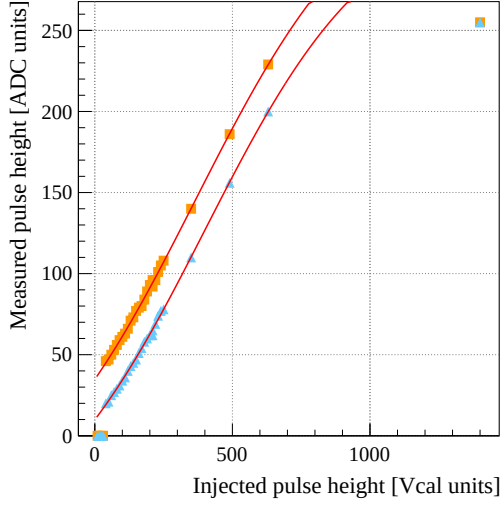
$$PH_{\text{ADC}} = p_{\text{gain}} \cdot PH_{\text{Vcal}} + p_{\text{pedestal}} \quad , \quad (3.4)$$

where p_{gain} and p_{pedestal} are free parameters.

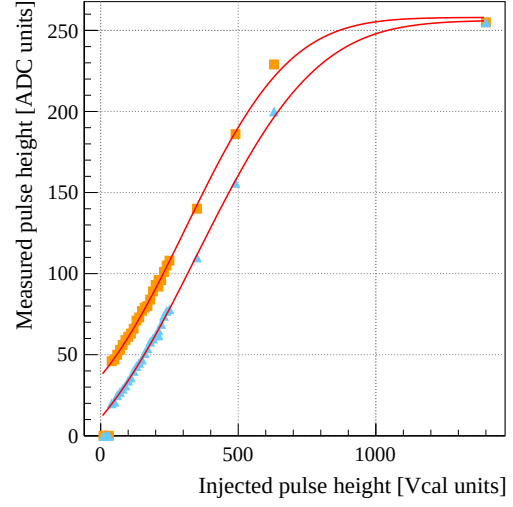
The parametrization allows a conversion from ADC units to Vcal units for any measured ADC value. The error function is used for the conversion because it describes the results accurately for both low and high Vcal values. The approximation with a hyperbolic tangent function is only valid for low ADC values but cannot describe the saturation. However, this function is used together with the linear function to find anomalously behaving pixels. Requirements are set on the largest and lowest allowed value of p_1 of the hyperbolic tangent function. This parameter is an indicator of the linearity of the pulse height response. The linear function is used to set requirements on the slope (p_{gain}) and the offset (p_{pedestal}) of the pulse height response. Pixels for which these values are not within the valid range are added to the list of defective pixels. The grading criteria are summarized in Table 3.1.

Further requirements are set on the relative width of the distribution of p_{gain} , which is defined as the ratio of standard deviation to mean value ($\sigma_{p_{\text{gain}}}/\mu_{p_{\text{gain}}}$), and the mean value of p_{pedestal} of all pixels. These requirements directly influence the ROC grading. They are also summarized in Table 3.1.

The fit results of all parameters are stored for every pixel in the production database. Furthermore, it is possible to convert from Vcal units to physical units with the Vcal X-ray calibration, which is described in Section 3.4.3.



(a) Data points fitted with hyperbolic tangent functions.



(b) Data points fitted with error functions.

Figure 3.15.: Pulse height calibration of two pixels (yellow and blue data points).

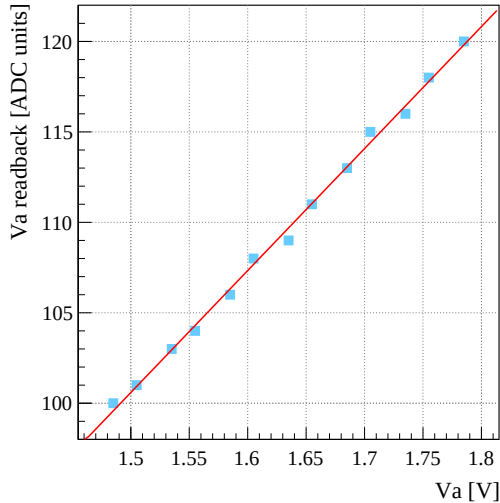
Table 3.1.: Grading criteria for the pulse height calibration. The criteria are applied per pixel or per ROC, as indicated.

Parameter	Allowed values
p_1 (per pixel)	$0 < p_1 < 7$
p_{gain} (per pixel)	$1 < p_{\text{gain}} < 5$
$\sigma_{p_{\text{gain}}}/\mu_{p_{\text{gain}}}$ (per ROC)	$< 10\%$ (grade A), or $< 20\%$ (grade B)
p_{pedestal} (per ROC)	$< 2500\text{ e}^-$ (grade A), or $< 5000\text{ e}^-$ (grade B)

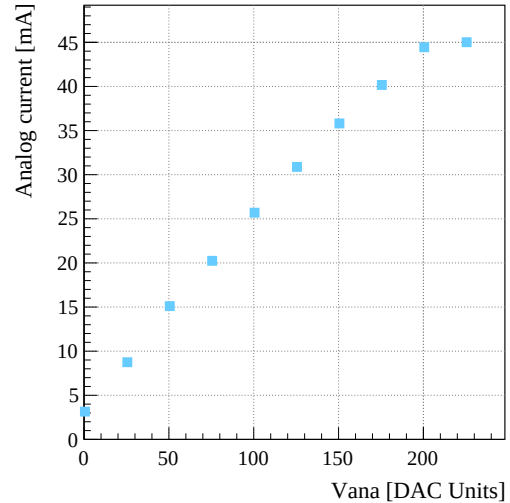
Readback Calibration

The Phase-1 readout chip can measure the actual analog and digital input voltages, V_a and V_d , as well as the analog current I_{ana} . A precise measurement of I_{ana} is important because the analog current changes with irradiation. The Vana DAC had to be optimized several times a year in the Phase-0 pixel detector already. With the conventional power system of the original pixel detector, it was possible to change the DAC settings and to monitor the power supply currents, because the module currents were equivalent to the power supply currents. However, this is not the case for the Phase-1 detector. The power supply currents also depend on the conversion ratio and the efficiency of the DC-DC converters, which may also change with irradiation. Direct measurements of voltages and currents with the readout chip simplify the Vana optimization and may also help troubleshooting power related problems.

The readback mechanism is calibrated by measuring the ADC output as a function of input voltage and input current. The output voltage of the testboard is varied for the calibration of the voltage readback, and the Vana DAC is varied for the calibration of the current readback. An example measurement is shown in Figure 3.16(a). The values of V_a , V_d , and I_{ana} measured by the testboard are used as the reference for the calibration. A linear model was fitted to the measured ADC output as a function of the input voltage or input current. The fit values were stored in the production database for later use. Since I_{ana} (measured by the testboard) and the readback value of the ROC are measured for different values of the Vana DAC in the calibration procedure, any conversion between these three parameters is possible. Figure 3.16(b) shows the dependence of the analog current on Vana.



(a) Calibration of the V_a readback.



(b) Dependence of I_{ana} on the Vana DAC setting.

Figure 3.16.: Results from the readback calibration of one readout chip.

Sensor Leakage Current

The silicon sensor is operated in reverse bias mode to increase the size of the charge carrier free depletion zone. A leakage current occurs due to electron-hole pairs that are generated by thermal excitation. Defects in the lattice can enhance the current, which are for example caused by impurities induced during the fabrication process. After irradiation, the leakage current is dominated by radiation-induced damage. Large leakage currents of unirradiated sensors are a sign of flaws. The leakage current was measured as a function of the bias voltage for every module during the qualification procedure.

Representative measurements for five pixel modules are shown in Figure 3.17. With increasing bias voltage the leakage current increases until the depletion voltage is reached. At this voltage, the bulk of the sensor is fully depleted. With a further increase of the voltage, the leakage current in a good sensor stays almost constant until the electric field is large enough to cause an avalanche breakdown. Operation above the breakdown voltage can damage the sensor and has to be avoided.

In the pixel detector, the sensors are operated in the plateau range with a voltage slightly larger than the depletion voltage. An initial bias voltage of 150 V was chosen. Sensors were graded A if the leakage current at 150 V was below 2 μA and were graded B if the leakage current was below 10 μA . If the leakage current was larger, the sensor was graded C. The ratio of the currents at 150 V and 100 V was required to be less than 2 to ensure that a plateau region exists.

An additional requirement was placed on the ratio of the leakage currents measured at $+17^\circ\text{C}$ and -20°C : $\frac{I_{150\text{V}}(17^\circ\text{C})}{I_{150\text{V}}(-20^\circ\text{C})} \geq 20$. This was motivated by the fact that bulk leakage currents, I_L , which are caused by thermally generated electron-hole-pairs, are strongly temperature dependent:

$$I_L(T) \propto T^2 e^{-\Delta E/2k_B T}, \quad (3.5)$$

where T denotes the absolute temperature in Kelvin, ΔE is the band gap energy of silicon (1.12 eV at room temperature), and k_B is the Boltzmann constant. According to Equation 3.5, the bulk leakage current doubles for $\Delta T \approx 7\text{ K}$. Thus, a factor of $\frac{I_{150\text{V}}(17^\circ\text{C})}{I_{150\text{V}}(-20^\circ\text{C})} \approx 30$ is expected. However, this is not the case for currents flowing across the sensor surface, which are less temperature dependent [76]. Surface currents may be generated, for example, by contaminants or scratches that occur in the manufacture of the sensors as well as in the handling and assembly of the pixel modules.

Sensors for which the leakage current did not scale with temperature as expected (a scaling factor of less than 20) were graded B. Although they have a more substantial amount of surface currents, they can still be used if the absolute leakage current criterion is not violated. After irradiation, the bulk leakage current increases by about three orders of magnitude, and the surface currents are no longer relevant.

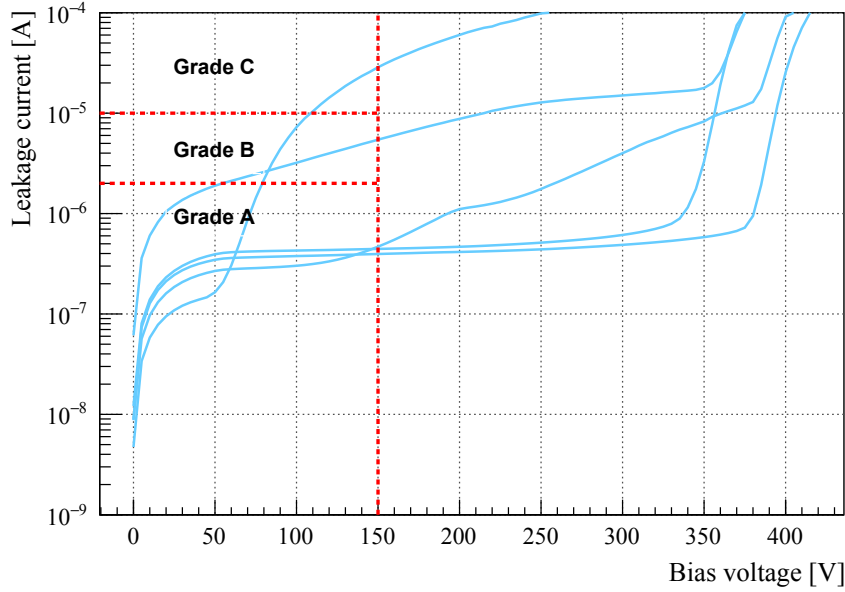


Figure 3.17.: Current-voltage characteristics (I-V curves) of five pixel module sensors, measured at $+17^\circ\text{C}$. The grading criteria for the absolute current are indicated. One of the shown sensors was graded B and one was graded C.

The results of the above tests are discussed in Section 3.5 together with the results from the X-ray setup, which is explained below.

3.4. X-Ray Tests

The pixel modules were tested in an X-ray setup to simulate the high particle fluence present in CMS. The advantage of X-ray tubes over radioactive sources is that they usually provide greater photon fluences and, more importantly, require fewer safety measures for daily laboratory use. The X-ray tube only generates radiation when actively used, while radioactive sources present a permanent hazard.

Photons are created by accelerating electrons and stopping them in a target material. An X-ray tube consists of a cathode and an anode in a vacuum chamber. A large voltage (several kV) is applied between the cathode and the anode. The cathode is heated to generate free electrons, which are then accelerated towards the anode in the electric field. The electrons interact with the anode material (a metal with a large atomic number, such as tungsten or gold) and their kinetic energy is converted into heat and high-energy photons. The photon energy spectrum consists of a continuous bremsstrahlung spectrum and sharp lines that are characteristic of the anode material. A spectrum of the tungsten anode used in the X-ray setup is shown in Figure 3.18 (left). Bremsstrahlung is caused by the deflection of electrons in the electric field of the nucleus.

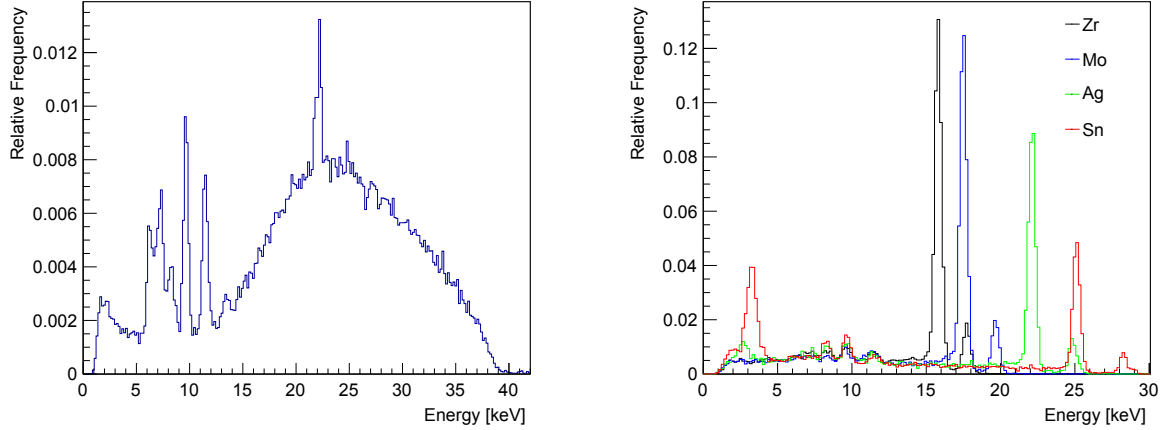


Figure 3.18.: Energy spectrum of the tungsten anode (left) and fluorescence spectra of four metals (right), measured in the X-ray setup. Modified from [7].

The characteristic lines are caused by ionization or excitation of atoms in the target material. When an atom is ionized, the empty electron orbital is filled by an electron from a higher energy orbital. In this transition, a photon with a specific energy is emitted, which corresponds to the energy difference between the two orbitals.

Two types of X-ray tests were performed during the mass production of pixel modules. The modules were illuminated with the direct beam of the X-ray tube, which offers a large photon fluence. Furthermore, they were illuminated with K_α -photons from metallic targets for an energy calibration. In this configuration, different targets were placed in the primary beam of the X-ray tube. The primary X-rays ionize the atoms of the target material but do not produce bremsstrahlung. The fluorescence photon spectrum thus consists only of the characteristic lines of known energies. Examples of spectra of four different metals are shown in Figure 3.18 (right). The dominant peaks are caused by K_α -photons. The K_β -peaks are also visible, but their intensities are about one order of magnitude lower.

The photons are absorbed in the silicon sensor by the photoelectric effect. As a result, the whole energy is deposited in a single pixel. This feature was used to calibrate the on-chip charge injection mechanism, allowing to convert Vcal units to physical units.

3.4.1. The X-Ray Setup

A test setup comprising a didactic X-ray tube has been developed for the qualification of pixel modules. Figure 3.19 shows a photograph of this setup. The photons are produced in an X-ray machine made by LD Didactic [77]. This device is designed for educational purposes in schools and universities. The main advantage compared to X-ray tubes used in industry is the low price (approximately 12 000 €). Also, no additional radioactive safety measures are required. This comes at the expense of reduced photon rates. However, it has been verified that the rates are sufficient to test pixel modules for layers 2-4 of the Phase-1 pixel detector. The X-ray tube uses a tungsten anode to generate photons with energies up to 35 keV at a maximum tube current of 1 mA.

The pixel modules are placed in a separated, darkened experimental chamber. Up to two modules are screwed to an aluminum cooling block. The mechanism is the same as in the cold box, i.e., the module holder is pressed against the cooling block by an aluminum holder, which is screwed to the block. The aluminum block has integrated cooling channels. A cooling circulator (Huber ministat 230 [78]) with a water-glycol bath is used to keep the devices under test at a constant temperature. It can be set to any value between -20°C to $+25^{\circ}\text{C}$. During the qualification procedure, all pixel modules were tested at $+17^{\circ}\text{C}$.

The experimental chamber is flushed with dry air to avoid condensation. The temperature of the cooling block is measured with a Pt-100 type RTD, which is glued to the backside of the cooling block. The air temperature in the test chamber is also measured with such a sensor. Both sensors are connected to a National Instruments NI6008 DAQ card, which is read out by a computer. The relative humidity inside the box is measured with a Honeywell HIH-4000-001 humidity sensor, which is connected to the same DAQ card.

The pixel modules are either illuminated with primary photons in the direct beam of the tube (Figure 3.20(a)), or they are illuminated with fluorescence photons (Figure 3.20(b)). In the fluorescence configuration, a collimator is used to reduce the size of the beam spot and thus to reduce stray radiation.

The hit rate R_H is a measure of the number of pixel hits per second and is normalized to the active area A :

$$R_H = \frac{N_{\text{Hits}}}{t_{\text{active}} \cdot A} \quad . \quad (3.6)$$

Nearly uniform illumination of two modules with hit rates up to 300 MHz cm^{-2} is possible in the direct beam position. In contrast, the hit rate in the fluorescence position is about two to three orders of magnitude lower, depending on the target.

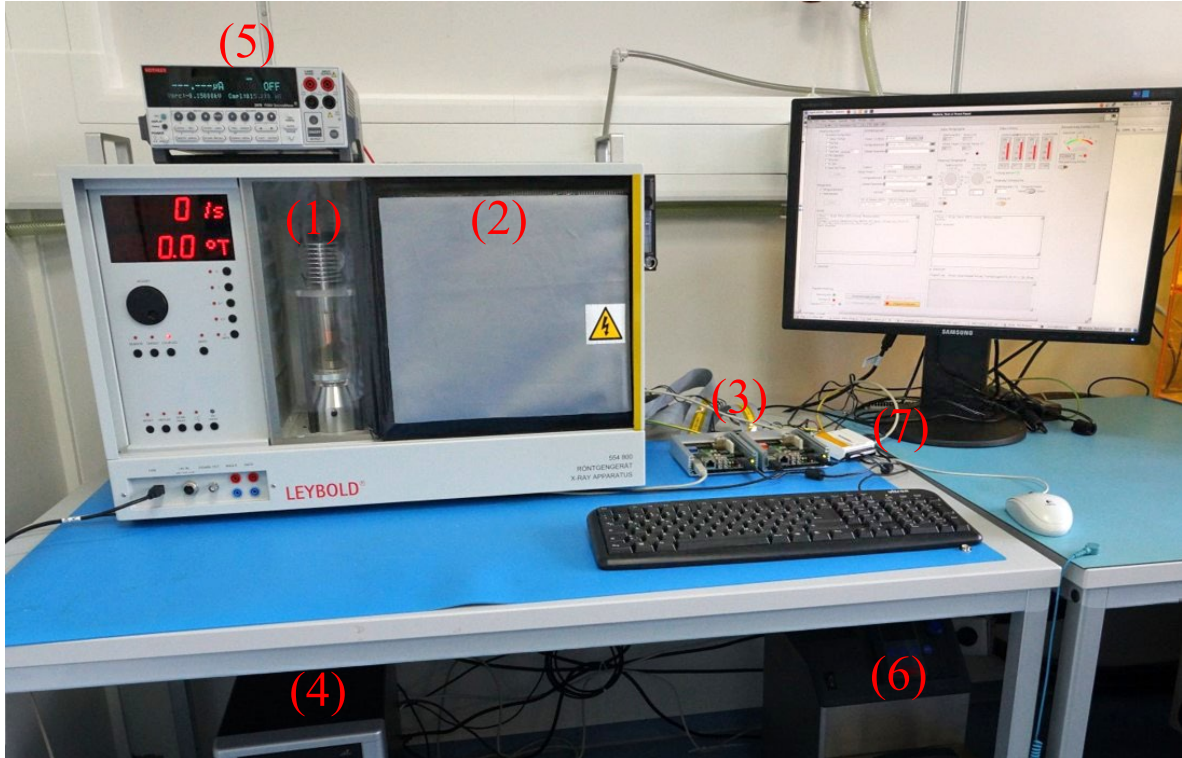
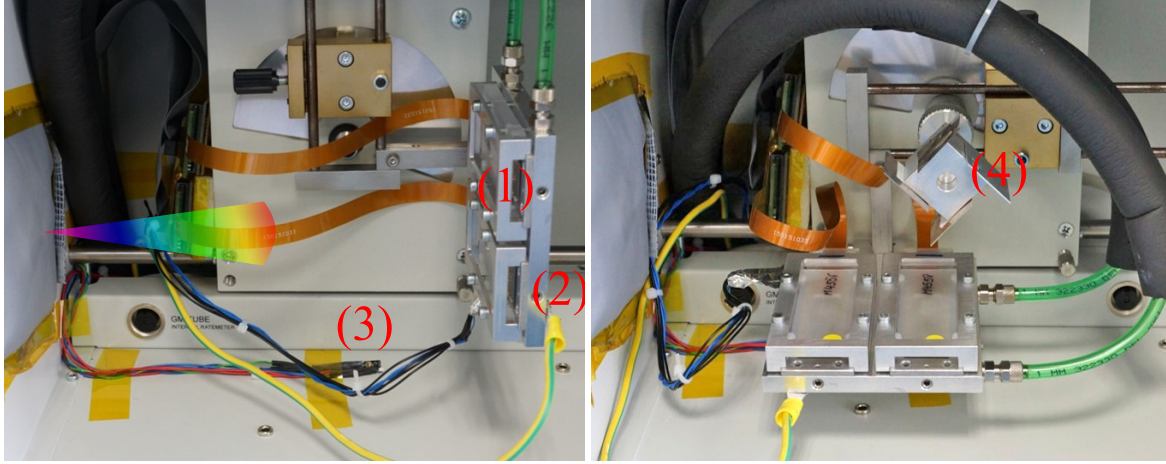


Figure 3.19.: Photograph of the X-ray setup. The X-ray tube (1) is separated from the measurement chamber (2). Two pixel modules are read out with DTBs (3) and a computer (4). The sensors are biased with a high-voltage power supply (5). A liquid chiller (6) is used to cool the modules. A DAQ card (7) with attached sensors measures temperatures and humidities.



(a) Direct beam configuration.

(b) Fluorescence configuration.

Figure 3.20.: Photographs of the measurement chamber, showing both configurations. The primary beam (indicated in rainbow colors) enters the chamber from the left side. The pictures show two pixel modules (1), the cooling block (2), environmental sensors (3), and the target holder (4).

Four different targets can be glued to a target holder (Figure 3.20(b)). The angle between adjacent targets is 90° . The module holder and the target holder are attached to a goniometer with two axes, which can be rotated by motors independently.

The sensor bias voltage is provided by a Keithley 2410 source meter. The pixel modules are operated at 150 V. They are read out by two digital testboards, which are placed outside the X-ray device to protect them from radiation. A computer with Ubuntu Linux operating system is used to run the pXar software.

A software for the automated control of the setup was developed with LabVIEW. This software acquires and logs all device data, including sensor leakage current, temperatures, and humidity. The front panel is shown in Figure 3.21. An interlock system has been implemented to stop running tests and to turn off the sensor bias voltage if the user opens the X-ray device or the cooling block temperature is less than 5 K above the dew point. It was desirable to automate the test sequence as much as possible. After placing the pixel modules in the setup, the user only has to enter their IDs, the folder where the correct module configurations are stored, and the test type. The LabVIEW VI controls the X-ray tube, the power supply, and runs the pXar test sequences. All results are automatically copied to a computer running MoReWeb, the same software that has been used to analyze data from the cold box setup.

3. Qualification of Pixel Modules

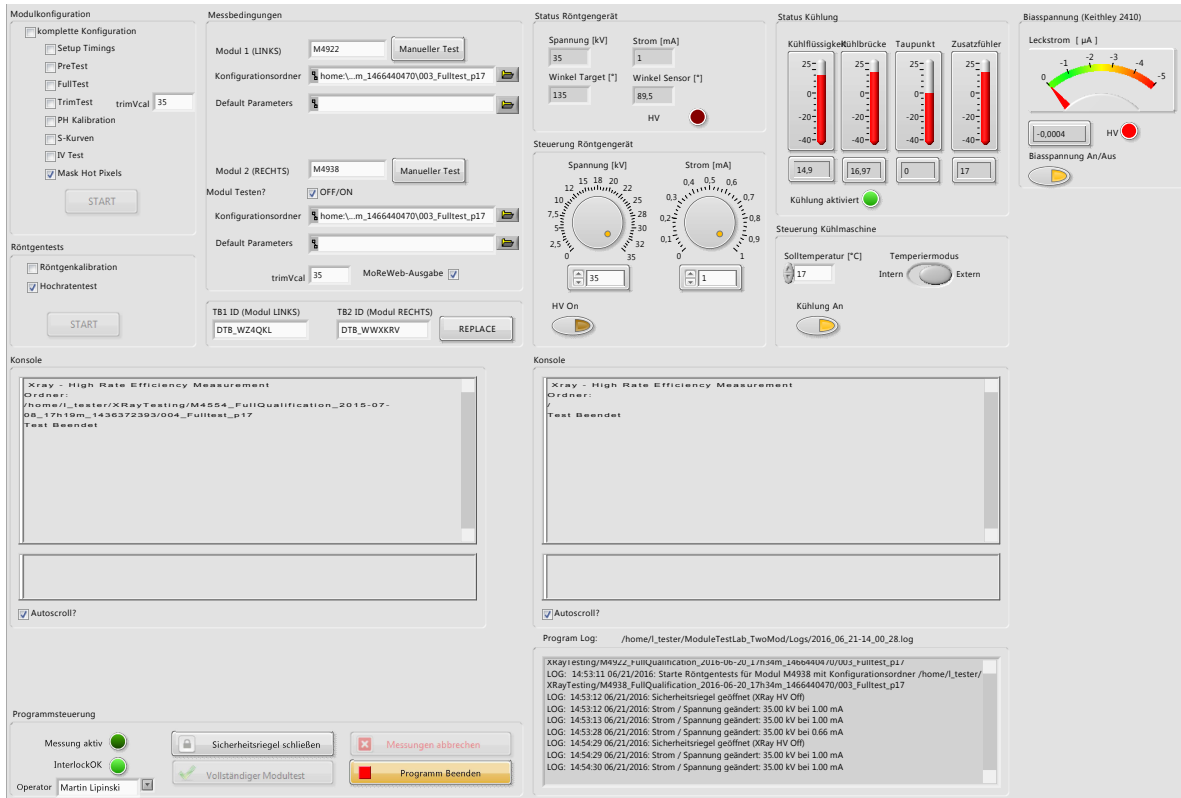


Figure 3.21.: User interface of the control software of the X-ray setup. The IDs of the pixel modules under test and the DAC configuration files have to be entered in the top left. The devices in the setup can also be controlled manually, and their status is summarized (top right). The text output of the module test routines and the status log of the setup are shown in the lower part of the GUI.

The target holder is rotated during the X-ray calibration automatically. However, the target holder and the collimator must be removed manually for the high rate tests. The full test sequence requires about two hours and a few additional minutes for the handling of the modules. In this setup, two pixel modules could be tested at the same time. Thus, six or eight pixel modules could be tested usually by a single person per day.

3.4.2. High Rate Test

The high rate test consisted of several subtests that were executed in a defined order. The complete test sequence was implemented in the LabVIEW control software, which was used to configure and start the individual test routines of the pXar software. Optimized DAC parameters were used to operate the pixel modules. They had been obtained during the electrical qualification at +17 °C in the cold box. All tests in the

X-ray setup were performed only at a cooling block temperature of $+17^{\circ}\text{C}$, but not at the detector operating temperature of -20°C . This was done for reasons of time-saving, as it eliminated the need to cool down and warm up the setup. It had been verified that important parameters like the efficiency do not depend on temperature.

The expected mean hit rates in the pixel detector, at the design instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, are 30 MHz cm^{-2} , 50 MHz cm^{-2} , and 120 MHz cm^{-2} for pixel modules in layer 4, layer 3, and layer 2, respectively. The modules were mainly tested at 50 MHz cm^{-2} and 150 MHz cm^{-2} in the qualification procedure. The hit rate was set by adjusting the X-ray tube current. For layer 3 and layer 4 modules this hit rates were much larger than the expected values. The reason to test at such high rates was that in this way it could be assumed that modules which pass the X-ray qualification will work in the detector without restrictions. It also allowed a standardized testing sequence for all module production centers, as modules for layers 2 to 4 were tested under the same conditions.

The subtests were performed in the following order:

1. Re-trimming of hot pixels
2. High rate data taking at two different hit rates
3. Noise measurement with S-curves under high hit rates
4. Measurement of the hit detection efficiency

1. Re-Trimming of hot Pixels

A few pixels produced noise hits in the X-ray tests when the pixel modules were operated with the trim parameters obtained in the cold box tests. This was because the threshold trimming was performed with a low chip activity. The large hit rates in the X-ray tests lead to increased crosstalk between pixels. Furthermore, it was observed that the noise in the pixel modules increased when the high voltage of the X-ray tube was turned on, even if the tube current was set to zero. Since noise hits can reduce hit detection efficiency and spoil results of uniformity tests and energy calibration, the first procedure of the X-ray qualification was the suppression of so-called hot (noisy) pixels. This was achieved by increasing the threshold or masking the affected pixels. It was observed that some pixels became noisy as soon as there was any activity in the readout chip, while other pixels were only affected at large hit rates. The test was thus repeated at low and high X-ray tube currents.

In a first step, the modules are illuminated at rates of about 200 kHz cm^{-2} for 5 s. Triggers are sent at a frequency of 100 kHz, and the number of registered hits is counted. If a single pixel has more than 7 hits in 5 s, it is regarded noisy. This threshold corresponds to a hit rate of about 3.8 MHz cm^{-2} for a specific pixel. The hit rate

is calculated with Equation 3.6 and the active time t_a , which depends on the trigger frequency f_{tr} , the trigger window width (25 ns), and the measurement time t_{meas} :

$$t_a = f_{tr} \cdot 25 \text{ ns} \cdot t_{meas} \quad , \quad (3.7)$$

$$R_H = \frac{N_{Hits}}{f_{tr} \cdot 25 \text{ ns} \cdot t_{meas} \cdot A} \quad . \quad (3.8)$$

The active area of a single pixel is 0.015 mm^2 . Pixels at the corners of a readout chip have twice this size, and the four edge pixels have four times this size. These pixels must be larger in order to compensate for gaps at the junction of two ROCs. For the corner pixels and the edge pixels, 7 hits in 5 s correspond to hit rates of 1.9 MHz cm^{-2} and 0.95 MHz cm^{-2} , respectively.

If a pixel has more hits than the cut value, its threshold is increased. This is done by changing the DAC value of the trim bit by one unit. The data taking is repeated, and the threshold of the pixel is increased further if the number of registered hits is still above the cut value. This procedure is repeated until no noisy pixels are left, or the trim value of these pixels is at the maximum. Pixels that are still noisy with the maximum trim value are masked, meaning they will not produce any hits at all.

The mentioned procedure is repeated with a larger X-ray tube current, which corresponds to a hit rate of about 150 MHz cm^{-2} . The threshold value is set to 200 hits in 1 s, corresponding to about 533 MHz cm^{-2} . The signal threshold of pixels with more hits than this value is increased or the pixels are finally masked. Typically, less than 5 pixels per module are found to be noisy.

2. High Rate Data Taking

In the following step, the pixel modules are illuminated with X-rays and read out for 100 s. Random triggers are sent with a constant trigger rate of 100 kHz. Two measurements are performed with different X-ray tube currents (0.22 mA and 0.88 mA), which correspond to hit rates of about 50 MHz cm^{-2} and 150 MHz cm^{-2} . A hit map of a pixel module (a schematic view of the module with the number of hits color-coded for each pixel) is shown in Figure 3.22. It is the result of the test at 150 MHz cm^{-2} . The hit rate of individual pixels varies with the position on the module, because X-ray photons are not only absorbed in the sensor, but also in components on the PCB (which are visible in Figure 3.2).

Several variables have been defined to grade the modules based on this data. The number of pixels without any hits is extracted from the map. The reason for pixels not having any hits can be a defect pixel cell in the readout chip or a missing bump bond connection between ROC and sensor. The test is used as a cross-check for the electrical

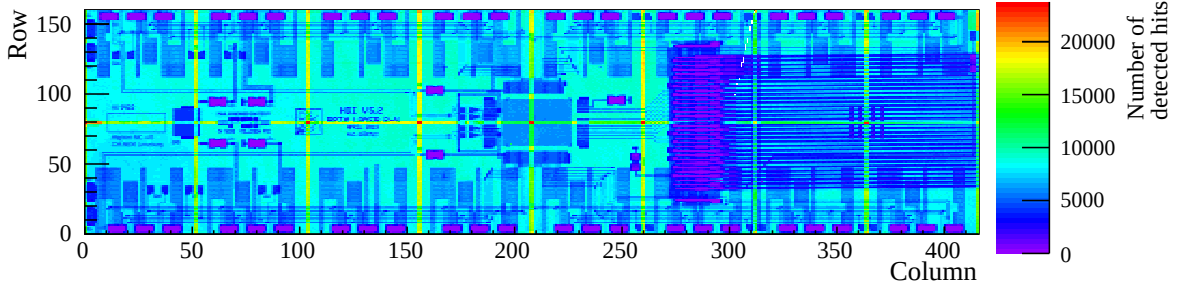


Figure 3.22.: Hit map of a pixel module, recorded in 100 s at a hit rate of 150 MHz cm^{-2} . The number of hits is color-coded for each pixel. Several pixels with no hits are visible on the third ROC from the top right.

test in the cold box because it is possible that the number of defect bump bonds is not determined properly from tests with calibration pulses. The standard grading criteria for defective pixels are applied, i.e., a readout chip could only be graded A (or B) if the number of dead pixels is below 1 % (4 %).

The tests are also used to validate that the rate of detected hits per column is uniform in time and that the rate scales correctly with the X-ray current. Any non-uniformity may be an indicator for severe problems in the readout chip. It is not possible to correct for this effect in the pixel detector. Thus, pixel modules with even a single readout chip with uniformity problems are graded C and cannot be used for the detector. The column uniformity U is defined as:

$$U = \frac{N_{150}}{N_{50}} \cdot \frac{50}{150} \quad , \quad (3.9)$$

where N_{150} corresponds to the sum of hits of all pixels in a column at a hit rate of 150 MHz cm^{-2} and N_{50} corresponds to the sum of hits at 50 MHz cm^{-2} . This variable depends only on the relative rates and not on the geometric location of the column. A value of $U = 1$ is expected because the number of hits in the chip is directly correlated with the X-ray hit rate. An example measurement of a ROC that failed this test is shown in Figure 3.23(a). If a readout chip has any column with a factor outside the range of 0.8 to 1.5, it is graded C. This test proved to be particularly sensitive to pixels that are noisy only in one of the two measurements (usually the measurement at large hit rates). As a result, the module could be erroneously rejected, because individual problematic pixels can be masked without influencing the overall performance of the module. Thus, if the non-uniformity is caused by a single pronounced pixel, this pixel is masked, and the module is retested.

The number of hits in every column is also evaluated over time to detect so-called column freezing, a feature that was present in an earlier version of the readout chip.

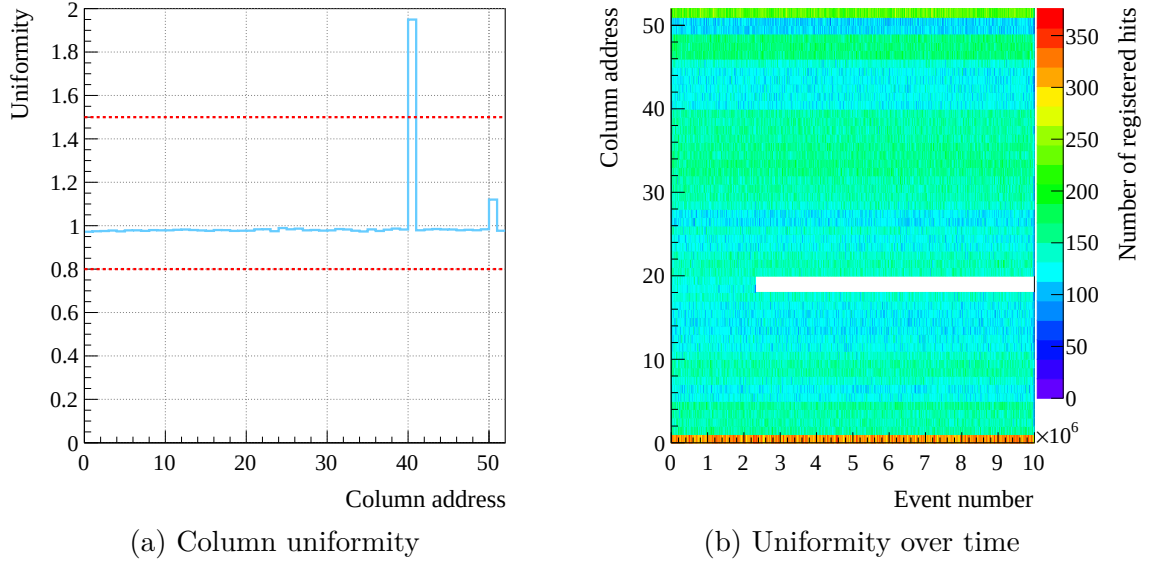


Figure 3.23.: Results from two modules that failed the readout uniformity tests. Left: histogram of the uniformity variables of all columns of module M4950 ROC 13. Two columns show a clear deviation from the expected value. The grading cuts (red dashed lines) are indicated. Right: number of hits per event (color-coded), shown versus the event number for all columns of module M4907 ROC 1. After about two million triggers column 18 and 19 stop giving hits.

Due to a bug in the chip, it was possible that single double columns no longer produced valid hits. Although this bug was fixed in the final version of the readout chip, every module was still tested for this effect. If in one of the measurements a double column stopped giving hits, the ROC was graded C. Three such cases were found. An example is shown in Figure 3.23(b).

The high rate data taking test is also sensitive to invalid data produced by the pixel modules. If the event information is not encoded in the correct format, the testboard cannot correctly decode it. Typical errors in the data stream are missing event end markers and missing ROC headers or trailers. Certain sanity checks are implemented in the firmware of the DTB to find flawed events. More details can be found in [42]. Modules with many encoding errors were investigated manually. Often the errors were caused by wrong ROC or TBM timings, which could sometimes be fixed by running a PreTest (Section 3.3.2) or by manually adjusting the DAC settings to known good values. If the readout errors could be fixed, the module was retested. Eight modules were found where the encoding errors could be fixed by increasing the digital current of an individual ROC with the Vdig DAC. A larger Vdig increases the speed of parts of the digital logic at the cost of an increased power consumption. If Vdig had to be increased by less than three DAC units, a module was still considered good. However, it was preferred to use such modules only as spares. In the Phase-0 detector, Vdig had never been changed from the default value.

3. High Rate S-curve Measurement

The electronic noise is measured while the pixel modules are illuminated with X-rays at a rate of 100 MHz cm^{-2} . S-curves are measured for each pixel by injecting calibration pulses. The calibration pulse height (Vcal DAC) is varied while the signal threshold is held constant. This procedure is the same that is used in the electrical tests (Section 3.3.2). At each step, 25 pulses per pixel are injected, and the number of registered events is counted.

The large activity in the readout chip under X-rays resulted in an increased noise of about 10%, compared to the qualification in the cold box. Furthermore, the signal threshold of the readout chips increased by about 250 electrons although the same DAC settings were used in both setups. Both effects are demonstrated in Figure 3.24. Readout chips were graded A or B if the mean noise was below 300 or 400 electrons, respectively. If the mean noise was above 400 electrons, the ROC was graded C. Individual pixels that had a noise above 400 electrons were added to the list of defective pixels.

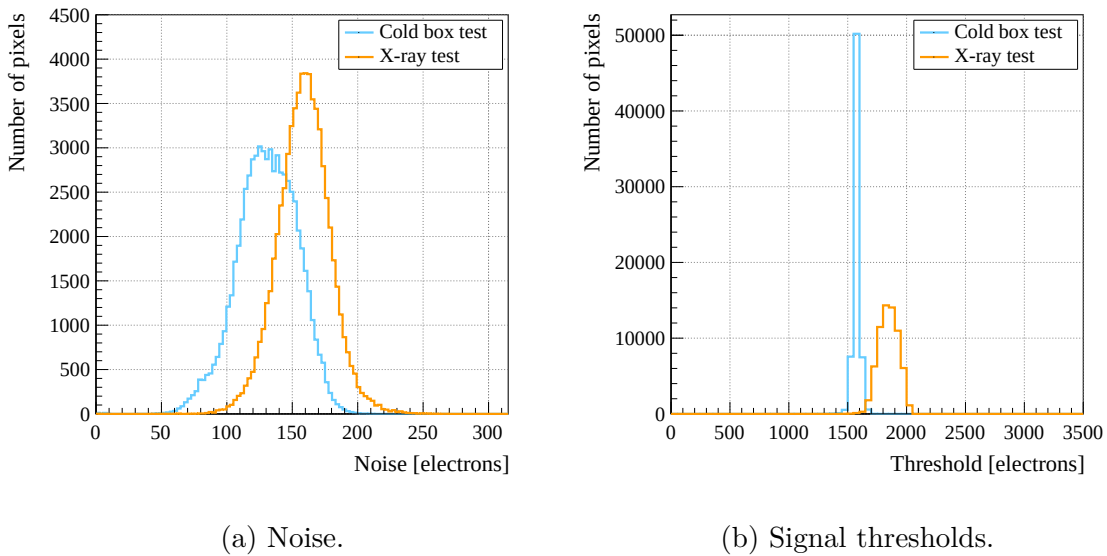


Figure 3.24.: Comparison of the noise and the signal thresholds between the measurement in the cold box (blue) and the X-ray setup (orange). The results for all pixels of one module are shown.

4. Efficiency Measurement

One of the main reasons to upgrade the CMS pixel detector was that the dynamic inefficiencies increased when the instantaneous luminosity was raised. These inefficiencies were mainly caused by overflowing buffers in the readout chip. Therefore, the last

step of the high rate qualification is the measurement of the hit detection efficiency. This test is used to verify that a module can operate at high luminosities without a performance degradation. It should be noted that efficiency measurements with X-rays cannot be used to conclude the real efficiency of the pixel detector in CMS. Photons hit only single pixels, while particles in CMS usually create clusters of several pixels⁴. The readout chip has more data buffers than timestamp buffers. Thus, the inefficiencies in the X-ray tests are produced mainly by overflowing timestamp buffers, while the data buffers are never entirely saturated.

In this test, calibration pulses are injected while the module is illuminated with X-rays. The X-ray background creates a lot of activity in the readout chip and fills the time stamp buffers with random data. Because the pixel address and the timing of the calibration pulses are known, the hit detection efficiency can be calculated as the ratio of registered hits N_{reg} to injected signals N_{inj} :

$$\epsilon = \frac{N_{\text{reg}}}{N_{\text{inj}}} \quad . \quad (3.10)$$

The statistical uncertainty of the efficiency is calculated as follows [79]:

$$\sigma_{\epsilon} = \sqrt{\frac{\epsilon(1 - \epsilon)}{N_{\text{inj}}}} \quad . \quad (3.11)$$

The efficiency measurement is divided into two parts. As a first step, the time delay setting of the calibration pulse (CalDel DAC) has to be adjusted. This DAC was optimized during the electrical qualification for pulses close to the threshold value of 35 Vcal units. However, a charge of 200 Vcal units is injected in the high rate test to avoid losing hits due to electronic noise. The effect of time-walk becomes relevant, which may cause pulses to be registered in the wrong bunch crossing. This would reduce the overall efficiency⁵. To obtain a large efficiency, the CalDel DAC is varied. A fixed number of calibration pulses is injected at every step, and the efficiency is measured. The module is illuminated at the same time with X-rays at a hit rate of 50 MHz cm^{-2} to simulate a moderate activity. The CalDel value that maximizes the efficiency of the readout chip is chosen.

In the next step, the module is illuminated with photons at hit rates of 50 MHz cm^{-2} , 100 MHz cm^{-2} , 150 MHz cm^{-2} , and 200 MHz cm^{-2} . At each hit rate, 50 calibration pulses are injected into every pixel. The efficiency is calculated per pixel with Equation 3.10. Furthermore, the average efficiency of all pixels in the same double column

⁴The mean cluster size depends on η and the radius. It varies between 2 pixels (FPix) to 5 pixels (BPix layer 1) [23].

⁵Time walk describes the effect that the time at which a pulse crosses an absolute threshold depends on the height of the signal. A larger signal with the same rise time exceeds the absolute threshold earlier.

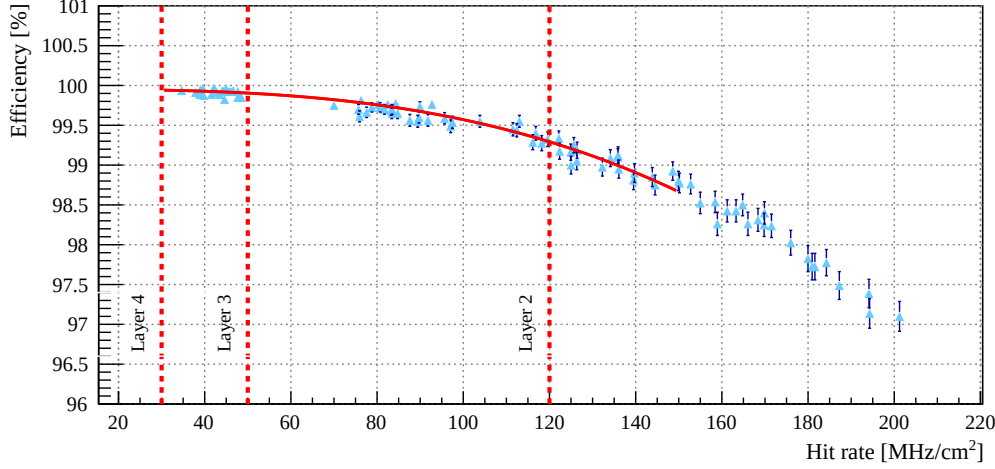


Figure 3.25.: Efficiency of a psi46digV2 ROC vs. hit rate, measured with four different X-ray tube currents. Each data point corresponds to the efficiency of one double column. Values are interpolated (solid red line) to extract the efficiencies at 50 MHz cm^{-2} and 120 MHz cm^{-2} . The dashed lines indicate the expected hit rates for pixel modules in BPix layers 2-4 at an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$.

is calculated. This is motivated by the fact that all pixels in a double column share the same buffers. The inefficiency of individual pixels depends on the total activity in the double column.

The hit rate of the X-ray background is calculated with Equation 3.8. Unlike the calibration pulses, the X-ray background rate is not affected by the inefficiency. The reason is that mainly the timestamp buffers overflow in X-ray tests, while the hit buffers can still be filled. In contrast to injected pulses, a mismatching between the timestamp and the pixel hits cannot be detected for background hits, because random triggers are used. The background hit rate depends on the geometric location of the respective readout chip in the X-ray beam and also on the location of the column within the module. The hit rate is also calculated per column to take this effect into account.

Figure 3.25 shows the measured efficiency versus hit rate for one readout chip from a production module. Each data point corresponds to one double column. The dashed lines correspond to the expected hit rates for modules in layers 2 to 4. The efficiencies are interpolated to 50 MHz cm^{-2} and 120 MHz cm^{-2} for the grading. A readout chip was graded A if the interpolated efficiency was above 98% at both hit rates, graded B if the efficiency was above 95%, or graded C if the efficiency was lower. Typical efficiencies were 99.8% at 50 MHz cm^{-2} and 99.2% at 120 MHz cm^{-2} .

Additionally, the number of pixels with a low efficiency is counted and added to the number of defective pixels. A pixel is considered defective if the efficiency is either lower than 50% or if the efficiency is more than ten standard deviations away from the mean value of all pixels.

It was observed that in some ROCs the efficiency of individual double columns was decreased, and the effect became more apparent at larger X-ray hit rates. An example is shown in Figure 3.26. Tests at PSI revealed that in the affected double columns at least one buffer cell was broken. When data is written to the buffer, all hits in cells behind the defective cell are lost. This effect is only visible at large hit rates, depending on the position of the defective cell in the buffer, because the data buffers are filled sequentially. The overall efficiency of the chip can still be large enough to pass the grading criteria if only one double column is affected. Such a module could in principle be used for the detector because less than 4 % of pixels are considered defective⁶.

However, a special grade called C* was assigned to the modules with a low-efficiency double column to separate them from modules with more severe errors. It was foreseen to install C* modules in the detector only in case not enough grade A/B modules were produced. This was not the case in the end, and no grade C* module was installed in the detector.

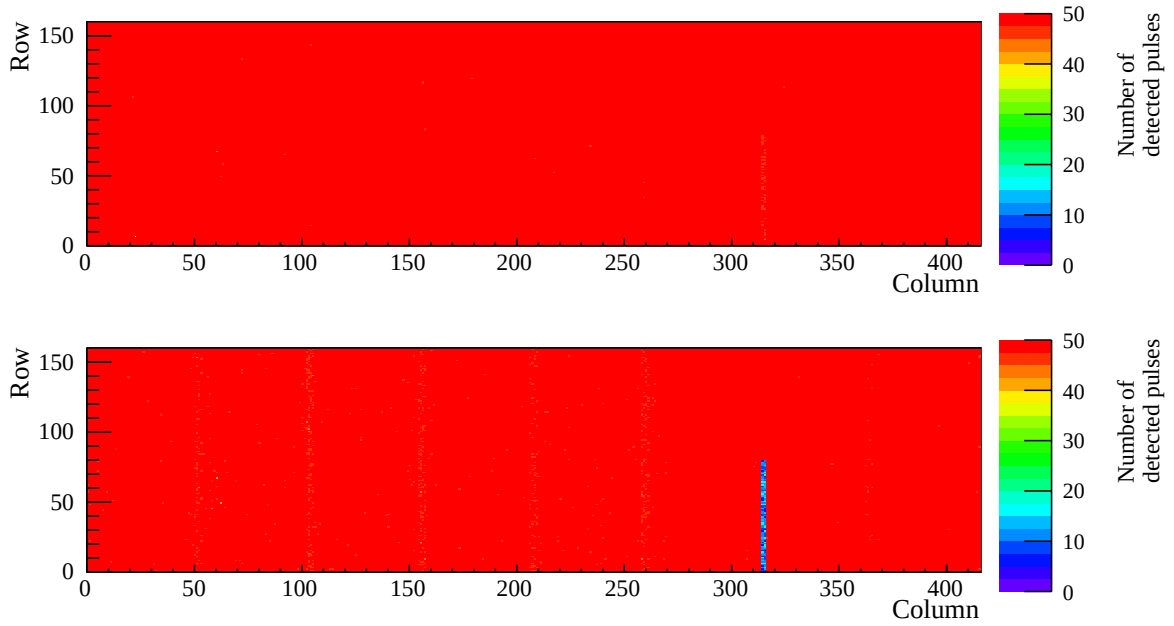


Figure 3.26.: Efficiency map of module M4634, which was graded C*. The number of registered calibration pulses is color-coded. At a hit rate of 50 MHz cm^{-2} (top), the efficiency is almost 100 %. At 100 MHz cm^{-2} (bottom), a single double column shows a severely degraded efficiency.

⁶A double column corresponds to 160 pixels and 3.85 % of all pixels on a ROC.

3.4.3. Energy Calibration

The pulse height of the sampled signal depends on the gain, which varies between pixels on the same readout chip. As a result, a certain physical signal can lead to different pulse heights (in ADC units) in different pixels. Two steps are required to deduce the physical height of a signal from the ADC units: first, the pulse height calibration (Section 3.3.2) is applied. The pulse height can then be expressed in terms of the on-chip charge injection mechanism (Vcal units). These are the same for all pixels on the same readout chip. However, the charge corresponding to one Vcal unit varies between different readout chips. A second calibration is required to convert from Vcal units to physical units. This so-called Vcal calibration was done for every pixel module as part of the qualification procedure.

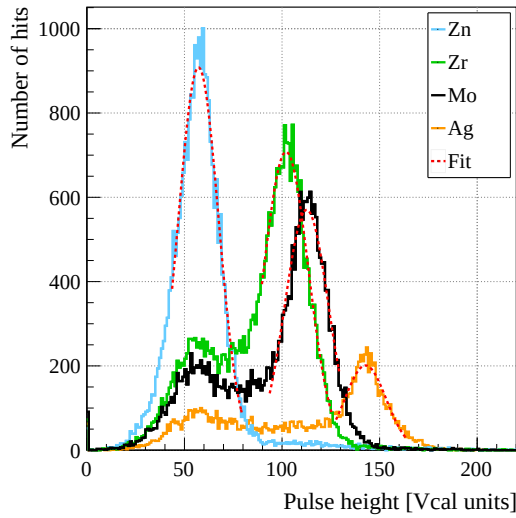
Fluorescence photons from four targets, namely zinc (Zn), zirconium (Zr), molybdenum (Mo), and silver (Ag), were used for the calibration. Their K_α -transition energies are summarized in Table 3.2. The total number of electrons that a photon creates in the sensor can be calculated because an energy of 3.65 eV [80] is required to create an electron-hole-pair in silicon.

The pixel modules are illuminated sequentially with photons from all four targets. For each target, the pixel module is illuminated with X-rays for 100 s, and the pulse height spectrum in Vcal units is measured by the ADC on the readout chips. The ADC value of every hit is converted to a Vcal value with the previously determined pulse height calibration. The spectra for the four used targets are shown in Figure 3.27(a). The energy peak of every spectrum is obtained by fitting a Gaussian function to the data. The energy resolution of the psi46dig readout chip is not sufficient to separate the K_α and K_β -lines. The contribution of K_β -photons leads to a slight shift of the spectrum to larger Vcal values. The effect is small, because the K_β -peak is one order of magnitude smaller compared to the K_α -peak (Figure 3.18). For reasons of simplification it was assumed that the measured energy corresponds to K_α -photons only.

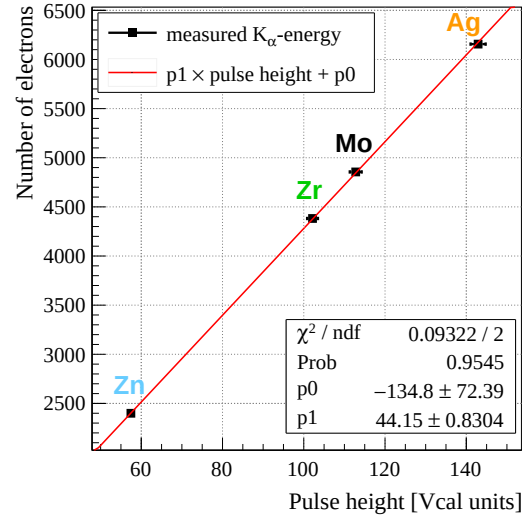
In the last step, the number of electrons created in the sensor is correlated to the measured peak values, as shown in Figure 3.27(b). The relative uncertainty of each energy measurement is estimated to be 1.35 %. This value was obtained from 15 identical measurements performed with one readout chip. The calibration factor corresponds to the slope of the fit function (about 45 e^- /Vcal unit). The offset can be caused by a non-linear behavior for low pulse heights and therefore has little relevance.

Table 3.2.: K_α -transition energies [81] of the targets used for the energy calibration, and the number of electron-hole pairs created in the silicon sensor (N_{e-}).

Target	K_α -energy [keV]	N_{e-}
Zn	8.64	2400
Zr	15.77	4382
Mo	17.48	4856
Ag	22.16	6156



(a) Energy spectra of four targets, measured with a psi46digV2 readout chip. Gaussian functions (red) are fitted to the data.



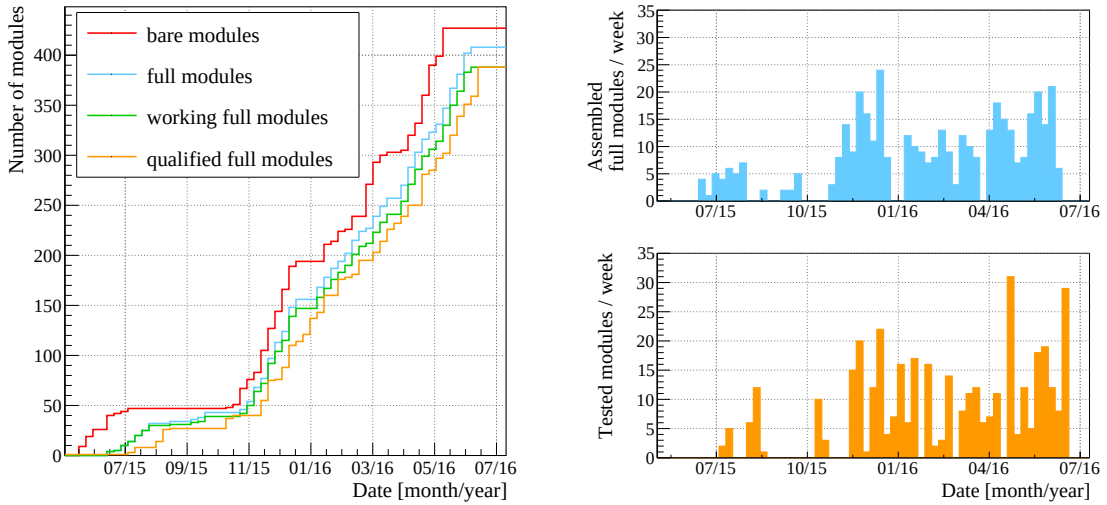
(b) Plot of the number of electrons created in the sensor vs. peak of the spectrum of each target. A linear fit (red) is performed to obtain the calibration constant.

Figure 3.27.: Energy calibration of the Vcal DAC.

3.5. Course of the Series Production

The series production of pixel modules at KIT started in May 2015 and finished in June 2016. Figure 3.28(a) shows the number of produced bare modules as well as the number of assembled and tested full modules over time. In total 437 bare modules have been built, out of which 409 full modules have been assembled. Histograms of the weekly number of assembled modules, as well as the number of entirely tested modules (cold box and X-ray test) per week, are shown in Figure 3.28(b). The mean rate was about 7 assembled full modules per week. The production was delayed several times due to unavailability of components caused by suppliers failing to meet delivery deadlines. If roughly 18 weeks, in which some components were missing, are excluded from the calculation, the resulting production rate is about 12 full modules per week. The pixel modules were qualified with a delay of one to two weeks because they were shipped to RWTH Aachen usually in batches of 18 or 36 pieces. The maximum throughput reached was 31 tested modules per week.

The original plan foresaw the construction of 256 modules, which are required for half of layer 4 of the barrel pixel detector, and about 50 spare modules. In the end, KIT



(a) Integrated numbers of produced bare modules (red), assembled full modules (blue), modules found working at KIT after assembly (green), and modules fully qualified at RWTH Aachen (orange).

(b) Number of assembled full modules per week (top) and number of fully tested modules per week (bottom).

Figure 3.28.: Progress of the pixel module production of the KIT/RWTH Aachen consortium.

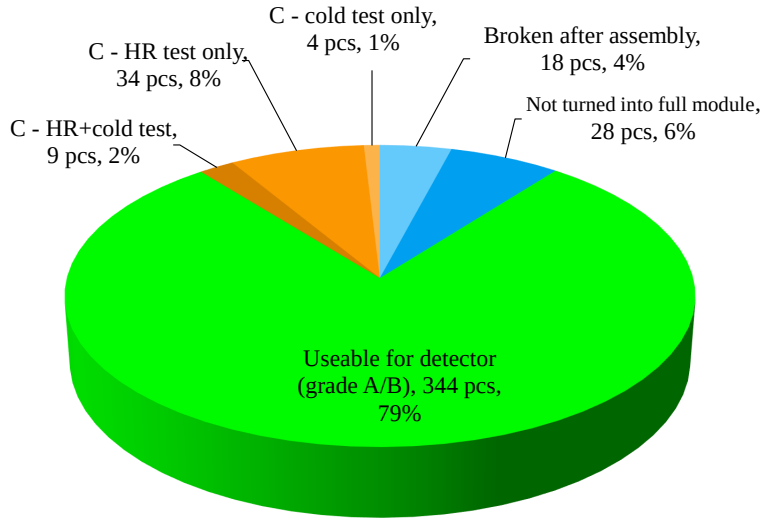


Figure 3.29.: Overview of the numbers of useable and rejected or damaged pixel modules. The absolute number of modules and the proportion relative to 437 produced bare modules are given.

built about 100 additional modules. These modules were installed in layer 3, for which other centers had not produced enough working modules.

The yield of the production is visualized in Figure 3.29. Bare modules were tested at KIT before further processing. Out of the 437 produced bare modules 420 (96 %) were found suitable for assembly into full modules. Out of these, 11 modules were used for tests or given to other production centers and were therefore not further processed. As a result, 409 full modules were assembled in total. A few failures occurred during the assembly procedure (e.g., damaged ROCs, damaged wire bonds, broken connectors), resulting in 18 modules that were broken. Overall, 391 working full modules (93 % of the 420 bare modules) were shipped to RWTH Aachen for the final qualification. There, 23 modules were graded C and 24 modules were graded C* in at least one of the electrical tests or the X-ray tests. In total, 141 modules were graded A, and 203 modules were graded B, resulting in 344 modules that passed all tests (88 % of 391) and were considered good enough for installation in the pixel detector. The combined yield from a bare module to a grade A or grade B full module was 79 %. Results from the individual qualification tests are presented in the following sections.

3.5.1. Results of Cold Box Tests

In the cold box setup, 153 of the tested modules (39 %) were graded A, 225 modules (58 %) were graded B, and 13 modules (3 %) were graded C or C*.

Most modules were downgraded in the I-V test of the silicon sensor. Results from this test are summarized in Figure 3.30. Five modules were graded C in this subtest. Three of them had a leakage current above 10 μA . The sensors of the other two modules were not connected to the bias voltage at all. The mean leakage current of all other modules was 0.6 μA at 150 V in the test at +17 °C. A large fraction of modules received the B grade because the leakage current did not scale with the temperature as expected, as shown in Figure 3.30(b). The leakage current at 150 V was measured at +17 °C and -20 °C. According to Equation 3.5, a factor of $I_L(+17^\circ\text{C})/I_L(-20^\circ\text{C}) \approx 30$ is expected if the current is caused by thermally generated electrons in the bulk of the sensor. For 222 modules the factor was below 20. All other production centers observed this effect as well. The larger than expected surface leakage current can be attributed to the quality of the sensors.

Only three pixel modules failed the tests due to bump bonding problems. In two of the three modules with a substantial fraction of missing bump bonds, the pixel cells were also damaged. As a result, the affected ROCs failed other tests as well. For example, they showed an increased noise, and for one ROC the trimming to a threshold of 35 Vcal units was not possible.

Figure 3.31 shows a comparison of the number of defective bump bonds before and after the thermal cycling ($\Delta N = N_{\text{after}} - N_{\text{before}}$). One entry of the histogram corresponds to a single readout chip. The mean value of the distribution is compatible with zero. For a few hundred ROCs there is a deviation of $1 < |\Delta N| < 8$ pixels. Since the distribution is symmetrical around zero, the deviations are likely to be caused by statistical fluctuations. The accuracy of the bump bond test is limited; thus it cannot separate perfectly between good and bad bump connections. One can conclude that the stress induced during the thermal cycling did not systematically break bump bond connections.

Only five modules did not pass the cold box test for other reasons. For one module the pulse height optimization algorithm failed repeatedly. No settings could be found which allow using the full ADC range. Three modules had a single problematic readout chip that did not send valid data in at least one of the tests. Finally, one module received grade C* because of a single dead double column.

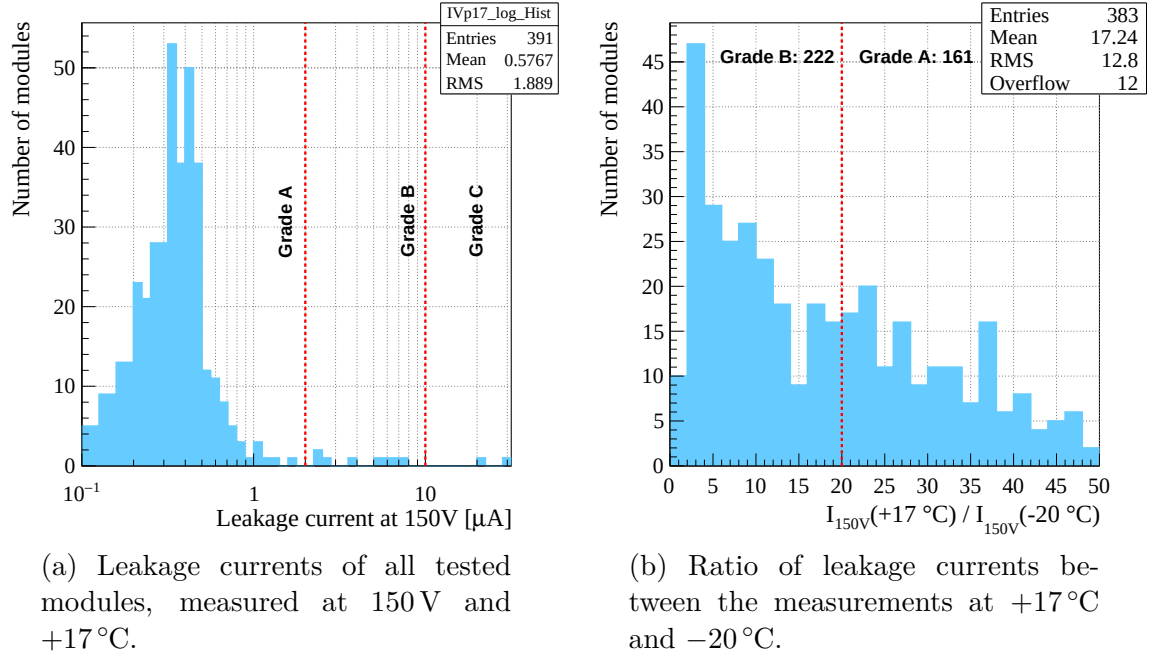


Figure 3.30.: Results of the current-voltage (I-V) measurement in the cold box. In both histograms, red dashed lines indicate the grading criteria.

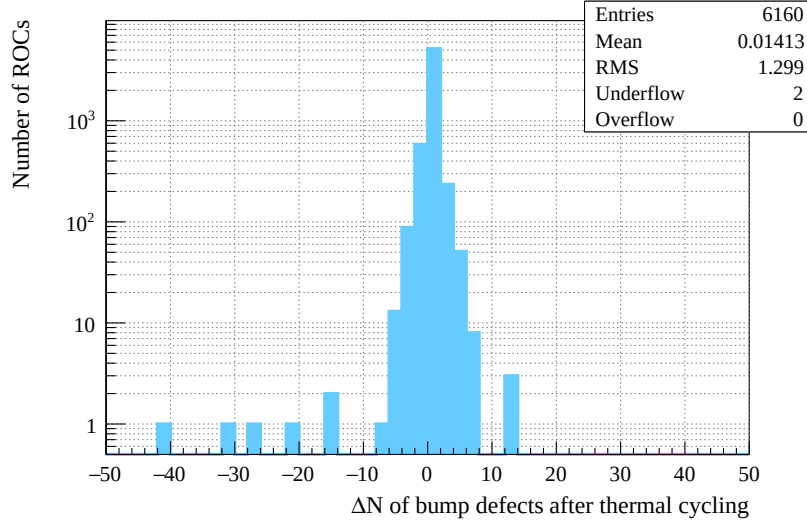


Figure 3.31.: Difference in the number of bump bond defects between the tests at -20 °C before and after thermal cycling. Each histogram entry corresponds to one readout chip.

3.5.2. Results of High Rate X-ray Tests

The majority of rejected modules failed the X-ray tests. A total of 339 modules (86.7 % of 391) were graded A, 9 modules (2.3 %) were graded B, 24 modules were graded C* (6.1 %), and 19 modules (4.9 %) were graded C.

The high-rate test was used, among other things, to find pixels that do not produce hit signals. In such pixels, the pixel unit cell is either defect or masked, or the bump bond connection between ROC and sensor is missing. The distribution of the number of pixel defects per readout chip is shown in Figure 3.32. The distribution of pixel errors for all production centers is also shown as a reference. Overall, the bump bonding quality at KIT was excellent, with a mean value of 8.2 defect pixels per module (0.013 % of 65 560 pixels per module).

The number of pixels without any hits can be used to cross-check results from the bump bond test in the cold box setup. Figure 3.33(a) shows the number of missing bump bonds obtained from the electrical tests in the cold box versus the number of defective pixels obtained from the X-ray tests. Only the absolute number of problematic pixels is compared, i.e., it was not checked whether in both tests the same pixels are defective. Nevertheless, this comparison is relevant because independent grades were given in both setups. The results of both tests are in good agreement. However, the bump bond test in the cold box tends to incorrectly identify some pixels as defective, as these pixels showed hits in the X-ray tests. On the other hand, in two cases not all defect bump bonds were found in the electrical qualification, and the ROCs passed the cold box test, while in the X-ray test a few hundred defective pixels were observed.

Figure 3.33(b) shows another indication that the electrical bump bond test overestimates the number of defective pixels. The results of both tests were compared for every pixel individually. For every module, the histogram shows how many pixels were found defective only in one of the two tests and how many were defective in both tests. On average the cold box test yielded about six additional alleged defects, which the X-ray test did not confirm. Because this corresponds to less than one false positive per ROC, the effect does not influence the grading and can be ignored.

Figure 3.34 shows an overlay of all tested modules, where the number of times a specific pixel has had a bad bump bond connection is color-coded. Dead or masked pixel unit cells also appear in the map, because they do not produce any hits. Most of the unconnected pixels are located at the edges of the readout chips. The corners of the ROCs on the top right (ROC 0) and bottom left (ROC 8) are more frequently affected by bump bond defects. There the same pixels are not connected in up to seven modules. Nevertheless, the test verifies that there were no severe systematic problems during the module assembly, which would have resulted in the same defective pixels on several readout chips. Also, some artifacts are visible in the map: six ROCs had a single problematic double column, which did not produce any hits at all.

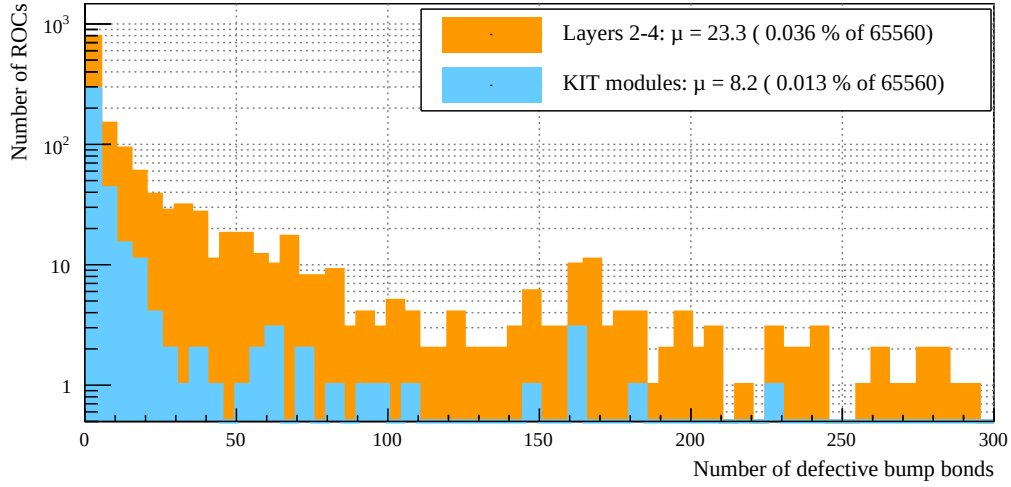
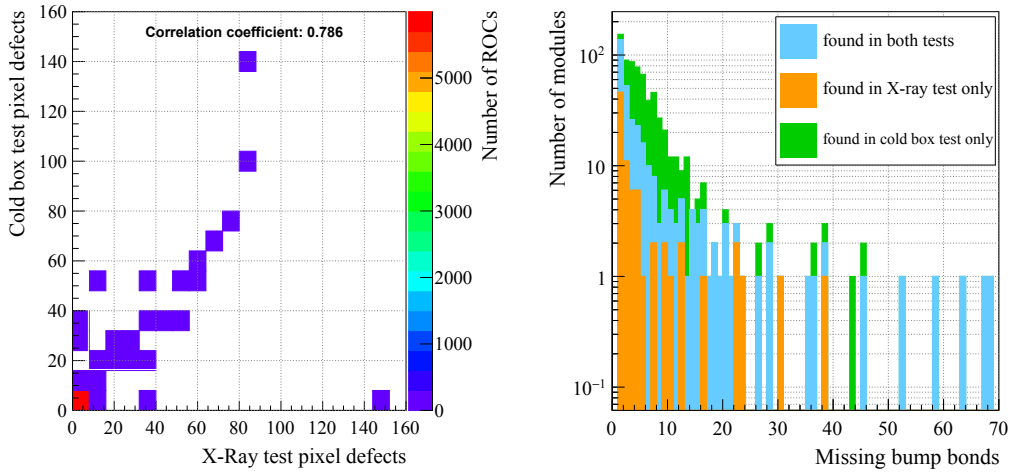


Figure 3.32.: Number of defective pixels per module, obtained from the X-ray tests. The blue histogram shows the results for modules built at KIT, the orange histogram shows the results for all modules produced for BPix layers 2-4.



(a) Correlation of the total number of pixel defects per ROC. It is not checked whether the same pixels are affected in both tests.

(b) Number of pixels per module that were found defective in both tests and the number of pixels allegedly found defective in only one of the tests. The results of both tests are compared for every pixel individually. The histograms are not stacked.

Figure 3.33.: Comparison of results from the bump bond test in the cold box (test at +17°C) and the high rate X-ray tests.

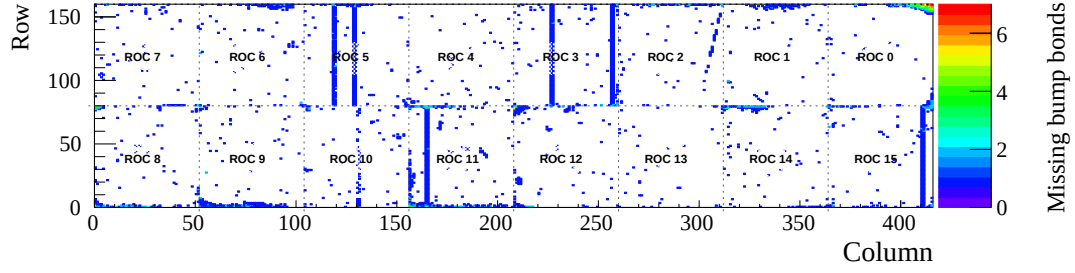


Figure 3.34.: Module map of missing bump bonds, determined in the X-ray tests. The results from 385 tested modules are overlaid. The locations of the 16 ROCs are indicated.

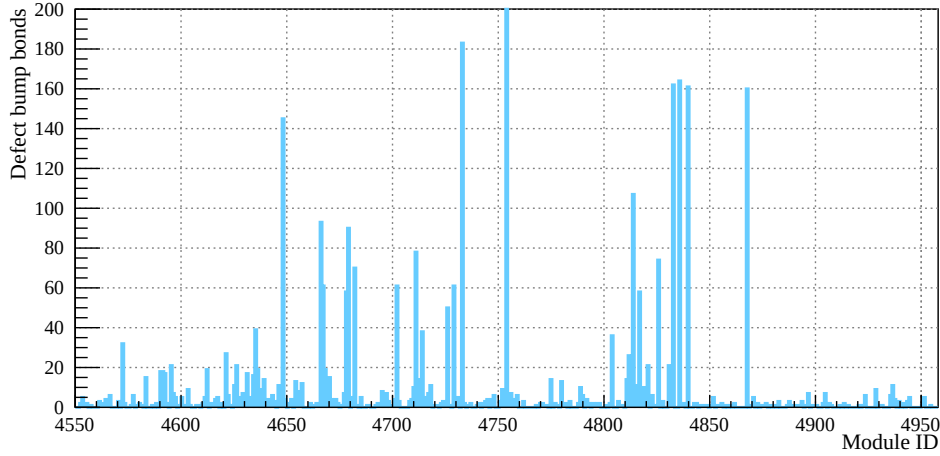


Figure 3.35.: Number of defective or disconnected pixel cells, obtained from the X-ray test. The result is shown for all modules that were tested at RWTH Aachen.

Figure 3.35 shows the number of defective pixels versus the ID of the module. The pixel modules were numbered consecutively, and thus the plot represents the evolution over time. At the end of production, the rate of defective pixels was slightly reduced. There are some periods with significantly more defects (for example M4800-M4840). The reason for this cannot be determined with the available data. Whether, for example, components were contaminated, or a setup was readjusted, is not known.

Frequent readout errors (wrongly encoded data) occurred in ten pixel modules. For seven of them, the errors could be fixed by increasing the Vdig DAC of the affected ROC by one or two units. This, however, leads to an increased digital current. The other three modules were graded C because either Vdig had to be increased by more than two DAC units or because the readout errors could not be fixed at all.

Three pixel modules were rejected because of a non-uniform readout. In these modules, a double column stopped giving any hits after a few seconds of data taking.

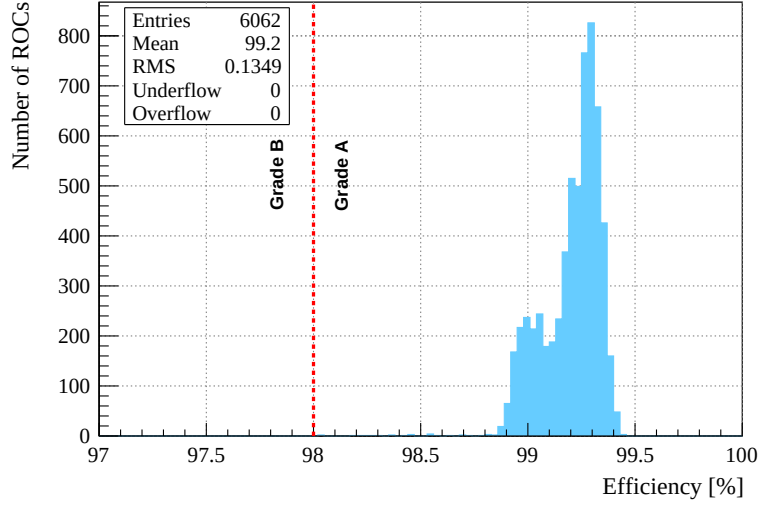


Figure 3.36.: Histogram of the interpolated X-ray hit detection efficiencies of all readout chips, at a hit rate of 120 MHz cm^{-2} . The red dashed line indicates the grading criterion.

Figure 3.36 shows the measured efficiencies of all readout chips. At an X-ray hit rate of 120 MHz cm^{-2} , which is expected for modules in layer 2 of the BPix detector, a mean detection efficiency of $(99.20 \pm 0.13) \%$ was measured. No module showed a significantly decreased efficiency and was therefore graded C. However, 24 pixel modules had a double column with reduced efficiency and were graded C*. These modules were not installed in the detector, because in the end enough grade A/B modules had been built.

3.5.3. Results of the Energy Calibration

A histogram of the measured Vcal calibration factors, which correspond to the slopes of the linear fits, is shown in Figure 3.37. For the psi46digV2 ROC, a unit of the Vcal DAC corresponds to a signal of about (45.3 ± 2.7) electrons. As a comparison, for the psi46V2 ROC used in the Phase-0 detector, a conversion factor of about $65 \text{ e}^-/\text{Vcal unit}$ was measured [82]. The energy calibration was used as a cross-check that the module works as expected. No grading criteria were applied, and thus no module was rejected in this test.

Figure 3.38 shows the mean calibration constant of all 16 readout chips of a pixel module versus the module ID. For several consecutive module IDs, small systematic deviations from the mean value are visible. This effect may be attributed to differences in the manufacturing process of the readout chips. The ROCs have been delivered to KIT in three batches. Ten modules, ranging from M4838 to M4852, are clear outliers. They have a calibration constant that is about $6 \text{ e}^-/\text{Vcal unit}$ lower than the mean value. These modules were built with ROCs from the same wafer. Probably some process parameters have varied in the production of this wafer.

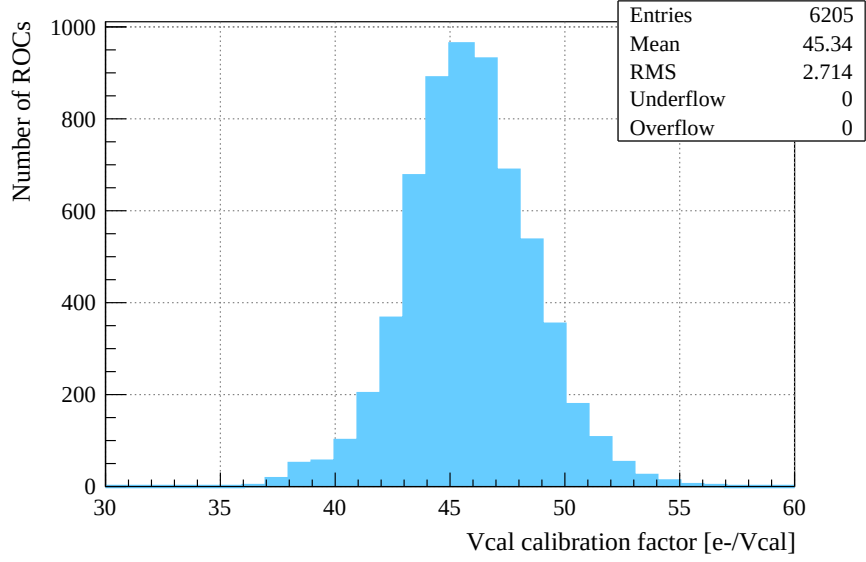


Figure 3.37.: Conversion factor from Vcal units to number of electrons created in the sensor, shown for all tested readout chips.

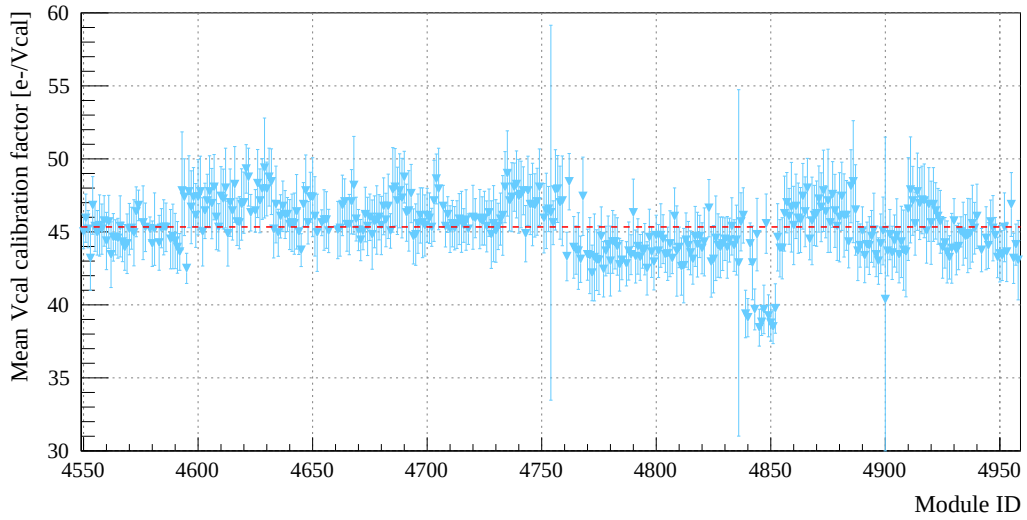


Figure 3.38.: Average Vcal-electron conversion factor of a pixel module, shown versus module ID. The red dashed line indicates the average over all ROCs.

3.6. Reception Test

Before pixel modules were mounted on the detector at PSI, modules from all BPix production centers were collected at ETH Zürich. A quick reception test was foreseen at ETH to ensure that no module was damaged during the transport. It was also desired to have a final test of all modules in the same test setup for better comparability of results. In addition, the Kapton covers, which protect all wire bonds, were glued to the KIT modules at ETH Zürich. Only after almost all modules had been produced and were fully tested, the decision was taken that protective covers needed to be glued to every module. At RWTH Aachen, where only testing of modules was foreseen, gluing was not possible. Thus it was considered to either send the modules back to KIT or to glue the covers at ETH, before the reception test. The latter was preferred because it required one transport and test cycle less.

All pixel modules were transported from Aachen to Zürich at the beginning of July 2016, two weeks after the qualification was finished. Modules were stored in the transportation boxes that had already been used for the shipment from Karlsruhe to Aachen. Every box was sealed in a plastic foil together with a desiccant.

Gluing of the protective covers and testing of the pixel modules at ETH Zürich involved people from KIT, ETH Zürich, and RWTH Aachen. Four gluing stations had been set up for this purpose. The gluing procedure is briefly described here.

A photograph of a protective cover is shown in Figure 3.39. As a first step, the edges of the flat Kapton sheet were bent with a special tool. In this way, the wire bonds were not only protected from above but also from the side of the module. The module was removed from the aluminum holder and was placed in the gluing station, and the sacrificial module cable was unplugged. Glue was applied to capacitors on the module with a stamp. In the last step, the protective cover was lowered onto the module, and force was applied to hold the cover in position. A curing time of about 1 h was required before the modules could be removed from the jigs. Because four gluing stations were used in parallel, up to 30 modules were equipped per day. A few grade C modules were not used, resulting in a total of 380 modules that were equipped with the protective cover. Every module was inspected under a microscope to verify that the gluing was successful.

After another 24 h of curing, the reception test in the cold box was performed. The first 116 pixel modules were tested twice, before and after the cap gluing. This was done to spot eventual problems during the gluing process, which could damage pixel modules.

The reception test was performed in the same cold box setup that had been used to qualify the modules for layer 2. It was possible to test up to four pixel modules in parallel. The test procedure, which was developed at ETH, was based on the full qualification (Section 3.3.2). However, the procedure was greatly simplified to reduce the time required for testing. It included the Pretest, the PixelAlive test, the electrical

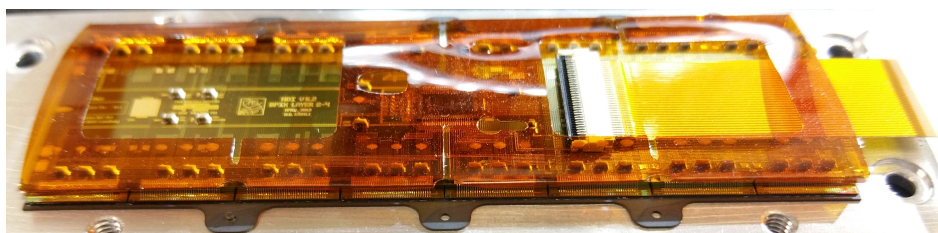


Figure 3.39.: Photograph of the protective cover, which was glued on top of all pixel modules.

bump bond test, and the calibration of the readback mechanism. Finally, the sensor IV-curve was measured again for every module. All tests were done at a temperature of $+17^{\circ}\text{C}$ only. All data were analyzed with a modified version of the MoReWeb software. A summary of the results is described below.

Only two pixel modules were severely damaged during transport or gluing. One pixel module had no leakage current in the reception test, and the other one had a broken connector (this module was already graded C* before). A broken base strip was found on six modules. The damage was likely caused by the plastic protection cover, which was used to clamp the modules on the module handle (Figure 3.2). Force applied to the cover is transferred to the base strips. This could have happened during any steps of the production, qualification, transport or handling. Because only one of six screw holes of the base strip was damaged, the modules could still be fixed on the detector support structure with the remaining five screw holes. It was decided to regard these modules still usable for the detector. However, in the end it was not required to install them.

The number of defect pixels in the reception test was found to be compatible with the full qualification, and no additional modules were rejected because of pixel defects. Only one module showed 13 additional dead pixels on a single readout chip, close to the module cable connector, after the gluing procedure.

Figure 3.40(a) shows the differences of the leakage currents at 150 V, measured directly before and after mounting of the protective Kapton covers. None of the modules showed a significantly increased current, which indicates that the gluing process did not cause a larger leakage current in general. Figure 3.40(b) compares the leakage currents between the reception test and the qualification at RWTH Aachen. The currents are comparable for a majority of the pixel modules, although in the reception test the mean value was about $0.09\text{ }\mu\text{A}$ larger. The relative increase is 16 % compared to the mean value of the leakage current in the qualification procedure ($0.58\text{ }\mu\text{A}$). The difference may be explained by a larger sensor temperature in the reception test, which could be caused by the different method of fixing the modules in the setup, or by different methods of measuring the temperature. According to Equation 3.5, an increase of the leakage current by 16 % at $+17^{\circ}\text{C}$ corresponds to a temperature difference of 1.8 K.

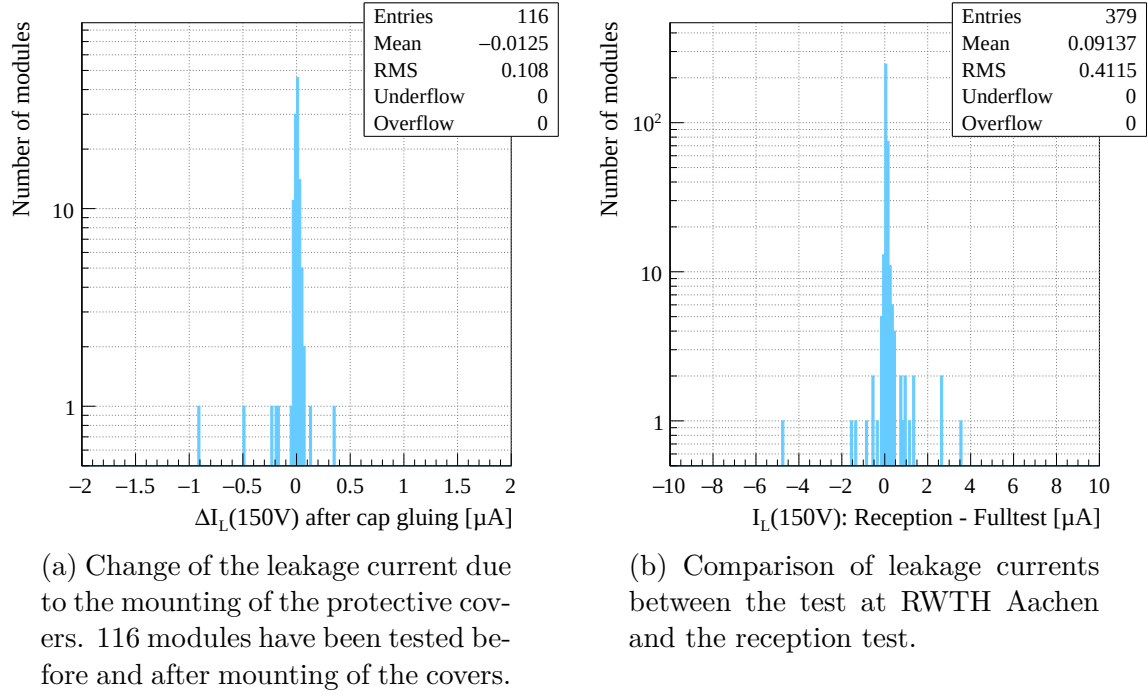
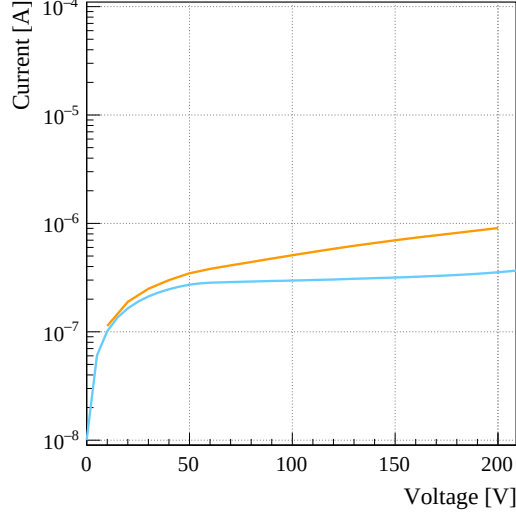


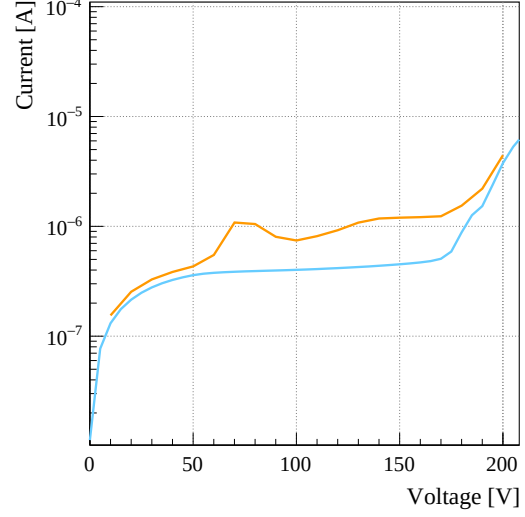
Figure 3.40.: Comparison of sensor leakage currents before and after mounting of the protective covers, and comparison with the measurement at RWTH Aachen. The currents were measured at a bias voltage of 150 V and at a temperature of $+17^\circ C$.

However, for six modules the current increased by more than $0.5 \mu A$ compared to the full qualification, and for six modules the current decreased by more than $0.5 \mu A$. For pixel modules with a significantly increased leakage current also the slope of the IV curve had changed. Two examples are shown in Figure 3.41. Most of the sensors had a steeper I-V curve with no plateau region (Figure 3.41(a)), and some of the sensors showed a so-called soft breakdown, with a sudden current increase below 150 V (Figure 3.41(b)). Nevertheless, all modules still had a leakage current below $10 \mu A$ at 150 V and thus no module was rejected. It is not known if the sensor properties have changed during storage or transport.

In total 343 modules were graded A or B in all tests, including the reception test, and were considered usable for the detector. Of these modules, 323 were finally installed in BPix layer 4 and layer 3. Table 3.3 summarizes the results of all tests.



(a) Module M4855.



(b) Module M4577.

Figure 3.41.: Two examples of I-V curves that had significantly changed between the full qualification at RWTH Aachen (blue) and the reception test at ETH Zürich (orange).

Table 3.3.: Final results of the pixel module qualification at RWTH Aachen and the reception test. The number of modules that received a certain grade in the individual tests, and the combined test results, are given. The yields correspond to the fraction of grade A and grade B modules in relation to the sum of modules.

Grade	Cold box test	X-ray test	Reception test	Combined
A	153	339	344	140
B	225	9	33	203
A+B	378	348	377	343
C	13	43	3	48
Defective	18	18	18	18
Sum	409	409	398	409
Yield	92 %	85 %	95 %	84 %

4. Integration Tests and System Tests of the Power System

Several parts of the Phase-1 power system have been developed at RWTH Aachen University. All phases, from design to prototyping to mass production, involved an extensive test program. These tests can be categorized as component tests, integration tests and system tests [83]. Such classification is often used in software development, but it applies here as well. In component tests, the functionality of individual parts of the system is validated. Integration tests investigate the interplay between major parts of the system. Finally, in system tests, it is verified that the fully integrated system meets the requirements.

Examples of component tests are measurements of characteristics of the DC-DC converters. These have been performed in other works: the line and load regulation, voltage ripple, radiated noise, efficiencies, and thermal properties have been measured [50, 84–86]. A prototype of the modified power supplies has also been tested [87]. Procedures for the testing of power distribution boards have been developed [88, 89].

Integration tests and system tests with the final components used for the pixel detector were performed in the context of this thesis. These include measurements of voltage drops along the supply tube, tests of the power system’s transient behavior (e.g., during power-on, power-off, and interlocks), and tests of implemented protection features. The communication with the CCUs via optical transmitters was established, and it was verified that DC-DC converters could be enabled and disabled. Finally, measurements with pixel modules powered by DC-DC converters were performed. The electronic noise of the ROCs was measured. The hit detection efficiency was determined in X-ray tests, and the energy calibration was performed.

4.1. The System Test Setup

A BPix system test setup, which reproduces the situation in the barrel pixel detector as closely as possible, has been developed. Within the entire Phase-1 upgrade project this is the only setup that has a specific focus on tests of the power system. The setup has also been used to investigate issues with broken DC-DC converters, which occurred during the data taking period in 2017. These tests are described in Chapter 6.



Figure 4.1.: Photograph of the system test setup. It shows the CAEN 4603D power supply (1), the CO₂ cooling system (2), the multi-service cables (3), the pixel module (4), a load board (5), and the computer with the FEC (6). The supply tube boards are covered by insulating foam (7), hence they are not visible.

A photograph of the setup is shown in Figure 4.1. The input voltage for the DC-DC converters, as well as the high voltage for biasing the silicon sensor of pixel modules, are generated by a CAEN A4603D power supply. This is the same type of power supply that is used in the Phase-1 pixel detector. The device is programmed and read out with a CAEN A1676A branch controller in an SY2527 mainframe [54]. A voltage of 48 V is supplied to the crate by a Delta Elektronika SM52-30 power supply [90]. The system can be controlled via a keyboard connected to the mainframe, or it can be controlled over a network by using the OPC (Open Platform Communications) protocol [91]. The latter enables automation of test sequences, for example with LabVIEW.

All devices of the CAEN power system are plugged into an electronics rack. The power supply is connected to the supply tube boards by two 43 m long multi-service (MS) cables. These cables are of the same type as the ones used in CMS, and they have a comparable length.

The setup represents an exact copy of the power parts in one BPix supply tube slot. A photograph of the installed boards, which are described in detail in Section 2.4.3, is shown in Figure 4.2. The high-voltage is routed through the MS cable to a high-

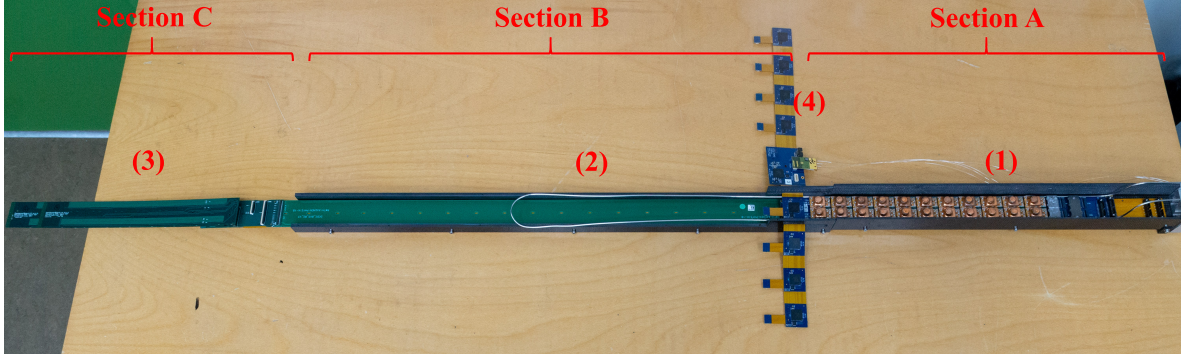


Figure 4.2.: Photograph of the PCBs used in the system test setup: DC-DC converter bus board (1), extension boards (2), adapter and connector boards (3), and CCU ring board (4). The HV flex board lies below the other boards and is not visible. The PCBs are installed in a carbon fiber structure that has the exact dimensions of one supply tube slot.

voltage flex board. The low voltages are routed to a bus board, which is equipped with 13 analog and 13 digital DC-DC converters. The whole chain of extension boards, adapter boards, and connector boards is connected to the bus board. A CCU ring board is also installed, which allows to enable and disable the DC-DC converters and to read out their PowerGood bit. One DOH, which is plugged into the CCU ring board, is connected via optical fibers to a Tracker FEC for control and readout of the CCUs. Only the Tracker FEC is not the same μ TCA-based device that is used in the Phase-1 pixel detector. Instead, it is built as a PCI Mezzanine Card, which is plugged into a computer system.

All boards are embedded in a carbon fiber structure that has the exact dimensions of a single supply tube slot. Thus, the installation procedures could be tested, and thermal measurements under realistic conditions could be carried out.

The DC-DC converters are cooled by a two-phase CO_2 cooling system that has been developed at RWTH Aachen. This system is based on the 2PACL method, like the cooling system in CMS. It can be operated with any CO_2 temperature between about -30°C to $+25^\circ\text{C}$. The stainless steel cooling tubes have the same cross-section as in the pixel detector, namely a wall thickness of $50\ \mu\text{m}$ and an outer diameter of $2.2\ \text{mm}$. Further information about the CO_2 system can be found in references [92, 93].

One sector of the BPix supply tube serves up to 39 pixel modules. Because it is impractical and also expensive to use so many pixel modules for system tests, programmable current sinks are used instead. They have been developed and built at RWTH Aachen University. Three of these devices, which are also called load boards, are used in the setup. Each load board has 26 channels (13 for the analog and 13 for the digital voltage) that can draw up to $3\ \text{A}$ each. Every channel can be programmed individually. Thus, any load situation in the detector can be simulated in the system test setup.

It is also possible to test pixel modules in the system. They are read out with a digital testboard but can be powered from external sources. An adapter cable is used for this purpose, which routes all signals from the pixel module to the DTB, except for the low and the high voltages.

4.2. Expected Front-End Currents of the Phase-1 Pixel Detector

A precise estimation of the currents drawn by the pixel modules is required to test the power system under realistic conditions. As described in Section 2.4, a pixel module requires two different voltages: one for the signal shaping and amplification circuits in the pixel unit cell, which is thus called the analog voltage, and a so-called digital voltage for the circuits that read out the pixel cells and further process the information.

The analog current is the same for all pixel modules and depends only on the settings of the Vana DACs of the readout chips. An analog current between 24 mA and 26 mA per ROC was foreseen for the Phase-1 detector. For the following tests, 26 mA per ROC (416 mA per module) was used as a baseline. The digital current, on the other hand, depends on the activity in the readout chip. It is made up of a constant current of 27 mA and a hit rate dependent current of 0.12 mA times the pixel hit rate in MHz cm^{-2} (Equation 2.1 on page 24). The Token Bit Manager is also powered by the digital voltage. It draws a constant current of about 35 mA.

The expected front-end currents were calculated for the nominal load scenario. This corresponds to proton collisions at the design instantaneous luminosity of the pixel detector of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The output currents of analog DC-DC converters depend only on the number of pixel modules that are connected to them. In layers 4 and 3 of the BPix detector, one pair powers four pixel modules, whereas in layer 2 each pair powers three or two pixel modules, and in layer 1 each pair powers only a single pixel module. Each slot of the BPix supply tube comprises 13 pairs of DC-DC converters in total.

The digital currents were estimated with a tool [94] provided by W. Bertl from PSI that uses measured data from the 2011 and 2012 run of CMS to predict the hit rates with the Phase-1 pixel detector geometry. In particular, it uses distributions of the cluster fluence and the cluster size in η and ϕ . The pixel hit rates were obtained from this tool for every pixel module in the detector. The expected digital currents were calculated with Equation 2.1.

Figure 4.3 shows the expected analog and digital currents for one slot of the supply tube. The naming of the DC-DC converters follows the same conventions used in the schematics. They are named after their type (A or D), their position on the bus board (0-7) within the power group and the power group itself (C1 or C2). For geometric

reasons not all supply tube sectors are connected to the same number of pixel modules. In two of eight sectors, one DC-DC converter pair for layer 3 does not power any modules. In two other sectors, a pair of layer 2 DC-DC converters is not connected to any modules. Figure 4.3 shows the currents for the worst case, i.e., the maximum number of modules is connected.

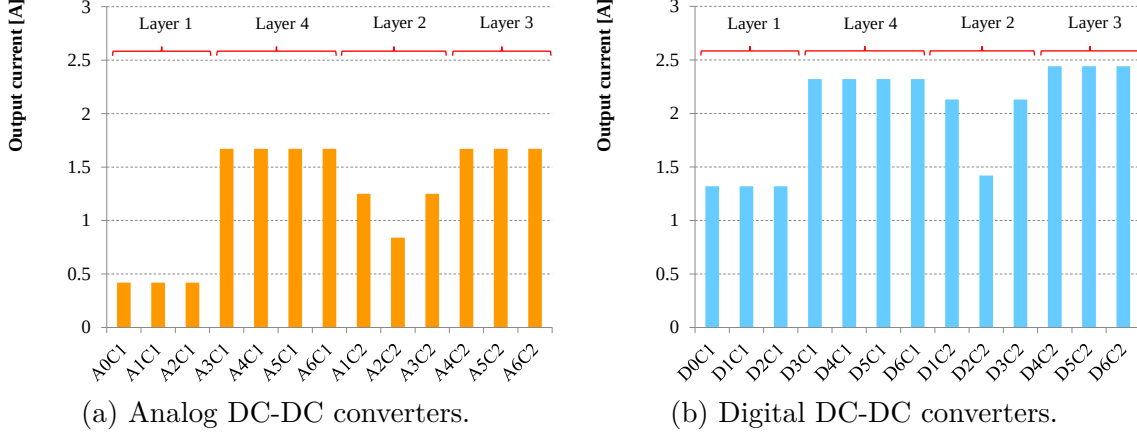


Figure 4.3.: Expected pixel module currents that are drawn from the DC-DC converters at an instantaneous luminosity of $L_{\text{inst}} = 2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The currents are shown for all DC-DC converters of one BPix supply tube sector.

4.3. Voltage Drops

Voltage drops along the supply tube reduce the input voltage at the pixel modules. According to Ohm's law, the voltage drop, ΔV , is proportional to the resistance R and the supply current of the pixel modules:

$$\Delta V = R \cdot I \quad . \quad (4.1)$$

The resistance of the boards is constant. The currents drawn by the pixel modules change with the instantaneous luminosity. Hence the voltage drops change dynamically. Small voltage drops can be realized by low resistances, which translate to thick copper layers. However, the power boards are within the active CMS volume and should have a low mass, which requires copper layers as thin as possible. A compromise in this respect had to be found during the design of the boards. Too large voltage drops can potentially be dangerous because they are dynamic: on the one hand, the voltage at the module could be too low at high instantaneous luminosities, but on the other hand, the voltage could be above the ROC specifications when there are no collisions in the LHC.

Voltage drops along the supply tube have been measured in the system test setup and were compared to the expected values. The total voltage drop is made up of the voltage drop along the power line (from the DC-DC converter to the module) and the voltage drop on the return line. The voltage drop along the power line is individual for every DC-DC converter. The return line, however, is common for multiple devices. On the connector board, all modules from the same layer share a return path. On the extension board, all modules from all layers have a common return path. This has implications for the measurement procedure: it is essential to draw the expected currents from every DC-DC converter at the same time to obtain correct voltage drops along the return line.

The 78 channels of the electronic loads were connected to all module connectors on the connector boards and the estimated currents for an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ were drawn. The voltage drops along the supply tube were measured between several probe points:

1. Voltage drop in sections A+B: measured between the DC-DC converter output capacitance and the connector of section B and section C.
2. Voltage drop in sections A+B+C: measured between the DC-DC converter output capacitance and the module cable connector in section C.
3. Voltage drop in section C: measured between the connector of sections B/C and the module cable connector in section C.
4. Voltage drops along the return lines: measured between the same connectors as mentioned above.

The connection between section A and section B was not accessible when the boards were plugged together. Thus, the individual drops along these sections could not be measured. Voltages were measured with a Keithley 2710 multimeter [73]. LeCroy current probes (CP031A [95] and AP015 [96]) were used with an oscilloscope to measure the currents drawn by the electronic loads.

Figure 4.4 shows the total voltage drops over the supply tube sections A to C for every DC-DC converter. For better readability, only the largest measured voltage drop is shown for DC-DC converters with multiple connected pixel modules. The largest voltage drop was always measured at the connector closest to the detector because that one has the longest traces. The expected voltage drops (Equation 4.1) were calculated with the resistance values of the PCBs and connectors. The PCB resistances were estimated by the respective designers. The adapter boards and connector boards in section C were developed at the Wigner Research Centre for Physics in Budapest. For these boards, the resistances were extracted from a simulation. The bus board and the extension boards (section A+B) were developed at RWTH Aachen University. The resistances of these boards were calculated with the size and thickness of the copper layers and values from the connector data sheets.

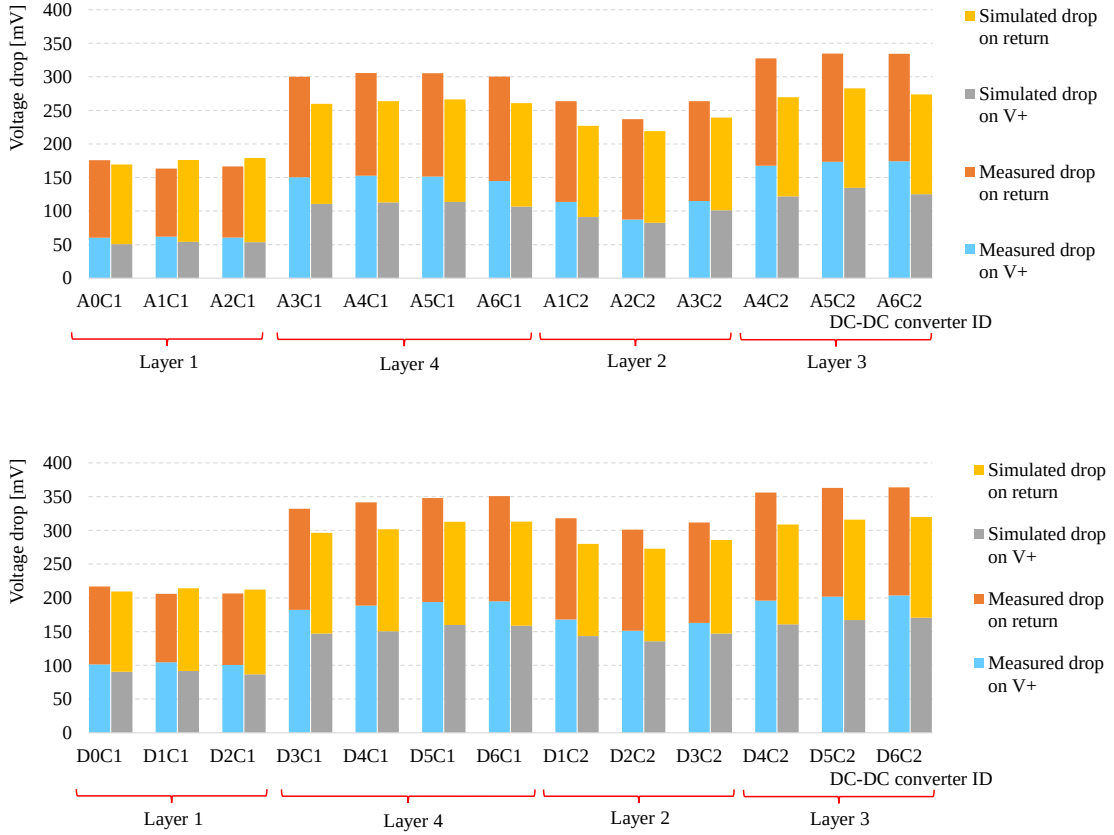


Figure 4.4.: Voltage drops on V+, and the corresponding return lines across the supply tube boards, corresponding to an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Top: analog DC-DC converters. Bottom: digital DC-DC converters. The measured voltage drops and the values expected by the PCB designers are shown for all DC-DC converters of one BPix supply tube sector.

The total voltage drops on the analog lines are in the range of 160 mV to 340 mV, while for the digital lines the voltage drops are between 200 mV and 360 mV. The measured voltage drops are on average 30 mV (about 15%) larger than expected. Layer 1 is closest to the expectation with a difference of less than 15 mV.

In order to assess the results, the accuracy of the measurement must be known. The uncertainty of the voltage measurement of the multimeter for a voltage of 200 mV is about 9 μV , according to the data sheet [97]. However, the measured voltage also depends on the quality of the contact between the probe and the probe pads. Thus, the realistic measurement accuracy is estimated to be about 1 mV.

It must be taken into account that the currents drawn by the load boards cannot be set to perfectly match the expected front-end currents of the nominal load scenario. The currents are also subject to uncertainty. They have been measured with a probe

that has an accuracy of 1 %. The additional uncertainty of the oscilloscope measurement corresponds to 1.5 % of the full scale. Thus, the total uncertainty of the current measurement is estimated to be:

$$\sigma_I = \sqrt{(I \cdot 0.01)^2 + (I_{\max} \cdot 0.015)^2} \cdot \sqrt{\frac{1}{3}} \quad , \quad (4.2)$$

where $I_{\max}$ is the range the oscilloscope was set to. The factor $\sqrt{\frac{1}{3}}$ in Equation 4.2 is introduced because no details about the type of the uncertainty are given in the data sheets [96, 98, 99]. Thus, a rectangular distribution is assumed. As an example, for a typical current of 2 A, measured with a range of 4 A, the resulting standard deviation is 37 mA (1.8 % of 2 A).

The relative uncertainty of the load board currents directly translates into a relative uncertainty of the voltage drop. As an example, for a voltage drop of 300 mV the uncertainty is about 5.5 mV. This is the dominant uncertainty, as it is much larger than the measurement uncertainty of the multimeter. The measured deviations from the expected values are several times larger than the uncertainty. Thus, it can be concluded that the real PCB resistances did not match the simulations and calculations.

The relative deviation from the expected values is largest on the connector boards (section C), as illustrated in Figure 4.5. The measured voltage drops are on average $(21 \pm 12) \%$ larger than simulated.

The significant voltage drops on the module cables (section D) also have to be taken into account. At the time of the tests, not enough of the final module cables were available to measure the voltage drops in section D of the supply tube with the method described above. Instead, the electrical resistivity of one cable was measured and the absolute resistance, which depends on the cable length, was calculated. In layer 1, the current per module is the largest. It leads to an additional voltage drop of up to 359 mV on the digital and 340 mV on the analog line. For all other layers the voltage drops are in the ranges of 220 mV to 239 mV (digital) and 250 mV to 260 mV (analog).

The measurement of the voltage drops was used to calculate minimal and maximal input voltages at the pixel modules to ensure that they are operated within the specifications. The voltage is maximal if the pixel modules draw no currents because the voltage drops along the supply tube are zero. In this case, the input voltage corresponds to the output voltage of the DC-DC converters. However, the pixel modules always draw some current, even when the DACs are not programmed, or no clock signal is available. Thus, the input voltage is always smaller than the DC-DC converter output voltage. By choosing a DC-DC converter output voltage below the critical value of the readout chip, it is ensured that the modules cannot be damaged due to overvoltage. Tests at KIT suggest that the ROCs can be operated with an input voltage of 3.6 V [100].

Effects that influence the DC-DC converter output voltage were taken into account to calculate the lowest input voltage at the pixel modules. These effects were estimated from earlier measurements [50, 85, 89] and are summarized in Table 4.1. The mean



Figure 4.5.: Measured and calculated voltage drops across the supply tube, shown for all digital DC-DC converters of one supply tube slot. Top: voltage drops in sections A and B. Bottom: voltage drops in section C.

output voltage of the DC-DC converters fluctuates around the nominal value due to component tolerances. For a pre-series of DC-DC converters, the relative standard deviation of the output voltage was 1.4 %. This corresponds to 34 mV for an output voltage of 2.4 V and 46 mV for an output voltage of 3.3 V. The output voltage decreases with temperature by a factor of about 0.7 mV K^{-1} . Furthermore, the output voltage depends on the current that is drawn from the DC-DC converter and decreases by about 10 mV A^{-1} . Finally, a safety margin of 100 mV is taken into account.

Figure 4.6 shows the difference between the calculated input voltage at the pixel modules and the lowest allowed voltage, for which a function of the readout chips can be guaranteed. The calculation takes all voltage drops and the effects mentioned above into account. The lowest allowed ROC input voltage is 1.6 V for the analog part. The PROC600 chips in layer 1 require a digital voltage of at least 2.5 V. The psi46digV2 chips, which are used in all other layers, require a digital voltage of at least 2.4 V. The DC-DC converter output voltages that were used for the calculation correspond to 2.4 V (analog) and 3.3 V (digital). With this DC-DC converter output voltages, the input voltages of all channels will always be above the allowed minimum.

Table 4.1.: Effects considered for the calculation of the minimum input voltage.

Effect	Reduction of the analog voltage [mV]	Reduction of the digital voltage [mV]
V_{out} spread	34	46
Temperature effect, $0.7\text{mV/K}\cdot 40\text{K}$	28	28
Safety margin	100	100
Sum	163	174

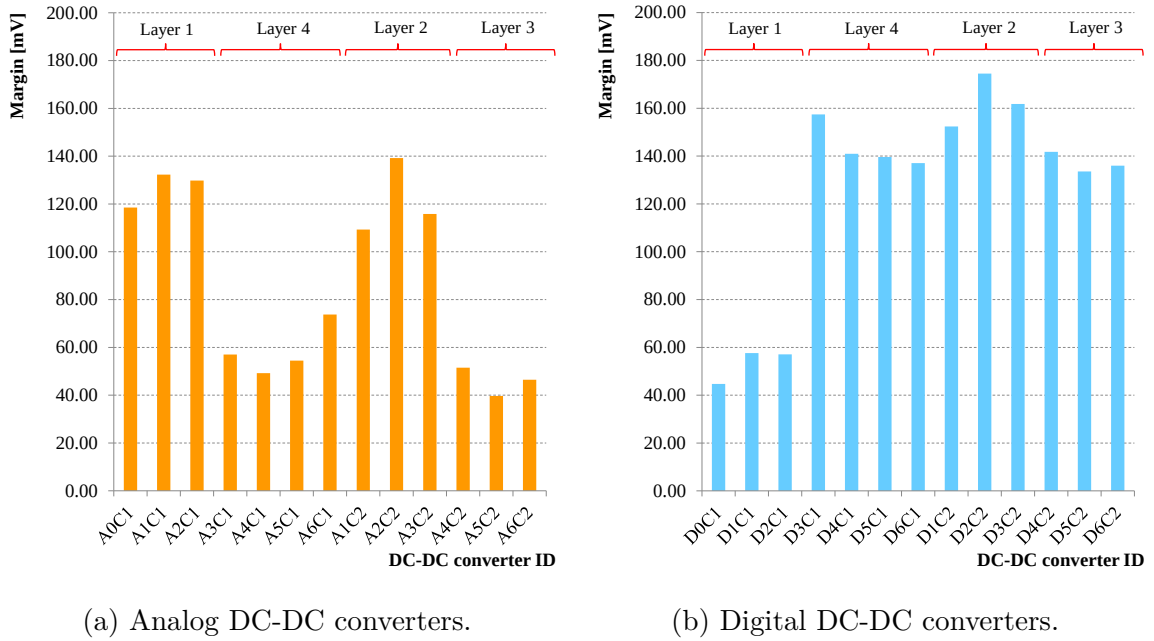


Figure 4.6.: Difference between the actual input voltage at the pixel modules and the lowest allowed input voltage, for which a functionality of the ROC can be guaranteed. The values are calculated for the design instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Output voltages of 2.4 V for analog DC-DC converters and 3.3 V for digital DC-DC converters were used for the calculation.

The measurement of the voltage drops was an essential input for the choice of the DC-DC converter output voltages. When the power system was designed, the initial requirement for the digital voltage was to be greater than 2.2 V. Tests with the final version of the readout chips revealed that this requirement had to be increased by 0.2 V [43]. The measurement of the voltage drops proved that the initially foreseen digital output voltage of 3.0 V would be too low to ensure a stable operation. It was decided to increase the voltage of the digital DC-DC converters to 3.3 V. For layer 2, an even larger voltage of 3.5 V was chosen. This decision was motivated by tests of

psi46dig ROCs that had been irradiated with a dose of 60 MRad. They showed a kind of memory effect, which lead to wrong pulse height measurements [101]. An increased input voltage can reduce the effect. Because modules in layer 3 and layer 4 will not receive this dose during the lifetime of the detector, the voltage was increased only in layer 2.

4.4. Transient Response

The pixel detector will undergo many power cycles during its lifetime. For example, the detector may be shut off during technical stops, or for safety reasons when the LHC is in some specific machine modes. A shutoff can also be triggered by the interlock system in case of a severe problem in CMS or the LHC. It is therefore important to ensure that all power-up and power-down procedures are safe for the power system and the pixel modules. The main risks are voltage spikes, which can be potentially dangerous for the pixel modules. It also has to be ensured that the pixel detector can be turned back on quickly, especially when the LHC is colliding particles, to keep the dead time low.

The system test setup was used to investigate the transient behavior of the BPix power system. It is possible to predict the behavior of the Phase-1 pixel detector from these measurements because the power supply, the cables, all power-related PCBs, and the DC-DC converters that were used were of the same type as the ones used in the pixel detector. The cables in the system test setup have a length of 43 m, which is comparable to the cable length in CMS.

The measurements were performed with a fully equipped bus board with 13 pairs of DC-DC converters. An electronic load was used to draw different currents from all DC-DC converters. The analog and digital input voltages of one power supply channel were analyzed with an oscilloscope. For this purpose, the input voltages were measured at the connector of the bus board. The input currents were measured with current clamps. At the same time, the output voltages of four DC-DC converters were monitored with a second oscilloscope.

4.4.1. Power-on Procedure without Load

The behavior of the system when the power supplies are switched on was investigated. No currents were drawn from the DC-DC converters in this measurement. Figure 4.7 shows the power-on procedure. The top part shows the input voltages and currents for the analog and digital part of the first power supply channel. The output voltage of two analog and two digital DC-DC converters from this power group are shown on the bottom. The first channel of the power supply was switched on while the second channel was already powered on and in a stable condition. The DC-DC converters are

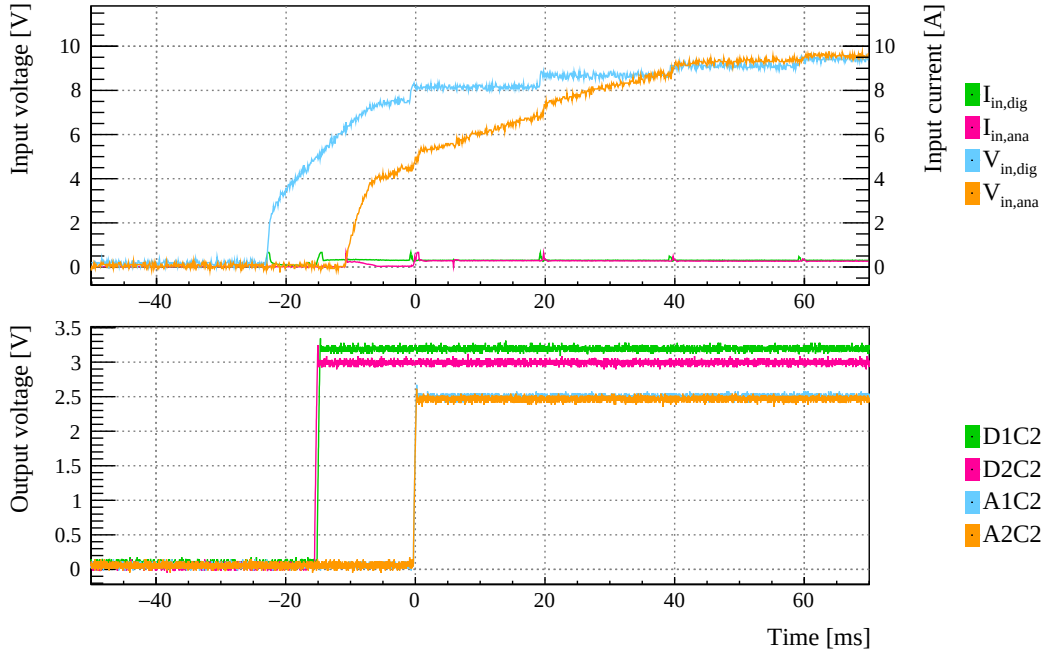


Figure 4.7.: Power-on procedure without any currents drawn from the DC-DC converters. The input voltages and the power supply currents of the first power channel are shown on the top. The output voltages of four DC-DC converters are shown on the bottom.

enabled by default. They were not disabled in this measurement. Hence all DC-DC converters turned on when the input voltage increased above their undervoltage-lockout (UVLO) threshold of about 4.8 V.

When the power supply is turned on, the digital voltage increases to 7.5 V within 22 ms. It then ramps up in steps of roughly 0.5 V every 20 ms. The analog voltage is turned on with a time delay. It reaches the UVLO threshold about 15 ms after the digital voltage. This time difference is relevant because the readout chips should not be operated with only one of the two low voltages. However, the time difference measured here was considered uncritical. The DC-DC converters regulate successfully and fast enough so that the steps of the input voltage are not visible in the output voltage of the DC-DC converters. A short voltage spike of less than 200 mV is visible when the DC-DC converters switch on. This is expected and is caused by the soft-start procedure of the DC-DC converter itself. A few inrush current spikes of about 0.7 A, twice as large as the static current, are observed for the analog and the digital voltage. Nevertheless, this current is small compared to the expected static current of several amperes during detector operation.

4.4.2. Power-on Procedure with nominal Loads and enabled DC-DC Converters

These observations no longer apply if a large load is connected to the DC-DC converters. Figure 4.8 shows the same power-on procedure, but with the design currents (Section 4.2) drawn from all DC-DC converters. In contrast to the previous measurement, the DC-DC converter switches on and off repeatedly when the voltage is around 4.8 V. The reason is that as soon as the converter starts to deliver output power, the input voltage drops, and the Undervoltage-Lockout of the FEAST2 ASIC switches the DC-DC converter off. This increases the input voltage again, and the converter switches back on. The procedure repeats for several microseconds until the power supply has ramped the input voltage to a larger value. During this period, the output voltage of the converter has a ripple in the order of 1 V. However, the output voltage does not increase above the nominal value. Hence the pixel modules are not at risk.

Large inrush currents are observed at the moment the DC-DC converters are switched on, when the input voltage is not yet at the nominal value. The peak value of the digital current in Figure 4.8 is 10 A. This is almost twice as large as the static current of about 5.2 A at an input voltage of 10 V. The large current is caused by the low conversion ratio when the input voltage is around 5 V. The input current of a DC-DC converter depends on the output current I_{out} drawn by the pixel modules, the input and output voltages V_{in} and V_{out} , and the conversion efficiency ϵ :

$$I_{\text{in}} = I_{\text{out}} \cdot \frac{V_{\text{out}}}{V_{\text{in}}} \cdot \frac{1}{\epsilon} \quad . \quad (4.3)$$

When the DC-DC converter turns on at around 4.8 V, it delivers the nominal output voltage and the nominal output current. According to Equation 4.3, the input current is expected to be about two times larger compared to the nominal operation at 10 V. A large current is potentially dangerous for the fuse on the DC-DC converter PCB.

The PixV13 DC-DC converters, which have been used in the pixel detector in 2017, have fuses rated with 1.5 A. Even in the case of nominal output currents, some DC-DC converters have input currents above the fuse rating during the switch-on procedure. This fact was not taken into account when the fuses had been selected. It will be discussed in more detail in Chapter 5.2.

Although the sustained digital current that the power supply can deliver is 9 A, the over-current protection did not trigger in the measurement presented above, because the trip limit was exceeded only for a short time. There is a risk that, depending on the activity in the detector, the large current at low input voltages could trip the digital channel. In this case, it would not be possible to switch the detector back on. This could happen, for example, if the pixel detector is to be switched on while the LHC is colliding particles.

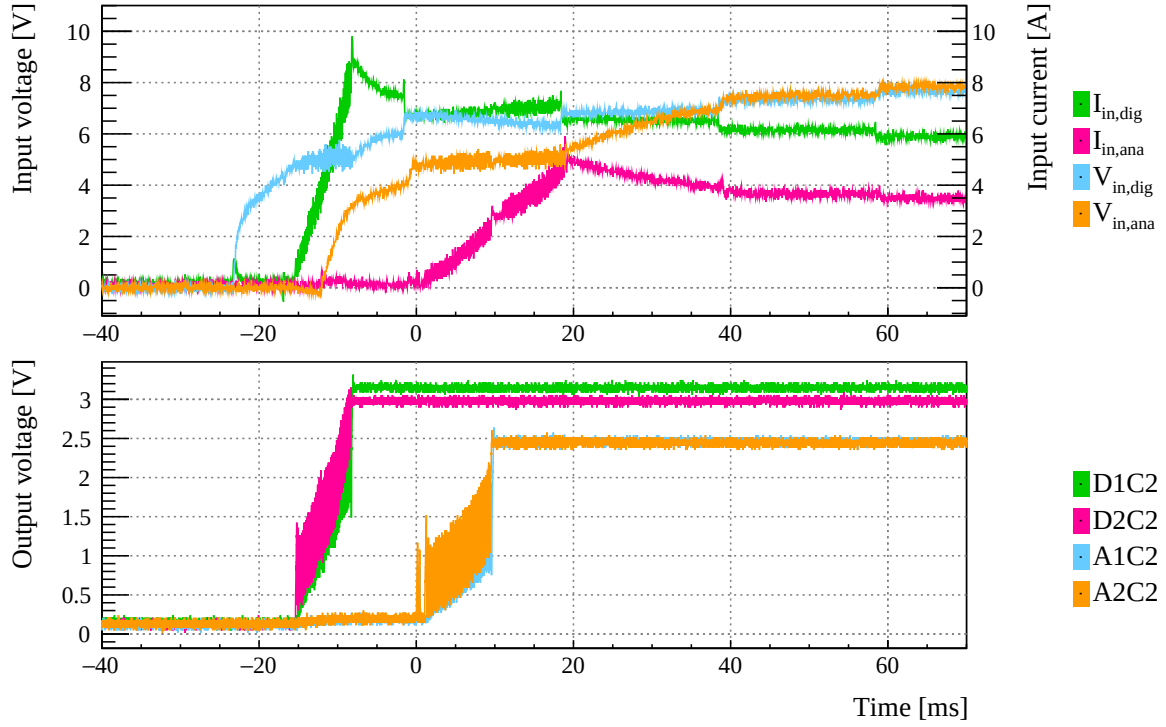


Figure 4.8.: Power-on procedure with nominal module currents drawn from all DC-DC converters. The low voltage is turned on while the DC-DC converters are enabled.

The limits for the detector operation were estimated by increasing the output currents of the DC-DC converters in multiple steps and repeatedly switching the power supply on and off. The system could be reliably switched on up to pixel module currents of 1.1 times the nominal value. For larger loads, it was not possible anymore to turn on the system.

4.4.3. Power-on Procedure with nominal Loads and disabled DC-DC Converters

It should be avoided to power up the low voltage without prior disabling of the DC-DC converters because of both effects described in the previous section, the ripple in the output voltage and large inrush currents. The recommended procedure is to disable the DC-DC converters first by programming the appropriate registers in the CCU ring. Only after that, the low voltage is turned on. When the input voltage has reached the nominal value, the DC-DC converters are enabled. The power-up sequence following this procedure is shown in Figure 4.9. The DC-DC converters switch on properly without any oscillations, and no excessive current is observed. The input voltage is

reduced by about 1.5 V when the DC-DC converters switch on, due to voltage drops on the multi-service cable.

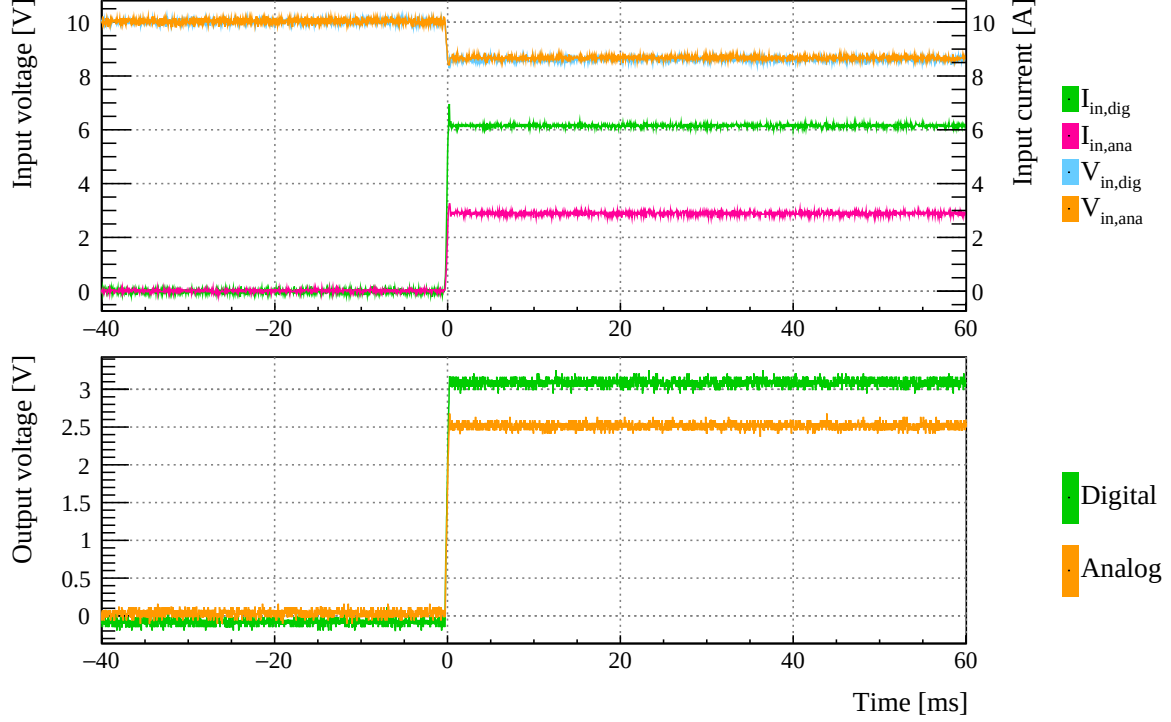


Figure 4.9.: Enabling of all DC-DC converters while the input voltage is already at the nominal value.

4.4.4. Validation of the Remote Sensing Functionality

The power supply has a remote sensing feature that can compensate voltage drops along the multi-service cable. In the BPix detector, the voltage is sensed at the DC-DC bus board. It was investigated if the remote sensing works as expected or if it does interfere with the fast regulation of the DC-DC converters. Such interference could, for example, lead to oscillations in the output voltage of the power supply. There are three important parameters defined as follows:

- V_{set} : set voltage of the power supply
- V_{con} : actual output voltage of the power supply, measured at its connector
- V_{mon} : measured voltage at the DC-DC bus board (= DC-DC converter input voltage)

V_{mon} depends on the voltage drops along the MS cable. It can be calculated with the cable resistance R_{cable} and the current I_{in} drawn by the DC-DC converters:

$$V_{\text{mon}} = V_{\text{con}} - I_{\text{in}} \cdot R_{\text{cable}} \quad . \quad (4.4)$$

Figure 4.10 shows a comparison of the input voltage and input currents at the bus board with remote sensing disabled and enabled. In both cases, the power supply was set to $V_{\text{set}} = 10 \text{ V}$. The DC-DC converters are enabled at the time of $t = 0 \mu\text{s}$, and the nominal currents are drawn. Hence the input voltage drops by 1.5 V. The output voltage of the DC-DC converters is shown in Figure 4.11.

If the remote sensing is disabled, V_{con} equals V_{set} . Due to voltage drops on the MS cable, the input voltage of the DC-DC converters is lower than the set value ($V_{\text{mon}} < V_{\text{set}}$).

With enabled remote sensing the power supply starts to regulate the output voltage after about $320 \mu\text{s}$. It increases the voltage in steps of about 0.5 V, until the nominal value is measured at the DC-DC bus board ($V_{\text{mon}} = V_{\text{set}}$). In this case, the power supply output voltage is above the set value ($V_{\text{con}} > V_{\text{set}}$). It takes about 1.4 s until the system is in a stable state. As expected from Equation 4.3, the input currents decrease at the same time, because the conversion ratio increases. The sensing does not interfere with the fast regulation of the DC-DC converters, as no spikes or increased ripple is visible.

Using the remote sensing feature has two benefits: it increases the maximum available output power of the power supply because V_{con} can be increased above the nominal DC-DC converter operation voltage. Furthermore, the voltage drops along the supply cables are minimized, because the conversion ratio is larger with enabled sensing. Therefore, it is advised to use the feature for the operation of the Phase-1 pixel detector.

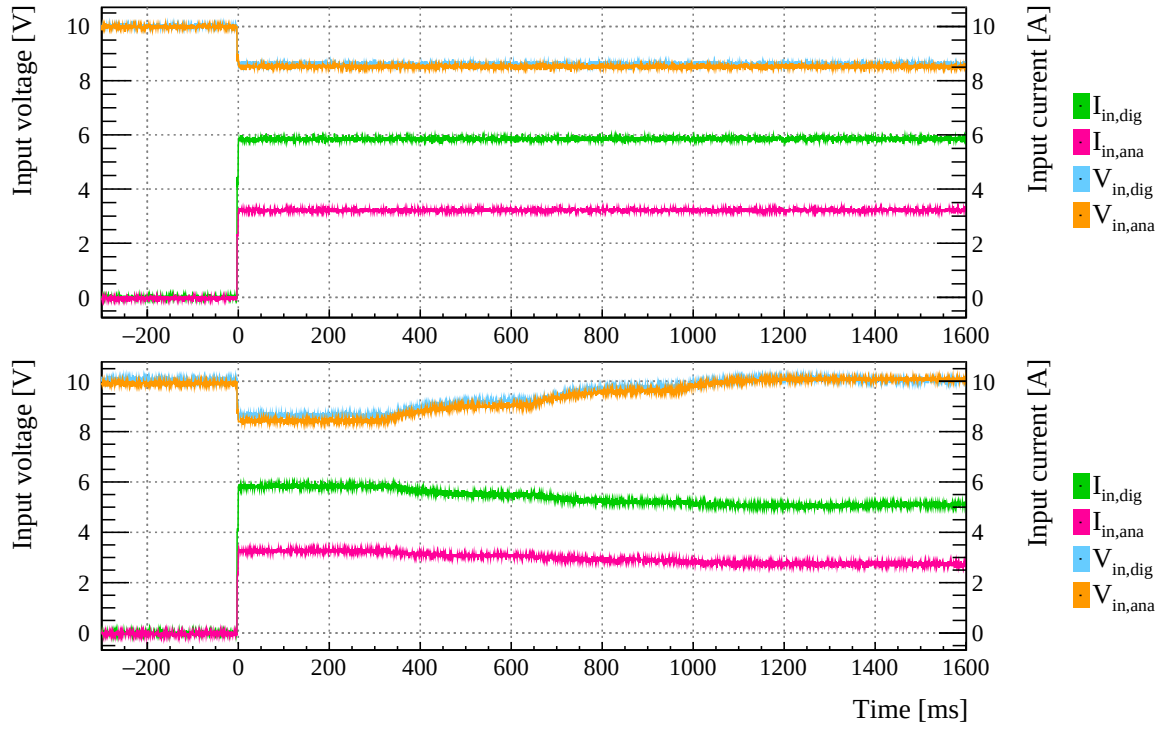


Figure 4.10.: Comparison of the DC-DC converter output enabling procedure with disabled remote sensing (top) and enabled remote sensing (bottom).

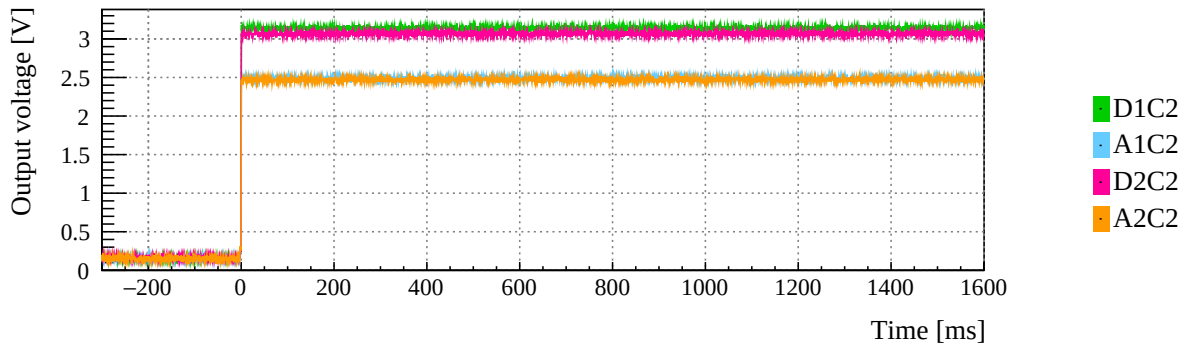


Figure 4.11.: Output voltage of the DC-DC converters in the measurement with enabled remote sensing.

4.4.5. Power-off Procedure

Similar conclusions as for the power-up can be drawn for the power-down of the system. Figure 4.12 shows the input voltage and the input current for the digital power channel. In this measurement, the CAEN power supply was switched off while all DC-DC converters were under realistic loads. The input voltage quickly drops to 4.8 V, where the undervoltage-lockout disables the DC-DC converters. A current spike of almost twice the stable value is observed, which is again caused by the lower conversion ratio.

The current is above the nominal value only for a few μs . This period is smaller as compared to the switch-on procedure. Nevertheless, the current spike could eventually harm the fuses of the DC-DC converters. Instead of just switching off the power supply, it is suggested that the DC-DC converters are disabled first. Figure 4.13 shows the input voltages and currents for one power supply unit and the output voltages of two pairs of DC-DC converters. The DC-DC converters were disabled at $t = 0 \mu\text{s}$. The input currents drop quickly, and no spikes are observed. The same applies to the output voltage.

This measurement demonstrates a drawback of the remote sensing feature. The sensing was enabled during the shut-off procedure. Before the DC-DC converters are disabled, the power supply compensates for voltage drops along the MS cables with a larger output voltage. At the moment the DC-DC converters switch off, these voltage drops disappear abruptly. The input current I_{in} is zero, and according to Equation 4.4, $V_{\text{con}} = V_{\text{mon}} > V_{\text{set}}$. The input voltage at the DC-DC converters increases by about 1 V. It takes about 250 μs until the power supply starts regulating the voltage back down in steps every 320 μs . A too large increase of the input voltage is potentially dangerous for the DC-DC converters. They are rated for a maximum continuous input voltage of 12.3 V [53].

Damage to the DC-DC converters can be avoided in two ways. One way is to choose a V_{set} such that V_{con} never exceeds 12.3 V. An alternative, which allows greater flexibility, is to ensure that no large load changes occur. This can be achieved by disabling DC-DC converters one by one. After a DC-DC converter has been switched off, it is important to wait for the power supply to regulate the voltage back to the nominal value before switching off the next DC-DC converter.

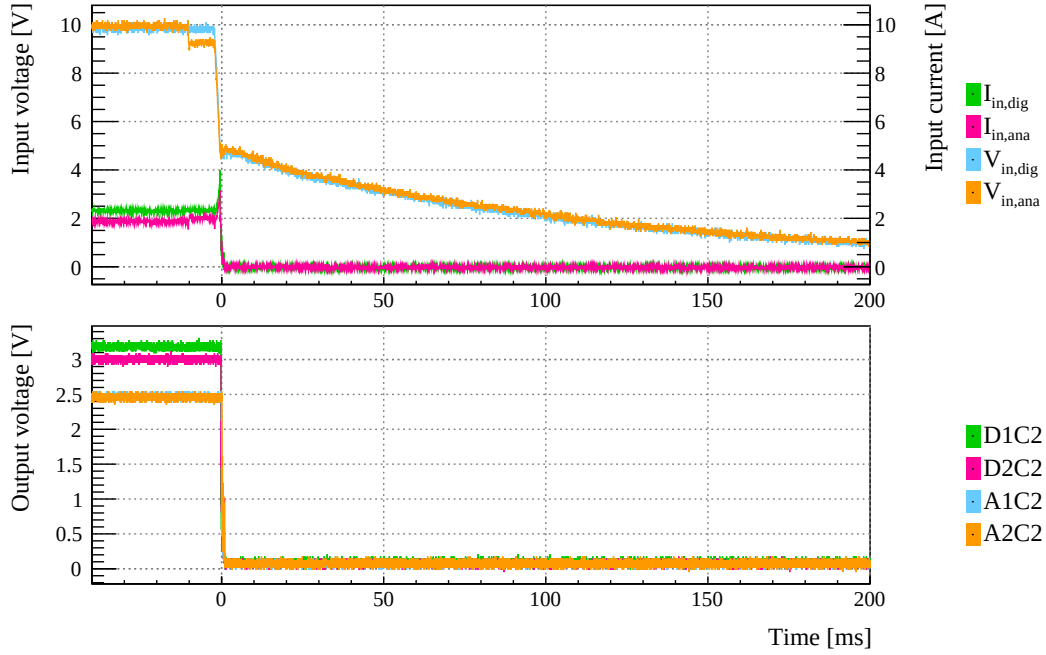


Figure 4.12.: Power-off procedure with nominal loads. The DC-DC converters are not disabled prior to switching off the power supply.

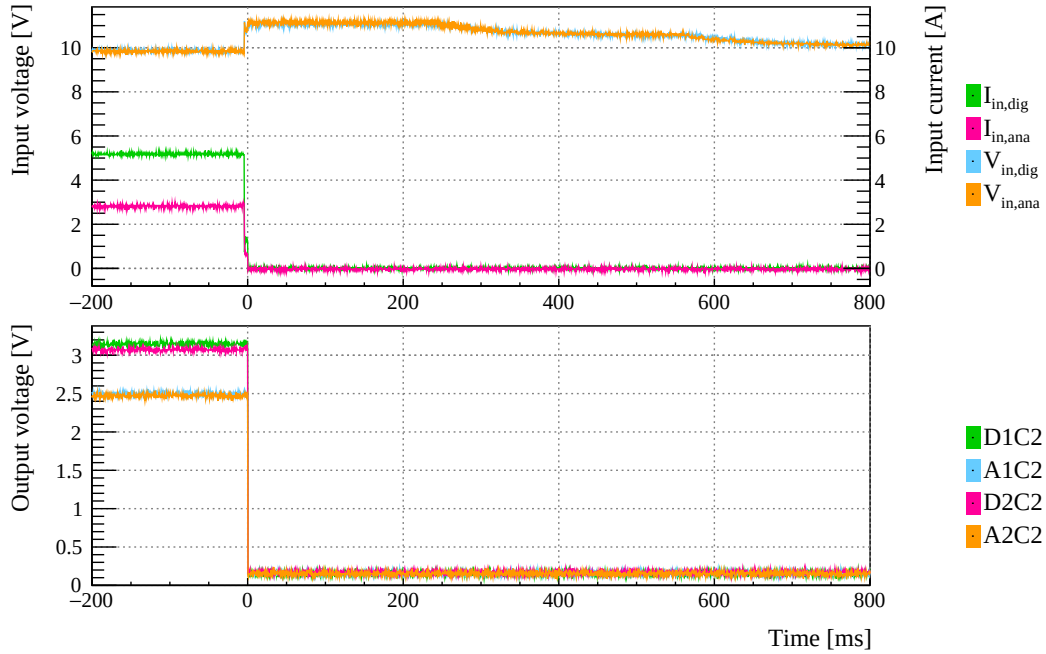


Figure 4.13.: Power-off by disabling DC-DC converters. The power supply remains on while the DC-DC converter outputs are disabled at $t = 0 \mu\text{s}$. The remote sensing feature of the power supply was enabled in this measurement.

4.4.6. Overcurrent Protection

It was tested how the system behaves when the overcurrent protection of the power supply is triggered. In this test, the system was switched on, and the nominal front-end currents were drawn from all DC-DC converters. After a few seconds, the electronic loads were programmed to draw larger currents. This resulted in larger input currents, which exceeded the trip limit of the power supply. The test was repeated for different trip limits and different overcurrent values. An example measurement with a trip limit of 6.0 A and an overcurrent of about 1.5 A is shown in Figure 4.14.

The maximum sustained current that the power supply delivers is limited to the trip value plus a few hundred mA. Thus, the input voltage at the DC-DC converters decreases until the threshold of the undervoltage-lockout is reached. Several converters switch on and off repeatedly, which increases the ripple of the input voltage and the input current. A current spike is observed, which reaches almost up to 14 A in the shown example. The power supply keeps the current at the trip value for the duration of the set trip time (100 ms in this example). If the power supply is still in overcurrent mode after the trip time has passed, all channels (analog voltage, digital voltage and both high voltage channels) are switched off.

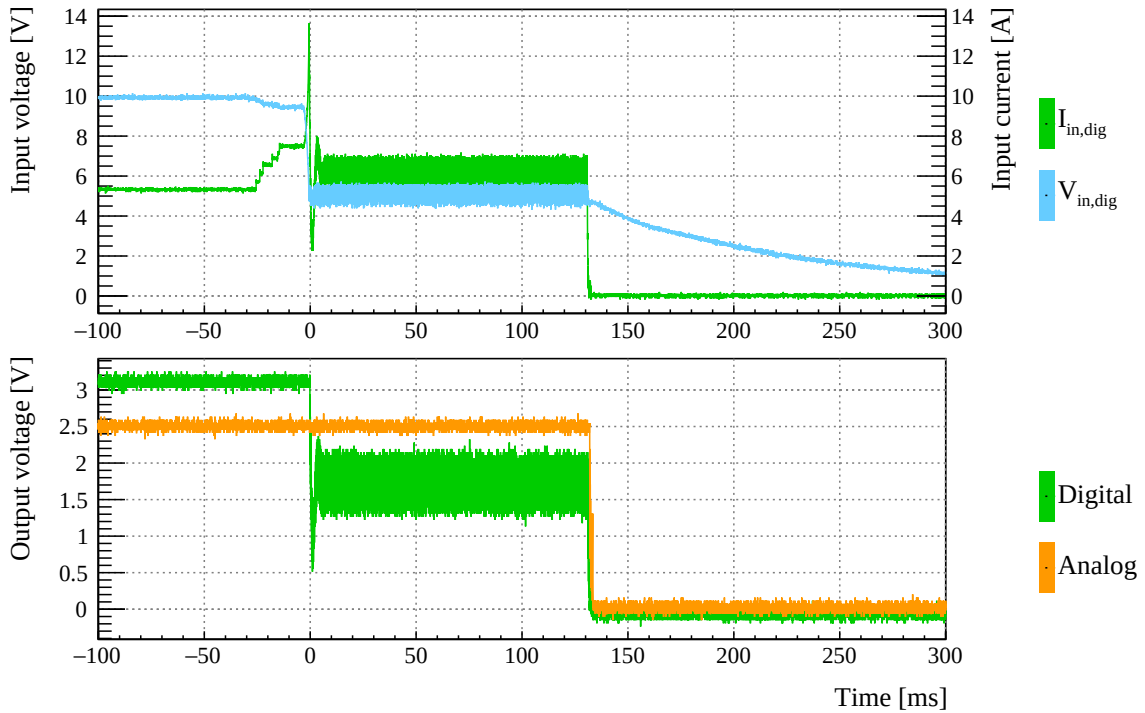


Figure 4.14.: Evolution of the power supply current during a power trip. To bring the power supply into overcurrent mode, the current drawn by the DC-DC converters was increased from 4.5 A to 6.7 A. The trip limit was set to 6.0 A.

As mentioned before, the current spike may be dangerous for the fuse on the DC-DC converter. In contrast to manual power cycles, which can be planned, a trip of a power supply is unpredictable. Thus, the DC-DC converters cannot be disabled first, and the current spike in case of a tripping power supply is inevitable.

4.4.7. Implications of Power Cycles on the Fuses

As mentioned in the previous sections, in case of overcurrents or interlocks the power supplies are turned off without prior disabling of the DC-DC converters. It was verified that the current spikes do not burn fuses. Different test sequences have been implemented in a LabVIEW VI, which are described below.

First, the influence of current spikes that occur when the power supply is switched off was examined. If the power supply is switched off by an interlock, the behavior is the same. The procedure was as follows:

1. Disable electronic loads
2. Switch on the power supply
3. Program loads to draw nominal currents ($L_{\text{inst}} = 2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$) from the DC-DC converters
4. Wait 15 s until the DC-DC converters have warmed up
5. Switch off the power supply

No currents were drawn from the DC-DC converters during switch-on to examine only the influence of the switch-off. This procedure was repeated for 10 000 times and again for 4000 times with a 15 % increased load. After the test was finished, all 26 DC-DC converters were still operating.

In the next step, the power supply was repeatedly brought into the overcurrent mode. The procedure was the same as before, except that in the last step the power supply was not switched off, but instead, the loads were programmed to draw currents corresponding to a total input current of 6.7 A. Because the overcurrent limit was set to 6.0 A, the power supply tripped. This test was repeated for 3000 times. Still, no fuse had blown. It was concluded that the fuses could tolerate a sufficiently high number of such current spikes, and no further action was taken.

4.5. Tests with Pixel Modules

Several measurements with pixel modules have been performed in the system test setup. These tests aimed to prove that the Phase-1 power system allows operating the pixel detector without degrading the performance. An adapter cable is used, with which a pixel module can be read out with a digital testboard, while at the same time the module is powered by external power supplies. Figure 4.15 shows a photograph of this setup. All supply tube boards (DC-DC bus board, extension boards, adapter boards, connector boards) and the module cable, which make up a large part of the electrical lines, are prototypes of the final boards. Additional cables with a total length of about 40 cm and an adapter to feed the high voltage into the test board are needed, which are not installed in the detector. These cables are required because the pixel module is read out by the testboard and not the final readout system.

The pixel module was operated in a light-tight cold box, where it was placed on an aluminum plate that was cooled to a temperature of $+17^{\circ}\text{C}$ by a liquid chiller. The module was operated with a bias voltage of 150 V.

All tests presented in this section followed the same scheme. First, a reference measurement was performed. In this measurement, the DTB provided the analog and the digital voltage for the readout chips, and a Keithley 2410 source meter provided the high voltage for the silicon sensor. In the second measurement, the pixel module was connected to a pair of DC-DC converters, and the CAEN A4603D power supply provided the high voltage. The other 12 DC-DC converter pairs on the bus board were powered but had no load connected to their output. In the third measurement, the electronic loads were used to draw the currents that are expected for a luminosity of $2.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ from the other 12 DC-DC converter pairs. From the converter that powered the module under test, the currents corresponding to three other pixel modules were drawn in parallel. This scenario leads to increased voltage drops on the supply tube boards, which decrease the input voltage of the pixel module. In the last step, fast load variations were introduced to simulate the LHC orbit gap structure. The LHC filling scheme foresees several empty buckets, corresponding to a gap of $3.0 \mu\text{s}$ before the first filled bucket, to account for the rise time of the beam dump magnet. This so-called abort gap leads to a lower activity in the readout chips every $89 \mu\text{s}$. This structure was implemented in the system test by switching the electronic loads with a pulse generator, drawing no currents every $89 \mu\text{s}$ for a period of $3 \mu\text{s}$. Fast load variations lead to variable voltage drops along the supply tube, resulting in variable input voltages at the pixel modules. It was studied if this could deteriorate the pixel module performance.

Initially, the tests were carried out with single prototypes of the readout chips, later with full pixel modules. The tests were first performed only with the bus board and the extension boards, and as more components were available, also with the connector boards and the pixel module cable. Here only the results with the complete set of components are presented, which best simulates the situation in the detector.

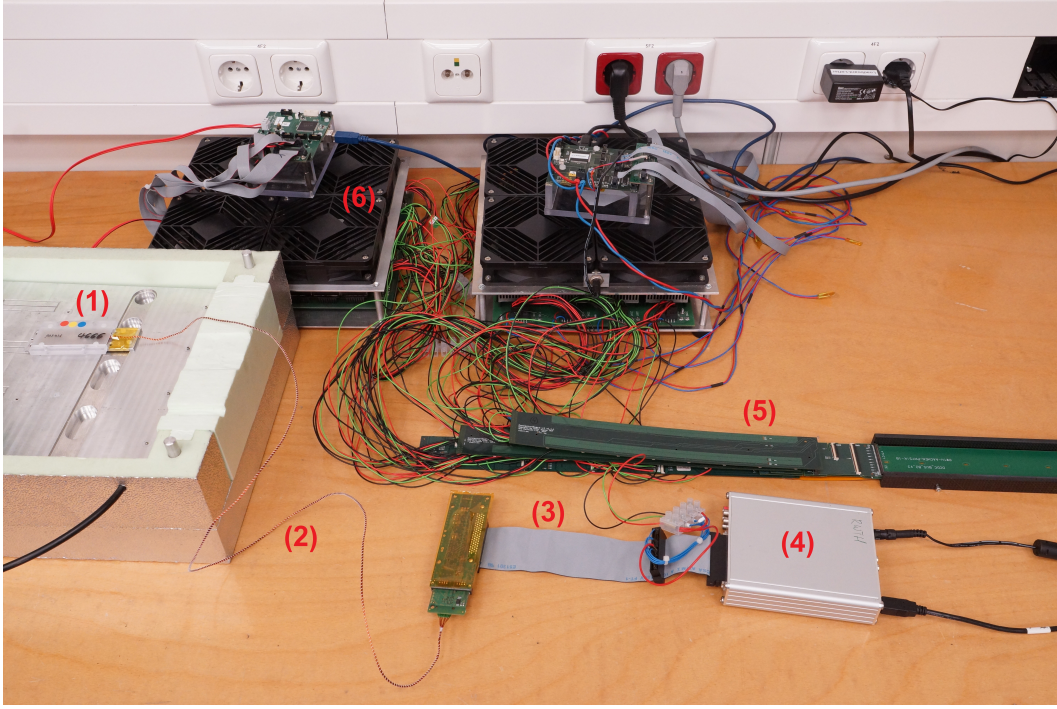


Figure 4.15.: Photograph of a pixel module in the system test setup. It shows the pixel module (1) in the cold box, the module cable (2), the adapter cables (3) and the DTB (4), the supply tube power boards (5), and load boards (6). The DC-DC converters are not visible.

The DAC settings of all readout chips were optimized once (while the DTB powered the pixel module). The same settings were then used for all tests. The optimization was done with the procedures from the pixel module qualification (Chapter 3). The pixel module was trimmed to a threshold of 35 Vcal units, which corresponds to about 1575 electrons.

4.5.1. Noise Measurements

The electronic noise is an essential indicator of the performance of the pixel module. A large noise reduces the resolution of the pulse height measurement and can even lead to fake hits in the readout chip. The noise could be increased, for example, by electromagnetic radiation emitted from the DC-DC converters, or by a ripple on the supply line. To quantify the influence of the power system on the electronic noise, S-curves were measured while the pixel module was operated with the four previously mentioned load scenarios. The S-curve measurement procedure is described in detail in Section 3.3.2.

Figure 4.16 shows the results from measurements with module M4558 from the series production. Using DC-DC converters to power the module did not have any influence

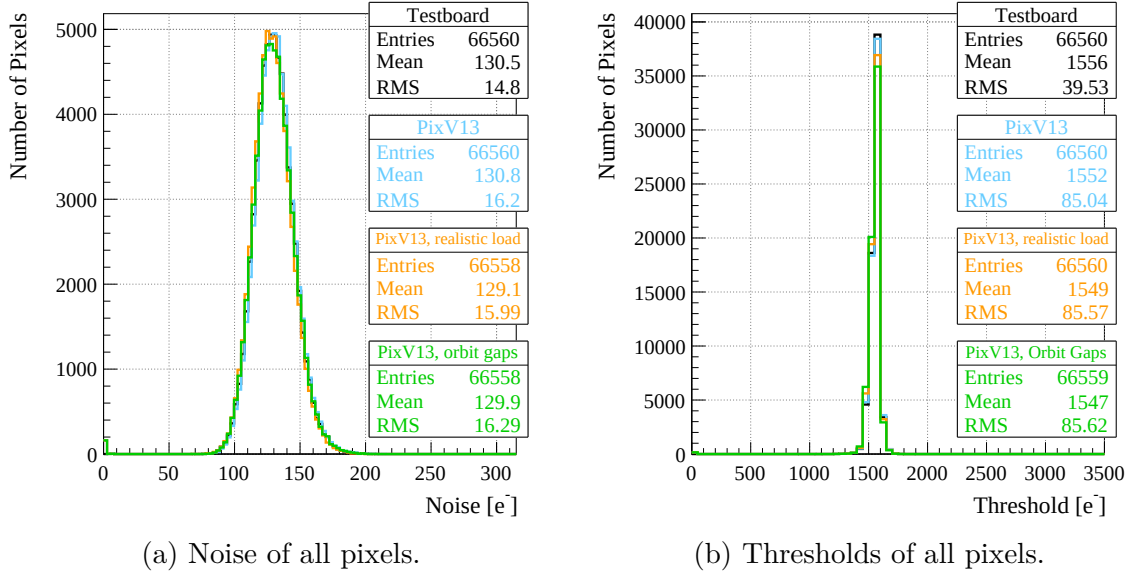


Figure 4.16.: Results from S-curve measurements with module M4558 in the system test setup. The module was either powered by the DTB (black) or by a pair of DC-DC converters. In the latter case, different load scenarios were tested: no currents drawn from other DC-DC converters on the same supply tube channel (blue), nominal loads (corresponding to $L_{\text{inst}} = 2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$) on all other DC-DC converters (orange), and nominal currents modulated with the LHC orbit gap pattern (green).

on the measured S-curves. In the scenario with nominal loads on all DC-DC converters, the pixel module operated with a reduced input voltage. The additional voltage drop was about 350 mV, according to the results from Section 4.3. Nevertheless, the noise and the threshold remained the same. Also, fast load variations due to the LHC orbit gap structure did not alter the performance. In all four measurements, the mean noise was about $130 e^-$, with an RMS of about $16 e^-$. A conversion factor of $45 e^-/\text{Vcal unit}$ was used.

The digital current and thus the voltage drop on the module cable depends on the hit rate. Although in the previous test nominal currents were drawn from all other DC-DC converters, the current drawn by the pixel module itself was below the nominal value at an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. In order to create a higher activity in the readout chip, tests with X-rays were also performed.

4.5.2. X-Ray Measurements

In tests with calibration signals, the pulses are injected at rather low frequencies of up to 100 kHz. The system was also tested with significant activity in the readout chips because the electronic noise and the crosstalk between several pixels increase with the hit rate. One way to achieve a large activity in the readout chips would be to fire multiple pixels of the same ROC at the same time. However, the injected signals would still follow a deterministic pattern. Instead, the pixel module was illuminated with high rate X-rays. The X-ray tube from the module qualification was used for this purpose.

Noise

The noise of module M4558 from the series production was measured under an X-ray hit rate of 100 MHz cm^{-2} . The rest of the setup was identical to the measurement described in the previous section. As a reference, the pixel module was powered by the DTB. In the next steps, power was provided by DC-DC converters, then nominal loads were drawn from all DC-DC converters on the bus board, and finally current variations to simulate LHC abort gaps were introduced. The results from the measurement are shown in Figure 4.17.

Under high rate X-rays, the noise of the readout chip had increased by 40 e^- , compared to the measurement with low activity (Figure 4.16). The difference in the average noise of all pixels was less than 2 e^- between the various powering schemes, except for the LHC orbit gap scheme. Introducing fast load variations increased the average noise per pixel by 9 e^- (5 %). However, this increase does not pose a problem for detector operation, because it is small compared to the signal threshold and the expected signal height of real particles.

The signal threshold increased by about 250 e^- in all four measurements. The same effect was observed in the X-ray tests during series production. Hence, the increase is not caused by the powering with DC-DC converters.

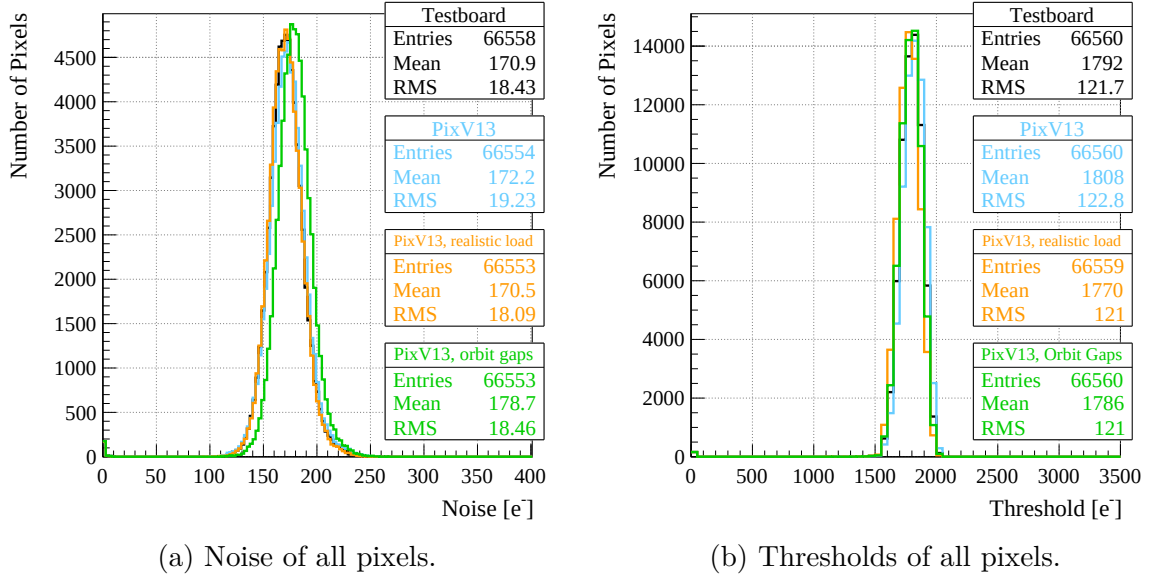


Figure 4.17.: S-curve measurements with module M4558, which was at the same time illuminated with X-ray photons at a hit rate of 100 MHz cm^{-2} . Four different powering scenarios are compared.

Hit Detection Efficiency

The hit detection efficiency is susceptible to noise hits because the primary sources of inefficiencies are overflowing buffers in the readout chip. Hence the efficiency measured under high X-ray hit rates can be used as another benchmark for the system performance. The setup and the measurement conditions for this test were the same as for the S-curve measurement. Only the CalDel DAC settings¹ of all readout chips were optimized before the measurements because they have a direct influence on the measured efficiency. The DAC settings were optimized while the module was illuminated with X-rays at a hit rate of 50 MHz cm^{-2} . The DTB provided the low voltages.

The efficiency was measured with the same method used for the pixel module qualification, which is described in detail in Section 3.4. For each pixel, 100 calibration pulses were injected in the preamplifier. The pixel module was illuminated with X-rays at the same time. The measurement was performed with X-ray tube currents of 0.25 mA, 0.50 mA, 0.75 mA, and 1.00 mA. The hit rates (Equation 3.6) and the efficiencies (Equation 3.10) were calculated per double column. The efficiencies at hit rates of 50 MHz cm^{-2} and 120 MHz cm^{-2} , which are the expected hit rates in BPix layer 3 and layer 2 at the design instantaneous luminosity, were obtained by interpolation between the measured values.

¹CalDel influences the timing of the calibration pulse compared to the trigger signal.

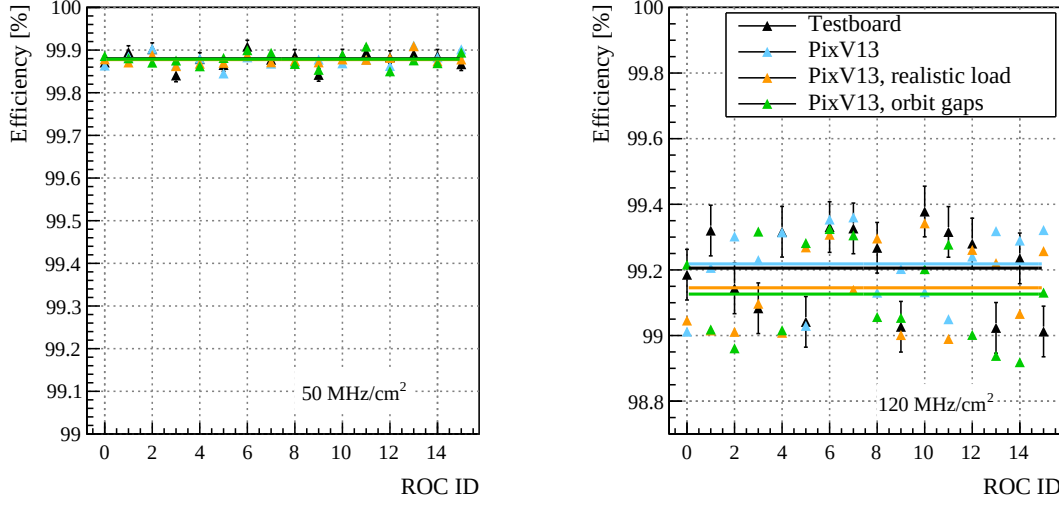


Figure 4.18.: Measured hit detection efficiencies at X-ray hit rates of 50 MHz cm^{-2} and 120 MHz cm^{-2} , shown for all 16 ROCs of one pixel module. The module was powered by the DTB (black), by a pair of DC-DC converters (blue), nominal loads (corresponding to $L_{\text{inst}} = 2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$) on all other DC-DC converters (orange), and nominal currents following the LHC orbit gap pattern (green). The mean values of all readout chips are indicated by solid lines.

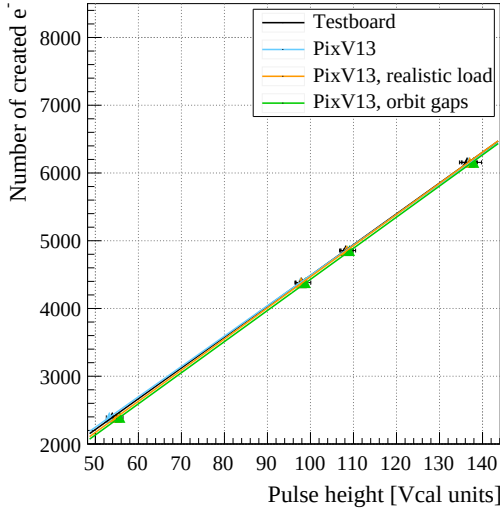
Figure 4.18 shows the interpolated efficiencies of all ROCs of module M4558. The uncertainty of the measurement was estimated with the results of several pixel modules from the series production. For eight modules, the optimization of the CalDel DAC, as well as the subsequent measurement of the efficiency, was performed up to four times. The standard deviation of these measurements was calculated for each ROC. The mean value of the standard deviations of all ROCs is assumed as the measurement uncertainty. It was 0.015% at a hit rate of 50 MHz cm^{-2} and 0.077% at a hit rate of 120 MHz cm^{-2} . For better clarity, the uncertainties are only shown for the measurement with power supplied by the testboard.

At a hit rate of 50 MHz cm^{-2} , the mean efficiency of all ROCs is above 99.8% . The powering scheme does not have any influence. Small variations between the four schemes can be accounted to measurement uncertainties. At 120 MHz cm^{-2} , the mean efficiency is $(99.21 \pm 0.13) \%$ in the reference measurement. The efficiency in the measurement with power provided by two DC-DC converters, but no currents are drawn from the other 12 DC-DC converters, is comparable. In case realistic currents are drawn from all DC-DC converters, the mean efficiency of all ROCs is $(99.14 \pm 0.13) \%$. The introduction of fast load variations does not reduce the efficiency further.

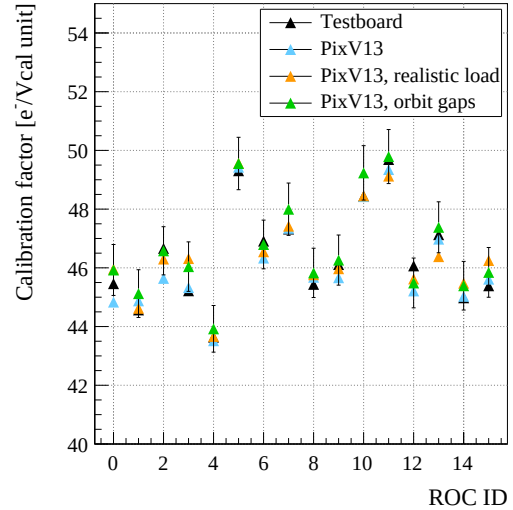
Energy Calibration

It was investigated if the powering influenced the energy calibration with X-rays. The calibration procedure is described in detail in Section 3.4.3. Four different targets, namely Zinc (Zn), Zirconium (Zr), Molybdenum (Mo), and Silver (Ag), were illuminated with X-rays. The pulse height spectra were measured while the pixel module was powered with the four previously mentioned powering schemes. For each measurement series, the number of electron-hole-pairs created in the sensor was plotted as a function of the peak value of the respective spectrum (in Vcal units). The calibration factors were then determined with a linear fit.

Figure 4.19(a) shows the Vcal calibration exemplarily for the first ROC of module M4558 from the final production for the four different powering schemes. Within the measurement uncertainties, which correspond to the uncertainty of the fit value of the energy spectrum, no difference of the measured pulse heights is observed for all four targets. Figure 4.19(b) shows the slope of the fit for all 16 readout chips. The measurement uncertainty corresponds to the uncertainty of the slope of the linear fit. Only the measurement uncertainties of the powering scheme with orbit gaps are shown for better clarity. No significant deviation from the reference measurement is observed. The DC-DC powering does not influence the calibration curve.



(a) Calibration fit, shown for one readout chip.



(b) Calibration constant (slope of the linear fit), shown for all ROCs of one pixel module.

Figure 4.19.: Results from the Vcal calibration with X-rays. Four different powering schemes are compared: DTB (black), a pair of DC-DC converters (blue), nominal loads (corresponding to $L_{\text{inst}} = 2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$) on all other DC-DC converters (orange), and nominal currents following the LHC orbit gap pattern (green).

4.6. The long-term Test Setup

DC-DC converters in the CMS detector have to operate several years with only a low rate of failure because they are not easily accessible and can only be exchanged by opening the detector and extracting the pixel system. Thus it was desired to demonstrate the longevity of the DC-DC converters before the installation into CMS. A setup with one fully equipped bus board with 26 DC-DC converters, which were monitored over several months, was built by the electronic engineering division of the I. Institute of Physics at RWTH Aachen University. Figure 4.20 shows a picture of the setup.

The DC-DC converters were powered with an input voltage of 10.5 V, which was provided by a laboratory power supply. This voltage was 0.5 V above the originally foreseen voltage in CMS. Resistances were connected to the DC-DC converter outputs. The resistor values were 1.0 Ω , 1.4 Ω , and 1.8 Ω , resulting in output currents of 1.3 A to 2.2 A, depending on the output voltage. The DC-DC converters were not power cycled, but were enabled and constantly under load. Their output voltage was monitored once per hour with a custom comparator board connected to a small single-board computer (Raspberry Pi 1 [102]). A water cooling at ambient temperature was used to cool the DC-DC converters.

The setup was commissioned in 2016, when PixV13 DC-DC converters from the mass production became available. Until April 2017, when the pixel detector was installed in CMS, no DC-DC converter in this setup had failed. However, in July 2017, about 18 months after start of operation of the long-term test setup, the first DC-DC converter

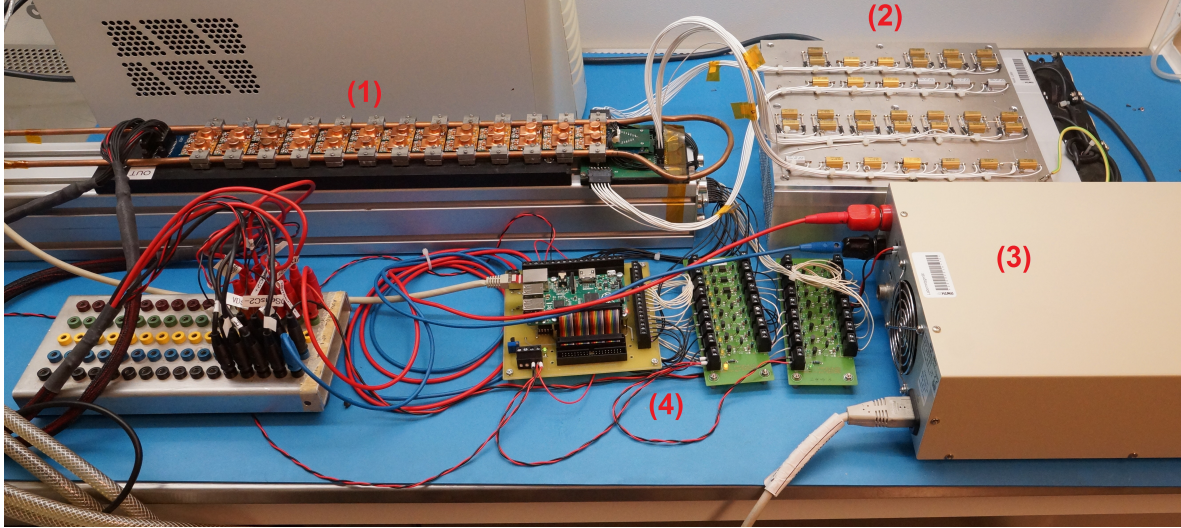


Figure 4.20.: Photograph of the long-term test setup. The picture shows a fully equipped bus board (1), output resistances (2), the power supply (3), and electronics for monitoring of the output voltages (4). The DC-DC converters are water-cooled.

broke because of a blown fuse. The nominal input current of the failing device was calculated to be about 0.6 A, which was much below the rated value of 1.5 A. Within the next few weeks, three more fuses blew. The input currents of the affected DC-DC converters ranged from 0.9 A to 1.1 A. The fuses of the defective devices were replaced to ensure that the FEAST2 ASIC was not broken. With a new fuse, all four DC-DC converters were functional again.

Several tests were performed to find the reason for the failures, and consultation with the manufacturer of the fuses was held. The fuses blew below the rated value because of the high temperatures on the bus board of up to 36 °C. These temperatures lead to accelerated aging, which is explained in the following.

The type of fuse used on the DC-DC converters works by the principle of diffusion. It is made from a layer of copper and a layer of tin on a ceramic substrate. When a high current flows through the fuse, a tin-copper diffusion starts. The electrical conductivity of pure copper is about $\sigma = 58 \times 10^6 \text{ S m}^{-1}$ at +20 °C [103]. The electrical conductivity of a tin-copper alloy decreases with the tin content and is below $\sigma = 10 \times 10^6 \text{ S m}^{-1}$ for a tin content above 5 % [104]. As diffusion progresses, the resistance of the fuse increases until it finally blows.

This type of fuse was chosen because it can operate inside the magnetic field of CMS. Irradiation tests also showed that the fuse was radiation tolerant. However, a disadvantage is that the fuse is by design subject to aging even when operated below the nominal current values.

In order to determine the influence of aging, the still functioning fuses of all DC-DC converters from the long-term test setup were characterized. The voltage drops across the fuses, which is proportional to the resistance, was measured. Figure 4.21 shows the voltage drops across the fuses of digital DC-DC converters used in the long-term test. They are compared to DC-DC converters that were used in the system test setup and also to new (unused) DC-DC converters. For this measurement, the DC-DC converters were operated in the system test setup, and variable output currents were drawn with electronic loads. The resistances of several fuses used in the long-term test (blue) were up to two times larger compared to the ones from the system test (yellow) and new ones (green). The increased resistances are a sign of progressed diffusion.

The diffusion process is highly temperature dependent. Therefore, the aging effect in the pixel detector, which is operated with a coolant temperature of −20 °C, is not as severe as in the long-term test. The diffusion coefficient D can be predicted by the Arrhenius equation:

$$D = D_0 e^{\frac{-E_A}{k_B T}} \quad , \quad (4.5)$$

where D_0 is the maximal diffusion coefficient at infinite temperature in $\text{m}^2 \text{s}^{-1}$, E_A is the activation energy, k_B is the Boltzmann constant, and T is the temperature.

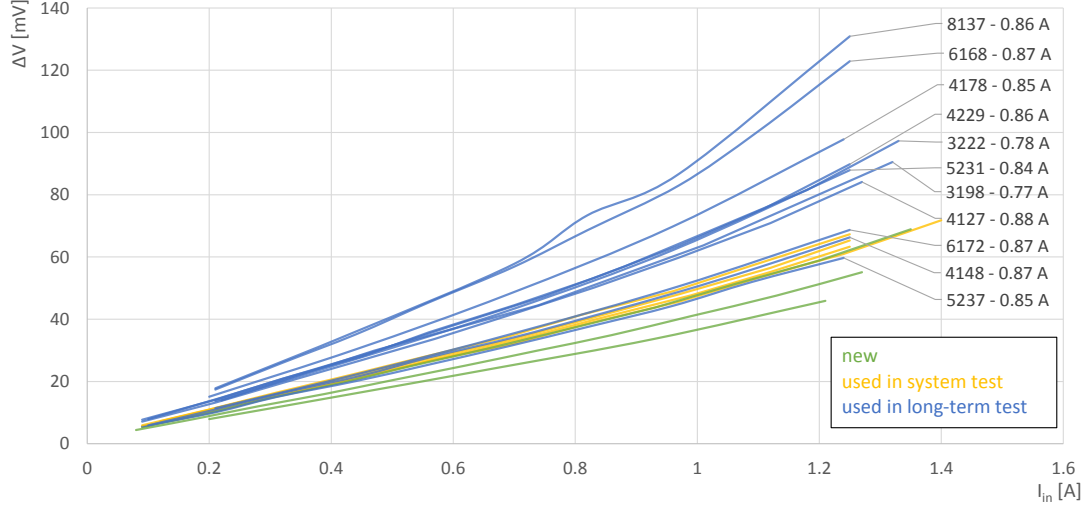


Figure 4.21.: Voltage drop across the fuse on the DC-DC converter as a function of the input current. Each line corresponds to one DC-DC converter used in the long-term test (blue), the system test setup (yellow) or never used for any tests (green). For DC-DC converters from the long-term test, the internal ID and the currents that were drawn in the long-term test are indicated.

The temperature dependence of the diffusion coefficient is thus:

$$\frac{D(T_1)}{D(T_2)} = k = e^{\frac{-E_A}{k_B}(\frac{1}{T_1} - \frac{1}{T_2})} \quad . \quad (4.6)$$

The activation energy E_A depends on the type of intermetallic layers evolving at the copper-tin interface. Also, other possibly mixed metals have an influence. According to the manufacturer, E_A is 0.829 eV, and a temperature drop of 10 K should slow down the aging process by a factor of two [105]. In the long-term test, the coolant temperature was about +30 °C. For the pixel detector, where the coolant temperature is −20 °C, this would translate to a factor of 32 increased lifetime compared to the long-term test.

It was desired to validate the vendor information. For a rough estimate of the activation energy, a measurement reported in the literature [106] is used. In this reference, it has been shown that at the interface of eutectic SnPb solder and a copper substrate layers of Cu_6Sn_5 and Cu_3Sn form. The activation energies are 0.8 eV for the formation of Cu_6Sn_5 and 1.69 eV for the formation of Cu_3Sn . According to Equation 4.6, a temperature reduction of approximately 7 K reduces the diffusion coefficient by a factor of two (at room temperature and for an activation energy of 0.8 eV).

Measurements with several DC-DC converters were performed in the system test setup to estimate the temperature influence. Large output currents were drawn from the DC-DC converters, which resulted in input currents above the nominal fuse rating. It was necessary to accelerate the diffusion process in this way because the aging process is slow and would otherwise not be observable on short timescales. The voltage drop over the fuse was measured with a resolution of $\pm 1 \mu\text{V}$. The increase per time of the voltage drop was used as an indicator for the ongoing diffusion process. The test was repeated at different temperatures to quantify the temperature influence.

Because the resistivity of the fuse depends on the temperature, the measurement was sensitive to temperature fluctuations. The whole bus board was embedded in a sealed aluminum box to reduce external influences. The box, which is described in [107], was made of hollow aluminum profiles, through which cooling liquid (silicone oil) was flowing. In this way the air volume inside the box was kept at a constant temperature, which was always set to the temperature of the CO_2 cooling of the DC-DC converters.

Figure 4.22 shows the voltage drop across the fuse over time for two DC-DC converters. They were operated with input currents of 1.81 A (blue) and 1.56 A (orange). The orange curve corresponds to a DC-DC converter that was used in the long-term test before. Therefore, its fuse had an increased resistance already, and the voltage drop was larger despite the lower current. The large changes in the voltage drop are caused by changes in the CO_2 temperature. The CO_2 temperature was $+20^\circ\text{C}$ at the beginning of the test. It was reduced to -20°C after 24 hours. After 48 hours, the temperature was set to $+20^\circ\text{C}$ again. Finally, the temperature was set to 0°C for another 48 hours.

The voltage drops and thus the resistances constantly increase, although the increase per time is smaller at lower temperatures. The relative increase of the voltage drop over a certain time period t_m is defined as:

$$\frac{\Delta V_{\text{rel}}}{\Delta t} = \frac{V(t_0 + t_m) - V(t_0)}{V(t_0) \cdot t_m} . \quad (4.7)$$

The scaling factor k between two different measurements is defined as:

$$k = \frac{\Delta V_{\text{rel}, T_1} / \Delta t}{\Delta V_{\text{rel}, T_2} / \Delta t} . \quad (4.8)$$

Here T_1 is always the measurement at the warmer temperature and T_2 is the measurement at the colder temperature. The values of $\Delta V_{\text{rel}} / \Delta t$ were extracted for every temperature with a linear regression. Table 4.2 shows the calculated scaling factors k between the three temperatures. The uncertainties have been estimated by dividing each fit region into three subregions and repeating the linear fit. The large uncertainty is dominated by the measurement at low temperature, as there is almost no increase in the voltage drop over time observable.

With the approximation that was given by the manufacturer, factors of 16 and 4 are expected for a temperature change by 40 K and 20 K, respectively. The measured values are compatible with this approximation. The absolute values of the scaling factors may not be directly applicable to the situation in the detector, because this test was done with accelerated fuse aging. Nevertheless, it can be deduced that the aging process in the detector is much slower as the cooling block temperature is about 50 K lower compared to the long-term test. It can be concluded that a safe operation of DC-DC converters in the CMS detector is ensured for several years, as it took 18 month for the first fuse to blow in the long-term test.

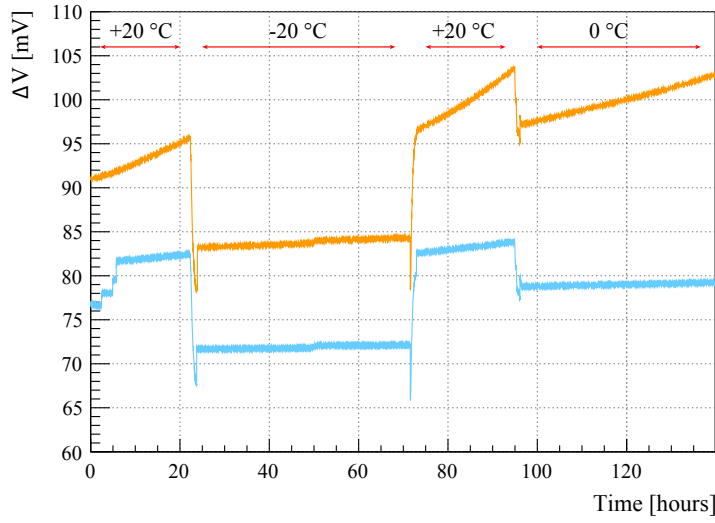


Figure 4.22.: Voltage drops across the fuses of two DC-DC converters over time. One DC-DC converter (blue) was operated with an input current of 1.81 A (blue) and one DC-DC converter was operated with a current of 1.56 A (orange). The set temperature of the CO₂ cooling is indicated.

Table 4.2.: Temperature scaling factors of the relative increase per time of the voltage drop across the fuse, shown for two DC-DC converters. Each scaling factor is calculated between two measurements at different temperatures.

Temperature change	k	k
	DC-DC 1	DC-DC 2
+20 °C → -20 °C	14.0 ± 9.1	13.4 ± 2.9
-20 °C → +20 °C	15.4 ± 10.1	17.6 ± 4.3
+20 °C → 0 °C	5.3 ± 1.1	2.5 ± 0.4

Fuses with a rating of 1.5 A were chosen for the PixV13 DC-DC converters because it is possible to blow them without tripping the power supply, even if the other DC-DC converters of a power group are under load. The fact that aging of the fuses was observable in the long-term test showed that their nominal value was chosen too low. It has been shown that the low operating temperature of the pixel detector significantly increases the lifetime of the fuse. On the other hand, it has been found that the pixel modules sometimes require a higher current than expected (this will be explained in the following chapter). Based on the knowledge of the measurements described in this chapter, it was considered to replace the fuses of all DC-DC converters with ones of a higher rating. However, it was decided that it was not required to extract the pixel detector solely for an exchange of the fuses. Instead, an exchange during LS2 in 2019, when the pixel detector was planned to be extracted for replacement of layer 1, was considered a sufficient safety measure.

5. Detector Commissioning

The integration of the barrel pixel detector took place in Switzerland. After the reception test of the BPix modules had been finished in August 2016, the modules were transported to PSI, where they were mounted on the support structure. All components of the supply tubes were integrated at the University of Zürich. In January 2017, the supply tubes were joined with the detector at PSI. That was the first time the fully integrated BPix detector could be operated. Because the year-end extended technical stop 2016/2017 was already ongoing, the time frame for testing of the detector was limited. It had to be done effectively and in a short time.

In this chapter, the three-stage commissioning procedure is described. Within the scope of this work, contributions to commissioning tests of the pixel detector at PSI and at CERN were made. The second part of this chapter is dedicated to an optimization of the operating parameters of the power system. New standard operating procedures have been developed, and optimized operating voltages of the power supplies were calculated.

5.1. Commissioning of the Barrel Pixel Detector

5.1.1. Overview

At PSI, each half cylinder of the barrel pixel detector was installed together with the corresponding supply tubes in aluminum frames, the so-called installation cassettes. The pixel detector was mounted on wheels in a rail system, which was later used to slide each half of the system into the space between the beam pipe and the strip tracker in CMS. A photograph of one half cylinder and the supply tubes mounted in the installation cassette is shown in Figure 5.1.

At PSI, the detector was operated at room temperature. The tests aimed to find defective components, which at that time could be repaired rather easily because all parts of the detector were accessible. A compact CO₂ cooling system (named CO2Lean) was used to keep the detector at +17 °C. The input voltages for the DC-DC converters and the bias voltage were provided by CAEN A4603D power supplies. The CCUs and the optical components were powered by the CAEN A4602 power supplies. The readout system consisted of the same μ TCA boards that are used for the detector operation. One tracker FEC was used for the detector slow control, a Pixel FEC was used for the

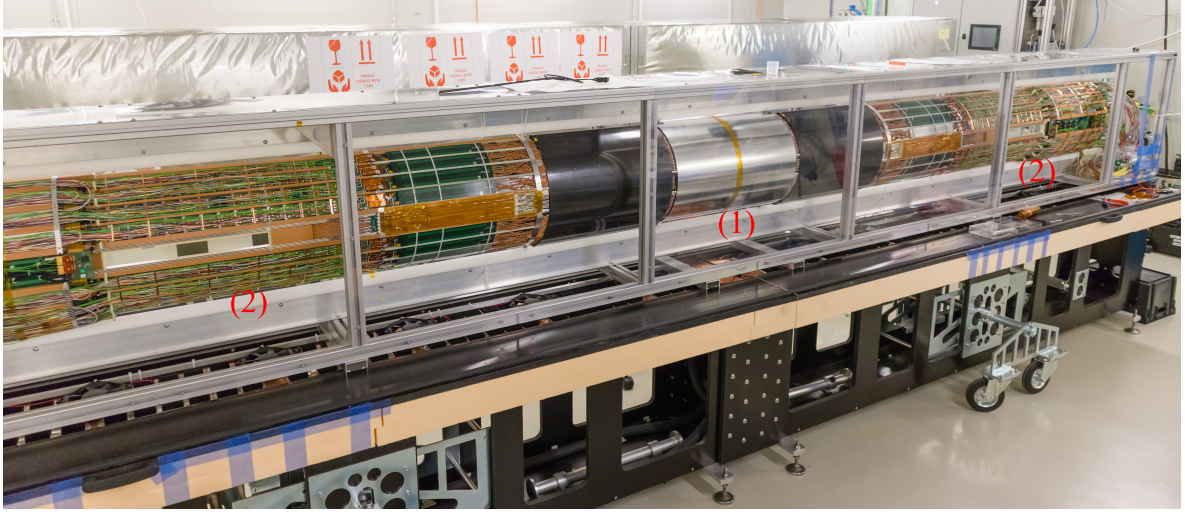


Figure 5.1.: Photograph of one half of the barrel pixel detector (1), which is mounted together with the supply tubes (2) in the so-called installation cassette. The pixel modules are below the shield and are not visible.

module programming and three FEDs were used for the receiving and decoding of the data sent from the pixel modules. One out of 32 sectors of the detector could be tested at a time. The tests were run with a modified version of the Pixel Online Software (POS). This is the standard CMS Pixel Data Acquisition Software, which had already been used for the operation of the Phase-0 detector. The main design concept of the pixel detector remained unchanged, therefore most software changes affected only the readout electronics.

After about three weeks of initial testing, the fully assembled BPix detector was transported to the CMS area at LHC Point 5 at CERN. There the detector was operated at room temperature and, for the first time, at the foreseen CO₂ temperature of -20°C . The power supplies and readout devices were of the same type as the ones that had been used at PSI.

The tests done at PSI were repeated at CERN, and additional optimizations of the module DAC settings were performed. The first half of the barrel pixel detector was installed in CMS on February 28, 2017, followed by the second half on March 02, 2017. The installation was followed by a short initial testing. The FPix detector was installed afterward, on March 07 and 08, 2017. All functionality tests were repeated and the DAC parameters were further optimized to prepare the detector for the operation in 2017. The commissioning procedures and results are described in more detail in the following sections.

5.1.2. Test Procedures

POH Bias Calibration

The amount of light sent from the POHs on the supply tube to the FEDs was optimized. The light level should be just large enough so that the FED receives all signals properly, but as low as possible to reduce the power consumption and heat load. A BPix POH features four laser diodes, which are driven by Linear Laser Driver chips [108]. The drivers bias the lasers with an adjustable constant current and modulate the input signal. The bias was optimized by measuring the signal above the detection threshold of the FED, while the bias current was increased. An example measurement is shown in Figure 5.2. The Received Signal Strength Indication (RSSI), which is a measure for the amount of light above the threshold, increases with the POH bias. Above a certain bias setting the slope of the measured curve increases. At this value all signals are detected, and the further linear increase of the RSSI is only caused by a larger bias current.

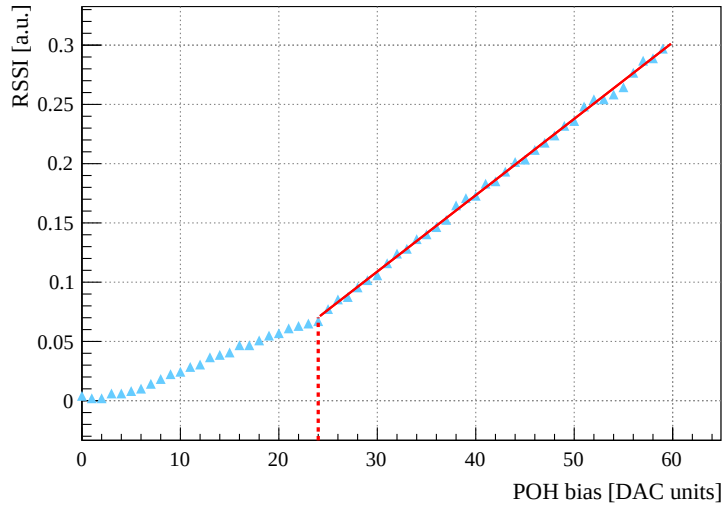


Figure 5.2.: Result of a POH bias scan. The Received Signal Strength Indication (RSSI) is measured by the FED. The red dashed line indicates the optimal value of the POH bias setting.

Delay25 Optimization

In the next step, the communication with the pixel modules was established. The readout chips and the TBMs are programmed using an I²C protocol. The phases between the clock signal (CLK) and the control data (SDA) have to be properly aligned such that the front-end chips can decode the data packets correctly. The settings of

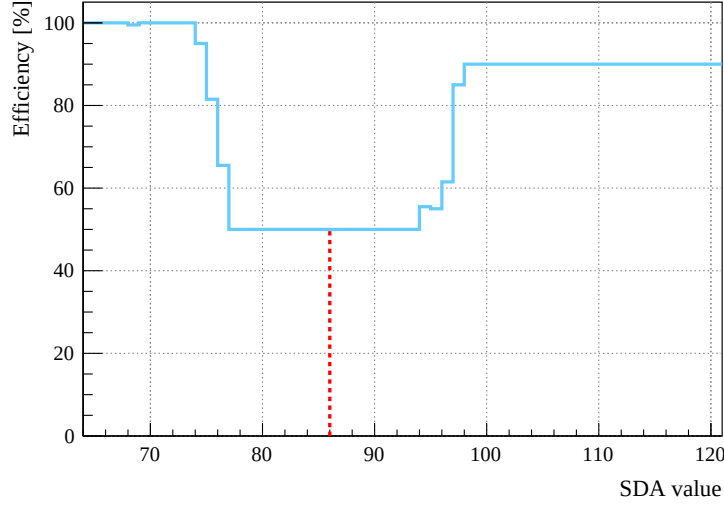


Figure 5.3.: Example result of the SDA scan with layer 1 and layer 2 pixel modules of one BPix sector. In case the TBMs of the attached modules are programmed successfully, the efficiency is 50 %. The optimized SDA value is indicated.

the DELAY25 chips, which are used to adjust the timing of the SDA signals, were optimized. The value of the SDA register was varied in this test. For each step, two triggers were sent to every pixel module, and the TBMs were programmed to ignore every second trigger. The number of valid events registered by the FEDs was counted. A result of such measurement is shown in Figure 5.3. It illustrates the total efficiency of all pixel modules in layer 1 and layer 2 in BPix BpO Sector 6, which has 20 readout channels. In case all TBMs were programmed successfully, the SDA was at a good value. In this case the efficiency was exactly 50 %. A region with good SDA settings was observed, and the center of that region was chosen as the optimal setting. In the shown example, not all TBMs were programmed correctly for SDA values above 94. Most modules remained in a state where they accept triggers. Two channels remained in a state where they no longer accept triggers.

By design, the optimal setting should enable the communication with every pixel module in a readout group because the delay is common to these modules. However, in a few cases, the communication with several modules could not be established with any SDA setting. A method similar to the module qualification was used in such cases to test whether the affected pixel modules could be programmed. The Vana DACs, which set the analog current of the readout chip, were changed for all ROCs on the module. At the same time the power supply output currents were monitored. If the ROCs were programmed correctly, the analog current would change.

If the analog current did not change, the problem had to be investigated further. For example, the optical fibers were cleaned or the module connectors on the supply tube were reconnected. Many of the observed problems were caused by the QPLL ASIC,

which is used to split the LHC trigger and clock signals (Section 2.3.2). When the QPLL did not properly align with the clock signal, the results of the SDA scan were not reproducible. This issue was always resolved by sending a reset signal to the QPLL.

TBM PLL Delay Optimization

The pixel modules were operated with optimized DAC settings that had been obtained in the qualification tests during the series production. It was verified that the modules send out valid data with these settings.

The TBM requires the 40 MHz LHC clock as an input. Internally the chip also works with clock signals of 160 MHz and 400 MHz, which are generated and synchronized with the 40 MHz clock by two phase-locked loop (PLL) circuits. The phases of all clocks have to be properly aligned, otherwise the data sent by the TBM can become invalid or data from readout chips can be missing. For this reason, several programmable delays are implemented in the TBM. It is possible to adjust the phases of the derived clock signals, to delay the ROC data streams, and to shift the TBM Header/Trailer and the readout token by one clock cycle.

The optimal settings of the 160 MHz and 400 MHz phase adjust registers were determined for every TBM. In this test, a 2D-scan of the adjustable phase values was performed. For every combination of settings a fixed number of triggers was sent to the TBM. It was checked whether the TBM header and trailer were found in the data stream. The result of such a measurement is shown in Figure 5.4. If the decoding efficiency was 100 % for the settings obtained from the module qualification, these settings were kept. Otherwise the center of the region with the largest efficiency was chosen and used for all following tests.

It was observed that several modules did not send out valid data after a power cycle. In these cases, the previously optimized settings were no longer valid. The optimization procedure described above had to be repeated several times during checkout, until stable settings were found. The behavior could later be reproduced in lab measurements done at PSI. These measurements showed that if the 400 MHz delay register was set to specific values (0, 4, or 6), the phases of the clock signals might shift after a power cycle [109]. Therefore, it was later avoided to set the delay to these values. For the checkout at CERN the optimization procedure was further modified. Only a one dimensional scan of the 400 MHz delay was performed. Afterward the 160 MHz delay was optimized independently.

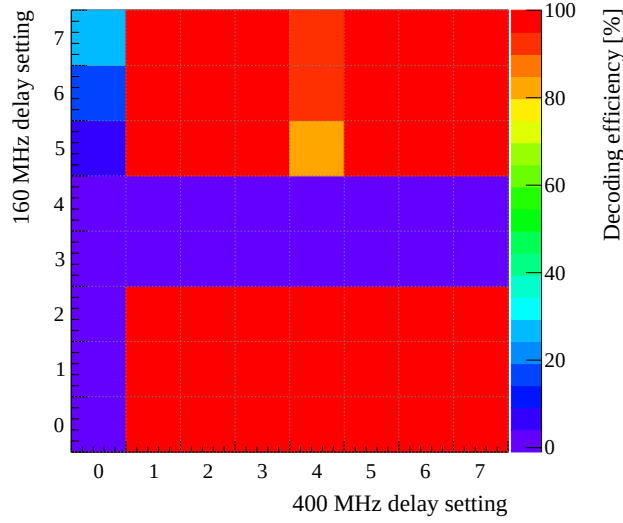


Figure 5.4.: Two-dimensional scan of the TBM PLL delays of one pixel module. The number of events that were properly decoded by the FED is color-coded.

Verification of the High Voltage Connectivity

It was verified that the high voltage was properly connected to the silicon sensors of all pixel modules. The output currents of the power supply could not be used to test individual connections, because in the pixel detector several modules are powered in parallel. Instead, the electronic noise of the pixel unit cells was used as a measure. The noise of a pixel module with an unbiased sensor is increased compared to a biased sensor.

The PixelAlive test (Section 3.3.2) was performed twice, with and without high voltage turned on. Example measurements for one layer 2 module are shown in Figure 5.5. When the high voltage was turned off, some pixels (mainly the large border pixels) became inefficient and showed no hits. If there was a difference between both tests, it was assumed that the sensor was properly biased. If no difference was observed, S-curves were measured to determine the electronic noise. This measurement was also performed with high voltage turned on and off. A comparison of both measurements for all pixel modules of BPix BmO Sector 3 is shown in Figure 5.6. In this sector, the high voltage was properly connected to all pixel modules. The noise was measured for nine pixels on each readout chip. If no difference was observed, the high voltage was assumed to be not properly connected to the pixel module. In this case, all relevant connections on the supply tube were checked and eventually reconnected.

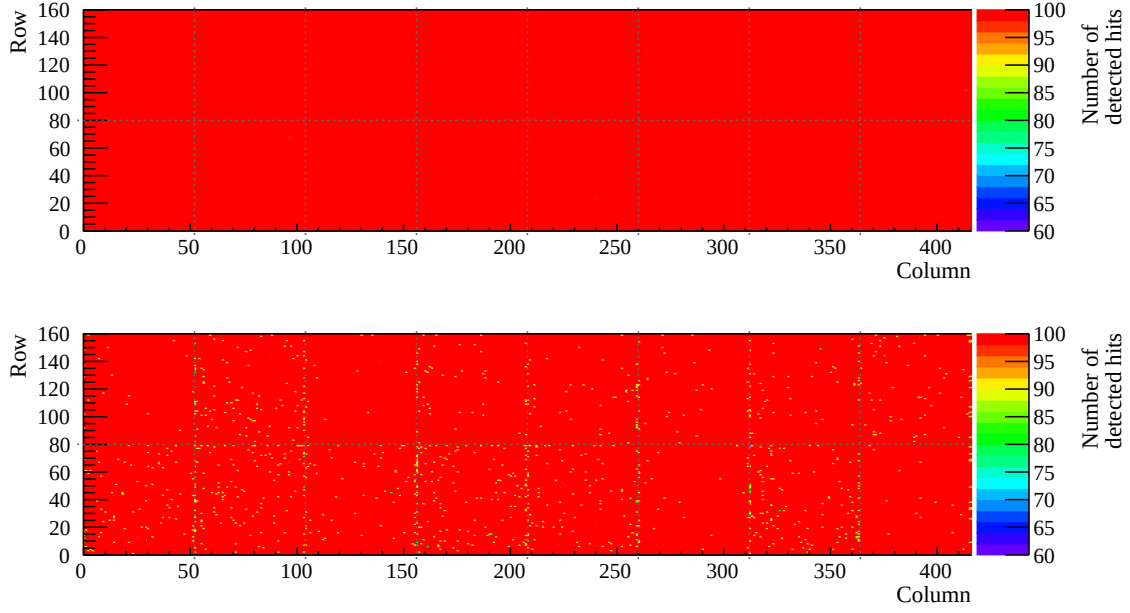


Figure 5.5.: Comparison of the PixelAlive test with sensor bias voltage turned on (top) and with sensor bias voltage turned off (bottom). The number of detected calibration pulses is color-coded.

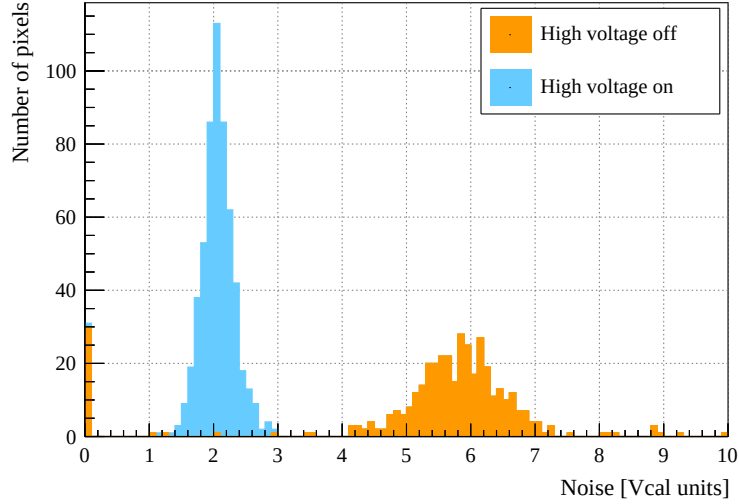


Figure 5.6.: Comparison of the electronic noise of all pixel modules in BPix BmO Sector 3, with sensor bias voltage turned on (blue) and with sensor bias voltage turned off (orange). S-curve measurements were performed for nine pixels per readout chip. The histograms are stacked. For pixels with a noise of zero the S-curve fit failed.

DAC Parameter Optimization

Other DAC parameters which adjust the analog current of the readout chip, the timing of the calibration pulse, and the signal threshold, have been optimized following the same procedures that were used during the module qualification. These procedures are described in Chapter 3. The trim bits of the individual pixels were not changed, because the optimization is very time consuming. The optimized values obtained during the module qualification were kept instead.

5.1.3. Results

When the BPix detector was installed into CMS, about 10 of 1184 pixel modules were not fully functional. It was not possible to replace these modules as they were not accessible without risking other damage. Within a month after the installation, when the whole pixel detector was not accessible anymore, a few more failures developed. These are illustrated in Figure 5.7. The figure was extracted from the CMS Online Data Quality Monitoring tools. It shows the number of hit clusters, measured during a data taking period in June 2017. Each of the four histograms represents a two-dimensional map of one layer of the BPix detector. The number of reconstructed clusters in a certain area of the detector is color-coded. In areas with no or a reduced number of entries, the ROCs or TBMs produce no signals. In ϕ -direction an increased number of clusters at the transition between two pixel modules is visible, because the pixel modules overlap in this direction. On contrast, the eight pixel modules of one ladder do not overlap in z-direction. Therefore, in this direction fewer clusters are reconstructed at the transition between two pixel modules.

In the BPix detector, one power group consisting of layer 2 and layer 3 modules could not be powered anymore. The MS cable was disconnected from the power supply, and the resistance between the analog power line and the return line was measured to find the reason. The circuit was open, meaning that the DC-DC converters did not receive any input voltage. The problem was caused either by a bad connection or by a broken cable inside the detector. As a result, 320 readout chips (1.7% of 18 944 BPix ROCs) could not be powered. In another sector, four pixel modules in layer 3 could not be supplied with the analog voltage because of a defective connection between the modules and a DC-DC converter. A connection between two power boards in section C of the supply tube was broken¹. A third defective connection developed, which left two pixel modules in layer 2 without sensor bias voltage.

Another problem observed was the loss of the programming functionality of one readout group of layer 3 and layer 4 modules. This was caused by a faulty DOH. The problem was related to the temperature in this sector. Above a certain temperature the pixel

¹The weak connection was found when the pixel detector was extracted in the year end technical stop 2017/2018.

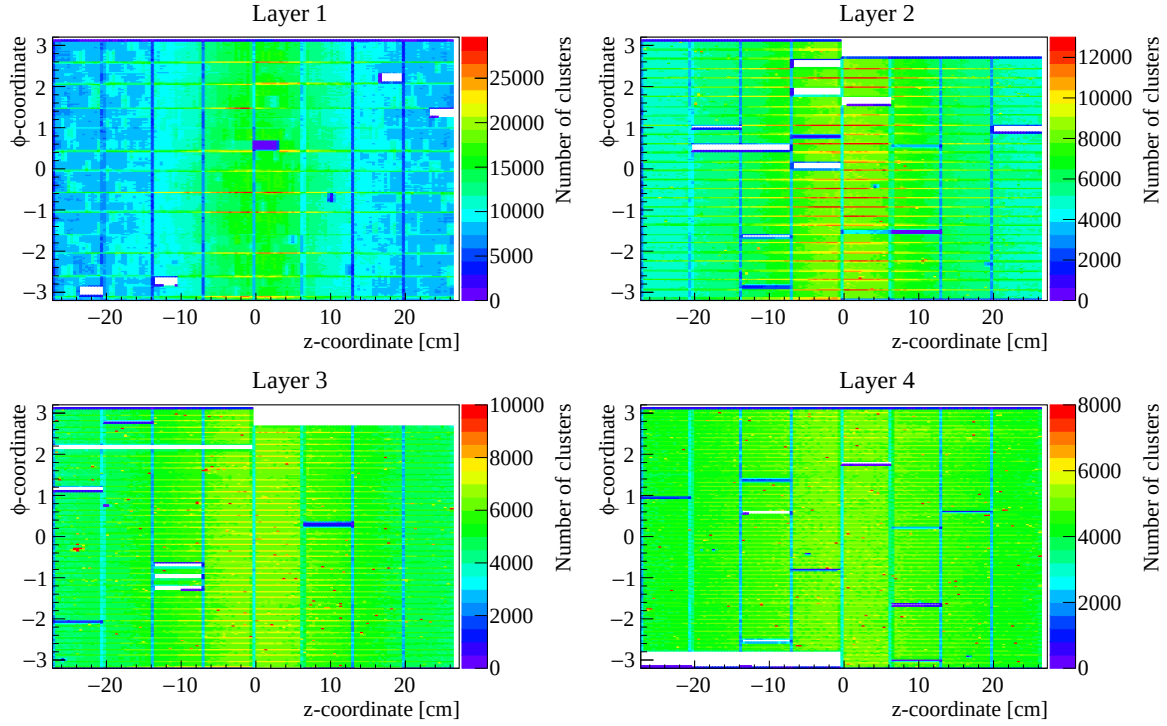


Figure 5.7.: Reconstructed hit clusters during a data taking period in June 2017, extracted from the CMS Online Data Quality Monitoring tools. Each histogram represents one layer of the BPix detector. The number of reconstructed clusters is color-coded.

modules of this group could not be operated anymore. To reduce the heat load in the affected sector, all layer 4 modules (256 readout chips) were disabled. This made a stable operation of at least the layer 3 modules possible.

The insensitive regions caused by the described failures did not overlap in ϕ , except for one sector in which layer 2 and layer 3 could not be powered. Therefore at least a three point coverage was ensured in most parts of the detector.

At the beginning of the 2017 data taking period, about 880 out of 18 944 ROCs (4.65 %) in BPix were masked. The combined fraction of active channels of the FPix and BPix detector was 95.47 %. The fraction is slightly lower compared to the Phase-0 detector, which had an active channel fraction of about 98 % at the end of its lifetime [110]. However, the absolute number of working channels in the Phase-1 pixel detector is almost twice as that of the Phase-0 detector. The new pixel detector is therefore a major improvement.

5.2. Investigation of blown Fuses

During the commissioning tests at CERN, before the installation into CMS, the fuses of four digital DC-DC converters (two in FPix, two in BPix) were blown due to over-current. In the FPix detector, two fuses of DC-DC converters on the same power supply channel were blown. Investigations revealed that the input voltage in the affected channel had been lower than nominal, probably due to a failure of the power supply. Because the output voltage of the DC-DC converters is fixed, this resulted in increased input currents (Equation 4.3 on page 111) of the DC-DC converters. At the same time, a wrong set of DAC parameters was loaded, which lead to an increased power consumption of the pixel modules. As a result, the input currents of the DC-DC converters were above the fuse rating of 1.5 A.

The failure scenario in the BPix detector was different. Just before the BPix detector was transported from PSI to CERN, the structure of the supply tube was reinforced by the installation of additional stiffeners. During this installation the electrical isolation of some pixel module cables was damaged, resulting in short circuits between the power lines and the ground potential. However, some of the short circuits had non-negligible resistances. This condition is the most dangerous, as the following calculation shows.

The FEAST2 ASIC's overcurrent protection prevents output currents greater than about 4 A. At an output voltage of 3.3 V of the DC-DC converter, this output current would correspond to an input current² of about 1.65 A according to Equation 4.3. With a converter that is operated in this state, the fuse would blow after a short time. Measurements have shown that in the event of a real short circuit at the output, the power of the DC-DC converter is limited to about 9 W. In this case the input current would be below 1 A and would not pose a risk to the fuse.

All four DC-DC converters were exchanged before the pixel detector was installed. These events lead to a reassessment of the safety of the power system and new recommendations for the operating voltage and current limits were developed. The results of this study are described in the following sections.

5.2.1. Optimization of the Power Supply Voltage

When the pixel detector was operated, it was found that if the modules are not operated with optimal DAC settings, the analog and digital currents of the readout chips can be twice as large as the nominal value at an instantaneous luminosity of $2.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. This is the case, among other situations, in tests which are used to find the optimum DAC settings. For example, the analog current exceeds the nominal value during the Vana DAC optimization. The digital current exceeds the nominal

²A conversion efficiency of 80 % and an input voltage of 10 V are assumed.

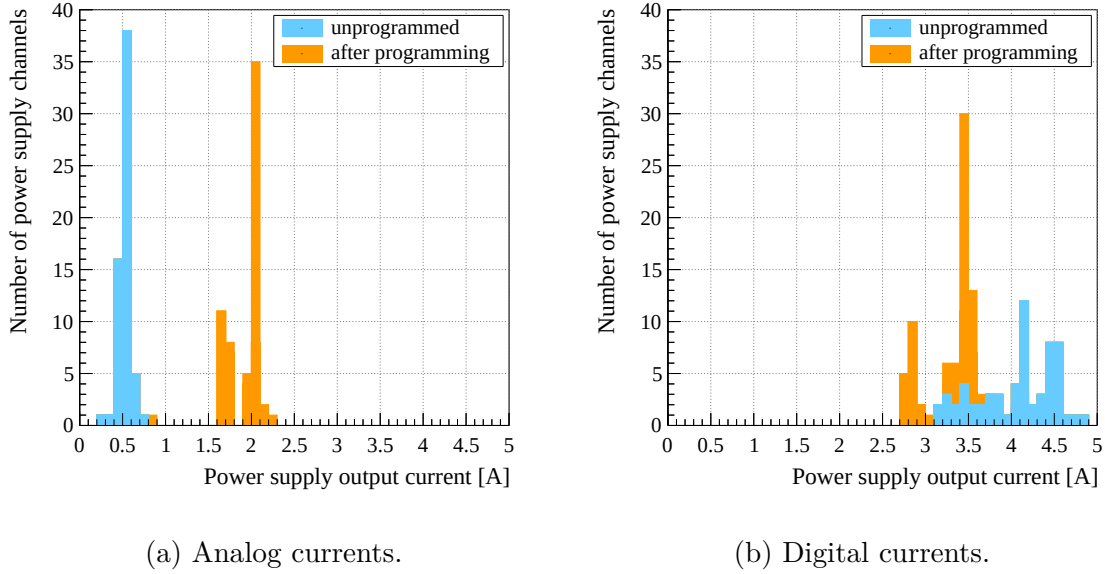


Figure 5.8.: Comparison of the analog and digital power supply currents with unprogrammed pixel modules (blue) and after the DACs of all ROCs have been programmed to the optimal values (orange). Each histogram entry corresponds to one power supply channel.

value if the signal threshold is set too low so that a large number of noise hits occur in the readout chip.

It has also been found that the low-power startup of the pixel modules does not work as expected. As soon as a module is supplied with power, but the DACs are not yet programmed, only the analog current is reduced. However, the digital current may be above the nominal value. This is demonstrated in Figure 5.8, which shows the currents of all BPix sectors³ during a power cycling on April 26, 2017, before and after the DAC settings of the readout chips have been programmed.

The input voltage of the DC-DC converters should be as high as possible to reduce the risk of a fuse blowing, because the input current is inversely proportional to the conversion ratio. On the other hand, the input voltage of the DC-DC converters must not exceed 12.0 V to avoid damaging the FEAST2 ASIC. The optimal output voltages of the power supplies have been calculated for the BPix and the FPix detector. In the calculations shown below, only digital DC-DC converters are considered because the results apply to the analog DC-DC converters as well. The input current of analog converters is always smaller than the input current of the corresponding digital DC-DC converters.

³Except the defective power group BpO 4 layer 2 and 3, which could not be supplied with power.

For a conservative estimate all values were calculated for pixel module currents that correspond to an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The front-end currents of the BPix detector were calculated as described in Section 4.2. The front-end currents of the FPix detector were taken from earlier estimates [111]. Table 5.1 summarizes the assumed values.

Table 5.1.: Estimated output currents of digital DC-DC converters at an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. DC-DC converters in BPix layer 2 serve either 2 or 3 pixel modules.

Layer	Output Current [A]
BPix Layer 1	1.50
BPix Layer 2	1.50 and 2.27
BPix Layer 3	2.54
BPix Layer 4	2.40
FPix Inner Disk	2.32
FPix Outer Disk	2.01

Calculation of the lowest allowed Power Supply Output Voltage

As a first step, the lowest allowed output voltage at the connector of the power supply, $V_{\text{con,min}}$, for which the input current of a DC-DC converter at nominal load is below the fuse limit of 1.5 A, was determined for each DC-DC converter as follows:

$$V_{\text{in,min}} = \frac{I_{\text{out}}}{1.5 \text{ A}} \cdot V_{\text{out}} \cdot \frac{1}{\epsilon} \quad , \quad (5.1)$$

$$V_{\text{con,min}} = V_{\text{in,min}} + I_{\text{in,tot}} \cdot R_{\text{cable}} \quad . \quad (5.2)$$

Here, $V_{\text{in,min}}$ denotes the lowest allowed input voltage and V_{out} is the nominal output voltage of a DC-DC converter. The output current I_{out} of each DC-DC converter corresponds to the according value in Table 5.1. The term $I_{\text{in,max}} \cdot R_{\text{cable}}$ accounts for voltage drops across cables between the power supplies and the DC-DC converters.

The resistance R_{cable} of the BPix multi-service cables in the Phase-0 detector has been measured. Because the cables were not changed, these measurements [94] could be used to calculate the voltage drops for every sector of the Phase-1 detector individually. For the FPix detector, the nominal resistances [112] were used to estimate the voltage drops. It was taken into account that the sense wires in FPix are connected to the filter boards, and that there is another voltage drop across the twisted pair cables that connect the filter boards to the DC-DC motherboards. Therefore, the voltage drop

across the multi-service cables is sensed, but the voltage drop across the twisted pair cables is not sensed.

The current $I_{\text{in,tot}}$ is the sum of the input currents of all DC-DC converters on the same power supply channel. Because several DC-DC converter could be operated at the fuse limit at the same time, the worst case is assumed for the calculation. In BPix, this corresponds to the current at the power supply limit (9 A), and in FPix this corresponds to the current when every converter is operated at the fuse limit ($4 \cdot 1.5 \text{ A} = 6 \text{ A}$). Figure 5.9 shows the calculated worst case voltage drop across the supply cables for all power channels of the Phase-1 pixel detector. The large spread for BPix is mainly caused by the variable cable length of 30 m to 44 m.

Equation 5.1 has to be calculated iteratively because the conversion efficiency ϵ depends on the input voltage. The efficiency of PixV13 DC-DC converters has been measured [113]. The efficiency at an output voltage of 3.3 V and an output current of 2 A can be approximated as follows:

$$\epsilon [\%] = 87.827 - 0.484 \cdot V_{\text{in}} [\text{V}] \quad . \quad (5.3)$$

In order to calculate the lowest permissible output voltage of the power supply, a conservative estimate is made, as mentioned before. It is assumed that the nominal output currents are drawn by a DC-DC converter, and that the voltage drops on the cables are at their maximum because other DC-DC converters could be operated with currents at the fuse limit as well. Figure 5.10 shows the lowest permissible output voltage of the power supply (V_{con}) for module currents corresponding to an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. DC-DC converter output voltages of 3.4 V and 3.6 V were used for the calculation. These voltages are 0.1 V higher than the nominal values to account for variations in output voltage due to component tolerances.

A power supply output voltage of at least 9.6 V ensures that the input current of all DC-DC converters is below the fuse limit. As a result, the pixel detector could be operated with the originally foreseen setting of 10 V. However, the detector was operated with increased voltages in 2017 to have a greater margin for pixel module currents larger than nominal.

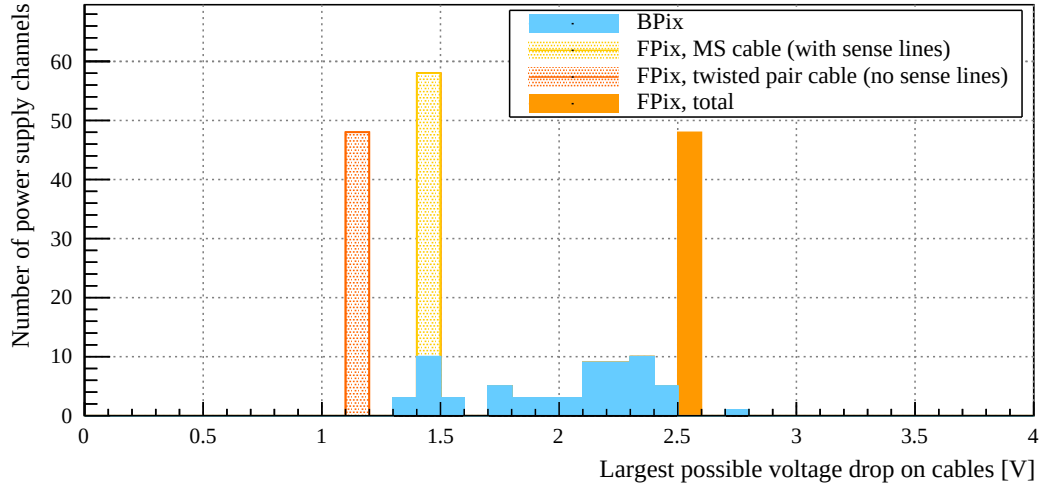


Figure 5.9.: Largest possible voltage drops across the supply cables between the power supplies and the DC-DC converters. The values for all power groups are shown. The assumed currents are 9 A in BPix and 6 A in FPix.

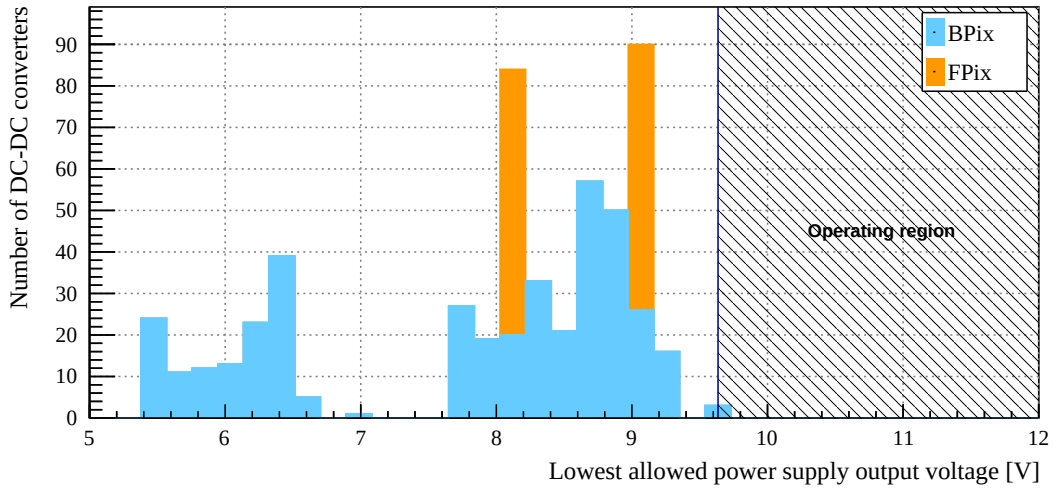


Figure 5.10.: Lowest allowed output voltage of the power supplies, for which the input current of the DC-DC converters is still below the fuse rating of 1.5 A. The values are shown for all digital DC-DC converters of the Phase-1 pixel detector. The calculation assumes an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and the largest possible voltage drops across the supply cables.

Calculation of the optimal Power Supply Voltage

Two possible powering schemes were considered, which are discussed in the following. The power supplies could be operated with remote sensing enabled, or they could be operated with a fixed output voltage. The operation with a fixed output voltage is discussed first.

When the DC-DC converters are disabled, the power supply currents are below 30 mA. Thus, voltage drops along the cables are negligible. When running at a fixed output voltage, the set value of the power supply cannot be larger than 12.0 V, to stay within the specifications of the FEAST2 ASIC. In order to have a safety margin, the output voltage would have to be set even lower. For nominal power supply currents the voltage at the DC-DC converters is reduced due to voltage drops on the supply cables. For example, typical currents in BPix are about 5 A, resulting in a voltage drop of up to 1.4 V (Figure A.8). In this case, the DC-DC converter input voltage would be at 10.6 V, or even lower when a safety margin is ensured or when the power supply currents are higher than expected.

When the remote sensing feature is used, the power supply regulates the output voltage such that the voltage at the DC-DC converter input equals the set value. The power supply can output up to 13.0 V when the currents are large. Hence, the input currents at nominal load are lower compared to the operation with a fixed output voltage. The downside is that sudden load changes from large to low currents may lead to input voltages above 12.0 V at the DC-DC converters. It takes about 600 ms for the power supply to react to load changes. The largest possible load change occurs when all DC-DC converters are disabled at the same time while the instantaneous luminosity is high. This situation can be avoided by disabling the DC-DC converters sequentially and waiting for the power supply voltage to stabilize after each DC-DC converter was switched off. In case of emergency interlocks there is no risk of overvoltage because the power supply is switched off without prior disabling of the DC-DC converters. The largest load change during normal operation occurs when the instantaneous luminosity is high and suddenly the beams are dumped, leading to zero activity in the readout chips. Before the power supply starts regulating, the voltage at the DC-DC converters corresponds to the set voltage plus the difference in voltage drops along the cables between both load situations:

$$V_{\text{in}} = V_{\text{con,load}} - I_{\text{in,idle}} \cdot R_{\text{cable}} = V_{\text{set}} + (I_{\text{in,load}} - I_{\text{in,idle}}) \cdot R_{\text{cable}} \quad , \quad (5.4)$$

where V_{in} is the voltage at the DC-DC converter, $V_{\text{con,load}}$ is the output voltage of the power supply during proton collisions, $I_{\text{in,load}}$ is the sum of all pixel module currents during proton collisions, and $I_{\text{in,idle}}$ is the sum of all pixel module currents when there is no activity in the detector.

The front-end currents that correspond to no activity in the pixel detector were calculated as described before. Figure 5.11 shows the input voltage at the DC-DC converters

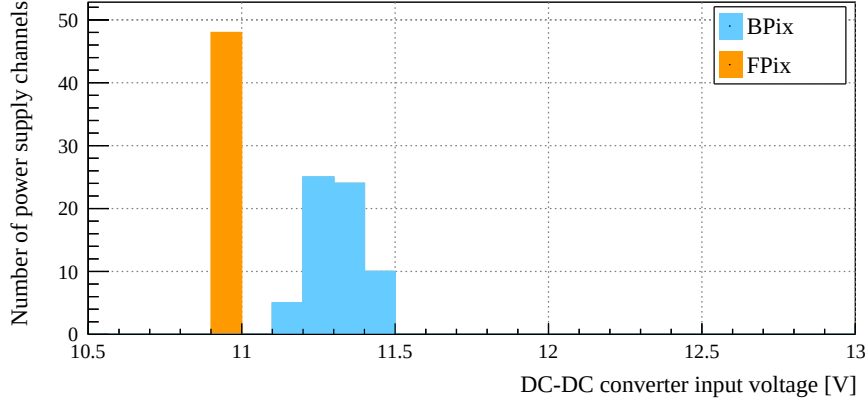


Figure 5.11.: Input voltage of the DC-DC converters in the event that the activity of the readout chips suddenly drops to zero. It is assumed that the instantaneous luminosity changes from $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ to zero and the remote sensing of the power supply is used. The values are calculated for a set voltage of the power supply of 11.0 V in BPix and 11.4 V in FPix.

directly after a beam dump, before the power supplies have started to regulate the output voltage. Set values of the power supply output voltages of $V_{\text{set}} = 11.4 \text{ V}$ in the FPix detector and $V_{\text{set}} = 11.0 \text{ V}$ in the BPix detector were used for the calculation. The input voltage stays below 11.5 V, resulting in a safety margin of 0.8 V compared to the largest allowed input voltage of the FEAST2 ASIC.

Following the above considerations it was concluded that the remote sensing feature of the power supply should be used. Set voltages of 11.4 V for the FPix detector and 11.0 V for the BPix detector were chosen for the operation in 2017. This configuration results in output voltages of the power supply lower than 12.5 V in BPix and 12.3 V in FPix (Figure A.9) for an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, and input voltages at the DC-DC converters below 11.5 V in case of dumped beams at the same instantaneous luminosity. The power-down procedure for regular power downs was changed so that the DC-DC converters are switched off sequentially to avoid large current changes.

5.2.2. Calculation of the Trip Limits

The output current limits have to be set accordingly to make use of the overcurrent protection feature of the power supply. The current limit should be set high enough that no accidental trips happen during normal detector operation but should also be as close as possible to the maximum values, because an increased current of a few hundred mA drawn by an individual converter can lead to the blowing of a fuse.

The power supply currents that are expected during operation at an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and input voltages of 11.4 V (FPix) and 11.0 V (BPix) are shown in Figure 5.12. In FPix all power channels are symmetric. In BPix there are eight sectors in which a DC-DC converter for layer 2 is not connected to pixel modules and eight sectors in which a DC-DC converter for layer 3 is not connected to pixel modules. The power supply currents of BPix layer 1/layer 4 and layer 2/layer 3 are very well balanced and cannot be distinguished in the histogram. The largest currents are in BPix with up to 5.4 A. About 3.6 A are expected in FPix. The input currents of individual DC-DC converters range from 0.56 A (BPix layer 1) to 0.95 A (BPix layer 3). A single DC-DC converter should only be able to draw a maximum current of about 0.5 A higher than the nominal value to stay below the fuse rating. Hence, the advised trip limits are 4.1 A for FPix and 5.0 A and 5.9 A for BPix.

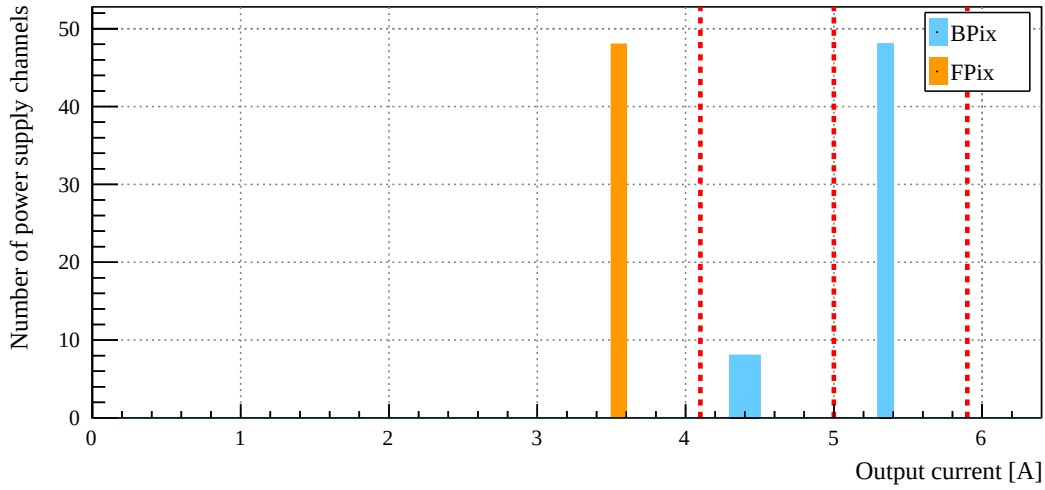


Figure 5.12.: Calculated output currents of all digital power supply channels of the Phase-1 Pixel detector. Set voltages of 11.4 V (FPix) and 11.0 V (BPix) are assumed. The values are calculated for an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The proposed trip limits are indicated.

5.2.3. Operation of the Power System in 2017

Several procedures for the operation of the pixel detector were revised to avoid excessive currents. For calibration tests that involve scans of DAC parameters (for example the Vana calibration) the range of the scans was reduced. It was also ensured that in threshold scans a maximum of four pixels per readout chip are enabled at the same time to reduce the activity of the digital domain of the ROC. The most important change was the implementation of a new power-on procedure, which was developed on the basis of the results of the system tests and calculations described in this thesis.

In the original procedure the auxiliary power for the CCUs and the optical transceivers was switched on first and after that the low voltage for the pixel modules was turned on. Then the configuration (DAC settings, register values) for the whole detector was loaded. For the Phase-1 detector this procedure would result in large currents, because the DC-DC converters are enabled by default and thus the power-on of the low voltage leads to a lower conversion factor and increased currents during the voltage ramp-up. It was also observed that the digital current of the pixel modules that use the psi46digV2 ROC in an unprogrammed state is larger as compared to the programmed state. This behavior was not expected and is in contrast to lab measurements that had been carried out with earlier versions of the readout chip.

In the new powering procedure the auxiliary power is also switched on first. Then the communication with the CCUs is established, and the DC-DC converters are disabled. Only after all DC-DC converters in a sector have been disabled, a software-lock is removed and the power supplies can be turned on. When the output voltage is stable, the DC-DC converters can be enabled one by one. After each DC-DC converter is switched on, a waiting time of a few seconds ensures that the power supply can readjust the output voltage before the next DC-DC converter is switched on. In addition, the DACs of the corresponding pixel modules in BPix are programmed directly after switching on the DC-DC converter in order to set them into a low-current state. This is achieved by maximizing the threshold and disabling all pixels. After the whole detector has been turned on in this way, it is programmed with the DAC settings required for data taking.

A downside of this procedure is that it requires a communication between the data acquisition (DAQ) system and the detector control system (DCS), because the power supplies are controlled by DCS but the communication with the CCU is integrated into the DAQ system. This was not foreseen in the original CMS software design, so several changes had to be implemented by DAQ and DCS experts. Another downside is that the programming of the pixel modules each time a DC-DC converter pair has been switched on is time consuming. It takes about 20 minutes to power-on the Phase-1 pixel detector. This may lead to larger data losses if the whole detector has to be power cycled unexpectedly during LHC collisions. This time requirement is unproblematic if the power cycles can be scheduled.

5.2.4. Operation of the Power System in 2018

A CMS internal safety assessment concluded that the increased input voltage and the optimized operational procedures allow a safe operation of the pixel detector. This was confirmed because only one fuse was blown during the 2017 data taking period, for yet unknown reasons. Nevertheless, it was obvious that with the increased current demand of the pixel modules (in case they are programmed with wrong settings) the DC-DC converters would be operated close to or above the design limit. It was foreseen to replace the fuses of all DC-DC converters with fuses of a higher current rating when

the pixel detector would be extracted from CMS for the next time. This was originally foreseen during the LHC Long Shutdown 2 in 2019 and 2020.

As described in the following chapter, the detector has already been extracted in YETS 2017/2018 and all DC-DC converters have been replaced. The new DC-DC converters have fuses which are rated for currents of 3A (analog) and 4A (digital). This ensures that the overcurrent protection of the FEAST2 ASIC sets in before the fuse is blown for any input voltage of the DC-DC converter. The new fuses only blow if there is a short circuit at the input of the DC-DC converter, as originally foreseen. In the 2018 data acquisition period the DC-DC converters can therefore be operated with lower input voltages. A value of 9 V has been chosen for the analog and the digital power supply voltages.

6. Investigation and Replacement of defective DC-DC Converters

The first proton-proton collisions were recorded with the new pixel detector around June 2017. The main goal of the Phase 1 upgrade, to increase the data collection efficiency at large instantaneous luminosities, was achieved. For example, the inefficiency at an instantaneous luminosity of $1.4 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, which was reached in 2016, has been reduced from about 5 % to about 1 % [114], despite layer 1 of the Phase-1 BPix detector being closer to the beam pipe. In the following months, the operating parameters were further optimized by the shift crew at CERN to even enhance the detector performance. For example, the signal threshold of the pixel modules in BPix layer 1 had to be increased from about 1800 e^- to 2500 e^- because the noise was higher than expected. It was also observed that during data acquisition in proton-proton collisions, an increasing number of pixel modules no longer sends data to the FEDs. This is caused by a problem in the Token Bit Manager (TBM) chip on the pixel modules. A single event upset (SEU) can cause the TBM to enter a state in which it no longer responds to external commands such as triggers. The TBM then remains in this state even after sending a reset command (so-called soft-reset). Only after power cycling of the supply voltage the TBM delivers data again. The probability for such an event to occur depends on the instantaneous luminosity. Pixel modules in BPix layer 1 are affected most, because the particle flux density in layer 1 is almost five times as large compared to layer 2. As the integrated flux increases during a LHC fill, the number of pixel modules that no longer transmit data also increases.

Therefore, at the beginning of data taking in 2017, power cycling of affected pixel modules was performed regularly between two LHC fills. For this purpose, the corresponding DC-DC converter pairs were disabled and enabled again, and the DACs of the readout chips were reprogrammed. Compared to a power cycling of power supplies, power cycling with DC-DC converters allows a more targeted switching off of pixel modules. When switching off a DC-DC converter, only a maximum of four pixel modules are affected. If the power supply is switched off, 19 or 20 pixel modules in BPix and 14 pixel modules in FPix are affected.

Power cycling was initially done manually by the shift crew. Later an automatic power cycling was implemented in the SEU recovery mechanism of the Pixel Online Software. The software monitors how many FED channels do not send data anymore. If a programmable threshold is exceeded, the CMS data acquisition is stopped, and the

DACs of affected pixel modules are programmed. If a module still does not send any data, it has to be power cycled and re-programmed. The data acquisition is continued afterward. In contrast to switching off and on entire power groups, automatic power cycling with DC-DC converters only takes a few seconds because only a small number of pixel modules have to be reprogrammed.

On October 5, 2017, two digital DC-DC converters on the same DC-DC motherboard in FPix produced no output voltage after an automated power cycle. Further three FPix DC-DC converters stopped working after a manual intervention on the same day. At that time no valid explanation for such a large number of failures was found, because no large currents, no temperature fluctuations and no other abnormal behavior of the pixel detector was observed. In the context of this thesis, several investigations were started, which are described in this chapter. In the following weeks more DC-DC converters failed in the FPix detector and also in the BPix detector. No local concentration of defects was observed. Analog and digital DC-DC converters and also one DC-DC converter without any pixel module connected were affected. Until the end of the 2017 data taking period, 61 of 1216 DC-DC converters (5%) broke. It was decided to produce new DC-DC converters and to replace all devices in the Year End Technical Stop 2017/2018 because it was not known how the damage would develop. The production of and the qualification procedures for the new DC-DC converters are described in Section 6.3.

6.1. Failure Investigation

The problem arose that sometimes after power cycling all pixel modules powered by a DC-DC converter pair did not deliver data anymore. At the same time, the output currents of the low voltage power supplies were reduced compared to the state before power cycling. One of the DC-DC converters that was found broken still worked after the power cycling, but stopped producing output voltage a few minutes later. New defects of DC-DC converters were observed also after switching the entire detector off and on again, e.g. during a technical stop. Since the pixel detector was not accessible, the source of error could not be determined immediately. It was considered possible that either the DC-DC converters or the pixel modules were defective, or that the connection between the pixel modules and the DC-DC converters was damaged. Figure 6.1 shows the analog and digital power supply currents of a power group from the FPix detector during power cycling. After the DC-DC converters had been enabled and the pixel modules had been programmed, the currents of both power supply channels were reduced. This is only an indication that the supply voltage was missing. From the data it cannot be determined whether the analog or the digital DC-DC converter is affected, because the absence of one of the two voltages at the pixel module also influences the other current.

Different methods were used to verify that the DC-DC converters did not deliver output voltage. In the FPix detector, the output voltage of DC-DC converters could be measured directly with Detector Control Unit (DCU) chips on the port cards. Most malfunctioning DC-DC converters did not produce any output voltage, but also cases were observed where the voltage was about 1 V.

In BPix, other methods were used to verify that the DC-DC converters were not working, because there are no DCUs installed. For instance, the so-called PowerGood (PG) status was read back. When a DC-DC converter delivers the nominal output voltage, a voltage of about 2.5 V is present at its PG pin. However, it is only possible to read back a combined PG signal of one analog and one digital DC-DC converter, because they are connected in parallel to the CCU. This method leads to ambiguities if only one of the two does not work. The digital logic of the CCU is defined such that below a voltage of 0.7 V at the PG input it returns the status 0. Above a voltage¹ of 1.7 V it returns the status 1. Values in between are not defined. If only one of the converters is not working, the common PG signal is at a value of about 1.5 V, which is within the non-permitted range of the CCU. Therefore, with only one defective DC-DC converter both a PG value of 0 and 1 can be read back. If the value is 0, at least one of the DC-DC converters is definitely defective. If a value of 1 is read back, it cannot be excluded that both DC-DC converters function and that the problem lies elsewhere. The PG bit of all DC-DC converters was read back on a regular basis. In some cases the reading could prove the defect of a DC-DC converter.

Communication with the pixel modules can give an indication whether the analog or the digital DC-DC voltage is missing. If a digital DC-DC converter fails, the entire communication with the pixel modules no longer works. If the analog DC-DC converter fails, the pixel modules can still be read out, but no hit information is generated in the readout chips. In this case it is possible to measure the analog input voltage of the ROCs with their readback mechanism. This method proved to be very reliable and it was possible to determine which DC-DC converter was defective for all power groups in BPix.

¹These values depend on the supply voltage of the CCU. The values given here refer to a supply voltage of 2.5 V.

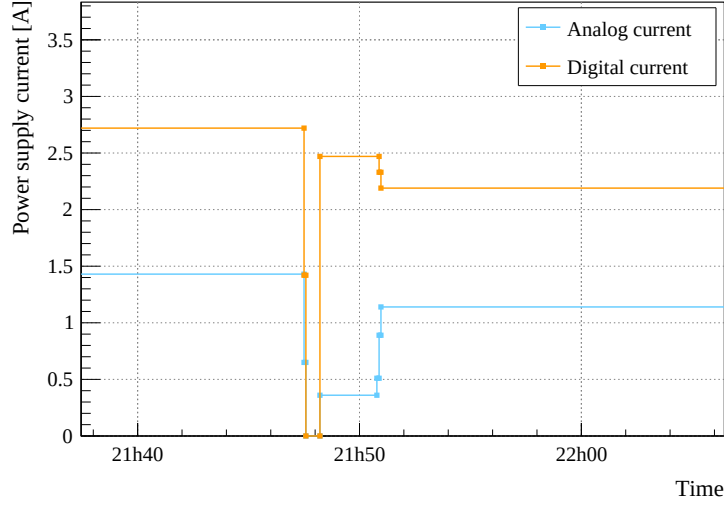


Figure 6.1.: Input currents of one FPix power group with four pairs of DC-DC converters during a powercycle on October 09, 2017. The DC-DC converters were disabled at 21:48 and were enabled again within one minute. The programming of the pixel modules started around 21:51.

6.1.1. Measurements in the System Test Setup

With the available data, it could only be determined that a vast majority of the broken DC-DC converters failed during a power cycling. It was not possible to determine whether the DC-DC converters failed in the switch-off procedure or in the switch-on procedure. In the context of this thesis, several tests were performed in the system test setup (Chapter 4) with the aim to reproduce the behavior in the pixel detector. Some examples will be explained in the following.

Disabling of DC-DC Converters

It was considered possible that the DC-DC converters were not defective, but unintentionally disabled. For 15 DC-DC converters the required disable voltage to switch off the device, and the voltage below it would turn on again, were measured. In this test, DC-DC converters used in the system test setup and in the long-term test setup were investigated. All devices switched off at the expected disable voltage of 0.9 V and switched on again at voltages below 0.7 V. Furthermore, four DC-DC converters that had been irradiated with protons of an energy of 23 MeV at the ZAG Zyklotron AG in Karlsruhe with doses of $2 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$ and $4 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$ were investigated. These DC-DC converters did not show any deviations from the unirradiated ones concerning the disable thresholds.

Since the required disable voltages are much lower than the nominal value of 2.5V generated by the CCU, the theory that the converters are only disabled but not defective was considered unlikely. A fine tuning of the disable voltage would have to take place to switch off only one of two DC-DC converters (analog or digital).

It was investigated whether disabling was harmful to DC-DC converters, because they failed almost exclusively during power cycling. In the system test setup, 26 DC-DC converters were operated over several days. They were disabled and enabled again every 15 seconds via the CCU. For the test, spare DC-DC converters that had not been used for any tests before, converters from the long-term test, and converters irradiated with doses of $2 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$ and $4 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$ were used. None of the devices was defective after more than 10 000 disable cycles.

Test of the Fuse

A method was been developed which can be used to test whether the fuse of a DC-DC converter is blown. Since the fuse is connected in series with the input of the FEAST2 ASIC, no current flows through a DC-DC converter with a defective fuse. For a functioning DC-DC converter, the input current depends on the input voltage and whether the device is enabled or disabled. Below an input voltage of about 4.4 V the first stage of the undervoltage-lockout mechanism of the FEAST2 ASIC prevents switching on. The input current in this state is below about 0.9 mA. Linear regulators, which provide a voltage of 3.3 V to the power transistors, switch on above this threshold voltage. In this state, the input current increases to about 3.3 mA. When the input voltage increases above 4.8 V, the DC-DC converter switches fully on and delivers an output voltage. The current of a DC-DC converter without load is about 40 mA to 50 mA. When the input voltage is above 4.8 V, but the device is disabled, it does not provide any output voltage. However, the linear regulators remain switched on, resulting in an input current of about 3.3 mA also in this state. Table 6.1 summarizes the operation modes.

By measuring the input current as a function of the input voltage (called I-V characteristics), it is possible to determine the state of a DC-DC converter. However, since

Table 6.1.: Expected input current of a DC-DC converter at different input voltages. The values are given for a disabled and for an enabled output of the device.

Input voltage	Input current [mA]	
	disabled	enabled
< 4.2 V	< 0.9	< 0.9
4.2 V - 4.8 V	3.3	3.3
> 4.8 V	3.3	> 40.0

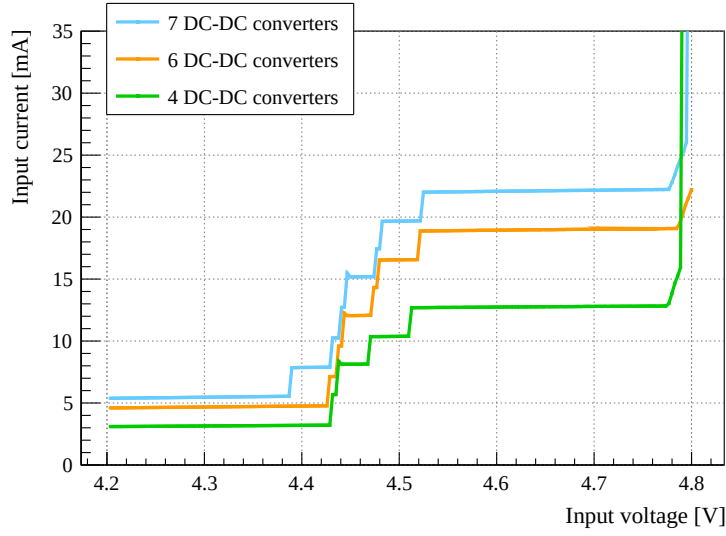


Figure 6.2.: Total input current as a function of the input voltage, measured for seven, six, and four DC-DC converters connected in parallel.

four, six or seven DC-DC converters are connected in parallel in the pixel detector, only the total current of these DC-DC converters can be measured. In the system test setup it was examined whether the method is sensitive enough to detect individual malfunctioning DC-DC converters. The CAEN A4603D power supply cannot provide an output voltage below 8 V, and the measurement accuracy of 10 mA is insufficient. For this reason, the multi service cable was disconnected from the power supply and was connected via an adapter cable to a laboratory power supply (HMP4040) which has a resolution of 0.1 mA. The output voltage was incrementally increased from 0 V to 4.8 V and the current was measured for each step. The measurement was performed for a variable number of working DC-DC converters on the bus board.

Figure 6.2 shows measurements of the total input current of several DC-DC converters as a function of the input voltage. The measurements with four, six and seven functioning DC-DC converters are shown as examples. The regulator of the first DC-DC converter switches on above a voltage of 4.39 V, which is indicated by a current increase of about 2.4 mA. Due to variations in production, not all DC-DC converters switch on at exactly the same voltage. If the voltage steps are sufficiently small (in this case 30 mV per step), the switching on of each individual DC-DC converter can be observed. The number of functioning DC-DC converters can be determined by counting the steps. If the resolution of the current measurement is in the range of about 0.5 mA, the number of DC-DC converters with a functioning fuse can also be determined from a single measurement of the current for example at 4.2 V or 4.6 V. The input current of individual DC-DC converters only fluctuates by about 0.1 mA.

The proposed measurement was performed during a technical stop by people responsible for the operation of the pixel detector. As in the laboratory, the cables to the A4603D

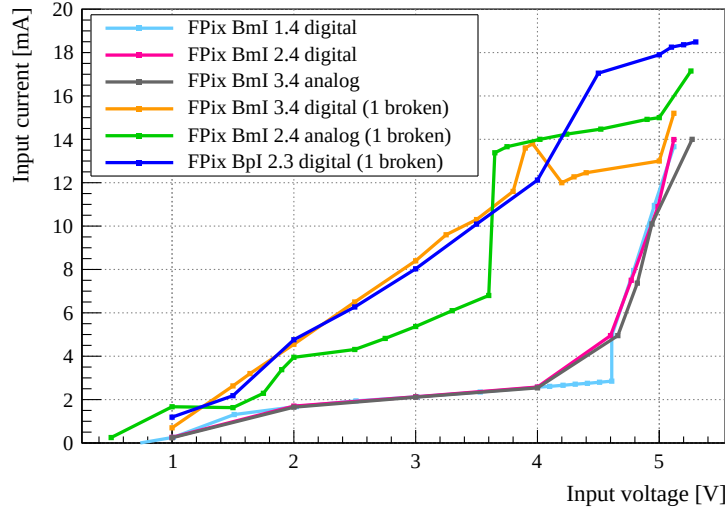


Figure 6.3.: Total DC-DC converter input current as a function of the input voltage, shown for six power supply channels of the FPix detector. The currents were measured for three fully functional channels and for three channels with one malfunctioning DC-DC converter.

power supplies in the experimental cavern were unplugged and connected to a voltage source via an adapter, to allow measurements at low input voltages. Due to the existing magnetic field, however, no laboratory power supply was used. Instead, the voltage for the DC-DC converters was provided by a battery and a voltage divider. The current was measured with a multimeter. The DC-DC converters were disabled by the CCU to prevent switching on at voltages of 4.8 V, which could damage the fuse of the DC-DC converters due to the low conversion ratio.

Figure 6.3 shows the input currents at different input voltages for six power channels of the FPix detector. Three functioning channels as well as three channels with a defective DC-DC converter were measured. For the functioning channels, the four² expected steps of the input current are visible. Due to additional voltage drops in the measurement setup, the threshold voltages are shifted to higher values compared to the laboratory measurement. According to the results described above, a total current of 13.2 mA is expected for four functioning DC-DC converters when the regulators are switched on. Values of 14 mA were measured.

In channels with a defective DC-DC converter, the current increased almost linearly at input voltages below the undervoltage-lockout threshold. Such behavior is not expected. The measurement shows that the fuse was not damaged, assuming that the extra current is drawn from the defective DC-DC converter. Instead, another defect must be present. In channel BmI 2.4 analog the current increased by 7.8 mA at an input voltage of 3.6 V. This may be a sign that the UVLO threshold of the defective

²Four DC-DC converters are connected to a power supply channel in FPix.

DC-DC converter has shifted, and that the input current with the regulators turned on has increased.

6.1.2. Controlled Damaging of DC-DC Converters

To find the cause of the damage, several DC-DC converters were operated under controlled conditions outside their specifications. A special PCB, with which a single DC-DC converter could be operated, was used for the tests. The input voltage and the disable voltage were provided by a laboratory power supply. A programmable electronic load could be connected to the output. The tests, performed with several DC-DC converters, included:

- Applying a negative input voltage of down to -1.5 V .
- Applying a positive input voltage of up to $+20\text{ V}$.
- Applying a negative disable voltage of down to -3.0 V while the DC-DC converter is supplied with input voltage.
- Applying a positive disable voltage of up to $+10\text{ V}$.
- Operation with a short circuit at the output for several hours.
- Removing of the main coil (L2 in Figure A.2).
- Cutting the line for the feedback loop on the converter PCB.
- Connecting the outputs of one analog and one digital DC-DC converter in parallel.

When voltages with wrong polarity are applied, large currents flow in the DC-DC converter. The input voltage and disable voltage were increased in the test as long as the input current of the DC-DC converter remained below 2 A , as the fuse would have blown within a very short time at higher currents. Also, no increased currents had been measured in the detector. The DC-DC converters were typically operated for a few seconds in the described modes. The I-V curve was then measured and compared with the expectation.

The current-voltage characteristic only changed for DC-DC converters which were operated with an input voltage of about 17.4 V or more. In all other cases, no change was observed. The damage due to overvoltage was therefore investigated further.

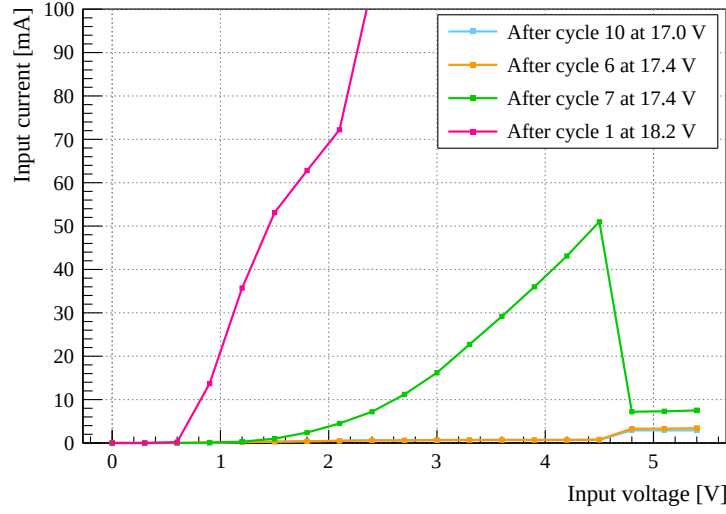


Figure 6.4.: I-V curves of one DC-DC converter, which was repeatedly subjected to overvoltage at the input.

Damage to the ASIC due to Overvoltage

A LabVIEW VI was developed, which increases the output voltage of the power supply in steps of 0.4V. At each step, the DC-DC converters were operated for 2 seconds. Then the output voltage of the power supply was set to zero, and the I-V curves were measured in the disabled state. This procedure was performed ten times for each voltage before increasing the voltage to the next step. In five of the ten iterations the DC-DC converter was disabled while the input voltage was switched on. Figure 6.4 shows the exemplary I-V curves of one DC-DC converter, measured after the operation with 17.0 V, after 6 and 7 cycles with 17.4 V, and after 2 cycles with 18.2 V. No changes of the I-V curve could be measured at input voltages below 17.4 V. After the 7th cycle at 17.4 V, the current below the UVLO threshold increased significantly in the I-V measurement and reached 50 mA. Above the UVLO threshold voltage of the linear regulator the current dropped below about 6 mA. When the DC-DC converter was enabled, it delivered the nominal output voltage. At an input voltage of 18.2 V the FEAST2 ASIC was severely damaged so that it no longer delivered an output voltage.

Three DC-DC converters that were damaged in this way showed the same behavior. For one, a change in the I-V curve was measurable at an input voltage of 17.0 V and above, and for the other two at 17.4 V and above. The tests were repeated with other DC-DC converters to investigate the influence of temperature and irradiation on the overvoltage tolerance. For this purpose, three devices were cooled down to -4°C with a Peltier cooling system. Damages were observed at input voltages of 17.4 V, 17.8 V, and 18.2 V, respectively. There was therefore no indication that the lower temperature in the detector would deteriorate the overvoltage tolerance. A DC-

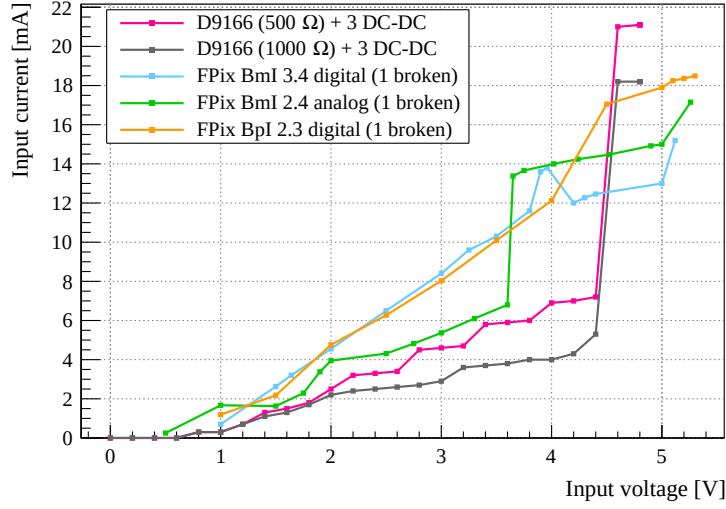


Figure 6.5.: I-V curve of a group of four DC-DC converters, of which one (with the internal ID D9166) was damaged by overvoltage. The laboratory measurement is compared to the measurements of three power groups of the FPix detector, which had one defective DC-DC converter.

DC converter irradiated with protons with an integrated flux of $2 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$ also showed no increased susceptibility to overvoltage at the input.

The overvoltage created a parasitic path between the input and the output of the FEAST2 ASIC. Therefore, the input current of the damaged DC-DC converters depended on the output resistance. Figure 6.5 shows the results of measurements, in which a DC-DC converter that was damaged by overvoltage at the input was operated in parallel with three functioning DC-DC converters. Different resistances were connected to the output of the broken DC-DC converter. For a resistance of 500Ω , the I-V curve follows a similar trend compared to the ones measured in the detector. However, when the regulators of all DC-DC converters turn on, the current in the laboratory measurement is several mA larger compared to the measurement in the pixel detector.

The theory that DC-DC converters were damaged by overvoltage at the input could neither be confirmed nor disproved with this measurement. The output resistance of 500Ω was chosen arbitrarily in the laboratory measurement. However, measurements with pixel modules indicate that the input resistance of a pixel module, which is not powered, is in the order of several $\text{k}\Omega$. Already for a resistance of $1 \text{ k}\Omega$ connected to the damaged DC-DC converter in the lab measurement, the slope of the I-V curve was smaller compared to the detector measurement. On the other hand, the currents at voltages above the UVLO threshold were significantly larger in the laboratory measurement compared to the detector measurement.

Search for possible Sources of Overvoltage

Possible sources of overvoltages in the detector were examined. At CERN, the output voltages of several power supplies of the detector were investigated over several days with an oscilloscope. There were no indications of voltage peaks.

In the context of this thesis, corresponding test were performed in the system test setup. For example, the voltage ripple at the input of DC-DC converters was measured. Modified DC-DC converters were investigated, in which the capacities of the input and output filters were reduced. The PixV13 DC-DC converters have a low-pass filter in a so-called π -topology, in which a coil with an inductance of 12 nH is connected in series to the input and two capacitances of 20 μ F each are connected in parallel. On the DC-DC converter PCB, each of the 20 μ F capacitances is realized by two 10 μ F capacitors connected in parallel (Figure A.2 in the Appendix). In case the functionality of the filter would be degraded, this could lead to voltage peaks at the input of the DC-DC converter.

For a PixV13 DC-DC converter, which was operated with an input voltage of 10 V and an output current of 2 A, a voltage ripple (peak-to-peak) of 0.45 V was measured at the pad of C1 (Figure A.2). If the values of the filter capacities were halved, no change of the ripple was observed within the measurement uncertainties. For a DC-DC converter equipped with only one capacitor (C4), a ripple of about 4.4 V was measured. During disabling and subsequent enabling, this value doubled for about 100 μ s. The input voltage reached about 18 V, which is sufficient to damage a DC-DC converter.

Because the input filter contains four capacitors, it seemed unlikely that defective solder connections could have lead to a degradation of the filter in several DC-DC converters. To investigate the possible influence of radiation damage, the capacitors of DC-DC converters irradiated with doses of 2×10^{14} n_{eq}/cm² and 4×10^{14} n_{eq}/cm² were characterized with an LCR meter. Figure 6.6 shows the measurement of the capacitance for different input voltages and frequencies for an irradiated and an unirradiated capacitor. For all measured components, a severe degradation due to radiation damage was not observable.

The designers of the FEAST2 ASICs conducted tests with irradiated DC-DC converters and tests in a 3 T magnetic field at CERN. Even in these tests it was not possible to reproduce the I-V curves of DC-DC converters that were measured in CMS. Until the pixel detector was extracted in December 2017, it was not possible to determine what the defect was.

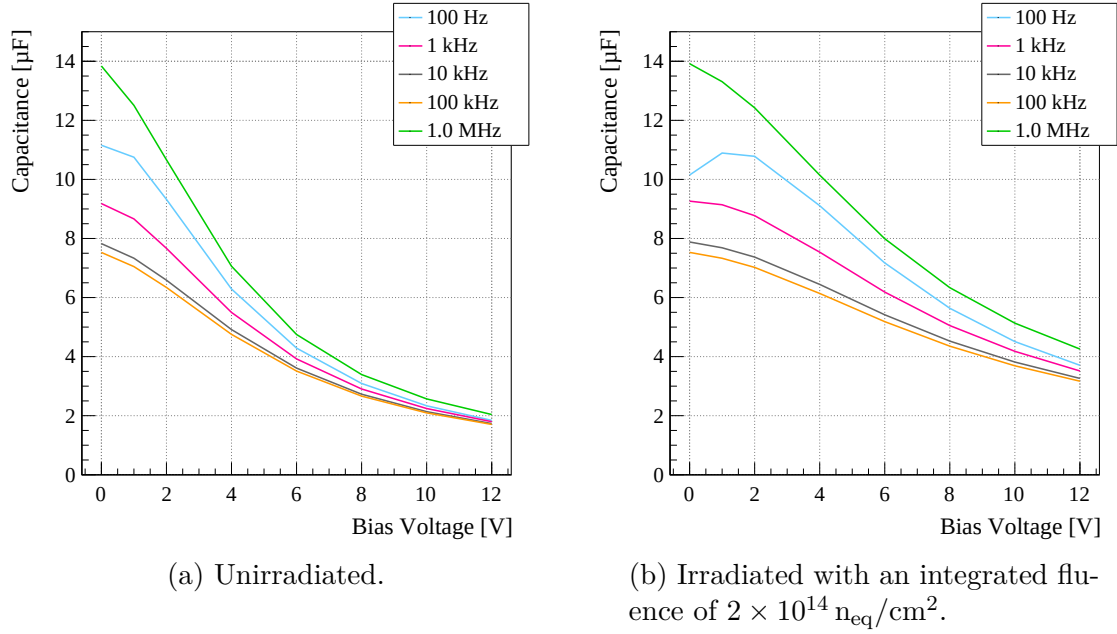


Figure 6.6.: Measurement of the capacitance as a function of the bias voltage and the frequency. The exemplary measurements of two capacitors of the type Murata GRM21BR61C106KE15L (used for C1 and C2) are shown.

6.2. Extraction of DC-DC Converters from CMS

In the Year-End Technical Stop in winter 2017/2018, the pixel detector was extracted from CMS to investigate the failures and to eventually replace all DC-DC converters. Within the scope of this work, a setup was developed with which the behavior of the DC-DC converters could be investigated. In the following the setup is introduced. Results of the measurements with defective and functioning DC-DC converters are presented. The results are interpreted in Section 6.2.4.

6.2.1. The DC-DC Converter Test Setup

The setup for examining the extracted DC-DC converters is shown in Figure 6.7. Up to three DC-DC converters can be tested simultaneously. Each device is plugged into a test PCB that provides connections for the input voltage, output voltage, disable voltage and the PowerGood signal. The required voltages are provided by a Hameg HMP4040 four-channel power supply. Three channels are used for the supply voltage of the DC-DC converters. The fourth channel generates, if required, the disable voltage for all three converters. All voltages can be set independently with a resolution of 1 mV. The currents of each channel are measured by the power supply with a resolution of 0.1 mA. A Keithley 2701 multimeter with a 20-channel differential multiplexer (Model

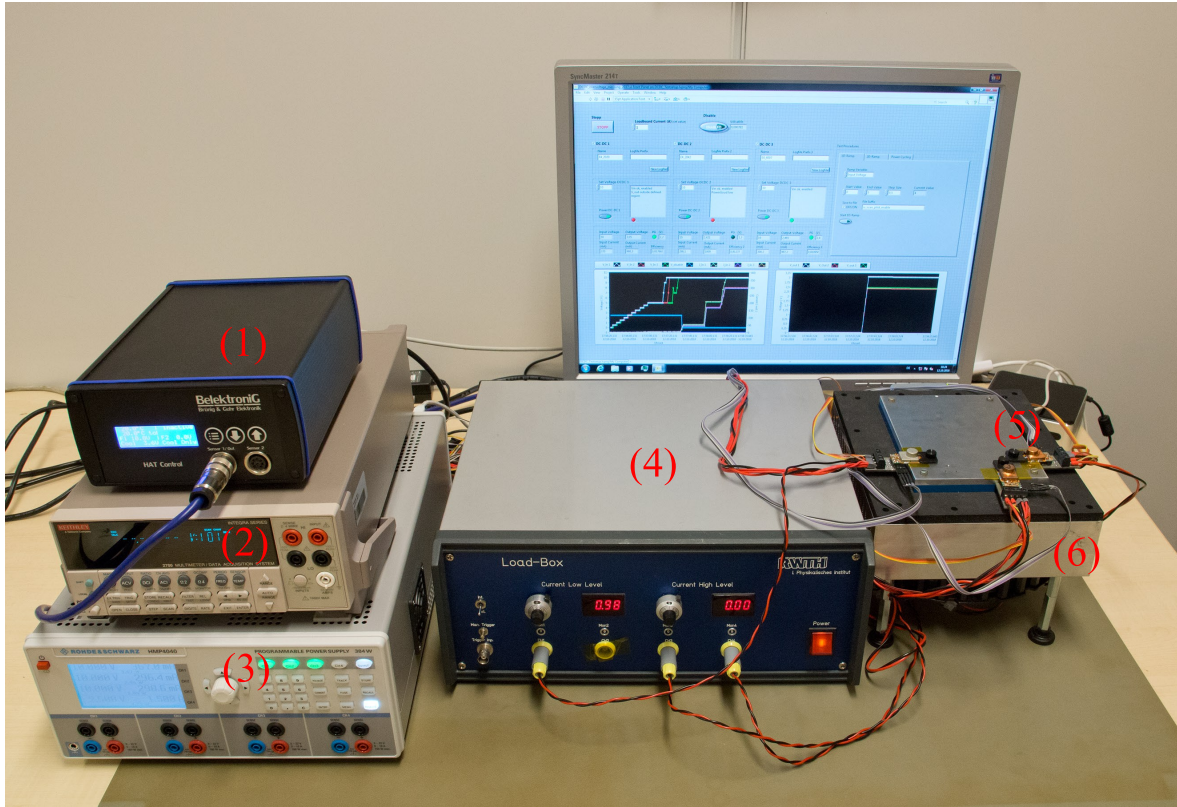


Figure 6.7.: Photograph of the setup for testing DC-DC converters. The picture shows the Peltier controller (1), the multimeter (2), the power supply (3), the electronic load (4), three DC-DC converters (5), and the cooling block (6).

7700) is used to measure the input voltage, output voltage, PowerGood and disable voltage of each converter on the test PCB. The outputs of the DC-DC converters are connected to a programmable electronic load that was developed in-house. The load has four non-independent channels which can be programmed to draw currents between 0 A and 3 A. The DC-DC converters are clamped onto a cooling plate using a 3D printed plastic part. Peltier elements regulate the temperature. For all following tests a cooling block temperature of $+20^{\circ}\text{C}$ was used.

A LabVIEW VI was developed to control the setup and to perform automated measurement series. The front panel is shown in Figure 6.8. For each DC-DC converter, the actual measured voltages and currents are displayed in text form, and the conversion efficiency is calculated. In addition, the input and output variables are shown over time. All values are stored in log files for later analysis. The measured values are compared to a status matrix in real time to give the operator a direct feedback. If a measured value deviates too much from the reference value, a status display of the affected DC-DC converter changes from green to red, and a description of the problem is presented in text form on the front panel.

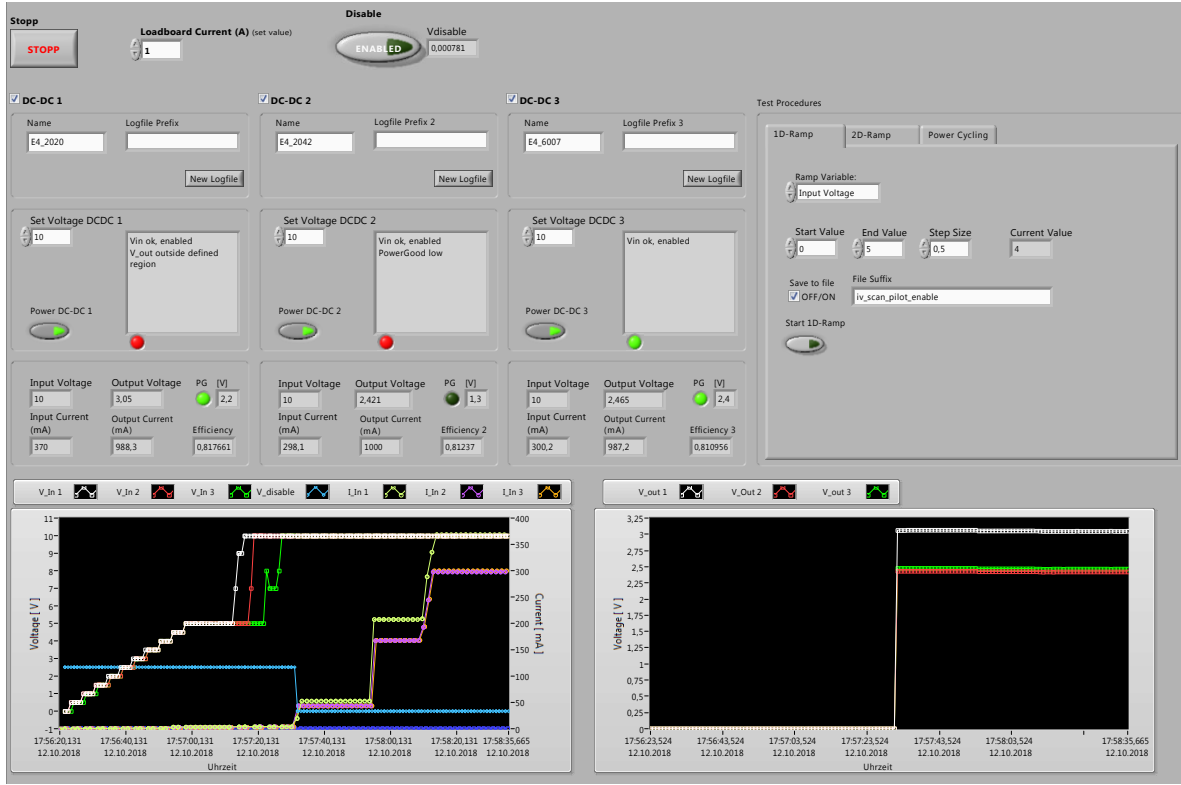


Figure 6.8.: User interface of the control software of the DC-DC converter test setup. The measured input and output voltages and currents of three DC-DC converters are shown in text form (center) and over time (bottom). A status window for each DC-DC converter indicates whether any of the measured values are outside of the expected range. Automated measurements and power cyclings can be performed (right).

The output voltage of the power supply and the electronic load are programmed via the GUI. The software also enables the automatic execution of 1-dimensional or 2-dimensional scans of these parameters. The parameters to be varied, the start and the end values of the scan, and the step size can be set. The results are stored in a separate log file. Furthermore, an automated power cycling by disabling and enabling or by switching off the input voltage is possible.

6.2.2. Investigation of defective DC-DC Converters

In the following, all DC-DC converters that at least once did not supply the nominal output voltages under normal conditions are referred to as defective. During the operation of the pixel detector, 61 DC-DC converters (5.0 % of 1216) were found defective. Of these DC-DC converters, 11 provided output voltage again after some time, or worked as long as the load at the output was small. The fuse of one DC-DC converter was

blown. After the extraction of the DC-DC converters, another four defective devices were found. It is assumed that these were damaged by handling.

The shield was removed from several defective DC-DC converters in order to be able to measure voltages directly at the FEAST2 ASIC. In eight out of ten defective DC-DC converters investigated, the voltage provided by linear regulators (so-called V33Dr) in the chip was only in the range of 0.9 V to 1.4 V instead of 3.3 V. The reduced voltages prevented the power transistors in the defective chips from switching. An increased input current was measured for 11 of 14 defective converters. In the disabled state and with an input voltage of 4.6 V, the average input current of these 11 devices was 9.3 mA, while a value of about 3.0 mA is expected. Furthermore, the UVLO threshold voltage, at which the regulators switch on, was reduced for almost all chips. Threshold values as low as 1.5 V were measured.

The designers of the FEAST2 ASIC found out that after applying an external voltage of 3.3 V to the V33Dr pin, a large fraction of the DC-DC converters delivered an output voltage again. Even after removing the external voltage, the V33Dr voltage was in the range of 3 V, and the chip provided the nominal output voltage. However, the input current remained above the nominal value, and the UVLO threshold was still reduced. Parasitic paths in the chip, which prevent the V33Dr linear regulator from switching on and cause a higher current flow, are a possible explanation for this observation. The application of an external voltage with a large current may break some of these paths, making the transistors switch again.

Damaged Pixel Modules

On the supply tubes and the service cylinders, some defective DC-DC converters were replaced by working ones during the tests. It was discovered that in some readout chips many pixel unit cells were damaged. When a pixel module is operated without low voltage, but the sensor bias voltage is provided, a current flows into the preamplifier of the PUC and damages it. This was the case during data collection in 2017. The granularity of the HV and LV channels did not allow the high voltage to be switched off for individual pixel modules that were connected to defective DC-DC converters. The severity of the damage depends on the leakage current in the silicon sensor and the time during which the pixel modules were operated in this condition. Pixel modules in the innermost BPix layer and in the inner rings of FPix were affected most, because the radiation damage and therefore the sensor leakage current is highest there. In BPix, the damaged modules of layer 1 that were accessible (six of eight pixel modules) were replaced.

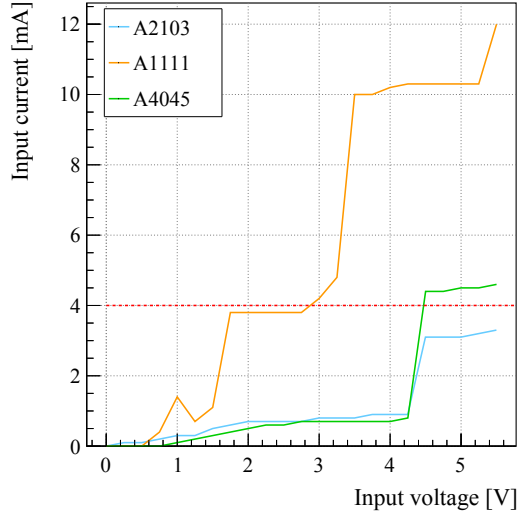
6.2.3. Investigation of working DC-DC converters

In the setup described, the majority of DC-DC converters from the pixel detector were examined with the help of several people to find out whether they showed signs of damage. For each DC-DC converter investigated, the I-V curve was measured for input voltages from 0 V to 5.5 V in the disabled state. The I-V curve was also measured for input voltages between 0 V and 10 V in the enabled state, while a current of 1.5 A was drawn from the output.

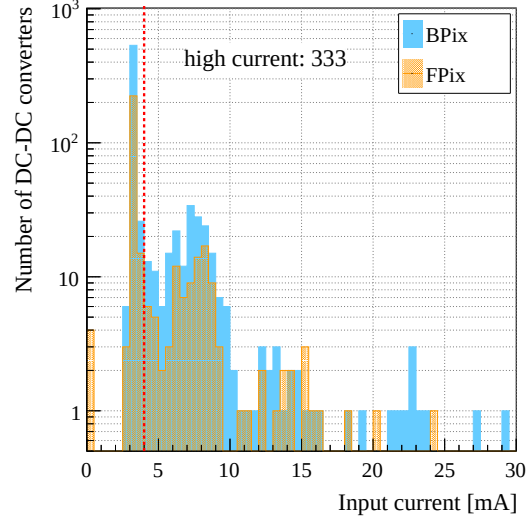
For 333 DC-DC converters (27.6 % of 1206) that provided the nominal output voltage, currents of more than 4.0 mA have been measured at an input voltage of 4.75 V in the disabled state. Figure 6.9(a) shows exemplary I-V curves of two devices with a high current and one device with the expected current measured in the disabled state. Figure 6.9(b) shows a distribution of the measured currents of all DC-DC converters at an input voltage of 4.75 V.

The distribution peaks at 3.0 mA. These are DC-DC converters which do not show signs of damage. Currents well below 3.0 mA were mainly measured for defective devices. For most of the DC-DC converters with an increased input current, values in the range of about 6 mA to 9 mA were measured.

The damage to the DC-DC converters was not correlated with the location in the detector. This is demonstrated in Figure 6.10, which represents a two-dimensional map of the BPix supply tubes. Defective DC-DC converters are marked red, DC-DC converters with a high input current but still delivering output voltage are marked yellow. Analog and digital DC-DC converters are affected. In one power group (BPix BpO Sector 4 layers 2 and 3), which could not be supplied with input voltage during data acquisition in 2017, no damage occurred. Also in FPix no concentration of defects was observed. Table 6.2 summarizes the numbers of good, high-current, and defective DC-DC converters in the BPix supply tubes and the FPix service cylinders.

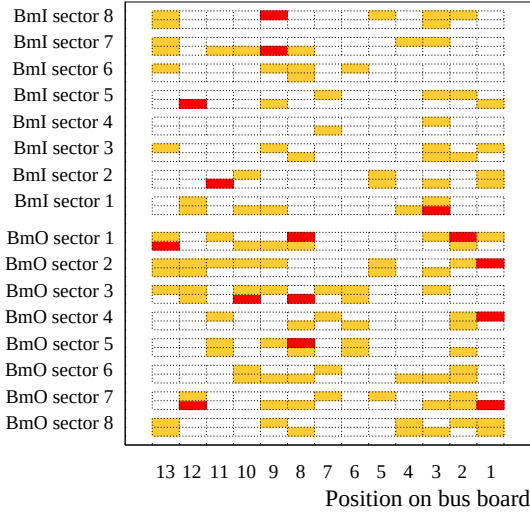


(a) I-V curves of three DC-DC converters in the disabled state. Their internal IDs are indicated.

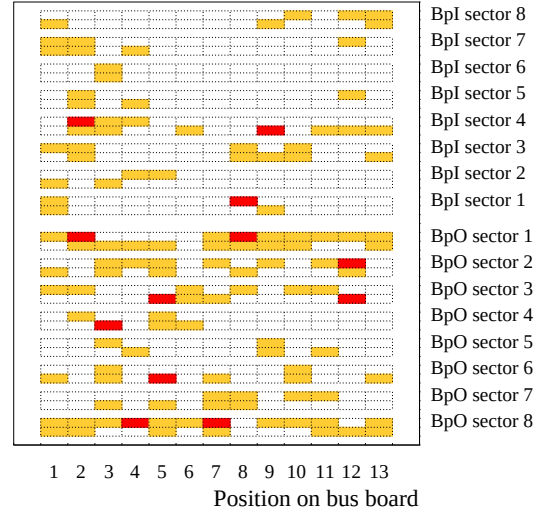


(b) Distribution of the input current at an input voltage of 4.75 V. The histograms for FPix and BPix are not stacked.

Figure 6.9.: Results from the characterization of the DC-DC converters that were extracted from CMS. DC-DC converters with a current above the indicated limit were considered damaged.



(a) Supply tubes in negative z -direction.



(b) Supply tubes in positive z -direction.

Figure 6.10.: Distribution of the defective and high-current DC-DC converters in the BPix supply tubes. Each square represents one DC-DC converter. Devices with a high input current are marked yellow, defective devices are marked red.

Table 6.2.: Numbers of DC-DC converters tested, defective devices, and DC-DC converters with an input current above 4 mA at an input voltage of 4.75 V. The individual numbers of each BPix supply tube and each FPix service cylinder are given. The percentage of defects and high-current devices is calculated in relation to the total number of tested DC-DC converters of each subdetector.

Subdetector	Tested	Defective	High-current	Defective [%]	High-current [%]
BPix BmI	205	5	44	2.4 %	21.5 %
BPix BmO	206	10	68	4.9 %	33.0 %
BPix BpI	204	3	42	1.5 %	20.6 %
BPix BpO	207	9	75	4.3 %	36.2 %
FPix BmI	96	11	25	11.5 %	26.0 %
FPix BmO	96	8	21	8.3 %	21.9 %
FPix BpI	96	11	34	11.5 %	35.4 %
FPix BpO	96	4	24	4.2 %	25.0 %
Total	1206	61	333	5.1 %	27.6 %

6.2.4. A Model for the Damage

The designers of the FEAST2 ASIC have developed a theory to explain the observations. The problem was localized in the linear regulator (V33Dr), which provides the voltages for switching of the power transistors. It is assumed that at least one of the transistors that are used for the soft-start procedure has been damaged by overvoltage. A leakage current in these transistors can impair the function of the undervoltage lockout. In addition, the power transistors in the ASIC can no longer switch at all when the leakage current is in the mA range. When a parasitic path develops in other components of the circuit, this only leads to an increased current at the input, but the DC-DC converter is still functioning. There are therefore two failure mechanisms. A high input current of a functioning DC-DC converter does not mean that the device will break in the near future.

In the months following the extraction of the DC-DC converters, several test campaigns were carried out at CERN, in which this theory was confirmed [115]. Radiation induced displacement damage can cause a leakage current in the nA range in an NLDMOS transistor in the V33Dr circuit. This leakage current is amplified in FEAST2 by a factor of about 500 by a current mirror. When the DC-DC converter is enabled, this

current flows through the drivers of the power transistors to ground. When disabled, the current integrates on the capacitor C9, leading to an increase in the voltage. This voltage can cause either damage to the two transistors for the soft-start procedure (DC-DC converter no longer switches), or damage to parts of the driver of the high-side transistor (increased input current). The effect occurs only after irradiation with a TID in the range of 500 kRad to about 6 MRad and also depends on the dose rate. The FEAST2 ASIC will only be damaged if the DC-DC converter is disabled.

The tests carried out at CERN are briefly presented below. Among other things, high-resolution 3D X-ray images of defective DC-DC converters from CMS were taken to check the quality of the soldering of the capacitance C9. An intermittent contact could have led to voltage peaks. No anomalies were detected.

A long-term test setup with 124 DC-DC converters of type FEASTMP [53] was built. These DC-DC converters were developed by the CERN group Electronics Systems for Experiments (PH-ESE) for use in high energy physics experiments. Like the DC-DC converters for CMS, they are based on the FEAST2 ASIC. In the setup the converters were repeatedly disabled and enabled again. The I-V curves of the DC-DC converters were measured regularly. No irregularities were discovered here either.

Furthermore, a series of tests on electromagnetic compatibility (EMC) with a replica of the power system of the pixel detector were carried out. Among other things, pulses of the size of several kV were capacitively coupled into the multi-service cables. Furthermore, high-frequency pulses were coupled via an antenna into the output lines as well as the disable lines of DC-DC converters. The ASIC was also exposed to ESD pulses. In some of these tests, DC-DC converters were damaged, but they showed different damage symptoms than the DC-DC converters from CMS.

Several irradiation campaigns were carried out. During the year-end technical stop, a setup with 32 DC-DC converters was installed on the so-called castor table of CMS. It is located about 15 m away from the interaction point, behind the hadron forward calorimeter. The particle fluence at this location is about one order of magnitude higher than at the location of the DC-DC converters in the pixel detector. In the setup, 16 PixV13 DC-DC converters and 16 FEASTMP DC-DC converters were operated. Their input and output voltages and currents were measured. The voltage of V33Dr was additionally measured at eight DC-DC converters via a soldered cable. An eight-hour test sequence was implemented. At the beginning of the sequence, the I-V curves of the DC-DC converters was measured. The converters were then operated for several hours at an input voltage of 9 V and enabled and disabled at various time intervals. At the end of the test sequence, the I-V curve was measured again, and the sequence was repeated. In this setup no defective DC-DC converters were observed until the time of this writing. However, already about 10 % of the DC-DC converters have an increased current in the I-V measurement.

In addition, 16 PixV13 DC-DC converters and 16 FEASTMP DC-DC converters were irradiated at the CERN IRRAD facility. There, a copper target was hit with protons

from the Proton Synchrotron to produce a mix of protons, neutrons and pions. The DC-DC converters were operated on four electronic boards. The devices were located at different distances from the target (about 20 cm to 50 cm) and from the axis of the primary beam (about 2.5 cm to 15 cm), resulting in variable radiation levels at different positions. The boards were placed in a cold box with a cooling temperature of -25°C . During irradiation, a two-hour test procedure was repeated several times. I-V curves were measured, then the DC-DC converters were enabled and operated for one hour. A disable and enable cycle was performed, and the DC-DC converters were operated again for one hour. In this irradiation test, 15 DC-DC converters were damaged to such an extent that they had a high current in the I-V measurement, and one DC-DC converter was defective. A direct correlation between the occurrence of the damage and the irradiation dose could be demonstrated. The first damage occurred at a TID of about 1.2 Mrad [116]. The ASICs were only damaged during the disable and enable cycles.

Finally, tests with X-rays were carried out. DC-DC converters were irradiated incrementally up to doses of some Mrad. At different doses a DC-DC converter was disabled, and the development of the voltage at the V33Dr node was measured. An increase of the voltage beyond the nominal value of 3.3 V was observed. This confirmed the theory that the ASICs were damaged due to the disabling. The increase depended on the received total ionizing dose and the dose rate. It turned out that the chip is only at risk in a range between about 500 krad and 6 Mrad.

6.3. Production of PixV14 DC-DC Converters

From the original production of PixV13 DC-DC converters, there were about 300 functioning spares left. These would have been sufficient to replace the defective DC-DC converters in the pixel detector. Nevertheless, a new production of DC-DC converters was already started in November 2017. This made it possible to replace other converters, if necessary, in case that further damaged devices were found.

All 1216 DC-DC converters required for BPix and FPix and 217 additional spares were produced. A new revision of the FEAST2 chip (FEAST2.1) was used, in which a problem with the PowerGood circuit was fixed. Some chips of the first revision produced the nominal output voltage, but the PG bit remained low. In the initial production of DC-DC converters for CMS, about 10 % of the devices were rejected because of this error. Fuses with a higher rating compared to the original ones were mounted on the new, so-called PixV14 DC-DC converters to accommodate the larger than expected module currents, and to be able to operate the detector at a lower input voltage. It was also discussed whether the fuse should be omitted entirely, as it is by design subject to aging effects. However, due to the risk of losing an entire power group in the event of a short-circuit at the input of a single DC-DC converter, it was decided not to do so.

The fuses were selected such that for an output current close to the overcurrent limit³, the input current of a DC-DC converter at an input voltage of 5 V corresponds to less than 75 % of the rated fuse value. The fuses comply with the UL 248-14 standard, meaning that they shall not be operated with currents above 75 % of the nominal value continuously. Based on a measurement with several DC-DC converters, which was conducted in the context of this thesis, values of 3 A were chosen for the fuse of the analog DC-DC converters and 4 A for the digital converters.

The required PCBs, coils, and electromagnetic shields were supplied by various manufacturers and then assembled by a specialist company. The assembly followed the specifications of IPC-A-610D (class 3). Of the new DC-DC converters, 234 were manufactured with remaining parts of the initial production in 2015. Further 1199 DC-DC converters required new PCBs, and 848 of these also required new shields. There were enough coils left so that new ones did not have to be produced. The production of the shields was the most time-critical process.

During the original production, 23 weeks were dedicated to the testing of the DC-DC converters. The tight schedule of the technical stop in winter 2017/2018 allowed only about three months for the production and the testing of all DC-DC converters. Therefore, a backup plan was to replace the fuses of all working DC-DC converters removed from the pixel detector and to reinstall them afterward. All fuses were replaced, but it was not required to reinstall the PixV13 DC-DC converters, because all PiXV14 DC-DC converters could be produced and tested within 11 weeks. The new DC-DC converters underwent the complete series of qualification tests that had been carried out during the initial production, which are described in references [88, 89], plus some additional tests. All DC-DC converters of the pixel detector were replaced by the new ones.

6.3.1. Overview of the Qualification Tests

Several quality control tests of every DC-DC converter were performed by the assembly company. When all SMD (surface-mounted device) components were soldered onto the PCBs, an automated optical inspection was performed. After the coil was soldered, a high-resolution X-ray imaging and a passive thermal cycling with ten cycles between -30°C and $+60^{\circ}\text{C}$ were performed. Before the mounting of the shield, an electrical test was also performed at the company. Devices that passed all tests were equipped with the shield and then delivered to RWTH Aachen University. There another electrical test was performed, and the DC-DC converters were actively thermally cycled with ten cycles between -28°C and $+20^{\circ}\text{C}$. A database, which had been developed for the initial production by the student M. Rauch, was used to collect and analyze the data from all tests. The database features a graphical user interface, which presents summary plots as well as results for every individual DC-DC converter.

³This equals the maximum output power.

6.3.2. Electrical Test before the Mounting of the Shield

In the context of this thesis, the setup that was used for the testing of DC-DC converters at the assembly company was developed. It is very similar to the setup used for the tests of DC-DC converters extracted from CMS (Figure 6.7). In particular, the same type of power supply (Hameg HMP 4040) and a multimeter with a differential multiplexer (Keithley 2700 series) are used to power a DC-DC converter and to monitor the input current, input voltage, output voltage, and the PowerGood status. Instead of a programmable current sink, a resistor with a value of $2.3\ \Omega$ is connected to the output of the DC-DC converter. The output current depends on the output voltage and is between 1.05 A for 2.4 V and 1.52 A for 3.5 V. In this setup, one DC-DC converter is tested at a time. The electrical connectivity with the device is established with a small PCB. The DC-DC converter is clamped onto an aluminum cooling block, which is kept at $+20\ ^\circ\text{C}$ with a Peltier element.

A LabVIEW VI was developed to control the system and to analyze the test results. The operator has to mount the DC-DC converter, enter the corresponding ID in the GUI, and start the test. After about 1 minute of testing, the result (failed or passed) is presented to the user. The test procedure is divided into three parts. In the first part, the DC-DC converter is power cycled ten times. At each repetition the DC-DC converter is disabled first, then the input voltage is turned on, and then the DC-DC converter is enabled. After two seconds, the device is disabled again, and the low voltage is switched off⁴. At every stage it is verified that the combination of the input voltage, output voltage, disable signal, and PowerGood signal is valid, meaning that the DC-DC converter can be properly enabled and disabled, that it provides the nominal output voltage and that the PowerGood status is correct.

In the second phase of the test, the DC-DC converter is switched on for 10 seconds, and the output voltage and the conversion efficiency (calculated with Equation 2.5) are monitored. This test is passed if the output voltage lies within $\pm 150\ \text{mV}$ of the nominal value and the efficiency is above 78 %.

In the last part of the test, the DC-DC converter is disabled, and the input currents at voltages of 4.6 V and 3.0 V are measured. These values had not been measured during the first production of DC-DC converters. The test was introduced in response to the results of I-V measurements of several power groups in the pixel detector, which are described in Section 6.1.1. As mentioned before, at an input voltage of 4.6 V the V33Dr linear regulator is active, but the second stage of the undervoltage lockout prevents the power transistors from switching. In this case, an input current of about 3 mA is expected. Below a voltage of 3.6 V the first stage of the UVLO also switches the V33Dr linear regulator off, thus at 3.0 V a current below 1.0 mA is expected.

⁴This procedure is similar to the procedure that was used to power on and off DC-DC converters in the pixel detector in 2017.

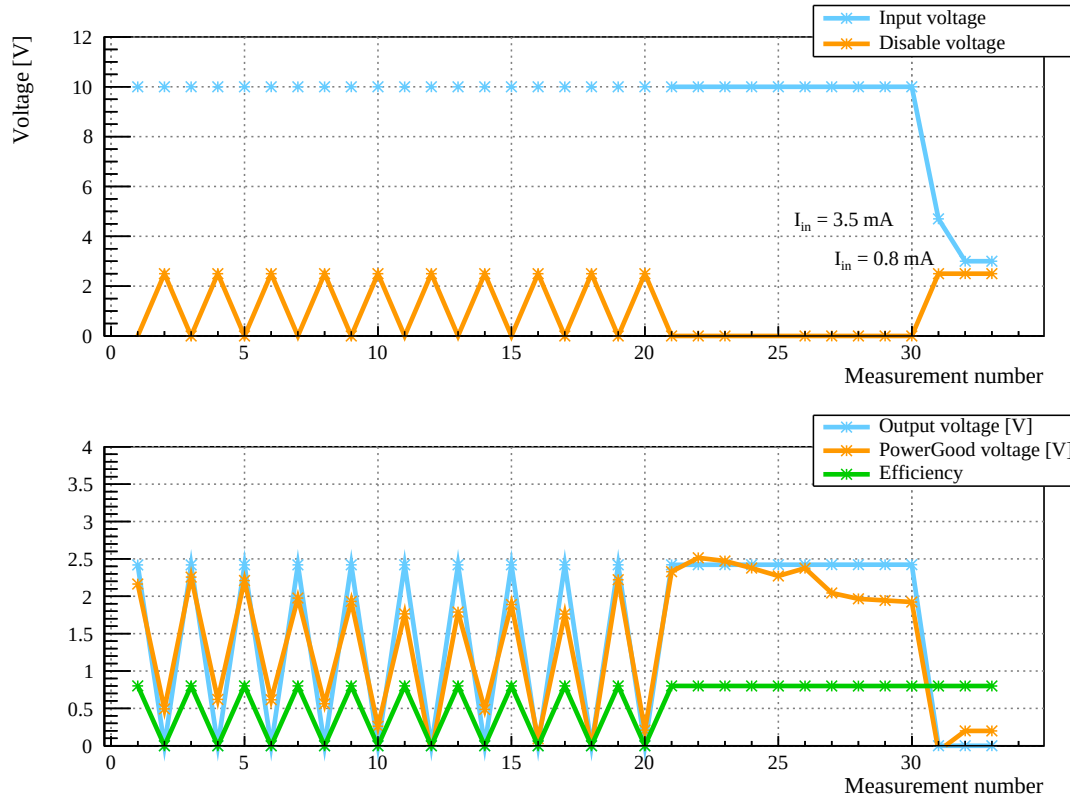


Figure 6.11.: Test sequence of the electrical test at the assembly company. The results of a DC-DC converter with the internal ID A0222 are shown. Top: input voltage and disable voltage. The input currents measured at 4.6 V and 3.0 V are indicated. Bottom: Measured output voltage, voltage of the PowerGood signal, and calculated efficiency.

The test sequence is illustrated in Figure 6.11. In the upper plot, the input voltage and the disable signal are shown. The output voltage, the PowerGood voltage, and the conversion efficiency are visualized in the lower plot. During the first part of the test, a power cycling is performed after every second measurement. In the second and third part of the test, the output voltage is not turned off in between the measurements. This is indicated by the solid line connecting the data points of the input voltage. The results are shown for a DC-DC converter that was rejected because of a fluctuating level of the PG voltage.

As a result of the electrical test at the assembly company, 18 DC-DC converters were rejected (1.3 % of 1433 converters):

- The efficiency of 11 DC-DC converters was below 78 %.
- Three devices were functioning but delivered an output voltage more than 150 mV away from the nominal value.

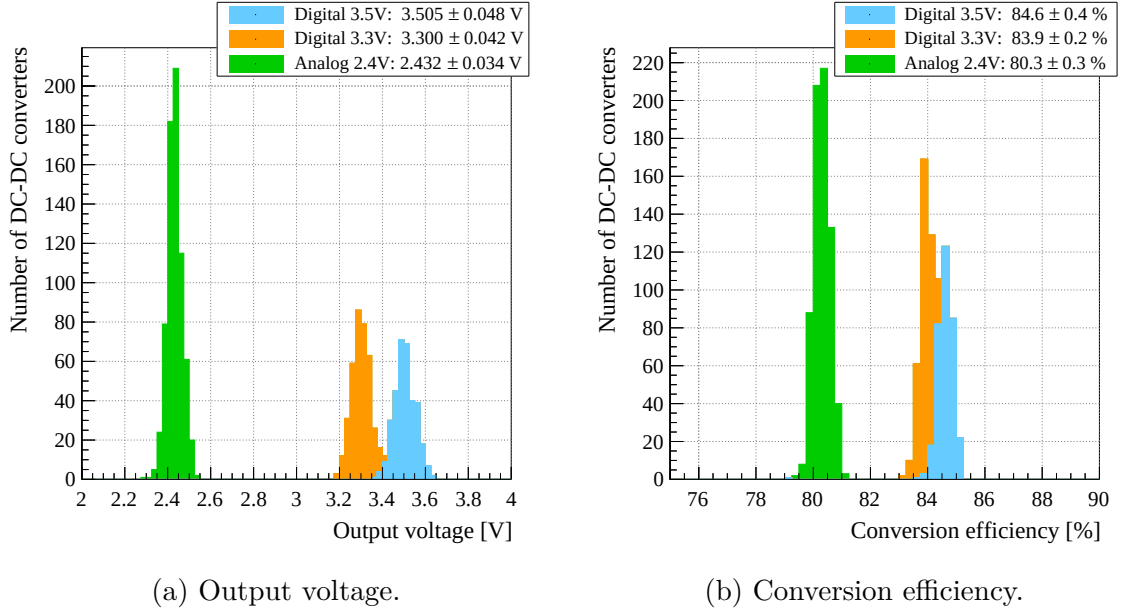


Figure 6.12.: Distributions of the output voltages and the measured conversion efficiencies of all DC-DC converters that passed the test at the assembly company. The histograms are stacked. The mean value and the RMS of the distributions are indicated.

- Two DC-DC converters were rejected because of an input current greater than 4.5 mA^5 at 4.6 V .
- The PowerGood signal level of one DC-DC converter was fluctuating.
- One device could not be disabled, but instead drew a current reaching the power supply limit of 1.5 A when a disable voltage was supplied.

Figure 6.12(a) shows a distribution of the measured output voltages and Figure 6.12(b) shows a distribution of the measured efficiencies. Analog DC-DC converters have a smaller efficiency than digital DC-DC converters due to the larger conversion ratio. However, the values cannot be directly compared because the output current influences the efficiency. The output currents in the setup depend on the output voltage and the selected resistor. The mean value of the calculated output currents was 1.07 A for the analog DC-DC converters and 1.45 A and 1.54 A for digital DC-DC converters with nominal output voltages of 3.3 V and 3.5 V , respectively.

6.3.3. Thermal Cycling

After the shields were mounted, the DC-DC converters were delivered to RWTH Aachen and tested again. The setup was developed and the tests were done by the electronics

⁵This threshold was determined in consultation with the designers of the FEAST2 ASIC.

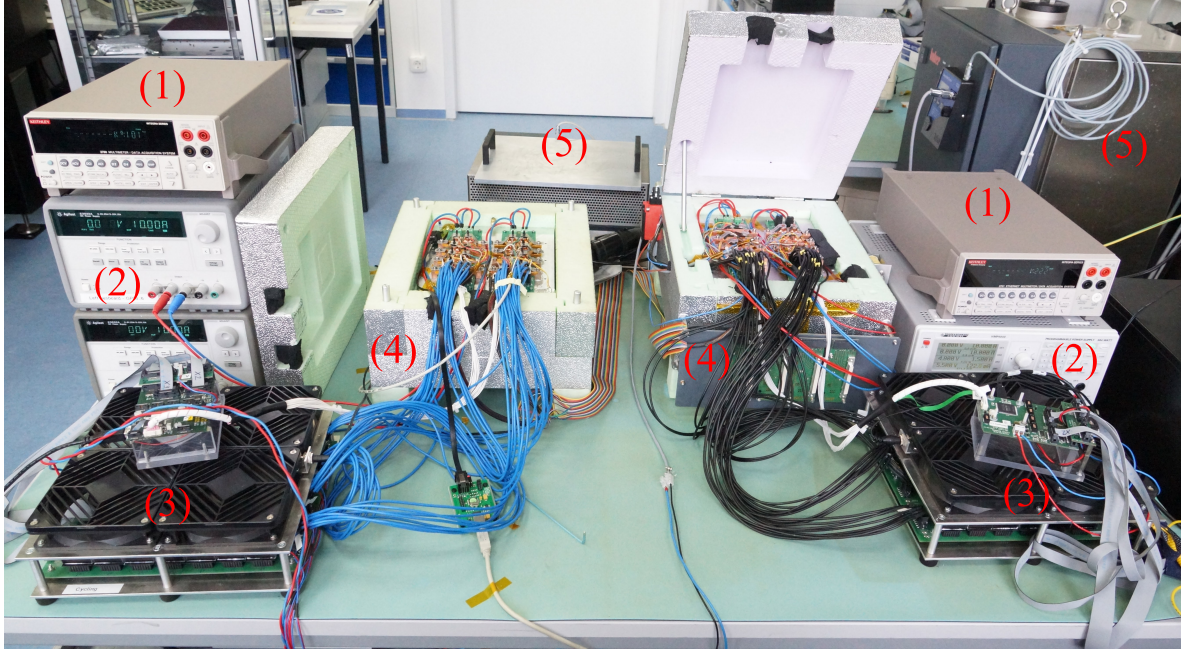


Figure 6.13.: Photograph of the two setups used for thermal cycling of DC-DC converters. For each setup the multimeter (1), the power supplies (2), the programmable load (3), the cold box (4), and the liquid chiller (5) are shown. The Peltier controllers are located below the table and are not visible.

group of the I. Institute of Physics. In this test, the output voltage and the efficiency as a function of the output current were measured. A programmable load was used to draw currents up to 3 A per device. None of the delivered DC-DC converters was rejected in this test.

The final step of the qualification procedure involved an active thermal cycling of all DC-DC converters. For the initial production in 2015, a setup for testing of 16 DC-DC converters was developed. In the context of this thesis, a similar setup was built to double the number of DC-DC converters that could be tested per day. This was required to be able to keep the short time limit for the delivery of the devices. The cold box setup, which was used for the pixel module qualification (Chapter 3.3), was used as a basis for the second setup because the main concept is similar. Both setups are shown in Figure 6.13. The original setup is located on the left side, and the new setup is shown on the right side.

The cold box is made from polystyrene foam and contains a two-stage cooling system. An aluminum block is cooled by Peltier elements and the heat from the Peltier elements is removed with a liquid chiller. Eight copper cooling bridges are mounted on the front side of the aluminum block together with two PCBs, as illustrated in Figure 6.14. The PCBs distribute the input voltage to the DC-DC converters and connect their output to electronic loads. Each load has 26 channels that can be individually programmed

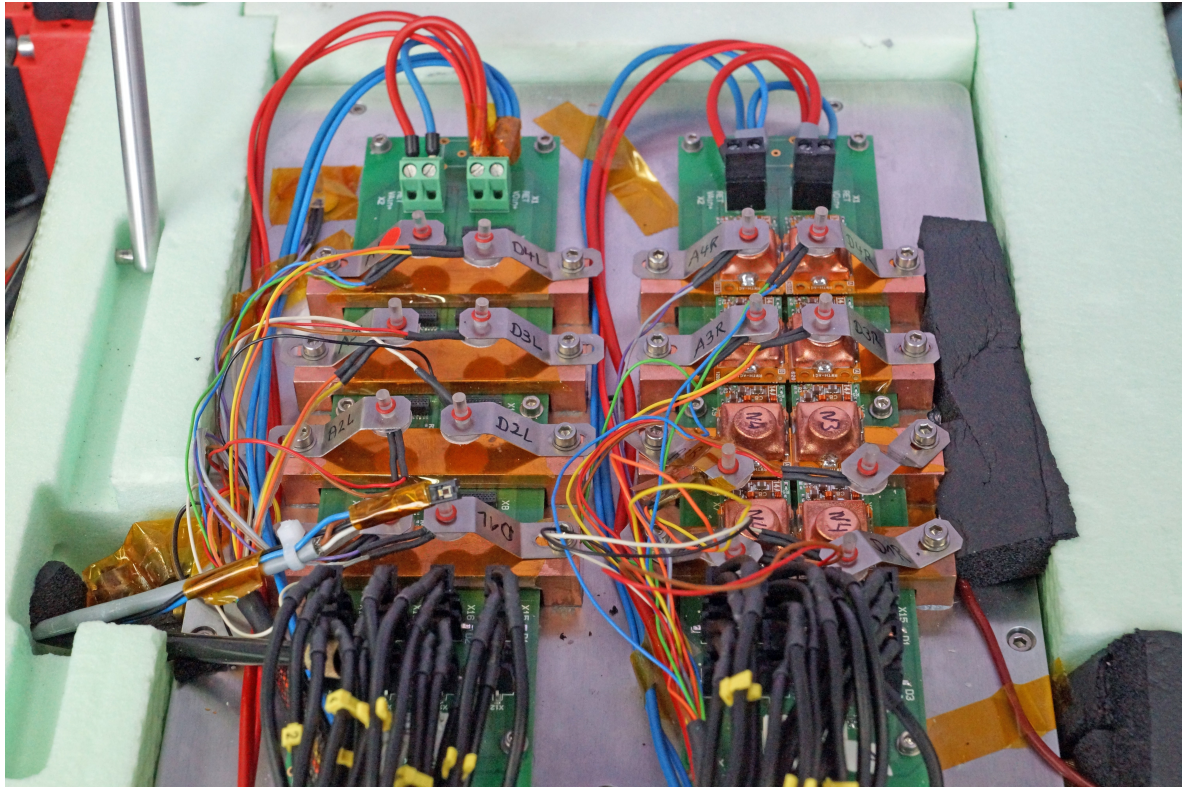


Figure 6.14.: Photograph of DC-DC converters in the thermal cycling setup. For illustrative purposes, DC-DC converters are mounted on the right PCB only.

to draw currents in the range of 0 A and 3 A. An FPGA of the electronic load creates the disable voltage for the DC-DC converters and measures the PowerGood status and the output voltage of each device. The DC-DC converters are clamped onto the cooling bridge with a small spring that presses slightly against the shield. The absence of screws allows a quick exchange of converters and speeds up the handling process. The temperature of the shields is measured with Pt-100 type resistance temperature detectors (RTDs), which are read out by a multimeter. The RTDs are located between the shields and the springs.

In the original setup, three power supplies are required. Two of them provide the input voltage for the DC-DC converters, and one provides the supply voltage for the electronic load. In the new setup, a single power supply with four channels is used instead. Eight DC-DC converters are connected in parallel to a power supply channel.

Test Sequence

A LabVIEW VI was used to control all devices, to log the measured data and to execute the test sequence. Ten thermal cycles between temperatures of +17 °C and

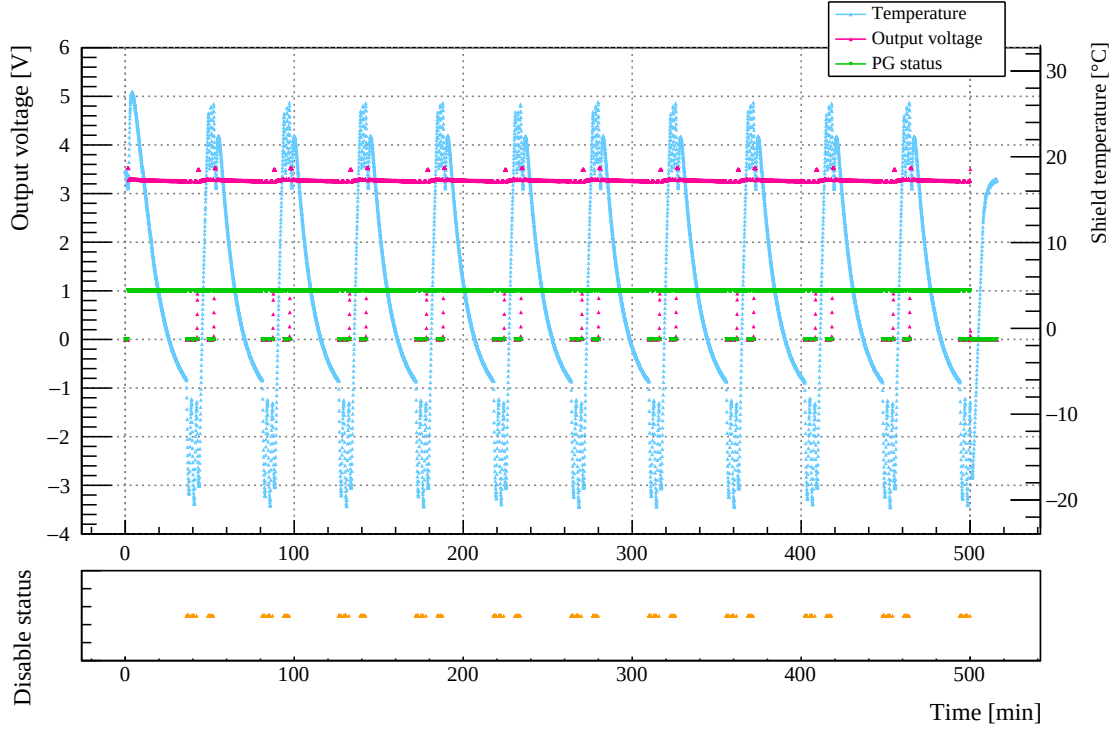


Figure 6.15.: Data measured during the thermal cycling, shown for one DC-DC converter. Orange markers indicate that the DC-DC converter was disabled.

-28°C (measured at the aluminum cooling plate) were performed. During the cycling, the DC-DC converters were operated with an input voltage of 10 V, and a current of 3 A was drawn from the output. For each DC-DC converter, it was constantly checked whether the combination of the input voltage, output voltage, disable voltage and PowerGood status met the expectation. Figure 6.15 shows typical data from the thermal cycling.

In each cycle, a series of additional tests were carried out when the low and high set temperatures were reached. A power cycling of the input voltage was performed. The DC-DC converters were also operated in the disabled state for 100 seconds and in the enabled state for further 100 seconds. The input voltage was reduced to 0 V and was then increased in steps of 1 V to 10 V to test the undervoltage-lockout functionality. In the range from 3 V to 6 V the step size was only 0.2 V. The input current could only be measured for a group of several DC-DC converters that were connected in parallel. Therefore, in contrast to the test at the assembly company, the current of individual DC-DC converters could not be determined. However, individual DC-DC converters of suspicious groups could be examined later.

Only three defective DC-DC converters were found in the thermal cycling test. One DC-DC converter produced no output voltage throughout the entire test sequence.

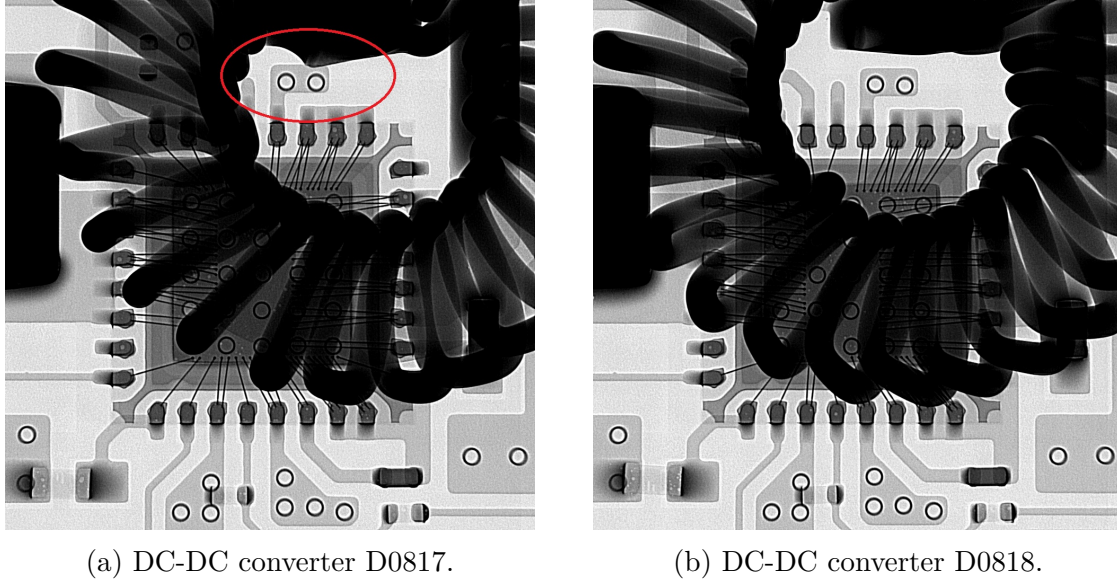


Figure 6.16.: X-ray images of DC-DC converters, taken by the assembly company. The contact wire of the coil touches a GND pad on the DC-DC converter with the internal ID D0817. This is not the case for device D0818, which is shown here as an example.

However, it worked both in the test at the assembly company and in the electrical test at RWTH Aachen University. It was therefore probably damaged during handling. An analog DC-DC converter delivered an output voltage only for input voltages of 5.6 V and higher. The output voltage at the turn-on was 3.5 V. Only at even higher input voltages did the output voltage drop to the nominal value of 2.4 V.

In a third DC-DC converter, a short circuit developed between a contact wire of the toroid (L2) and a nearby pad at ground potential during the third thermal cycle. The coil was slightly displaced from the nominal position, which led to this problem. After this incident, all X-ray images taken by the assembly company were examined. A total of 33 DC-DC converters were found in which a contact wire of the coil protrudes beyond the solder pad, as illustrated in Figure 6.16. These DC-DC converters have been rejected for safety reasons. In total, 52 of 1433 DC-DC converters were rejected after all tests. The yield of this production was 96.4%.

6.4. Results

The time schedule for the production of the new DC-DC converters was met. By the end of January 2018, all required DC-DC converters were installed in the pixel detector. The new DC-DC converters are operated with a lower input voltage than in 2017, which is 9 V. Since it is known that the FEAST2 ASIC can only be damaged by disabling, this feature is no longer used for the operation of the pixel detector where possible. For the power cycling of pixel modules, the power supplies are switched off and on again

instead. However, power cycling without disabling has the disadvantages described earlier. Because the pixel modules draw a higher current in the unprogrammed state than in the programmed state, not all power channels of the barrel pixel detector can be switched on with this method. Sometimes the trip limits must be increased to the maximum value, the input voltage must be increased during switch-on, or at least one DC-DC converter must be disabled in order to reduce the inrush currents. As a result of these measures, none of the new DC-DC converters have failed by the time of this writing in October 2018.

The main goal of the Phase-1 upgrade of the CMS pixel detector, to cope with the increased instantaneous luminosity of the LHC and to preserve the tracking efficiency, was met. Figure 6.17 shows the single hit efficiency as a function of the instantaneous luminosity for the original and the upgraded detector. At the design value of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, the efficiency of all FPix disks and BPix layers 2 to 4 in the Phase-1 pixel detector is about 99 % or larger. The efficiency of the innermost layer of the barrel detector is about 97.5 %. The hit detection efficiency of the innermost layer of the Phase-0 pixel detector was already below 95 % at an instantaneous luminosity of $1.4 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, despite being further away from the interaction point. About 109 fb^{-1} of collision data have been recorded with the new pixel detector. This already exceeds the amount of data collected by the original pixel detector during its entire lifetime.

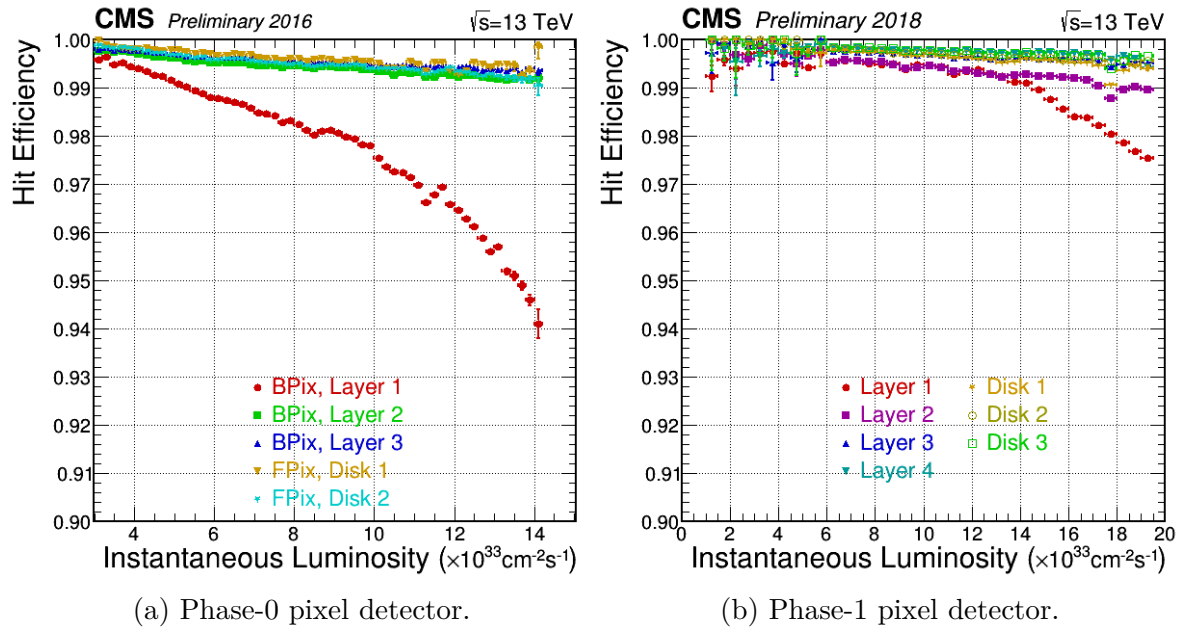


Figure 6.17.: Hit efficiency of the Phase-0 and the Phase-1 pixel detector as a function of the instantaneous luminosity, measured during the 2016 and 2018 data taking periods [117, 118].

7. Summary and Outlook

A new pixel detector was installed in the CMS experiment in winter 2016/2017. The so-called Phase-1 pixel detector was designed to provide the same or better tracking performance at an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ than the original pixel detector, which was designed for an instantaneous luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Among others, the readout chips were upgraded for this purpose. The new readout chips of type PSI46dig have larger buffers compared to the original chips, and use a new digital data format. The hit efficiency is above 99 % at the design instantaneous luminosity in most parts of the detector. Only in the innermost layer of the new barrel pixel detector, which has a radius of 2.9 cm instead of 4 cm, the changes are not sufficient. The PROC600 readout chip was developed for this layer. It has a new readout architecture in which the information of clusters of four pixels is copied into the memory instead of the hit information of individual pixels. The efficiency at a hit rate of 580 MHz cm^{-2} , which is expected in the innermost BPix layer, is about 98 %.

The new pixel detector has an additional third layer of pixel modules in the endcaps and an additional fourth layer in the barrel. As a result, the number of active channels has almost doubled. German institutes produced the 512 pixel modules required for the new outermost layer in the barrel. At the Karlsruhe Institute of Technology, 409 pixel modules were built between May 2015 and June 2016. These were tested in the context of this work at the RWTH Aachen University for possible use in the detector. Two test setups were developed for this purpose. In a cold box setup, the pixel modules were electrically tested at room temperature and with the foreseen cooling block temperature of -20°C . In these tests, defective pixels or pixels with a missing connection between ROC and sensor were searched for, among other possible defects. Furthermore, the current-voltage characteristics of the silicon sensors were measured. A grading scheme with four grades (A, B, C, C*) was used to characterize the pixel modules. Only pixel modules with grades A and B are used in the pixel detector. In the tests in the cold box, 3 % of 389 functioning pixel modules were rejected. For more than half of the modules, the leakage current did not scale as expected with the temperature, which is why grade B was assigned to these modules. This effect is not caused by the production of pixel modules at KIT but was observed in all production centers. In the cold box, the modules were also subjected to ten thermal cycles between -25°C and $+17^\circ\text{C}$ to ensure their long-term reliability. The thermal cycling did not introduce additional defective pixels in any of the pixel modules.

In addition, the pixel modules were tested in an X-ray setup. This setup uses an X-ray machine designed for didactic purposes in schools and universities. It is possible to

illuminate two pixel modules almost uniformly with hit rates of over 200 MHz cm^{-2} . Each pixel module was subjected to a high rate test to find defective pixels and inefficient readout chips. A majority of the rejected pixel modules did not pass at least one test in the X-ray setup. In total, 43 of 389 tested modules (11 %) were rejected in this setup. The average efficiency of the readout chips at a hit rate of 120 MHz cm^{-2} , which is expected in layer 2 of the barrel pixel detector, was $(99.20 \pm 0.13) \%$. The average number of defective pixels per module was about 8 out of 65 560 pixels. Furthermore, an energy calibration of the chip-internal charge injection mechanism with monochromatic X-rays from four different targets was performed. An average calibration factor of $45 \text{ e}^-/\text{Vcal unit}$ was determined. This factor is used to convert pulse heights measured by the readout chip into physical signal heights.

The pixel modules of all production centers were transported to ETH Zurich. There a short reception test was carried out to find possible damages caused by the transport. In addition, a protective cover was glued to the pixel modules produced at KIT. In the reception test, only one further pixel module was rejected. For 12 pixel modules, a significant change of the I-V curve compared to the measurement at RWTH Aachen University was observed. However, the leakage current was still low enough so that these modules were not sorted out. A total of 343 pixel modules were classified as grade A or B after all tests including the reception test. In relation to 409 produced full modules, the yield is 84 %. In relation to 437 produced bare modules (which consist only of a sensor and ROCs), the yield is 79 %.

Due to the almost doubled number of readout channels, the front-end currents of the new pixel detector have also increased by a factor of about two. With the classic direct powering scheme of the Phase-0 pixel detector this would have led to unacceptable losses in the cables. Due to space limitations inside the CMS detector, the number of supply cables could not be doubled. Therefore, a novel powering scheme was developed, in which higher voltages of about 10 V are fed to the detector and converted by DC-DC converters inside CMS to the voltages required by the pixel modules. By using DC-DC converters with output voltages of 2.4 V to 3.5 V the power dissipation in the cables could be reduced by about an order of magnitude. These output voltages take into account voltage drops on the supply lines of the pixel modules. The power supplies of the Phase-0 pixel detector could be reused after a modification.

The Phase-1 pixel detector is the first high-energy physics experiment to use DC-DC converters inside the detector. The operation in the 3.8 T magnetic field of CMS, the high particle flux density, and the large radiation doses put special demands on the DC-DC converters. Because commercial devices that meet the requirements are not available, the radiation tolerant buck converter ASIC FEAST2 was developed at CERN. Based on this chip, the so-called PixV13 DC-DC converter, which is optimized for the use in CMS, was developed at the I. Institute of Physics of RWTH Aachen University. Furthermore, large parts of the power system of the barrel pixel detector were designed at the RWTH Aachen University.

The results obtained in the context of this thesis demonstrated the proper functioning of the new power system. As part of this work, a system test setup was built in which all components of the power system of the barrel pixel detector are installed. Various measurements were carried out in this setup to validate the function of the power system. Among other things, voltage drops along the power lines on the supply tube were measured. With output currents of the DC-DC converters corresponding to an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, the voltage drops are in the range of about 500 mV to 600 mV, depending on the layer. Based on these measurements and taking into account other effects that reduce the output voltage of the DC-DC converters, output voltages of 2.4 V for the analog DC-DC converters, 3.5 V for the digital DC-DC converters in layer 2, and 3.3 V for all other digital DC-DC converters in BPix were selected. In FPix the output voltage of all digital DC-DC converters is 3.5 V.

The transient behavior of the BPix power system was investigated with the system test setup. Switching the input voltage on and off while nominal currents are drawn from the DC-DC converters results in current peaks of approximately twice the nominal value. If the DC-DC converters are disabled before such switching operations, current peaks can be prevented. Up to a load of about 1.1 times the nominal value, power supplies can be switched on without disabling the DC-DC converters beforehand. It could be shown that the remote sensing feature of the power supply works as expected and does not interfere with the regulation of the DC-DC converters.

Furthermore, the influence of DC-DC converter powering on the performance of pixel modules was investigated. Electronic noise and hit detection efficiency were measured. Without additional activity in the readout chips, no influence of the DC-DC converters was measurable. During irradiation with an X-ray machine, a pixel module was also operated at hit rates in the range of 100 MHz cm^{-2} . With power supplied by DC-DC converters under nominal load, the noise was not increased compared to power supplied by the digital test board. When introducing fast load variations that simulate the LHC orbit gap pattern, the noise increased from 170 to 179 electrons. Compared to the signal threshold of about 1600 electrons, this increase is unproblematic. The hit detection efficiency for powering with DC-DC converters under realistic loads at a hit rate of 120 MHz cm^{-2} was $(99.14 \pm 0.13) \%$. Within the measurement uncertainties, this value is compatible with powering by the test board. Powering with DC-DC converters in the system test setup also did not influence the result of the energy calibration.

In a long-term test setup, four fuses blew after 18 months of continuous operation of 26 DC-DC converters. A fuse is located on the PCB of each DC-DC converter to prevent the loss of entire power groups in the event of a short circuit at the input of a single DC-DC converter. An investigation of all fuses showed that they were subject to accelerated aging due to the cooling block temperature of about $+30^\circ \text{C}$ in the setup. Operation at a colder temperature of -20°C in CMS significantly reduces the aging effect. In measurements in the system test setup, fuses were operated with currents above the nominal value at different temperatures. Calculations and a measurement

predict a reduction of the aging rate by a factor of two for a temperature drop of about 7 K. According to this results, safe operation of the pixel detector for the complete lifetime is ensured.

In January 2017, the commissioning of the barrel pixel detector started at the Paul Scherrer Institute in Switzerland. Various tests were carried out to find possible problems with pixel modules or auxiliary electronics on the supply tubes. These tests were repeated after transporting the detector to CERN. In addition, optimal settings for the operation of the detector were determined. During the checkout, four fuses of DC-DC converters blew. Although this incident could be attributed to human error, a detailed evaluation of the operating parameters of the power system was carried out as part of this work. As a result of these investigations the output voltages of the power supplies were increased from the original value of 10.0 V to 11.4 V in FPix and 11.0 V in BPix. It was shown that with these values the pixel detector could be operated safely at an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Optimized procedures for switching the pixel detector on and off have been developed to prevent fuses from being damaged by inrush currents.

In February and March 2017, the BPix and the FPix detectors were installed into CMS. A few problems found during checkout could not be fixed without causing damage to other components. At the beginning of data collection in June 2017, the proportion of active channels in the pixel detector was 95.47 %. Since then, the detector has provided essential data for many physics analyses. For example, data recorded with the Phase-1 pixel detector were used for the recently published observation of the $H \rightarrow b\bar{b}$ decay [119].

A problem in the Token Bit Manager chip can put the TBM into a stuck state after a single event upset. In this case, a pixel module only delivers data again after power cycling. During the operation of the pixel detector in 2017, the power cycling was performed by disabling and enabling the associated DC-DC converters. Since October 2017, an increasing number of DC-DC converters have failed after power cycling, so that at the end of the year about 5 % of the devices installed in CMS were defective. Within the framework of this work, tests were carried out to find the reason for the failures. It was shown that the measurement of the I-V curves below the UVLO threshold voltage could be used to find possible damage to a DC-DC converter. The channels with defective DC-DC converters in CMS showed various irregularities in this measurement. In laboratory experiments, the failure mode observed in the pixel detector could not be reproduced. The theory of an overvoltage at the input of the FEAST2 ASIC could not be falsified. It was also not possible to determine the cause of the damage with measurements performed by other working groups.

In winter 2017/2018 the pixel detector was extracted from CMS, and the DC-DC converters were examined. For these tests, a setup was developed in the context of this work. For about 30 % of the working DC-DC converters, a larger than expected input current at voltages below the UVLO threshold was measured. In the following months, several tests were performed at CERN. As a result of these tests, the designers

of the FEAST2 ASIC were able to prove that a radiation-induced leakage current in the chip caused the damage. The leakage current is dangerous if the TID is in the range of 400 kRad to 6 MRad. The ASIC will only be damaged if it is disabled during operation.

All DC-DC converters installed in the pixel detector have been replaced. A new production was already started in November 2017. The new DC-DC converters, which are called PixV14, use a newer revision of the FEAST2 chip in which a problem of the PowerGood circuit is fixed. Larger fuses with values of 3 A (analog DC-DC converters) and 4 A (digital DC-DC converters) were equipped to be able to operate the detector at lower input voltages. Within only 11 weeks, all required devices were produced and tested. The tests performed during the original production as well as some additional tests were carried out. In the setup developed within the scope of this work, almost all DC-DC converters that failed the qualification tests were identified already at the assembly company. Further tests were performed at RWTH Aachen University. Among others, an active thermal cycling between -28°C and $+20^{\circ}\text{C}$ was performed. An assembly problem was found after the failure of one DC-DC converter. As a precaution, 33 DC-DC potentially affected DC-DC converters were rejected. The total yield of the production was 96.4 %

When the new DC-DC converters were produced, and also at the time of their installation in the pixel detector, no explanation for the defects had been found. Except for the changes mentioned above, no further changes have been made to the ASIC or the PCB design of the PixV14 DC-DC converters. It was assumed that if the DC-DC converters were operated in the same way as in 2017, this would again result in failures. As a consequence, the input voltage of the DC-DC converters was reduced to 9 V for operation in 2018, and the disabling feature is no longer used. Until the time of this writing in October 2018, none of the new DC-DC converters has failed.

It is planned to replace all DC-DC converters again during the Long Shutdown 2 in 2019 and 2020. A revision of the FEAST2 ASIC, in which the transistors that were damaged in the pixel detector are omitted, will be used for the new devices. In this revision, a 15 k Ω resistor has been introduced, such that excessive current in the V33Dr linear regulator can flow to ground instead of charging the external capacitance. Furthermore, a new ESD protection circuit has been added. It was also considered possible to add an external resistor in parallel to C9 on the DC-DC converter PCB. Two types of prototypes of the new DC-DC converters have already been produced. One type uses only the new revision of the ASIC, while the second type uses an additional resistor with a value of 3 k Ω . These prototypes are operated in the setup on the castor table. Results as to whether the external resistance must necessarily be used were not available as of October 2018.

During Long Shutdown 2, the pixel modules of the innermost layer of the barrel pixel detector will be replaced to mitigate the performance reduction caused by radiation-induced damage. A revision of the TBM, which makes regular power cycling unnecessary, is to be used for the new pixel modules. Furthermore, broken pixel modules of

layer 2, and the accessible broken pixel modules of layers 3 and 4 will be replaced by spare pixel modules.

This work made important contributions to the development of the power system, to the quality assurance during component production, and to the commissioning and debugging of problems of the Phase-1 pixel detector.

A. Appendix

A.1. DC-DC Converters

The following section contains additional material that explains the design of the DC-DC converters used in the pixel detector. Figure A.1 shows a circuit diagram of the PixV13 DC-DC converter. The design of the input and output filters in so-called π -topology is visible. The configuration of the enable circuit is chosen such that the DC-DC converter is switched on by default (active low). The output of the FEAST2 ASIC can be switched off by applying an external voltage to the enable pin.

Figure A.2 shows the layout of the top layer of the PixV13 DC-DC converter PCB. The copper layer is shown in green. Orange circles represent vias that connect to the second layer of the PCB. The electromagnetic shielding is soldered to the four blue square pads and the blue pentagonal pad.

Figure A.3 shows a block diagram of the FEAST2 ASIC. Among others, the integrated protection circuits (undervoltage, overcurrent, overtemperature), the control of the power transistors (labeled HS and LS), the V33Dr linear regulator, and the block for generating the PowerGood signal are shown.

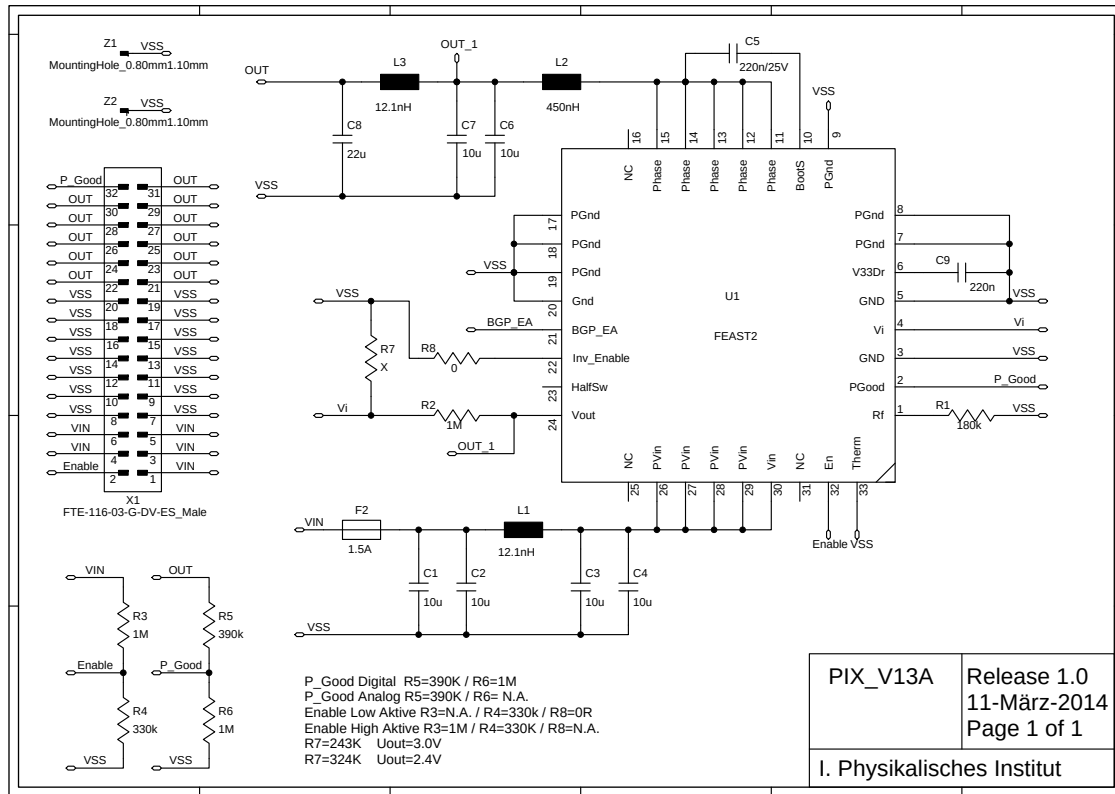


Figure A.1.: Schematic of the PixV13 DC-DC converter.

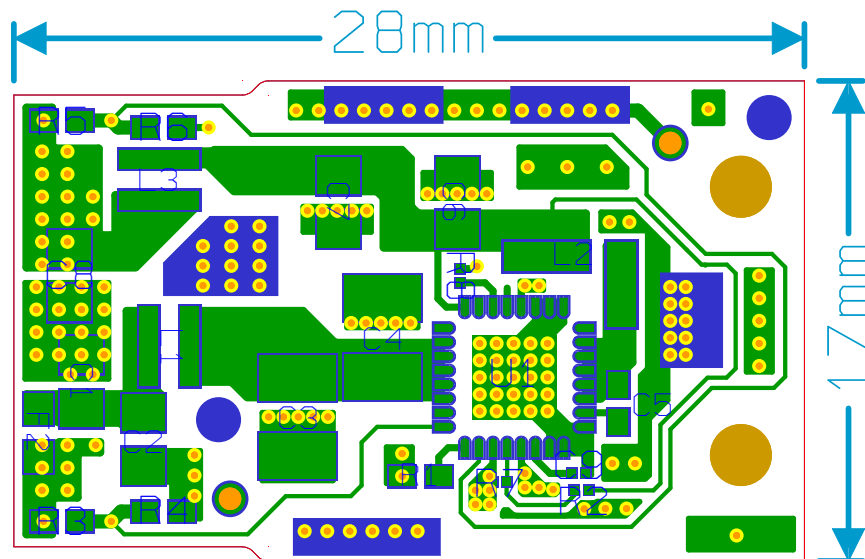


Figure A.2.: Schematic of the top layer of the PixV13 DC-DC converter PCB.

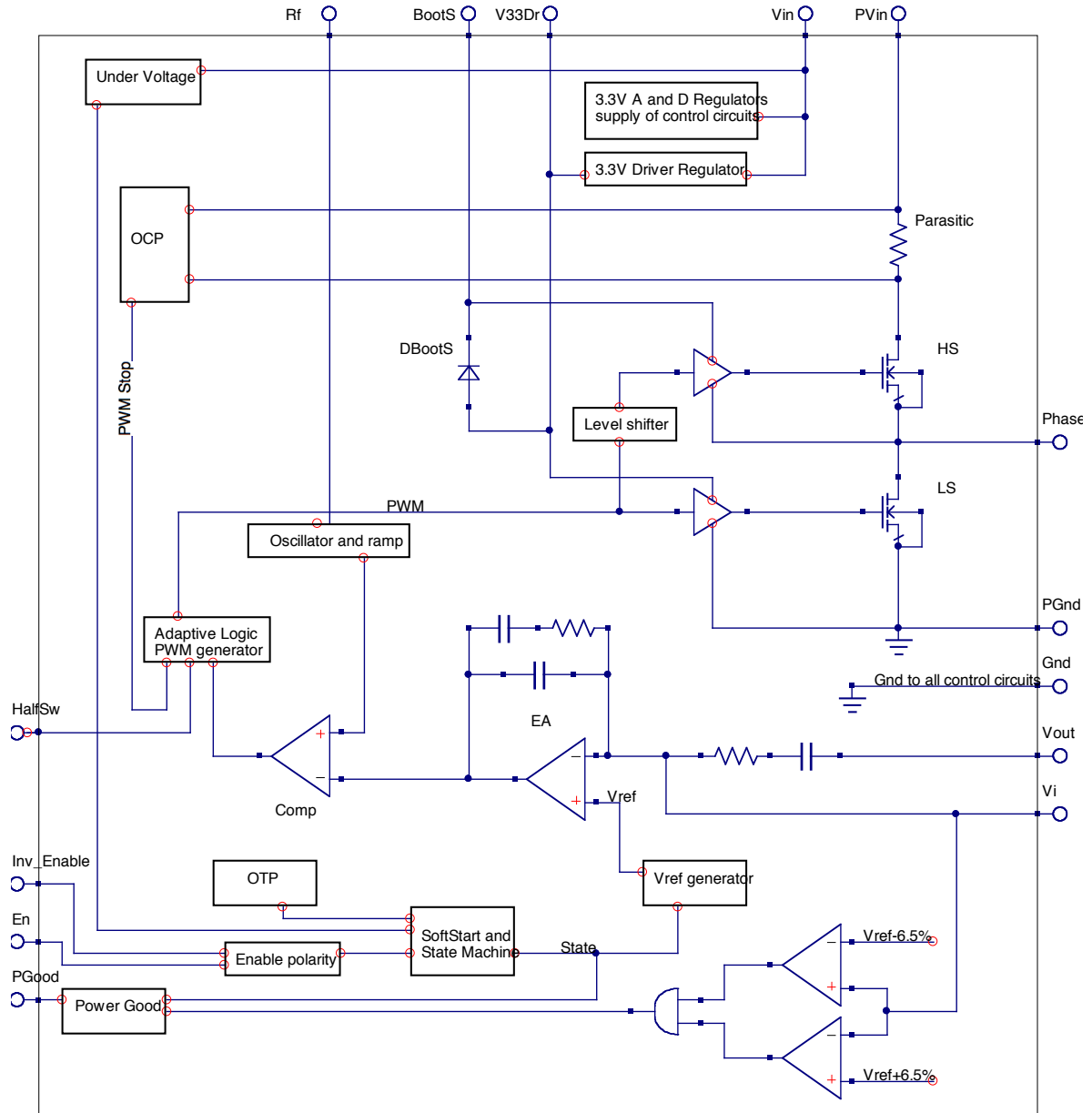


Figure A.3.: Block diagram of the FEAST2 ASIC [51].

A.2. Photographs of Supply Tube Boards

This section contains photographs of the boards used in the power system of the BPix detector. Figure A.4 shows one bus board, extension boards, adapter boards and the high voltage flex board in sections A and B of the supply tube. For illustrative purposes, the bus board is connected to a cooling loop of the CO₂ system used at RWTH Aachen University. In the pixel detector, each side of the bus board is cooled with individual cooling loops that extend along the entire supply tube and also cool the pixel modules. Figure A.5 shows a detailed view of the connector boards of layers 3 and 4, which are located in section C of the supply tube. Figure A.6 shows a photograph of a CCU ring board. It is equipped with CCUs for eight sectors and a ninth CCU located in the center of the PCB, that is used for redundancy. Four boards of this type are used in the Phase-1 pixel detector.

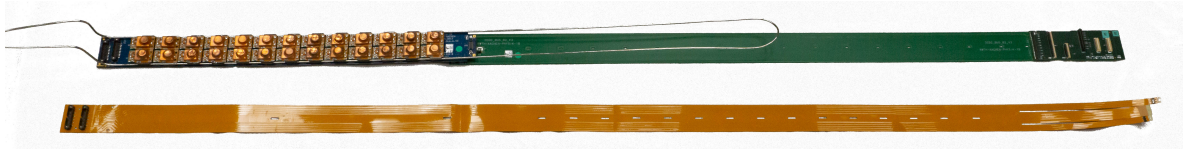


Figure A.4.: Photograph of boards in Section A and B of the supply tube. Top: bus board equipped with 26 DC-DC converters, extension boards and adapter boards. Bottom: high voltage flex board.

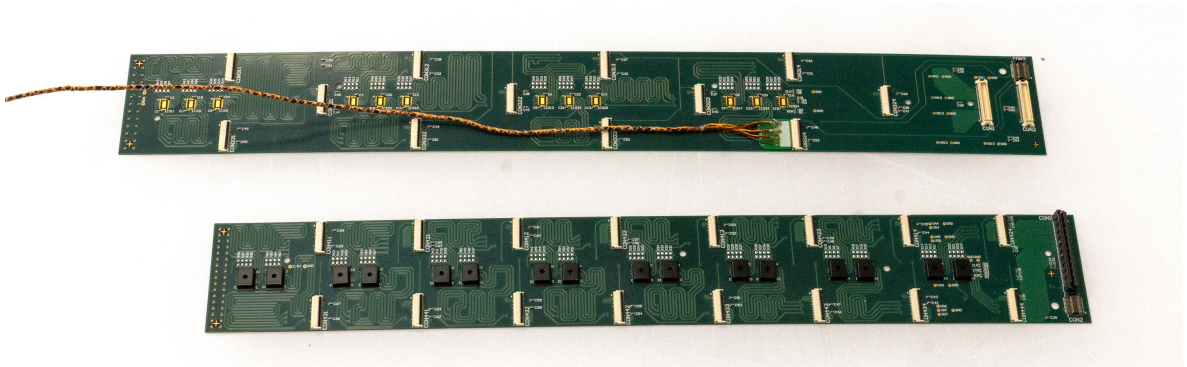


Figure A.5.: Photograph of the connector boards of layer 3 (top) and layer 4 (bottom). One pixel module cable is plugged into the layer 3 board for illustrative purposes.

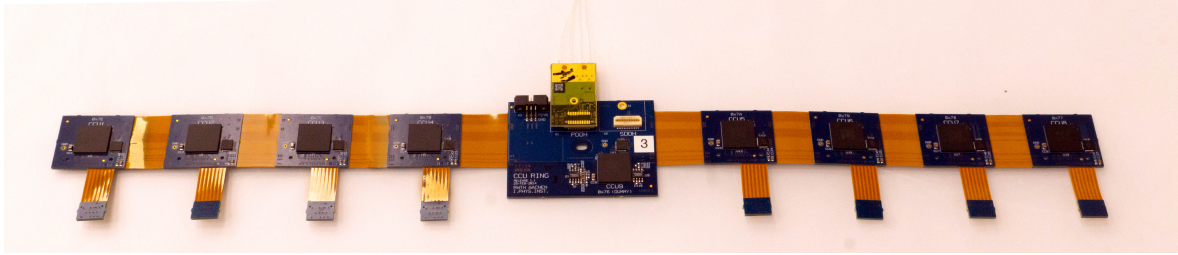


Figure A.6.: Photograph of the CCU ring board. One of two digital optohybrids (DOHs) is connected to the central part of the PCB.

A.3. Pixel Module Qualification

Figure A.7 shows an exemplary web page of the database that shows the grades assigned to individual pixel modules. The data generated by the pXar software during the module tests were uploaded to the database server. They were analyzed with MoReWeb, and a grade was assigned to the pixel modules. Test results of individual components, e.g. I-V curves of silicon sensors measured by the manufacturer, were also entered into the database. It was also used for tracking components.

A. Appendix

Home Inventory > Tools > Batches&Wafers > Sensors > HDI > Roc > BareModules > FullModules >														
Full Module Overview														
Draw histogram Draw for all Mod ID ▼ Xmin: Xmax: Nbins: LogY: ☐														
Select all Unselect all Exact per column search (you can still add the % yourself) Show 50 entries Search: Print Reset view														
Inventory					Full Qualification			More full tests		XRay tests			BareModule test	
Mod ID	Built By	Status	Center	Final Gr	FullQual	#Def	ROC>1%	Reception	OtherQual	VCal	HR	GR	Grade	
M4550	KIT	INSTOCK	ETH	B	B	20	0	B	A (DBTest)	(44.20,130.25)	A	A	A	
M4551	KIT	MOUNTED	ETH	B	B	21	0	A	A (Fulltest)	(46.65,-85.84)	A	A	A	1
M4552	KIT	MOUNTED	ETH	B	B	11	0	A	A (Fulltest)	(45.74,-103.05)	A	A	A	1
M4553	KIT	INSTOCK	ETH	B	B	24	0	A	A (Fulltest)	(43.79,78.09)	A	A	A	1
M4554	KIT	INSTOCK	ETH	C	B	59	1	A	B (Fulltest)	(47.15,-85.33)	C	C	A	1
M4555	KIT	MOUNTED	ETH	B	B	19	0	A	B (Fulltest)	(45.92,-38.94)	A	A	B-	0
M4556	KIT	INSTOCK	ETH	C	A	15	0		A (Fulltest)	(45.56,-107.47)	C	C	A-	1
M4557	KIT	MOUNTED	ETH	A	A	14	0	A	A (Fulltest)	(45.96,-133.44)	A	A	A	1
M4558	KIT	INSTOCK	ETH	C	A	15	0	A	A (Fulltest)	(45.81,-47.59)	C	C	A	1
M4559	KIT	MOUNTED	ETH	B	B	13	0	A	A (Fulltest)	(46.22,-34.34)	A	A	A	1
M4560	KIT	MOUNTED	ETH	A	A	16	0	A	A (Fulltest)	(45.18,-49.54)	A	A	A-	1
M4561	KIT	MOUNTED	ETH	A	A	35	0	A	A (Fulltest)	(46.25,3.57)	A	A	A	1
M4562	KIT	MOUNTED	ETH	A	A	21	0	A	A (Fulltest)	(44.02,-44.97)	A	A	A	1
M4563	KIT	INSTOCK	ETH	C	B	184	1	B	B (Fulltest)	(45.42,-47.29)	C	C	A	1
M4564	KIT	MOUNTED	ETH	B	B	91	1	A	C (Fulltest)	(45.10,-85.38)	A	A	A	1
M4565	KIT	MOUNTED	ETH	B	B	11	0	A	A (Fulltest)	(45.76,-30.36)	A	A	A	1
M4566	KIT	MOUNTED	ETH	A	A	23	0	A	A (Fulltest)	(45.78,-83.24)	A	A	A	0
M4567	KIT	MOUNTED	ETH	B	B	26	0	A	A (Fulltest)	(45.21,-123.77)	A	A	A	1
M4568	KIT	MOUNTED	ETH	B	B	14	0	A	A (Fulltest)	(44.70,-83.28)	A	A	A	1
M4569	KIT	MOUNTED	PSI	A	A	16	0	A	A (Fulltest)	(45.14,-154.32)	A	A	A-	1
M4570	KIT	MOUNTED	ETH	B	B	27	0	A	A (Fulltest)	(45.62,-17.51)	A	A	A	1
M4571	KIT	MOUNTED	PSI	A	A	28	0	A	A (Fulltest)	(45.90,-73.84)	A	A	A	1
M4572	KIT	MOUNTED	PSI	B	B	43	0	A	A (Fulltest)	(45.35,-47.87)	A	A	A	1
M4573	KIT	MOUNTED	ETH	A	A	17	0	A	A (Fulltest)	(46.99,-138.20)	A	A	A	1
M4574	KIT	MOUNTED	PSI	B	B	10	0	A	A (Fulltest)	(47.27,-83.11)	A	A	A	1
M4575	KIT	BROKEN	KIT	C	C	-1	-1		-	(-1.00,-1.00)	C	C	A	1
M4576	KIT	MOUNTED	ETH	A	A	15	0	A	A (Fulltest)	(46.08,-66.02)	A	A	A	1
M4577	KIT	MOUNTED	ETH	A	A	20	0	A	A (Fulltest)	(45.98,-154.32)	A	A	A-	1
M4578	KIT	BROKEN	KIT	C	C	-1	-1		B (Fulltest)	(-1.00,-1.00)	C	C	A	1
M4579	KIT	MOUNTED	PSI	A	A	19	0	A	A (Fulltest)	(45.79,-131.32)	A	A	A	1
M4580	KIT	MOUNTED	PSI	A	A	17	0	A	A (Fulltest)	(44.92,8.93)	A	A	A-	1
M4581	KIT	MOUNTED	ETH	A	A	16	0	A	A (Fulltest)	(45.70,22.46)	A	A	A	1
M4582	KIT	BROKEN	KIT	C	C	-1	-1		C (Fulltest)	(-1.00,-1.00)	C	C	A	1
M4583	KIT	MOUNTED	ETH	A	A	37	0	A	A (Fulltest)	(45.29,-51.19)	A	A	A-	1
M4584	KIT	INSTOCK	ETH	C	B	15	0		B (Fulltest)	(46.06,-105.20)	C	C	A	1
M4585	KIT	MOUNTED	ETH	A	A	8	0	A	A (Fulltest)	(45.80,-75.17)	A	A	A	1
M4586	KIT	MOUNTED	ETH	B	B	17	0	A	B (Fulltest)	(45.23,-98.06)	A	A	A	1
M4587	KIT	BROKEN	KIT	C	C	-1	-1		C (Fulltest)	(-1.00,-1.00)	C	C	A	1
M4588	KIT	MOUNTED	ETH	B	B	15	0	A	A (Fulltest)	(45.09,-23.35)	A	A	A	1
M4589	KIT	MOUNTED	ETH	B	B	11	0	A	B (Fulltest)	(45.39,30.66)	A	A	A	1
M4590	KIT	MOUNTED	ETH	A	A	29	0	A	A (Fulltest)	(45.13,-11.25)	A	A	A-	1
M4591	KIT	MOUNTED	ETH	A	A	21	0	A	A (Fulltest)	(44.76,-65.65)	A	A	A	1
M4592	KIT	MOUNTED	PSI	A	A	18	0	A	A (Fulltest)	(44.37,12.24)	A	A	A	1
M4593	KIT	MOUNTED	PSI	B	B	35	0	A	B (Fulltest)	(48.01,0.29)	A	A	A	1

Figure A.7.: Screenshot of the GUI of the database, which was used to keep track of parts and testing results across all production centers.

A.4. Optimization of the Power Supply Output Voltages

This section contains supplementary material that was used for the optimization of the output voltages of the power supplies, which is described in Section 5.2.1. Figure A.8 shows the calculated voltage drops for all digital power channels of the Phase-1 pixel detector at an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. For the voltage drops in FPix, the nominal resistances were assumed. The remote sensing feature of the power supply can be used to compensate for voltage drops along the MS cable. The twisted pair cables that connect the filter boards to the DC-DC motherboards have no sense wires. The total voltage drop is the sum of the voltage drops along both parts. For the BPix detector, measured values of the cable resistances were used. The calculation assumes that the remote sensing feature is used, and that the power supply set voltages are 11.0 V and 11.4 V in BPix and FPix, respectively. Figure A.9 shows the calculated output voltage of all digital power supply channels in case the remote sensing feature is used.

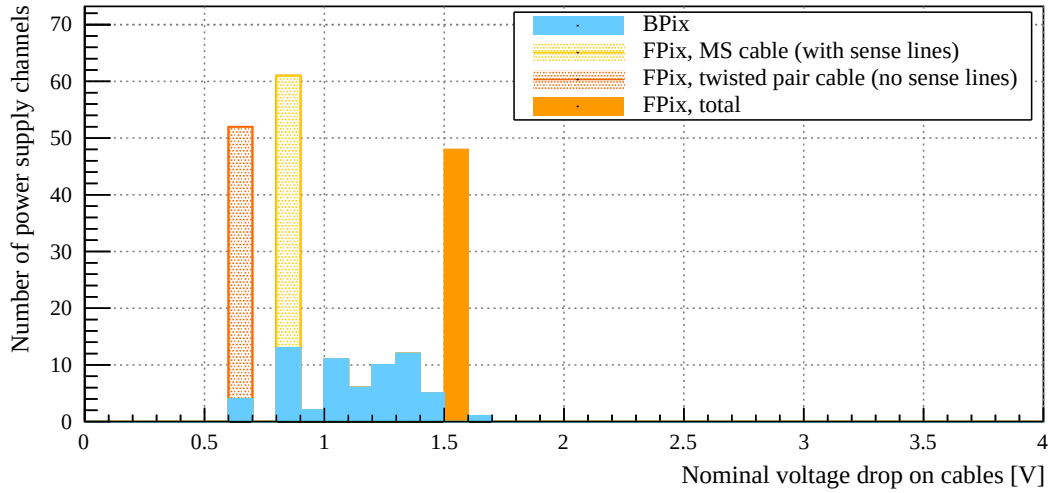


Figure A.8.: Expected voltage drops across the supply lines between the power supplies and the DC-DC converters, shown for all digital power channels of the Phase-1 pixel detector. The values are calculated for an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$.

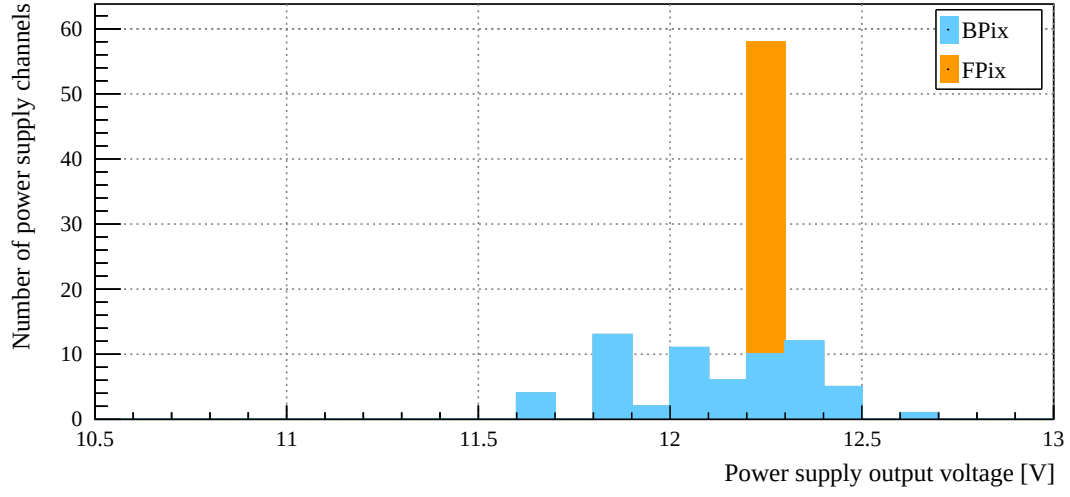


Figure A.9.: Output voltages of the power supplies in case the remote sensing feature is used, shown for all digital power channels of the Phase-1 pixel detector. The values are calculated for an instantaneous luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and set voltages of 11.0 V and 11.4 V in BPix and FPix, respectively.

Bibliography

- [1] ATLAS Collaboration, *Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC*, Phys. Lett. B **716** (2012) 1–29.
- [2] CMS Collaboration, *Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC*, Phys. Lett. B **716** (2012) 30–61.
- [3] CERN, *CERN Website*.
URL: <http://home.cern> (visited on September 13, 2018).
- [4] L. Evans and P. Bryant, *LHC Machine*, 2008 JINST **3** S08001.
- [5] CMS Collaboration, *CMS Luminosity - Public Results*.
URL: <https://twiki.cern.ch/twiki/bin/view/CMSPublic/LumiPublicResults> (visited on September 13, 2018).
- [6] P. Malek, *Aufbau und Inbetriebnahme eines Kälteteststandes für Pixelmodule des CMS Phase 1 Upgrades*, Master thesis, RWTH Aachen University (2014).
- [7] M. Lipinski, *Charakterisierung und Energiekalibration von Prototypen der Pixelmodule für das CMS Phase 1 Upgrade mit einem Röntgenteststand*, Master thesis, RWTH Aachen University (2014).
- [8] C. Lefevre, *LHC: the guide (English version)*, Geneva (2009).
- [9] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, 2008 JINST **3** S08003.
- [10] CMS Collaboration, *The CMS experiment at the CERN LHC*, 2008 JINST **3** S08004.
- [11] LHCb Collaboration, *The LHCb Detector at the LHC*, 2008 JINST **3** S08005.
- [12] ALICE Collaboration, *The ALICE experiment at the CERN LHC*, 2008 JINST **3** S08002.
- [13] CERN Council, *The Large Hadron Collider Project*, Report CERN/2039 Geneva (1994).
- [14] CERN Council, *Resolution Approval of the Large Hadron Collider (LHC) Project*, Report CERN/2075 Geneva (1995).
- [15] T. Schörner-Sadenius, *The Large Hadron Collider: Harvest of run 1*, Springer International Publishing (2015), ISBN: 978-3-319-15001-7.

- [16] CERN, *Accelerator Performance and Statistics*.
URL: <http://acc-stats.web.cern.ch/acc-stats/#lhc/> (visited on July 12, 2018).
- [17] I. Bejar et al., *High-Luminosity Large Hadron Collider (HL-LHC) Technical Design Report V. 0.1*, Technical Report CERN-2017-007-M, Geneva (2017).
- [18] CERN, *LHC long term schedule - LHC commissioning*.
URL: <https://lhc-commissioning.web.cern.ch/lhc-commissioning/schedule/HL-LHC-plots.htm> (visited on July 13, 2018).
- [19] CERN, *CMS detector design*.
URL: <http://cms.web.cern.ch/news/cms-detector-design> (visited on February 25, 2014).
- [20] CMS Collaboration, *The CMS tracker system project: Technical Design Report*, Technical Report CERN-LHCC-98-006, CMS-TDR-5, Geneva (1997).
- [21] CMS Collaboration, *The CMS tracker: addendum to the Technical Design Report*, Technical Report CERN-LHCC-2000-016, CMS-TDR-5-add-1, Geneva (2000).
- [22] CMS Collaboration, *CMS Tracking Performance Results from early LHC Operation*, The European Physical Journal C **70** (2010) 1165–1192.
- [23] J. Karancsi, *Operational experience with the CMS pixel detector in LHC Run II*, 2016 JINST **11** C12057.
- [24] CMS Collaboration, *The CMS tracker operation and performance at the Magnet Test and Cosmic Challenge*, 2008 JINST **3** P07006.
- [25] CMS Collaboration, *Energy calibration and resolution of the CMS electromagnetic calorimeter in pp collisions at $\sqrt{s} = 7$ TeV*, 2013 JINST **8** P09009.
- [26] CMS Collaboration, *The CMS muon project: Technical Design Report*, Technical Report CERN-LHCC-97-032, CMS-TDR-3, Geneva (1997).
- [27] The CMS collaboration, *The performance of the CMS muon detector in proton-proton collisions at $\sqrt{s} = 7$ TeV at the LHC*, 2013 JINST **8** P11002.
- [28] CMS Collaboration, *CMS TriDAS project: Technical Design Report, Volume 1: The Trigger Systems*, Technical Report CERN-LHCC-2000-038, CMS-TDR-6-1, Geneva (2000).
- [29] CMS Collaboration, *Technical proposal for the upgrade of the CMS detector through 2020*, Technical Report CERN-LHCC-2011-006, LHCC-P-004, Geneva (2011).
- [30] CMS Collaboration, *CMS Technical Design Report for the Level-1 Trigger Upgrade*, Technical Report CERN-LHCC-2013-011, CMS-TDR-12, Geneva (2013).
- [31] CMS Collaboration, *CMS Technical Design Report for the Phase 1 Upgrade of the Hadron Calorimeter*, Technical Report CERN-LHCC-2012-015, CMS-TDR-10, Geneva (2012).

-
- [32] CMS Collaboration, *CMS technical design report for the pixel detector upgrade*, Technical Report CERN-LHCC-2012-016, CMS-TDR-11, Geneva (2012).
 - [33] CMS Collaboration, *The Phase-2 Upgrade of the CMS Tracker*, Technical Report CERN-LHCC-2017-009, CMS-TDR-014, Geneva (2017).
 - [34] CMS Collaboration, *The Phase-2 Upgrade of the CMS Muon Detectors*, Technical Report CERN-LHCC-2017-012, CMS-TDR-016, Geneva (2017).
 - [35] CMS Collaboration, *CMS Technical Design Report for the Muon Endcap GEM Upgrade*, Technical Report CERN-LHCC-2015-012, CMS-TDR-013, Geneva (2015).
 - [36] H. C. Kästli, *Frontend electronics development for the CMS pixel detector upgrade*, Nucl. Instr. Meth. A **731** (2013) 88–91.
 - [37] H. C. Kästli et al., *Design and performance of the CMS pixel detector readout chip*, Nucl. Instr. Meth. A **565** (2006) 188–194.
 - [38] A. Starodumov, P. Berger, and M. Meinhard, *High rate capability and radiation tolerance of the PROC600 readout chip for the CMS pixel detector*, 2017 JINST **12** C01078.
 - [39] E. Bartz, *The token bit manager chip for the CMS pixel readout*, CERN-2003-006 pp.185-189 (2003).
 - [40] M. Barbero et al., *Design and test of the CMS pixel readout chip*, Nucl. Instr. Meth. A **517** (2004) 349–359.
 - [41] B. Meier, *CMS pixel detector with new digital readout architecture*, 2011 JINST **6** C01011.
 - [42] S. Spannagel, B. Meier, and H. C. Perrey, *The pxarCore Library - Technical Documentation, Reference Manual, and Sample Applications*, Geneva (2015).
 - [43] J. H. Hoß, *Search for Supersymmetry with Multiple Charged Leptons at $\sqrt{s} = 13$ TeV with CMS and Radiation Tolerance of the Readout Chip for the Phase I Upgrade of the Pixel Detector*, PhD thesis, ETH Zürich (2017).
 - [44] CMS Collaboration, *Test Beam Performance Measurements for the Phase I Upgrade of the CMS Pixel Detector*, 2017 JINST **12** P05022.
 - [45] S. Spannagel, *Test Beam Measurements for the Upgrade of the CMS Pixel Detector and Measurement of the Top Quark Mass from Differential Cross Sections*, PhD thesis, Deutsches Elektronen-Synchrotron (2015).
 - [46] J. Troska et al., *Prototype pixel optohybrid for the CMS phase 1 upgraded pixel detector*, 2012 JINST **7** C01113.
 - [47] PICMG, *MicroTCA*.
URL: <https://www.picmg.org/openstandards/microtca/> (visited on September 13, 2018).
 - [48] M. Pesaresi et al., *The FC7 AMC for generic DAQ & control applications in CMS*, 2015 JINST **10** C03036.

- [49] C. Paillard, C. Ljuslin, and A. Marchioro, *The CCU25: a network oriented Communication and Control Unit integrated circuit in a 0.25 μm CMOS technology*, CERN 2002-003 pp.174-178 (2002).
- [50] J. Sammet, *A novel powering scheme based on DC-DC conversion for the luminosity upgrades of the CMS tracking system at CERN*, PhD thesis, RWTH Aachen University (2014).
- [51] F. Faccio and S. Michelis, *FEAST2.1 datasheet*.
URL: <http://project-dcdc.web.cern.ch/project-dcdc/public/Documents/FEAST2.1%20datasheet.pdf> (visited on July 12, 2018).
- [52] ON Semiconductor, *I3T80: 0.35 μm Process Technology*.
URL: <http://www.onsemi.com/pub/Collateral/I3T80-D.PDF> (visited on October 23, 2018).
- [53] F. Faccio and S. Michelis, *FEASTMP datasheet - rev 2.1*.
URL: http://project-dcdc.web.cern.ch/project-dcdc/public/Documents/FEAST2Mod_Datasheet.pdf (visited on July 12, 2018).
- [54] Costruzioni Apparecchiature Elettroniche Nucleari (CAEN) S.p.A., *MOD. SY 1527 User's Manual Rev.18*.
URL: <http://www.caen.it/servlet/checkCaenManualFile?Id=8221> (visited on November 2, 2018).
- [55] Costruzioni Apparecchiature Elettroniche Nucleari (CAEN) S.p.A., *EASY3000 / 4000 Embedded Assembly SYstem*.
URL: www.caen.it/servlet/checkCaenManualFile?Id=10067 (visited on November 2, 2018).
- [56] S. Timpone, *Laser Welding of the CMS FPIX Phase 1 Upgrade Cooling Pipes*, Forum on Tracking Detector Mechanics 2016 Bonn (2016).
- [57] B. Verlaat and A. Colijn, *CO₂ Cooling Developments for HEP Detectors*, PoS (VERTEX2009) 031 (2009).
- [58] A. Colijn and B. Verlaat, *CO₂ Cooling for Particle Physics Experiments*, 9th IIF/IIR Gustav Lorentzen Conference on Natural Working Fluids, Sydney (2010).
- [59] S. Dambach et al., *Qualification of the CMS Barrel Pixel Detector Modules*.
URL: <http://www.phys.ethz.ch/~ursl/home/v0/projects/main.pdf> (visited on February 3, 2014).
- [60] National Instruments, *LabVIEW*.
URL: <http://www.ni.com/labview/> (visited on October 23, 2018).
- [61] B. Hiti, *Probe Station for Functionality Tests of Bare Modules for the Phase I Upgrade of the CMS Pixel Detector*, Diploma thesis, Karlsruhe Institute of Technology (2015).
- [62] F. Colombo, *Packaging and assembly technologies for the pixel detector upgrade and measurement of $\tau\tau$ final states with the CMS experiment at the LHC*, PhD thesis, Karlsruhe Institute of Technology (2016).

-
- [63] S. Heindl, *Bau und Qualitätssicherung von Modulen und Studie von optimierten Pixelsensordesigns für die Erneuerung des CMS-Pixeldetektors*, PhD thesis, Karlsruhe Institute of Technology (2016).
- [64] B. Freund, *Modulproduktion für den CMS-Phase-I-Pixeldetektor und Untersuchung der erwarteten Leistungsfähigkeit über dessen Betriebsdauer*, PhD thesis, Karlsruhe Institute of Technology (2017).
- [65] F. Kreith and D. Y. Goswami, *The CRC handbook of mechanical engineering*, 2. ed., CRC Press Boca Raton (2005), ISBN: 0849308666.
- [66] M. Dall’Osso, *Production of the new pixel detector for the upgrade of the CMS experiment and study of anomalous couplings in the non-resonant Higgs bosons pair production in p - p collisions at $\sqrt{s} = 13$ TeV*, PhD thesis, Padua University (2016).
- [67] CMS Collaboration, *pXar - pixel Xpert analysis & readout*.
URL: <https://github.com/psi46/pxar> (visited on July 23, 2018).
- [68] R. Brun and F. Rademakers, *ROOT - An object oriented data analysis framework*, Nucl. Instr. Meth. A **389** (1997) 81–86.
- [69] JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, *Chip-Package Interaction Understanding, Identifikation, and Evaluation*, JEP156A (2018).
- [70] JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, *3D Chip Stack with Through-Silicon Vias (TSVS): Identifying, Evaluating and Understanding Reliability Interactions*, JEP158 (2009).
- [71] Peter Huber Kältemaschinenbau AG, *Unichiller 020Tw*.
URL: https://www.huber-online.com/download/pdf_datasheets/deutsch/3024.0025.01.PDF (visited on October 29, 2018).
- [72] Honeywell International, *HIH-4000 Series Humidity Sensors*.
URL: <https://sensing.honeywell.com/honeywell-sensing-hih4000-series-product-sheet-009017-5-en.pdf> (visited on October 29, 2018).
- [73] Keithley Instruments, *Keithley Series 2700 Multimeter/Data Acquisition/Switch Systems*.
URL: <https://uk.tek.com/keithley-switching-and-data-acquisition-systems/keithley-2700-multimeter-data-acquisition-switch-sys> (visited on July 24, 2018).
- [74] Keithley Instruments, *Model 2410 High-Voltage SourceMeter*.
URL: <https://www.tek.com/keithley-source-measure-units/keithley-smu-2400-series-sourcemeter> (visited on July 23, 2018).
- [75] National Instruments, *Application Design Patterns: Master/Slave*.
URL: <http://www.ni.com/white-paper/3022/en/> (visited on July 23, 2018).
- [76] F. M. Hartmann, *Evolution of silicon sensor technology in particle physics*, 2. ed., Springer International Publishing (2017), ISBN: 9783319644349.

- [77] LD DIDACTIC GmbH, *Röntgengerät*.
URL: <https://www.leybold-shop.de/roentgengeraet-mo-komplett-554801.html> (visited on October 29, 2018).
- [78] Peter Huber Kältemaschinenbau AG, *Ministat 230-cc-NR Betriebsanleitung*.
URL: <http://www.huber-online.com/download/datasheets/abverkauf/de/2015.0012.04.PDF> (visited on October 23, 2018).
- [79] G. Cowan, *Error analysis for efficiency*.
URL: <http://www.hep.ph.rhul.ac.uk/~cowan/stat/notes/efferr.pdf> (visited on September 23, 2018).
- [80] H. Kolanoski and N. Wermes, *Teilchendetektoren: Grundlagen und Anwendungen*, Springer Berlin, Heidelberg (2016), ISBN: 9783662453506.
- [81] R. D. Deslattes et al., *X-ray transition energies: new approach to a comprehensive evaluation*, Rev. Mod. Phys. **75** (2003) 35–99.
- [82] P. Trüb, *CMS pixel module qualification and Monte-Carlo study of $H \rightarrow \tau^+ \tau^- \rightarrow l^+ l^- E_T$* , PhD thesis, ETH Zürich (2008).
- [83] K. H. Pries and J. M. Quigley, *Testing complex and embedded systems*, CRC Press Boca Raton (2011), ISBN: 9781439821404.
- [84] L. Feld et al., *A DC-DC conversion powering scheme for the CMS Phase-1 pixel upgrade*, 2013 JINST **8** C02024.
- [85] D. Rittich, *Charakterisierung von DC-DC-Konvertern für das Phase-1-Upgrade des CMS-Pixeldetektors*, Master thesis, RWTH Aachen University (2013).
- [86] L. Feld et al., *Development of a DC-DC conversion powering scheme for the CMS Phase-1 pixel upgrade*, 2014 JINST **9** C01048.
- [87] C. Fimmers, *Systemtestmessungen zur Spannungsversorgung für das Phase-1-Upgrade des CMS-Pixeldetektors*, Bachelor thesis, RWTH Aachen University (2013).
- [88] L. Feld et al., *Experience from design, prototyping and production of a DC-DC conversion powering scheme for the CMS Phase-1 Pixel Upgrade*, 2016 JINST **11** C02033.
- [89] L. Feld et al., *Experience from design, prototyping and production of a DC-DC conversion powering scheme for the CMS Phase-1 Pixel Upgrade*, Nucl. Instr. Meth. A **845** (2017) 591–594.
- [90] Delta Elektronika, *SM 1500 Series*.
URL: https://www.delta-elektronika.nl/upload/DATA_SHEET_SM1500_V201801.pdf (visited on October 30, 2018).
- [91] OPC Foundation, *OPC Foundation Website*.
URL: <https://opcfoundation.org/> (visited on August 19, 2018).
- [92] F. Scholz, *Untersuchung der Eigenschaften eines CO₂ Kühlsystems für das Upgrade des CMS-Spurdetektors*, Bachelor thesis, RWTH Aachen University (2012).

-
- [93] M. Preuten, *Thermische Designstudien für die Upgrades des CMS Pixel- und Spurdetektors*, Diploma thesis, RWTH Aachen University (2013).
- [94] W. Bertl (deceased), private communication, *Bpix2017_12f_power_distribution_v13.1.xlsm*, April 28, 2014.
- [95] Teledyne LeCroy, *CP031 Operator's Manual*.
URL: <http://teledynelecroy.com/probes/current-probes/cp031> (visited on August 28, 2018).
- [96] Teledyne LeCroy, *AP015 Current Probe Operator's Manual*.
URL: http://cdn.teledynelecroy.com/files/manuals/ap015_current_probe_manual.pdf (visited on August 28, 2018).
- [97] Keithley Instruments, *Integra Series Data Sheet*.
URL: <https://uk.tek.com/datasheet/2700-multimeter-data-acquisition-switch-systems/integra-series-technical-data-sheet> (visited on October 8, 2018).
- [98] Teledyne LeCroy, *CP03x/CP03xa Current Probe Operators Manual*.
URL: <http://cdn.teledynelecroy.com/files/manuals/cp03x-cp03xa-current-probe-operators-manual.pdf> (visited on September 10, 2018).
- [99] LeCroy, *WaveSurfer® Xs-A and MXs-A Oscilloscopes*.
URL: <https://www.manualslib.com/manual/563799/Lecroy-Xs-A.html> (visited on October 8, 2018).
- [100] A. Kornmayer (KIT), private communication, *Stress test of ROCs with Elevated Digital Voltage*, July 25, 2018.
- [101] R. Horisberger (PSI), private communication, September 10, 2015.
- [102] Raspberry Pi Foundation, *Raspberry Pi 1 Model B+*.
URL: <https://www.raspberrypi.org/products/raspberry-pi-1-model-b-plus/> (visited on August 31, 2018).
- [103] David Chapman, *High Conductivity Copper for Electrical Engineering*, CDA Publication 122, Copper Development Association (2016).
- [104] Deutsches Kupferinstitut, *Kupfer-Zinn und Kupfer-Zinn-Zink-Gusslegierungen (Zinnbronzen)*.
URL: https://www.kupferinstitut.de/fileadmin/user_upload/kupferinstitut.de/de/Documents/Shop/Verlag/Downloads/Werkstoffe/i025.pdf (visited on October 9, 2018).
- [105] SCHURTER AG, private communication, September 09, 2017.
- [106] Y. Wu et al., *The formation and growth of intermetallics in composite solder*, Journal of Electronic Materials **22** (1993) 769–777.

- [107] M. Rauch, *Thermal Measurements and FEA of the 2S Module for the CMS Phase-2 Tracker Upgrade*.
URL: https://indico.cern.ch/event/590227/contributions/2613219/attachments/1486462/2308577/MaxRauch_20170703.pdf (visited on September 4, 2018).
- [108] G. Cervelli et al., *A radiation tolerant laser driver array for optical transmission in the LHC experiments*, CERN 2001-005 pp.155–159 (2001).
- [109] L. Caminada (PSI), private communication, *TBM Phases*, Mai 05, 2017.
- [110] CMS Collaboration, *Active Channels Summary*.
URL: <https://twiki.cern.ch/twiki/bin/view/CMSPublic/ActiveChannelsSummary> (visited on September 20, 2018).
- [111] G. Bolla (deceased), private communication, September 09, 2014.
- [112] W. Johns (Vanderbilt), private communication, March 17, 2017.
- [113] K. Klein (RWTH Aachen), private communication, August 21, 2014.
- [114] V. Veszpremi, *Performance verification of the CMS Phase-1 Upgrade Pixel detector*, 2017 JINST **12** C12010.
- [115] F. Faccio, S. Michelis, and G. Ripamonti, *Summary of measurements on FEAST2 modules to understand the failures observed in the CMS pixel system*.
URL: <http://project-dcdc.web.cern.ch/project-dcdc/public/Documents/SummaryMeasurements18.pdf> (visited on October 24, 2018).
- [116] F. Faccio, *FEAST2.1 irradiation in the IRRAD facility*.
URL: http://project-dcdc.web.cern.ch/project-dcdc/public/Documents/Report_IRRAD_tests.pdf (visited on October 30, 2018).
- [117] CMS Collaboration, *Run II Pixel Performance plots for data and simulation*.
URL: <https://twiki.cern.ch/twiki/bin/view/CMSPublic/PixelOfflinePlots2016> (visited on October 30, 2018).
- [118] CMS Collaboration, *The Performance plots for Phase 1 Pixel Detector, August 2018*.
URL: <https://twiki.cern.ch/twiki/bin/view/CMSPublic/PixelOfflinePlotsAugust2018> (visited on October 30, 2018).
- [119] CMS Collaboration, *Observation of Higgs boson decay to bottom quarks*, Phys. Rev. Lett. **121** (2018) 121801.

Acknowledgements

I would like to thank all the people who have supported me in recent years. Working in a large international collaboration has been an enriching experience for me and has always been a pleasure. Many people have given me suggestions and support during my research. I would like to thank some of them in particular.

First, I would like to thank Prof. Dr. Lutz Feld, who gave me the opportunity to obtain my PhD degree. This thesis benefited significantly from his dedicated mentoring. I also thank him for his confidence in my work, which has enabled me to pursue my own ideas and strategies. Furthermore, I would like to thank Prof. Dr. Jörg Pretz for being the second assessor of this thesis. Many thanks to Dr. Katja Klein, who has provided me with valuable help and advice over many years.

For their professional support and their contributions to this work, I thank the members of the electronics and the mechanical departments of the I. Institute of Physics at RWTH Aachen University, especially Waclaw Karpinski and Michael Wloch, Sebastian Arendt, Karl-Heinz Dreger, Franz-Josef Neus, Irfan Ötzen, Gerhard Pierschel, and Stefan Schmitz.

I would also like to thank all the other members of the institute and the students in our working group for their organizational work, the constructive and pleasant working atmosphere, and the fruitful discussions. Special thanks go to Tanja Bingler, Natalie Drießen, Dr. Georg Schwering, and my long-time office colleagues Marius Preuten and Max Rauch. I would like to thank Samuel Möller and Frederic Stepp for their help during the pixel module qualification.

I would like to thank Dr. Danek Kotlinski and his colleagues from Paul Scherrer Institute for giving me the opportunity to participate in the checkout of the pixel detector.

Last but not least, I would like to thank my wife, my parents, and my brother for their constant support. Otherwise, this work would not have been possible.