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TID Tolerance of commercial 130nm CMOS Technologies for HEP experiments

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Introduction

The work presented in this thesis is a study of the radiation tolerance of commercial $0.13\mu\text{m}$ CMOS technologies, in view of their use in the design of Integrated Circuits (ICs) for High Energy Physics (HEP) experiments and it has been carried out in the Microelectronics group of CERN.

Today, the most challenging project of the High Energy Physics (HEP) community is the Large Hadron Collider (LHC), a new accelerator currently under construction at CERN. The main goal of the LHC is to answer some of the fundamental questions in physics, the most important concerning the origin of matter. It will start its operation in 2007 providing collisions between protons and lead ions at energies never attained before (14TeV at the centre of mass for protons and 1148TeV for lead ions). Four main detectors (i.e. experiments), called ATLAS, CMS, LHCb and ALICE, will be built around each collision point along the particles trajectory to study the products of the collisions. Each detector will be equipped with electronic circuits to read the signals generated by the particles crossing it.

Due to the high density of channels needed for the read-out operation, the electronic equipment for the detector system of the LHC has to be made of integrated circuits. The latter are customized to match the requirements of the particular application in which they are involved, hence becoming what's called Application Specific Integrated Circuits (ASICs).

Low power consumption is required as well to relax the cooling requirements: the cooling system should be the less intrusive as possible not to disturb the trajectory of the particles.

The most important requirement for ASICs in HEP experiments is that they must be radiation-tolerant. In such experiments, very high radiation levels are reached. For instance, in the LHC, due to the kinds of particles accelerated and to the high luminosity of this accelerator ($10^{34}\text{cm}^{-2}\text{s}^{-1}$ and $19.5\cdot 10^{27}\text{cm}^{-2}\text{s}^{-1}$ respectively for protons and lead ions), the total dose expected in 10 years experiment life-time, close to the collision point, is of the order of tens of Mrad, a value 10 to 100 times higher than the one reached

in spatial applications. Fluences of neutrons and hadrons of the order of 10^{14} particles/cm² will be present too.

In order to face these severe conditions from a radiation standpoint, at the beginning of the 90s several HEP groups investigated the possibility of using special technologies, called radiation hardened, for ASICs design. These technologies use particular processing methods to improve the radiation tolerance of integrated circuits. In most cases this effort was unsuccessful. Due to the small market represented by ICs for HEP experiments, radiation hardened technologies are more expensive and less technologically advanced than commercial ones (usually a couple of generations behind) and often suffer problems such as low yield and unreliable radiation performance for large quantities. Variation of the devices parameters can even occur from lot to lot and from wafer to wafer as well. In addition to that, these processes were discontinued and foundries closed due the drop of demand. Radiation hardened technologies were in fact developed especially for defense electronics, which represented the 70% of the market in 1960. In 1999 this percentage was reduced to only the 0.5%.

On the other hand, the use of commercial CMOS technologies has several beneficial aspects such as speed, reduced power consumption, high level of integration, high volume production (i.e. low cost and high yield). Moreover, the inherent radiation tolerance of commercial CMOS technologies improves in successive generations. As it will be seen in chapter 1, in a MOS (Metal-Oxide-Semiconductor) transistor the part most sensitive to radiation effects is the gate oxide. One way to reduce the effects of ionizing radiation is to reduce its thickness. An example is shown figure 1, where the radiation-induced threshold voltage shift of a MOS transistor is plotted as function of the gate oxide thickness. The threshold voltage shift decreases as $(t_{ox})^2$, for t_{ox} down to $0.35\mu\text{m}$, and even more for smaller values of the oxide thickness.

Reducing the gate oxide thickness is a natural trend in modern technologies. The market of computer memories, microprocessors and in general digital ICs has driven a very fast technological evolution in the past 30 years, following Moore's law, leading to today's deep submicron technologies whose gate oxide, having a thickness of about 2nm, is practically immune from radiation. In 1965 Gordon E. Moore foresaw that the number of Integrated Circuit components would have doubled every year [2], i.e. the logarithm of the number of ICs components plotted versus the time would approximate a straight line. Amazingly enough¹, the prediction turned out to be true. This

¹This prediction was based on the trend of only six previous years, starting from the

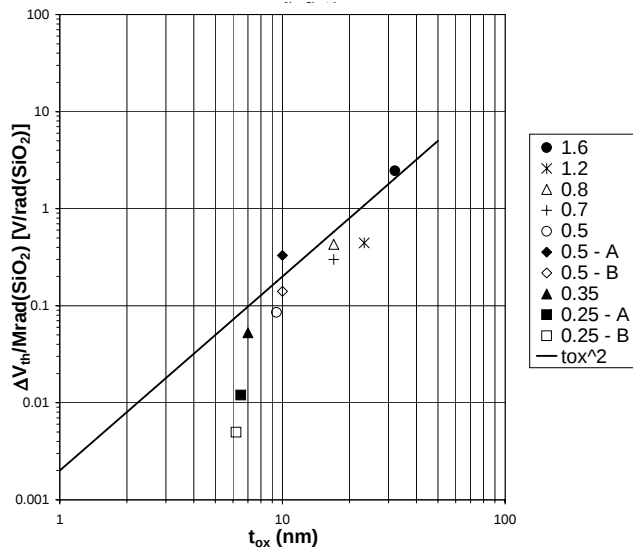


Figure 1: *Decrease of the radiation-induced threshold voltage shift of a MOS transistor as a function of the gate oxide thickness [1].*

prediction was of course for digital circuits. In 1975 Moore reviewed the “slope” of his prediction for the future saying that the number of transistors per chip would have doubled every 18 months [3] and in 1996 Moore himself wrote: “The definition of “Moore’s Law” has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I don’t want to do anything to restrict this definition.” [4]. An example of how Moore’s law has turned out to be true from the early seventies up to now is shown in figure 2.

The radiation tolerance of the gate oxide of commercial deep submicron CMOS technologies suggested the possibility of using them in a radiation environment without the need of introducing or modifying any process steps. Starting from these considerations, around mid-90s, groups in the HEP community started to investigate alternative ways to improve the radiation tolerance of ASICs based on the use of commercial CMOS technologies. Having a radiation tolerant gate oxide in fact does not solve all the possible problems when irradiating an integrated circuit made in a standard deep submicron technology. To solve these problems one can still adapt the layout and the architecture of the circuits and of the system, solutions which are called

production of the single planar transistor in 1959.

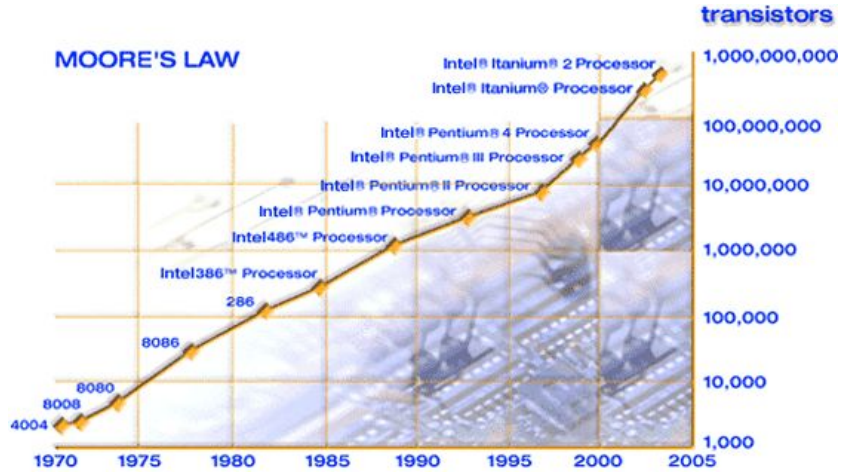


Figure 2: The picture shows a practical example of how Intel's microprocessors satisfies the Moore's law. In 30 years the number of transistors on a chip has increased from a few thousands on the 4004 in 1971 to nearly 1 billion on the Pentium Itanium 2 Processor in 2003 [5].

Hardening By Design techniques (HBD). Two layout solutions were developed, which allowed the design of the ASICs for the LHC using a commercial $0.25\mu\text{m}$ CMOS technology: Enclosed Layout Transistors (ELTs) to prevent radiation-induced leakage at the edge of the transistor, and p+ guard rings to cut leakage paths between adjacent n+ diffusions or n-wells at different potentials.

Nevertheless, although HBD techniques allow to design very reliable radiation tolerant integrated circuits, profiting of all the benefits of CMOS commercial technologies, they have some drawbacks, such as lower density, lower performance and larger power consumption. Additionally, those measures required the development of a dedicated digital library for the quarter micron process where all the cells were carefully designed in HBD, the cost of which was not trivial in term of manpower and time. In addition to that future LHC upgrades and the SLHC (Super LHC) will require higher-performance ICs, tolerant to larger TID levels and the use of a more modern technology node. The $0.25\mu\text{m}$ CMOS process is already an old process and will not stay around much longer.

Hence, there is a growing need in the HEP community to study the commercial, state-of-the-art CMOS technologies to understand the radiation effects and their relevance, anticipate the radiation performance of commercial

integrated circuits and evaluate whether HBD techniques are necessary in the extreme radiation environment of today's and future HEP experiments. Modern deep submicron CMOS processes, like the one considered in this work, have in fact the potential of higher TID tolerance and much better performances.

In this framework, this thesis presents a study of the TID (Total Ionizing Dose) response of three different commercial 130nm CMOS technologies.

Chapter 1

Radiation effects on MOS devices and hardening by layout techniques

The effects of radiation on electronic devices can be divided in two classes: cumulative effects and Single Events Effects (SEE).

Cumulative effects are gradual effects taking place during the whole time the device is exposed to radiation and they are due to the energy deposited by particles passing through the materials constituting the electronic devices. Typical cumulative effects are ionizing effects, called **Total Ionizing Dose (TID) effects**, generated by particles like photons and electrons, or **displacement damage**, generated by particles such as neutrons. A device sensitive to TID or displacement damage will exhibit failure in a radiation environment when the accumulated TID, or particle fluence, has reached its tolerance limits. It is therefore in principle possible to foresee when the failure will happen for a given, well known and characterized component.

On the contrary, **Single Events Effects** are due to the energy deposited by one single particle in the electronic device and they can happen in any moment. Hence, a device sensitive to SEE can exhibit failure at every moment since the beginning of its operation in a radiation environment.

MOSFETs (Metal-Oxide-Semiconductor Field Effect Transistors, figure 1.1) are more sensitive to ionization effects than to displacement damage. A major effect of displacement damage is in fact the reduction of the minority carriers lifetime in the silicon bulk, but MOS transistors are devices in which the conduction is based on the flow of majority carriers below the SiO₂-Si interface, a region which does not extend deeply in the bulk. In addition to that, the substrate is usually doped enough not to be affected by displacement

damages until fluences of the order of some 10^{15} particles/cm². For these reasons we will not consider these effects in the analysis of the effects of radiation on MOS devices carried out in this chapter.

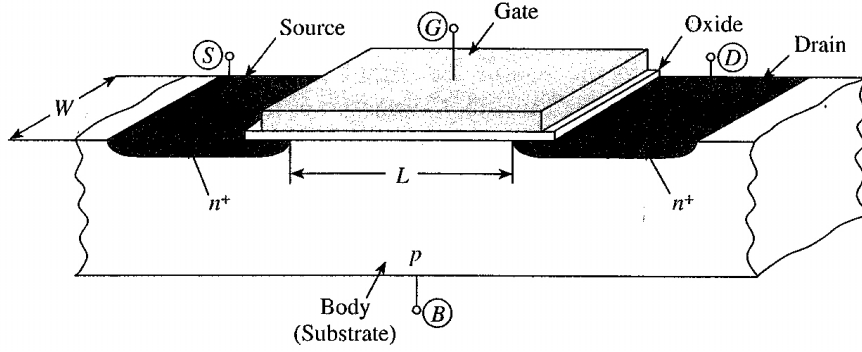


Figure 1.1: *Simplified structure of an n-channel MOS transistor. The conductive channel between source and drain is at the SiO₂-Si interface [6].*

1.1 Total Ionizing Dose effects

1.1.1 Defects in silicon dioxide and at the interface SiO₂-Si

In order to achieve a better understanding of TID effects on MOS transistors, it is worth giving a short foreword about the nature of defects usually present in the silicon dioxide and at the interface SiO₂-Si. These defects introduce localized energy states in the energy band gap of the material (SiO₂ or Si in this case) and act as traps for the carriers (electrons in the conduction band and holes in the valence band).

In the silicon dioxide, defects are due to a precursor, which is not active in its normal condition, but which is activated by radiation, becoming a trap center for positive charges. This precursor is already present in the oxide before irradiation and it represents the physical origin of the oxide traps.

At the interface SiO₂-Si, the defects are due to the abrupt transition between a crystalline material (Si) and an amorphous one (SiO₂) and to the consequent interruption of the crystalline structure of silicon. These defects, called interface states, are located at the interface or a few angstrom from it and they are responsible for the interface traps. Opposite to the oxide traps,

which are only donor like, the interface traps can be both donor or acceptor like. A donor trap releases an electron when it passes from below to above the Fermi level so it is neutral when full and positively charged when empty. An acceptor trap captures an electron when it passes from above to below the Fermi level so it is neutral when empty and negatively charged when full. The net charge of the interface traps can then be positive or negative according to their position with respect to the Fermi level.

1.1.2 Formation of oxide trapped charge and interface traps

When ionizing radiation goes through a MOSFET [Fig. 1.2 (1)], electron-hole pairs are generated. In the gate material (metal or polysilicon) and in the substrate the electron-hole pairs quickly disappear, since these are materials of little resistance. On the contrary in the oxide, which is an insulator, electrons and holes have different behaviors, as their mobilities differ from five to twelve orders of magnitude¹.

A few picoseconds after the generation, a fraction of the radiation-induced electron-hole pairs recombines, while the others are separated by the electric field applied to the device [Fig. 1.2 (2)]. The fraction of non-recombined pairs is a function of the kind of incident radiation, of the material and of the applied electric field. The electron and holes which do not recombine will start to move because of the electric field in opposite directions. If we suppose a positive bias applied to the gate, as in figure 1.2, then the electrons will drift to the gate and due to their high mobility, they will exit the oxide in few picoseconds, whereas the holes will move toward the SiO₂-Si interface with a dispersive transport phenomenon called small polaron hopping [Fig. 1.2 (3)]: the higher the temperature and the electric field, the faster the transport phenomenon. During their migration toward the interface, holes can be trapped because of the defects present in the silicon dioxide and consequently give origin to a fixed positive charge [Fig. 1.2 (4)]. The fraction of trapped holes depends on the mean trap density, their hole capture cross-section and the width of their distribution. The non-trapped holes which reach the SiO₂-Si interface (in the case of positive gate bias) will recombine with electrons coming from the silicon. Moreover these electrons may tunnel from the surface into the oxide and recombine with trapped holes, giving origin to tunnel-effect-based annealing. This effect depends both on

¹For electrons the typical mobility at room temperature in silicon dioxide is $20\text{cm}^2\text{V}^{-1}\text{s}^{-1}$. For holes the mobility depends strongly on the temperature and on the electric field and varies from 10^{-4} to $10^{-11}\text{cm}^2\text{V}^{-1}\text{s}^{-1}$.

the electric field in the oxide, becoming more effective as the electric field increases (in this way the potential barrier which has to be crossed by the electrons is lower) and on the spatial distribution of the traps in the oxide, which is in turn strongly dependent on the fabrication process. The tunnel annealing, which tends to reduce the amount of positive charge trapped in the oxide, is helped by other two phenomena. The first is the electrons generated within the trapped holes distribution. Depending on the local density of trapped holes and the cross-section of the capture of an electron by a trapped hole, an electron can recombine with a trapped hole. The second consists of electrons in the oxide valence band which, having a sufficient thermal energy to jump into the oxide, recombine with holes trapped in the oxide (thermal annealing). In this case, due to the strong dependence of the process on the temperature, it is the distribution in energy of the traps which matters: these have to be close enough to the valence band.

Thanks to tunnel and thermal annealing, the amount of positive charge trapped in the oxide undergoes a slow process of annealing which can take place, not just at the end of the irradiation, but already during irradiation, depending on the temperature, the electric field in the oxide, and the dose rate used for the irradiation. The importance of the other recombination process increases with the total dose and is one of the effects which contributes to the saturation of the threshold voltage shift component associated to the holes trapped in the oxide².

Another effect of the ionizing radiation on MOS devices is the increase by several orders of magnitude of the trap density at the interface SiO₂-Si [Fig. 1.2 (5)]. This phenomenon has been studied for many years and is not fully understood yet. The two major models to describe it are the WML (Winokur-McLean, [7] and [8]) and the (HH)² (Hole-Trapping/Hydrogen-Transport, [9] and [10]). According to these models, the creation of radiation induced traps is a secondary phenomena, subsequent to the generation of electron-hole pairs. In the first stage of the process, hydrogen ions are created by the holes while they are moving toward one of the two oxide surfaces (WML) or when they are trapped ((HH)²). In the second stage, these ions move toward the SiO₂-Si interface (in the case of positive gate bias), where they give origin to new interface states which serve as traps. These radiation-induced traps have energy between the valence and conduction band of the silicon. Experiments indicate that the major part of the traps present above midgap are acceptors while traps below are donors.

²The saturation of the threshold voltage shift component due to the holes trapped in the oxide was observed experimentally. ΔV_{ox} does not increase linearly with the dose and its value tends to saturate at high TID.

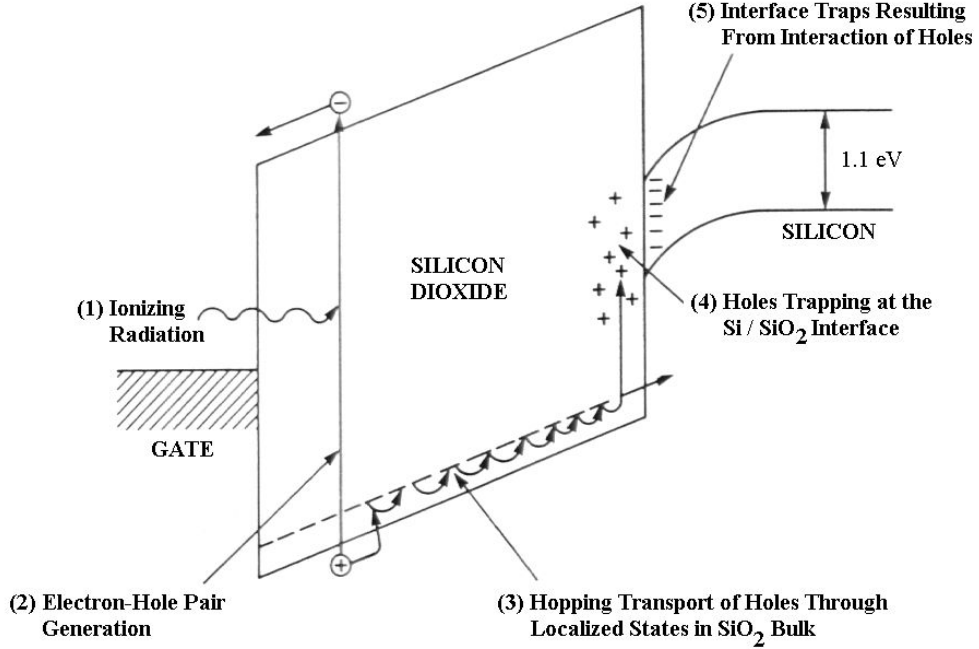


Figure 1.2: Schematic illustration of the effects induced by ionizing radiation in a MOS device, when the gate is positively bias [6].

These models explain why the formation of interface states is slower than the holes trapping in the oxide, since the ions have a lower mobility with respect to the holes, and why the amount of generated traps is lower if the gate is negatively biased. In this case only hydrogen ions generated very close to the SiO₂-Si interface will give origin to traps.

Opposite to the case of oxide trapped charge, there is generally no significant annealing of the interface traps at room temperature.

1.1.3 Consequences of the radiation on the electrical parameters of a MOS transistor

In this section we present the consequences of hole trapping in the oxide and of interface traps generation at the SiO₂-Si interface on the electrical parameters of a MOS transistor, namely the threshold voltage, the leakage current, the carrier mobility μ and the transconductance g_m .

Threshold voltage shift

The threshold voltage of a MOS transistor changes when the device is irradiated. The threshold voltage shift ΔV_{th} ³ is given by the sum of two contributions, ΔV_{ox} and ΔV_{it} , which are related to the hole trapping in the silicon dioxide and to the charge state of the interface traps respectively.

The oxide trapped charge gives origin to a threshold voltage shift proportional to the density of trapped holes and to the position of the charge distribution in the oxide with respect to the SiO₂-Si interface: the closer the charge to the SiO₂-Si interface, the bigger the threshold voltage shift. Since the charge trapped in the oxide is always positive, the threshold voltage shift due to this contribution is always negative. Hence, the threshold voltage of an NMOS transistor decreases, whilst the one of a PMOS increases (in absolute value). Since, as just mentioned, the effect of the oxide charge on the voltage shift is weighted by its position in the oxide, its contribution is less important for PMOS transistors than for NMOS. In the case of PMOS transistors in fact, due to the negative gate bias, holes move towards the SiO₂-gate interface.

The threshold voltage shift component associated with the radiation induced interface states is proportional to the charge (per unit area) which fills the interface states after and before irradiation and it can have positive or negative values. As mentioned in section 1.1.2, we assume that the traps above midgap are acceptor like and those below are donor like. This means that for a n-channel transistor, where the Fermi level in the silicon close to the silicon-dioxide interface lies between E_i and E_c (Fig. 1.3), the acceptor-like traps which are below the Fermi level will be negatively charged and the threshold voltage shift will be positive. Similarly for a p-channel the threshold voltage shift will be negative (i.e. the threshold voltage increases, in absolute value, both for a NMOS and for a PMOS transistor).

As well as for the oxide trapped charge case, the bias condition of the gate is of relevant importance for the role played by interface states in the threshold voltage shift. As explained by the WML and (HH)² models, there is a correlation between the transport and/or trapping of holes in the oxide and the increase of interface states. In NMOS transistors, because of the positive bias applied on the gate, holes move toward the SiO₂-Si interface where they can contribute to the creation of interface traps. Hence, the polarization of an NMOS device to make it conductive, is a worse case bias under irradiation. On the contrary, in PMOS transistors, the negative voltage applied to the

³The threshold voltage shift, ΔV_{th} , is the difference between the threshold voltage value after irradiation and before irradiation.

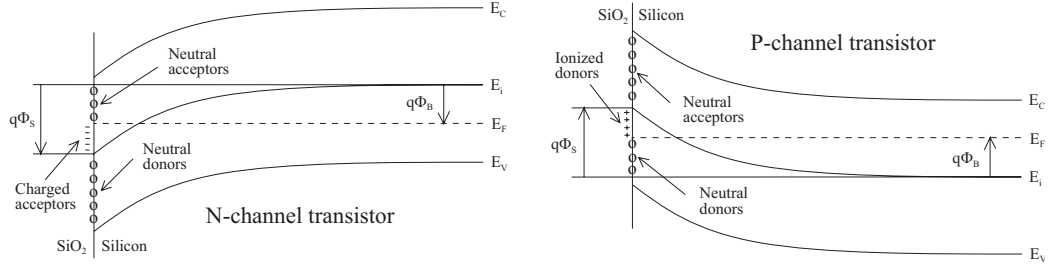


Figure 1.3: *Energy band diagrams at the interface $\text{SiO}_2\text{-Si}$ for an n-channel and a p-channel transistors. The diagrams show the behaviour of the interface traps in two typical cases (gate bias, referred to the substrate, positive for the n-channel transistor and negative for the p-channel) [6].*

gate to make the transistors conductive has the effect to reduce the creation of interface states, because the holes move toward the $\text{SiO}_2\text{-gate}$ interface.

Since the contribution of the radiation induced interface states to the threshold voltage shift has different signs for NMOS and PMOS transistors, the radiation effect on the threshold voltage shift ($\Delta V_{th} = \Delta V_{ox} + \Delta V_{it}$) is different for n-channel and p-channel MOSFETs. For the p-channel transistors, both the contributions, ΔV_{ox} and ΔV_{it} , are positive, so the threshold voltage increases in absolute value during irradiation. For the n-channel transistors, the two contributions have different signs and the threshold voltage shift presents a rebound. This is a well-known effect due to the fact that, as explained earlier, the interface states increase is a slower phenomenon than the build up of positive charge in the oxide. As a consequence, ΔV_{it} starts to play a role later than ΔV_{ox} and, at high TID, due to the saturation of the oxide trapped charge, only the interface traps contribute to the threshold voltage shift. Moreover interface states can still influence the threshold voltage shift after the end of the irradiation and some annealing (i.e. the threshold voltage will increase (in absolute value) for both PMOS and NMOS transistors during annealing), due to their slow creation dynamics.

A method proposed by McWorther and Winokur [11] allows to separate the measured threshold voltage shift for the two contributions to understand the behaviour of both the trapped oxide charge and the interface traps. It is based on the variation of the subthreshold slope before and after irradiation. The drain current of a MOSFET below threshold (i.e. for values of the surface potential Φ_S comprised between Φ_B and $2\Phi_B$, where Φ_B is the Fermi potential in the semiconductor bulk, figure 1.3) varies exponentially with

V_{gs} . The plot of the drain current (log scale) as a function of the gate-source voltage is therefore a straight line. The slope of this line is called subthreshold slope and its inverse, called subthreshold swing, can be expressed as:

$$S = \frac{KT}{q} \cdot \ln 10 \cdot \left(1 + \frac{C_d + C_{it}}{C_{ox}} \right) \quad (1.1)$$

where C_d and C_{ox} are the capacitances per unit area respectively of the depletion region in the silicon and in the gate oxide. C_{it} is the capacitance associated with the charges trapped in the interface states, and is the term which varies with irradiation, since $\Delta C_{it} = q \Delta D_{it}$ and ΔD_{it} is the variation of the interface state density, expressed in $V^{-1}cm^{-2}$. $(KT/q) \cdot \ln 10$ at room temperature has the value 60mV/decade, which is the minimum theoretical value for the subthreshold swing. The subthreshold swing variation as a function of the radiation induced variation in the interface state density can be expressed as

$$\Delta S = \frac{KT}{q} \cdot \ln 10 \cdot \frac{q \Delta D_{it}}{C_{ox}}. \quad (1.2)$$

The quantity ΔS (which is positive for both n-channel and p-channel transistors, since the effects of radiation is always to increase the interface state density) is easy to measure leading to an estimation of ΔD_{it} .

To extract $\Delta V_{it} = -\Delta Q_{it}/C_{ox}$ from ΔD_{it} , we have to integrate ΔD_{it} over the energy gap to obtain ΔQ_{it} and then ΔV_{it} . The integral leading to ΔQ_{it} ⁴

$$\Delta Q_{it} = q \cdot \int_{gap} \Delta D_{it} d\Phi_s \quad (1.3)$$

can be easily solved considering that the interface state density is constant close to the band gap centre both before and after irradiation (i.e. the difference before and after irradiation is constant) and assuming that the interface states are acceptor-like above midgap and donor-like below it. With these assumption ΔD_{it} is constant and can be taken out of the integral. The extremes of integration are Φ_B and $2\Phi_B$, since for $\Phi_S = \Phi_B$ the Fermi level starts to charge negatively the first acceptors for n-channel transistors (or positively the first donors for p-channel transistors) and for $\Phi_S = 2\Phi_B$ the threshold condition is reached; beyond this the surface potential is fixed at $2\Phi_B$. The result of (1.3) is then

$$\Delta Q_{it} = q \Delta D_{it} \cdot \Phi_s. \quad (1.4)$$

⁴The integral (1.3) has to be taken with its sign for p-channel transistors and with the opposite signs for n-channel.

Since $\Delta V_{it} = -\Delta Q_{it}/C_{ox}$, using (1.4) and (1.2) we can write

$$|\Delta V_{it}| = \frac{\Phi_B}{\frac{KT}{q} \cdot \ln 10} \cdot \Delta S. \quad (1.5)$$

Knowing ΔS and ΔV_{th} is then possible to calculate the threshold voltage shift given by the interface trapped charges ΔV_{it} , and also ΔV_{ox} . This is very useful to get information on the quality of the oxide and of the oxide-silicon interface and also if we want to study the annealing of the holes trapped in the oxide and of the interface states.

Leakage current

The “off-state” current in a MOS transistor is defined as the current which flows from drain to source when $V_{gs}=0V$ and $V_{ds}=V_{dd}$, and it is referred as leakage current. Only NMOS transistors undergo an increase in the off-state current after irradiation. Two effects lead to this increase: the increase of the subthreshold current and the generation of parasitic currents.

The increase in the subthreshold current is related to two factors, illustrated in figure 1.4. The first is the decrease of the threshold voltage, due to early trapping of positive charge in the oxide. The pre-irradiation solid line in figure 1.4 shifts towards the y axis (V_{th} goes from V_{th1} to V_{th2}) and becomes the dotted line after some irradiation. The second is the radiation-induced decrease of the subthreshold slope due to the built up of interface states at higher TID (Figure 1.4, curve after irradiation 1). In this case the subthreshold current which before irradiation was I_{leak1} becomes therefore I_{leak2} due to the threshold voltage shift and then I_{leak3} due to the subthreshold slope decrease. As mentioned earlier anyway, the threshold voltage shift of a NMOS transistor is negative because of the early trapping of holes in the oxide, but it can become positive because of the interface states built-up. If this happens, it can help in compensating for the decrease of the subthreshold slope, i.e. the subthreshold current might not increase after irradiation (Figure 1.4, curve after irradiation 2). This can be checked only with measurements on the technology of interest.

The other contribution to the post-irradiation “off-state” current in a standard n-channel transistor is given by the generation of parasitic currents. It has been shown that this contribution to the total leakage current dominates over the one due to the subthreshold current.

Although the gate oxide becomes thinner and hence less sensitive to TID, the field oxide of modern CMOS technologies, used for the isolation between devices, does not scale down correspondently. It is a lot thicker than the gate

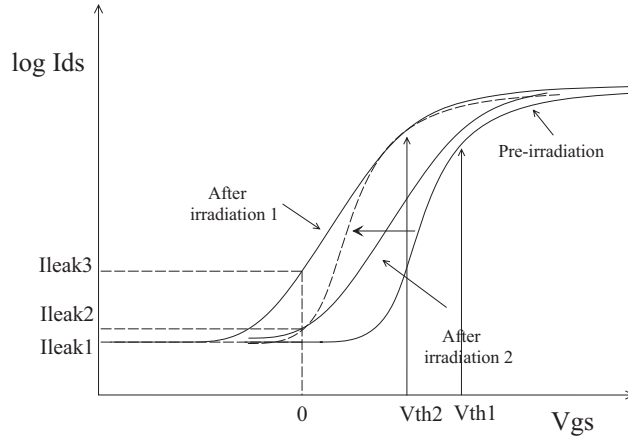


Figure 1.4: *Increase of the subthreshold current in a n-channel transistor given by a decrease in the threshold voltage and in the subthreshold slope.*

oxide, usually several 100nm. In addition to that, opposite to the thermally grown gate oxide, it is grown with a variety of different techniques and their trapping characteristics are not controlled. It is therefore still very sensitive to TID.

The field oxide, used for the isolation between devices, is responsible for the creation of two parasitic current paths between drain and source (Fig. 1.5). These leakage paths are due to the positive charge trapped in the transition region between the gate oxide and the thick oxide. In CMOS technologies down to the 0.35 μm node employing local oxidation of silicon (LOCOS) to isolate devices, this region had the typical shape of a “bird’s beak”, as shown in figure 1.5. In modern CMOS technologies, like those considered in this thesis, this isolation has been replaced by the Shallow-Trench-Isolation⁵ (STI). Although this new kind of isolation replaces the “bird’s beak” region with a more steep transition region between the gate oxide and the thick oxide, it does not eliminate post-irradiation leakage paths between source and drain.

One can imagine two parasitic transistors in parallel with the principal one, with a thicker gate oxide (i.e. the field oxide) but with the same gate of the main one, as shown in figure 1.5. Each of them can in turn be seen as a parallel combination of several transistors with width ΔW and roughly the same L of the main transistor, but with increasing gate oxide thickness, when going towards the field oxide. Due to their thick gate oxide, the parasitic

⁵Later on in the text we will refer to the field oxide also as the STI oxide.

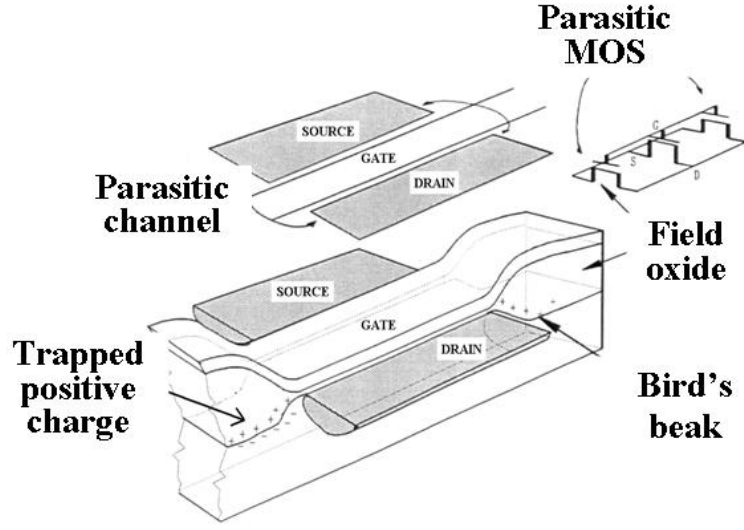


Figure 1.5: Schematic illustration of the parasitic transistors which are in parallel to the main transistor and of the parasitic leakage paths in the bird's beak region or underneath the field oxide which connects source and drain [6].

transistors have both a very high threshold voltage and a low current so that they can't be seen in the normal working condition of the NMOS transistor before irradiation. This situation is represented in figure 1.6, where the characteristics of the parasitic transistors in parallel are shown. However, due to the large amount of holes trapped by the lateral oxides during irradiation, the threshold voltage of the parasitic transistors decreases giving origin to a leakage current, as shown in figure 1.7. Since this leakage current is anyway smaller than the current flowing in the main transistor, it influences only the subthreshold region of the curve of the transistor but not the region above threshold. It is still worth mentioning that the threshold voltage of the parasitic transistors can be of the order of several volts, but since their gate oxide is rather thick the threshold voltage shift can be of the same order of magnitude. Moreover the parasitic transistors with the higher threshold voltage will have the higher shift, having the thicker gate oxides (Fig. 1.7). The shape after irradiation of the I_{ds} vs V_{gs} characteristic strongly depends on the total dose absorbed and on the quality and type of the oxide. Two examples are shown in figure 1.7.

The operational consequence of the radiation-induced leakage current is that the NMOS transistor would have trouble working as a switch (it could

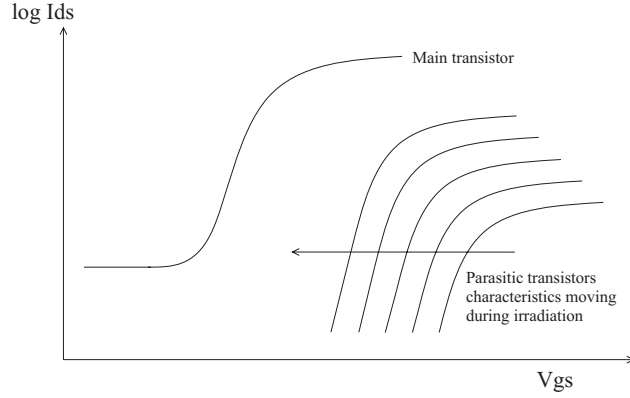


Figure 1.6: Curves representing the drain current of the main transistor and of the parasitic transistors before irradiation. The curves of the parasitic transistors move during irradiation [6].

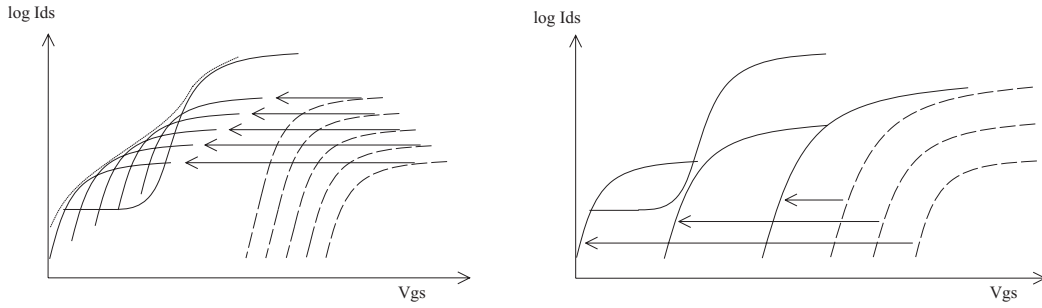


Figure 1.7: Two possible examples of the effects on the main transistor of the shift of the parasitic transistor characteristics caused by the irradiation. Note that the parasitic transistor with the higher threshold voltage shift (i.e. thicker gate oxide) is the one which moves further [6].

never be turned completely off) or, in an analog circuit, in weak inversion.

Positive charge trapping in the field oxide can also give origin to radiation induced leakage between different devices. An example is shown in figure 1.8, where the well of a p-channel transistor, connected to the power supply, is leaking toward the grounded source of a n-channel transistor (n+ diffusion). The same can happen between two adjacent n-wells or n+ diffusions at different potentials. If a biased interconnection line (made of polysilicon in the case of the figure) passes over the thick oxide, it creates an electric field during irradiation, worsening the TID effects.

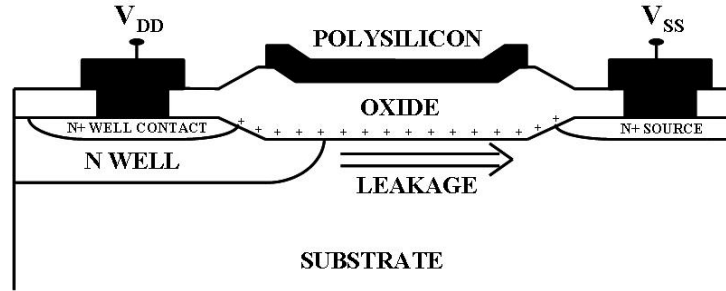


Figure 1.8: *Example of a radiation induced parasitic path in a n-well CMOS technology with LOCOS isolation [6].*

Decrease of mobility and transconductance

The mobility degradation after irradiation is essentially related to the increase of the interface traps, since the conduction in the MOS transistor is due to the carrier motion close to the silicon-oxide interface. Interface states trap charges from the channel leading to a decrease of the mobility. For the same reasons mentioned in the case of the threshold voltage shift, the degradation of the mobility is much stronger for NMOS (positive gate bias) than for PMOS (negative gate bias). The degradation of the mobility in turn gives origin to a degradation of the transconductance after irradiation, which decreases the driving capabilities of the device.

1.2 Single Event Effects

Single Events Effects⁶ are instantaneous effects generated when highly energetic particles, such as protons and heavy ions, go through a MOS device or an Integrated Circuit (IC). Opposite to the TID damages which are related to the deposited TID and lead to a progressive degradation of the device, SEE are generated in a non recurrent manner in time and space as a function of the particles fluence (particles/cm³) and can cause an immediate malfunctioning of one or more transistors which can then influence the entire circuit. The generated errors can be both reversible (i.e. non destructive), causing a temporary failure of the device, or non reversible (i.e. destructive), leading to a permanent failure of the device. The first are called soft errors, the latter are called hard errors.

⁶The following description of the SEE is brief, since they are not part of the work presented in this thesis.

The circuit sensitivity to SEE is characterized by its cross-section as a function of the Linear Energy Transfer (LET), which expresses the linear transfer of energy to the material by the incident particles. The LET depends on the nature and on the energy of the incident particles and on the absorbing material. It is defined as the mean energy transferred to the material per unit path length (dE/dx), normalized to the material density (ρ):

$$\text{LET} = \frac{1}{\rho} \frac{dE}{dx}. \quad (1.6)$$

The cross-section is the number of events (SEE) per unit fluence. A typical curve of the cross-section as a function of the LET of the incident particles for an integrated circuit is shown in figure 1.9. The LET threshold, LET_{th} , is the minimum LET which can cause a SEE in the most sensitive circuit node. Only particles with a LET higher than the threshold can generate SEE.

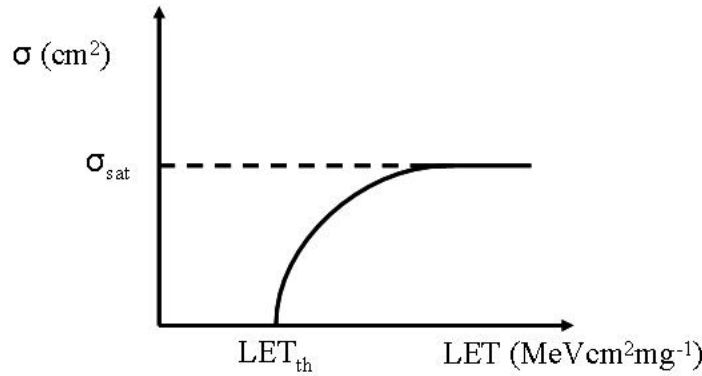


Figure 1.9: *SEEs cross-section as a function of the LET of the incident particle.*

The most important SEE for deep submicron CMOS technologies are the Single Event Upset (SEU) and Single Event Latch-up (SEL). Before treating them, a short discussion of the effects of heavy-ions and protons when crossing a semiconductor device is presented. For completeness some other SEE will be mentioned at the end of the paragraph.

1.2.1 Heavy-ions and protons effects

The incoming heavy ion loses energy in the semiconductor through Rutherford scattering (i.e. Coulomb interaction) with the lattice structure. The energy is transferred to the lattice as a tail of free electron-hole pairs. In the

bulk of the semiconductor, these will recombine with no effect. In a p-n junction or in its proximity, the pairs will be separated and collected, giving rise to a spike current (Fig. 1.10). The charge collection will have a fast (of the order of hundreds of ps or less) and a slow component (of the order of ns). The mechanism of charge collection are multiple and the collection region might extend also relatively far from the junction through a phenomenon called "funneling", as shown in figure 1.11.

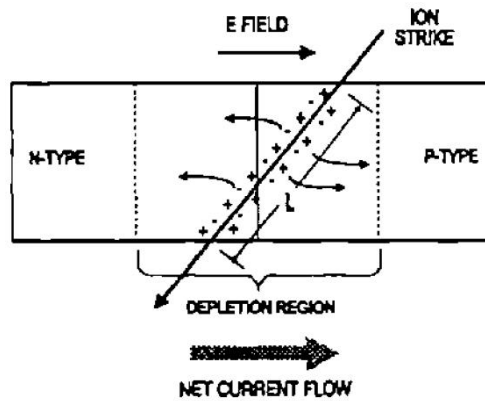


Figure 1.10: Along the ion track, electron-hole pairs are created. In presence of an electric field (depleted junction) the charge will flow and a current spike might be observed [12].

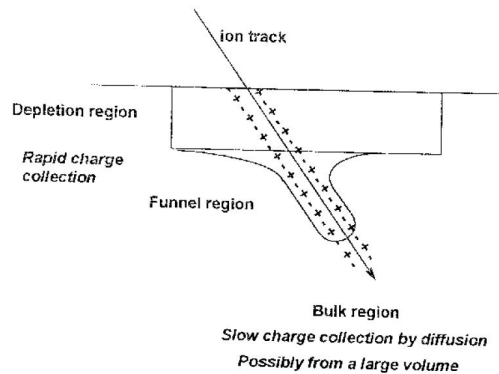


Figure 1.11: Charge collection has a prompt and a slow component and might extend far from the depleted junction (funneling) [12].

High energy protons can't cause SEE in the same way as heavy ions do.

Due to their low LET, less than $1 \text{ MeVcm}^2\text{mg}^{-1}$, protons direct contribution to SEE is negligible in most devices, since there are just few of them with a LET threshold lower than $1 \text{ MeVcm}^2\text{mg}^{-1}$. They can cause SEE by generation of secondary ions from the interaction between protons and atoms of the material constituting the device. These ions have a higher LET (up to $15\text{MeVcm}^2\text{mg}^{-1}$ in the case of silicon) and can in turn cause SEE.

1.2.2 Single Event Upset (SEU)

A SEU is the instantaneous reversible modification of the logic state of an elementary memory cell. It is induced by the charges generated along the track of the incoming particle which are collected in the circuit sensitive node.

An example is the case of the SRAM cell showed in figure 1.12. It is made of two inverters, the output of each inverter being connected to the input of the other one. The sensitive nodes in a SRAM are the transistor drains. The charge collection at the drain of the NMOS transistor will temporarily change the state of node 2. Before the deposited charge might be evacuated to the power supply through the open transistor of this inverter, the second inverter (whose input is node 2) switches. This changes the state of node 1, which in turn enforces the wrong state at node 2. In this way, the error is latched into the memory cell.

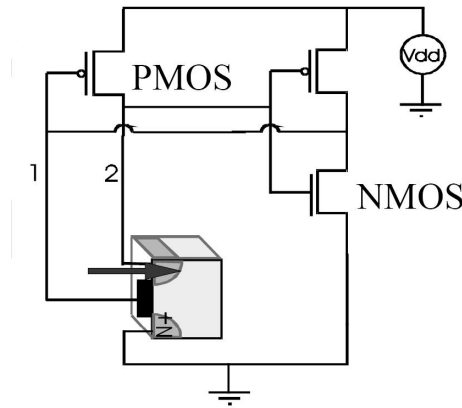


Figure 1.12: *Schematic illustration of a SRAM [12].*

In complex memories, the memory cells and the peripheral circuits are connected to others circuits with additional features, as for example Error Detection and Correction (EDAC). If an energetic particle strikes one of these circuits, the error will influence the functioning of the whole circuit. This

error, which can be thought of as a particular case of SEU, is called Single Event Functional Interrupt (SEFI).

1.2.3 Single Event Latch-up (SEL)

Latch-up is a phenomenon which can occur in CMOS ICs and which consists of the turning on of a parasitic PNP structure (called thyristor, figure 1.13) which can short the power lines, allowing for a sudden current which can destroy the device if not interrupted promptly. Manufacturers are aware of possible electrical latch-up initiated by electrical transients on input/output lines, high temperature or improper power supply sequencing and hence circuits are often protected against these failure modes. Nevertheless, circuits operating in a radiation environment might be subject to a ionizing particle-induced latch-up, called Single Event Latch-up.

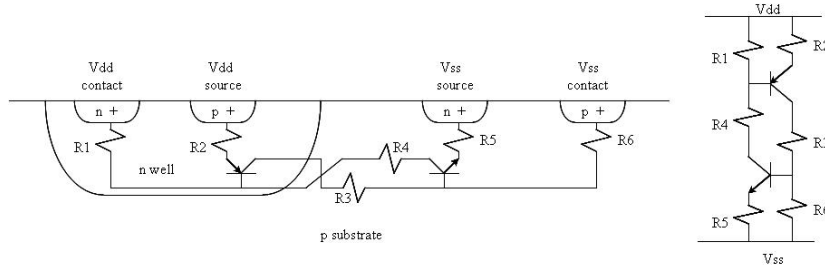


Figure 1.13: *Schematic illustration of the parasitic thyristor in a n-well CMOS process [6].*

The parasitic thyristor, as shown in figure 1.13, is made by two parasitic bipolar transistors, interconnected such that the collector current of each BJT feeds the base current of the other. In such structure, an increase in the pnp collector current gives origin to an increase in the npn base current. This in turn increase the npn collector current which gives an increase in the pnp base current. This positive feedback is such that, if the overall gain of the thyristor is higher than 1, any perturbation, for instance an ionizing particle strike, turning on one of the parasitic BJT structures can trigger latchup.

After the latchup is initiated it can be interrupted by cutting the power supply to the circuit. In that case, the circuit can be saved from destruction and can be returned in the operational condition.

1.2.4 Other SEEs

To be complete, we will now mention briefly some others SEE: Single Event Gate Rupture (SEGR) and Single Event Burn Out (SEBO).

The SEGR is a destructive effect which consists of the destruction of the gate oxide by a ionizing particle. It can happen when an high electric field is applied to the gate, as during the writing or erasing phase of a EEPROM (Electrically Erasable Programmable Read-Only Memory) or in power MOSFET devices. SEGR can be an issue in deep submicron CMOS technologies, since scaling down the technology increases the electric field in the oxide.

SEBO is present in n-channel power MOSFETs and bipolar transistors. These devices contain a parasitic bipolar transistor. In some bias conditions it is possible that a ionizing particle turns on the bipolar transistor and if this is able to conduct enough current, the locally dissipated power can be high enough to melt the device.

1.3 Hardening by layout techniques

There are three possible levels on which the radiation tolerance of CMOS integrated circuits can be improved. The first consists in acting on the process, modifying some technological parameters or process steps to reduce the sensitivity to radiation-induced problems (Hardening by process technique). The second employs special layout techniques, to solve the problem of radiation-induced leakage currents and SEL and to reduce the vulnerability to SEU (Hardening by layout). The third regards the study of special circuit and system architectures which are less sensitive than others to the changes in the device characteristics due to TID or SEE (Hardening by circuit and system architecture). These last two techniques goes under the general name of Hardness By Design (HBD) techniques.

We will focus our discussion on the hardening by layout techniques because they have been used in the design of some of the test structures used in this work.

These techniques relies on the use of Enclosed Layout Transistors (ELT, also called edgeless transistors) and p+ guard rings.

ELTs are used to avoid the post-irradiation leakage current in n-channel MOSFETs (i.e. at device level). In this case the parasitic paths between source and drain are eliminated designing the transistor with an enclosed geometry as shown in figure 1.14 D. This layout has been proved to be very effective and the safest from a radiation hardness standpoint hence its use is mandatory if high total dose radiation tolerance has to be achieved with deep

submicron technologies. Other solutions can be possible, like those shown in figure 1.14, but they are less effective. Solution B consists in increasing the length of the parasitic devices and though it is the least intrusive solution, it is also the least effective. The design solution C defines the limit of the thin oxide with a p+ diffusion. The transistor is then built inside the thin oxide region. This solution allows to keep the transistor geometry close to the one of standard transistors, but it violates some design rules of commercial processes.

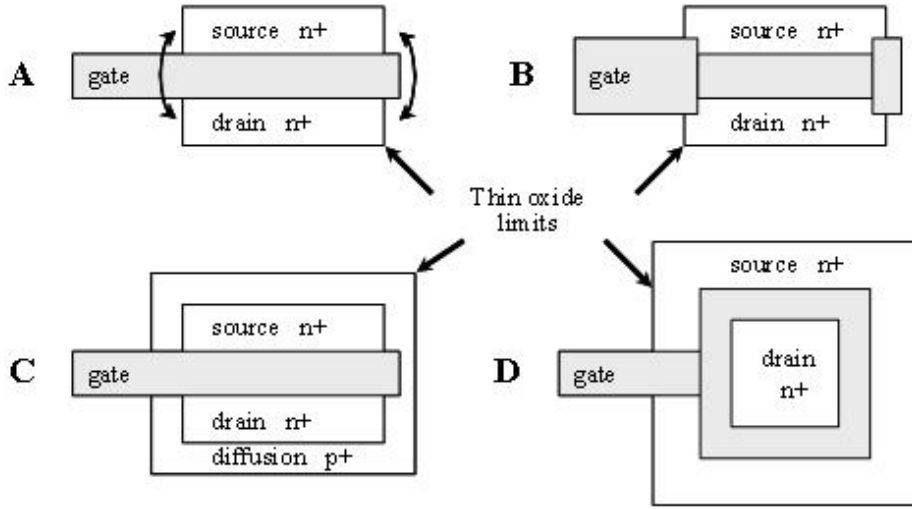


Figure 1.14: Layouts of a standard self-aligned n-channel transistor (A) and of three possible layout approaches to avoid leakage paths between source and drain in standard transistors [6].

Unfortunately the use of ELT has some drawbacks. One is the difficulty in modeling the W/L ratio. There are many different shapes which can be chosen for the design of ELTs, such as square, octagonal, square with corners cut at 45° , and each one needs to be modeled separately. We will focus on the last shape (Fig. 1.15), which is compatible with the design rules of many deep submicron technologies and it is the one used for the design of the Enclosed Layout Transistors used in this work. Studies on the electric field under the gate of the device supported by simulations and measurements have been done in the quarter micron process to enable the computation of the effective W/L of ELTs leading to the following formula [13]

$$\left(\frac{W}{L}\right)_{eff} = 4 \cdot \overbrace{\frac{2\alpha}{\ln \frac{d'}{d'-2\alpha L}}}^{T1} + 2K \cdot \overbrace{\frac{1-\alpha}{\frac{1}{2}\sqrt{\alpha^2 + 2\alpha + 5} \cdot \ln \frac{1}{\alpha}}}^{T2} + 3 \cdot \overbrace{\frac{\frac{d-d'}{2}}{L_{eff}}}^{T3}. \quad (1.7)$$

It has been derived by decomposition of the transistor in three parts, called T1, T2 and T3 shown in figure 1.15. The transistor T1 corresponds to the linear edges of the transistor, the transistor T2 to the transistor corners without the transistor T3 which consists of the 45° angle transistor. c , d , $d' = d - c\sqrt{2}$ and α are shown in figure 1.15. L_{eff} is used in the formula to take into account for the gate length shortening due to underdiffusions, photolithography and etching. α is a fitting parameter needed to identify the borderline between transistors T1 and T2. Its value is not known a priori but it is extrapolated fitting the experimental data. After testing on different CMOS technologies, scaling from 2.5 to $0.25\mu\text{m}$, α has been found to be almost technological independent, with a value of 0.05. The parameter K which multiplies the second term in (1.7) is a technological parameter, used to take into account the number of transistors T2 present in the ELT. Due to the fact that the polysilicon strip, used to integrate the gate contact outside the thin gate oxide region, has a constant width (A in figure 1.15) independent from the transistor gate length, K is geometry dependent: for short channel transistors ($L \leq 0.5\mu\text{m}$) its value is $7/2$, since the polysilicon strip “hides” one of the transistors T2, for longer channel devices its value is 4. Due to the presence of the polysilicon moreover, the third term in the formula (1.7) is multiplied by 3.

In addition to the W/L modeling difficulties, the shape of the enclosed layout transistors does not allow aspect ratio (W/L) lower than a certain value. To increase the aspect ratio it is enough to stretch the device in one or two dimensions, without modifying the corners and the calculation of the obtained W/L is straightforward, but to have lower aspect ratio the only way is to increase L , while keeping the minimum size for the distance d . The problem of these devices is that increasing the L , automatically increases the W , as it can be seen by the formula 1.7. It has been shown that in the case of the geometry in figure 1.15, the minimum W/L achievable is 2.26 and it is almost reached with $L = 7\mu\text{m}$ [6].

This leads to another drawback, the maximum density achievable using ELTs is always smaller than the one achievable using the standard layout. This is due also to the fact that the use of ELTs leads to a considerable waste of area compared to the standard transistors: for the same aspect ratio, the area occupied by an enclosed layout transistor is bigger than the

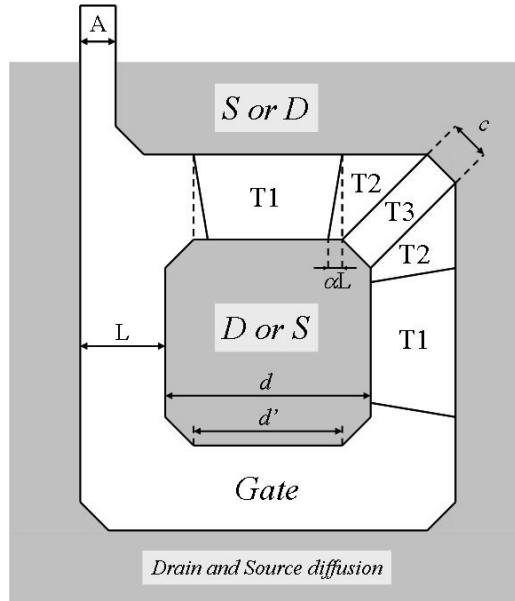


Figure 1.15: Square shaped ELT with corners cut at 45° . The transistor can be thought as being formed by transistors of three different kinds in parallel, labeled in the picture T1, T2 and T3 [6].

area occupied by a standard layout one, and this difference increases for small W/L . As just explained in fact, in order to reach small W/L for ELTs, L should be increased.

Nevertheless this drawback can be useful to reduce the sensitivity to SEU. This can be in fact simply achieved by either increasing the W/L ratio of the transistors in order to increase the capacitance and the driving power, or adding additional capacitances to the most sensitive nodes. Since the need for ELTs does not allow to have minimum size devices, the parasitic capacitances (and therefore critical charges) and the device drive capability are automatically increased.

P+ guard rings have to be used to isolate n-type diffusions at different potentials to cut any radiation-induced parasitic path at circuit level as the one showed in figure 1.8. In order to do so, p+ guard rings are built around each n-channel device. This method has been verified to be very effective but again, as for ELTs, this solution is area consuming.

The systematic use of guard rings, not only p+ but also n+, is used to render the circuits practically immune to SEL. P+ guard rings around n-channel transistors in fact decrease the gain of the NPN parasitic bipo-

lar transistor (see figure 1.13), introducing a strongly doped p region in the base and keeping the base firmly close to ground. The behavior of the n+ guard rings with the PNP parasitic bipolar transistor is similar. Other layout stratagems to solve SEL problems consist in increasing of the distance between the p+ diffusion in the well and the n+ diffusion in the substrate and the number of substrate and well contacts: putting them as close as possible to the latch-up loop minimizes the resistances R1 and R6.

To conclude this paragraph, we would like to do a final remark. The use of ELTs and guard rings decreases the density which could be obtained with the standard layout using the same CMOS technology node. On the other hand, the alternative would be to use a radiation hardened technology. For economical reasons, these technologies are generally less advanced than the available commercial CMOS technologies, usually a couple of generations behind, and it has been shown that using an available commercial CMOS technology with the layout approach discussed in this paragraph (i.e. ELTs and guard rings) allows to obtain higher densities than those obtainable with the available radiation hardened technologies. Speed and power consumption are also better.

Chapter 2

Experimental details

2.1 Test structures

Measurements were performed on samples provided by three different manufacturers of commercial 130nm CMOS technologies, called in the text A, B and C.

The test structures from foundries A and B are Process Monitoring Devices (PMD) designed as columns of 12 pads each to give access to all the terminals of NMOS and PMOS transistors of different type. We tested two types of transistors in these test structures: **core transistors**, with gate oxide thickness of $\approx 2\text{nm}$, and **input/output (I/O) transistors** with a thicker gate oxide (about 5nm). These latter are available to allow the integration of ASICs in the 130nm technology within systems requiring 2.5V logic levels. They are also recommended for on-chip analog circuitry, wherever the 1.5V supply voltage of the core transistors does not provide enough room for stacked transistors, as frequently used in analog circuit architectures.

For foundry A we chose the following transistor sizes:

- A W array with $L=0.12\mu\text{m}$ (W from minimum size , $0.16\mu\text{m}$, to $10\mu\text{m}$), two transistors with $W=10\mu\text{m}$ ($L=10$ and $0.11\mu\text{m}$) and a transistor with aspect ratio $0.16/10$ for measurements on core transistors;
- An L array with $W=10\mu\text{m}$ (L from minimum size , $0.3\mu\text{m}$, to $0.68\mu\text{m}$) for measurements on I/O transistors.

For foundry B, the chosen transistor sizes were:

- A W array with $L=0.13\mu\text{m}$ (W from minimum size , $0.14\mu\text{m}$, to $10\mu\text{m}$) for measurements on core transistors;

- A W array with $L=0.34\mu\text{m}$ (W from minimum size, $0.40\mu\text{m}$, to $0.8\mu\text{m}$) for measurements on I/O transistors.

The test structure from foundry C was custom-developed. It has been designed on purpose to study the degradation induced by radiation and therefore it integrates some particular structures:

- Core and I/O MOSFETs, not just linear, as the ones in structures from foundries A and B, but also enclosed. The latter have been integrated not just to assess the radiation tolerance of this particular transistor geometry, but also to understand whether the formula (1.7) for the computation of the effective W/L of ELTs, validated for the $0.25\mu\text{m}$ CMOS process, is still applicable to the 130nm process and to estimate the error in doing so.

The available sizes of core linear transistors were a W array with $L=0.12\mu\text{m}$ (W from minimum size, $0.16\mu\text{m}$, to $2\mu\text{m}$) and a L array with $W=10\mu\text{m}$ (L from minimum size, $0.24\mu\text{m}$, to $10\mu\text{m}$), whilst a L array with minimum W (L from minimum size, $0.12\mu\text{m}$, to $2\mu\text{m}$) was available for core enclosed transistors. The sizes for I/O linear transistors were a W array with $L=0.24\mu\text{m}$ (W from minimum size, $0.36\mu\text{m}$, to $2\mu\text{m}$) and two transistors with $W=10\mu\text{m}$ ($L=1$ and $10\mu\text{m}$). One enclosed layout I/O transistor with minimum W and $L=0.26\mu\text{m}$ was available as well;

- A few core transistors with “ringed” layout (a L array with $W=3\mu\text{m}$) as shown in figure 2.1. This transistor geometry as well as the enclosed design is used to cut the leakage path between source and drain. As we can see in figure 2.1, due to the overlapping of the gate polysilicon and the active-source edge, the high-dose source implant is set away from the field oxide through a p- area. Opposite to the enclosed layout, this solution allows to integrate transistors with small W/L ratio;
- Special transistors called FOXFETs, which stands for Field Oxide Field Effect Transistors, mainly to investigate the radiation-induced leakage between devices due to positive charge trapping in the field oxide (see 1.1.3). In FOXFETs in fact the gate oxide is made with field oxide hence, measuring their current, it is possible to measure directly the leakage underneath a STI isolation structure as a function of the total dose. This makes FOXFETs also useful to study the radiation-induced leakage current in MOSFET transistors. This is in fact mostly due to parasitic currents generated at the transistor’s edges (i.e. under the STI), which in MOSFET can’t be measured independently but

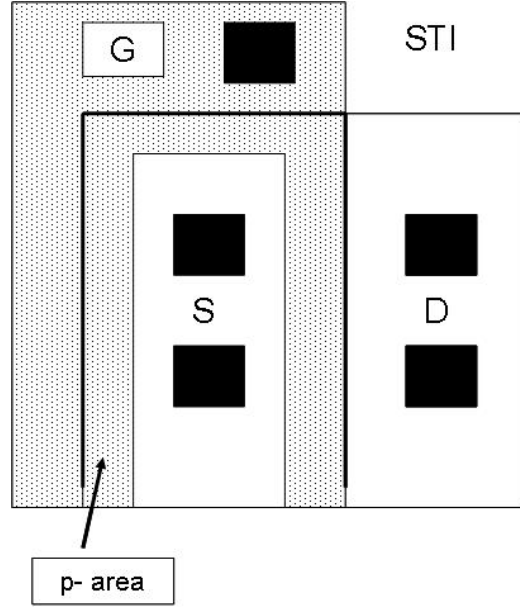


Figure 2.1: *Schematic illustration of the upper halve of a ringed-source transistor.*

just through the current flowing in the main transistor. In addition to that, since the evolution with TID of FOXFETs parameters, such as threshold voltage and subthreshold swing, is entirely due to the effects of radiation in the STI, FOXFETs can be used to study the characteristics of charge trapping and detrapping in the field oxide, through irradiation and isochronal annealing cycles.

The available FOXFETs are of three types: with n+ diffusions as source and drain (Figure 2.2), with n-well as source and drain and with n-well as source and n+ diffusion as drain (Figure 1.8). The gate, made of polysilicon for FOXFETs between n-wells and of metal in the other two configurations, it is used to simulate the worse case, i.e. a biased interconnection line running on top of the field oxide.

The sizes of the devices are $W=200\mu\text{m}$, $L=0.92$ and $1.48\mu\text{m}$ for the two FOXFETs between n-wells, 200/0.18 for the FOXFET between n+ diffusions, 200/0.3 and 200/0.6 for the two FOXFETs between n-well and n+ diffusion;

- Three rows of digital cells designed to study whether the guard ring is needed in library cells or not. As shown by the experience in the development of radiation tolerant digital libraries in fact, a lot of area

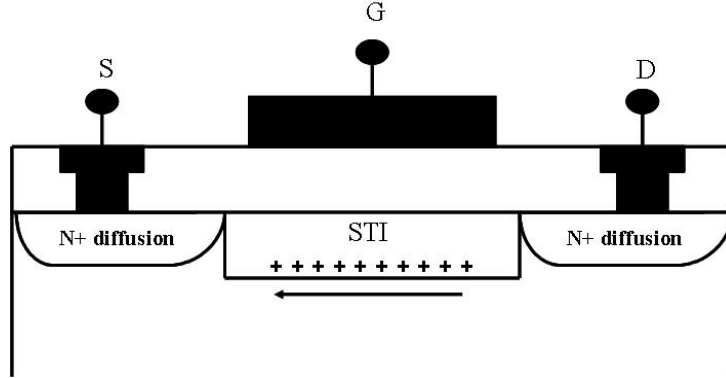


Figure 2.2: *Schematic illustration of a FOXFET between two n+ diffusions (i.e. the source and drain of two neighbor transistors).*

is lost because of guard rings which systematically separate n-wells and NMOS transistors. This is due to the fact that polysilicon lines can not be drawn above guard rings without preventing p+ implant in the guard ring. As a consequence, the guard ring would not be effective under the polysilicon and a conductive path could still be opened by TID. Connections across the guard ring have then to be made with metal, requiring poly-metal contacts to be added on the 2 sides. These contacts in turn require some space that expands the vertical dimension of the cell, as shown in figure 2.3.

The basic block of the digital cell contains an inverter and a flip flop, repeated for a total length of about $350\mu\text{m}$. In each row, the basic blocks are connected serially, the output of each flip flop being connected to the input of the inverter in the following block, whilst the input of the first inverter in the row is at V_{dd} potential. The V_{dd} potential of each row is separated, whilst the clock signal and the substrate V_{ss} are in common. In each row, the separation between n-well and NMOS transistors is either a full guard ring, a partial guard ring or nothing, as shown schematically in figure 2.3.

2.2 Test setup

A unique test setup (Fig. 2.4) has been developed on purpose at CERN to perform all the characterization, irradiation with X-rays and some annealing operations on an individual chip without the need for any manipulation,

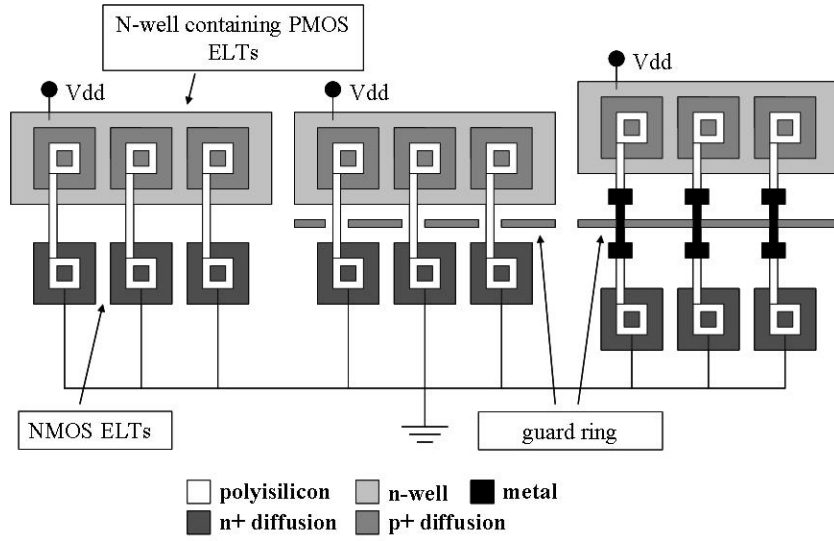


Figure 2.3: *Schematic illustration of the three rows of digital cells.*

hence ensuring that the extremely thin and fragile gate oxide of the transistors under test is not damaged due to mounting on a package or other handling. It is a wafer probe station equipped as follows:

- an X-ray irradiation system (SEIFERT RP149), in which a 3kW X-ray tube uses a tungsten target typical of radiation-effects studies on semiconductors;
- a Karl-Suss PA200 semi-automatic 8-inch wafer probe station, installed inside the X-ray cabinet, where the X-ray tube and a CCD camera can move via a computer-controlled motorized stepper. This allows the operator to either obtain a view of the chip under test to correctly position the probe tips of the probe card on the pads, or to position the X-ray tube over the chip to perform irradiation. The wafer chuck is from Digit Concept and it is thermally controlled over a range of +5 to +200°C;
- a custom-developed probe card, one for each of the three different test structures (A, B and C), with two columns of probe tips to match the number, size and pitch of the pads in the test structures. As for any high-precision low-noise measurement, the signal line is “protected” by a guard surrounding it all the way from the measurement instrument until almost the probe tips;

- a semiconductor parameter analyzer (HP4145B) to perform the static transistor measurements, applying and measuring currents and/or voltages (typically I_{ds} is measured as a function of V_{gs} and V_{ds});
- a voltage source to keep the transistors under correct bias during the irradiation and annealing steps;
- a Keithley 707 switching matrix to connect the measuring channels of the HP4145B or the output of the voltage source to the appropriate pads in the test structures.
- a PC running Labview which controls all the instrumentation and allows to perform the full measurement of the transistors connected to the pads in the test structures sequentially and fully automatically.

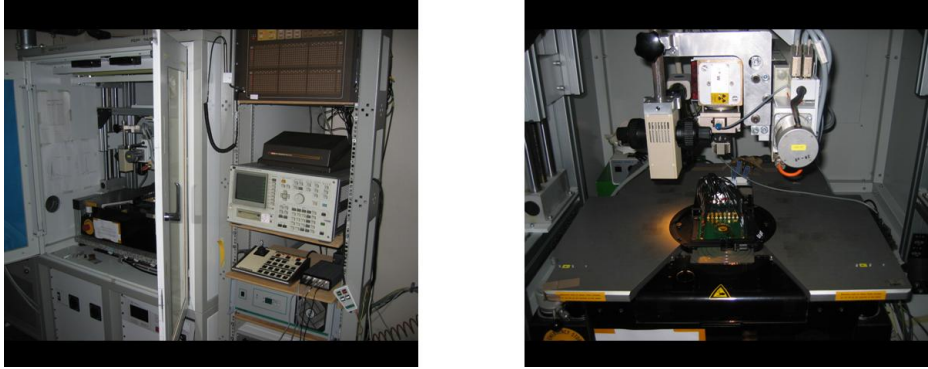


Figure 2.4: *Pictures of the test setup (left) and the wafer probe station (right).*

Additional low dose rate irradiation testing on FOXFETs between n-well and n+ diffusion has been performed using a ^{60}Co source. In that case the device was packaged in ceramic DIL40 packages and measured with the HP4145 using a test feature. The irradiation was performed at the ESTEC¹ Co-60 radiation facility (Fig 2.5). It provides a collimated Co-60 gamma rays source with a normal activity of 2000.00Ci (present activity: 1121.1Ci),

¹The European Space Research and Technology Centre (ESTEC) is the European Space Agency's main technology development and test centre for spacecraft and space technology. It is situated in Noordwijk, South Holland, in the western Netherlands. The test centre provides extensive test facilities to verify the proper operation of spacecraft, such as the Large Space Simulator (LSS), acoustic and electromagnetic testing bays, multi-axis vibration tables. Almost all equipment that ESA launches is tested at this test facility.

maximum rate of 66rad/min, minimum rate of 0.3rad/min. The facility consists of a control room and a radiation cell (each approximately 20m²), as shown in figure 2.5. In the radiation cell, a trolley movable on a rail system through a Remote Positing System (RPS), allows placing the samples for irradiation at a given distance from the source according to the desired dose rate. The RPS is controlled by a software suite installed on a PC in the control room. Automated total dose and dose rate setting, monitoring of experiments under test and standard logging options (i.e. timestamp, time into run, temperature in the control room and radiation cell) are available via software too. A multiplexer (which is connected to the control computer through IEEE) allows setting of voltages and currents as well as the standard logging values mentioned. A four-channel power supply (also connected via IEEE) is available for the software setting of voltages and currents. Cables between the two rooms run through path panel as shown in figure 2.5.

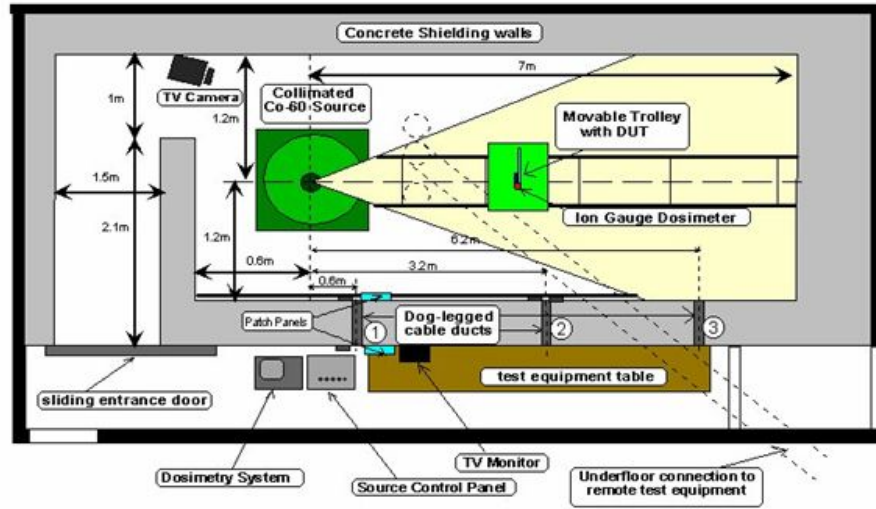


Figure 2.5: *ESTEC 2000 Ci Co-60 radiation facility [14].*

2.3 Irradiation details

In this work all the doses are expressed in SiO₂. Irradiation with X-rays was performed at room temperature at dose rates between 20 and 30krad/min².

²The total dose is generally expressed in Gray (Gy): 1Gy=1Joule/Kg. In the radiation effects community, as well as in this work, the old unit rad is used: 1rad=0.01Gy

All chips were irradiated in steps up to a TID around 100Mrad, some even to TID of about 200Mrad.

Irradiation with gamma rays was performed at room temperature as well but the dose rate was of only 64.8rad/min. The FOXFETs were irradiated up to a TID of 3.2Mrad.

During irradiations the transistors were kept under worse case bias: all terminal grounded for PMOS transistors and all terminal grounded except the gate, which was kept at 1.5V for core NMOS. In the case of NMOS dual gate transistors and FOXFETs that value was increased to 2.5V. Digital cells had the clock and the common V_{ss} connected to ground and the V_{dd} to 1.5V.

2.4 Isochronal annealing details ([15], [16])

The isochronal annealing technique is one of the simplest to setup among the techniques used to study the characteristics of radiation-induced charge trapping in MOS oxides. Opposite to other techniques, such as for instance isothermal and tempering measurements, which are time consuming and are based on the continuous measurement of a physical parameter while emptying the traps (i.e. as the sample is heated), the isochronal annealing can be performed fast and measurements are done at room temperature. It consists in fact in measuring at room temperature the effect of sequentially emptying a fraction of the traps through a succession of short annealing periods at increasing temperatures. Hence the traps characteristics can be obtained from isochronal annealing also when the other methods cannot be used. For some devices in fact it is not convenient or even possible to make high temperature measurements that provide information on the filled traps. Moreover, from the isochronal annealing it is possible to predict the isothermal annealing of the device. Combining this information with the charge trapping information (activation energy, frequency factor and trap density) makes it possible to extract from a time saving isochronal annealing experiment the long term behavior of the device.

This prediction method is based on the following assumptions: 1) the radiation exposure (i.e. trapping of charge) and the thermal annealing (i.e. detrapping of charge) causing time dependent effects are assumed to occur independently and are competitive; 2) the trapping rate is assumed to be proportional to the dose rate; 3) the detrapping probability is assumed to follow an Arrhenius law.

As a consequence it is possible to find the same net trapped charge either with a short annealing time at high temperature or with a long annealing

time at low temperature. Thus, the net trapped charge can be evaluated if the exposure conditions (temperature, dose rate, etc.) and the traps characteristics are known. Since trapping and detrapping processes are decoupled, the irradiation can be performed first and then isochronal annealing can be performed to determine the trap parameters.

The experimental determination of the trap characteristics, in particular their activation energy E_0 and the equivalent trapped density Y_0 , using an isochronal annealing curve is the first step of the prediction method. Isochronal experiments are based on the measurements of an electrical parameter Y , either voltage or current, related to the trapped charge as a function of the temperature.

In the case of a single trap, the inflection point of the $Y(T)^3$ curve (or maximum value of the $dY(T)/dT$ curve) is called the characteristic temperature T^* . Once this temperature has been found, the frequency factor F , the heating rate c and the activation energy E_0 associated with T^* are related, according to the simplified formalism on which this method is based, by the following formula:

$$\frac{E_0}{KT^*} = \ln\left(\frac{FKT^*}{cE_0}\right). \quad (2.1)$$

The heating rate is determined experimentally (in our case, according to the annealing procedure we followed, the heating rate was $5.5 \times 10^{-2} \text{Ks}^{-1}$). Then for a given frequency factor (we assumed for our calculations $F=10^{-7} \text{s}^{-1}$ as reported in [16]), equation (2.1) makes it possible to calculate the activation energy E_0 associated with any experimental value of the characteristic temperature T^* . The initial trapped-charge density Y_0 can be determined by integrating the $dY(T)/dT$ curve.

Starting from the experimentally deduced trap parameters, the second step is the prediction of the isothermal annealing behavior, an approach which makes it possible to avoid time-consuming measurements.

Since, as mentioned earlier, the detrapping probability follows an Arrhenius law, the annealing of the trapped charge as a function of the time t at a constant temperature T can be represented by

³In this work the $Y(T)$ curve was the un-annealed fraction of trapped charge as a function of the temperature. We calculated both the un-annealed fraction of oxide trapped charge and the un-annealed fraction of interface states as the percentage difference between the total ΔV (respectively ΔV_{ox} and ΔV_{it}) before annealing and the total ΔV (respectively ΔV_{ox} and ΔV_{it}) after each annealing step. Y_{0i} was then the fraction of the initial un-annealed trapped charge corresponding to the energy E_{0i} .

$$Y(t) = Y_0 \exp(-\sigma t). \quad (2.2)$$

Here σ is defined as the probability per unit time for a charge to be released from its trap, through the Arrhenius relation:

$$\sigma = F \exp\left(\frac{-E_0}{KT}\right) \quad (2.3)$$

where T is the annealing temperature in Kelvin.

Substituting the values of E_0 and Y_0 deduced from the isochronal annealing in (2.3) and (2.2), the isothermal annealing curve can be predicted.

This procedure presented for a single trap level can be extended to n levels by summing the contribution of each trap. Then, equations (2.3) and (2.2) yield

$$Y(t) = \sum_{i=1}^n Y_{0i} \exp\left(-F \exp\left(\frac{-E_{0i}}{KT}\right)t\right). \quad (2.4)$$

To perform the isochronal annealing the standard procedure was followed: the sample was cyclically heated to reach a dwell temperature, kept in that condition for a dwell time, then cooled down to room temperature to be measured. The dwell temperature was increased at each subsequent step, typically by 20°C.

Since the thermal inertia of the temperature controlled chuck used in this work is such that the heating and cooling times are far too long for an isochronal annealing study⁴, we had to remove the silicon die containing the test structure from the wafer probe station for each thermal cycle, during which it was consequently un-biased, and to bring it back for the measurement at the end of the cycle.

In agreement with [15] and [16], we chose dwell times of 360s and temperature steps of 20°C, in a range between 40 and 300°C. The sample was positioned on a pre-heated bulky metal plate inside an oven for each annealing step. Given the thermal conductivity of silicon, the tiny mass of the silicon die and the large mass of the metal plate, the sample was heated almost instantaneously to the dwell temperature. At the end of the dwell time, the sample was extracted from the oven and positioned 120s on top of a bulky metal plate pre-cooled to -27°C, ensuring a quick cooling time. It was then measured at our probe station at room temperature.

⁴The difficulty of the experiment is often to ensure that the heating and cooling times are short compared to the dwell time, so that the effects during heating and cooling are minimal.

2.5 Measurements and parameter extraction

The characterization of MOSFETs has been done measuring the I_{ds} vs V_{gs} curve in linear regime ($V_{ds}=20$ mV) and in saturation ($V_{ds}=1.5$ V for core transistors and $V_{ds}=2.5$ V for I/O transistors) and the I_{ds} vs V_{ds} curve for $V_{gs}=1$ V and $V_{gs}=1.5$ V. The electrical parameters of MOS transistors of interest for our work were the threshold voltage, the leakage current and the transconductance g_m . They have been extracted from the transistors characteristics as follow:

- Threshold voltage has been extracted in two different ways. One consists in linearly fitting the square root of the I_{ds} vs V_{gs} curve in saturation ($V_{ds}=1.5$ V) and finding the intercept with $I_{ds}=0$ A. The other one consists in linearly fitting the I_{ds} vs V_{gs} curve in linear regime ($V_{ds}=20$ mV) for values of V_{gs} around the maximum of the g_m (in linear region as well) and finding the intercept with $I_{ds}=0$ A;
- The leakage current is the current which flows between drain and source for $V_{gs}=0$ V and $V_{ds}=1.5$ V for core transistors and 2.5V for I/O transistors;
- The transconductance has been extracted as the derivative of the I_{ds} vs V_{gs} curve in linear regime. We then considered for our calculations the maximum value of g_m .

FOXFETs have been characterized measuring the I_{ds} vs V_{gs} curve for $V_{ds}=20$ mV and $V_{ds}=2.5$ V. The parameters of interest extracted were V_{th} and S. To extract the latter, first a linear fit has been performed on the subthreshold region of the logarithmic I_{ds} vs V_{gs} curve in saturation. S has then been calculated as the inverse of the swing of the linear fit.

For the digital cells we wanted to measure the current between V_{dd} and the substrate for each row because it is the leakage between the n-well and the grounded diffusions of NMOS transistors. We measured it varying V_{dd} from 0 to 1.5V and for voltages applied to the clock line of 0 and 1V.

Chapter 3

Core transistors

3.1 Enclosed Layout Transistors (ELT)

The results obtained on the edgeless transistors, both NMOS and PMOS, demonstrate the extremely high TID tolerance of the gate oxide of the studied technologies. As it can be seen from figure 3.1, the shape of the I_{ds} vs V_{gs} curve of these transistors is not affected by radiation, being the same before and after irradiation. Hence, the effect of the radiation on the characteristics of ELT core transistors, such as threshold voltage and leakage current, is practically unnoticeable (Figures 3.3 and 3.5).

As already mention in 2.1, the measurements on the ELTs have been used to assess the validity of the formula (1.7) for the 130nm CMOS process. In order to do so, we extracted the effective W/L ratio from the measurements and compared it with the one calculated using the formula.

To extract the effective W/L ratio we compared the maximum value of the transconductance in linear region of ELT transistors with the maximum value of the transconductance in linear region of standard devices with the same L: since the W for standard devices is known, from the transconductance ratio we can extract the W for the ELTs. The effective W/L is then obtained dividing the extracted W for the effective L (L_{eff} , see 1.3).

From the results shown in table 3.1, we can notice that the agreement between the formula and the measured W/L ratios is less good than in the case of the quarter micron process reported in the literature¹ [17]. It is worth considering that since the transistor shape didn't change, we assumed that the modeling work still held (i.e. there are no new effects that have to be

¹In the quarter micron process the difference between the calculated and extracted $(W/L)_{eff}$ was 0% for $L=0.5$ and $5\mu m$, around 1% for most lenght sizes and 6.25% for $L=3\mu m$.

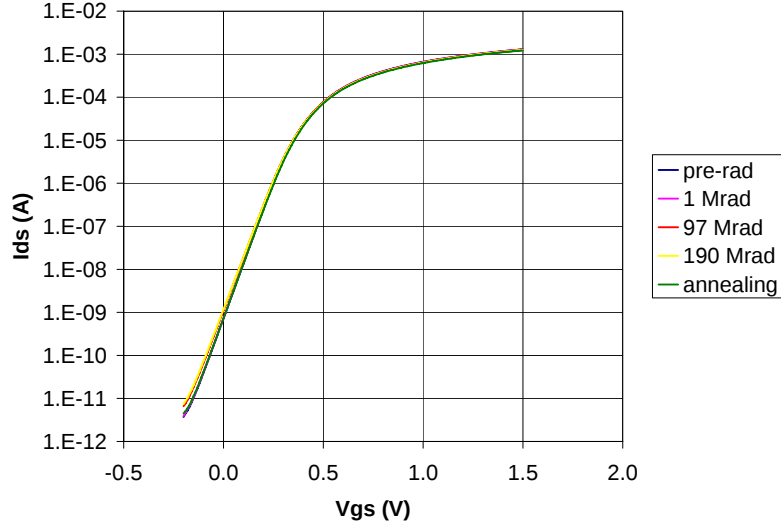


Figure 3.1: I_{ds} vs V_{gs} curve in saturation for different TID for an enclosed transistor with minimum W and $L=0.12\mu\text{m}$ in technology C .

	L_{drawn}	Calculated $(W/L)_{eff}$	Extracted $(W/L)_{eff}$	Diff.
NMOS	$0.12\mu\text{m}$	17.91	17.12	+4.64%
	$0.24\mu\text{m}$	8.93	9.59	-6.84%
	$0.48\mu\text{m}$	5.27	5.64	-6.61%
	$0.96\mu\text{m}$	3.60	3.82	-5.72%
	$2\mu\text{m}$	2.76	2.53	+9.09%
PMOS	$0.12\mu\text{m}$	17.91	16.27	+10.13%

Table 3.1: Calculated and extracted $(W/L)_{eff}$ and percentual difference between the two for edgeless transistors.

taken into account) and we used the value of α calculated for the technology nodes from 2.5 to $0.25\mu\text{m}$. The bigger percentage difference we have in the case of 130nm process might be due to these two facts. The agreement is anyway acceptable for most practical applications. For instance, from the design point of view, a difference of 10%, as in the case of the PMOS enclosed transistors, can be taken in consideration in the design phase.

3.2 Linear Transistors

Opposite to the ELTs, linear transistors are affected by TID, as typically observed in any commercial technology.

The most evident effect we noticed is a deformation of the subthreshold region of the I_{ds} vs V_{gs} curve of NMOS transistors. An example is shown in figure 3.2 for a transistor of technology C. Though different, this effect has been observed in all the three studied technologies, both in wide ($W \geq 1\mu\text{m}$) and narrow NMOS transistors ($W < 1\mu\text{m}$). A consequence of this deformation is the variation in the leakage current of the devices with TID. In the case of figure 3.2, for example, the leakage current increases for TID up to a few Mrad and decreases for higher TID and after annealing.

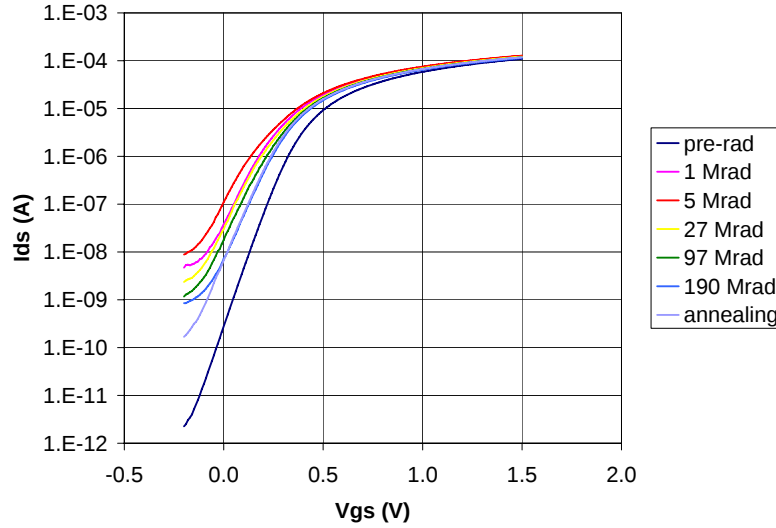


Figure 3.2: I_{ds} vs V_{gs} curve in saturation for different TID for a linear transistor with aspect ratio 0.16/0.12 in technology C.

This can be better observed in figure 3.3 where the evolution of the leakage current with TID for different NMOS transistor sizes in the three technologies is shown. For technology A we can observe a peak which has little dependence on the transistor width or length. Although the pre-irradiation values of the leakage current change with size, depending on the threshold voltage of the transistors (which in turns depends on the size), all curves peak approximately between 10^{-6} and 10^{-5}A , for a TID of about 1-10Mrad. A similar peak can be noticed in the case of technology C as well, but less

pronounced than the one in technology A, in particular for larger transistors ($W=10\mu\text{m}$). The maximum values of the leakage current are all distributed in a range between 10^{-8} and 10^{-7}A and for a TID of about 1-7Mrad. After annealing the value of the leakage current of the transistors with $W=10\mu\text{m}$ is close to the pre-rad one, whilst for the others transistors, it is still about one order of magnitude bigger than the pre-rad value. In the case of technology B, we can first of all notice that the values of the leakage current before irradiation are higher than in the other two technologies. For the narrow transistors it is still possible to recognize a peak around a few 10^{-7}A , as in technologies A and C, but smaller (the leakage current increases of just one order of magnitude). The current peaks for TID of about 3Mrad. After that it decreases slowly, showing a significant decrease just after annealing, when it reaches values close to the pre-rad ones. The leakage current of the wide transistor does not seem to be affected by radiation.

These observations can be explained as follows. Radiation-induced positive charges are quickly trapped in the STI oxide at the transistor edge and their accumulation eventually builds up an electric field sufficient to open an inversion channel through which source-drain leakage current can flow (i.e. the parasitic lateral transistors turn on). At higher TID, due to their slower formation process, the interface states start to appear. Hence, the negative charge trapped in the interface states (in the case of NMOS transistors) only starts to compete with the oxide-trapped charge with some delay, giving origin to the rebound effect. For the STI oxide of the studied technologies and the dose rate used for the irradiation, this happens when the TID reaches a value between 1-10Mrad for foundry A, around 3Mrad for foundry B and 1-7Mrad for foundry C. From this point on the interface states contribute significantly to the charge balance at the transistor edge, increasing the threshold voltage of the parasitic lateral transistor and hence decreasing the leakage.

Nevertheless, the contribution of the parasitic lateral transistors to the leakage current can only be observed when the current in the parasitic lateral transistors is larger than the current in the the main transistor, at the same V_{gs} . For instance, in the case of the two transistors with $W=10\mu\text{m}$ in technology C and for the transistors in technology B, the effect of the lateral parasitic transistors is partially or totally “hidden” because of the high leakage current before irradiation of these devices. This value, as already mentioned before, depends on the threshold voltage of the devices and on their size.

For technology B one more consideration has to be done. Because of

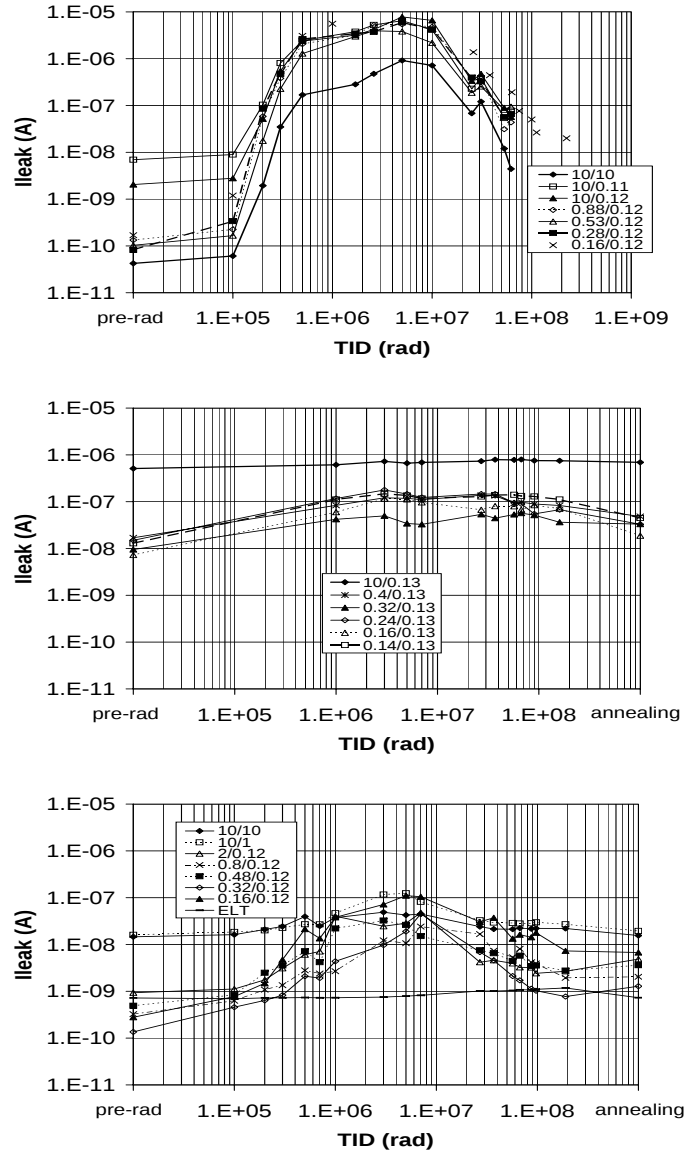


Figure 3.3: Evolution of the leakage current with TID for different transistor size in technology A(top), B(middle) and C(bottom). The transistor with aspect ratio 0.16/0.12 in technology A has been measured on a different chip with respect to the others. The last point in technology B and C refers to full annealing at 100°C for one week.

differences in the processing in the three foundries, the effect of the lateral parasitic transistors is less pronounced in this technology then in the other

two. Hence, the small variation of the leakage current with TID in technology B is due also to the smaller deformation of the subthreshold region of the I_{ds} vs V_{gs} curve.

To summarize we can say that the effect of the parasitic lateral transistors is present in all the three technologies, but it is quantitatively different for every one because of differences in the processing in the three foundries, being smaller in technology B with respect to the other two technologies. Transistors of the same technology are affected in the same way but, due to the differences in their threshold voltage and size (i.e. in the value of the leakage current before irradiation), the evolution of the leakage with the dose might be different for transistors made by the same foundry.

In the case of linear PMOS transistor, the leakage current is never a problem, since the radiation-induced positive charge trapping in the lateral STI increases, in absolute value, the threshold of the parasitic lateral transistors, reducing their current. Hence what we observe in figure 3.4 for V_{gs} below 0V is not a leakage between source and drain but another form of “off-state” current in MOS transistors called Gate-Induced Drain Leakage (GIDL) [18] leaking between drain and substrate. In NMOS transistor it is probably hidden by the higher leakage current at the transistor edges.

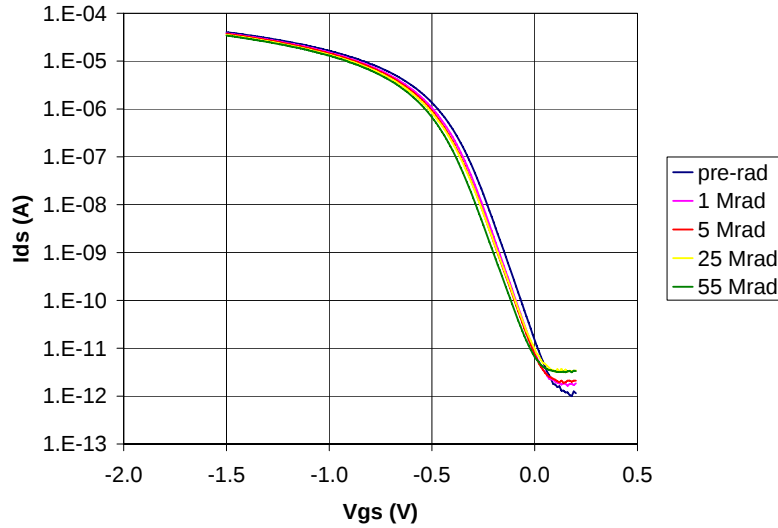


Figure 3.4: I_{ds} vs V_{gs} curve in saturation for different TID for a PMOS linear transistor with aspect ratio 0.16/0.12 in technology C.

Looking at figures 3.2 and 3.4 we can observe another effect: a shift of the threshold voltage for narrow transistors, both NMOS and PMOS. This is due to the fact that, for narrow channel transistors, the charge balance at the transistor edges not only influences the leakage current, by determining the accumulation, depletion and inversion condition of the parasitic lateral transistors, but also influences the electric field of the main transistor. This effect is known in CMOS technologies as “narrow channel effect” and it is observable in any deep submicron process as a decrease of the V_{th} with transistor width.

The radiation-induced threshold voltage shift for the NMOS transistors peaks, for every technology (Figure 3.5), at the same TID as for the leakage current evolution. In this case, though, it is strongly dependent on the transistor width, the transistors with W larger than about $1\ \mu\text{m}$ showing only a marginal effect. This is due to the fact that because of the positive charge trapped in the STI oxide, the narrow channel effect decreases the threshold of sufficiently narrow NMOS transistors, whilst it should increase it (in absolute value) for PMOS transistors. In the case of the PMOS the charges trapped in the interface states are also positive and add to the effect of the oxide-trapped charge; thus, rather than the peaking observed for the threshold voltage of NMOS transistors (Figure 3.5), we observe an increase of the slope of the V_{th} shift with TID.

This is indeed what we observe clearly for technologies A and C in figure 3.6: the threshold voltage shift increases with TID, mostly because of the build-up of interface states², but it does not seem to be dependent on the transistors W in the case of technology A. The same observation can be done for technology B, where we observe a general rising trend of the curves. Anyway, a threshold voltage shift of 15-20mV is smaller than the natural dispersion of the threshold voltage shift values before irradiation and hence can be neglected for practical purposes. Therefore, other than for the narrower transistor in technology C, we can conclude that there is no significant threshold voltage shift for PMOS core transistors.

The different sensitivity to TID of transistors with different gate width illustrated in figure 3.5 and 3.6 has been reported in the literature as “Radiation Induced Narrow Channel Effect” (RINCE) [19].

²As already mentioned in 1.1.3, due to the bias condition of the gate in PMOS transistors, the effect of the oxide trapped charge is negligible in p-channel MOSFETs.

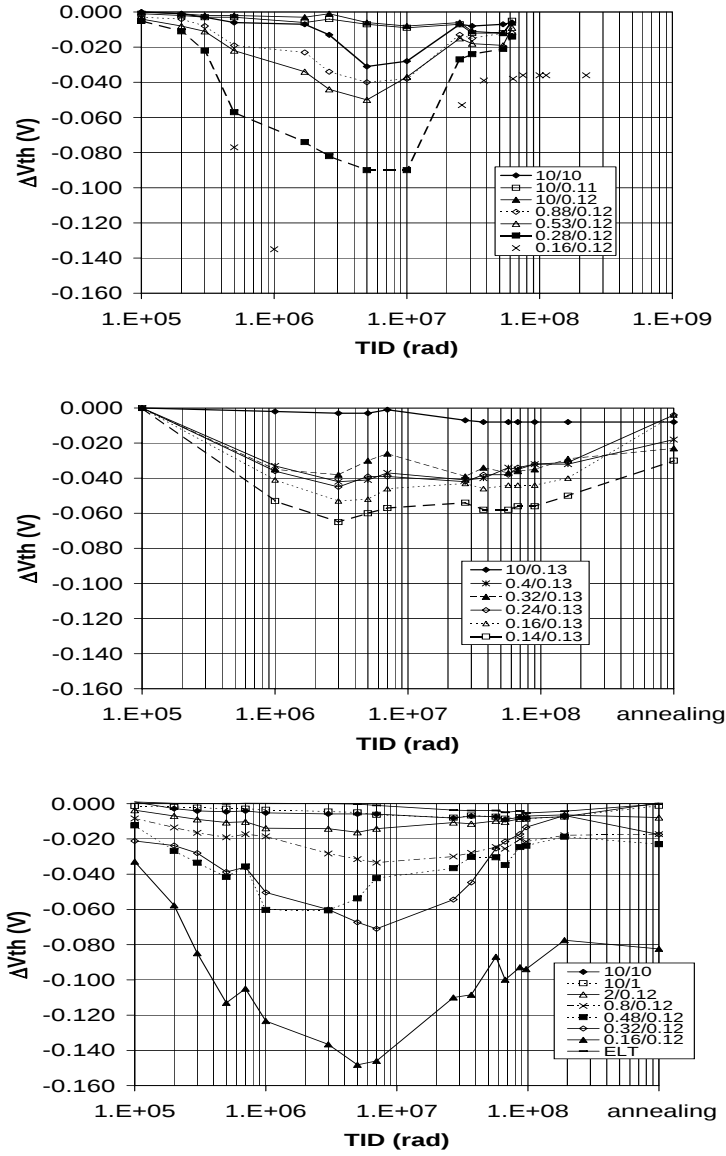


Figure 3.5: V_{th} shift with TID for different NMOS transistor size in technology A(top), B(middle) and C(bottom). The transistor with aspect ratio 0.16/0.12 in technology A has been measured on a different chip with respect to the others. The last point in technology B and C refers to full annealing at 100°C for one week. The threshold voltage has been extracted in saturation ($V_{ds}=1.5\text{V}$).

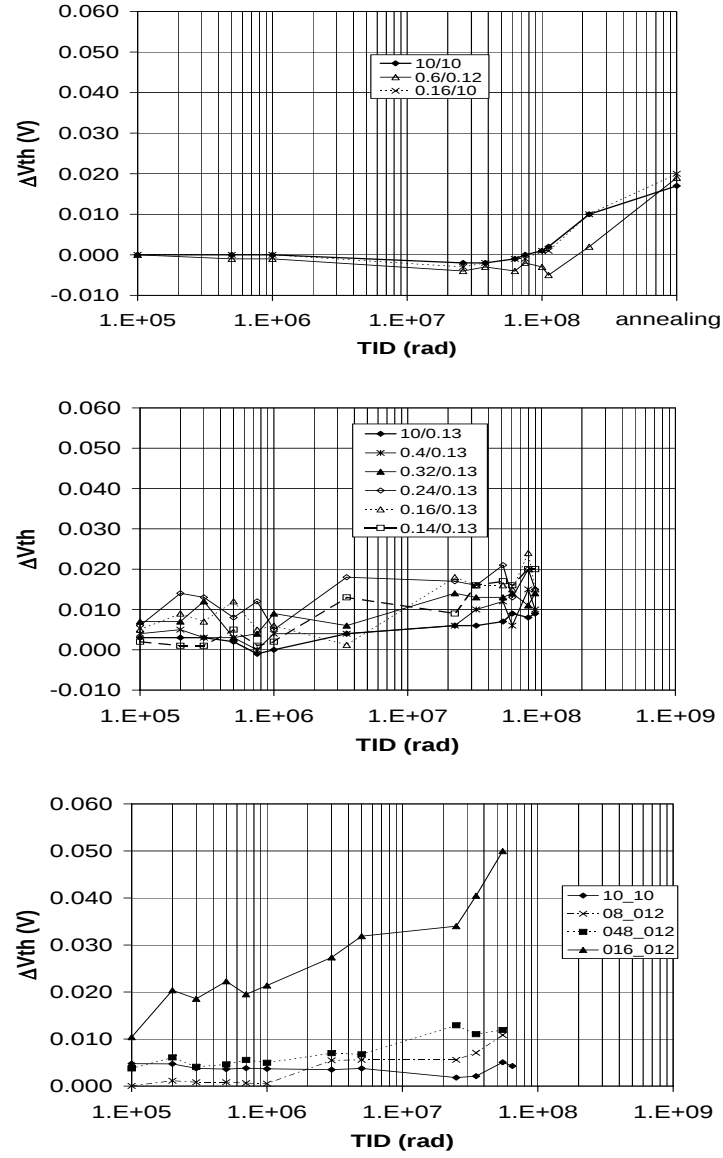


Figure 3.6: V_{th} shift (in absolute value) with TID for different PMOS transistor size in technology A(top), B(middle) and C(bottom). The last point in technology A refers to full annealing at 100°C for one week. The threshold voltage has been extracted in saturation ($V_{ds}=1.5V$).

3.3 Ringed Transistors

A previous work on NMOS ringed transistors [20] accounted for a total-dose-induced parasitic effect in this kind of structure. According to the results shown in the paper, the normal radiation-induced edge leakage current becomes gate controlled in ringed-source transistors. This effect has been explained as follows.

The total-dose-induced leakage path between source and drain, due to positive charge trapping in the lateral STI (Figure 3.7 left, black arrow), is cut because of the overlapping of the gate polysilicon and the active-source edge. As already mentioned in 2.1, thanks to this overlapping, the high-dose source implant is set away from the field oxide through a p- area. Nevertheless, the p- area can reach inversion for high enough gate voltages applied on the polysilicon gate, hence opening the leakage path between source and drain (Figure 3.7 left, dashed arrow).

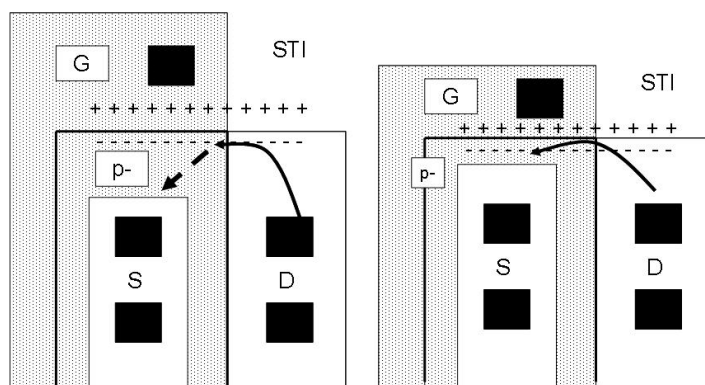


Figure 3.7: *Schematic illustration of the upper half of a ringed-source transistor and of the possible total-dose-induced edge leakage path for an older CMOS process (0.35μm, left) and for a modern one (130nm, right). We can see that the negative charge induced by the positive charge trapped in the lateral STI is an important part of the p- area at the active-source edge in new technologies.*

As a consequence, in small W/L NMOS, where the gate-controlled leakage current approaches the magnitude of the ideal channel current, an additional drain current and transconductance appear, having a major impact on analog applications.

The results we obtained from our measurements on NMOS ringed transistors in technology C showed that, for modern CMOS processes (the one

used for the work presented in [20] was the $0.35\mu\text{m}$ CMOS process), the ringed layout solution is not at all effective anymore in preventing leakage at the device edge, so that also the digital applications would be compromised by the use of this transistor layout.

If in older CMOS processes the leakage path between source and drain at the edge of the transistor was cut at least for low voltages applied to the gate, in more modern CMOS processes, due to the shrinking of the p- area, the charge trapping in the lateral STI determines itself the inversion of the p-channel opening a leakage path between source and drain (Figure 3.7, right). Hence, as well as in linear layout transistors, the leakage current is due only to radiation effects in the field oxide (STI) and at its interface $\text{SiO}_2\text{-Si}$ (p- in this case).

This can be seen in figure 3.8, where we can see a deformation of the subthreshold region of the I_{ds} vs V_{gs} curve of an NMOS ringed transistor similar to the one we observed for the linear design (Figure 3.2).

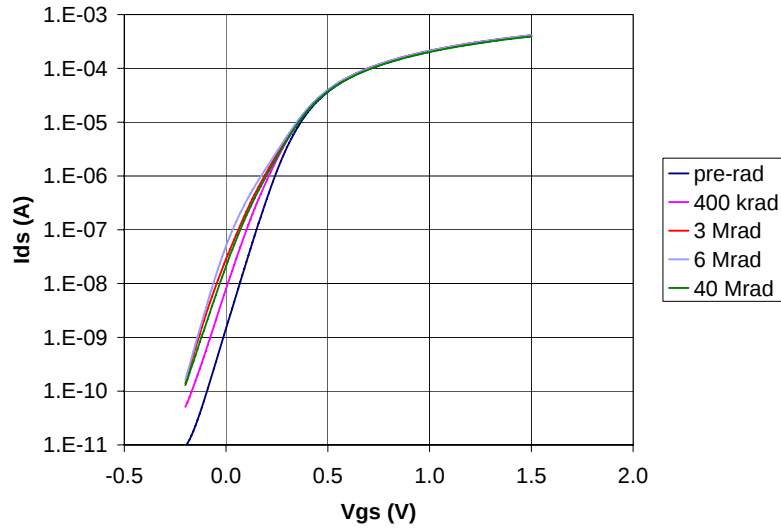


Figure 3.8: I_{ds} vs V_{gs} curve in saturation for different TID for a NMOS ringed transistor with aspect ratio 3/0.24 in technology C.

Looking at figures 3.9 and Figure 3.10 we can clearly observe the opposite contribution of the positive charge trapping in the STI and of the interface states built-up on the p- area. The leakage current reaches a peak for the same values of current (a few 10^{-7}) and TID (3-6Mrad) as in the case of linear

layout transistors (Figure 3.3), in particular as the 2/0.12 linear transistor which is the one with the closest aspect ratio. For the threshold voltage shift the rebound is observed at a TID of about 6Mrad. Anyway, being the transistors large ($W=3\mu\text{m}$), the threshold voltage shift is negligible.

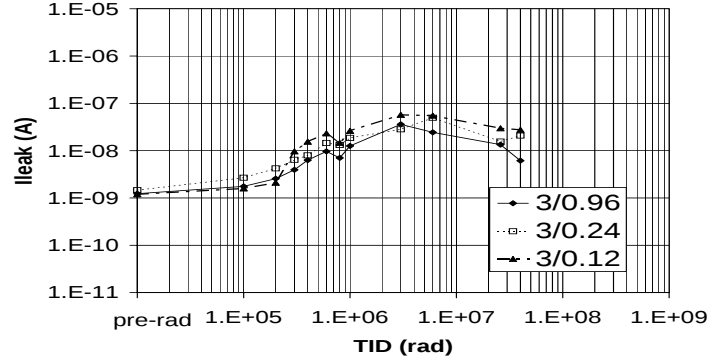


Figure 3.9: *Evolution of the leakage current with TID for ringed layout transistors in technology C. The scale on both axes has been expanded to make a comparison with figure 3.3.*

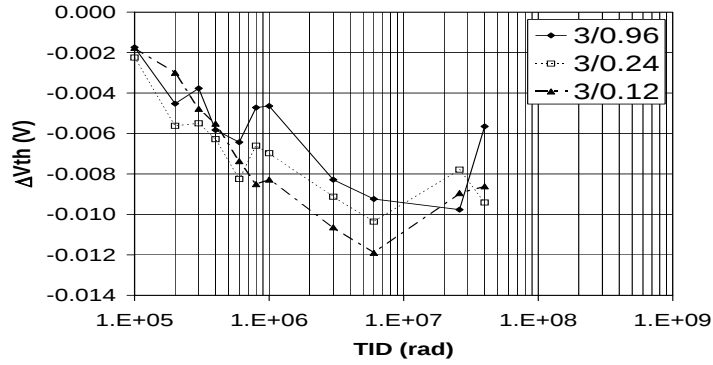


Figure 3.10: *Threshold voltage shift evolution with TID for ringed layout transistors in technology C. In this case, the threshold has been extracted in linear regime.*

To avoid leakage current in ringed transistors one solution would be to increase the p-area. This will come at a cost of area which is not convenient

in digital applications in general and not in this case in particular because it will not bring significant advantages.

The advantages of using ringed transistors are in fact that, opposite to ELTs, there are no restriction on the achievable W/L and moreover their area is smaller than the area of an enclosed transistor for the same W/L .

If the area of ringed transistors has to be increased to avoid leakage then ELTs can be used instead, as long as small W/L are not required. Nevertheless, small W/L transistors are mostly used in strong inversion, a region which is not affected by radiation. Hence, in this case, no measures have to be taken to avoid radiation effects and standard layout transistors can be used.

Chapter 4

Input/Output transistors

4.1 Enclosed Layout Transistors (ELT)

The results obtained on I/O transistors are conceptually similar to those presented for the core transistors, but with the addition of a noticeable sensitivity of the thicker gate oxide itself. This is evident looking at the I_{ds} vs V_{gs} curve of an I/O NMOS enclosed transistor in figure 4.1. Opposite to the core case, a threshold voltage shift can be observed. Also the GIDL is evident in this case [18].

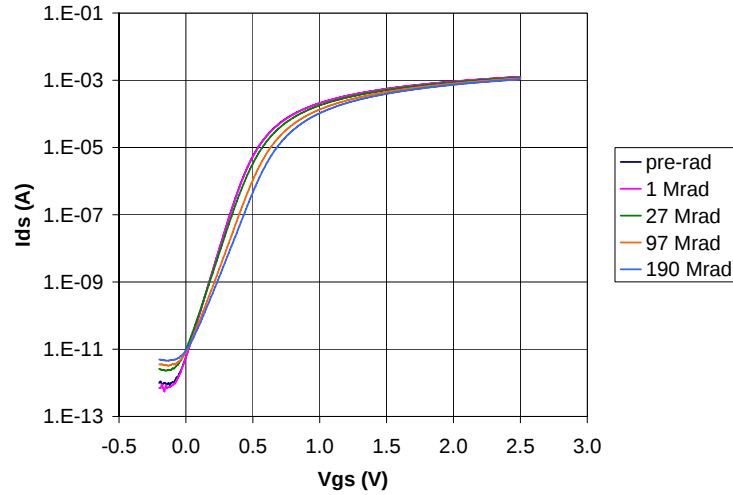


Figure 4.1: I_{ds} vs V_{gs} curve in saturation for different TID for an I/O enclosed transistor with minimum W and $L=0.26\mu\text{m}$ in technology C .

The threshold voltage shift for NMOS and PMOS enclosed transistors is shown in figure 4.2. We can observe a relevant ΔV_{th} for both types of transistors, although more pronounced for PMOS ELTs: for a TID of 40Mrad, the threshold voltage shift is around 40mV for the n-channel ELT and 180mV for the p-channel one (Figure 4.2).

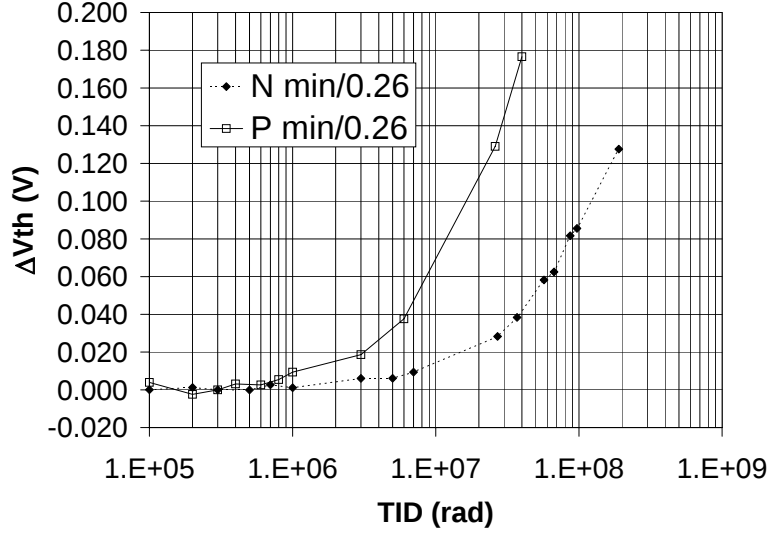


Figure 4.2: Evolution of the threshold voltage shift (in absolute value for the PMOS transistor) with TID for I/O enclosed transistors. The threshold has been extracted in saturation ($V_{ds}=1.5V$).

4.2 Linear Transistors

The effect of radiation in the thicker gate oxide of I/O transistors can be observed also for linear transistors both NMOS (Figure 4.3) and PMOS (Figure 4.4).

In the case of technology A, opposite to the core transistors case (Figure 3.5 and 3.6 top), also large NMOS and PMOS transistors ($L=10\mu m$) undergo a relevant threshold voltage shift (Figure 4.3 and 4.4 top). Hence we can deduce that the threshold voltage shift we observe is only due to radiation effects in the gate oxide and not in the lateral STI.

For NMOS transistors we can observe a peak in the threshold voltage shift, more pronounced for longer transistors, at a TID of 4Mrad due to

early trapping of positive charge in the gate oxide and later formation of interface states (Figure 4.3 top). This latter continues during annealing to give a final shift of 100mV. For PMOS transistors the total shift is of about 150-180mV at a TID of about 70Mrad (Figure 4.4).

For NMOS transistors in technology B the threshold voltage shift peaks at a higher TID than in the core case, of about 60Mrad, as we can see from figure 4.3 middle. As well as for the core case, the RINCE contributes to the shift: the narrower transistor ($W=0.4\mu\text{m}$) has a threshold voltage shift of 60mV, whilst for the other transistors it is about 30-40mV (Figure 4.3 middle).

In the case of PMOS transistors the threshold voltage shift is negligible¹ (Figure 4.4 middle) as it was for core PMOS transistor in this technology (Figure 3.6 middle).

For NMOS transistors in technology C we can again observe the rebound of the threshold voltage shift (Figure 4.3 bottom). In analogy with the core devices (Figure 3.5 bottom), the narrower transistors show a more pronounced peak in the threshold voltage shift at doses around 1-3Mrad due to the early trapping of positive charges in the lateral STI oxide. At doses larger than about 10Mrad, the threshold voltage shift rebound is due to radiation effects in the gate oxide and not in the lateral STI, as demonstrated by the ELT results.

In the case of PMOS transistors we observe a relevant threshold voltage shift (Figure 4.4 bottom). Whilst for the core transistors case the threshold voltage shift of the larger transistor with $W=10\mu\text{m}$ was negligible (Figure 3.6 bottom), in this case it reaches 170mV at a TID of 65Mrad. This proves that there is a contribution to the threshold voltage shift from the charge trapped in the gate oxide. Anyway the RINCE is still important: for narrower transistors the threshold voltage shift is bigger than for wide transistors, around 330mV after 55Mrad. Hence for I/O PMOS transistors, the contribution to the shift comes both from the RINCE and from the charges trapped in the gate oxide.

¹The negative value of the threshold voltage shift is due to the algorithm used for the threshold extraction.

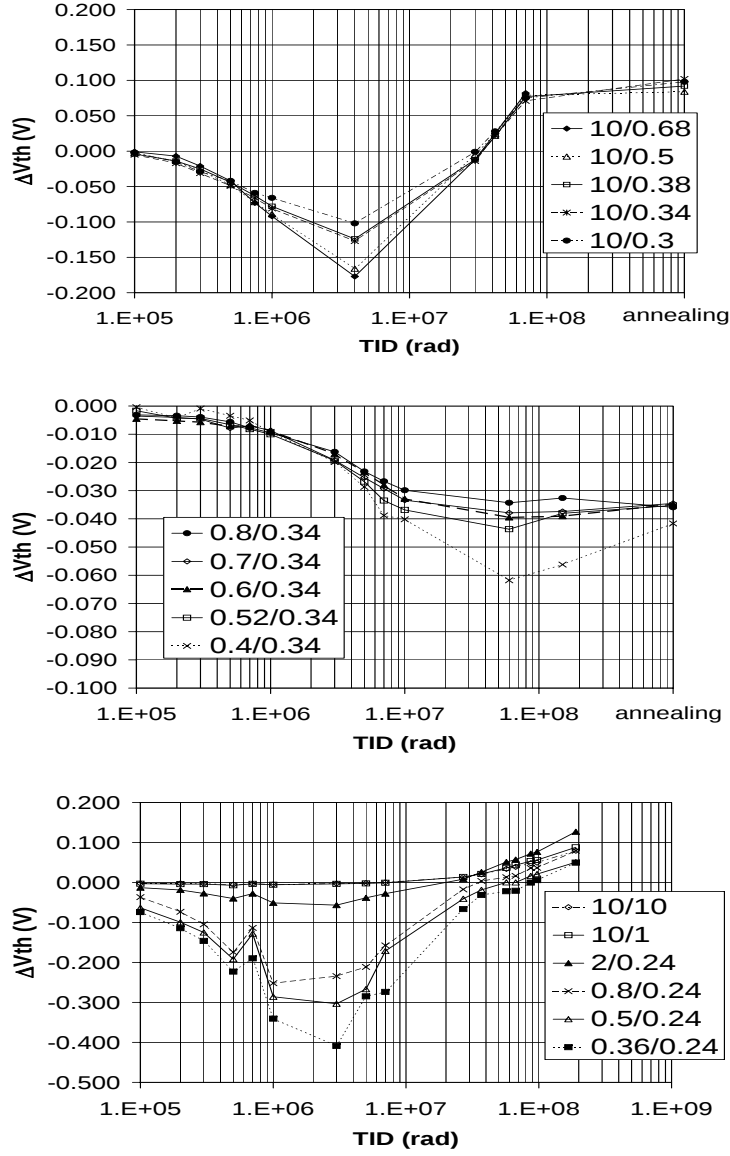


Figure 4.3: V_{th} shift with TID for different NMOS transistor size in technology A(top), B(middle) and C(bottom). The last point in technology B refers to full annealing at $100^{\circ}C$ for one week. The threshold voltage has been extracted in saturation ($V_{ds}=1.5V$).

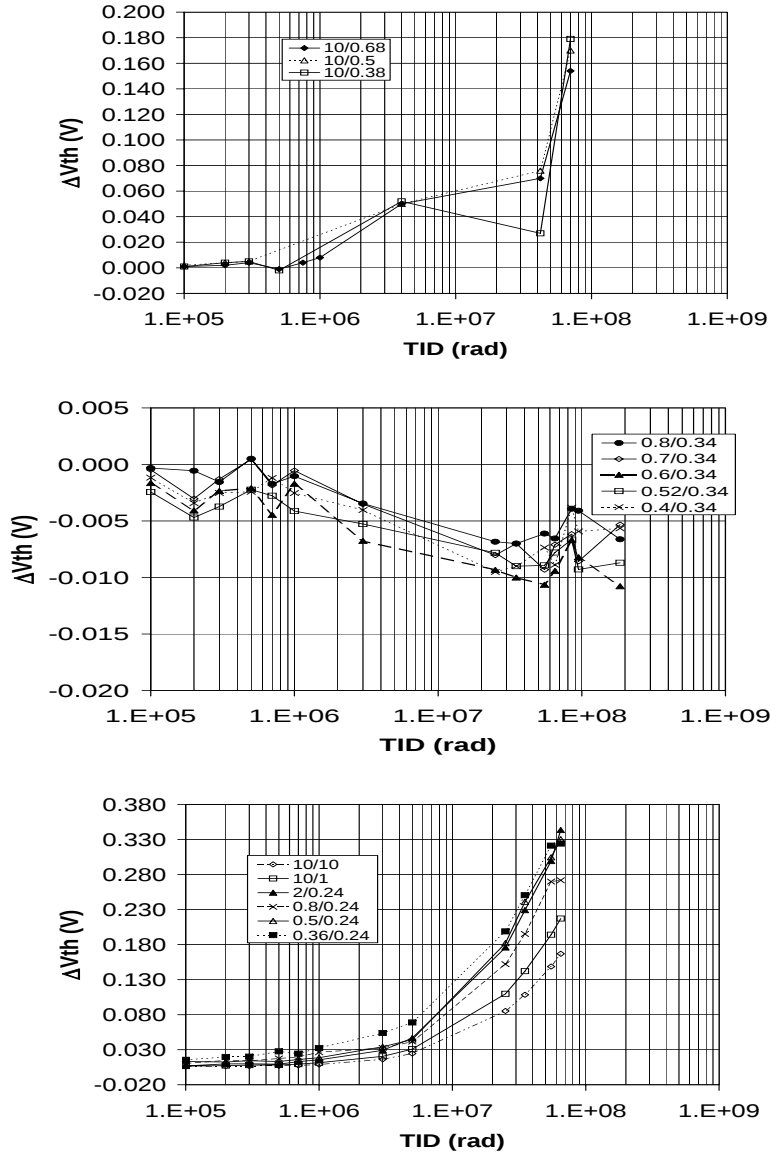


Figure 4.4: V_{th} shift (in absolute value) with TID for different PMOS transistor size in technology A(top), B(middle) and C(bottom). The last point in technology B refers to full annealing at 100°C for one week. The threshold voltage has been extracted in saturation ($V_{ds}=1.5\text{V}$).

The leakage current for NMOS I/O transistors, shown in figure 4.5 reaches maximum values higher than in the core case (a few 10^{-4} A for technology A, a few nA for technology B and a few μ A for technology C). For technology A and C the peak is reached for the same TID as in the core case, whilst for technology B the leakage current peaks at a dose of about 100Mrad as the threshold voltage shift.

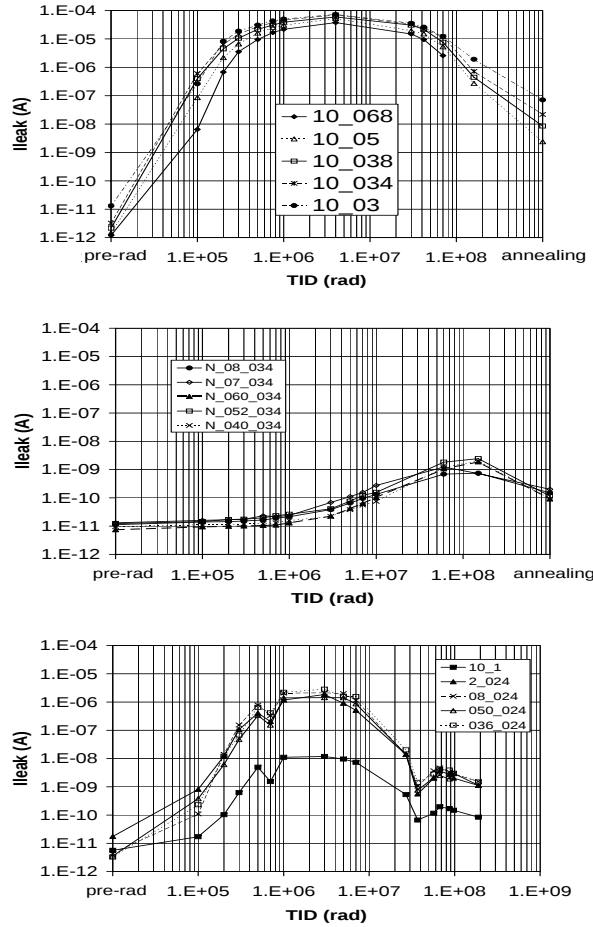


Figure 4.5: Evolution of the leakage current with TID for different transistor size in technology A(top), B(middle) and C(bottom). The last point in technology A and B refers to full annealing at $100^{\circ}C$ for one week.

Chapter 5

FOXFETs and Digital Cells

5.1 FOXFETs with n-well as source and n+ diffusion as drain

This type of FOXFET was designed to simulate a very common situation in the CMOS digital logic: an n-well connected to the power supply leaking toward the grounded source of an n-channel transistor (n+ diffusion). With the gate contact, we also simulated an interconnection line running on top of the field oxide in the first metal level, biased at 2.5V during irradiation. The closest real case is the CMOS inverter, although in this case the interconnection line, connecting the gate of the NMOS transistor with the gate of the PMOS transistor, would be of polysilicon with a bias of 1.5V. Anyway, since the polysilicon is closer than the first metal level to the field oxide, we can assume that the electric field in the STI during irradiation would not be that different in the two cases and hence we can consider our FOXFETs a good simulation of the real structure and use them to study the leakage current between n-wells and n+ diffusions at different potentials in real applications.

The results of the irradiation of FOXFETs between n-well and n+ diffusion are shown in figure 5.1. In the early irradiation stages (i.e. for doses of a few hundreds of krad), we observe a significant shift of the I_{ds} vs V_{gs} curve to lower V_{gs} , or, in other words, a decrease of the threshold voltage of the device due to positive charge trapping in the STI. Increasing the TID, due to the interface states built-up, the curve starts to shift to higher V_{gs} and the subthreshold swing increases considerably.

This can be better seen in figure 5.2, where the subthreshold swing S is plotted as function of the TID. Starting from a value of about 10V/dec, at a TID of 40Mrad, S reaches a value around 41V/dec, for the FOXFET with

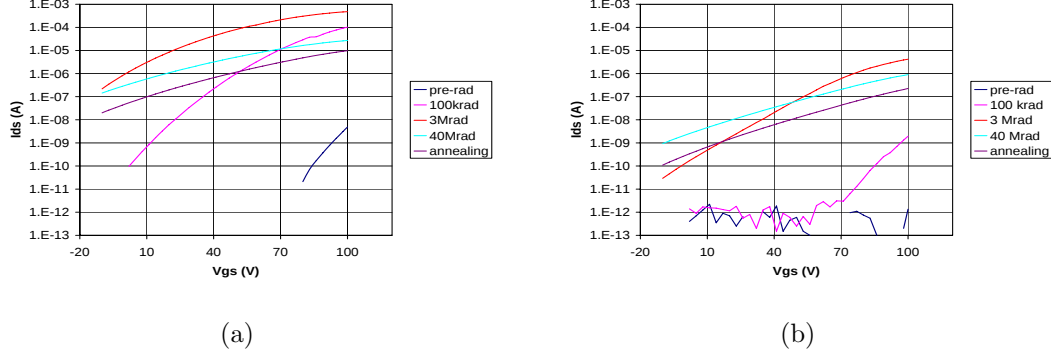


Figure 5.1: I_{ds} vs V_{gs} curve for different TID for FOXFETs between n-well and n+ diffusion with aspect ratio 200/0.3 (a) and 200/0.6 (b). Annealing has been performed for 60 hours at room temperature with the chip under bias.

aspect ratio 200/0.3 and 33V/dec for the one with aspect ratio 200/0.6. After annealing at room temperature for 60 hours with the chip under bias, we can observe that the subthreshold slope starts to decrease for both FOXFETs.

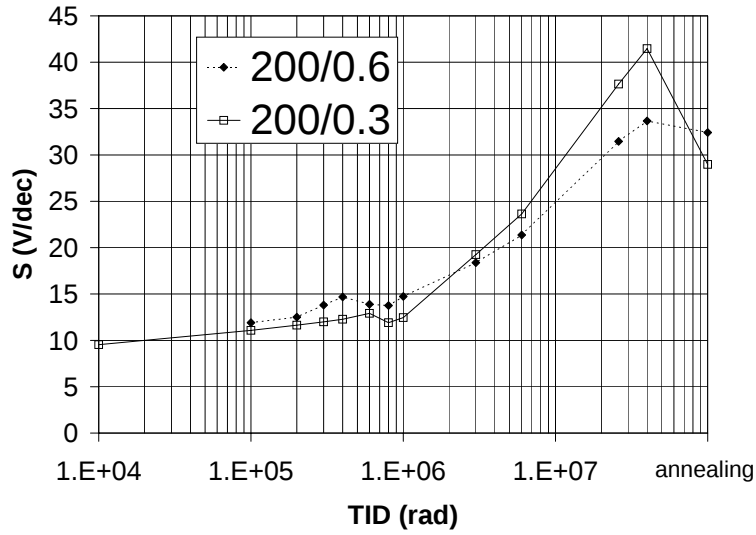


Figure 5.2: Subthreshold swing evolution with TID. The last point refers to annealing at room temperature for one week.

From our results we can see that with a 1.5V bias on gate, the maximum

value of the leakage between n-well and n+ diffusion would be of a few 10^{-6} A (at a TID of 3Mrad) for a distance of $0.3\mu\text{m}$ and of a few nA (at a TID of 40Mrad) for a distance of $0.6\mu\text{m}$ (Figure 5.1). Hence, the leakage current of a inverter, in normal working conditions (i.e. with 1.5V applied to the common gate), will decrease of about 3 orders of magnitude doubling the distance between n-well and n+ diffusion.

What we can conclude is that, although the leakage current is small at the minimum distance allowed by the design rules (i.e. $0.3\mu\text{m}$) and without a guard ring, it is safer to double the distance between the n-well and the n+ diffusion since in this way the leakage can still be considerably reduced. Unfortunately this solution, as well as the use of a guard ring, implies a waste of area.

Since the waste of area is a problem of major concern in digital design, some digital cells were integrated to directly measure the leakage current between n-well and n+ diffusion at minimum distance in a real design. This will drive the conclusion on the approach to use.

As already mentioned in 2.1, the available configurations of digital cells were three: without guard ring, with partial guard ring and with full guard ring (Figure 2.3). In all cases we measured their leakage current, that is the current flowing between V_{dd} (i.e. the n-well) and the grounded diffusions of NMOS transistors, for two different clock signals (see 2.5). The results are shown in figure 5.3, where the leakage current for a V_{dd} of 1.5V is plotted as a function of the dose for the three available configurations of digital cells.

We can observe that in the digital cell without guard ring the leakage current increases by two orders of magnitude, peaking around 10^{-5} A for a TID of 3Mrad. On the contrary the use of a guard ring effectively cuts the leakage path since no current increase is measured with dose.

However, the most interesting observation is that there is no significant difference between the configuration with partial guard ring and the one with full guard ring, the current is around a few 10^{-7} A in both cases. This result is of particular importance since the use of a partial guard ring does not imply a significant waste of area.

Hence, we can conclude that the best solution to cut the leakage path between n-wells and n+ diffusions at different potentials is to use a partial guard ring.

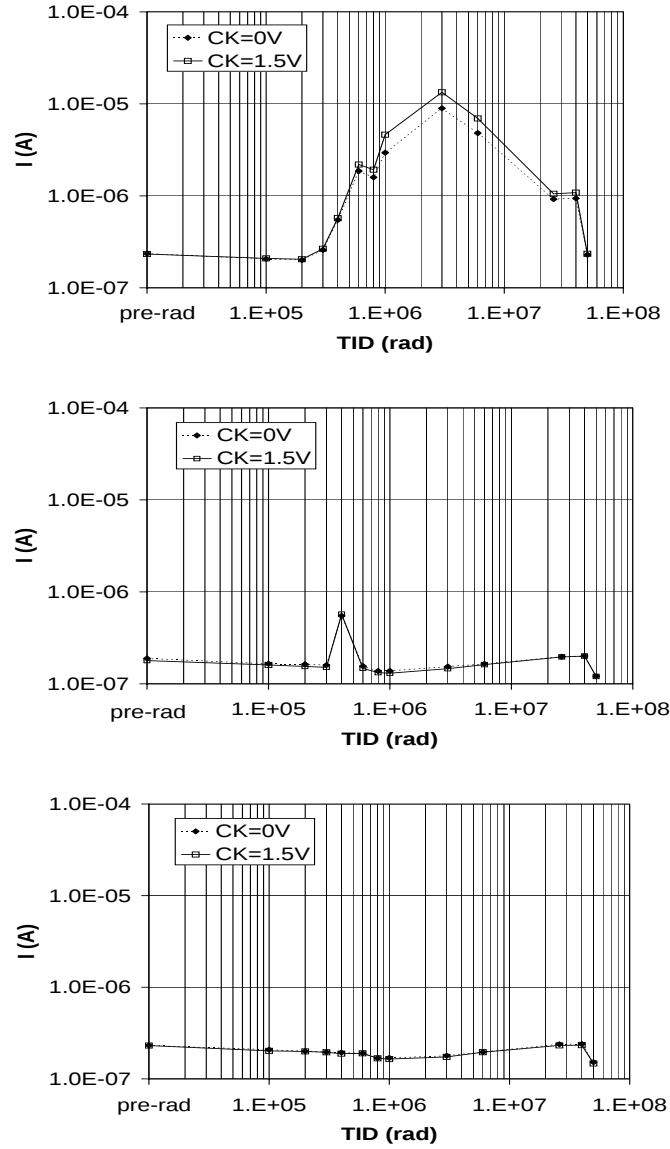


Figure 5.3: Evolution of the leakage current with TID for $V_{dd}=1.5V$ for the three configurations of digital cells: without guard ring (top), with partial guard ring (middle) and with full guard ring (bottom).

5.2 FOXFETs with n+ diffusions as source and drain

A FOXFET with n+ diffusions as source and drain has been designed to study the leakage between sources and/or drains of NMOS transistors at

different potentials. In particular, to picture the worst case, the gate is made in the first metal level (interconnection lines of polysilicon in this case are anyway very rare), hence the closest to the field oxide (i.e. strongest electric field across the STI), its length is the minimum allowed distance between diffusions and it is biased at 2.5V during irradiation, instead of 1.5V as in a real situation.

For this configuration there is no current flowing until the TID reaches 3Mrad, as we can observe from figure 5.4, when it becomes possible to see part of the subthreshold slope of the I_{ds} vs V_{gs} curve of the device. From this dose on, the effect of radiation is mainly a decrease of the subthreshold slope of the curve which leads to an increase of the leakage current. At a dose of 65Mrad the current reaches a value around a few nA in all the measured V_{gs} values, before starting to decrease because of the annealing. This has been performed in two steps: first a two weeks annealing at room temperature with the chip unbiased, which has reduced the current of one order of magnitude in all the voltage range, then isochronal annealing from 40 to 300°C in steps of 20°C, which has brought the curve back to the pre-rad value after the step at 160°C.

Since, as explained earlier, our FOXFET simulates the worse case, we can conclude that the leakage between n+ diffusions at different potential can be neglected in most practical cases.

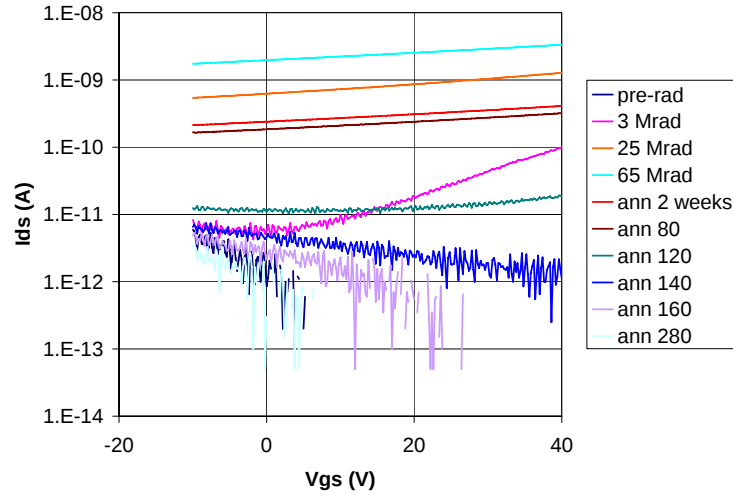


Figure 5.4: I_{ds} vs V_{gs} curve in saturation for different TID and after annealing for a FOXFET with n+ diffusion as source and drain ($W/L=200/0.18$).

5.3 FOXFETs with n-wells as source and drain

Leakage between n-wells is not a frequent case in CMOS ICs. In digital design all the n-wells are at V_{dd} , whilst in analog design, where there are usually a few n-wells at different potentials, guard rings can be used to cut the leakage. In this case in fact this solution has usually no relevant impact in terms of area since in analog applications the maximum available density is rarely needed.

The curves we measured were anyway useful to make a deep study of the radiation effects in the STI. Opposite to the other two FOXFET configurations, which did not allow to measure the I_{ds} versus V_{gs} curve after all the irradiation and annealing steps, in this case it was possible to extract from all the curves the threshold voltage and subthreshold swing values. As already mentioned in chapter 2, these are fundamental parameters for the extraction of the charge trapping and de-trapping characteristics.

Hereafter we will discuss the results obtained on the FOXFET with aspect ratio 200/0.92.

From each measurement point during irradiation it was possible to extract the relative contribution to the threshold voltage shift of interface states and oxide trapped charge, with the method presented in 1.1.3. The results are shown in figure 5.5.

The total ΔV_{th} has a behavior qualitatively similar to what we observed for the leakage current of linear-layout transistors and for the threshold voltage shift of narrow transistors: the degradation peaks at doses around 3Mrad. This proves that FOXFETs can effectively be used to study the leakage current behavior of linear transistors and that both the peak in the leakage of linear transistors and the rebound in the threshold voltage shift for narrow transistors is due to the balance of interface states and oxide trapped charge in the STI oxide. From figure 5.5 we can in fact observe that the trapped charge dominates at first, whilst interface states start to play a role after a few Mrad.

The relative dominance of the oxide trapped charge in the early stage of irradiation is also shown in figure 5.6, where the generation rate¹ of interface states and oxide trapped charge is plotted as a function of the TID. We can

¹What we call here generation rate is actually a quantity proportional to the effective generation rate. It has in fact simply been calculated for interface states (oxide trapped charge) as the ratio between the ΔV_{it} (ΔV_{ox}) and the ΔTID for each irradiation step, not as the increase of the number of traps per unit dose, $\Delta N_{it}/\Delta TID$ ($\Delta N_{ox}/\Delta TID$). The two quantities are anyway proportional: $\Delta N_{it} = \Delta V_{it} C_{ox}/q$ ($\Delta N_{ox} = \Delta V_{ox} C_{ox}/q$).

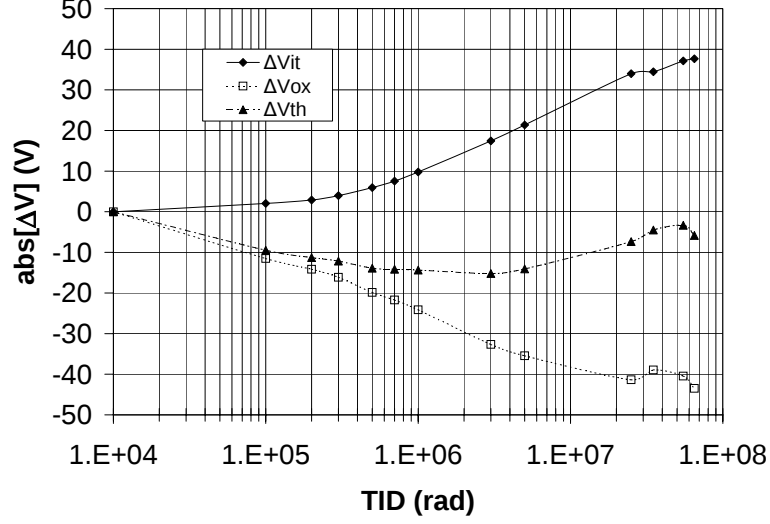


Figure 5.5: Evolution with TID of the threshold voltage shift (ΔV_{th}) and contributions from the oxide trapped charge (ΔV_{ox}) and interface states (ΔV_{it}).

observe that for TID below 1Mrad the generation rate of oxide trapped charge is higher than the one of interface states, consistently with the known later evolution of the latter. It is anyway interesting to note that both interface states and oxide trapped charge are generated mainly in the early irradiation stages and that the generation rate decreases with TID for both of them. We believe this might be due to some saturation phenomenon of the traps, both oxide and interface state traps. According to the extracted energy levels of the traps from the isochronal annealing (see 2.4) in fact this decrease cannot be due to annealing of the traps created in the early irradiation stages².

The decrease of the generation rate of interface states can also be seen looking at the derivative of the subthreshold swing S as a function of the TID (Figure 5.7): the maximum change occurs at the beginning of the irradiation and constantly decreases after. This has been observed also with a negative bias applied on the gate (-2.5V) during irradiation (Figure 5.7). In this case in fact, as well as the positive bias case, there is interface states built-up.

This can be seen in figure 5.8, where the I_{ds} versus V_{gs} curve in the nega-

²The total time for the irradiation was around 2 days and from the energy levels of the traps extracted from the isochronal annealing only a minor fraction of the charge is annealed at room temperature at this time.

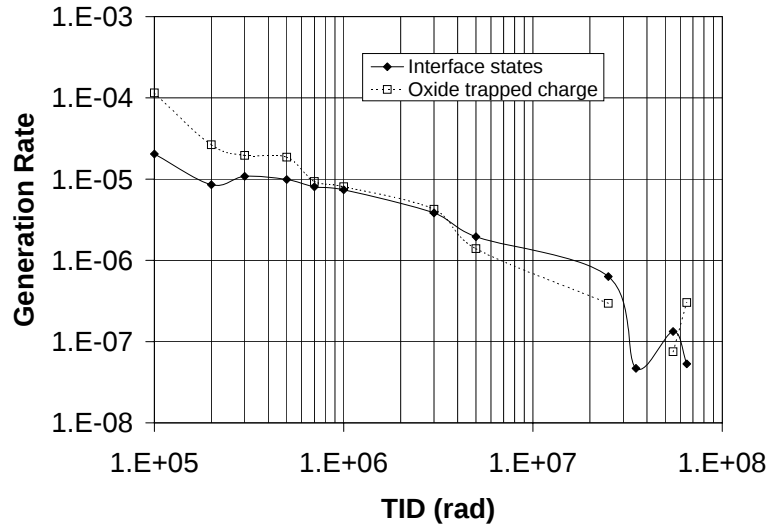


Figure 5.6: Generation rate per dose unit of oxide trapped charge and interface states as a function of the dose.

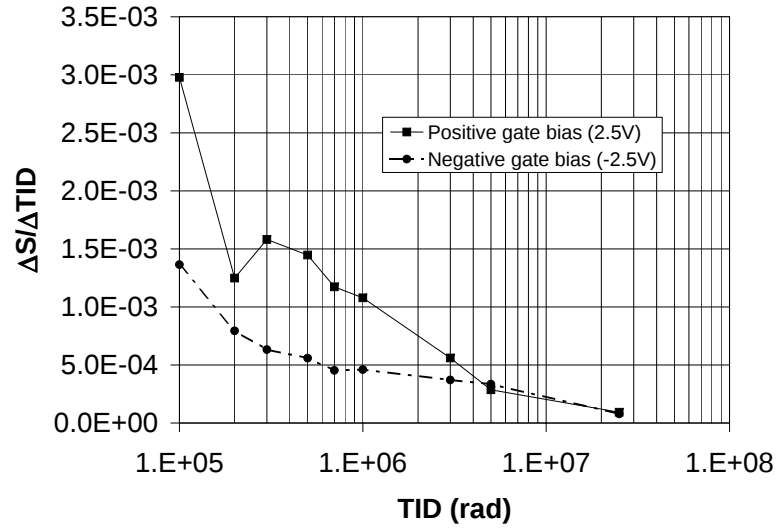


Figure 5.7: Differential swing change ($\Delta S/\Delta TID$) versus TID for positive (+2.5V) and negative (-2.5V) bias applied to the gate.

tive bias case is shown: the slope of the curve changes with TID. According to what is predicted by the WML and $(HH)^2$ models (see 1.1.2) anyway, the interface states built-up with a negative bias applied on the gate is smaller than in the case of positive gate bias. This can be seen clearly in figure 5.9: the values of S are smaller for a negative potential applied on the gate.

Concerning the oxide trapped charge, as expected, contrary to the experiments with positive bias, the curve does not shift to lower V_{gs} . This is consistent with little or no trapping of positive charges in the oxide close to the SiO_2 -Si interface because of the negative bias.

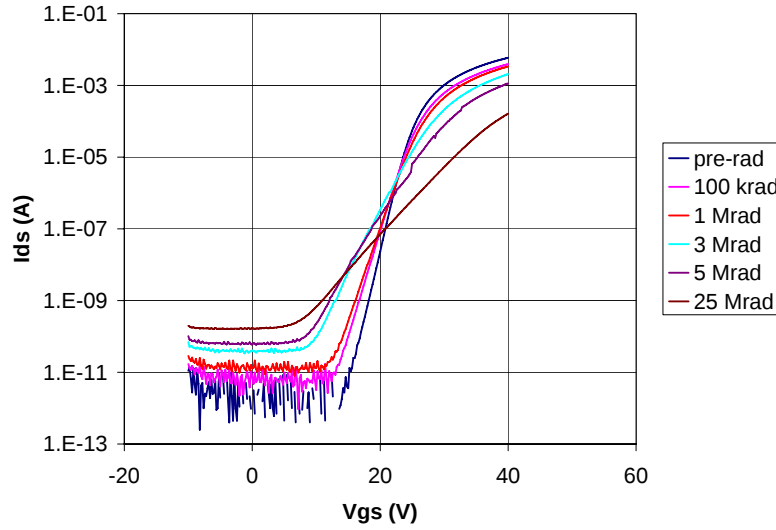


Figure 5.8: I_{ds} versus V_{gs} curve for different irradiation steps for the negative gate bias case (-2.5V).

The results of the isochronal annealing are particularly interesting because they show, contrary to what is known, that interface states anneal at low temperatures ($80\text{-}100^\circ\text{C}$) and part of the oxide trapped charge does not anneal even after isochronal annealing at 300°C . This can be observed in figures 5.10.

As expected, for temperatures below 355K (80°C), the oxide trapped charge starts to anneal whilst interface states seem to get created instead of annealed. The latter start to anneal at temperatures around $80\text{-}100^\circ\text{C}$, although slower than the oxide trapped charge.

This can be observed in figure 5.11, where we show the results of an

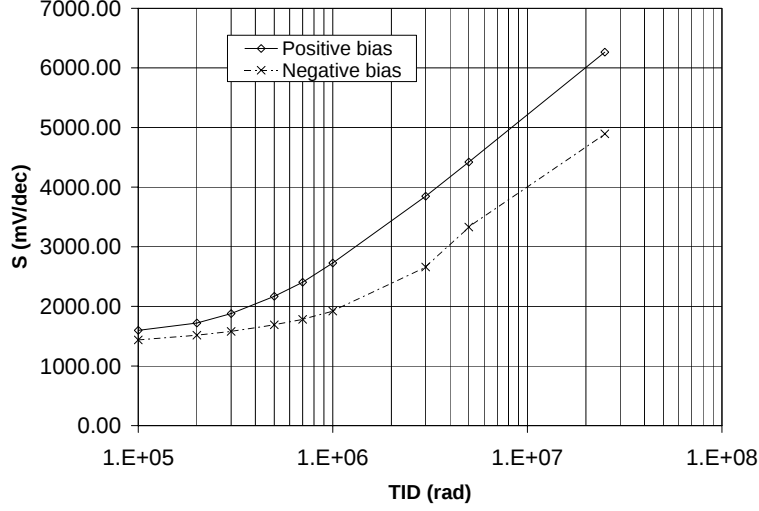


Figure 5.9: *Subthreshold swing measured during irradiation with positive and negative bias applied to the gate.*

experiment made according to the following procedure: irradiation and annealing steps were performed cyclically and measurements were performed after each irradiation and annealing step. Initial irradiation steps of 1-2Mrad were used, then increased to eventually reach a TID of 100Mrad. Annealing³ steps were performed at a temperature of 80°C for a few hours (4-72, but typically about 16 hours).

In figure 5.11 the first point refers to the measurement before irradiation. The successive points refer alternatively to the values of ΔV_{it} and ΔV_{ox} after an irradiation step and after an annealing step.

We can observe that after each annealing step the value of V_{ox} goes back to 10-15V, whilst the value of V_{it} tends to increase with successive annealing step, meaning an accumulation of interface states after each irradiation-annealing cycle. From this we can deduce that the annealing of interface states at 80°C is less important than for the oxide trapped charge.

The same experiment was also performed with an annealing temperature of 100°C. In this case we observed that the annealing of interface states was closer to the one of the oxide trapped charge.

³This was the only case in which the chip was biased during annealing. The FOXFETs were biased as during irradiation, hence with a potential 2.5V on the gate and all the other terminals at ground.

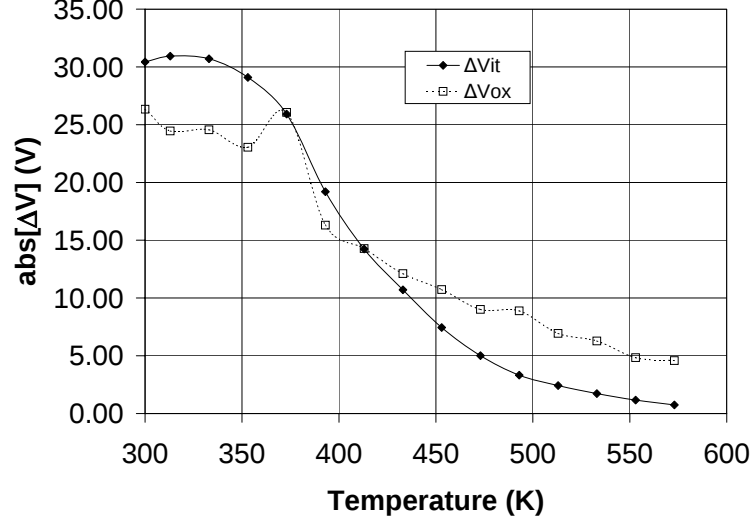


Figure 5.10: *Evolution of the two contributions to ΔV_{th} as a function of the temperature of the isochronal annealing steps. The points at 300K are the ΔV_{it} and ΔV_{ox} after irradiation at 65Mrad and 2 weeks annealing at room temperature with the chip unbiased.*

This is in agreement with what we can see in figure 5.10: from temperatures of 100°C to 160°C, the annealing of oxide trapped charge and interface states are very closely similar. For higher temperatures interface states anneal more and after the last isochronal step, they are completely annealed, whilst a fraction of the oxide trapped charge is still un-annealed. As we can see from figure 5.12, at the end of annealing the 20% of the oxide trapped charge is still un-annealed⁴.

Isochronal annealing has been performed also on the chip irradiated with a negative bias applied on the gate. The results were similar to those obtained with the positive bias, a part from the fact that, in this case, the oxide trapped charge anneals completely at 300°C.

To summarize, from these experiments we can say that for both positive and negative gate bias interface states are mainly generated at the beginning of the irradiation. The generation rate then decreases, but it is possible to see interface states built-up during all the irradiation and after the first

⁴The un-annealed fraction of oxide trapped charge and interface states have been calculated as explained in 2.4.

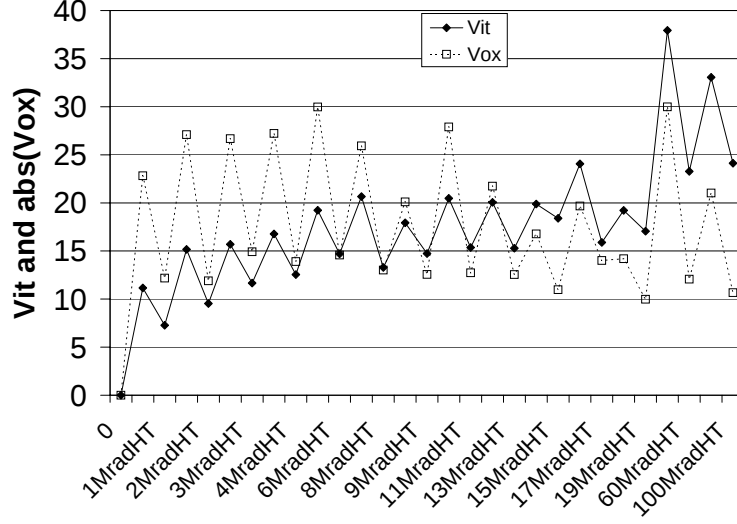


Figure 5.11: Evolution of the threshold voltage shift components due to interface states, V_{it} , and oxide trapped charge, V_{ox} , after irradiation and annealing steps.

isochronal annealing steps. At temperatures around 80-100°C interface states start to anneal and after the last isochronal annealing step at 300°C the annealing of interface states is complete. Concerning oxide trapped charge, we observed that, as for interface states, the generation rates decreases with TID. As expected they are not generated with negative bias applied to the gate, they start to anneal at temperatures around 40-60°C, but they are not completely annealed at a temperature of 300°C in the case of positive potential applied to the gate.

In all the above experiments the dose rate used for irradiation was about 400rad/sec. One low dose rate (LDR) experiment was performed as well. In this case the irradiation, made with a ^{60}Co source, was performed at a dose rate of 1rad/sec. A TID of 3.2Mrad was reached after 5 weeks. The FOXFET was measured before and at the end of the irradiation.

The results are shown in figure 5.13, where the measured ΔV_{th} decomposed in contributions from ΔV_{it} and ΔV_{ox} has been superposed to the same measurement performed with X-rays at high dose rate (HDR).

We can observe that the ΔV_{th} at LDR is smaller than at HDR. This was expected especially on the ground of the activation energy of the charge trapped in both the oxide and interface states: of the charge trapped at

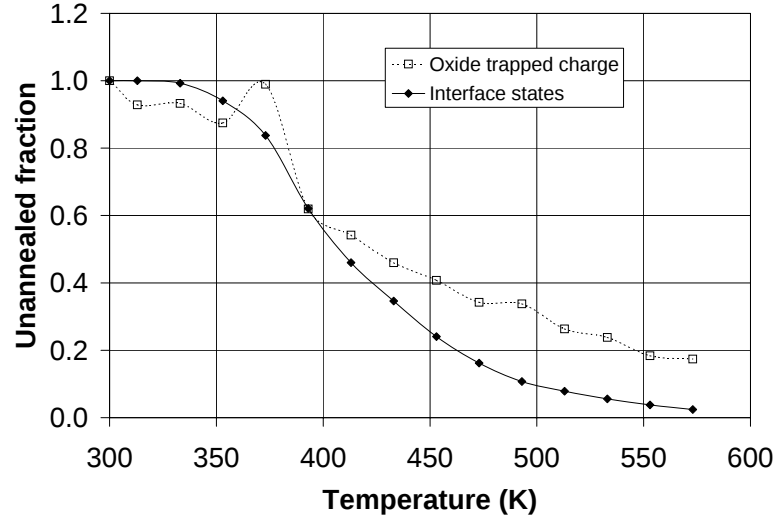


Figure 5.12: *Un-annealed fraction of oxide trapped charge and interface states as a function of the temperature.*

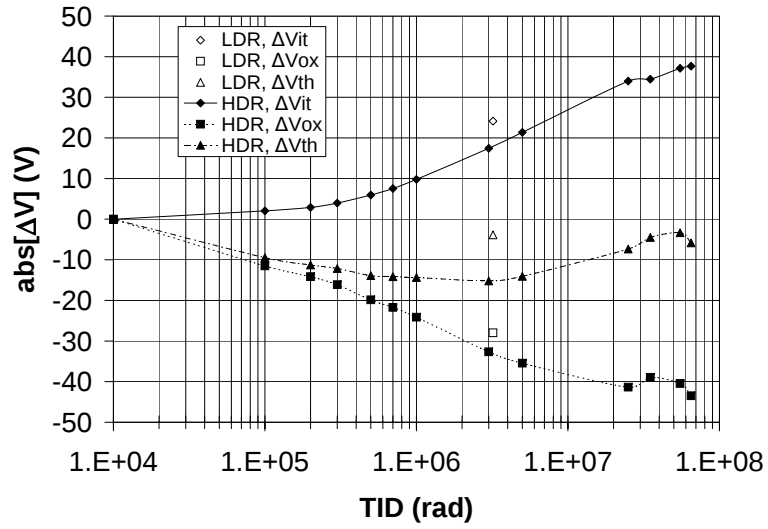


Figure 5.13: *Results of LDR and HDR irradiations on FOXFETs.*

the beginning of the irradiation, we estimate that only about 20-30% is still

trapped after 5 weeks at the end of the irradiation. This confirms also that the leakage current observed in standard transistors at HDR is a pessimistic estimate of the damage in real applications.

As expected from the annealing prediction the ΔV_{ox} is smaller at LDR.

A problem in the interpretation arises for the ΔV_{it} . In this case the contribution seems to be larger at LDR than at HDR. From the isochronal annealing tests and consequent extraction of the activation energy of the interface states, we would also expect a large fraction of them to anneal during the LDR irradiation.

Different hypothesis have been made. First, this can be due to a real “latent” built-up of interface states, but, if that was the case, then it should be more than compensated by the annealing. We can think about a difference in the effect of ^{60}Co gammas and X-rays (it is known that the fractional yield is different at low electric fields) but this should be the same for both interface states and oxide trapped charge. The only possible explanation up to now is a different creation of interface states at different dose rates. This would be a real LDR effect as observed in bipolar transistors. This possibility has still to be verified.

Conclusions

The work carried out in this thesis is the study of the TID tolerance of 130nm CMOS technologies from three different manufacturers. The aim of the work was to assess their radiation tolerance, in order to predict the behavior of integrated circuits manufactured in such technologies in the radiation environment typical of HEP experiments and evaluate whether HBD techniques should be used or not in the design of ASICs for the LHC experiments. The answer to such question is relevant since the use of HBD for digital design requires the development of a custom digital library, the cost of which is large in terms of manpower and time. We remind that HBD techniques based on the systematic use of enclosed layout transistors and guard rings have been common in ASICs for the LHC in a quarter micron CMOS technology.

The study has been done on MOSFETs, both core and I/O, linear and enclosed and on isolation test structures (here called FOXFETs).

Core linear transistors are affected by radiation-induced edge effects common to deep submicron technologies. The thin gate oxide is in fact practically immune from radiation, as shown by the results on ELTs whose characteristics do not change with TID, whilst the lateral isolation (STI) is still source of problems for applications in radiation environments. The charge balance between oxide trapped charge and interface states at the transistor's edge influences the main transistor's characteristics: for both leakage current and threshold voltage shift in the case of narrow transistors (RINCE), a peak is observed for a TID of a few Mrad. RINCE, negligible in PMOS transistors, increases its importance in narrower NMOS transistors, leading to a V_{th} shift around 60-160mV, depending on the fabrication process. Peaks in the leakage current around fractions to few μA , depending on the technology, have been measured in n-channel MOSFETs.

Radiation effects on the lateral isolation contribute to increased inter-device leakage as well. Such leakage typically flows between adjacent NMOS transistors and in digital cells between n+diffusions and n-wells. In the studied technologies, the value of the leakage current measured between NMOS, through the use of particular transistors called FOXFETs with n+ diffusions

as source and drain, is very small being of the order of few nA. Leakage current values around a fraction of μA have been measured between n+diffusions and n-wells. In both cases there was no guard ring and the n+ diffusions and n-wells were at minimum distance.

Nevertheless the observed leakage current both at device and inter-device level is a few orders of magnitude smaller than in older generations of the technology. This is clear from the results on I/O transistors whose gate oxide thickness and dimensions are typical of a $0.25\mu\text{m}$ CMOS process. They are in fact considerably more damaged by TID showing a higher leakage current and a larger threshold voltage shift, not only on narrow transistors. Even enclosed transistors can have considerable radiation-induced threshold voltage shifts.

Moreover, the results just discussed have been obtained from experiments in which a high dose rate was used and the transistors were kept in the worst case bias, hence they represent the worst case. We are confident that in real applications, hence with a low dose rate and different bias, the above mentioned degradations will be considerably smaller. This was proved for one of the tested technologies by the time-temperature evolution of the charge at the transistor's edge (obtained with isochronal annealing tests) and the low dose rate test.

For these reasons, we think that circuits designed with commercial 130nm CMOS technologies have the potential of standing Multi-Mrad radiation levels and as a consequence HBD techniques such as ELTs and guard rings, can in principle be avoided.

We would in fact suggest to use them in digital circuits very sensitive in term of timing, where the threshold voltage shift can cause problems and in analog circuits where transistors work in weak inversion, since this is the region where radiation effects manifest themselves mostly. For digital circuits, if needed the leakage current can be decreased with the use of a partial guard ring a solution which has proved to be very effective with a negligible cost in terms of area. Last but not least particular attention has to be taken in the design of the periphery of the circuit in case I/O transistors are used. ELTs can be used to cut the leakage paths but the designer should remember that for I/O transistors also edgeless transistors will show considerable threshold voltage shifts and evaluate carefully the impact of this effect on the I/O circuitry.

One more consideration needs to be done. In case the choice is to rely on the natural radiation tolerance of the technology, this will have to be constantly monitored during the full manufacturing life of the circuit because changing in the process might result in a different radiation response.

Concerning the future of the technology, if the fabrication process will not dramatically change (introduction of high K dielectrics, multiple-gate transistors on SOI, etc.) we would expect that good radiation tolerance can be maintained. With thinner gate oxides (still SiO₂) radiation effects should not affect the performance. The STI oxide should instead not change considerably hence the behavior of the parasitics at the transistor's edges should be comparable. In fact, RINCE could even become more important in newer technology generations with smaller feature sizes.

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