

**Simulation and Hardware Development
of the Liquid-Argon Calorimeters Phase-II Read-out Path
of the ATLAS Detector**

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Abstract

The LHC is upgraded in two phases up until the year 2027 to increase its luminosity. This requires an improved trigger of the ATLAS detector to suppress pileup background. Therefore, the readout electronics of the LAr calorimeter including the digital signal processing are upgraded. The digital signal processing is implemented in FPGAs, which are programmed with firmware. Improvements in the firmware need to be planned, developed and tested. This thesis presents the improvement of the readout simulation software AREUS for gain selection analysis and baseline shift studies for the Phase-2 upgrade. A gain selection in the front-end reduces the cost, but introduces gain mixing effects. It could be shown, that one gain is sufficient for the determination of the baseline.

In the Phase-2 LASP FPGA, firmware developments were conducted. A finite impulse response filter was installed by chaining several digital signal processor modules together. The filter is used to reduce electronic and pileup noise contributions. Multiplexing capabilities were added to use the same hardware blocks for multiple channels. In addition, a new selection and packing algorithm was developed to prepare data for a new trigger processor. A fast data transmission was tested and 27 Gigabits per seconds were achieved. The firmware development, described in this thesis, corresponds to central features of the digital processing systems of the Phase-1 and Phase-2 upgrade. This will improve the trigger capabilities of the ATLAS detector and aid in the discovery of possible new phenomena.

Kurzdarstellung

Der LHC wird in zwei Schritten bis 2027 aufgerüstet, um eine höhere Luminosität zu erreichen. Dies erfordert einen verbesserten Trigger des ATLAS Detektors für die Unterdrückung von Pile-Up-Untergrund. Deswegen wird die Auslese Elektronik des LAr Kalorimeters, einschließlich der digitalen Signalverarbeitung, ausgebaut. Die digitale Signalverarbeitung ist auf FPGAs implementiert, die mit Hilfe von Firmware programmiert wird. Verbesserungen an der Firmware müssen geplant, entwickelt und getestet werden. Diese Doktorarbeit erläutert die Verbesserung des Auslese Simulation Programs AREUS für Phase-2 Studien. Diese betreffen die Position der Signalauswahl mit mehreren Verstärkerstufen und die Verschiebung der Nulllinie. Eine Auswahl in der Nähe des Detektors würde die Kosten reduzieren, aber auch verschiedene Verstärkerstufen vermengen. Es konnte gezeigt werden, dass zur Bestimmung der Nulllinie eine Verstärkerstufe ausreicht.

Die Entwicklungen am Phase-2 LAr FPGA sind ebenfalls beschrieben. Ein Filter mit endlicher Impulsantwort wurde mithilfe verbundener digitaler Signalprozessor Modulen installiert. Der Filter wird verwendet um elektronisches und Pile-Up Rauschen zu unterdrücken. Die Multiplexeigenschaft wurde hinzugefügt um dieselben Hardwareblöcke für mehrere Kanäle zu verwenden. Außerdem wurden ein neuer Selektions- und Komprimierungsalgorithmus entwickelt um Daten für einen neuen Trigger Prozessor vorzubereiten. Eine schnelle Datenübertragung wurde getestet und 27 Gigabits pro Sekunde wurden erreicht. Die in dieser Doktorarbeit beschriebene Firmware-Entwicklung beinhaltet essenzielle Features der Digitalverarbeitung Systeme der Phase-1 und Phase-2 Verbesserung. Dies wird die Trigger Fähigkeit verbessern und bei der Entdeckung von möglichen neuen Phänomenen helfen.

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Chapter 1

Introduction

Particle physics looks into the fundamental laws of nature, and is necessary to describe physics phenomena like the evolution of the universe. The numerous Nobel prizes awarded in this area demonstrate the many tremendous achievements. The findings were used to develop quantum field theories like the Standard Model [1–14]. All model predictions are tested in many precision experiments.

Despite these successes, there are still some gaps in our knowledge. The matter-antimatter asymmetry observed in the universe cannot be fully explained at the moment [15]. The fourth fundamental interaction, gravitation, is not included in the Standard Model [16]. A huge mystery is dark matter and dark energy, which make up 95 % of the universe [17]. The Standard Model, its successes and challenges are described in chapter 2.

To fill these gaps and to come closer to an answer of the introductory question, dedicated experiments are built. A very successful method is the acceleration and collision of particles, resulting in high energy concentrated in a very small space. These are conditions, which are similar to those at the beginning of the universe. Many experiments try to increase the delivered energy because this brings the conditions time-wise closer to the so-called big bang, which is assumed to be the very beginning for our universe. At the moment, the Large Hadron Collider (LHC) [18] achieves the highest particle collision energies, using protons accelerated in a nearly circular machine.

In high energy proton–proton (pp) collisions, the intermediate states and particles usually have a very short lifetime so that only final state products of the particle reactions can be detected. The ATLAS [19] experiment is one of the detectors installed at the LHC. It consists of several layers with different functions. In this thesis, the focus is set on the Liquid-Argon (LAr) calorimeter, which measures the energy of particles. The setup of LHC, ATLAS, the LAr calorimeter and their readout are explained in chapter 3.

With the LHC and the ATLAS experiment important physics measurements have

already been made, including the discovery of a Standard Model like Higgs boson [20]. However, advancing technology enables the accelerator to operate at higher instantaneous luminosities and the detector at higher efficiencies. Therefore, a multiple-phase upgrade plan was developed [21]. The main objective is the increase of the number of collisions produced by the LHC because many interesting processes occur only very rarely. In turn, the trigger capacities of the detectors need to be enhanced to distinguish between these interesting events and background. The upgrade plan is described in chapter 4.

The readout of the LAr calorimeters is also affected by the changes. Chapter 5 explains the design and the simulation of the new readout path. Different studies, which helped to take design-related decisions, are also addressed. Special hardware, which handles multiple readout channels at high bandwidth, is needed to implement the new readout. An introduction to the dedicated hardware components is given in chapter 6. There are two specific electronic boards, to which the work of this thesis has contributed. Their purpose and design are described in chapter 7 and chapter 8.

Chapter 2

Physics Motivation

2.1 The Standard Model of Particle Physics

The Standard Model (SM) [1–14] is one of the most important and acknowledged theories. It combines the majority of known principles in particle physics and explains most experimental results in particle physics. This chapter contains a short overview of the SM. More information about this topic is given in [22].

2.1.1 Elementary Particles

Elementary particles have no known substructure and are considered point-like. The SM describes a wide range of phenomena, which make up all visible matter in the universe. Elementary particles can be divided into several classes with different properties and behavior. The main classification is into fermions and bosons. This refers to the wave functions for identical particles. Fermions must be asymmetric under the interchange of two particles, which leads to the Pauli exclusion principle [23]. Two identical fermions cannot occupy the same quantum state. This results in the formation of stable bound states and the construction of matter. They also have half-integer spin according to the spin-statistics theorem [24].

The fundamental fermions can be divided into leptons and quarks. They can also be separated into three generations of matter. All leptons carry a weak charge but only three of the six have an electric charge. The remaining three are called neutrinos and are considered massless in the original SM. All six quarks have weak, electric, and an additional color charge. Some of their properties can be seen in table 2.1. Each of these particles has a partner, the so called antimatter. They have the same mass, but opposite charges. It is not possible to detect free quarks, which is called color confinement. It states, that quarks can only exist in the form of colorless combinations. At low energies, quarks are confined in hadrons composed of two or three quarks. The latter are called baryons with known examples like the proton, which consists of two up and one down valence quarks, and the neutron holding two down and one up valence quark. Mesons

are bound states of a quark and an antiquark.

	1	Generation 2	3	Electrical charge	Color charge
Quarks	up (2.2)	charm (1280)	top (173100)	+2/3	red, blue, green
	down (4.7)	strange (96)	bottom (4180)	-1/3	
Leptons	electron (e) (0.511)	muon (μ) (105.66)	tau (τ) (1776.8)	-1	none
	e-neutrino ($< 10^{-6}$)	μ -neutrino (< 0.17)	τ -neutrino (< 18.2)	0	

Table 2.1: Overview of the different generations of fermions and their properties with their approximate mass in MeV in the parentheses

Boson wave functions are symmetric after the interchange of two identical particles, which leads to bosons having an integer spin. The Pauli principle does not apply to them, and they can all occupy the same ground state. There are four electroweak and eight strongly interacting gauge bosons, which function as force carriers and mediate three of the four fundamental interactions. The most commonly known boson is the massless photon. It is the mediator for the electromagnetic force and can interact with every particle carrying an electric charge. Since the photon has no charge, it cannot couple directly with itself. Other massless bosons are the eight gluons [6–9], which are a force carrier for the strong interaction. They couple with every particle holding a color charge including the gluons themselves. The other three gauge bosons are massive and mediate the weak interaction. There are two charged $W^\pm$ bosons and the neutral Z boson. Since they all have a spin of 1, they are also called vector bosons. The last fundamental particle is the Higgs boson [10–14]. This massive and neutral particle has a spin of 0, which makes it a scalar boson. Its function within the SM is described in section 2.1.3. An overview of the bosons is shown in table 2.2.

2.1.2 Symmetry Groups

The SM is a collection of Quantum Field Theories (QFTs). A good starting point for the construction of QFTs are symmetries. A symmetry is an operation performed on a system, that leaves it invariant. In addition, the Noether’s theorem [25] proves that symmetries are associated with conservation laws. As an example, the translational invariance in time is connected with the conservation of energy.

A set of all symmetry operations on a particular system has the same properties as a mathematical group. These can in turn be described as groups of matrices. The most

	Force	Elektromagnetic Charge	Mass	Spin
photon (γ)	electromagnetic	0	0	1
gluon (g)	strong	0	0	1
Z	weak	0	91.19	1
$W^\pm$		± 1	80.39	1
Higgs (H)		0	124.97	0

Table 2.2: Overview of the different bosons and their properties with their approximate mass in GeV

common one in particle physics is $U(n)$. It is the collection of all unitary $n \times n$ matrices. If in addition the determinant of each matrix is 1, the group is called $SU(n)$.

The framework for the SM is formed by the set of symmetry groups $SU(3) \times SU(2) \times U(1)$. The $SU(3)$ transformations generate the Quantum Chromodynamics (QCD) sector. It defines the strong interaction between quarks and gluons. Every quark can have one of the three color charges red, blue or green. The symmetry results in the requirement for the existence of eight different colored gluons.

The $SU(2) \times U(1)$ group generate the electroweak sector. The $SU(2)$ invariance requires three massless W bosons of weak isospin, T , while the $U(1)$ group generates one massless B boson of weak hypercharge, Y . The massive gauge bosons and the photon are linear combinations of the massless states and obtain mass by the Electroweak Symmetry Breaking (EWSB).

2.1.3 Spontaneous Symmetry Breaking

The symmetry breaking occurs because the vacuum or ground state of the system does not share the full symmetry of the system, usually described by a Lagrangian density. It is spontaneous, because no external mechanism drives the transition from the symmetric system to the broken ground state. Two of the massless W bosons combine to the massive $W^\pm$ bosons. The third massless W and the B boson unite to the Z boson and the photon via the weak mixing angle. The electric charge, Q , is given by the third component of the weak isospin and the hypercharge: $Q = \frac{Y}{2} + T_3$.

It is stated by the Goldstone's theorem [26], that spontaneous breaking of a continuous global symmetry is always accompanied by the appearance of new particles, the Goldstone bosons. Four of those would be generated, but three are absorbed by the weak interaction gauge bosons. In the Higgs mechanism the remaining Goldstone boson is the Higgs particle, which is also an excitation of the Higgs field. This field also gives mass to fermions via Yukawa couplings.

2.1.4 Achievements and Challenges

The SM successfully predicted several elementary particles before their detection. This includes the $W^\pm$ and Z bosons, which were discovered in 1983 [27, 28]. Another prediction was the top quark with its discovery in 1995 [29]. The final example is the Higgs boson, which was discovered in 2012 [20]. In addition, their properties were predicted and confirmed with high experimental precision.

In spite of its successes, the SM has also many important issues, that are not addressed. There are over 20 arbitrary parameters like the quark and lepton masses and the weak mixing angle. Their values are only measured in experiments, but cannot be explained or calculated from basic principles. In addition, the fourth fundamental interaction, gravitation, with the hypothetical graviton is not included [16]. Dark matter and dark energy represent over 95 percent of the universe, but are not included in the theory [17]. Neutrinos are considered massless in the classic SM. This contradicts the experimentally confirmed neutrino oscillation [30], which requires the neutrinos to have a mass. However, if neutrinos are pure Dirac particles, they can be easily integrated in the SM. Finally, the weak interactions cannot fully explain the matter-antimatter asymmetry in the universe [15].

2.1.5 Extensions of the Standard Model

Some of the above mentioned issues could be resolved by new theories. Since the SM has met most experimental tests, any new theory has to be an extension of it. The most popular ones are based on Supersymmetry (SUSY) [31]. SUSY would double the number of particle degrees of freedom, associating every boson to an additional fermion and vice versa. Since these particles have not been found yet, they must have a much higher mass or very small crosssection. The mass differences indicate that the supersymmetry must be broken. This huge number of new unexplained parameters stands against the following advantages of this theory. The lightest supersymmetric particle would be a good candidate for dark matter [32]. In addition, a QFT of gravity most likely requires supersymmetry. Finally, an extension to the SM would also make way for a Grand Unified Theory (GUT). This means, that at high energies electromagnetic, weak, and strong interaction are unified into a single force, similar to the electroweak interaction.

There are also theories, which go a step further. A Theory of Everything (TOE) would include all four fundamental forces. The most famous example is string theory, which proposes one dimensional strings as basic units of matter instead of zero dimensional particles [33]. This requires many extra dimensions and the first versions only contain bosons. Fermions are added via supersymmetry, which led to the name superstrings. The theories mentioned in this section have no experimental validations yet. It remains in the hands of future experiments to solve the problems of the current SM and to find evidence of the mentioned theories.

2.2 Proton Collider Physics

The theory provides predictions for parameters, which can be verified by experiments. An important parameter is the cross section, σ , which is the probability that a certain reaction occurs. By accelerating and colliding particles, and detecting the resulting products, the number of events N of a certain process can be counted for a time, t . The mean value is proportional to the cross section:

$$\frac{dN}{dt} = L \sigma. \quad (2.1)$$

The proportional factor is the luminosity L , which depends on the collider configuration. The integrated luminosity indicates how well a collider performed in a period of time, and is calculated by integration:

$$L_{\text{int}} = \int L dt. \quad (2.2)$$

This thesis covers the LHC, which accelerates and collides two proton beams. Because of their high mass, protons generate only a small amount of synchrotron radiation, . This results in a high center-of-mass energy, which is another important parameter in collider physics. A high center-of-mass energy is needed to increase the probability of the generation of new heavier particles. The value states the maximal possible energy, which is available in the collision. In head-on colliding beam experiments, it is calculated by the sum of the energy of the two particle beams. This pp center-of-mass energy cannot be fully utilized because the actual hard scattering takes place between the partons, the quarks and gluons, which only carry part of the proton impulse. The actual energy, which contributed to an interaction is not known a priori and cannot be measured in all reactions. To solve this problem, the fact is used, that the transverse momentum before the collision of the partons is approximately zero. The laws of conservation of energy and momentum dictate the same value afterwards and any net momentum indicates missing transverse energy, because not all particles can be detected.

A huge number of events are minimum bias, which is a specific classification of pp collision events. They achieve only the minimal trigger thresholds of the detector and are dominated by inelastic pp collisions with low p_T interactions. These are typically considered background. Figure 2.1 displays several of the production cross sections in theory and experimental measurements at the LHC. Many of the interesting reactions have a very small cross section. The luminosity needs to be increased as much as possible to enable sufficiently large number of signal events to be measured. Therefore, the High Luminosity LHC (HL-LHC) project was established, which is an upgrade plan for the

LHC with the aim to increase its luminosity. This will, for example, result in the production of 15 million Higgs bosons per year instead of the three million at the LHC in 2017 [34].

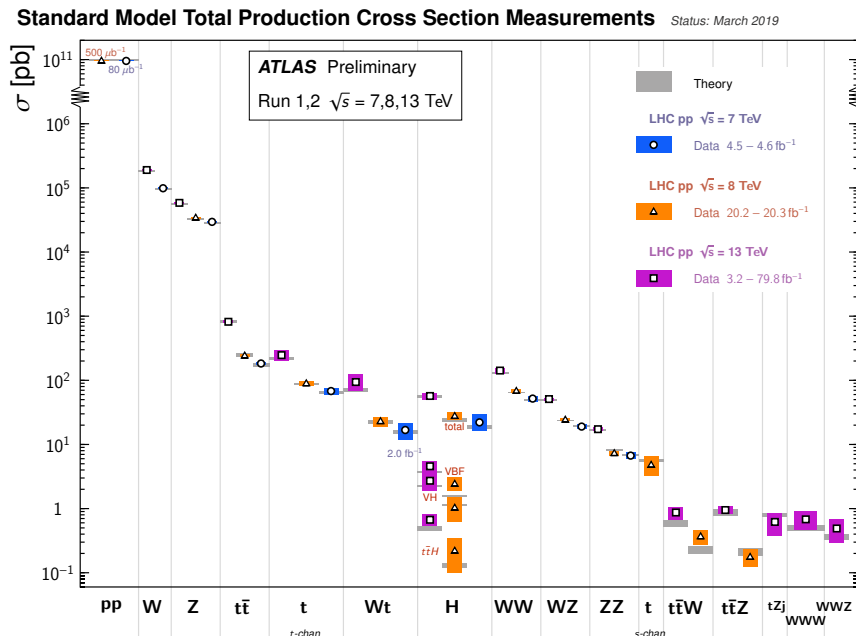


Figure 2.1: Cross-sections of Standard Model processes measured by the ATLAS Collaboration compared to theoretical predictions [35]. Good agreement is observed.

2.3 Physics prospects of a High-Luminosity Large Hadron Collider

The increased production rate enables an in-depth study of the Higgs and its decay channels. One important example is the decay into two photons. Figure 2.2 displays the reconstructed diphoton invariant mass obtained in the LHC data taking period 2015-2018 (LHC Run 2), and different simulations settings for the HL-LHC. A comparison between two curves with different numbers of interactions per collision, μ , shows the degradation of the mass resolution at higher luminosity. With an optimistic photon resolution scenario, the resolution can still be slightly better than Run 2. An excellent photon energy reconstruction is therefore needed during HL-LHC operation of the particle detectors. This will be achieved by an improved calorimeter system, in particular by new readout electronics with an improved signal treatment adapted to the high luminosity conditions.

One of the most promising channels to study Higgs self-coupling, $H \rightarrow HH$, is the final state of a bottom quark pair and two photons. Figure 2.3 shows the diphoton

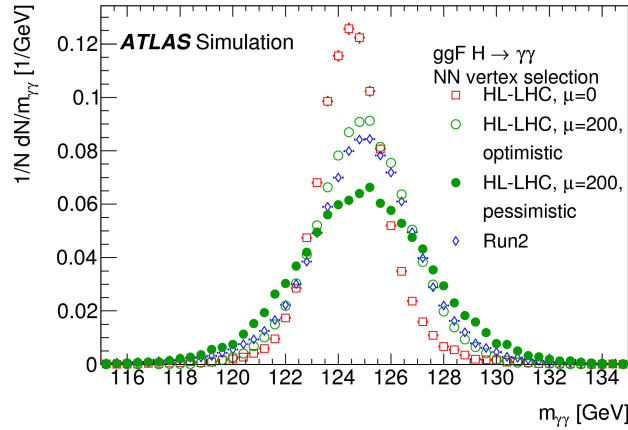


Figure 2.2: Diphoton invariant mass [36]. Data from Run 2 is compared with several simulation settings for the high luminosity LHC, including optimistic and pessimistic photon resolution scenarios. μ is the mean number of interactions per collision.

invariant mass distribution after applying most selection cuts. The diphoton invariant mass cut window could be reduced with a narrower mass peak. This would reduce the expected number of events from the continuum background by a factor of 1.4 [36]. Again, the diphoton mass reconstruction requires a very good performance of the electromagnetic calorimeter under HL-LHC conditions.

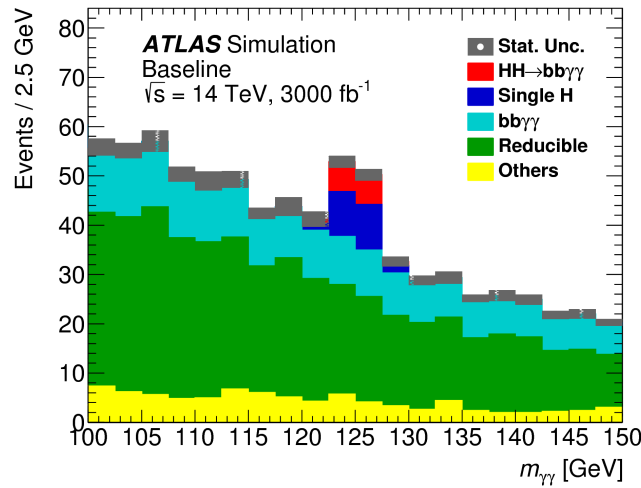


Figure 2.3: Diphoton invariant mass distribution of signal and background contributions [36]. The 'Reducible' background contains $b\bar{b}j\gamma$, $b\bar{b}jj$, $c\bar{c}\gamma\gamma$ and $c\bar{c}j\gamma$. 'Others' consists of $t\bar{t}$ and $\gamma\gamma Z$.

The search for physics beyond the SM is an important part of the HL-LHC program.

The large integrated luminosity increases the reach for high mass dilepton resonances. Figure 2.4 shows the invariant mass distribution for events satisfying all selection criteria in the dielectron channel. A SUSY Z' with a mass of 5 TeV is displayed together with the expected background. This shows that a good energy resolution is also important for electrons at the upper end of the energy range.

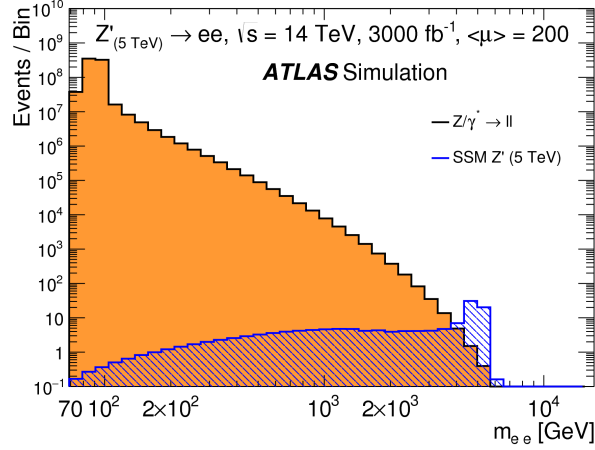


Figure 2.4: Invariant mass distribution for events in the dielectron channel [36]. The expected background is shown together with a SUSY Z' boson with a mass of 5 TeV.

These examples show that a good energy resolution for photons and electrons is vital for future Higgs studies and the search for new physics. This is directly coupled to the performance of the ATLAS LAr calorimeter. Moreover, the calorimeters provide real-time information to the trigger systems, which make first decisions about physics events to be interesting for further analysis. Therefore, the upgrade of the LAr calorimeter readout is vital for preparing the ATLAS detector for HL-LHC operation.

Chapter 3

Experimental Setup

3.1 The Large Hadron Collider

The LHC is a huge machine located at European Organization for Nuclear Research (CERN), in Geneva near the Swiss-French border. It is inside a circular 26.3 km long tunnel at a depth between 45 m and 170 m [18]. The tunnel was previously used by the Large Electron-Positron Collider (LEP) [37]. The LHC is the largest and most powerful accelerator in the world. It consists of two rings, in which protons or ions are accelerated in opposite directions. These rings cross at four locations, called Interaction Points (IPs), to enable collisions. Before arriving at the LHC, the particles pass several pre-accelerators, which are depicted in fig. 3.1. For protons, the procedure starts in the linear accelerator 2 (Linac2). The energy of the particles is increased with each circular accelerator, namely the Proton Synchrotron Booster (PSB), the Proton Synchrotron (PS), the Super Proton Synchrotron (SPS) and finally the LHC. Since the particles travel 11,000 times per second around the circle and reach energies up to 7 TeV, the beam pipes need to be evacuated to minimize collisions with the residual gas.

The LHC has eight straight sections and eight arcs, in which the particles need to be redirected to stay inside the accelerator. Due to their high momentum, this can only be done with very powerful magnets. The bending of the beam is done by dipole magnets, while quadrupoles squeeze the beam either vertically or horizontally. There are also magnet types of higher orders close to the former to correct for imperfections in the magnetic field [39]. The 1200 dipole magnets have a field of 8.33 T. This is achieved by superconducting technology, which means they need to be cooled by liquid Helium to around 2 K at all times. At these temperatures the material has no electrical resistance and can conduct much larger currents, while traditional electromagnets would produce too much heat. Similarly, the acceleration devices are cooled to 4.5 K to support a maximum voltage of 2 MV [40].

The acceleration is done by 16 Radio-Frequency (RF) cavities, which generate a resonant electromagnetic field. Energy is transferred from the field to the charged particles,

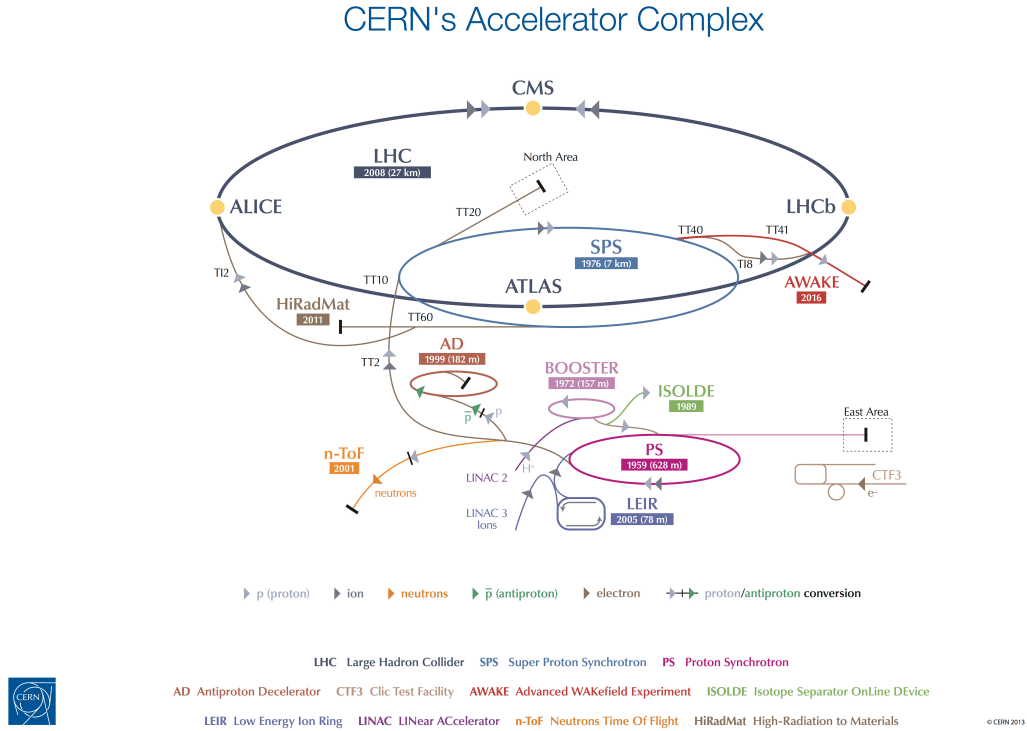


Figure 3.1: Sketch of the different accelerators and detectors at CERN [38]

which then experience an accelerating force. The dipole magnets increase their magnetic field, being synchronized to the rising kinetic energy of the charged particles, making the LHC a synchrotron. The fields in the cavities are tuned to oscillate at 400 MHz. This makes the timing of the arrival of the particle important. Ideally, when the bending magnets are at full energy, a particle should not be accelerated anymore. If it is slower, then it arrives a bit later and receives a positive acceleration, while a faster particle is decelerated, because it arrives sooner in the cavity. Therefore, the particles are not forming a continuous beam but rather several bunches.

There are several possibilities to set up these bunches [41]. For protons the spacing between two possible bunch positions is 25 ns. The inverse is a frequency of 40 MHz giving information about the collision or Bunch Crossing (BC) rate. There are 3564 possible bunch positions, numbered by a Bunch Crossing Identifier (BCID). They cannot all be filled due to the rise time of the LHC injection kickers and the pre-accelerator structure. The principal scheme allows for 2808 bunches in the LHC and can be seen in fig. 3.2. There are 39 batches of 72 filled bunches, each containing 1.15×10^{11} protons nominally.

The particle collisions of the LHC are used by seven experiments. The first four are the main detectors located directly at an IP.

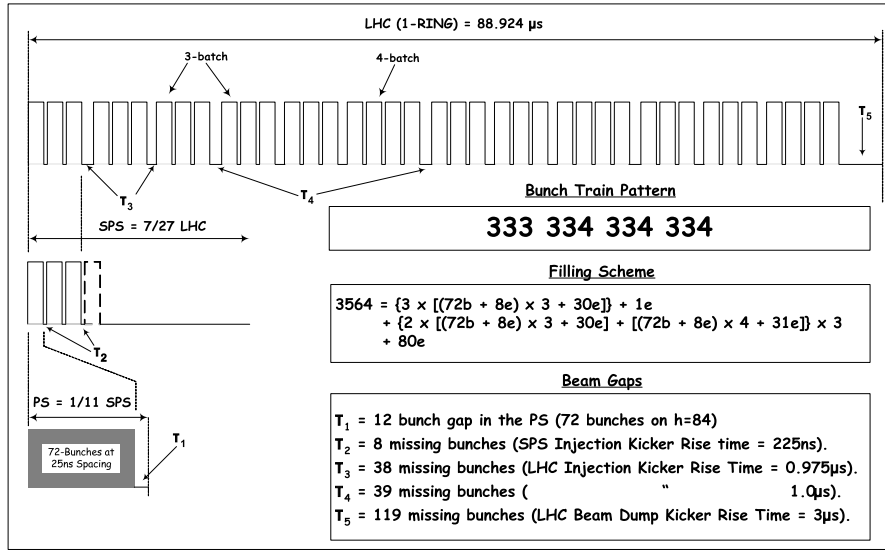


Figure 3.2: Filling scheme for the LHC [41]

- ATLAS is the biggest detector at the LHC and of major importance in this thesis. As a general purpose detector, ATLAS investigates a wide range of physics. It is described in more detail in the next section.
- CMS is the other general purpose detector with the task to explore the pp collisions. One of the main distinguishing features is a high-field solenoid for the measurement of the momentum of muons and other charged particles [42]. It also has a full silicon based inner tracking system and a homogeneous electromagnetic calorimeter equipped with scintillating crystals.
- LHCb performs precision measurements of CP violation, which is the combination of charge and parity symmetry violation, and rare decays of B hadrons [43]. A study of heavy flavor physics might produce rare decay branching fractions or forbidden decay modes. The detector has a single arm geometry, which is justified by B hadrons being predominantly produced in the same forward or backward cone.
- ALICE is a heavy-ion detector focusing on the strong interaction [44]. It is designed to study the quark-gluon plasma at extreme energy density and temperature values. This is a state of matter at which the particles are freed of their strong attraction. ALICE consists of a central barrel part and a forward muon spectrometer.
- MoEDAL searches for the magnetic monopole and other highly ionizing stable massive particles [45]. These would move too slow to be effectively measurable by ATLAS or CMS. The detector consists of an array of plastic nuclear track detectors around the IP near LHCb

- TOTEM measures the total pp cross section and studies electric scattering and diffractive dissociation at the LHC [46]. It is located in the CMS forward region and consists of two tracking telescopes.
- LHCf provides information on high energy cosmic ray physics [47]. Therefore, it consists of two detectors located 140 m on either side of the ATLAS IP. The small calorimeters measure forward production spectra of photons and the leading particle spectrum.

3.2 The ATLAS Detector

This section gives an overview of one of the two general purpose experiments, the ATLAS detector. Its task is the precise measurement of SM parameters and the search for new physics [19]. The first benchmark was the successful discovery of the Higgs boson in 2012 [20]. It is mostly observed via lepton and photon decay channels. A decay into hadrons is difficult to detect due to QCD backgrounds, but was also observed recently [48]. When a quark or gluon is one of the generated particles, a stream of particles, called jet, is produced. Now there is a search for Physics Beyond the Standard Model (BSM) in the foreground. One of the typical signatures for new particles are measurements of significant amount of missing transverse energy (E_T^{miss}), because some of them would interact very weakly with the detector.

The coordinate system of ATLAS has the origin at the IP. The positive x -axis is defined as pointing towards the center of the LHC ring and the positive y -axis points upwards. In agreement with the right-hand rule, the z -axis runs along the beam direction. The side-A of the detector has positive z , while the side-C has negative z . The already mentioned transverse energy is defined in the x - y plane. Usually, the azimuthal angle, ϕ , and the pseudorapidity, η , is used to describe a position in the detector. The former is measured as usual around the beam axis and the latter is defined as $\eta = -\ln(\tan(\frac{\theta}{2}))$, with θ , also known as polar angle, being the angle from the beam axis. The pseudorapidity has the advantage to be Lorentz invariant under boosts along the z -axis.

The dimensions of the ATLAS detector are 25 m x 25 m x 44 m with an overall weight of approximately 7000 t. Its structure can be seen in fig. 3.3. The particles enter the detector from the left and right side and collide in the IP in the center. Closest to this point is the Inner Detector (ID), which is surrounded by a superconducting solenoid. The calorimeter system around the ID is surrounded by three superconducting toroids. This was a fundamental choice and drove the design of the rest of the detector. Finally, the muon spectrometer defines the outer dimensions of the ATLAS experiment. The detailed explanations of the individual parts are given in the following sections.

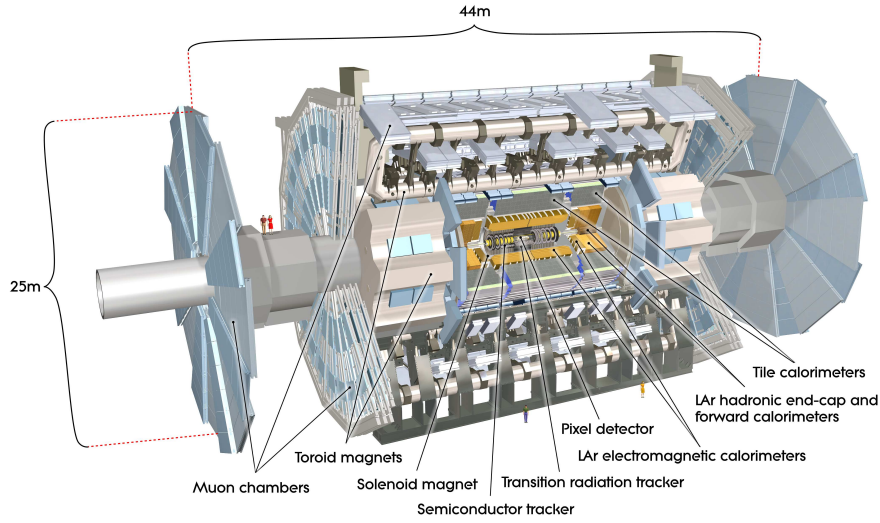


Figure 3.3: Structure of the ATLAS detector with the different sections [19]

3.2.1 The Inner Detector

The task of the ID is to reconstruct the tracks of the particles after the collision [49]. It contributes to the electron, photon and muon recognition. The surrounding solenoid provides a 2 T magnetic field. It forces charged particles on a bent track and their momentum can be calculated from the curvature. The ID consists of three different sections, which can be seen in fig. 3.4.

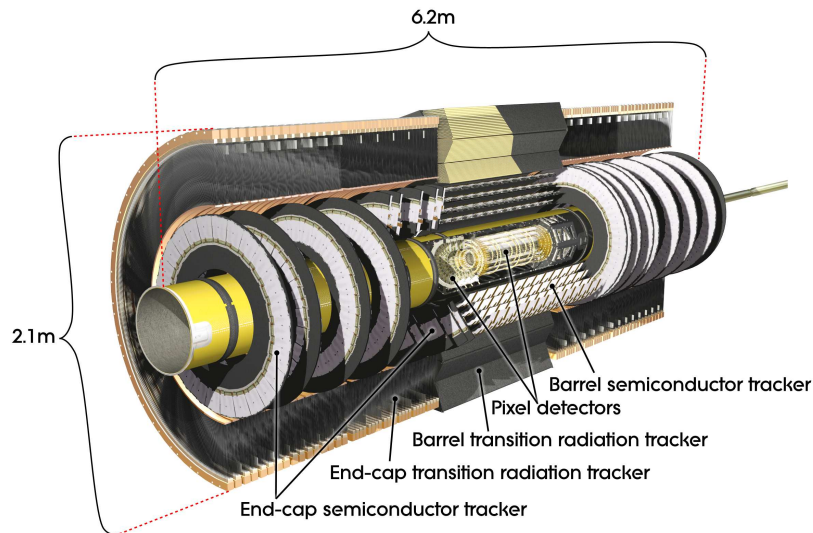


Figure 3.4: Structure of the Inner Detector with the different sections [19]

The innermost part is a semiconductor pixel detector. It provides a very high granularity and precision very close to the IP. The 140 million detector elements are located on several barrels and disks with the closest radius of 4 cm up to a distance of 20 cm. An additional Insertable B-Layer (IBL) was installed between the beamline and the previous innermost Pixel layer [50] in the years 2013-14. The Semiconductor Tracker (SCT) uses silicon microstrip technology and consists of barrel and forward modules. The semiconductor diodes of these detectors are depleted by applying a reverse voltage to their electrodes. An entering ionizing particle generates charges, which produce a signal due to the electric field [51].

Because of its lower cost and material budget in front of the calorimeters, a Transition Radiation Tracker (TRT) is used for the rest of the ID. It consists of 4 mm diameter drift tubes kept at a high voltage [52]. Each has a gold-plated tungsten wire in the center and is filled with a xenon based gas mixture, which is replaced by Argon in certain detector regions due to leaks. A passing particle ionizes the gas atoms. The resulting charges drift to the wire and the tube. By measuring the timing, the distance between the track and the wire can be deduced. The straws are interleaved with polypropylene foils as radiators. When electrons of sufficient momentum traverse the TRT layers, transition-radiation photons are created, which adds electron identification capabilities. In total the ID has a radius of 115 cm and a length of 7 m covering a region of $|\eta| \leq 2.5$.

3.2.2 Calorimetry

The ATLAS calorimetry system can be seen in fig. 3.5. It covers a region of $|\eta| \leq 4.9$ and is divided into an electromagnetic and a hadronic section. The former is an important part of this thesis and described in more detail in section 3.3. The task of a calorimeter is to measure the energy of passing particles by decelerating and stopping them. This is mostly done by an absorber material, while an active material provides the measurable signal generation. In ATLAS these are two different materials hence it is called a sampling calorimeter. In contrast, a homogeneous calorimeter only uses one material for absorption and signal generation.

The central hadronic calorimeter is called Tile Calorimeter, which consists of a cylindrical structure with an inner radius of 2280 mm and an outer radius of 4230 mm [53]. It is divided into three barrels covering a range of $|\eta| \leq 1.7$ and has a coarser granularity compared to its electromagnetic counterpart. This is sufficient for jet reconstruction and E_T^{miss} measurements. The Tile Calorimeter uses steel as absorber material and scintillating plates as the active medium. The latter are excited by ionizing and emit the energy in form of light, which are read out by wavelength shifting fibers. They absorb these higher frequency photons and emit lower frequency photons. Finally, a measurable electronic signal is generated using photomultipliers.

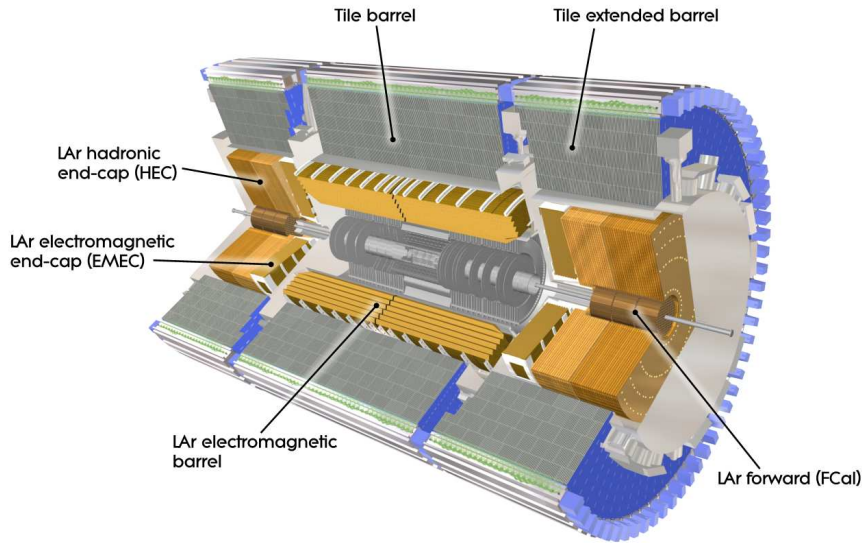


Figure 3.5: Structure of the calorimeter system with the different sections [19]

3.2.3 The Muon Spectrometer

Due to their little energy loss in matter and long lifetime, muons usually pass through the other parts of the experiment. However, they are amongst the most promising signatures of interesting physics [54]. Therefore, the outermost section of ATLAS is designed to detect charged particles exiting the calorimeters and to measure their momentum. This is done by using a barrel toroid and two end-cap toroids generating magnetic fields of approximately 0.5 T and 1 T, respectively. The magnetic fields bend the track of the muons and, similarly to the ID, the curvature can be used to calculate their momentum. The setup covers a pseudorapidity range of $|\eta| \leq 2.7$ and can be seen in fig. 3.6.

Monitored Drift Tubes (MDTs) are used for the track coordinate measurements. There are more than 350,000 tubes filled with argon and carbon dioxide, and they are connected to a high voltage of around 3000 V. In the forward region closer to the beam, Cathode Strip Chambers (CSCs) with higher granularity are installed. They need to sustain the demanding rate and background conditions of this region. The CSCs are multiwire proportional chambers with the wires oriented in the radial direction. Both cathodes are segmented in strips, one parallel and one perpendicular to the wires. Only the strips are used for readout.

There are additional detectors for the trigger system, which is explained in section 3.4. They provide a track coordinate measurement orthogonal to the precision measurement in the range of $|\eta| \leq 2.4$. Resistive-Plate Chambers (RPCs) are gaseous parallel-plate detectors, which are used in the barrel region. A uniform electric field between the two Bakelite plates produces the avalanche multiplication of the ionization particles. Thin-

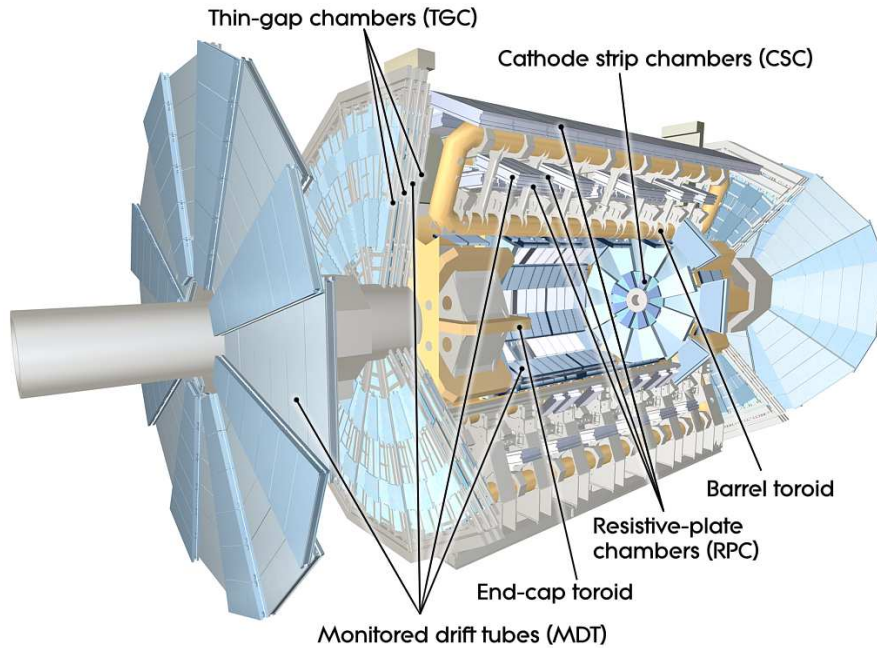


Figure 3.6: Structure of the muon system with the different sections [19]

Gap Chambers (TGCs) are used in the forward regions and are required to have good time resolution and fine granularity. Their structure is similar to multiwire proportional chambers.

A summary of the interactions between particles and different parts of the detector can be seen in fig. 3.7.

3.3 The Liquid-Argon Calorimeter

3.3.1 Working Principle

The LAr calorimeter measures the energy of particles by their complete absorption. The electromagnetic calorimeter can detect also hadrons and electromagnetic particles inside jets, and E_T^{miss} , but mainly focuses on precision measurements of the energy of electrons and photons [56]. These particles interact differently with the detector depending on their energy. High energy electrons or positrons mainly decelerate via bremsstrahlung, which is the emission of a photon due to the deflection of the particle mainly by nuclei in the detector material. High energy photons usually interact by electron-positron pair production. Both of these interactions result in additional secondary particles, which in turn also generate particles via the same processes. This cascade of particles is called shower development and is an important phenomenon of calorimeters [57]. The energy of the shower particles steadily decreases with increasing number of particles until no

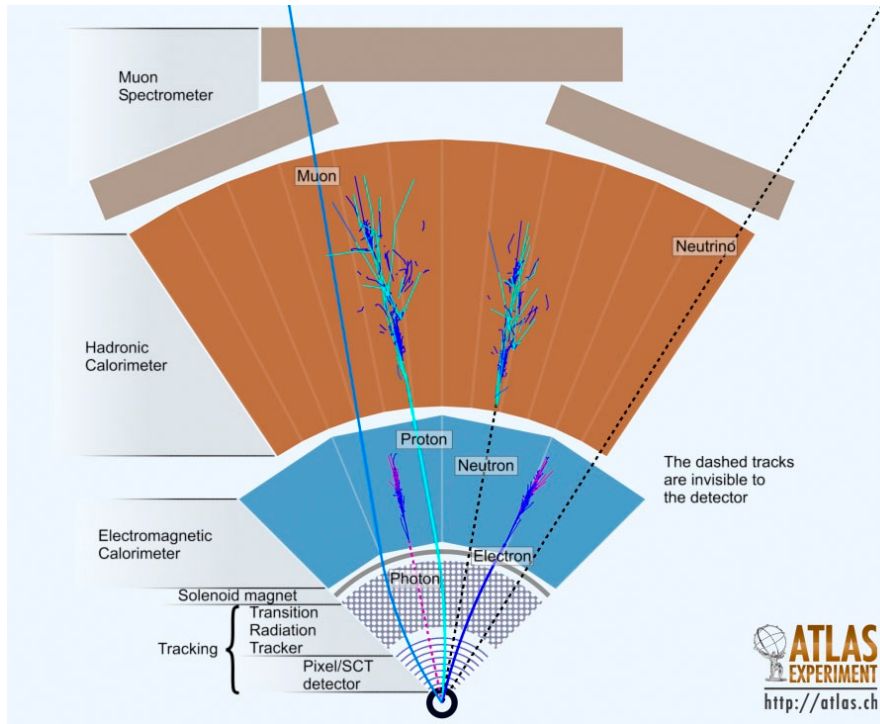


Figure 3.7: Interaction of different particles with the detector sections [55]. Only charged particles are visible in the Tracker. Most particles develop a shower in the calorimeter.

further electrons, positrons or photons can be produced. At lower energies, the latter interacts with the detector through Compton scattering, which is the scattering with an electron, and the photoelectric effect, which is the emission of an electron after the photon absorption by the material. Low energy electrons and positrons lose their energy through collisions inside the medium resulting in the ionization of the material.

The longitudinal and lateral size of electromagnetic showers can be parameterized by the radiation length X_0 , which depends on the atomic numbers and composition of the detector material. It represents the average distance, after which the energy of the primary electron is reduced to $1/e$ of its original value. Similarly, the intensity of a photon is reduced to $1/e$ of the original value after traveling a distance of $\frac{9}{7}X_0$. The longitudinal length of a shower has a logarithmic dependence on the incident particle energy. The LAr calorimeter has a thickness of around $30X_0$, depending on the pseudorapidity. This is sufficient to keep the longitudinal leakage of the showers to a minimum. The lateral size is a result of multiple scatterings of electrons and photons in the transverse direction. For electromagnetic showers the lateral extension is kept small and roughly energy independent.

An important parameter in calorimetry is the energy resolution. It can be written

as:

$$\frac{\sigma}{E} = \frac{a}{\sqrt{E}} \oplus \frac{b}{E} \oplus c$$

where $\oplus$ indicates a quadratic average. The first term on the right side is called the stochastic term, which includes the fluctuations related to the physical development of the shower. In homogeneous calorimeters these are small, but in sampling calorimeters the energy deposited in the active medium fluctuates event by event due to the interleaved absorber layers. These sampling fluctuations are the most important limitation to the energy resolution in these detectors and in the electromagnetic LAr calorimeter the stochastic term is around $10\%/\sqrt{E}$. The second term is the noise term, which depends on the features of the readout circuit. In this thesis it is referred to as electronic or thermal noise. Since the signal arises from the collection of charge carriers, the first element in the readout chain is a preamplifier, which contributes a large fraction of noise. The noise needs to be minimized by shaping and filtering. Due to the energy dependency, smaller signals have a higher relative noise contribution. In sampling calorimeters the noise term can be decreased by increasing the sampling fraction $f_{\text{samp}} = E_{\text{active}}/E_{\text{total}}$. Finally, there is a constant term, which scales with the energy of the particle. In the LAr calorimeter, contributions are for example gaps in the mechanics of the modules and temperature inhomogeneities. The value of the constant term is kept below 0.7%.

3.3.2 Structure of the Liquid Argon Calorimeter

The sampling calorimeter consists of alternating layers of an active and an absorber medium. Liquid Argon is used as the former and motivates the naming of the electromagnetic calorimeter. Each active material sector has readout electrodes consisting of three conductive copper layers separated by insulating polyimide sheets. The outer layers are connected to a high voltage potential of up to 2000 V, which generates an electromagnetic field in the liquid Argon. The inner layer is used for readout via capacitive coupling. A single electron between the electrodes would drift to the anode due to the force generated by the electromagnetic field. It would create a constant current for as long as it takes the electron to drift to the positive electrode [58]. A passing particle ionizes the liquid Argon and produces ions and electrons uniformly inside the gap. Because of their lower mobility, ions contribute very little to the collected charge. At the beginning, all electrons contribute to the produced current, while close to the end of the maximum drift time of around 450 ns only few of them are still in the gap. This results in a triangular current pulse shape at the readout, whose height is proportional to the deposited energy.

Figure 3.8 displays the structure of the LAr calorimeter and the separation into different regions. In the center, there is the Electromagnetic Barrel (EMB), which is made out of two half barrels and covering a range of $|\eta| \leq 1.4$. The two Electromagnetic End-Caps (EMECs) are separated into two co-axial wheels with a range of $1.375 < |\eta| < 2.5$ and $2.5 < |\eta| < 3.2$, respectively. Both sections use lead plates as absorbers, which are glued to stainless steel sheets, to provide mechanical strength. In addition, they are

arranged in an accordion structure visible in fig. 3.9. This provides a full coverage in ϕ without any cracks and makes sure that electrons are uniformly generated inside the gap.

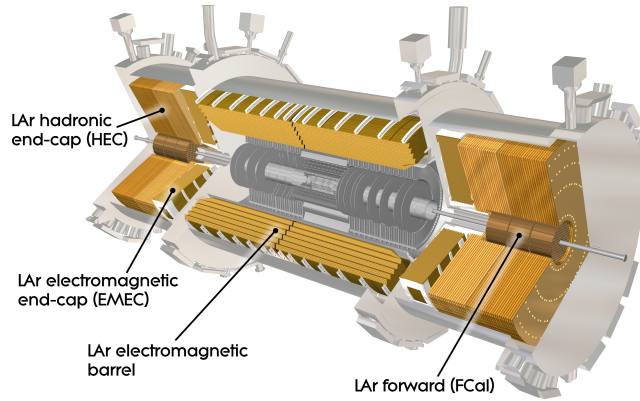


Figure 3.8: Structure of the LAr calorimeter and its components [59]

In the EMB, the folding angles of the waves vary with the radius to keep the liquid-Argon gaps constant, while in the EMEC, the gaps increase with the radius. Figure 3.9 also shows the three different layers, whose main distinguishing feature is the η granularity, and the presampler. The first layer has a very fine segmentation for an accurate position measurement in this region. This helps to discriminate between a single $e^\pm/\gamma$ and a π^0 , which decays into two photons with a small opening angle. The largest fraction of the energy is collected in the second layer, while the third layer only collects the tail of the electromagnetic shower and therefore needs less segmentation in η . This separation in layers also applies to the outer wheel ($1.5 < |\eta| < 2.5$), while the rest of the EMEC is only segmented into layers with coarser granularity. To correct for the energy loss of photons and electrons upstream of the calorimeter and to atone for the big amount of dead material, the presampler is installed in front of the accordion structure. This is a single active liquid-Argon layer and covers the region $|\eta| < 1.8$.

The Hadronic End-Cap (HEC) also uses liquid Argon as an active material, but copper as an absorber medium. It covers a range of $1.5 < |\eta| < 3.2$ and is divided into two wheels, each containing two longitudinal sections. An important aspect is the detection of muons and the measurement of any radiative energy loss. Finally, the Forward Calorimeter (FCal) also belongs to the LAr calorimeter even though only one of the three modules is optimized for electromagnetic measurements. It uses copper as an absorber medium, while the other two modules use tungsten and measure predominantly the energy of hadronic interactions. The FCal covers a region of $3.1 < |\eta| < 4.9$ with a distance of approximately 4.7 m from the IP. The high η value leads to very high particle

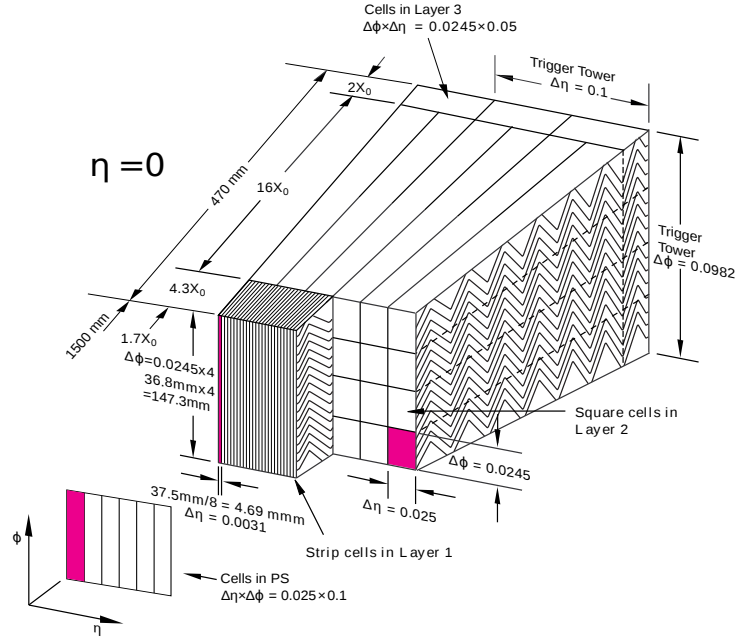


Figure 3.9: Accordion geometry of the LAr calorimeter [19]. The detector consists of the presampler, the finely segmented front layer, the widest middle layer and the back layer. Three single elementary cells are highlighted. The figure uses the ATLAS coordinate system.

fluxes. To avoid the problem of the consequential build up of ions, the liquid-Argon gaps are smaller than the 2 mm of the EMB. This leads to a smaller electron drift time and faster signals.

3.3.3 Readout

The liquid-Argon gaps are connected to a total of 182,468 readout channels, which consist of a complex system of electronics. In the original design, it has the task to provide the trigger with reduced granularity energy information, and to forward the full granularity of accepted events to the Data Acquisition (DAQ). The operation of the trigger, including the specific Level-1 (L1) part, is described in section 3.4. Each channel provides an energy range from around 10 MeV up to 3 TeV. The lower limit is set by the thermal noise of the calorimeter electronics. The readout can be separated into a front-end, which is located directly at the detector and needs to be radiation resistant, and the back-end, which is in a separate room further away from the ATLAS detector. An overview can be seen in fig. 3.10.

The analog signal arrives from the detector at the Front-End Board (FEB), which can process up to 128 calorimeter channels and is housed in a Front-End Crate (FEC). After the signal is increased at a preamplifier, it is split into a trigger and a main

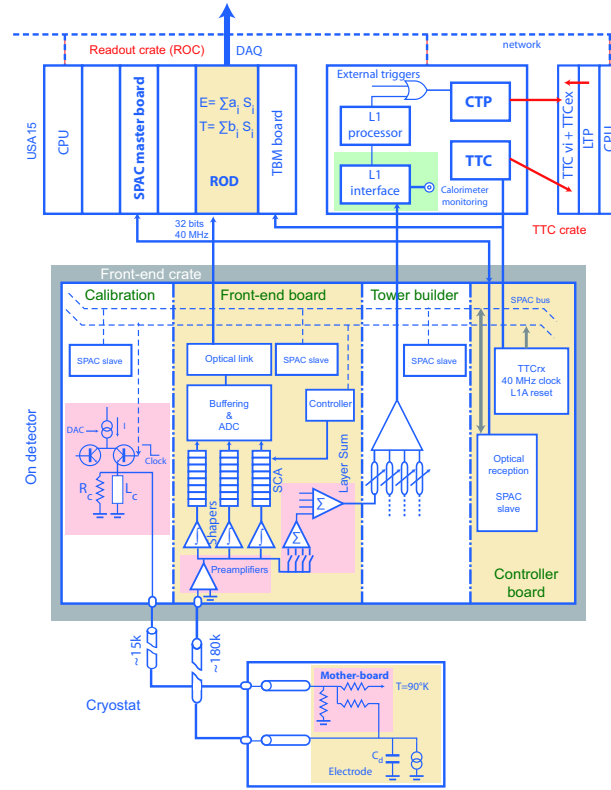


Figure 3.10: Readout system of the LAr calorimeter [19]

readout path. The latter is again divided into three different gain scales ($\times 1$, $\times 10$ and $\times 100$). The reason is that the preamplifier is designed to cover a dynamic range of 17 bits, which is too much for one Analog-to-Digital Converter (ADC). Therefore, the range is split into several gain scales, to later choose the optimal gain depending on the pulse height. Each scale is directed into a shaper, where it gets reformed into a bipolar pulse, which is improving the signal-to-noise ratio. First, a single differentiation CR step removes the long tail of the triangular pulse and then two integration RC steps limit the bandwidth reducing the noise. The time constant of the shaper is set to 15 ns as a compromise between the two main noise contributions, namely electronics noise and pileup noise, which decrease and increase with the shaping time, respectively. Pileup is the overlap of multiple pulse shapes from subsequent collisions and is described in more detail in section 5.1.1. After the shaper, the signal is stored in Switched-Capacitor Arrays (SCAs), where it awaits the result of the L1 trigger. Upon acceptance, the pulse is sampled by an ADC at the BC frequency, 40 MHz. Only the first four to five samples of one of the gains per channel, chosen by a gain-selector chip, are sent to the back-end electronics via optical fibers. The transformation of the signal from the triangular to the bipolar pulse and the sampling of the ADC can be seen in fig. 3.11.

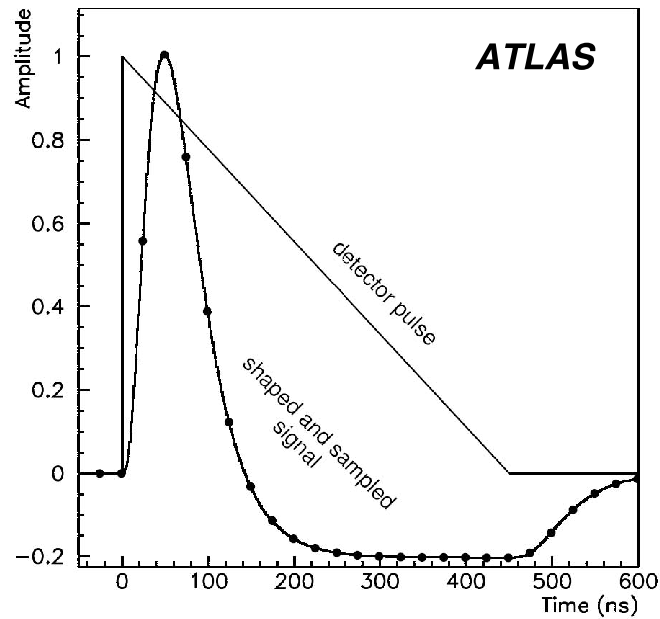


Figure 3.11: Different stages of the pulse shape [60]. A triangular signal arrives from the detector. It gets shaped into a bipolar form, which is sampled every 25 ns.

The trigger readout path passes through a series of channel summing devices, because the trigger processor uses a coarser granularity of the detector ($\Delta\eta \times \Delta\phi = 0.1 \times 0.1$). The final level of summing for the EMB and EMEC is done on the Tower-Builder Board (TBB). For the HEC and the FCal no further summing is needed and the corresponding boards are called Tower-Driver Boards (TDBs). In both cases the analog signals are transmitted to the back-end.

Another part of the front-end is the controller board, whose main task is the reception and distribution of the 40 MHz clock and the L1 trigger accept signal. Finally, the calibration board generates precisely known current pulses to simulate energy deposits in the calorimeter. This is done via discharging a capacitor, which results in an exponential curve. Therefore, the difference to the triangular pulse needs to be corrected for in the electronic calibration procedure.

The core of the back-end are the Readout Drivers (RODs), which receive the digitized samples from the FEB. To minimize noise, the data is processed by an Optimal Filter (OF) inside the Digital Signal Processors (DSPs). OFs will be described in more detail in section 5.1.2. After formatting and several checks, the data is forwarded to the DAQ for continuous processing. The trigger path from the TBB or the TDB proceeds at the L1 processor. Here, the signal is digitized and converted from energy to transverse energy. The Trigger, Timing and Control (TTC) system distributes the clock and trigger signal to the front-end.

3.4 The Trigger System

The detector produces data at a frequency of 40 MHz. Each event produces several MB in the ATLAS detector. This is on the one hand far too much information to be stored and analyzed. On the other hand it mainly consists of already well-known inelastic pp scattering events. The function of the trigger system is to select the more interesting and rare high p_T signatures to effectively reduce the data rate. It is divided into three distinct levels: L1, Level-2 (L2) and the Event Filter (EF). The former is already mentioned in the readout section 3.3.3 and uses custom-made electronics. The latter two together form the High-Level Trigger (HLT) and are based on commercially available hardware. At each level, the data has to be stored until the decision is made and the event is accepted or discarded.

Currently, the L1 trigger needs to reduce the rate to 100 kHz having less than $2.5\ \mu\text{s}$ to make a decision to accept an event. As seen in fig. 3.12 it uses information from the calorimeter and the muon spectrometer. The RPC and TGC (see section 3.2.3) from the latter search for high p_T muons. In the calorimetry, elementary readout channels are combined to Trigger Towers, which can be seen in fig. 3.9. This reduced granularity information from the whole calorimeter (see section 3.2.2) is used to identify electrons, photons, τ -leptons, E_T^{miss} , and large total transverse energy. The L1 decision is based on multiplicities of trigger objects and given energy or momentum thresholds. In the calorimeter, isolation can also be required, which implies that the energetic particle needs to have a minimum angular separation from other identified physics objects. The L1 trigger also defines Regions of Interest (RoIs), including the geographical coordinates in η and ϕ , which are sent to the L2 section.

The L2 trigger uses this information to reduce the data rate further to 3.5 kHz with a processing time of about 40 ms. In contrast to L1, it uses the full granularity and all available detector data including the ID inside the RoI, which is around 2% of the total event data. Until the decision is made, the data is temporarily stored in local buffers in the first stage of the DAQ. Events selected by L2 are transferred to the event-building system and afterwards to the EF as the last trigger stage. At this point, offline analysis on fully-built events is used to reduce the rate to 200 Hz in around 4 s. Accepted events are classified and finally moved to permanent storage at the CERN computer center.

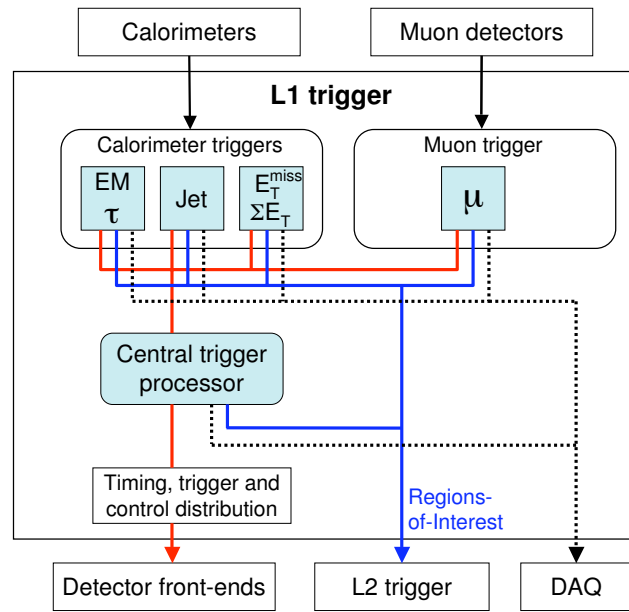


Figure 3.12: Parts of the LAr trigger system [19]. The L1 trigger uses calorimeter and muon detector information to make a decision on an event and sends RoIs to L2.

Chapter 4

The Upgrade Plans

The LHC and all detectors performed excellently during the first years of operation. In July 2012, the discovery of the Higgs particle was announced [61] and many new limits on where to search for new physics have been set. A maximum collision energy of 13 TeV was reached by the LHC so far [62]. At the end of 2018, the total integrated luminosity since the beginning of operation was 189.3 fb^{-1} for ATLAS and CMS [63]. For the future, improvements of the LHC and the detectors are planned to be able to provide more accurate measurements of SM processes and improved sensitivity for new particles. Observations of rare processes that occur below the current sensitivity level would also be possible [21]. The current plan including past modifications can be seen in fig. 4.1.



Figure 4.1: Project plan for the LHC [21]. Data collection takes place during the Runs. The Long Shutdowns are used to improve the accelerator and detectors.

The data-taking is done during LHC Runs, interrupted by Long Shutdowns, which are used to install phases of the upgrades. At the end of Run 1 in 2012, an integrated luminosity of 28.6 fb^{-1} was delivered to ATLAS and CMS [64]. A peak luminosity of

$7.7 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ and a maximum collision energy of 8 TeV was reached [65]. In the Long Shutdown 1 (LS1) from 2013 to 2015, the Phase-0 upgrade was installed, which was necessary after an accident in September 2008. During powering tests, a fault occurred in a superconducting electrical bus connection resulting in mechanical damage and the release of helium [66]. Due to the availability of spare magnets, the damage could be repaired. There was only a delay of 6 months, but the LHC could only operate at a reduced center-of-mass energy [67]. During LS1, the electrical connections were consolidated to ensure that such an incident does not happen again. This and other activities in the accelerator system made an operation of the LHC at design center-of-mass energy possible. In addition, during Run 2, a peak luminosity of about $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, which is twice the design luminosity, was reached [63].

Currently, the LHC is in the Long Shutdown 2 (LS2), which started in 2019 and ends in 2020. The Phase-1 upgrade is installed during that period. It is explained in more detail in section 4.1. The upgrade enables the collider to have a slightly higher center-of-mass energy and luminosity in Run 3 between the years of 2021 to 2024. The following upgrade is Phase-2 during the Long Shutdown 3 (LS3) in the years from 2025 to 2027, which is explained thoroughly in section 4.2, because of its high importance for this thesis. This period allows further improvements in the accelerator and the detectors to enable even higher luminosities. Further data-taking is done under the HL-LHC project, which is planned to last for over 10 years.

4.1 Phase-1

The current performance of the accelerator and the experiments is not sufficient to meet the requirements of the HL-LHC project [68]. Phase-1 plans to allow a peak luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and an integrated luminosity of 28.6 fb^{-1} . This is done by doubling the intensity of the injected beam and multiplying its brightness by 2.5, which is realized by the LHC Injectors Upgrade (LIU) project [68]. This includes the new linear accelerator 4 (Linac4) and upgrades of the PSB, PS and SPS. Linac4, providing a kinetic energy of 160 MeV, replaces Linac2, which only generates 50 MeV. To cope with the higher energies the injection lines of the consecutive circular accelerators are improved and new accelerator systems enable higher beam intensities. There are also improvements planned for the LHC itself, e.g. a replacement of several main superconducting magnets. The increased luminosity changes the mean number of interactions per BC, μ , from 20 to 80.

The individual experiments are also upgraded, partly due to the higher luminosity. A new high-resolution inner tracking system is installed in ALICE [69], and CMS replaces the pixel detector and upgrades the trigger [70]. LHCb has all the front-end electronics and part of the detector itself exchanged, because the hardware trigger is removed [71]. In ATLAS the muon spectrometer is enhanced by a New Small Wheel (NSW), which improves its muon trigger capability [72].

4.1.1 Changes at the ATLAS Detector

The already mentioned higher number of interactions leads to more events with high p_T signatures. This, consequently, results in a higher acceptance rate of the L1 trigger. Difficulties arise with the exceeding of 100 kHz, which is the maximum possible frequency that can be processed by the hardware DAQ systems and the L2 trigger. There are two solutions to lower the acceptance rate. The current lepton p_T threshold of about 25 GeV for electrons and muons could be increased. This would in return mean the loss of a lot of interesting physics. For instance the electroweak scale starts around 40 – 50 GeV, which is around half the mass of the $Z/W^\pm$ bosons.

Another solution is the revision of the current electron/photon algorithm, which is currently used in the L1 trigger [19]. New shower recognition algorithms for the LAr can improve the background rejection and reduce therefore the acceptance rate without losing interesting physics. These algorithms group several calorimeter elementary cells and calculate shower parameters in a more refined way as it is done now. The exact definition and more information can be found in [60]. The result can be seen in fig. 4.2, which shows the acceptance rate for several energy thresholds with and without these shower parameters. A successful use can only be guaranteed by increasing the granularity of the L1 trigger.

Currently, the already mentioned Trigger Towers are used for the L1 stage in most parts of the calorimeter. This is a summation of all elementary cells in a $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ area of all layers. This equals to 60 cells in the electromagnetic barrel calorimeter, which can be seen in fig. 4.3 on the left side. The right side shows the granularity after Phase-1. Here the elementary cells are combined to Super Cells, which are not summed across the layers. The area of one Trigger Tower equals to ten Super Cells, with one Super Cell in the presampler and the back layer and four Super Cells in the other two layers each. This change in the trigger setup results in the replacement of parts of the readout electronics.

4.1.2 Upgraded Readout Electronics

Figure 4.4 shows the Phase-1 readout electronics. New systems are located on the lower section and are marked with a red rectangle. The remaining parts show the current system and the graph only uses a different representation (compare with section 3.3.3). In this figure the front-end is on the left and the back-end is on the right. In the upgrade, only the trigger path is changed. The signals are first led through a new Layer Sum Board (LSB), where the cells are summed to Super Cells. They are then transferred to the LAr Trigger Digitizer Board (LTDB) via a new baseplane. Each LTDB processes up to 320 Super Cell signals. Here the path is split, with one path being summed to Trigger Towers and leading to the TBB of the original trigger path. This enables a comparison between the old and the new electronics. On the other path, the pulse is digitized, serialized and sent to the back-end via optical links. This reduces the noise

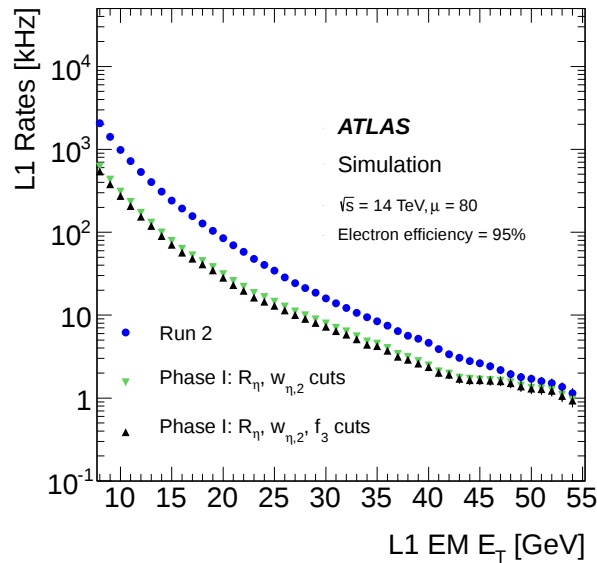


Figure 4.2: Acceptance rate of the L1 trigger with respect to the energy threshold [60]. Naturally the bandwidth can be decreased by increasing the threshold. Another possibility is the introduction of shower parameters (e.g. R_η , $\omega_{\eta,2}$), which also lowers the trigger rate. These group cells and calculate ratios to help distinguish between signal and background.

compared to the analog cables of the original trigger path.

The signal arrives in the LAr Digital Processing System (LDPS), which has the main purpose of extracting energy and timing information from the digital pulse. First, the up to 320 channels are received, deserialized, aligned, and reordered. Afterwards, an OF (see section 5.1.2) is applied in order to reduce noise. The Front-end Link Exchange (FELIX) system [73] converts detector data transport protocols to a commercial standard. It provides the clock and trigger signal to the LDPS. The energy information is sent to the Feature Extractor (FEX), an upgraded trigger processor divided into three parts. There is the electron Feature Extractor (eFEX) for electron, photon and τ -lepton detection in the region $|\eta| < 2.5$. The jet Feature Extractor (jFEX) identifies jets and E_T^{miss} based on the LAr calorimeter region $|\eta| < 2.4$, and the Tile calorimeter. Finally, the global Feature Extractor (gFEX) processes an entire event, but uses a coarser granularity.

4.1.3 Demonstrator

In order to test the proposed Phase-1 upgrade, a demonstrator was installed during LS1. It operated during Run 2 in parallel to the existing ATLAS detector, which ensured the compatibility of the two systems. The motivation for a demonstrator was to collect

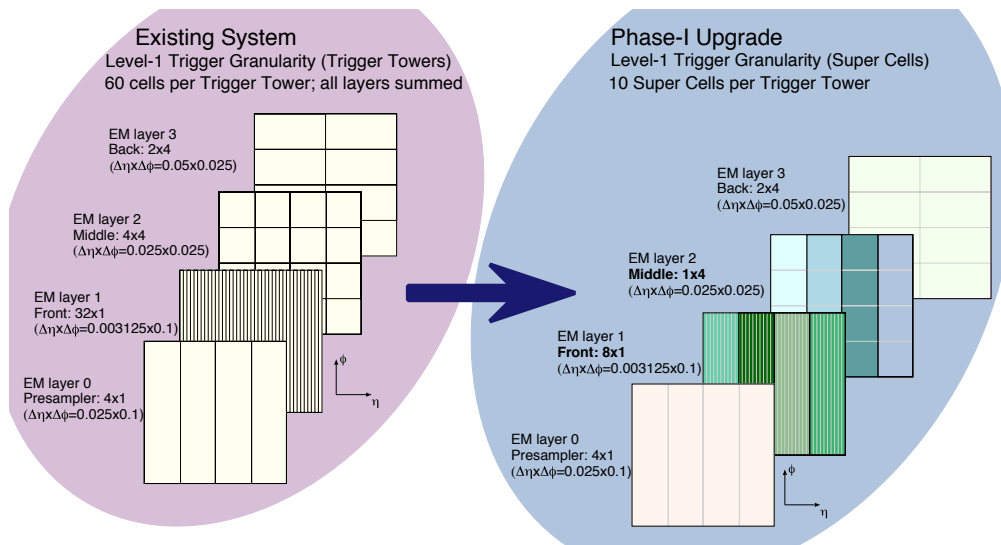


Figure 4.3: Elementary cells in a $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ area in all layers [60]. On the left side all of them get summed to one Trigger Tower. On the right side 10 Super Cell are formed with the same cells.

data from Super Cells for the validation of energy reconstruction and bunch crossing identification algorithms [60]. In addition, trigger efficiency and jet background rejection could be measured. One FEC in the EMB, covering a region of $\Delta\eta \times \Delta\phi = 1.4 \times 0.4$, was equipped with boards, which are required for the Phase-1 upgrade. This included new LSBs for the FEBs, two new baseplanes and two pre-prototype LTDBs in the front-end. Long fiber cables were used to connect the LTDBs to the back-end, where two pre-prototype LDPSs, called ATCA Board for a Baseline of Acquisition (ABBA) [74], were installed inside an Advanced Telecom Computer Architecture (ATCA) crate.

ABBA incorporated three ALTERA Stratix IV Field Programmable Gate Arrays (FPGAs) [75]. FPGAs are discussed in more detail in section . The two so-called Front FPGAs represented the core functionality of the future LDPSs [76]. They were connected to the LTDBs via high-speed optical transceivers and optical fibers. There was also an interface to the so-called Back FPGA by using an Extended Attachment Unit Interface (XAUI). In addition, the Back FPGA was connected to the ATCA backplane via XAUI as well. The ATCA crate was in turn linked to the computing framework.

From the computer, data was requested by the TDAQ system via an Ethernet connection [77] applying the IPbus protocol [78]. The Back FPGA received these requests, processed the different protocols, and transmitted them to the correct Front FPGA. The setup of the Back FPGA can be seen in fig. 4.5. Packets arrived from the right at the transceiver and were sent to the reset module to handle special reset requests. In the Ethernet module, the first header and trailer were decoded, which contained the Media Access Control (MAC) addresses of sender and receiver. The Address Resolution Proto-

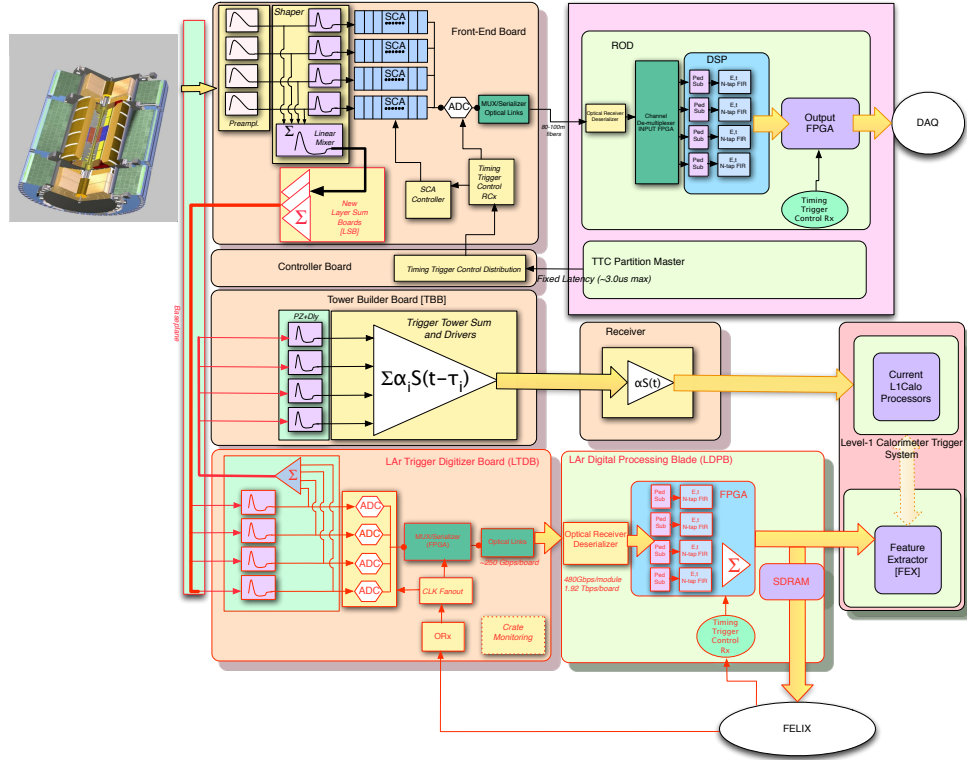


Figure 4.4: Upgraded readout system of the LAr calorimeter for Phase-1 [60]. New components have a red rectangular.

col (ARP) module stored pairs of MAC and Internet Protocol (IP) addresses. The latter were important for the IP module, which handled the corresponding protocol. Then, the User Datagram Protocol (UDP) module processed the header containing the source and destination port, before the packet was sent to the Front FPGAs. In the Front FPGA, the IPbus header is decoded.

4.2 Phase-2

The next upgrade for the HL-LHC enables the LHC to deliver a peak luminosity of $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, and an integrated luminosity of 4000 fb^{-1} after 12 years [36]. This increases the number of collisions per BC, μ , to 200 and is mainly achieved by the following changes of the accelerator setup [79]. The backbone of the upgrade are new superconducting magnets in the collision areas, which can withstand the higher radiation and keep the size of the bunches as small as possible. A very interesting new concept is the installation of superconducting crab cavities [79]. These are RF deflectors, which are located around the IP. They compensate the geometric crossing angle of the beams by applying a transverse kick and subsequently rotating the particle bunch. A visual

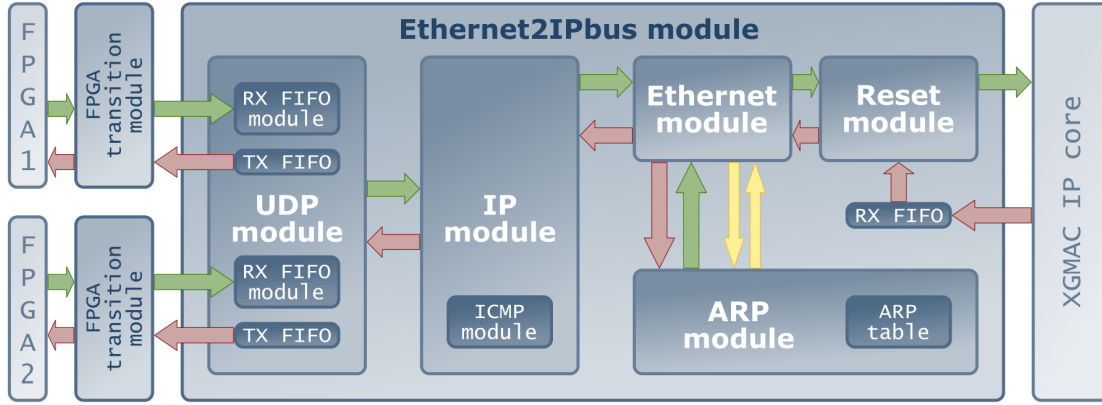


Figure 4.5: Different modules of the ABBA Back FPGA [76]. The TDAQ requests arrived from the right, were processed, and continued to one of the two Front FPGAs on the left.

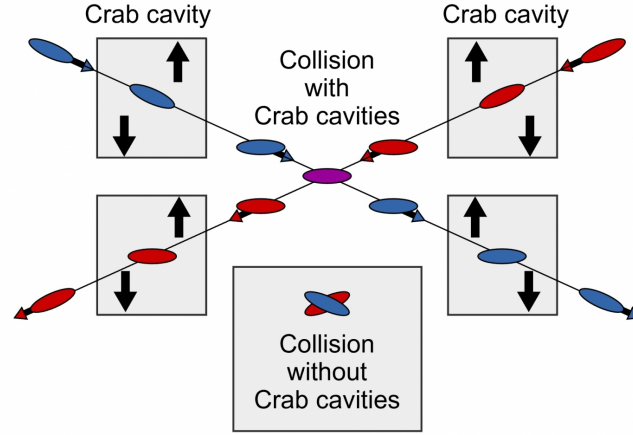


Figure 4.6: Effect of crab cavities on proton bunches [80]

representation can be seen in fig. 4.6.

During Phase-2, ATLAS and CMS are upgraded mainly because detector parts near the beamline show effects of aging caused by radiation exposure. Therefore, the tracker and the calorimeter endcaps of the CMS detector need to be replaced [81]. In addition, the muon endcaps are enhanced to maintain good L1 acceptance, and the trigger latency is increased. Similarly, by the end of Run 3, the silicon tracking systems of ATLAS will reach the end of their lifetimes. The TRT's occupancy is significantly increased in Run 4 [82]. This requires a complete replacement of the tracking system by pixel layers and a strip system. The ATLAS muon spectrometer is mainly upgraded to improve the performance of the muon trigger, which includes new MDT and RPC detectors [83].

4.2.1 New ATLAS Trigger System

While in Phase-1 the L1 trigger rate and latency can be kept the same, this will not be possible during Phase-2, because of the significantly higher instantaneous luminosity. The increased number of interactions per BCs for Run 4 results in a higher number of triggered events. Similar to Phase-1, it is still the goal to keep the p_T threshold at the level of 20 GeV. The solution is a new trigger system for the ATLAS detector [83]. The main new feature is an additional Level-0 (L0) hardware trigger with a latency of 10 μ s and an acceptance rate of 1 MHz. As an alternative it produces a rate of 2 to 4 MHz and is positioned in front of the L1 trigger, whose latency is increased to 30 μ s and rate up to 700 kHz. An overview of the new system can be seen in fig. 4.7.

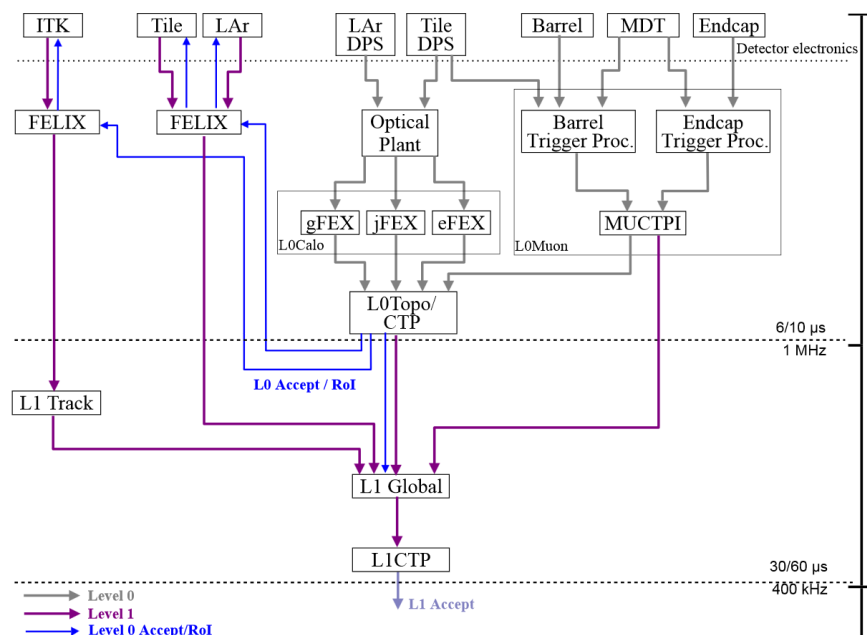


Figure 4.7: Schematic of the ATLAS phase-2 trigger [83]. On the right the latency and trigger rate of the stages is displayed.

The L0 trigger on the upper right side is based on muon and calorimeter data. New components from the MDT and the NSW from Phase-1 will give information to the muon trigger. This information is sent, together with the increased coverage of the RPC triggers, to the Muon Central Trigger Processor (CTP) Interface (MuCTPI). The L0 calorimeter trigger will be largely based on the Phase-1 L1 system (see section 4.1) with three FEXs. Finally, the trigger objects are processed by the topological processor. Here derived quantities, such as scalar sums of jet transverse energies, are used. Similar to the original trigger system, RoI are seeded by L0 to the L1 trigger.

The RoIs are used by the Level-1 Global Trigger (L1Global) and the Level-1 Track

Trigger (L1Track), which searches the Inner Tracker (ITk) for high momentum tracks. The former also has access via FELIX to the L1Track and the L0 muon trigger. In addition, it uses the full granularity of the LAr and Tile calorimeter for these RoIs and reduced granularity for the rest of the calorimeter. As seen in fig. 4.7, the L0 and L1 CTPs collect the trigger elements and distribute the accept signals. The next step is the DAQ system, which uses FELIX to transfer the data to the EF. The front-end electronics, installed during Phase-1, will stay intact, while most of the rest of the electronics needs to be replaced to cope with the higher trigger rate and latency.

4.2.2 Upgraded Readout Electronics

Figure 4.8 displays the LAr readout electronics after the Phase-2 upgrade [36, 84]. The changes from Phase-1, which can be seen in the lower part, stay mostly in place. A new Global Event Trigger Processor (GETP) will be included to provide additional input for the L0 trigger. All calorimeter cells with an energy deposition above a certain threshold will be sent here for topological clustering and additional shower shape information. This will improve jet triggers and increase electron and photon trigger efficiency.

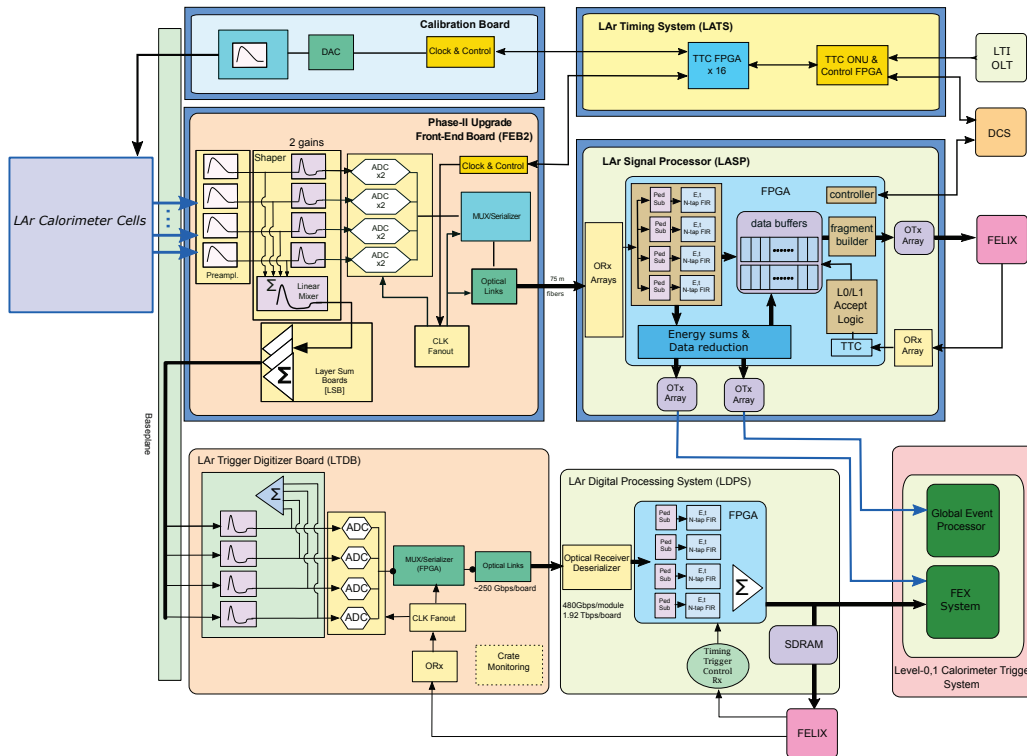


Figure 4.8: Upgraded readout system of the LAr calorimeter for Phase-2. New components have a blue rectangular.

The two new boards for the front-end are the Phase-2 Front-End Board (FEB2) and

a calibration board, which delivers an electronic pulse with precisely known amplitude. As in the original readout, the true triangular pulse is approximated by an exponential pulse (see section 3.3.3). Each FEB2 will handle 128 calorimeter cells, just as a current FEB. The input cable is actively terminated by the preamplifier, and the signal is split into two active linear gain scales ($\times 1$ and $\times 30$), which are called low and high gain, respectively, before it is digitized by an ADC. The two gains are necessary because of the total dynamic range of 16 bits, while the ADCs are restricted to 14 bits. This range is defined on the low end by the Least Significant Bit (LSB), which needs to be below the Minimum Ionizing Particle (MIP) signal for calibration purposes and low noise. The maximum preamplifier current and energy specify the higher end of the range. The usage of only two gains in contrast to three in the original system is justified by the requirement to have the electrons from the Z decay, which are used for calibration, and the photons from the Higgs decay in the same gain scale. This eliminates the systematic uncertainty by imperfect knowledge of the gain intercalibration. Then both gains are digitized by a 14-bit ADC, which consists of two main sections: a Dynamic Range Enhancement (DRE) and a 12-bit Successive Approximation Register (SAR) block. The former is displayed in fig. 4.9 and in front of the latter. The DRE samples the signal in two gain scales ($\times 1$ and $\times 4$) and a comparator chooses which gain is sent to the SAR block. Here, the actual digitization takes place via a binary search through all possible quantization levels. As an alternative, the usage of a Multiplying Digital-to-Analog Converter (MDAC) instead of the DRE is also studied [85]. Afterwards, the high and low gains are serialized and sent to the off detector via optical fibers.

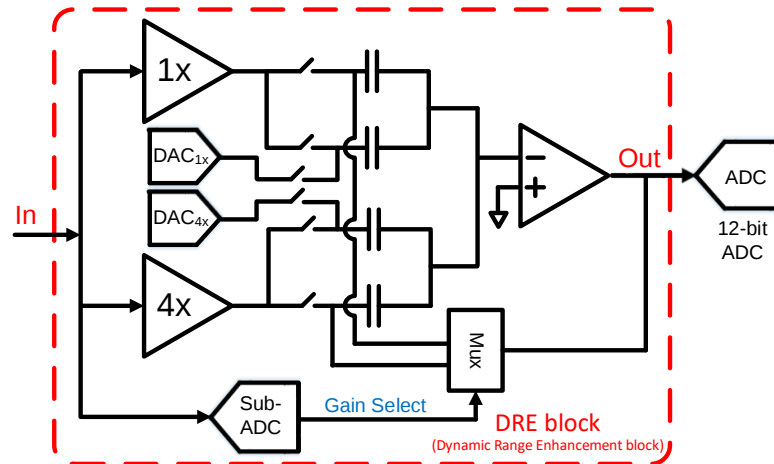


Figure 4.9: Block diagram of the DRE block including the two gains ($\times 1$ and $\times 4$) [60]

In the back-end, there will be a new LAr Signal Processor (LASP) board installed, which is discussed in more detail in the next section. The LASP system will receive the TTC information and provide data to DAQ for the regular detector readout via FELIX. It will also send trigger data to the already mentioned GETP and Super Cell energy sums for the HEC and all FCal energies to the L0 calorimeter FEX system. The

distribution of TTC data to the front-end will be done by a new LAr Timing System (LATS) to separate the functionalities to the LASP system.

4.2.3 LAr Signal Processor

The main functionality of the LASP is the energy reconstruction and time measurement of 512 channels. It incorporates an ALTERA Stratix 10 FPGA [86]. Its firmware and data flow are displayed in fig. 4.10. The Low Level Interface module handles the connection to the outer world. It deserializes, for example, the incoming data from the FEB2 starting the main data flow. The information is then aligned, and the Low Power GigaBit Transceiver (lpGBT) protocol, which is used by the front-end, is decoded in the Input Alignment block. For module testing purposes, a pattern generator can provide special input instead of the regular data. The configurable remapping module reorders data following the detector geometry.

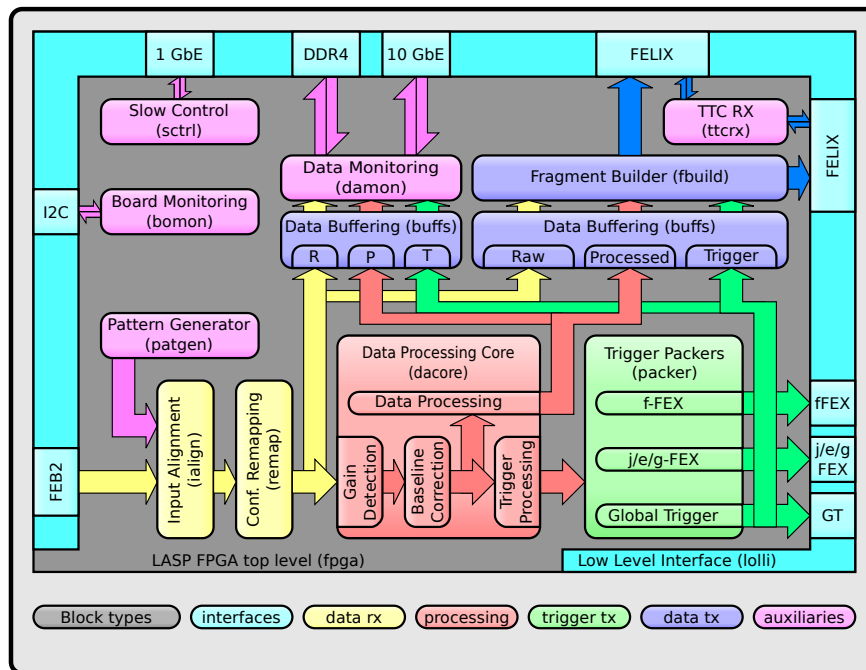


Figure 4.10: Different modules and the data flow of the LASP system

The core functionality is done in the Data Processing Core module. First, the optimal gain is detected, which is selected by applying a threshold to the low gain. Below this value, the preamplifier did not saturate and the high gain is used. Above the threshold, the low gain is used and a timer guarantees, that the preamplifier has time to recover after the saturation, before the high gain is used again. During digitization, a pedestal is used in the ADC to prevent negative values during the undershoot of the pulse. This pedestal is subtracted at the baseline correction step. It is also possible to implement

active pileup correction, which is discussed in more detail in section . Then the data processing takes place, where digital filtering algorithms reduce the effects of electronic and pileup noise. This may be an OF or an advanced machine learning method.

The data for the L0 trigger is then summed to Super Cells for the FEX modules in the Trigger Packers block. In addition, there is a data reduction for the GETP, which only accepts energy values above a certain threshold. This data is then serialized and prepared for transmission in the Low Level Interface. Until the trigger decision is made, the data from different steps of the process is buffered, and only accepted events are sent to the FELIX. Monitoring information can be sent via a 10 Gigabit Ethernet (GbE) for verification of all processing steps or dedicated studies on raw data. FELIX provides the TTC signal for the firmware and a GbE connection is used for the Slow Control block, which monitors and controls the functionality of the separate modules. Some connections are routed via a Rear Transition Module (RTM), which provides most of the optical links.

Chapter 5

Readout Simulation

A realistic simulation is crucial during the research and development phase of the new readout electronics. Section 5.1 gives theoretical background on the topics of pileup noise and OFs. Next, AREUS [87, 88], a tool designed at the TU Dresden, is introduced in section 5.2. Then, it is described how this tool has been extended for the research presented in this thesis. The first research topic was the application of the gain selection, explained in section 5.3. Finally, the baseline shift and a possible active correction were examined.

5.1 LAr Readout Simulation for HL-LHC Conditions

5.1.1 Pileup Noise

Next to electronic noise, pileup noise is one of the two main noise contributions. Pileup are contributions from multiple energy depositions in the same readout channel. This form of noise increases with luminosity and will be the dominant contribution after the Phase-2 upgrade. During Run 4 up to 200 collisions per BC are possible and interesting events with high p_T signatures are likely to be superposed by background events.

There are two different types of pileup: In-time pileup is the deposition of energy by particles from different collisions in the same BC. The filter algorithm of that cell cannot distinguish these energy deposits. In-time pileup is therefore not regarded as noise for the energy reconstruction algorithm, but should rather be handled by later trigger or data processing stages. Another type is out-of-time pileup, which are energy depositions before and right after the actual event. The length of the pulse shape spans over multiple BCs, typically up to 25, and therefore affects near BCs. It deteriorates a precise energy reconstruction and is therefore regarded as noise.

As mentioned in section 3.1, there are 72 consecutive filled bunches in a default batch of the bunch train, followed by a number of empty bunches. Due to the vanishing integral of the bipolar pulse shape, the baseline does not rise continuously after each bunch train,

but has a specific pattern. At the beginning of the 72 filled bunches the baseline rises due to the positive slope of the pulse shape. There is a positive overcompensation of the pileup. After several BCs, the negative contributions of the pulse shapes take effect and the baseline drops again. The baseline stabilizes at the pedestal, when there is a compensation between both contributions. After the 72 bunches, there are no new pileup contributions, which results in a negative overcompensation. A schematic can be seen in fig. 5.1. Only filled bunches are used for the energy deposition measurements. The negative overcompensation can still be observed by the energy reconstruction algorithms, when the number of empty bunches is small enough to influence the measurements of the consecutive bunch train.

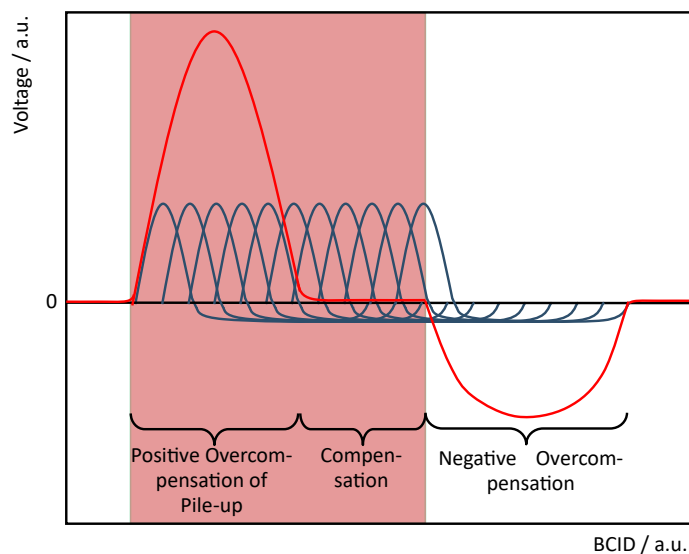


Figure 5.1: Schematic of the baseline shift [89]. The filled bunches are displayed in red. Pileup shapes, drawn in blue, contribute in a positive overcompensation, compensation and finally a negative overcompensation.

5.1.2 Optimal Filter

The LAr back-end readout applies a digital filter algorithm to the ADC samples in order to reduce electronic and pileup noise contributions. The filters will also be adopted to further upgrades of the ATLAS detector. More specifically an OF, based on a Finite Impulse Response (FIR) system is used. FIR filters have an impulse response that returns to zero after a finite time interval [90]. The values of the impulse response are in our case the same as the filter coefficients. Only M most recent input samples are used in forming the output and prior samples are neglected. The calculation of the output sample, $y(n)$, is done by weighting the input samples, $x(n-k)$, with the filter coefficients, a_k , and summing the resulting products:

$$y(n) = \sum_{k=0}^{M-1} a_k x(n-k). \quad (5.1)$$

An OF [91] aims to obtain timing and amplitude information from the calorimeter signal. The filter coefficients are calculated by maximizing the signal-to-noise ratio. The derivation starts with the samples, S_i , of a known signal shape, $g(t)$, but unknown Amplitude, A , time origin, τ , and noise term n_i :

$$S_i = Ag(t_i - \tau) + n_i. \quad (5.2)$$

A Taylor expansion is applied to linearize the dependence on τ :

$$g(t_i - \tau) \approx g(t_i) - \tau \frac{dg}{dt_i} = g_i - \tau g'_i. \quad (5.3)$$

The resulting samples are:

$$S_i = Ag_i - A\tau g'_i + n_i. \quad (5.4)$$

Two FIR filters with coefficients, a_i and b_i , are applied to the samples:

$$u = \sum_i a_i S_i, \quad (5.5)$$

$$v = \sum_i b_i S_i. \quad (5.6)$$

To recover the amplitude, A , and phase shift, τ , the expected value of u is required to be A and the expected value of v to be $A\tau$:

$$A = \langle u \rangle = \sum_i (Aa_i g_i - A\tau a_i g'_i + \langle n_i \rangle), \quad (5.7)$$

$$A\tau = \langle v \rangle = \sum_i (Ab_i g_i - A\tau b_i g'_i + \langle n_i \rangle). \quad (5.8)$$

With the noise averaging to 0, this leads to constraints on a_i and b_i :

$$\sum_i a_i g_i = 1, \quad \sum_i a_i g'_i = 0, \quad (5.9)$$

$$\sum_i b_i g_i = 0, \quad \sum_i b_i g'_i = -1. \quad (5.10)$$

With $R_{ij} = \langle n_i n_j \rangle$ as the noise autocorrelation function evaluated at time $t_i - t_j$, the variances of u and v are given by:

$$\text{Var}(u) = \sum_{ij} a_i a_j R_{ij}, \quad (5.11)$$

$$\text{Var}(v) = \sum_{ij} b_i b_j R_{ij}. \quad (5.12)$$

Using Lagrange multipliers, λ , κ , μ and ρ , to include the constraints of eqs. (5.9) and (5.10), the functions to be minimized are:

$$I_u = \sum_{ij} R_{ij} a_i a_j - \lambda \left(\sum_i a_i g_i - 1 \right) - \kappa \sum_i a_i g'_i, \quad (5.13)$$

$$I_v = \sum_{ij} R_{ij} b_i b_j - \mu \sum_i b_i g_i - \rho \left(\sum_i b_i g'_i + 1 \right). \quad (5.14)$$

The partial derivatives with respect to a_i and b_i are set to 0:

$$\frac{\partial I_u}{\partial a_i} = \sum_j R_{ij} a_j - \lambda g_i - \kappa g'_i = 0, \quad (5.15)$$

$$\frac{\partial I_v}{\partial b_i} = \sum_j R_{ij} b_j - \mu g_i - \rho g'_i = 0. \quad (5.16)$$

This set of linear equations can be expressed in matrix form. The solution for $\mathbf{a} \equiv a_i$ and $\mathbf{b} \equiv b_i$ is:

$$\mathbf{a} = \lambda \mathbf{V} \mathbf{g} + \kappa \mathbf{V} \mathbf{g}', \quad (5.17)$$

$$\mathbf{b} = \mu \mathbf{V} \mathbf{g} + \rho \mathbf{V} \mathbf{g}'. \quad (5.18)$$

The matrix $\mathbf{V}$ is the inverse of the autocorrelation matrix $\mathbf{R} \equiv R_{ij}$. The Lagrange multipliers can be determined from the constraint eqs. (5.9) and (5.10):

$$\mathbf{g}^+ \mathbf{a} = \lambda \mathbf{g}^+ \mathbf{V} \mathbf{g} + \kappa \mathbf{g}^+ \mathbf{V} \mathbf{g}' = 1, \quad (5.19)$$

$$\mathbf{g}'^+ \mathbf{a} = \lambda \mathbf{g}'^+ \mathbf{V} \mathbf{g} + \kappa \mathbf{g}'^+ \mathbf{V} \mathbf{g}' = 0, \quad (5.20)$$

$$\mathbf{g}^+ \mathbf{b} = \mu \mathbf{g}^+ \mathbf{V} \mathbf{g} + \rho \mathbf{g}^+ \mathbf{V} \mathbf{g}' = 0, \quad (5.21)$$

$$\mathbf{g}'^+ \mathbf{b} = \mu \mathbf{g}'^+ \mathbf{V} \mathbf{g} + \rho \mathbf{g}'^+ \mathbf{V} \mathbf{g}' = -1. \quad (5.22)$$

The solution is:

$$\lambda = \frac{Q_2}{\Delta}, \quad \kappa = \frac{-Q_3}{\Delta}, \quad (5.23)$$

$$\mu = \frac{Q_3}{\Delta}, \quad \rho = \frac{-Q_1}{\Delta}, \quad (5.24)$$

with use of the following matrix abbreviations:

$$Q_1 = \mathbf{g}^+ \mathbf{V} \mathbf{g}, \quad (5.25)$$

$$Q_2 = \mathbf{g}'^+ \mathbf{V} \mathbf{g}', \quad (5.26)$$

$$Q_3 = \mathbf{g}'^+ \mathbf{V} \mathbf{g}, \quad (5.27)$$

$$\Delta = Q_1 Q_2 - Q_3^2. \quad (5.28)$$

This shows that by measuring the autocorrelation matrix, $\mathbf{R}$, and by using the known pulse shape, $\mathbf{g}$, the filter coefficients, a_i and b_i , can be calculated.

5.2 AREUS

ATLAS Readout Electronics Upgrade Simulation (AREUS) is a hardware simulation program, which was created to perform detailed design studies for the detector upgrade. It provides a flexible simulation of the trigger readout electronics of the ATLAS LAr calorimeter. In contrast to the ATLAS physics simulation framework ATHENA [92], which works in a triggered mode, AREUS provides samples continuously [93]. A specific artificial sequence of energy depositions or ATLAS Monte Carlo (MC) samples [94] function as input. The latter are created by MC event generators, which use random numbers to simulate high-energy collisions. The mapping of the calorimeter cells, pulse shapes, noise and ADC characteristics are included in AREUS. There are different digital

signal processing algorithms for energy and time reconstruction available. The software provides final and intermediate results as output to evaluate the performance of these algorithms.

The program is written in C++ and designed in a strictly modular manner and the subject–observer pattern. Each module can act as a subject, which means that it runs algorithms and sends data to other modules acting as observers. The observers then again can act as subjects and thus create a chain of modules including generic interfaces. A factory creates one or more modules of a certain type and also takes care of the configuration and connection to the subject. A visualization can be seen in fig. 5.2. The parameters of each object are specified in XML files.

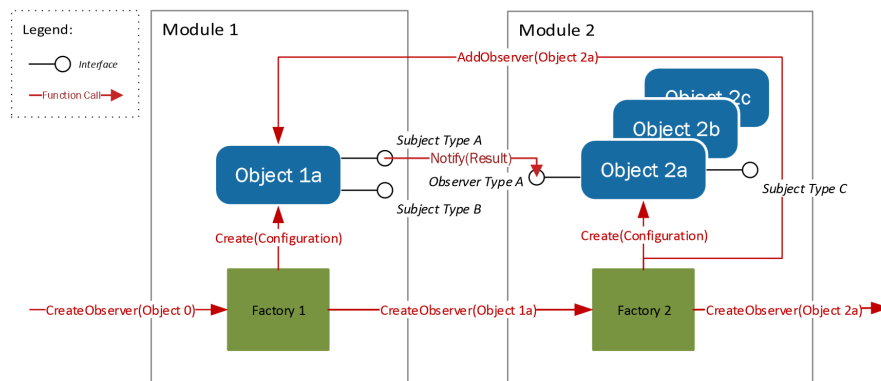


Figure 5.2: Working principle of the AREUS modular design [87]. Each module can act as subject and observer and is created by a factory.

5.2.1 Existing Modules

There are two possible modules to start a simulation: the `Lar_test` cell module and the `Event_loop` module. The former simulates a single LAr cell and reads a simple hit sequence, which is directly forwarded to the `Lar_digitization` module. The latter represents the LHC clock and only generates a global BCID with filled or empty BCs. It is activated by one or more `Hit_sample` modules, which use MC samples to determine the ATLAS coordinates of a particle hit and its deposited energy. Multiple modules are needed for separate signal and pileup MC samples. All of them are activated by the `Lar_cell_map` module, which combines them to the corresponding LAr calorimeter cell before they are directed to the `Lar_super_cell_map` module. For Phase-1 studies the calorimeter cells were summed to Super Cells, which is not necessary for Phase-2 studies. The module is still needed to convert the data type before the signal is finally directed to the `Lar_digitization` module.

The `Lar_digitization` module simulates the response of the front-end readout electronics and combines multiple functionalities. First, the hit is converted to a bipolar pulse shape corresponding to the analog signal of the real readout after the shaper. It

is possible to configure the module to calculate the pulse shape via an analytical formula [95] or to use a database obtained by SPICE [96]. In the database, multiple pulse shapes can be added for the same cell with different associated energies. Depending on the hit energy, a pulse shape is calculated and scaled from this database. Another input for this module is a noise database. The correct noise distribution is selected from the database and added to the signal. Finally, the pulse is sampled by an ADC with configurable width, LSB in units of energy, Effective Number of Bits (ENOB) and pedestal.

The **Lar_filter** module incorporates several possible signal processing algorithms, which can be chosen via its type. An important one is the OF (see section 5.1.2) with a configurable filter depth. Usually, the first 1000 BCs of the simulation are used to train the filter. This means the readout of the ideal pulse shape and the evaluation of the autocorrelation (see section 5.1.2). After the OF, another type of the **Lar_filter** module can be added: the maximum finder. It detects the maximum out of a sequence of three consecutive inputs, and outputs the sample if it is above a given threshold and zero. Finally, there are two important output modules: **Lar_filter_analysis** and **Ntuple_maker**. The former creates several histograms to check the filter performance and the latter generates files containing all simulated data, which can be used for further analysis.

5.2.2 New and Revised Modules

Several changes of AREUS had to be conducted to enable the studies of the gain selection. The **Lar_digitalg_muxer** module already existed, but was only able to multiplex several filters from the same digitization module. The updated version can now merge readout chains from multiple digitization modules, which represent the different gains. It takes different LSBs and pedestals into account. The decision, which readout chain to forward, is made sample by sample and is based on the priority value of the data. The values themselves are arbitrary, but only the readout chain with the highest priority is forwarded.

The priority values are generated by the saturation filter, which is a type of the **Lar_filter** module. The value is usually set to the default priority and, if saturation is detected, the it is set to the saturation priority. Both of these are configurable. For example, a **Lar_digitalg_muxer** module needs to multiplex between a high and low gain chain. The **Lar_filter** of the low gain always sends the priority value 1. As long as no saturation is detected, the saturation filter of the high gain chain sends 2, because this is set as its default priority. Therefore, the multiplexer forwards the samples from the high gain chain, because they have a higher priority. If the saturation filter detects a saturation of the high gain, it sets the priority of the samples to 0, which is the configured saturation priority. This results in the forwarding of the samples from the low gain chain, because now the low gain has a higher priority compared to the high gain.

The saturation detection is done by comparing the input to a threshold. The threshold is set relative to the full scale minus the pedestal. In addition, it is possible to keep this saturated state for the duration of the whole pulse or to apply the check at every BC. Finally, a buffer can be enabled, which delays the output. If the saturation is detected in the peak sample, this would allow the declaration of pre-peak samples as saturated a posteriori.

Another type of the `Lar_filter` module has been developed: `Fir_sets`. It basically works like an OF, but it has two sets of coefficients, which are selected based on the priority of the samples. If the priority value is above a configurable threshold, the first set of coefficients is used. Otherwise, the filter utilizes the second set of coefficients for the response calculations. The training of the coefficients needs to be done beforehand so that the resulting values can be added in the configuration of the module. This new filter type could be replaced by using two OFs, which get the same input, and a multiplexer to combine the results into one chain. This would necessitate a new method to determine, which of the two results should be forwarded to the next module. The development of `Fir_sets` simplifies this by combining all of these modules into one `Lar_filter`.

5.3 Gain Selection

Two 14-bit ADCs are necessary to cover the required 16-bit range of the readout. At some point on the readout chain, the decision, which gain is forwarded to the DAQ, has to be made. The baseline solution is to implement this gain selection in the firmware of the LASP board in the back-end, which is discussed first in this section. Another possibility is to locate it in the front-end, which would greatly decrease the number of cables from the detector to the back-end since only one gain would be sent. This would in turn have other disadvantages explained later in this section.

5.3.1 Back-end solution

To verify the functionality of the new and revised modules, the simulation of the relative resolution of the LAr calorimeter as a function of deposited energy, shown in fig. 5.3, has been replicated with AREUS. The electronic noise contribution should always be negligible compared to the intrinsic resolution of the calorimeter, which is displayed as a black curve in fig. 5.3. The whole energy range is divided into two gain channels, which differ in the scale used by the preamplifier. In the simulation, the high gain uses an LSB of 11.3 MeV, which was adopted in the AREUS setup. This is a possible value and not the final specification. It was chosen, that the high gain is amplified 30 times more than the low gain. Therefore, the ADC of the high gain has a smaller LSB value and consequently has a better resolution than the ADC of the low gain. Overall, the relative resolution decreases with increasing energy until the upper end of the range is reached and the next gain is chosen. Each gain has an additional abrupt change of resolution observable as an edge in the distribution at the values 40 GeV and 1 TeV. These arise

from the DRE inside the ADC, which is explained in section 4.2.2. It uses two gains ($\times 1$ and $\times 4$) to increase the range from 12 to 14 bits.

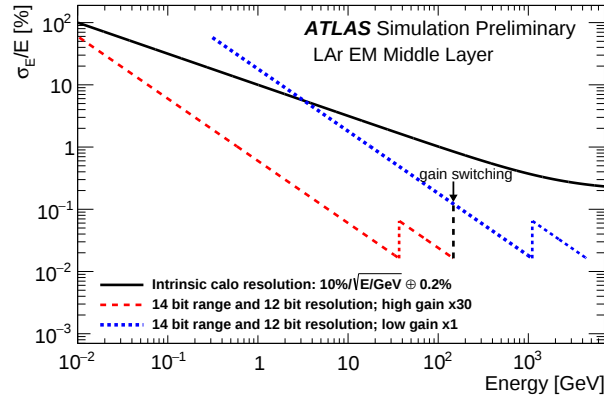


Figure 5.3: Simulation of the relative energy resolution of the ATLAS LAr calorimeter [97]. It shows the intrinsic calorimeter resolution and the resolution of the two ADC gains. The gain switching is indicated by a sharp rise of the graphs.

The representation of an ADC in AREUS can be seen in fig. 5.4. It consists of two digitization modules containing the same noise and pulse shape databases, which were both generated by SPICE. The pulse shapes of one digitization module were multiplied by a factor of four to account for the higher gain DRE stage inside the ADC. Therefore, it also has a four times lower LSB than the other module, which also results in a better resolution. The setup of two saturation filters and the `Lar_digital_muxer` module is similar to the example about the priority from an earlier section. The saturation filter in the low gain chain always generates a priority value of 1 and does not check for any saturation in the low gain samples. The high gain saturation filter has a default priority of 2 and lowers it to 0, if a saturation occurs. Therefore, in the default mode, the multiplexer, which is depicted as `Muxer` in the schematic, transmits the high gain samples to the following modules. If the high gain saturates, the low gain samples have a higher priority and are transmitted by the multiplexer. For an accurate representation of the ADC, the relative saturation threshold is set to 1, which means that saturation is only detected, if the high gain sample has the maximal possible value. For the same reason, if saturation is detected, the filter checks the next sample again and does not stay saturated for the length of the pulse. This setup of two digitization modules, two saturation filters and a multiplexer is depicted as `ADC` in the following schematics.

Figure 5.5 displays the order of the modules of AREUS to generate the resolution distribution. The simulation starts with the `test_sequence` module, which activates a detector cell in the middle layer in the EMB at the coordinates $\eta = 0.5125$ and $\phi = 0.125$. Energy signatures, called input energy, are injected repeatedly into the subsequent modules. The hits have enough BCs between them to avoid overlay. The whole energy

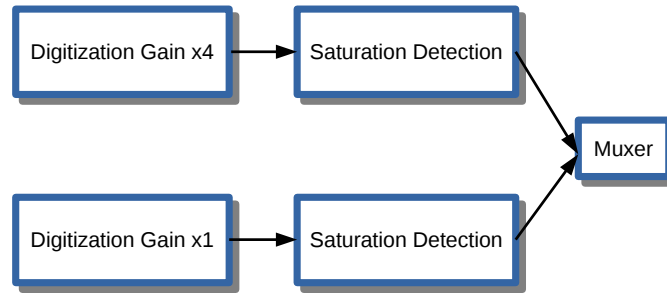


Figure 5.4: Schematic of the ADC representation in AREUS. Two digitization modules simulate the two gains inside the ADC. The multiplexer receives the priority of the data from the saturation detection.

range up to 3 TeV is covered in 10 GeV steps and each value is repeated 200 times to reduce statistic uncertainties. Four digitization modules, representing the high and low gain ADCs, receive the energy information from the `test_sequence` module. There are specific noise and pulse shape databases for high and low gain, which were generated by simulations of the Liquid Argon Upgrade Read-Out Chip 0 (LAUROC0) [98]. The configuration of the digitization modules for the middle layer can be seen in table 5.1. The setup of the saturation filter and `Lar_digital_muxer` modules, which represent the ADC, is the same as mentioned before.

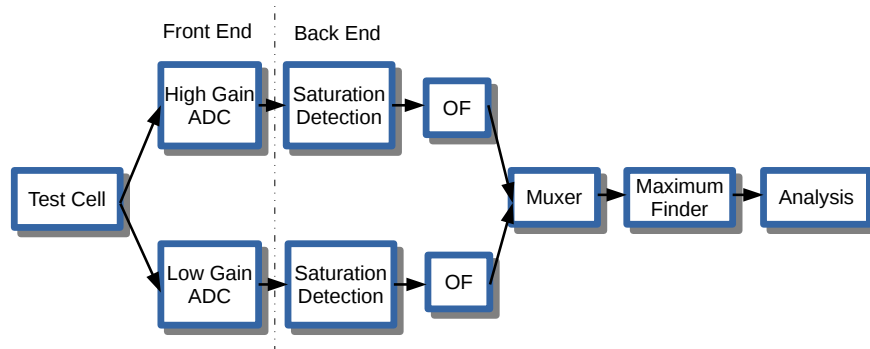


Figure 5.5: Schematic of the simulation chain for the gain selection in the back-end in AREUS

The following modules simulate the back-end of the LAr readout. Each multiplexer from the ADC setup transmits data to a saturation filter, which have a different configuration compared to the ones inside the ADC setup. The actual saturation detection takes place in the low gain readout chain, because otherwise saturation effects in the high gain chain could influence the result. Therefore, the low gain saturation filter module has a default priority of 0 and as soon as the saturation threshold is reached, the priority is set to 2. The relative saturation threshold is set to 0.03, because this translates to 0.9 in the high gain chain, which is the current design choice. This value is not fixed and

	LSB [MeV]		Pulse Shape
High Gain x 4	11.3		high_gain_shapes_x4
High Gain x 1	45.2	x4	high_gain_shapes
Low Gain x 4	339	x30	low_gain_shapes_x4
Low Gain x 1	1356	x4 x30	low_gain_shapes

Table 5.1: Configuration of the four digitization modules. This contains the used pulse shapes and the LSB including the relation to the first module. The smallest LSB was provided by Sergey Peleganchuk and is not the final value. The other LSBs are calculated from the factors between the gain stages.

may change in the future. In addition, the saturated mode is kept for the duration of a whole pulse width. The next module in each readout chain is an OFs, which was trained on pulse shapes of their corresponding gain using 1000 BCs. After the filter algorithm, one `Lar_digialg_muxer` module decides if high or low gain should be forwarded. A maximum finder filter module passes only peaks in the reconstructed energy. Finally, the analysis receives these output energies and generates multiple histograms.

The histogram of the relative resolution is displayed in fig. 5.6. Each bar represents one of the energy values and has a width of 10 GeV. The distribution clearly shows the three gain switching edges at energies similar to the first simulation, and the resolution is also on the same order of magnitude. A difference can be seen in the final gain switching at higher energies. There is not one single edge but rather several plateaus, which are not visible in the peak of the primary gain switch. The difference arises from the different configurations of the saturation filters. In the gain switching of the DRE inside the ADC the saturation filters are not kept in the saturated state for the duration of the pulse, which can lead to a gain mixing between different gains inside the OF. The five samples used for the filter calculation can partly originate from a higher gain. These samples have a better resolution, which also has an effect on the result. There are multiple plateaus for the different possible combination of samples.

With the verification of the functionality of the new modules beeing successful, the gain selection study could be started. Figure 5.7 shows the energy correlation if the gain selection is performed by the off-detector electronics. The energy is correctly reconstructed on the whole energy range. The distribution shows that this baseline solution is a safe and reliable way to determine the correct value since the relative difference is close to zero for the whole energy range.

5.3.2 Front-end solution

A slightly different setup of modules, shown in fig. 5.8, has been used to test a gain selection location at the front-end. The test sequence module and the two ADC simulation blocks are identical to the setup in fig. 5.5. The different is that the `Lar_digialg_muxer`

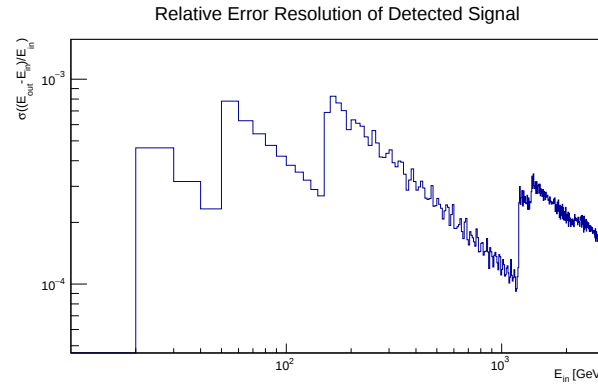


Figure 5.6: Relative energy resolution of the ATLAS LAr calorimeter received from AREUS. The sharp rises indicate the switching of gains. At 150 GeV there is the main switch between high and low gain, while the other two are due to the intrinsic setup of the ADC.

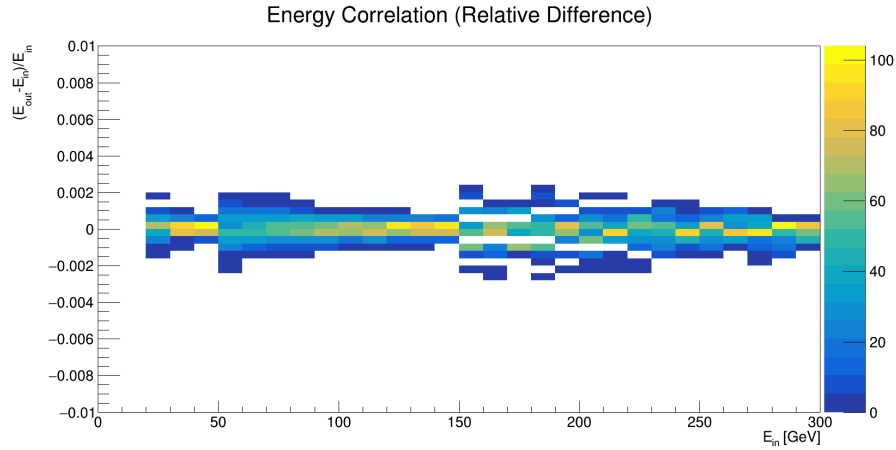


Figure 5.7: Relative energy correlation if the gain selection is performed in the back-end electronics. It shows the relative difference between input and output energy on the y-axis, and the input energy on the x-axis. The energy is correctly reconstructed on average and the different gain switches can be seen due to the width of the distribution.

module is located earlier in the readout chain, which simulates the fact that only one gain is transmitted to the back-end. Therefore only one OF instead of two are used, because filtering is still done in the back-end. This OF uses coefficients, which are trained by high gain pulse shapes. All displayed modules have the same configuration as in the other setup.

Figure 5.9 shows the results if the gain selection is done in the front-end electronics, analog to fig. 5.7. In contrast, this graph is clearly split into three sections depending on

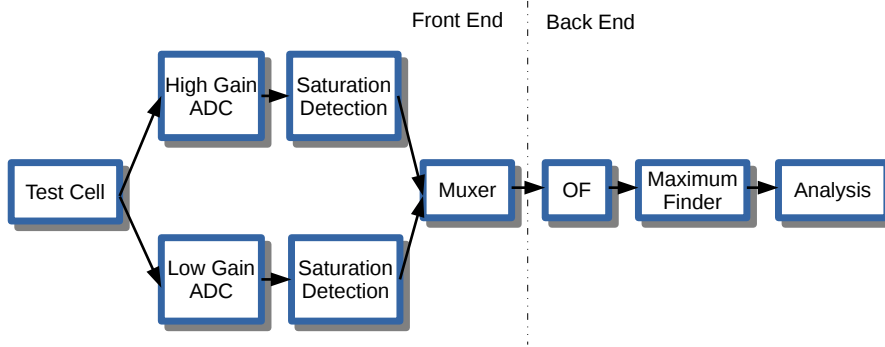


Figure 5.8: Schematic of the simulation chain for the gain selection in the front-end in AREUS. The test cell starts the chain, and there are two ADCs for the two gains and the gain selection in the front-end. The back-end contains one OFs.

the input energy. At lower energies, the setup works as intended and the resolution is similar to the baseline solution. Since no gain switching takes place, the single OF only processes high gain pulse shapes, which were also used to train the filter coefficients. In the range from 150 GeV to 220 GeV, the energy deviations from zero are the highest. At these energies, saturation of the preamplifier takes place and low gain samples are used for the filter calculation. The energy is not high enough to detect the saturation of the pulse immediately. This results in a mixing of high and low gain samples. Therefore two different pulse shapes in the OF calculation causes the particularly strong difference. Energies above 220 GeV show a better average error, but are still not reconstructed correctly. In this range, the saturation is detected soon enough to minimize the gain mixing to one sample. However, there is still the problem that the OF is trained on high gain pulse shapes, but only samples from low gain pulses are received.

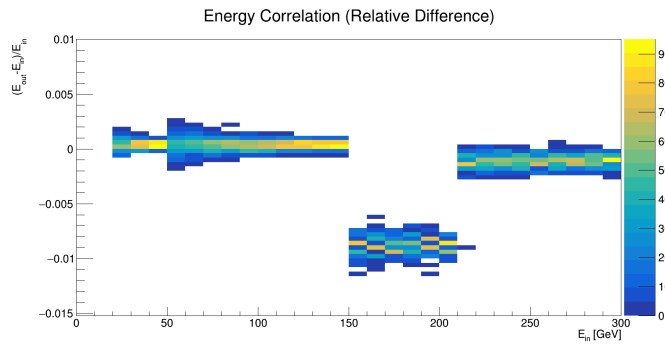


Figure 5.9: Relative energy correlation if the gain selection is performed in the front-end electronics. It shows the relative difference between input and output energy on the y-axis, and the input energy on the x-axis. The energy is correctly reconstructed until 150 GeV. At higher energies, gain mixing and filter training with the wrong pulse shapes results in a deviation of the reconstruction from the input value.

The gain mixing problem could be solved by sending low gain samples to the back-end before the saturation is detected. This can be implemented by using a buffer in front of the gain selection. If saturation is detected, the samples in the buffer of the low gain are read out. This results in an additional latency in the readout chain. In AREUS, this is realized by a buffer inside the saturation filter, which stores the data of the low gain chain for a configurable amount of BCs. After detection of the saturation, samples of the low gain channel inside the buffer can be forwarded. Therefore, the gain switching effectively happens before the saturation detection, and the OF exclusively uses samples from one of the two gains for the calculation. Figure 5.10 shows the resulting distribution, which otherwise uses the same module setup as before. The buffer length is set to one or two BCs respectively and reduces the relative difference between the input and output energy.

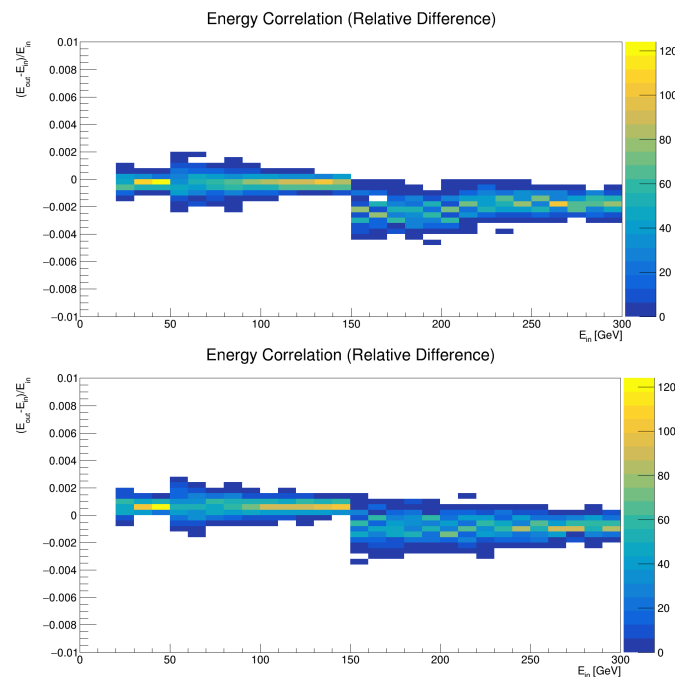


Figure 5.10: Relative energy correlation if the gain selection is performed in the front-end electronics. A buffer of length 1 (top) and 2 (bottom) has been used to avoid gain mixing. It shows the relative difference between input and output energy on the y-axis, and the input energy on the x-axis. The inclusion of a buffer improved the energy reconstruction.

For energies above 150 GeV, the bias in the reconstruction error is caused because the OF is trained on high gain pulse shapes but applied to low gain pulses. The application of the filter coefficients to low gain pulse shapes does not give the desired results. As a solution, two OFs could be used instead of one. They both get the same input from the front-end, but they have different coefficients. One filter is trained with high gain

pulse shapes and the other with low gain pulse shapes. In AREUS, the new `lar_filter` module type `fir_sets` can be used instead of multiple OF modules. It uses two sets of coefficients instead of one. These sets need to be included via configuration and cannot be trained in the same simulation. The second set can be trained by low gain pulse shapes and a priority threshold decides which set of coefficients are used. Figure 5.11 shows the result with different values for the buffer parameter and is now very similar to the baseline solution.

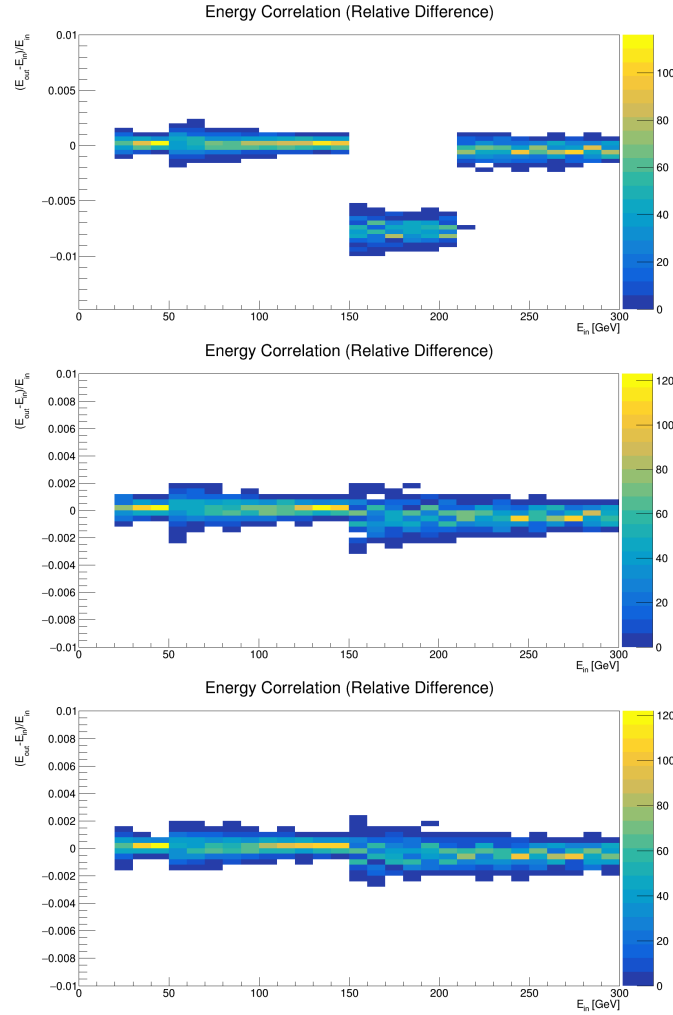


Figure 5.11: Relative energy correlation if the gain selection is performed in the front-end electronics. An additional set of filter coefficients was used to improve the reconstruction of higher energies. A buffer of length 1 (middle) and 2 (bottom) has been used to avoid gain mixing, but was not included in the upper graph. It shows the relative difference between input and output energy on the y-axis, and the input energy on the x-axis. The upper graph does not use a buffer and shows therefore effects of gain mixing. The other graphs use a buffer with the length of 1 and 2 BCs, respectively.

This shows that with a few changes, a gain selection in the front-end is a possible alternative to the back-end model. Its implementation would reduce cost by requiring fewer cables between the front-end and back-end because only one gain is forwarded. The changes in the firmware of the back-end FPGA is minimal, because the effective number of OFs does not change. However, the usage of buffers in the front-end would increase the latency by two BCs. The next section investigates if the new setup can apply baseline correction algorithms similar to the baseline solution.

5.3.3 Baseline Correction

Pileup results in a baseline shift, which is explained in section 5.1.1. This source of bias can be reduced by introducing an active baseline correction algorithm. The baseline correction can only be executed on the firmware in the back-end. Low gain samples are only forwarded to the back-end, when the high gain preamplifier is saturated. Therefore, the baseline of the low gain is not known. The following study investigates if baseline correction is still possible for both gains under these circumstances.

The AREUS setup for this study is shown in fig. 5.12. Instead of a simple test sequence of energies, a more sophisticated setup is needed to include the pileup events. The energy information of these events is sent to the ADCs and the resulting samples are stored for further analysis. For the baseline studies, no OF or gain selection is necessary, because the baseline correction would take place at the level of ADC values before the OF.

AREUS uses two files, which are the result of simulations by GEANT4 [99]. They contain the energy deposition in the detector from low p_T and a high p_T pileup events, respectively. These events were generated by Pythia8 [100]. The high p_T pileup events contribute to 0.1 percent of the mean number of collisions, $\mu = 200$. Other energy signals apart from pileup are not needed for baseline studies. A specific detector cell in the EMB at the coordinates $\eta = 0.5125$ and $\phi = 0.125$, which was also used in the previous study, is assigned. The module structure, which represents the high and low gain ADCs, is identical to the previous setup. In the `ntuple_maker` module, the data is written to a root file.

All samples of a specific bunch position in the bunch train structure are averaged to improve statistics. This is done for all positions from BC 1 to 72. The result can be seen in fig. 5.13. It shows the energy over the bunch train position. The positive overcompensation up to 75 MeV at the beginning and compensation at the position 20 can be seen. Both low and high gain are pictured and their difference is shown in the lower graph. The disagreement arises from the dissimilar pulse shapes of the two gains. The high gain has a stronger overcompensation and compensates at a lower energy than the low gain. Nevertheless, the difference is only a few MeV. This shows, that the baselines of high and low gain are very similar.

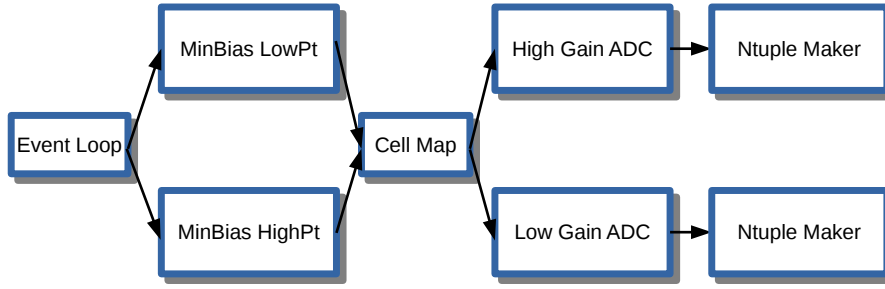


Figure 5.12: Schematic of the simulation chain for the baseline studies in AREUS. The event loop starts the chain. Pileup samples are fed into the cell map. There are two ADCs for the two gains and they are written into ntuples.

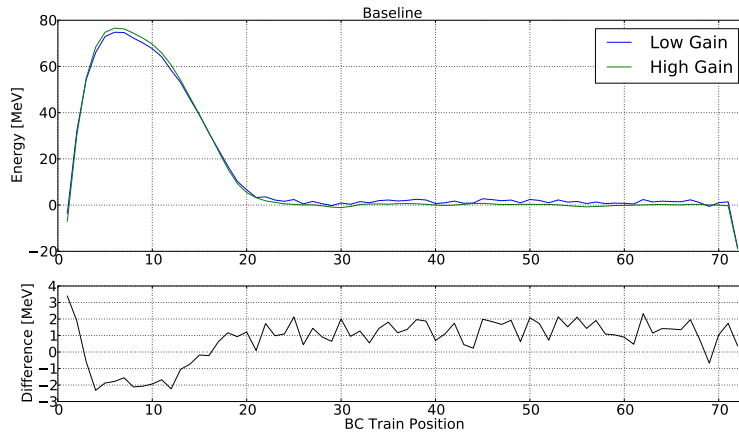


Figure 5.13: Baseline shift of the low and high gain and their difference for the EMB

Figure 5.14 shows the same graph for a different detector position. A calorimeter cell in the EMEC at $\eta = 2.0$ and $\phi = 0.125$ was chosen. This region is closer to the forward direction and therefore has more pileup noise. The positive overcompensation reaches a maximum value of 340 MeV for the low gain. The energy difference between the two gains is greater, up to 100 MeV.

It is important to keep in mind that the LSB of the low gain is 339 MeV, while the value is 11.3 MeV for the high gain (see table 5.1). This indicates that a baseline correction for the low gain is not needed, since the maximum baseline shift might not be resolved. Alternatively, it is also possible to use the high gain samples for the baseline correction of the low gain. The difference between the baseline shifts of the gains is small, even if the pulse shapes would have a stronger disagreement in the actual readout.

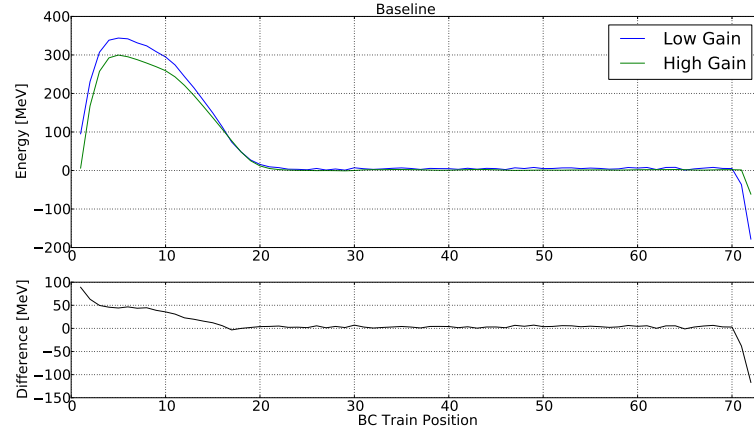


Figure 5.14: Baseline shift of the low and high gain and their difference for the EMEC

5.4 Conclusion

These studies show that gain selection in the front-end is possible. Negative effects like gain mixing and insufficient training of the OF can be compensated by increasing the latency by 2 BCs. In addition, the low gain baseline shift has only a small influence on the data and can be corrected by a calculation based on the high gain's baseline shift.

Unfortunately one issue that remains is the transition from low to high gain at the end of the saturation window. A mixing of samples in the OF at this moment cannot be avoided and will deteriorate the energy resolution. Since the saturation duration of the preamplifier depends on the input energy, it is also not clear at which point this switch should occur. Therefore, it is very likely that no gain selection will be implemented in the front-end electronics.

Chapter 6

Introduction to the Hardware Development

The hardware development of the ATLAS LAr readout is in an important phase: final design decisions will need to be made on the basis of prototypes, which shall function as realistically as possible. In this thesis, central features of the LAr signal processing are developed. Section 6.1 serves as an introduction to FPGAs, which are used in the back-end electronics of the calorimeter. Their configuration via the programming language Very High Speed Integrated Circuit Hardware Description Language (VHDL) is discussed in section 6.2. Finally, the development environment of ABBA and LASP is explained in section 6.3.1 and section 6.3.2, respectively.

6.1 FPGA

During the Phase-I and Phase-II detector upgrades, numerous new FPGAs will be installed in the back-end to take over a central part of the readout, namely the reception of the detector data, the digital signal processing and the sending of data to the trigger and data acquisition systems.. A FPGA is an integrated circuit mainly consisting of input and output ports, logic blocks and the interconnections between them. A simple version of a logic block contains a Lookup Table (LUT) to implement logical functions and a Flip Flop (FF) to store data. An exemplary presentation is displayed in fig. 6.1. During configuration, the results of specific functions are stored in a LUT, whereas and in operation they can be retrieved very quickly. The FF is a memory element controlled via the clock signal, which switches between one and zero with a specific frequency resulting in a fixed latency for operations inside the FPGA.

In contrast to a processor, which executes commands successively, an FPGA is a programmable electronic circuit. It can perform multiple tasks in parallel resulting in the usage of FPGAs in image processing or cryptography. It is also well suited for detector readout, because its huge bandwidth allows fast processing of a large number

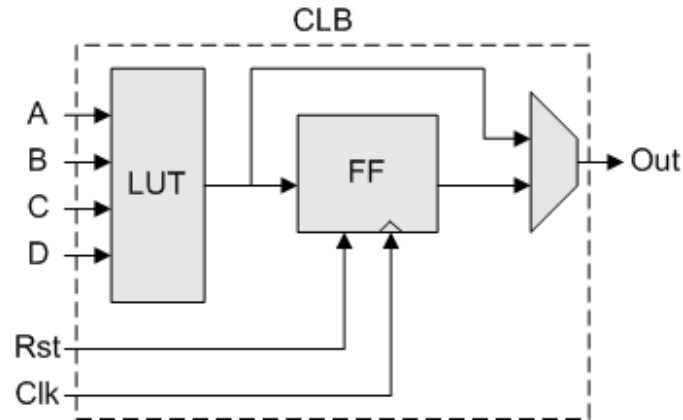


Figure 6.1: Setup of a simple Configurable Logic Block (CLB) [101]. There are four inputs to the LUT. Its output can be buffered in an FF, which is controlled by a clock and a reset signal.

of channels.

The previously mentioned interconnections can be reconfigured by applying a voltage. A representation can be seen in fig. 6.2. This technique provides a fast and easy way to implement new features and to correct errors. The configuration is done via a Hardware Description Language (HDL), which is discussed in section 6.2.

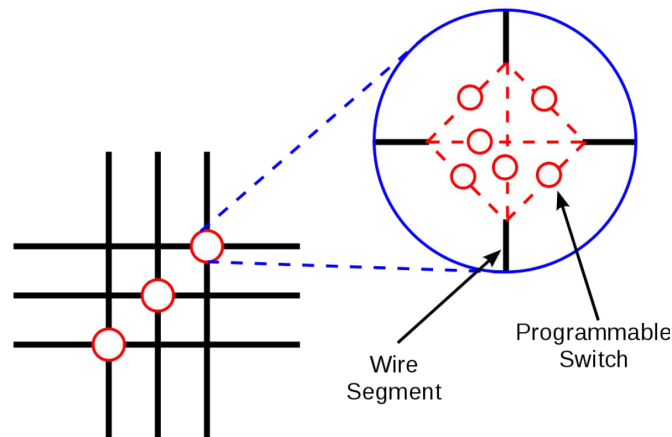


Figure 6.2: Sketch of a programmable switch of an FPGA [102]. The configuration is done by applying a voltage. The wires are connected to logic blocks, ports or registers.

The FPGA holds common and complex embedded functions hard-coded on the device. This is faster and more resource efficient than configuring a large number of logic blocks. This includes additional memory blocks, DSPs for multiplication and serializers/deserializers for transceivers.

Disadvantages of FPGAs are the high power consumption and low radiation resistance. The latter is the reason for the usage of ASICs in the front-end closer to the detector. In contrast, these are not programmable after manufacturing, but less susceptible to radiation.

6.2 VHDL

The configuration of an FPGA is done via the programming language VHDL. It describes the operation of the logical circuit in text models. The design tool Quartus Prime [103] by the vendor Intel is used here for compilation and to program the FPGA. First, the written code is tested for syntax errors and hardware compatibility. Then, the design is implemented in three subprocesses: "Translate", "Map" and "Place and Route". The VHDL text is converted into the logic blocks of the FPGA and interconnected according to its functionality. Finally, a bit file is generated, which is uploaded onto the FPGA and makes it ready for operation. It is also possible to simulate the VHDL code first to verify the functionality.

Each VHDL file is divided into three parts, visible in listing 6.1. The important keywords are displayed in blue and comments in green starting with `--`. First, the necessary libraries are listed, which include `std_logic_1164`. It provides the important data type `std_logic` with the possible values of 0 and 1. Among others, it can also hold U for undefined and X for unknown, which plays a role in simulation. The second part is the definition of the entity or module. There should only be one entity per file. The interface to the outer world can be defined in this part with two keywords: `generics` give the possibility to configure the module and can be compared to global variables from other languages; `port` lists all input and output connections.

```
1 library IEEE;
2 use IEEE.std_logic_1164.all;
3 -- additional libraries are included here
4
5 entity example is
6     -- generics can be defined here
7     port (
8         -- input and output are defined here
9         input1 : in  std_logic;
10        input2 : in  std_logic;
11        output  : out std_logic := '0'
12    );
13 end entity;
14
15 architecture arch of example is
```

```

16  -- internal signals are declared here
17  signal internal : std_logic := '0';
18  begin
19  -- functionality of the module is described here
20  internal <= input1 and input2;
21  output <= not internal;
22  end arch;

```

Listing 6.1: This code shows a basic VHDL file. The three parts library inclusion, entity declaration and architecture definition are visible. Generics are not needed in this entity and are therefore omitted.

The last part is the architecture, where additional internal signals can be declared and the actual functionality is implemented. The signals on the right can be combined with logical operations and assigned via `<=` to the signal on the left. At this point, the order of the assignments is not important, and they are not executed in the usual programming sense. It is rather a definition on how the input and output ports are connected internally at all times. If the input changes at any point the output changes almost instantly as well.

Listing 6.2 shows additional common data types and their conversion. The `boolean` type, which can have the values `true` or `false`, is used for condition and relational operators. The `std_logic_vector` is an array of `std_logics`, but it does not represent a number. This can only be achieved by including the `numeric_std` library and defining an `unsigned` or `signed`. The latter can also describe negative numbers by applying a negative sign to the numeric representation of the highest bit. Other data types for calculations are `integer`, `natural` and `positive`. The difference between the last two is that `natural` also contains zero as a possible value. A conversion between `integer` and `std_logic_vector` is only accomplished via the `unsigned` or `signed` data type.

```

1  -- Data types
2  signal E1      : boolean := false;
3
4  signal A_std   : std_logic_vector(6 downto 0) := (others => '0');
5
6  signal B_uns   : unsigned(2 downto 0) := "110"; -- = 6  (4 + 2)
7  signal C_sig   : signed(2 downto 0) := "110";   -- = -2 (-4 + 2)
8
9  signal D1      : integer := -2;
10 signal D2      : natural := 0;
11 signal D_int    : integer range 5 to 100 := 7;
12
13 -- Conversions

```

```

14 A_std <= std_logic_vector(B_uns);
15 A_std <= std_logic_vector(C_sig);
16 B_uns <= unsigned(A_std);
17 C_sig <= signed(A_std);
18
19 D_int <= to_integer(B_uns);
20 D_int <= to_integer(C_sig);
21 B_uns <= to_unsigned(D_int,bit_width);
22 C_sig <= to_signed(D_int,bit_width);

```

Listing 6.2: Several data types and conversions

Other options to be included in the architecture section and their keywords are displayed in listing 6.3. There are two possibilities to implement conditional signal assignment. The **when/ else** assigns the value corresponding to the first true condition, and **with/ select** assigns the value by comparing selection with the different choice values. It is also possible to define a loop via **generate**, which creates the enclosing code multiple times. An important aid is the **process** keyword, which operates procedural and is preceded by event control. If a signal in the sensitivity list, usually a clock, changes, the sequential statements are executed. Inside, if conditions, case assignments and loops are defined similar to procedural computing languages. There is also the option to reuse a module in another entity by mapping the generics and ports. Finally, it is also possible to reuse modules, so called Intellectual Property (IP) cores, from other parties. This includes memory blocks, transceivers and DSPs.

```

1  output1 <= input1 when cond1 else
2      input2 when cond2 else
3      input3;
4
5  with internal select
6      output2 <= input1 when choice1,
7                  input2 when choice2,
8                  input3 when others;
9
10 generate_label: for i in 3 downto 0 generate
11     matrix_s(i)(4 downto 0) <= internal;
12 end generate;
13
14 process_label: process(sensitivity list)
15 begin
16     -- sequential statements
17 end process process_label;

```

```
18  
19 map_label: entity other_module  
20 generic map(  
21     invert => true  
22 )  
23 port map(  
24     input  => A,  
25     output => B  
26 );
```

Listing 6.3: Additional keywords for signal processing inside the architecture section

6.3 Development Environment

A development environment for designing VHDL projects is provided by Intel in form of the Quartus Prime software. Quartus Prime contains useful tools for simulation and compilation of the VHDL code. The software can be operated via a GUI or the command line. For a large project with multiple developers, it is recommended to use the distributed version control system Git [104]. To manage the numerous files and their dependencies, Quartus Prime is not sufficient. Therefore, a new development environment, `hdl_env`, which is based on `hdlmake` [105], was designed for the Phase-1 LDPS.

6.3.1 ABBA

The ABBA project used a simplified version of `hdl_env`. The fundamental functionality is the generation of Makefiles to execute simulations and compilations. Necessary files and their dependencies are automatically collected via `Manifest.py` files. Each simulation and compilation folder has its dedicated `Manifest.py` file, where the configuration is determined. This file contains information about the tools, devices and used files in this folder, e.g. simulation testbenches or project constraint files for compilations. There is also a list of modules, which points to the location of additional `Manifest.py` files in other folders containing source files with VHDL code or IP cores. A shortened example of a compilation `Manifest.py` can be seen in listing 6.4.

```
1 # Project description  
2 description = "Compilation of the ABBA Back FPGA (top level)"  
3  
4 # Compiling the design  
5 action = "synthesis"  
6  
7 # Compilation tool is Quartus v13.1
```

```
8 syn_tool = "quartus"
9 syn_tool_version = "13.1"
10
11 # Targeted device
12 syn_family = "Stratix IV"
13 syn_device = "EP4SGX290NF45C2"
14
15 # Top module used for compilation
16 top_module = "ABBA_back_top"
17
18 # List of modules
19 modules = {
20     "local" : [
21         "../back_fpga_src/ethernet_lib",
22         # ... (shortened)
23     ],
24 }
25
26 # Default library
27 library = "ABBA_BACK_TOP"
28
29 # List of source files for compilation
30 files = [
31     "ABBA_back_top.vhd",
32     "quartus_tcl/fpga_io_standard.tcl",
33     # ... (shortened)
34 ]
```

Listing 6.4: Manifest.py for a compilation

6.3.2 LASP

One part of this thesis deals with the choice for the optimal development environment for the LASP project. In the following, the decision-making process is explained. One mentionable candidate was the Pile of Cores (PoC) library, designed at the TU Dresden [106]. PoC provides implementations for often required hardware functions in VHDL code. It is equipped with a Python based infrastructure and various simulation and synthesis tool chains. Unfortunately, PoC does not incorporate a module based system, which is necessary for a large project. Therefore, it was not chosen as the development environment. Instead the library is used as a source for useful VHDL functions.

The tool `hdl_env` is a very flexible and powerful development environment, which supports modularity. But it has also unnecessary components, which prevents an efficient work flow. This results in the choice of a slightly simplified version of `hdl_env` for

the LASP project. It needs to be more sophisticated than the environment for the ABBA project, because of the dimensions of LASP with multiple modules. Therefore, it additionally uses the `top_level.py` file, which can be seen in listing 6.5 as a shortened version.

```
1  # Project name
2  project_name = 'lasp'
3
4  # Top-level module name
5  top_level_name = 'fpga'
6
7  # List of top level modules
8  modules = {
9      top_level_name: {'path': 'fpga',
10                      'description': 'Top-level FPGA'},
11      'packer':      {'path': 'packer',
12                      'description': 'Trigger packers'},
13      'lolli':       {'path': 'lolli',
14                      'description': 'Low Level Interface'},
15      # ... (shortened)
16 }
```

Listing 6.5: Definition of top module and list of modules in python file

The `top_level` file declares the top module and lists all other modules and the locations of the corresponding python files. These python files can define constants, registers and the interface between the modules. The interface definition could be used to generate the VHDL port declarations for each module. But the python syntax for the interface is very confusing and many unnecessary type definitions are automatically generated as well. Therefore, it was decided to manually write the VHDL code for the port declarations and to refrain from this feature of `hdl_env`.

The mentioned constants are used for the configuration of the project. Examples are the chosen hardware target, the enabling of modules, and the data width of signals. It was decided to define global constants, which are used by multiple modules, in the `fpga.py` file. A shortened version can be seen in listing 6.6. Local constants, which are only used in a single module, are defined in the corresponding python file for that module. This results in no dependencies between the modules and makes the development more independent. The constants can then be changed in the Manifest.py files of a simulation or compilation. Finally, the definition of registers is necessary for the slow control, which reads and overwrites control and status registers of all modules.


```
43         'description': 'lower 32 bits'},  
44     },  
45 } ),  
46 ],  
47 } ),  
48 # ... (shortened)  
49 }
```

Listing 6.6: Definition of global constants and registers

Chapter 7

ABBA Development

ABBA is part of the demonstrator setup for the Phase-1 upgrade. It is located in the back-end and has the task to read out detectors cells via Ethernet. The board contains one Back FPGA, which handles most of the Ethernet communication, and two Front FPGAs, whose task is the ADC readout and handling the data transmission and control tool IPbus. An introduction to ABBA was given in section 4.1.3. It placed emphasis on the Back FPGA with a schematic of the modules in fig. 4.5. It receives packets from the computer, which contain requests for data. The different protocols are processed in the corresponding modules, namely Ethernet, UDP and IP module. The remaining packet is forwarded to one of the Front FPGAs. The received response passes through the modules in reverse order and is sent to the computer.

For this thesis, only adjustments in the firmware of the Back FPGA were conducted. First, the packet tracing feature was implemented to enable simultaneous requests from several computers, which is discussed in section 7.1. Then, an IPbus module was included for the IPbus header processing. This enabled packet counting and a soft reset feature, which is explained in section 7.2.1 and section 7.2.2, respectively. ?? highlights several measurements, which were done with the ABBA demonstrator readout.

7.1 Packet Tracing

The first task was the implementation of a packet tracing feature in the Back FPGA. Originally, the source UDP port and IP address of the request packet were recorded in a table inside the IP module. In the UDP module, a First-In-First-Out (FIFO) memory stored the source UDP port. When the response packet from one of the Front FPGAs arrived, this FIFO was read out. The UDP port was set as destination in the header, before the packet was sent to the IP module. Here, the corresponding IP address was read from the table and placed into the header. A representation of the process can be seen in fig. 7.1. The FIFO in the UDP module led to problems when multiple computers requested data simultaneously. The Back FPGA could receive responses from the Front

FPGAs in a different order compared to the transmitted requests, which resulted in addresses being assigned incorrectly.

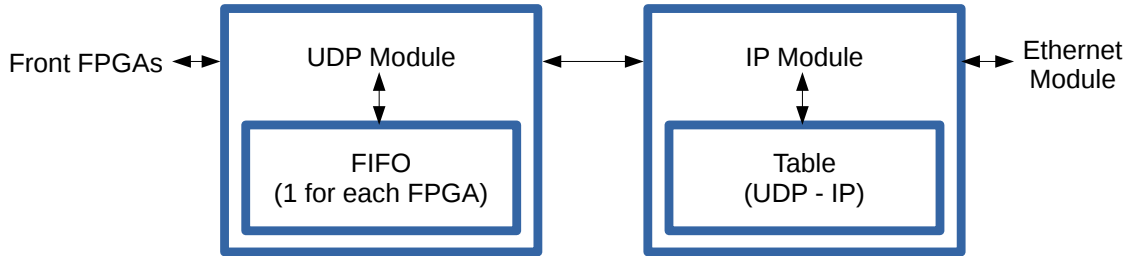


Figure 7.1: Part of the Back FPGA firmware without packet tracing

In the revised version, a table is added to the UDP and IP module. When a packet with a new source IP address arrives at the IP module, a new identifier number is generated and both are stored as a pair in the table. This identifier is then fed to the UDP module along with the packet. There, the source UDP port is paired with the identifier and stored in the table. The identifier number is written into the IPbus header of the packet, which is sent to the Front FPGA. The firmware of the Front FPGA is changed to force the response packet to contain the same number. This way, the correct destination UDP port can be extracted from the table and put into the header. The identifier number is forwarded to the IP module, where it is used to identify the destination IP address. A representation of the process can be seen in fig. 7.2.

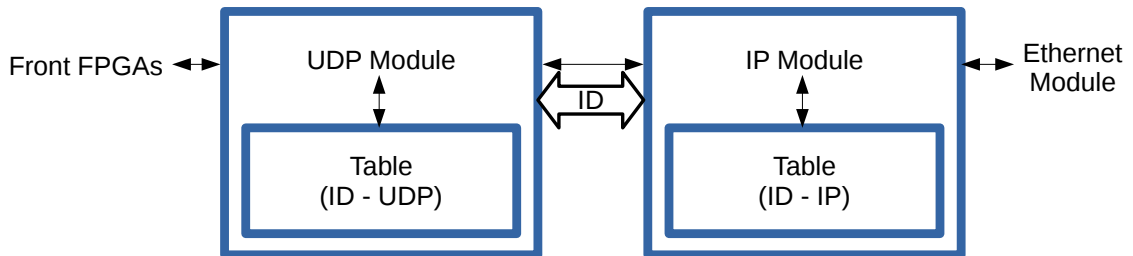


Figure 7.2: Part of the Back FPGA firmware with packet tracing by using an identifier (ID)

7.2 IPbus Module

The IPbus modules in the Front FPGAs are used to process the IPbus protocol headers of the packets. It enables the access to control and status registers, and the readout of ADC data. This module was originally missing in the Back FPGA. Therefore, the second task was to implement an IPbus module to make monitoring and controlling features available. A new UDP port is assigned to the Back FPGA. The IPbus module is mainly connected to the UDP module and has also links to the other modules of the

Back FPGA, which is explained in the following sections. A representation can be seen in figure fig. 7.3.

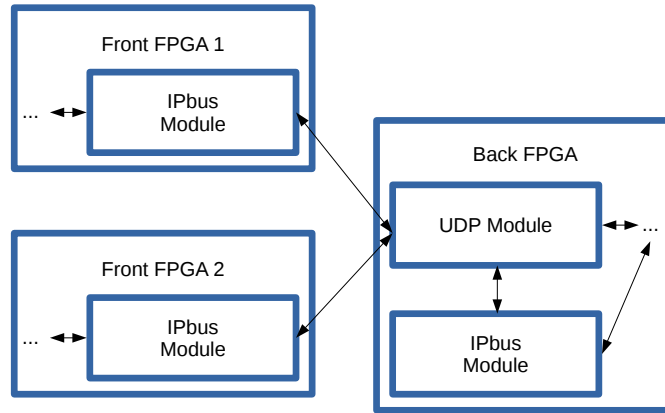


Figure 7.3: Interface between Front and Back FPGAs. A new IPbus module was added to the Back FPGA firmware. It has an interface to each module in the Back FPGA.

7.2.1 Packet Counter

The first problem, which could be tackled with the new IPbus module, was event losses from the ABBA readout. There was an investigation necessary if this occurred because of packet losses in the Back FPGA or if there was an issue with the ADC readout in the Front FPGAs. Therefore, numerous packet counters were added in the firmware of the Back FPGA with the results being stored in registers. Their location can be seen in fig. 7.4. The registers could be read out via the IPbus protocol.

Table 7.1 shows the result of two counting runs. There is a pair of counters in each location with a receiving (RX) direction from TDAQ to the Front FPGA and a transmitting (TX) direction from the Front FPGA to TDAQ. There is a discrepancy between the counters of the receiving and transmitting direction at the Ethernet module, because the counter is located before the MAC filter. Therefore, packets are also counted, when they are not directed to ABBA. The short counting run shows, that there is a difference of two between each counter step, e.g. UDP module and IP module. The sum of the last three counter pairs is also by two larger than the counter pair in front of the UDP module. The reason is, that the counters are not read out simultaneously, but sequential, and the list is generated from top to bottom. For example, it requires two additional packets to read out the IP module counters before the UDP module counters is read out.

The long run shows, that the counter for the Front FPGA 2 in the receiving direction is too large compared to the other counters. The reason could be the increment of the counter when the `start_of_packet` signal is asserted and not during the low to high transition. Therefore, one packet was counted multiple times. The run also reveals some

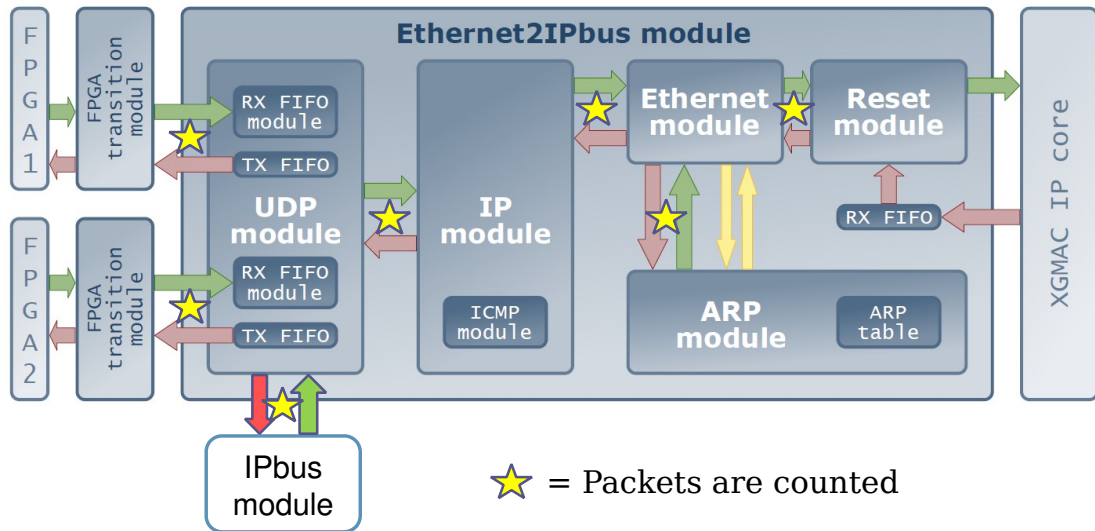


Figure 7.4: ABBA Back FPGA with the location of the packet counters marked by a star

deviations in the other counters, but the receiving and transmitting counter pairs are with one exception identical. Therefore, the event loss cannot be explained with packet losses during the IPbus readout.

Counter location	Short run	Long run
Ethernet_RX	383	149697984
Ethernet_TX	352	149664690
ARP_RX	2	1246
ARP_TX	2	1246
IP_RX	354	149663450
IP_TX	354	149663450
UDP_RX	356	149663449
UDP_TX	356	149663450
IPBus_RX	354	1253
IPBus_TX	354	1253
FPGA1_RX	4	0
FPGA1_TX	4	0
FPGA2_RX	0	152378407
FPGA2_TX	0	149663755

Table 7.1: A short and long counting run of the Back FPGA of ABBA. For each location, there is a receiving and transmitting counter.

7.2.2 Soft Reset

The new IPbus module in the Back FPGA also made a soft reset structure possible. The already existing reset module is only able to reset all three FPGAs at the same time. A soft reset enables to only reset certain areas of the Back FPGA, similar to a structure already in operation in the Front FPGAs. The soft reset signal is a 32 bit vector, which is written in a dedicated reset register. Each bit is able to reset a specific module or register in the Back FPGA. It is also possible to reset each of the Front FPGAs. The summary can be seen in fig. 7.5.

soft_resets commands							
byte	bit	reset name	dedicated to	byte	bit	reset name	dedicated to
0	0	Ethernet module	back FPGA modules	2	16	front FPGA 1	front hard resets
	1	ARP module			17	front FPGA 2	
	2	IP module			18		
	3	UDP module			19		
	4	IPbus module			20		
	5				21		
	6				22		
	7				23		
1	8	counter ETH_RX + ETH_TX	packet counters	3	24		
	9	counter ARP_RX + ARP_TX			25		
	10	counter IP_RX + IP_TX			26		
	11	counter UDP_RX + UDP_TX			27		
	12	counter IPbus_RX + IPbus_TX			28		
	13	counter FPGA1_RX + FPGA1_TX			29		
	14	counter FPGA2_RX + FPGA2_TX			30		
	15				31		

Figure 7.5: The soft reset vector of the Back FPGA. Each bit resets a specific area on ABBA.

7.3 Measurements with the ABBA Demonstrator readout

The discussed firmware developments guaranteed a functioning readout of the demonstrator Super Cell. Several possible sources of error were eliminated. This sections highlights several measurements, which were generated by the ABBA readout. These plots validate all functions of the future readout, which were tested with the demonstrator system.

Figure 7.6 displays the measurement of several calibration pulses in a front layer Su-

per Cell. At the beginning of the signal, the separate ADC samples can be distinguished. The high number of data points is only possible due to repeated sampling of the same pulse shape with different delays. The shape of the calibration pulse is slightly different to a physics pulse. This is because the calibration board works with a capacitor, which generates an exponential instead of a triangle curve. Varying Digital-to-Analog Converter (DAC) values generate different pulse heights with the expected linearity. The exception is the highest value, which shows effects of the analog saturation.

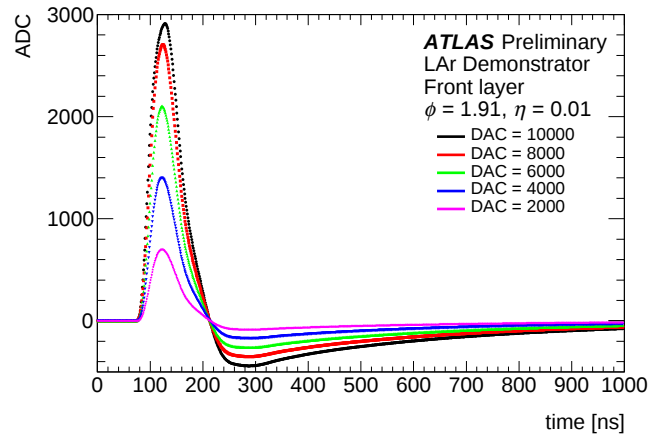


Figure 7.6: Calibration Pulse Shapes of a Super Cell [97]. Pulses were injected with different DAC values into the demonstrator system.

ABBA also recorded data from pp collisions. The reconstructed energies of the sampled pulse shapes were matched and compared to summed detector cells of the main ATLAS readout. Figure 7.7 shows the correlation of these two energy measurements in a middle layer Super Cell. There is a good agreement between the two readouts, which confirms the functionality of the ABBA system.

The good agreement can also be seen in fig. 7.8. It shows an event display of the demonstrator region measured by the ABBA and the main readout. The figure also highlights the improved trigger readout after the Phase-1 upgrade, which has a higher granularity and is able to distinguish between different layers. This improves the identification of $e^\pm/\gamma$ showers.

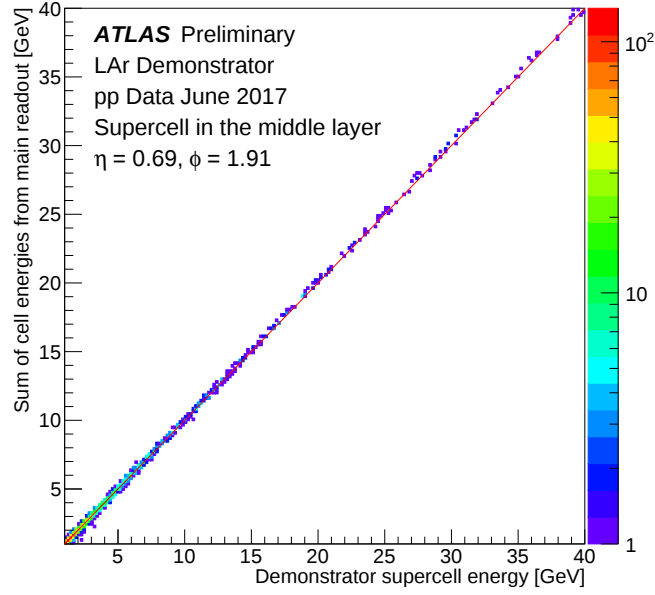


Figure 7.7: Correlation of energy measurements [97]. Measured Super Cell energies of the demonstrator are compared to summed LAr cell energies of the main ATLAS readout.

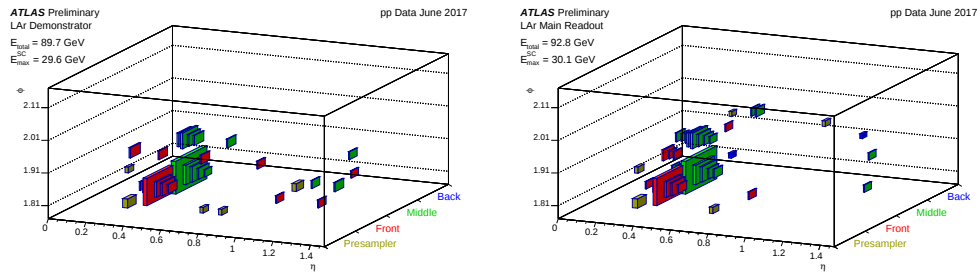


Figure 7.8: Event display of the demonstrator region [97]. The measurements of the demonstrator (left) and the main readout (right) show good agreement. The volume of the depicted boxes is proportional to the deposited energy.

Chapter 8

LASP Development

The LASP is the main processing device of the digital calorimeter data in the HL-LHC phase. An introduction was given in section 4.2.3. In this chapter, the development of the LASP system is presented. Section 8.1 discusses the design of a FIR filter, which is the main function of the board. A fraction of the processed channels need to be sent to the GETP. Section 8.2 explains an algorithm, which is used to select the most energetic energy entries in the LAr calorimeter cells. The result of the FIR filter is transmitted via fast optical links. Testbench measurements are performed and discussed in section 8.3.

8.1 FIR Filter

An introduction to FIR filters was given in section 5.1.2. They are a valuable tool in signal processing and is used for noise suppression. This improves the result of energy reconstructions and time determinations. FIR filter have the additional advantage of being stable, because the impulse response returns to zero after a finite time interval.

The basic building block for the implementation of FIR filters in FPGAs are DSPs. For this thesis, DSPs from the Stratix 10 were used [107]. DSP blocks are specialized systems, which are optimized for arithmetic operations. They can be added to the VHDL code as an IP core. A simple representation of a DSP inside a Stratix 10 can be seen in fig. 8.1. It contains several registers and two multipliers, whose result can be added or subtracted. The inputs `ax` and `bx` will be used for the coefficients, while `ay` and `by` will receive the ADC samples from the detector.

FIR filters can be constructed by chaining multiple DSP cores together and operate them in systolic mode. A visual representation of two connected DSP blocks can be seen in fig. 8.2. Each multiplier has a data point and a coefficient as input. The resulting products are subsequently added and buffered in intermediate registers until they form the final output. The example is the equivalent to a 4-stage FIR filter. It is also possible to include additional DSPs for more stages.

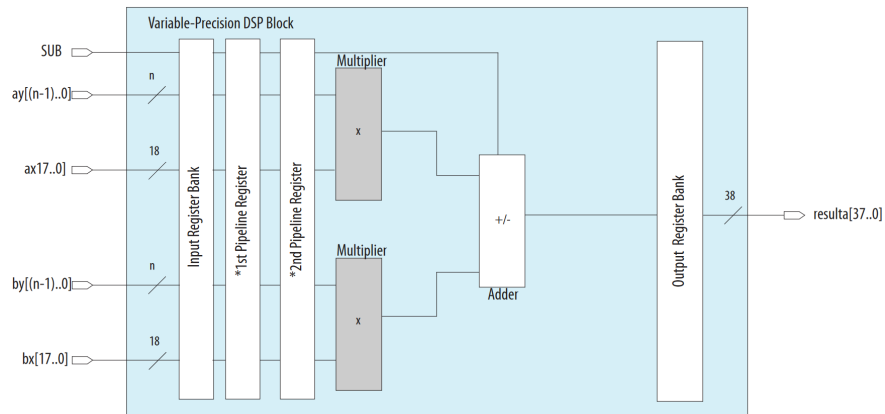


Figure 8.1: Simple representation of a Stratix 10 DSP. The block contains several registers, two multipliers and an adder.

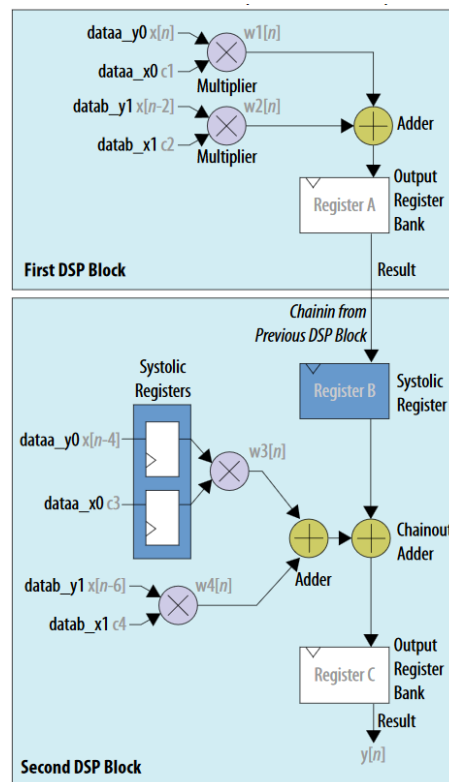


Figure 8.2: Two chained DSPs in systolic mode. The result of the first block is forwarded to the second. This setup forms a 4-stage FIR filter.

A DSP IP core is a complex VHDL module with many configurable parameters. The functional representation can be seen in fig. 8.3 Not all of these functionalities are

needed for the FIR filter implementation. Therefore, a simplified wrapper was written for the IP core. In this wrapper, several ports are unconnected, e.g. `scanin` and `scanout`, which can be used for input cascade. The `loadconst` and `accumulate` signals enable the feature to reuse the calculated result in the next iteration inside the same DSP. There are also the `negate` and `sub` signals, which are not needed, because subtraction is not used in the FIR filter. It is possible to choose a stored coefficient as input for the multiplication, but this disables the configuration of the coefficients during runtime and therefore the `coefsela` and `cofselb` signals are not used. Many settings like the bit widths, usage of clocks and registers, operation mode and preadders are done inside the wrapper.

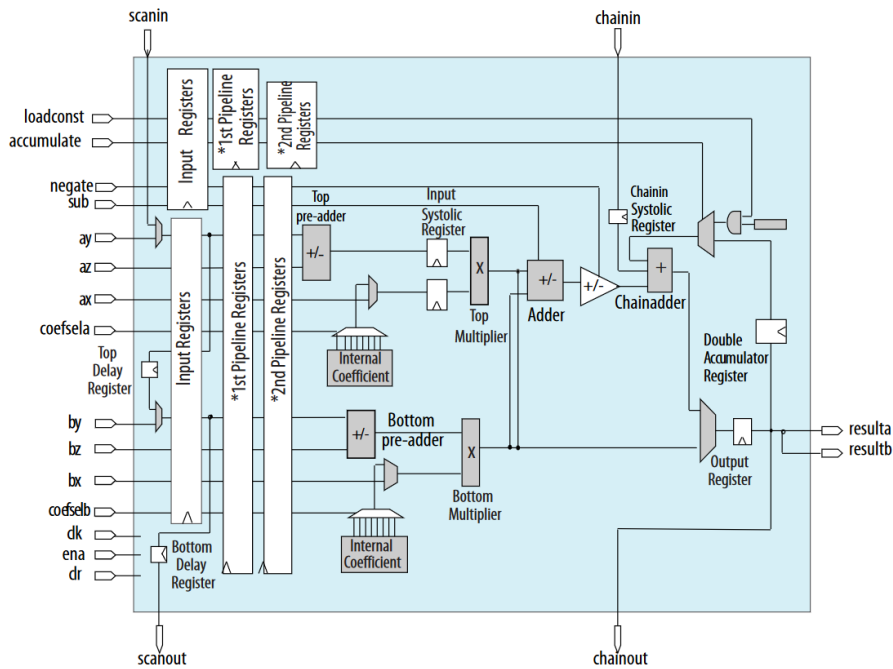


Figure 8.3: Functional representation of a Stratix 10 DSP block

Figure 8.3 also shows, that the signals `bx` and `by` pass three registers until they reach the main adder. When the systolic mode is enabled, there are additional registers in the path of `ax` and `ay`, which increases their delay to four. In a 2-stage FIR it would be sufficient to send the current sample to both inputs `ay` and `by`. The different number of registers adds a delay to `ay`, so that two different samples are summed at the adder, after the multiplication with the coefficient took place. If another DSP is chained to the first one, the input signals from the first DSP have to pass two additional registers compared to the input signals from the second DSP: the output registers from the first DSP and the `chainin` systolic registers from the second DSP. This is the correct delay for the summing at the `chainadder`. This setup makes additional delay blocks outside the DSP unnecessary and reveals a simple structure for the basic FIR filter.

There is an additional constraint, which has to be taken into account. If each channel is processed by one set of DSPs, the required hardware is immense. In addition, with this setup, the data is processed at the frequency of the ADC 40 MHz, but a DSP is able to handle much higher frequencies. Therefore, the data is multiplexed, meaning that several channels are serialized into one channel, which then needs a clock with a higher frequency. If, for example, four channels are multiplexed, the 512 channels of a single LASP board could be processed by 128 FIR filters at a clock frequency of 160 MHz.

This is implemented by adding more registers in front of the DSPs, which store the extra samples. If we assume that four channels are multiplexed, there should be three additional registers in front of the second input compared to the first input of the FIR. The third input in turn also needs three registers more than the second input and so on. A simulation of this setup can be seen in fig. 8.4, which shows the correct behavior.

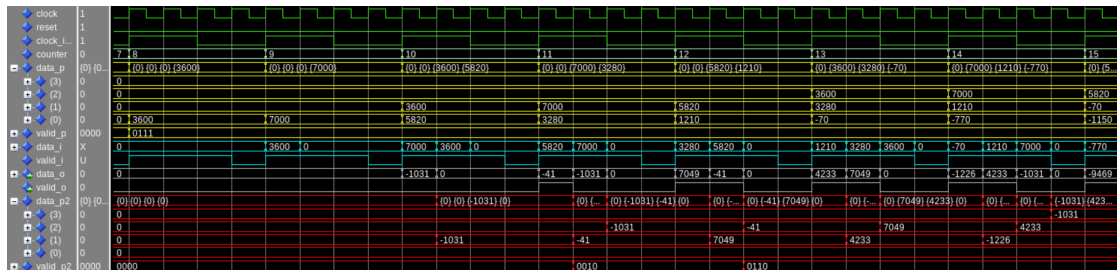


Figure 8.4: Simulation of a FIR filter. A defined pulse (yellow) is generated synchronous to a slow clock three times at different `counter` values. The three pulses and a constant signal are multiplexed into one serial channel (blue), which is fed into the FIR filter. The output (gray) is demultiplexed into four channels (red). They all show the expected responses, while the timing and the mapping is not the one to be used for final implementation, because only a very basic multiplexer showcase was used.

To find out the resource requirements and maximum possible clock frequency for the Stratix 10 FPGA, several compilations with Quartus Prime 18.1 are conducted. The baseline solution is to multiplex eight channels and therefore the usage of 64 FIR filters. Table 8.1 shows the result for various numbers of stages of the filter. The baseline solution is the usage of FIR filters with 6 stages. If there is the need to use more filters per channel, the number of Adaptive Logic Modules (ALMs) and DSPs is proportional to the desired number of FIRs. A maximum possible clock frequency of around 890 MHz was reached with the Slow 900mV 0C Model of the Timing Analyzer for all compilations.

The high value for the maximum clock frequency offers the opportunity to increase the frequency up to 480 MHz and therefore process more channels with one FIR. Table 8.2 displays the resource requirements for 43 filters with 12 channels per filter. It results in fewer DSPs, but a slightly higher ALM usage. This design reaches a maximum possible clock frequency of around 820 MHz. These properties are in line with the specifications and therefore a viable alternative to the design with 8 channels per filter.

Number of stages	Number of ALMs	Number of DSPs
6	10,240 (1 %)	192 (3 %)
8	13,882 (1 %)	256 (4 %)
10	17,546 (2 %)	320 (6 %)

Table 8.1: ALM and DSP requirements for 64 FIRs with various stages and eight channels per filter.

Number of stages	Number of ALMs	Number of DSPs
6	10,326 (1 %)	129 (2 %)
8	14,065 (2 %)	172 (3 %)
10	18,031 (2 %)	215 (4 %)

Table 8.2: ALM and DSP requirements for 43 FIRs with various stages and 12 channels per filter.

With these results, the implementation of 43 filters with 12 channels per filter is recommended. Each channels consists of a high gain and low gain signal. In addition, it may be helpful to use different filters in the trigger and the regular readout path. This results in a factor of four in ressource requirements, which is still feasible. To make additional studies more realistic, more features like gain selection should be added.

8.2 Energy Selection Algorithm

The second task involved data preparation for the GETP. It is intended that LASP sends signals from individual LAr cells. The bandwidth interface to the GETP is estimated to support 153 cells, which equals to 30 % of the 512 input cells of a LASP board. A solution is to only send cells, which are above the 2σ -above-noise energy threshold [36]. On average, this corresponds to 5.5 % of all cells in a board. This number can be exceeded for certain event topologies, e.g. high-energy jets or local noise bursts [36]. There are two possible solutions to cope with such situations. Large event fragments could be sent in asynchronous mode or the LASP sends all cells ordered by energy until the output bandwidth saturates. The former can handle high-occupancy, low-rate events, but does not prevent bandwidth saturation during noise bursts. The latter solution requires an algorithm to provide a bit pattern, which points to the 153 hottest cells. Such a solution is explained in this section and a simplified version for fewer cells can be seen in fig. 8.5.

For reasons of simplification, the selection of the three greatest out of five signals is explained, as an example. The signals consist of eight-bit vectors. The **Remaining spots** value is set to three, indicating the number of spots, which need to be filled by the highest signals. The greatest energy values are selected by the bits set, starting

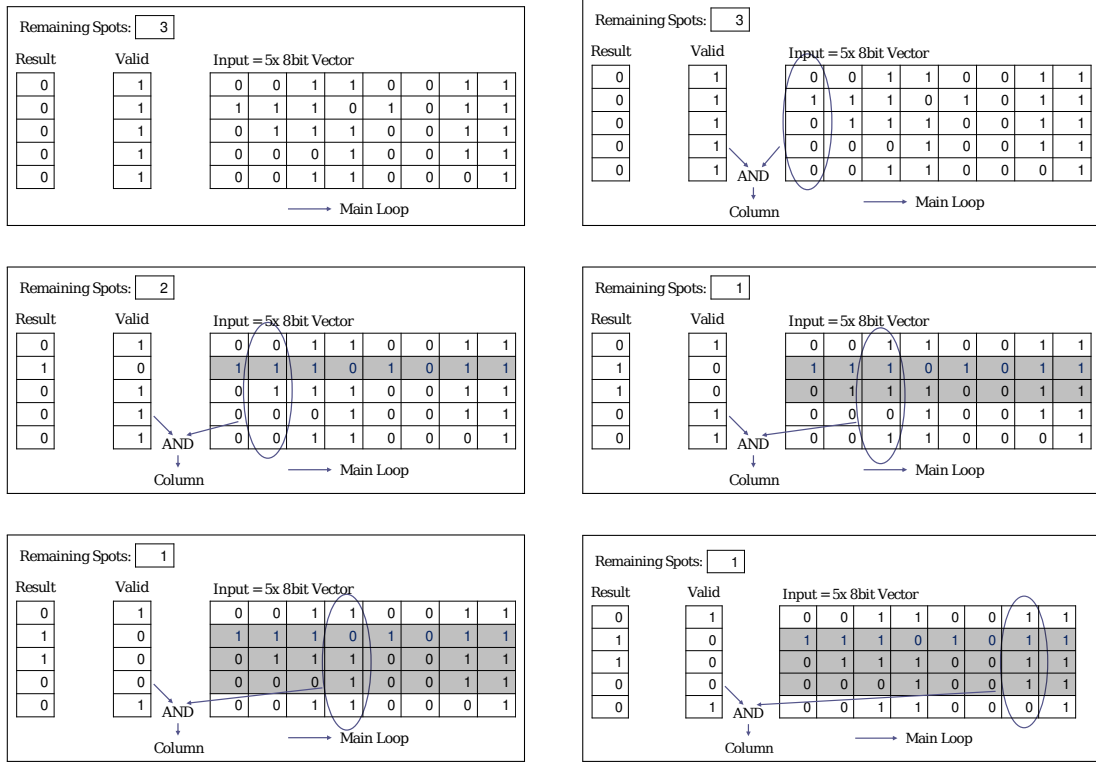


Figure 8.5: Demonstration of the energy selection algorithm row-wise from left to right. The input vectors are on the right and the result vector on the left of each graphic. At the top there is the number of remaining spots. The valid vector in the middle shows which vectors are still to be considered in the algorithm. There is a main loop over each bit from the most to least significant. At each stage the number of set bits of an AND combination of the valid vector and `column` are counted. Invalid vectors are depicted in gray.

from the Most Significant Bit (LSB). The five-bit vector `result` stores the information about which energy is already selected. The information about which energy is still to be considered is stored in `valid`, another five-bit vector. The position of the three greatest energy values are kept in memory and are updated while the selection loop is executed. The algorithm can be described as a loop over the eight bits starting at the MSB. First, the number of set bits in `column`, consisting of the MSB of each vector, are counted. The result is compared to the number of remaining spots to fill. Depending on the outcome, one of the following procedures is executed:

1. There are less vectors with a set bit compared to the number of remaining spots. This means, that these vectors amongst the largest ones. Their position is stored in the result vector by performing an OR combination of the result vector and `column`. The largest vectors should also be excluded from the following processes and are ignored

by performing an AND NOT combination of the valid vector and `column`. Finally, the `Remaining spots` are reduced by the number of set bits.

2. There are more vectors with a set bit compared to the number of remaining spots. In this case, all vectors, whose bit is not set, are not among the highest vector and can be ignored by the algorithm. Therefore, an AND combination of the valid vector and `column` is performed.

3. There is the special case, in which the number of set bits is equal to the remaining spots. All vectors with a set bit belong to the largest ones. The algorithm can terminate after it remembers the highest vectors by an OR combination like in the first outcome.

After one of these processes is executed, the same is done with the next significant bit of all vectors and so on until all bits are handled. If several vectors are the same, it can happen that the loop finished, but there are still remaining spots. In the current version, these positions would be left unfilled. A possible modification could add some of the equal vectors to the result.

The most time and resource consuming process in this algorithm is the counting of the set bits. There are several possibilities to solve this task. A simple loop over `column` could be used to increase a counter if a bit is set. Another approach is a recursive function, which cuts the vector in half and insert it into the same function. This is repeated until the length of the vector small enough for a trivial solution.

The last possibility, which was studied, is the population count or hamming weight [108]. It is a more complex approach to implement, because it is working with several bit shifts and masking. The resource requirements and maximum possible frequencies of the three algorithms with an input of a 512 bit vector is displayed in table 8.3. Each uses 30 dedicated logic registers.

Algorithm	Number of ALMs	Maximum clock frequency [MHz]
simple loop	805	1201
recursive function	824	1481
population count	1069	1180

Table 8.3: ALM requirements and maximum frequency for several algorithms, which count the number of set bits

A simulation of a complete algorithm can be seen in fig. 8.6. The recursive function was used for counting the number of set bits. The compilation of the project results in a resource requirement of 6539 ALMs. 2523 dedicated logic registers are used and a maximum clock frequency of 192 MHz is achieved.

The output of the selection algorithm is sent to the GETP, along with the chosen

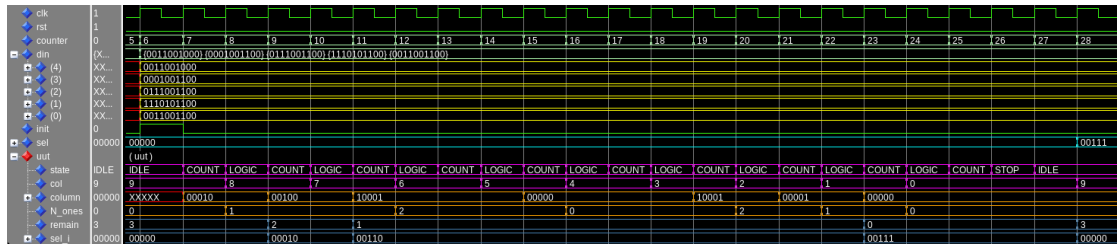


Figure 8.6: Simulation of the selection algorithm. Below the **clock**, **reset** and **counter** signal, the five input vectors are displayed (yellow). The **init** signal starts the process and the result is stored in the **sel** signal (cyan). The algorithm loops over all bits, indicated by the **col** signal, and switches between two states for each bit (magenta). The bits are combined to **column** and the number of set bits is counted (orange). The remaining spots and the preliminary result are displayed last (blue).

channels. This means that the 512 channels need to be packed into an array of 153 vectors by removing the unnecessary channels. Unfortunately, this cannot be parallelized, because the position of each selected channel in the final packet is not known initially. The process needs to go through each of the 512 bits and assign the channels according to the pattern. This would result in a long signal path and therefore a low operation clock frequency. The solution is the extension of the process over several FPGA clock cycles. A simulation can be seen in fig. 8.7.

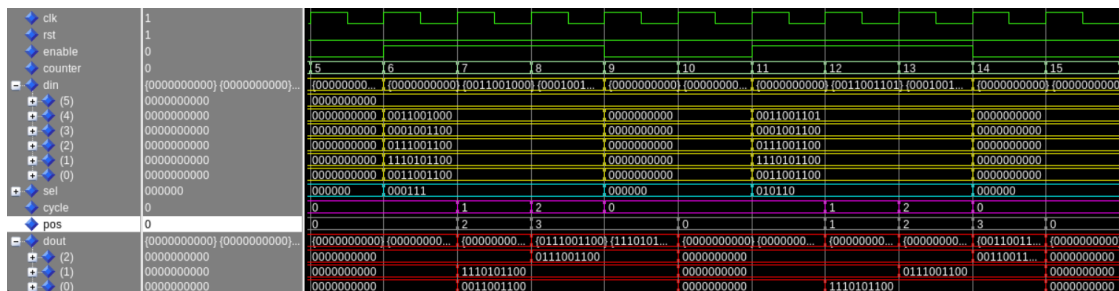


Figure 8.7: Simulation of the compression algorithm. Below the **clock** and the **reset**, there is the **enable** signal, which controls the process. The input consists of the data vectors (yellow) and the result of the selection algorithm (cyan). An integer (magenta) is used to cycle through the three parts of the **sel** signal. The **pos** integer (gray) is used to assign the input vectors to the output signals (red).

The simulation works with an input array of 6 vectors, where 3 are selected to be transmitted. The process is extended over three FPGA clock cycles and handles two vectors per cycle. In the final design, the 512 channels are divided into 16 parts with 32 channels each. This means the algorithm would induce an additional latency of 16 FPGA clock cycles. The compilation of the design results in the usage of 29,559 ALMs and achieves a maximum clock frequency of 40 MHz. This shows, that the approach is

possible, but further studies need to be conducted to improve the performance.

8.3 Gigabit Transceiver

There are several data links to the trigger and DAQ systems. For the compressed data, LASP is planned to have an interface to the GETP with a link speed of 25.78 Gbps [36]. FireFly, produced by Samtec, will be used as an electro-optical transceiver system [109]. Figure 8.8 shows a FireFly connector mounted on a circuit board. This section describes the setup of a testbench to verify the intended link speed. The Sargon Stratix 10 development kit [110] is used as the test board. It features two FireFly slots.

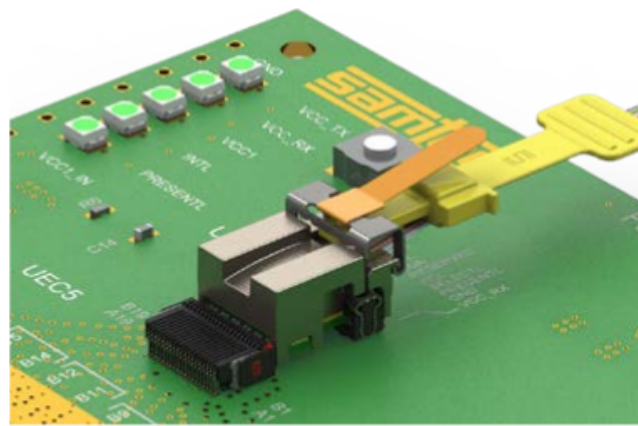


Figure 8.8: Firefly connector

The FireFly modules have several control and status registers, which can be used for configuration and monitoring. Some store basic information, e.g. vendor name and serial number. Monitoring registers contain, for example, the status of the current temperature, several alarms and optical power measurements of the receiving channels. It is also possible to separately disable transmitter channels and to enable the clock and data recovery system. The registers can be accessed from the FPGA via an I²C interface [111]. I²C is a serial protocol for a two-wire connection. There is a master I²C module in the FPGA and each FireFly is a slave module.

For the communication between the computer and the FPGA, the USB Blaster connection with the four-wire JTAG interface is used. This connection is used for the FPGA configuration, debugging and can also serve as a data transfer. Intel provides the System Console software, which uses tcl-scripts to read and write registers. With these registers, the I²C master can be controlled to access the registers on the FireFly connectors. They are also used to reset the FireFly connectors and to start the transmission test runs.

The physical setup of these test runs are shown in fig. 8.9. Each FireFly connector

possesses 12 optical fibers. A splitter is used to separate these fibres into 12 individual cables. Four of the fibres are configured as transmitters, which are connected to four receivers to create an external loopback. The other four fibres have no function and are left unused.



Figure 8.9: Physical setup for transmission tests. The FireFly connectors and part of the development board can be seen in the upper left corner. The 12 optical fibers of the FireFly are split into separate cables and four loopbacks are created, while four cables are left unused.

Figure 8.10 displays the representation of the firmware section, which executes the transmission test runs. The transceiver (XCVR) handles the interface to the FireFly and can also work with an internal loopback for debugging purposes. It serializes the parallel data from the pattern generator and deserializes the data stream from the FireFly. A bit-slip input signal is used to align the conversion to packet. The serial data requires a high-frequency clock, which is provided by the ATX PLL module. There is also a separate reset module for the transceiver. These three modules are provided as IP cores. Two transmitter/receiver pairs require two transceiver IPs, one PLL and one reset module.

The previously mentioned pattern generator produces data, which consists of a constant and a variable part. The former is used to control the bit-slip signal. It is asserted when the received data does not have the same constant part. Then the transceiver can shift the serial data until it is aligned. The variable part is a rearranged counter, which is used to record the number of errors occurring during a test run. When the computer gives the signal to start a test run, the patterns are sent to the transceiver and written into the FIFO at the same time. As soon as the first data packet returns from the loopback, the FIFO is read out and the two patterns are compared. An error counter is increased if they do not match.

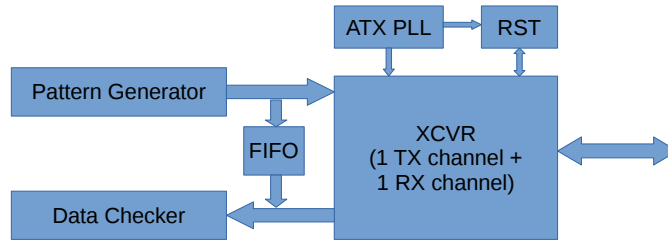


Figure 8.10: Firmware setup for transmission tests. The three blocks on the right represent IP cores, which handle the transceiver. On the left, the test pattern is generated. The data is transmitted and stored in a FIFO at the same time. The received pattern is compared with the output of the FIFO inside the Data checker.

Figure 8.11 shows a snapshot of several signals in the firmware at the start of a test run. `tx_data` contains the data, which is produced by the pattern generator. The asserted `wr_en` shows, that the FIFO already stores data for a number of clock cycles. The signal `rd_en` just asserted, because the received data (`rx_data`) matches the first transmitted pattern (`first_pattern`). This means, that the FIFO started to read out its data (`data_fifo`). If `rx_data` and `data_fifo` do not match, `error_signal` is asserted and `error_counter` is increased. Because `error_signal` has a delay of two clock cycles, the counter is increased by two at the beginning of a test run, which has to be subtracted from the result at the end. `measure_value` displays the frequency of the clock for the parallel data in Hertz.

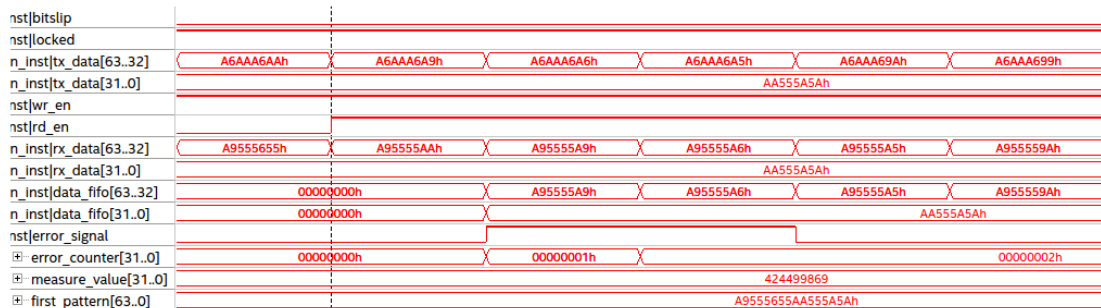


Figure 8.11: Signal snapshot of a test run. The content of the transmitted data (`tx_data`), received data (`rx_data`) and data from the FIFO (`data_fifo`) are shown over several clock cycles. `wr_en` and `rd_en` are the control signals for writing and reading the FIFO. `error_counter` is increased, when `error_signal` is asserted. The first transmitted pattern (`first_pattern`) and the measured clock frequency in Hertz (`measure_value`) are also shown.

If the frequency is multiplied by the number of bits, which were transmitted each clock cycle, the bandwidth can be calculated. In this case, the parallel data is a 64 bit vector resulting in a bandwidth of 27.17 Gbps. This is more than the required 25.78 Gbps, which means, that the FireFly module can be used for the LASP project. Long term test

runs over several days showed no errors in the four channels of one FireFly connector. The other FireFly had three channels with an increased `error_counter` signal, which indicates faulty hardware.

An eye diagram is another reference for the quality of a transmission. The received signal is repeatedly sampled and shows the transition between the two binary states 0 and 1. Figure 8.12 shows the eye diagram for the FireFly system at a bandwidth of 10 Gbps. Unfortunately due to limitation of available oscilloscopes, a higher bandwidth could not be sampled. The diagram shows an open pattern with acceptable noise, but has strange effects in the center area. The reasons are most likely bad connections on the test board, which has to be studied with different hardware in the future.

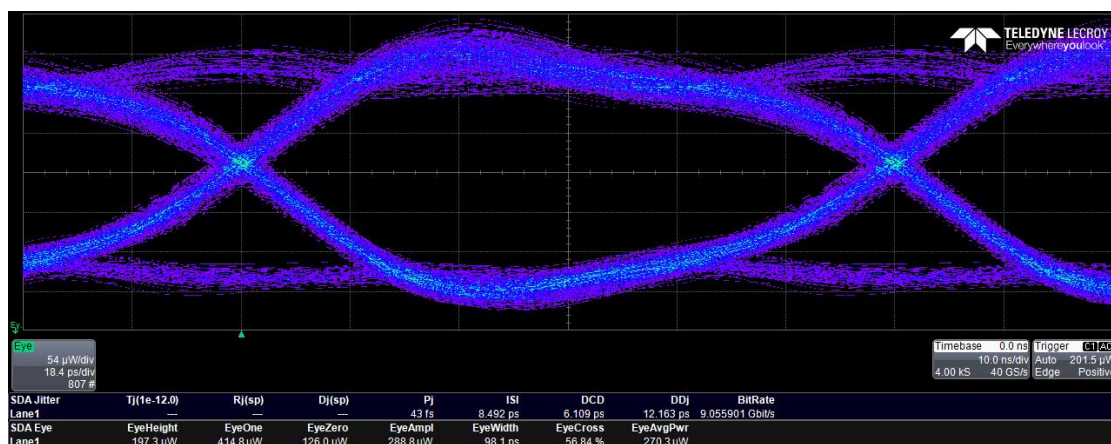


Figure 8.12: Eye Diagram of the FireFly system

Chapter 9

Summary and Outlook

To observe rare events, the number of collisions at the LHC needs to be increased. This target results in the development of a two-phase upgrade plan to enlarge the luminosity of the accelerator. This plan also affects the ATLAS detector, because it needs to cope with higher pile-up of events. An enhanced trigger system is needed to distinguish between interesting events and background. This requires a new readout system of the LAr calorimeter in order to provide higher granular trigger information, but also to cope with higher trigger rates and longer buffering times.

The simulation of the readout path with the AREUS software framework was discussed. New features were added to AREUS to study the usage of multiple gains efficiently. With this framework a gain selection procedure by the digital back-end was worked out in detail and its feasibility has been demonstrated. However, the more flexible two-gain approach implies higher costs because more data need to be transmitted and processed. An alternative was studied, which sets the gain selection closer to the detector. In this case, there is only one filter in the back-end for both gains, leading to several challenges, which were mostly solved, but results in an increased latency of 1 or 2 LHC clock cycles. Baseline shift studies showed that the influence on the low gain data is small and can be corrected by the usage of the high gain data. A remaining problem is the transition from low to high gain, which results in a small deterioration of the energy resolution. Based on these studies, the baseline solution is recommended.

The firmware development comprises a major part of this thesis. For the first phase of the LAr electronics upgrade, the data transfer protocol has been implemented on the FPGA demonstrator system ABBA. This enabled first measurements with prototype modules of the new trigger readout. Using the recorded data, it could be shown that novel trigger variables are able to improve the discrimination of electrons and hadronic jets.

Several core functionalities of the digital readout system needed for the second upgrade phase have been developed and implemented: digital signal filtering, trigger data

preparation and very fast data transmission by optical links. An FIR filter was implemented by chaining several DSP modules together. Several registers in front of the input enabled the multiplexing of channels. By time multiplexing, the FPGA resource usage could be optimized by a factor 8-12. In the future, additional features like the gain selection and baseline correction can be added to the design.

Another project was the development of a selection algorithm. The GETP requires data from LASP, but the bandwidth only allows 30% of the input channels. A special algorithm was designed to select the channels with the highest content. After the application of the algorithm, these channels need to be compressed and unnecessary data removed. The simulation validated the design, but the resource requirements are high and the maximum frequency would be small. This has to be improved to make the algorithms more usable.

In addition, a 27 Gbps transceiver testbench was set up. FireFly modules are used to transmit data from the LASP to the TDAQ system. In order to check if the required bandwidth could be reached, this setup needed to be verified. The FireFly connectors on the development board were configured via I²C and JTAG. The transceiver test setup consisted of several external loopbacks. A pattern generator sent the data and stored it in a FIFO simultaneously. The received data is compared to the readout data from the FIFO, and mismatches are counted. Long term test runs showed, that the required bandwidth was reached with an acceptable number of errors. The FireFly system is therefore validated and as a next step, a special protocol for transmission can be implemented.

In conclusion, central features of the future LAr calorimeter electronics have been developed and their proper functioning was validated, both in simulation and hardware. The development enabled first demonstrator measurements together with the full ATLAS detector. The results on gain selection, digital signal filtering, trigger data preparation and fast optical links contributed to the baseline design of the upgraded LAr electronics. The Phase-1 electronics is currently being installed during the LHC LS2, while the final Phase-2 readout system will go into operation after the LHC LS3. Both systems will allow a more refined trigger selection and will enable the ATLAS experiment to enhance the sensitivity for possible new phenomena and to collect more pure data sets for future precision measurements.

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Glossary

ABBA ATCA Board for a Baseline of Acquisition 31, 33, 57, 62, 64, 67, 69–72, 87
ADC Analog-to-Digital Converter 23, 36, 37, 40, 43, 45–51, 54, 55, 67–69, 72, 75, 78
ALICE A Large Ion Collider Experiment 13, 28
ALM Adaptive Logic Module 78, 79, 81, 82
AREUS ATLAS Readout Electronics Upgrade Simulation 39, 43, 45–48, 50–55, 87
ARP Address Resolution Protocol 31
ASIC Application-specific Integrated Circuit 59
ATCA Advanced Telecom Computer Architecture 31, 93
ATLAS Proper name, formerly “A Toroidal LHC Apparatus” vii, 1, 10, 13–17, 22, 25, 27–30, 33, 34, 40, 43, 44, 47, 50, 57, 72, 73, 87, 88, 93
BC Bunch Crossing 12, 23, 28, 32, 34, 39, 40, 44–47, 49, 52–54, 56, 96
BCID Bunch Crossing Identifier 12, 44
BSM physics Beyond the Standard Model 14
CERN European Organisation for Nuclear Research 11, 12, 25
CLB Configurable Logic Block 58
CMS Compact Muon Solenoid 13, 14, 27, 28, 33
CSC Cathode Strip Chamber 17
CTP Central Trigger Processor 34, 35
DAC Digital-to-Analog Converter 72
DAQ Data Acquisition 22, 24, 25, 29, 35, 36, 46, 83
Data Processing Core Data Processing Core 37
DRE Dynamic Range Enhancement 36, 47, 49
DSP Digital Signal Processor 24, 58, 61, 75–79, 88
EF Event Filter 25, 35
eFEX electron Feature Extractor 30
EMB Electromagnetic Barrel Calorimeter 20–22, 24, 31, 47, 54, 55
EMEC Electromagnetic End-Cap Calorimeter 20, 21, 24, 55, 56
ENOB Effective Number of Bits 45
EWSB Electroweak Symmetry Breaking 5
FCal Forward Calorimeter 21, 24, 36
FEB Front-End Board 22, 24, 31, 36
FEB2 Phase-2 Front-End Board 35–37
FEC Front-End Crate 22, 31

FELIX Front-end Link Exchange 30, 35, 38
FEX Feature Extractor 30, 34, 36, 38
FF Flip Flop 57, 58
FIFO First-In-First-Out 67, 84, 85, 88
FIR Finite Impulse Response 40, 41, 75–79, 88
FPGA Field Programmable Gate Array 31–33, 37, 54, 57–59, 67–71, 75, 78, 82, 83, 87
GbE Gigabit Ethernet 38
GETP Global Event Trigger Processor 35, 36, 38, 75, 79, 81, 83, 88
gFEX global Feature Extractor 30
GUT Grand Unified Theory 6
HDL Hardware Description Language 58
HEC Hadronic End-Cap Calorimeter 21, 24, 36
HL-LHC High Luminosity LHC 7–10, 28, 32, 75
HLT High-Level Trigger 25
IBL Insertable B-Layer 16
ID Inner Detector 14–17, 25
Input Alignment Input Alignment 37
IP Interaction Point 11–14, 16, 21, 32
IP Intellectual Property 61, 62, 75–77, 84, 85
IP Internet Protocol 32, 67–69
ITk Inner Tracker 35
jFEX jet Feature Extractor 30
L0 Level-0 34–36, 38
L1 Level-1 22–26, 29, 30, 33–35
L1Global Level-1 Global Trigger 34
L1Track Level-1 Track Trigger 34, 35
L2 Level-2 25, 26, 29
LAr Liquid-Argon 1, 2, 10, 18–23, 26, 29, 30, 32, 35–37, 40, 43, 44, 46–48, 50, 57, 73, 75, 79, 87, 88, 94, 95
LASP LAr Signal Processor 36, 37, 46, 57, 63, 64, 75, 78, 79, 83, 85, 88
LATS LAr Timing System 37
LAUROC0 Liquid Argon Upgrade Read-Out Chip 0 48
LDPS LAr Digital Processing System 30, 31, 62
LEP Large Electron–Position Collider) 11
LHC Large Hadron Collider 1, 2, 7–9, 11–14, 27, 28, 32, 44, 87, 88, 93–95
LHCb Large Hadron Collider Beauty 13, 28
LHCf Large Hadron Collider Forward 14
Linac2 Linear accelerator 2 11, 28
Linac4 Linear accelerator 4 28
LIU LHC Injectors Upgrade 28
Low Level Interface Low Level Interface 37, 38
lpGBT Low Power GigaBit Transceiver 37
LS1 Long Shutdown 1 28, 30

LS2 Long Shutdown 2 28, 88
LS3 Long Shutdown 3 28, 88
LSB Least Significant Bit 36, 45–47, 49, 55
LSB Layer Sum Board 29, 31
LTDB LAr Trigger Digitizer Board 29, 31
LUT Lookup Table 57, 58
MAC Media Access Control 31, 32, 69
MC Monte Carlo 43, 44
MDAC Multiplying Digital-to-Analog Converter 36
MDT Monitored Drift Tube 17, 33, 34
MIP Minimum Ionizing Particle 36
MoEDAL Monopole and Exotics Detector at the LHC 13
MSB Most Significant Bit 80
NSW New Small Wheel 28, 34
OF Optimal Filter 24, 30, 38–41, 45, 46, 49–54, 56
PoC Pile of Cores 63
pp Short for “proton–proton” 1, 7, 13, 14, 25, 72, 96
PS Proton Synchrotron 11, 28
PSB Proton Synchrotron Booster 11, 28
QCD Quantum Chromodynamics 5, 14
QFT Quantum Field Theory 4, 6
RF Radio-Frequency 11, 32
ROD Readout Driver 24
RoI Region of Interest 25, 26, 34, 35
RPC Resistive-Plate Chamber 17, 25, 33, 34
RTM Rear Transition Module 38
SAR Successive Approximation Register 36
SCA Switched-Capacitor Array 23
SCT Semiconductor Tracker 16
Slow Control Slow Control 38
SM Standard Model 3–6, 9, 14, 27
SPICE Simulation Program with Integrated Circuit Emphasis 45, 47
SPS Super Proton Synchrotron 11, 28
Super Cell Super Cell 29, 31, 36, 38, 44, 71–73
SUSY Supersymmetry 6, 10
TBB Tower-Builder Board 24, 29
TDAQ Trigger and Data Acquisition 31, 33, 69, 88
TDB Tower-Driver Board 24
TGC Thin-Gap Chamber 17, 25
TOE Theory of Everything 6
TOTEM Total Elastic and Diffractive Cross Section Measurement 14
Trigger Packers Trigger Packers 38
Trigger Tower Trigger Tower 25, 29, 31

- TRT** Transition Radiation Tracker 16, 33
- TTC** Trigger, Timing and Control 24, 36–38
- UDP** User Datagram Protocol 32, 67–69
- VHDL** Very High Speed Integrated Circuit Hardware Description Language 57, 59, 60, 62–64, 75, 76
- XAUI** Extended Attachment Unit Interface 31
- μ the average number of pp interactions per BC 8, 9, 28, 32, 54

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