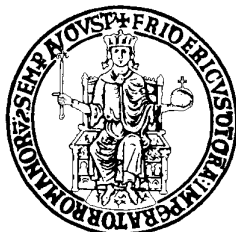


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**CORSO DI LAUREA SPECIALISTICA IN INGEGNERIA
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**A RADIATION TOLERANT ACQUISITION SYSTEM
AND SIGNAL PROCESSING FOR LVDT SENSOR**

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Ai miei genitori

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Introduction

The verification of theories aiming to explain how the world in which we all live is formed, pushes Particle Physics towards new technological challenges. At CERN (European Organization for Nuclear Research) particle accelerators and High Energy Physics experiments are built in order to discover new sub-nuclear particles and to verify the models that explain the interactions of these particles. The LHC accelerator will reach the energies necessary to verify the existence of the Higgs boson and other particles. The task to detect new particles is given to the experiments that surround the four interaction points where the two 7 TeV beams of the LHC accelerator will collide.

Beam targets and absorbers are widely used for safety purposes in all the main rings of CERN. The locations of the targets are affected by significant radiation levels. Position sensors are employed to control the position of the targets and one of the most reliable sensors is the LVDT (Linear Variable Differential Transformer) which can be manufactured in order to be radiation hardened. However, the LVDT needs an electronic conditioner to retrieve the sensor position. Such electronic modules are placed in radiation free areas preferentially. However, that is not always possible and there might exist zones in the accelerator rings, such as the SPS, where the electronics cannot be protected in dedicated alcoves.

Therefore, this thesis work aims at designing a new electronic board which wants to be a generic acquisition card with numerical processor capabilities for reading LVDT or other position sensors. The requirements of the board are fixed on the basis of the performance of the LHC collimator reading system. The position is to be read with an uncertainty less of 20 μm . The target for the numeric resolution is 0.5 μm . The board will be based on commercial parts and is designed to be radiation tolerant . That means that the electronics works properly up a given limit of radiation levels. Those

levels are the following: 100 Gy of Total Ionizing Dose (TID), 10^{11} n/cm² of High Energy Hadrons (HEH) fluence, 3×10^{11} n/cm² of 1 MeV eq. neutron fluence. Those numbers fix the limits of the boards in terms of long term parameter degradation due to ionizing and non-ionizing effects and in terms of both destructive and non-destructive Single Event Effects (SEE). In particular, the board must be immune to destructive single events and can tolerate soft single events upsets if the probability at which they occur is sufficiently low. At this aim, this work is focused on the choice of a commercial ADC and FPGA to be used on the LVDT conditioner board. An ADC is chosen and tested under radiation. Then, a flash based FPGA, known to be latch-up free, is selected to perform the Sine Fit algorithm in fixed point precision to retrieve the sensor position. The Sine Fit algorithm is deeply analyzed and 3 different implementations in fixed point representation are investigated in order to achieve a numerical precision that can assure the target requirements. The third algorithm makes use of the CORDIC functions. The tests are done on a proof demonstrator board with ADC and FPGA.

In Chapter 1, a brief introduction to CERN, to its radiation field, and to the position reading of the LHC collimation is given. In Chapter 2, the working principle of the LVDT is explained highlighting the specifications on the basis of the performance of the LHC collimation system which has proven to be very reliable in the first 2 years of operation. In Chapter 3, the design and the implementation of the proof demonstrator is shown. Then, the detailed analysis of the Sine Fit algorithm and possible implementations are described. In Chapter 4, the experimental results for comparing the algorithms with emulated and real data are presented, highlighting the benefits of the CORDIC functions. Finally, the radiation test results of the FPGA and the ADC are described and the preliminary results are shown.

Chapter 1

LHC Collider

A description of the LHC and its working principle is given in this Chapter. The radiation environment in the LHC cavern is also described. Finally a brief review of the LHC collimation design is provided because its positioning system is used as reference for fixing the targets and the specification for the position sensor conditioning presented in this work.

1.1 The CERN structure and the accelerator principles

1.1.1 The CERN accelerator complex

The European Centre for Nuclear Research (CERN) in Geneva, Switzerland, is the largest laboratory for particle physics in the world. Founded in 1954, the laboratory is one of the first born of collaborations between European countries and now involves physicists and researchers from around the world, with a total of over 500 between institutes and universities involved in the various experimental programs. Pure research is the *raison d'être* of CERN, but this laboratory also plays a crucial role in the development of future technologies. Engineering, computer science and particle physics make this an important reference for industry worldwide.

The CERN accelerator complex depicted in Figure 1, includes seven main accelerators, built in various periods starting from the birth of the organization. Since the beginning, it has been stated that every new and more powerful machine would have used the previous ones as injectors, creating actually an accelerators chain which brings gradually a particles beam to higher and higher energies. As a matter of fact, every particles acceleration technology has precise limits in terms of minimum and maximum operative energy.

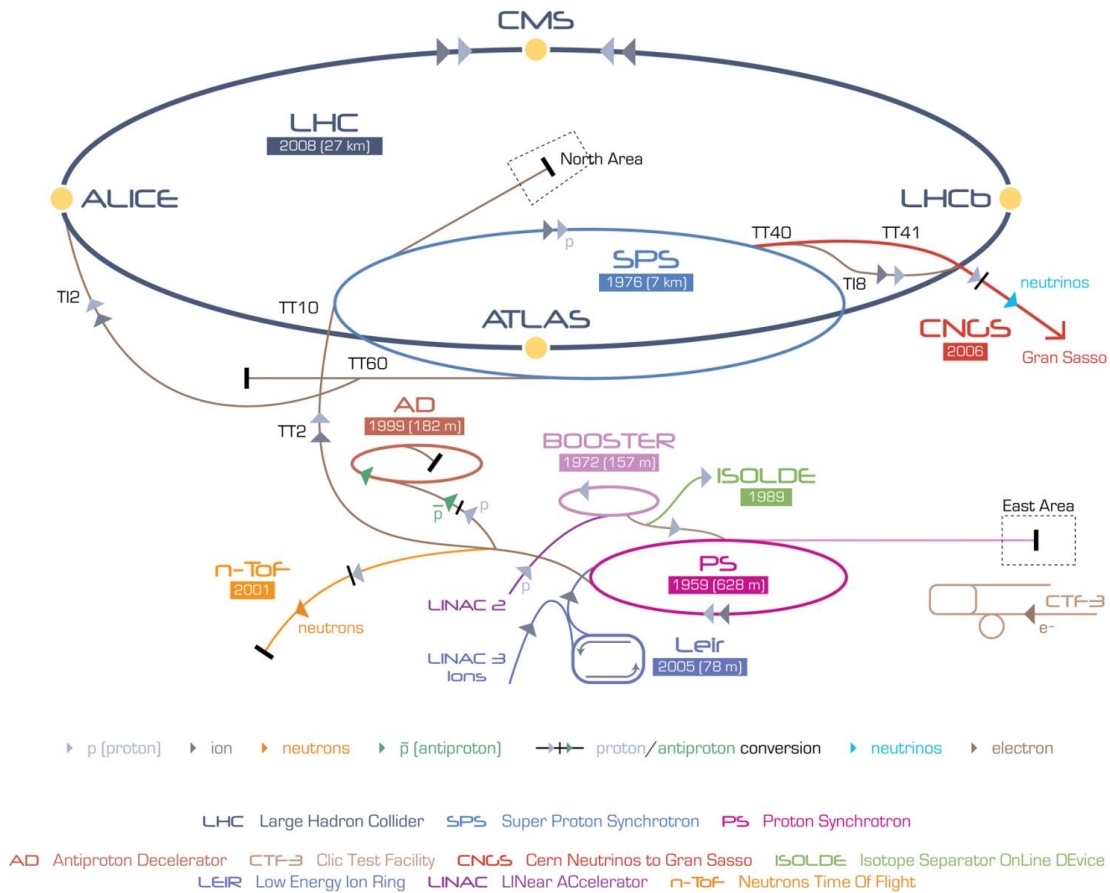


Figure 1. The CERN accelerator complex.

Here we describe the three major accelerators at CERN. The first accelerator installed in 1959 and is still working *Proto-Synchrotron* (PS), with a diameter of 200 meters. The PS has the ability to accelerate different types of particles to energy up to 23.1 GeV. The PS is added to a system of experimental machines called "PS Complex" along with two linear accelerators and an accelerator *booster* (LINAC2, LINAC3 and PSB respectively) and is now only used to produce beams of protons and different types of charged particles. The particles can then be extracted from PS and sent to the larger ring (SPS / LHC), or sent to some fixed-target experiments (ISOLDE, East Hall) or entered in the ring AD to produce antiprotons. After the PS, in 1977, the *Super-Proto-Synchrotron* (SPS), an accelerator of 6 km circumference located underground was put into operation. This can carry the particles to energies of 450 GeV. Initially this machine was used as a proton-antiproton collider allowing

to discover, in the early '80s, the particles mediators of the weak force. Following the construction of LEP, SPS assumed the role of injector of electrons and positrons and now works as a injector of hadrons for the LHC.

In the summer of 1989 came into operation the "*Large Electron Positron collider*" (LEP) a machine of 27 km of circumference, made out of a tunnel excavated at more than 100 meters under the ground level. The LEP used conventional electromagnets and had a configuration with a single ring: here were accelerated, in opposite direction, particles of different charge (electrons and positrons) that were made to collide in four interaction points, where they were placed experiments (DELPHI, ALEPH, L3, OPAL). The LEP was designed and made work to achieve an energy in the center of mass of about 91 GeV, allowing the production of a large number of secondary particles. The LEP was closed on November 2000 to make room at the LHC.

1.1.2 Introduction to LHC

The Large Hadron Collider is a two-ring, superconducting accelerator and collider installed in the 27 km long Electron–Positron (LEP) tunnel aiming to discover the Higgs particle and the study of the rare events with the centre of mass collision energies of up to 14 TeV.

The LHC is the world largest and most powerful particle accelerator. It mainly consists of a long ring of superconducting magnets with a number of accelerating structures to boost the energy of the particles along the way.

Inside the accelerator, two beams of particles travel at close to the speed of light with very high energies before colliding with one another. The beams travel in opposite directions in separate beam pipes – two tubes kept at ultrahigh vacuum. They are guided around the accelerator ring by a strong magnetic field, achieved using superconducting electromagnets. These are built from coils of special electric cable that operates in a superconducting state, efficiently conducting electricity without resistance or loss of energy. This requires chilling the magnets to about

-271°C. For this reason, much of the accelerator is connected to a distribution system of liquid helium, which cools the magnets, as well as to other supply services.

Thousands of magnets of different varieties and sizes are used to direct the beams around the accelerator. These include 1232 dipole magnets of 15 m length which are used to bend the beams, and 392 quadrupole magnets, each 5–7 m long, to focus the beams. Just prior to collision, another type of magnet is used to 'squeeze' the particles closer together to increase the chances of collisions.

In general particle accelerators are machines that accelerate charged particles to high kinetic energies by applying electromagnetic fields. A particle of charge q and momentum moving through an electromagnetic field is submitted to the Coulomb and Lorentz's forces given by:

$$\vec{F} = \frac{dp}{dt} = q(\vec{E} + \vec{v} \times \vec{B})$$

where F is the electromagnetic force by the electric field E and the magnetic field B on a particle of velocity v .

The electric field E changes the particle trajectory and velocity so the momentum and the energy can be modified. This force can be used to accelerate and decelerate particles.

Modern circular accelerators, such as the LHC, make use of both principles. The particle beams are constrained by strong magnetic fields to circulate on a closed orbit. In this condition the particle beams can be accumulated, stored in the ring and accelerated.

A constant magnetic field B normal to the particle velocity produces variations of the particle trajectory without changing the module of the particle's momentum.

The LHC and its experiments are not only complex because of the technology needed in order to detect particles, but also because of the protection and safety systems that must ensure the reliability of the measurements over time and survival of the equipment in case of accidents that, in such a complex machine, may happen.

1.1.3 LHC Design

To explore the physics in this energy range, is not sufficient enhance the performance of the LEP, or build a new machine electron-positron, as the high losses of energy of the beam (due to synchrotron radiation emitted by accelerated particles) are a limit on the maximum achievable energy. The increase of energy leads large, higher costs and therefore the only practical way to beyond this limit is to accelerate and to collide protons. The synchrotron power (P_{snc}) radiated by a particle, when accelerated, it is given by the following equation:

$$P_{snc} = \frac{1}{6\pi\epsilon_0} \frac{e^2 f^2}{c^3} \gamma^4$$

$$\gamma = \frac{E}{m_0 c^2}$$

where: e is the electron charge, f is the frequency of rotation of the particle, c the speed of light in vacuum, ϵ_0 the dielectric constant in vacuum and where, in addition to the energy possessed by the particle (E), also appears the mass (m_0) of the particle [1]. The protons then, with a rest mass 2000 times larger than that of electrons, radiate a quantity of radiation infinitely smaller at the same beam energy, making so this type of energy loss totally negligible.

The number of events per second and per unit area that are obtained from the collision between the two beams of protons is measured by the luminosity. The luminosity is given by:

$$L = \frac{N_1 N_2 \cdot f_b}{\sigma_x \sigma_y}$$

where N_1 and N_2 are the number of particles per pack of two beams, f_b is the packet rate and σ_x, σ_y are the cross sections of beams at the point of interaction [2]. In the particular case of the LHC (two equal colliding beams) is $N_1 = N_2 = N$. Actually (April 2011) the LHC sets the record of luminosity equal to $4.67 \times 10^{32} \text{cm}^{-2} \text{s}^{-1}$. The collisions take place in four point indicated in Figure 2.

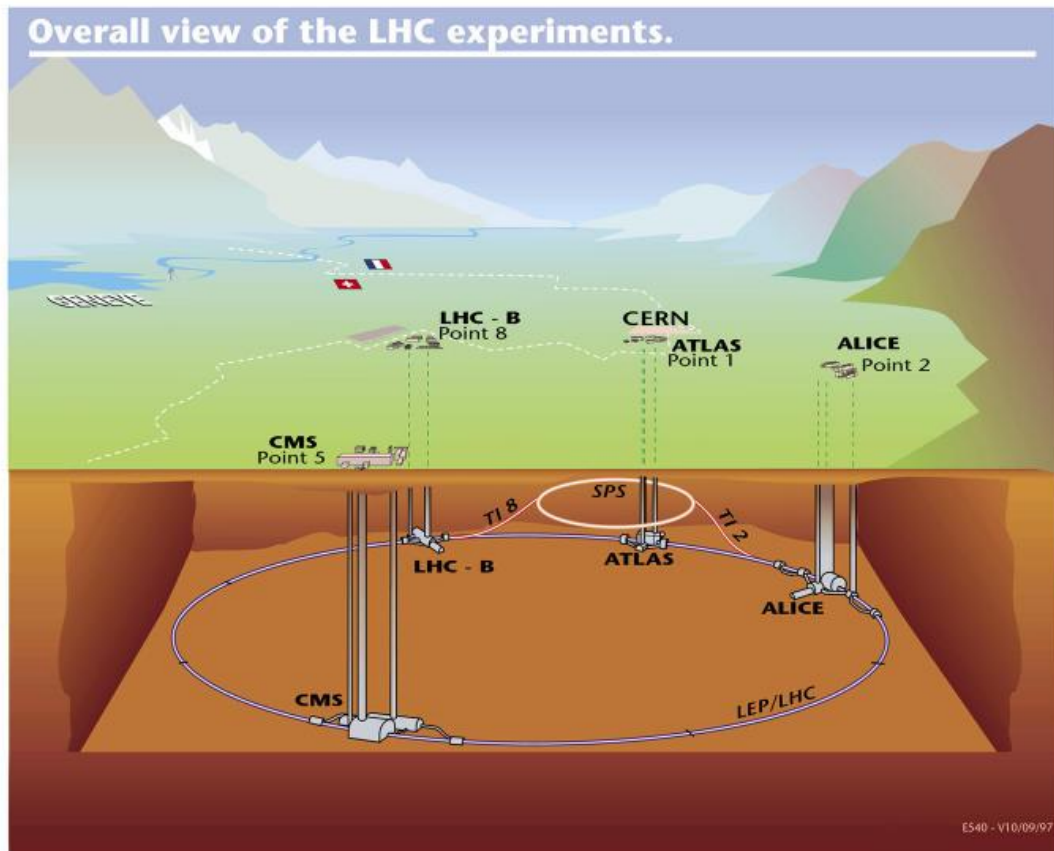


Figure 2. The LHC experiments: ATLAS, CMS, ALICE and LHCb.

To be able to collide beams of particles having the same charge a configuration called "cryodipole" has been adopted, consisting of two vacuum chambers, each with their superconducting coils able magnetic fields of equal magnitude but opposite direction, all supported by a single mechanical structure and cryogenic to reduce the size and cost.

Dipole magnets, in total 1232, keep the beams on their circular path, while additional 392 quadrupole magnets are used to keep the beams focused, in order to maximize the chances of interaction between the particles in the four intersection points, where the two beams will cross.

Approximately 96 tons of liquid helium are needed to keep the magnets at their operating temperature, making the LHC the largest cryogenic facility in the world at liquid helium temperature.

The LHC has eight arcs and eight straight sections. Each straight section is approximately 528 m long and can serve as an experimental or utility insertion.

In four sections will be hosted collimation systems, shutting down and acceleration of the beams, while the other will collide beams.

The arcs of LHC lattice are made of 23 regular arc cells. The arc cells are 106.9 m long and are made out of two 53.45 m long half cells, each of which contains one 5.355 m long cold mass (6.63 m long cryostat), a short straight section (SSS) assembly, and three 14.3 m long dipole magnets. The LHC arc cell has been optimized for a maximum integrated dipole field along the arc with a minimum number of magnet interconnections and with the smallest possible beam envelopes[3]. Figure 3 shows a schematic layout of one LHC cell.

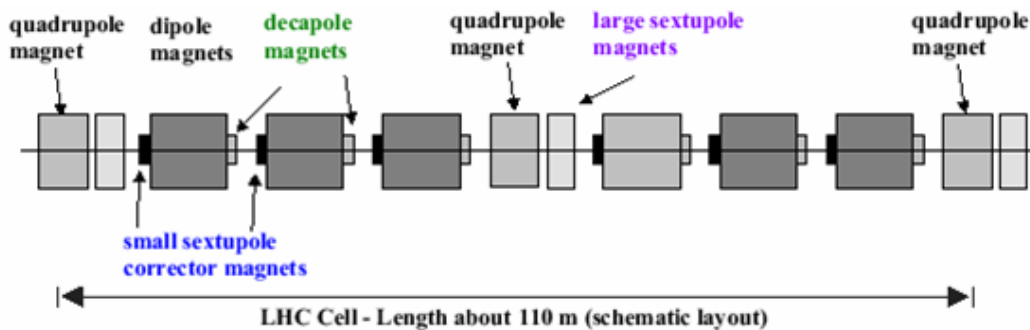


Figure 3. LHC Cell Schematic.

Two cells, placed in proximity of the points of interaction, then play the task of "suppression of dispersion". The dispersion suppressors are located at the transition between an LHC arcs and a straight sections, yielding a total of 16 dispersion suppressor sections. The aim of the dispersion suppressors is threefold:

- Adapt the LHC reference orbit to the geometry of the LEP tunnel.

- Cancel the horizontal dispersion arising in the arc and generated by the separation/recombination dipole magnets and the crossing angle bumps.
- Facilitate matching the insertion optics to the periodic optics of the arc.

The straight sections used to collide two beams are used by ATLAS experiments at point 1 and point 5 to the CMS, designed to search for the Higgs Boson. In section 2 and section 8 there are the ALICE experiment designed to study future collisions with ions of Pb and the experiment LHC-b for the study of B mesons, as shown in Figure 4.

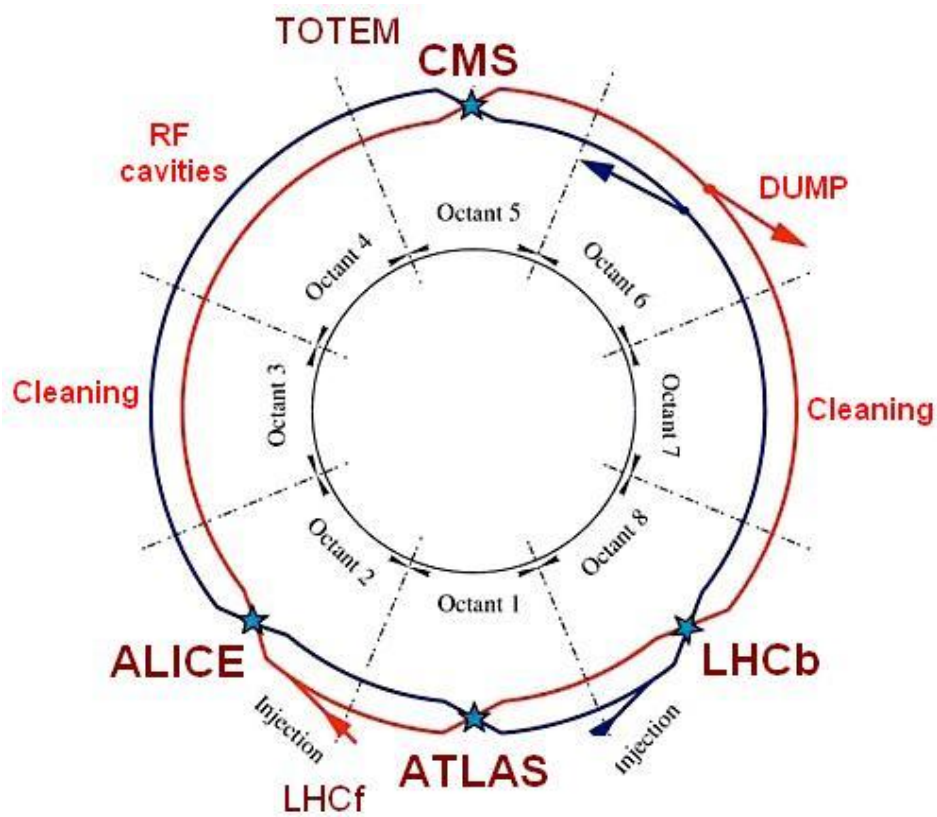


Figure 4. LHC Machine Layout.

1.2 Radiation environment

1.2.1 The LHC radiation environment

Radiation in the LHC underground areas and in the accelerator tunnel is produced when protons interact with the nuclei of the residual gas atoms (beam gas interactions) or with the nuclei of the atoms of any other material surrounding the beams, such as collimators, magnets, cables, cryostats or the beam dump. When there are circulating beams in the LHC, there is a small but continuous loss of protons along the ring. These lost protons will interact with the material that is close to the beams. These primary reactions produce secondary particles such as neutrons, pions, kaons and other protons. Some of these secondary particles have sufficient energy to interact again and cause the production of tertiary particles and so on.

The equipment in the LHC tunnel will be irradiated with many different kind of particles at energies ranging from a few eV to several hundreds of GeVs. This is referred to as a complex radiation field. For many purposes, it is convenient to distinguish between the electromagnetic contribution, the contribution for charged hadrons and the contribution from neutrons.

The electromagnetic component is made up of particles such as photons, electrons and positrons which have radiation lengths of only a few centimeters. Hadronic showers consists mainly of pions (π^+ , π^- , π^0), protons and neutrons that may initiate nuclear reactions if their energy is sufficiently high (approximately 20 MeV in silicon). The spallation process breaks the nucleus into a few large fragments with a high Z that are slowed down on a short length in a dense material. Such an event can thus lead to the deposition of a large amount of energy in a small volume.

The fragments of the struck nuclei produced in the hadronic cascade are radioactive and decay on a timescale between a fraction of a second and many days. The accelerator thus continuously produce radioactivity even though there are no more

circulating beams. These fragments will then become radioactive. This means they emit radiation even when the beams are off.

Figure 5 gives an overview of the distribution of radiation along the LHC ring. Radiation close to the mid-ARC region is expected to come from the beam-gas interactions (yellow colored parts in Figure 5). When the LHC machine will be operational at full luminosity, the beam losses are expected to be lower than 10^7 protons/s. Beam-gas interaction are estimated to be around 10 particles/m/s.

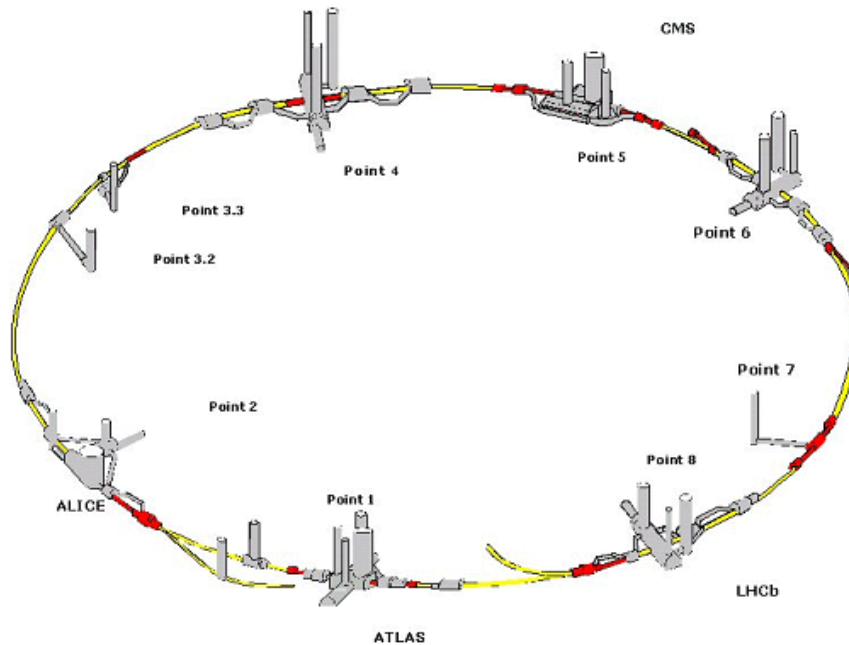


Figure 5 Radiation level around the LHC ring.

Thus, the main source of radiation are the secondary particles generated from the proton collisions of the LHC beams (around 10^9) particles/s. Moreover also the point losses part make an increasingly important contribution (red colored parts of Figure 5).

Depending on the location, the composition and the levels of the radiation fields, and consequently the main radiation effects can be very different. The majority of the LHC electronic equipment is installed in alcoves separated from the beam line by various shielding configuration, e.g. concrete and iron blocks/walls. These alcoves are distributed around the LHC in the various insertion regions. In addition some equipment is also installed directly below or in the vicinity of the beam line

inside the LHC tunnel itself. When evaluating the radiation field, therefore it is important to distinguish between two main categories of areas respectively referred to as shielded areas and tunnel areas.

The most important difference from shielded area and the tunnel ones are the particles energy spectra. In the first one the field is typically dominated by neutrons while in the tunnel areas the contribution is due not only to neutrons but also to other many high energy hadrons such as proton and pions [4].

1.3 Collimation Project

1.3.1 Introduction to collimation project

Each of the two LHC rings will handle a stored beam energy of up to 350 MJ (3×10^{14} p at 7 TeV), two orders of magnitude beyond the achievements in the Tevatron or HERA [5] (Figure 6). This makes the LHC beams highly destructive. At the same time the superconducting (SC) magnets in the LHC would quench at 7 TeV if small amounts of energy (about 30 mJ/cm³, induced by a local transient loss of around 2×10^6 protons) are deposited into the SC coils [5]. A so-called “primary beam halo” will continuously be filled by various beam dynamics processes and the beam current lifetime will be finite. The handling of the high intensity LHC beams and the associated proton loss rates requires a powerful collimation system with the following functionality:

- Halo cleaning: Efficient and reliable cleaning of the beam halo during the LHC beam cycle, such that beam-induced quenches of the super-conducting magnets are avoided.
- Background tuning: Minimization of halo-induced back-grounds in the particle physics experiments.

- Protection: Passive protection of the machine aperture against abnormal beam loss. Beam loss monitors at the collimators detect unusually high loss rates and generate a beam abort trigger.
- Abort gap cleaning: Abort gap cleaning is required for avoiding spurious quenches after normal beam dumps.
- Scraping : Shaping of beam tails and halo diagnostics.

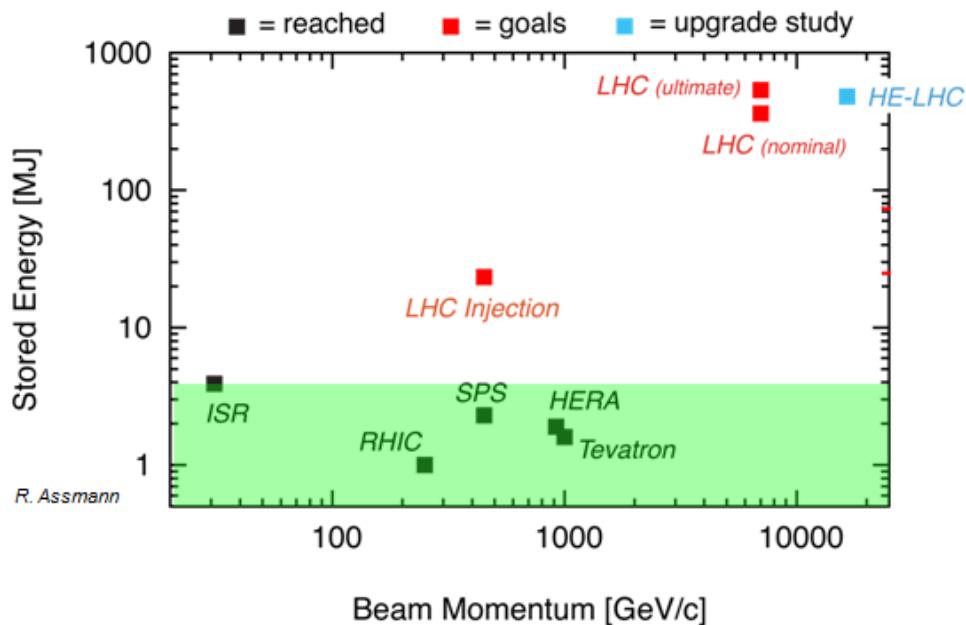


Figure 6. Stored Energy in LHC.

1.3.2 Collimator constraints

Two long straight sections in the LHC are dedicated to collimation ("cleaning insertions"). Some of the collimators design constraints are:

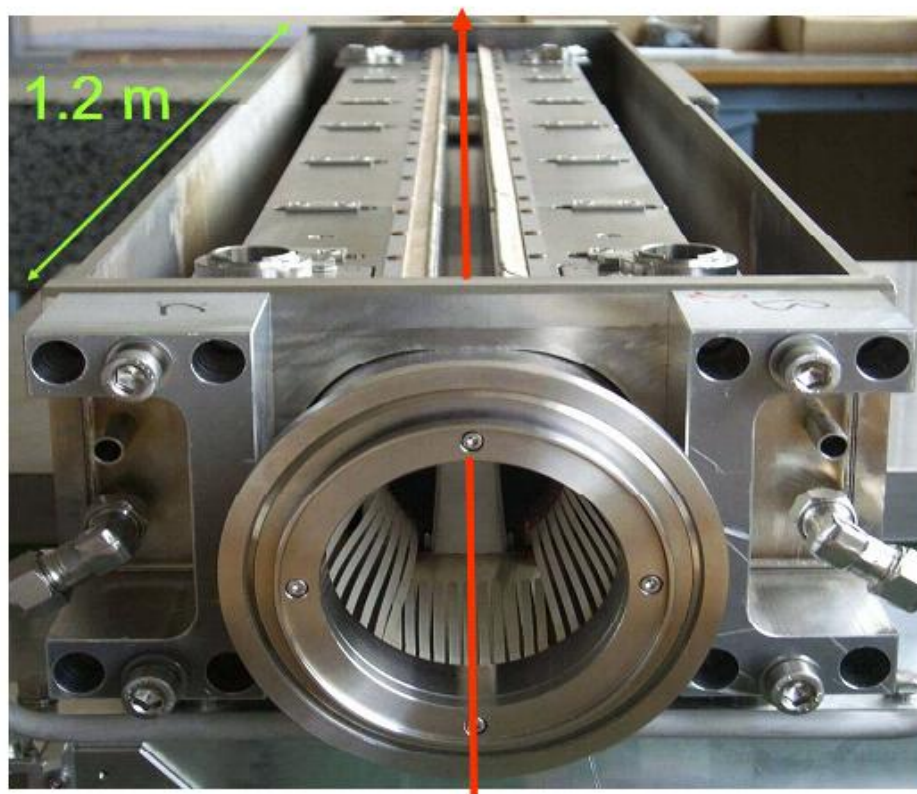
- Efficiency : For achieving high efficiency a proton hitting a secondary collimator must undergo an inelastic interaction with high probability. It is then stopped for circulation. This is traditionally achieved with high Z materials. If a low Z material is used the jaws must be made long.
- Robustness : The collimators must be sufficiently robust to withstand normal and abnormal operational conditions without damage. Shock beam

impact due to mis-kicked beam is expected to occur with 2.7 MJ/mm² over 200 ns at least once per year. It has been shown that carbon-based jaws with a length of up to 1 m provide the required robustness and efficiency.

- Precision: The LHC requires the LHC collimators to be set at around 6 σ for primary and 7 σ for secondary collimators. At 7 TeV nominal optics the beam size is about 200 μm at the collimators, imposing a relative accuracy in setting of primary and secondary collimators of less than 100 μm . Several errors can affect the effective relative accuracy: surface flatness of jaws, collinearity of jaws and beam, accuracy and reproducibility of jaw positioning, orbit drifts and transient beta beat. As errors can be additive, stringent tolerances must be met, e.g. a 25 μm surface flatness is specified over the 1 m long jaw.
- Radiation: Much of the stored LHC beam will end up on the collimators. The LHC collimators and adjacent equipment will become highly radioactive and must be designed for quick handling.

1.3.3 Collimator design

A collimator houses two parallel jaws inside a vacuum box (see Figure 7) The flange-to-flange length of a collimator is standardized at 1.48 m. The rotation of the tank is used to define a horizontal, vertical or skew collimator. The vertical, horizontal and skew collimators perform cleaning in the vertical, horizontal, skew plane through jaws placed perpendicular to the cleaning plane. The jaws are the material blocks put closest to the beam. Different jaw materials identify different collimation types. The jaw is constituted by a flat part, determining the jaw active length, and by 10 cm tapering at both ends to minimize impedance effects. The flat top length of the jaws is always 1.0 m, except for primary (0.6 m) and transfer line collimators (1.2 m).



362 MJ proton beam

Figure 7. View into an open vacuum tank of an LHC Phase I collimator. The two.

Each jaw is supported at its two extremities and movable in order to be centered and aligned with respect to the beam envelope and to follow the change of beam dimensions as a function of the energy. Precise stepping motors are used to move the jaws. Four of these, located at each jaw ends, are used for aperture and angular adjustments, while a fifth motor shifts transversally the whole collimator tank. Movements are monitored independently with precision sensors like Linear Voltage Differential Transformer and resolvers [6]. Excessive tilt of the jaw is prevented by a rack and pinion system. The return springs ensure a semi-automatic back-driving of the jaw in case of motor failure. Figure 8 shows the collimator mechanical integration described above and the sensors' position.

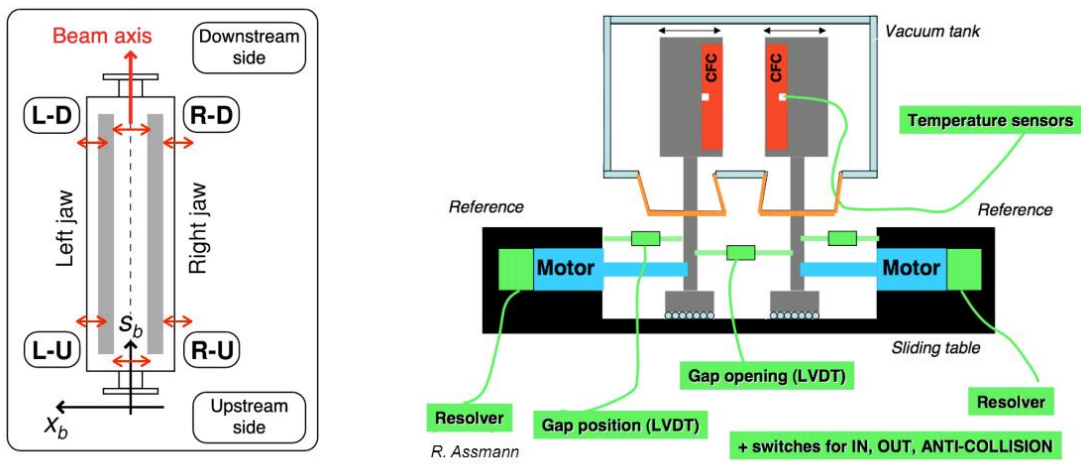


Figure 8. Mechanical drawing of the Collimation systems and components.

Chapter 2

LVDT sensor and radiation effect on electronic devices

In this chapter the linear variable differential transformer (LVDT) and different types of conditioning techniques are presented. The main constraints of the project in terms of position are described taking as reference the working system of the LHC collimators. Finally a description of radiation effect on semiconductor devices and the radiation constraints for this project are reported.

2.1 LVDT sensor

2.1.1 An introduction to LVDT sensor

The linear variable differential transformer is an accurate and reliable method for measuring linear distance. By the end of World War II, the LVDT had gained acceptance as a sensor element in the process control industry largely as a result of its use in aircraft, torpedo, and weapons systems. The publication of *The Linear Variable Differential Transformer* by Herman Schaevitz [7] made the user community aware of the applications and features of the LVDT. It is a position sensor whose output is proportional to the position of a movable magnetic core. It is a contactless sensor with an infinite resolution used in many application such as modern machine-tool, robotics, avionics, and computerized manufacturing.

Practical linear sensors could have a non linearity of less than 0.2% and full scale ranges from less than 1 mm to over 100 mm. Usually an LVDT is sold as a sensing device with an electronic reading circuit as a separate device. Indeed an LVDT that

includes the reading electronic within his housing is called *DC* LVDT because it uses a DC voltage power supply and the output is in DC. The LVDT sensor without the built-in conditioning electronics is called AC LVDT. In this thesis is always considered the bare sensor (AC LVDT).

2.1.2 LVDT Structure

A basic LVDT consists of one primary coil , two secondary coils and a movable core (Figure 1.a -1.b).

The center primary coil and two outer secondary coils are wound on a cylindrical form. The LVDT core normally is a cylinder of magnetically permeable material and provides inductive coupling between the primary coil and the secondary coils. The core moves linearly inside the inner part of the windings.

In the transformer theory, two or more coils are coupled by mutual inductance. If a voltage is impressed to one coil, the voltage produced on a second coil is related to the magnitude of the primary voltage by the ratio of the number of turns of the respective coils. The three coils of an LVDT are wound on a common bobbin. The material of the bobbin has to be selected to give rigidity and stability. When temperature stability is required, the best option is to choose steel made bobbin, due to much lower coefficient of thermal expansion of steel, compared to that of plastic materials. To achieve high accuracy over temperature changes and time, it is recommended to use Layer Wound LVDT (Figure 1.c). In this type of LVDT, there is no separation between secondary coils. The primary coil is neatly wound across the full width of the LVDT. Adhesive material are often used to protect the coils. The housing of the sensor has to shield magnetically the sensor. For this reason a permeable material such as the Nikel-plated steel is use. The core usually is made up of Nikel-Iron alloy, a soft magnetic material [8].

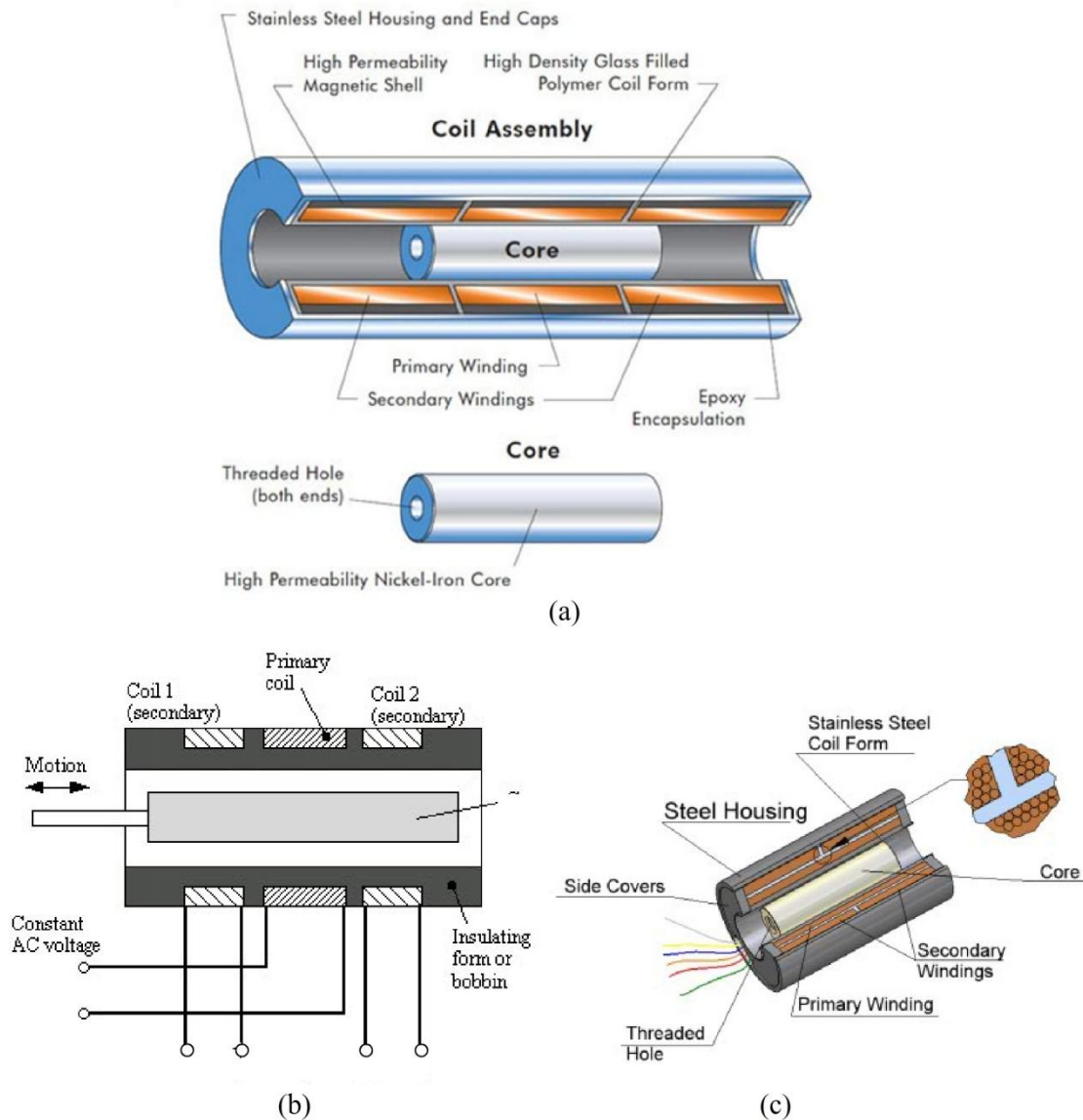


Figure 1. (a) LVDT sensor structure, (b) Sensor basic structure, (c) Layer Wound LVDT.

2.1.3 LVDT working principle

The primary center coil establishes a magnetic flux that is coupled through the core to the secondaries .

When the moving armature is centered between the two series opposed secondaries, equal magnetic flux couples into both secondaries and the voltage induced in one half of the secondary winding is balanced and 180 degrees out of phase with the voltage induced in the other half of the secondary winding. Figure 2 illustrates what happens when the LVDT's core is in different axial positions. The LVDT's primary winding, P, is powered by a constant amplitude AC source. The magnetic flux thus developed is coupled by the core to the adjacent secondary windings, S1 and S2. If the core is located midway between S1 and S2, equal flux is coupled to each secondary so the voltages, E_1 and E_2 , induced in windings S1 and S2 respectively, are equal. At this reference midway core position, known as the null point, the differential voltage output, $(E_1 - E_2)$, is essentially zero. The balanced condition provides total cancellation of secondary voltages and therefore zero voltage output.

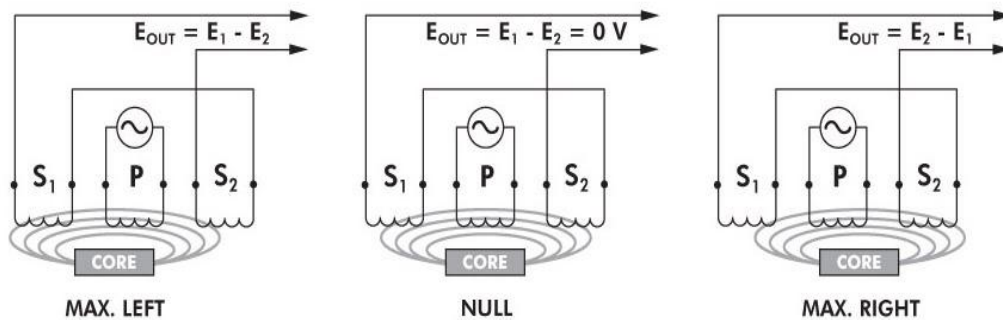


Figure 2. Different position of the core respect to the secondaries.

Figure 3 shows the dynamic of the differential output voltage (E_{out}) respect to the position. The value of E_{OUT} at maximum core displacement from null depends upon the amplitude of the primary excitation voltage and the sensitivity factor of the particular LVDT. The phase angle of this AC output voltage, E_{OUT} , referenced to the primary excitation voltage, stays constant until the center of the core passes the null point, where the phase angle changes abruptly by 180 degrees, as shown graphically in Figure 3.b

This 180 degree phase shift can be used to determine the direction of the core from the null point by means of appropriate circuitry. This is shown in Figure 3, where the polarity of the output signal represents the core's positional relationship to the null point. The Figure 3 shows also that the output of an LVDT is very linear over its specified range of core motion, but that the sensor can be used over an extended range with some reduction in output linearity.

The input and output voltage could be expressed by the following equation.

$$p(t) = A \cos(2\pi f_0 t)$$

$$y_{s1}(t, x) = A_{s1}(x) \cos(2\pi f_0 t + \varphi_1)$$

$$y_{s2}(t, x) = A_{s2}(x) \cos(2\pi f_0 t + \varphi_2)$$

Where $p(t)$ is the input signal and y_{s1} and y_{s2} are the output on the two secondaries. Naturally the output voltage amplitude ($A_{s1}(x), A_{s2}(x)$) depends on the position x .

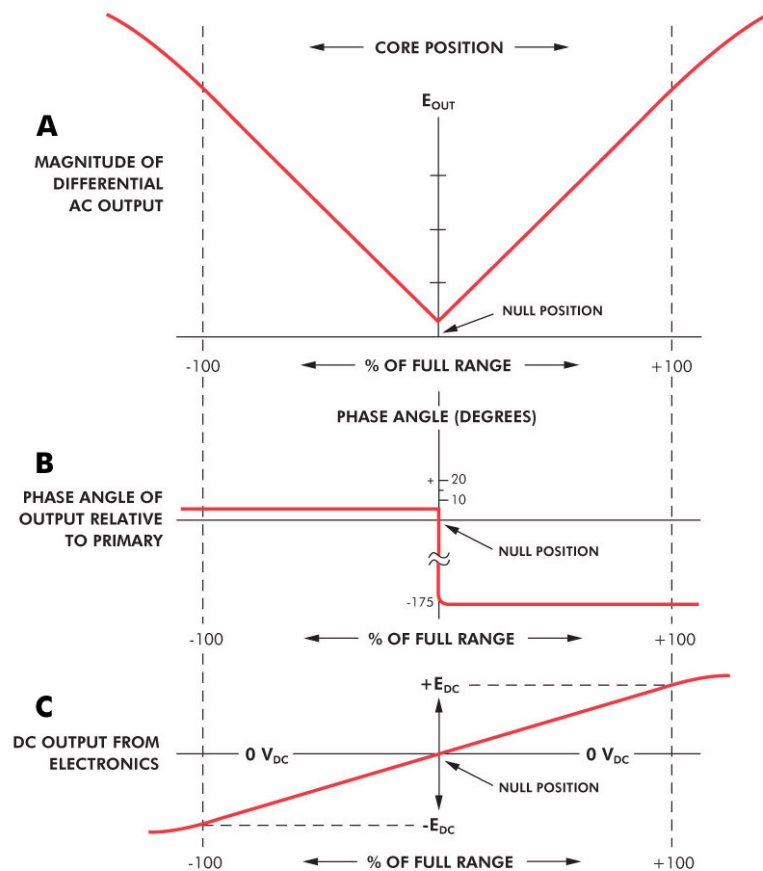


Figure 3. The output characteristics of an LVDT respect different positions.

2.2 LVDT Signal Conditioning Technique

2.2.1 Typical conditioning techniques

Two general styles of LVDT available today are the 4-wire and 5-wire LVDT. The difference between the 4-wire and 5-wire LVDT is that the 5-wire design includes an additional wire which represents the connection point (center tap) for both secondary windings, allowing the voltage at both windings to be computed relative to the center tap. The signal at the output terminals of a 4-wire LVDT is the difference of the secondary windings. The 4-wire LVDT does not have a center tap available.

There are many resources available on LVDT signal conditioning. The only available commercial solutions found are the Analog Devices AD598 and AD698 integrated circuits.

A simple signal conditioning circuit is shown in Figure 4 where the absolute values of the two output voltages are subtracted. Using this technique, both positive and negative variations about the center position can be measured.

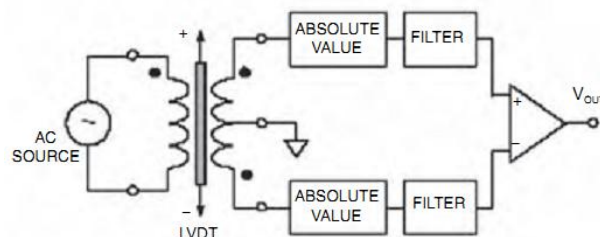


Figure 4. Simple conditioning circuit for the LVDT sensor reading.

While a diode/capacitor-type rectifier could be used as the absolute value circuit, the precision rectifier shown in Figure 5 is more accurate and linear. LVDT connected to a synchronous detector that rectifies the sine wave and presents it at the output as a DC signal.

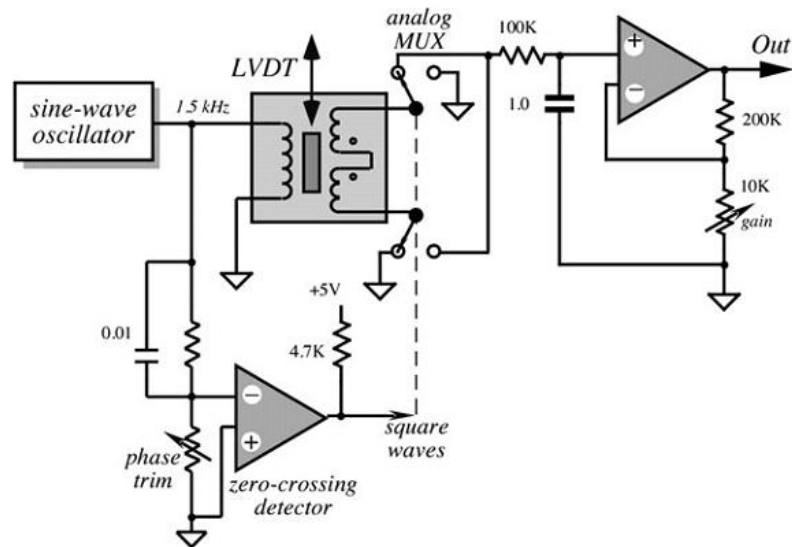


Figure 5. Conditioning circuit with precision rectifier.

The synchronous detector is comprised of an analog multiplexer (MUX) and a zero-crossing detector, which converts the sine wave into the square pulses compatible with the control input of the multiplexer. A phase of the zero-crossing detector should be trimmed for the zero output at the central position of the core. The output amplifier can be trimmed to a desirable gain to make the signal compatible with the next stages. The synchronized clock to the multiplexer means that the information presented to the RC-filter at the input of the amplifier is amplitude and phase sensitive. The output voltage represents how far the core is from the center and on which side.

The industry standard AD598 LVDT signal conditioner [9] shown in Figure 6 (simplified form) performs all required LVDT signal processing. The on-chip excitation frequency oscillator can be set from 20 Hz to 20 kHz with a single external capacitor.

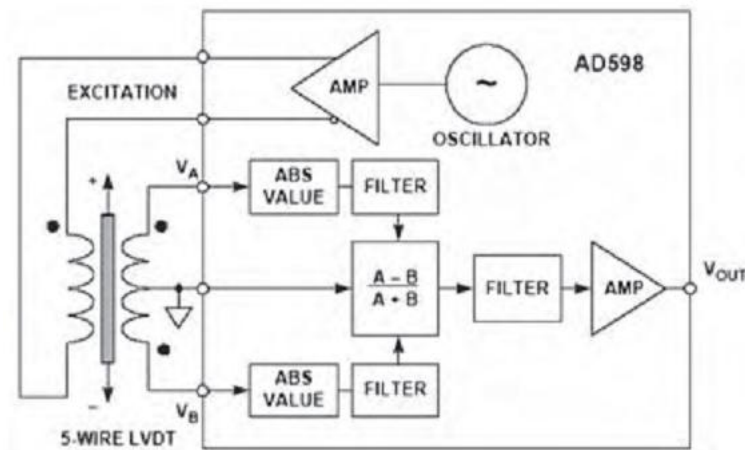


Figure 6. Schematic of commercial conditioning circuit AD598.

Two absolute value circuits followed by two filters are used to detect the amplitude of the A and B channel inputs. Analog circuits are then used to generate the ratiometric function $[A-B]/[A+B]$. Note that this function is independent of the amplitude of the primary winding excitation voltage, assuming the sum of the LVDT output voltage amplitudes remains constant over the operating range. This is usually the case for most LVDTs, but the user should always check with the manufacturer if it is not specified on the LVDT data sheet. Note also that this approach requires the use of a 5-wire LVDT. An external resistor sets the AD598 excitation voltage from approximately 1 V rms to 24 V rms. Drive capability is 30 mA rms. The AD598 can drive an LVDT at the end of 300 feet of cable, since the circuit is not affected by phase shifts or absolute signal magnitudes. The position output range of V_{OUT} is ± 11 V for a 6 mA load and it can drive up to 1000 feet of cable. The V_A and V_B inputs can be as low as 100 mV rms.

The AD698 LVDT signal conditioner [10](see Figure 7) has similar specifications as the AD598 but processes the signals slightly different. Note that the AD698 operates from a 4-wire LVDT and uses synchronous demodulation. The A and B signal processors each consist of an absolute value function and a filter. The A output is then divided by the B output to produce a final output which is ratiometric and independent of the excitation voltage amplitude. The problem with AD698 is

the phase shift the secondaries can have respect the primary. The secondaries output can be expressed by:

$$y(t) = A(x) \cos(2\pi f_0 t + \varphi)$$

The synchronous demodulation is obtained by multiplying a signal synchronous with the carrier and low pass filtering:

$$\begin{aligned} [y(t) \cos(2\pi f_0 t)]_{\text{lowpass}} &= [A(x) \cos(2\pi f_0 t + \varphi) \cos(2\pi f_0 t)]_{\text{lowpass}} \\ &= \left[A(x) \frac{\cos(\varphi)}{2} + A(x) \frac{\cos(4\pi f_0 t + \varphi)}{2} \right]_{\text{lowpass}} = A(x) \frac{\cos(\varphi)}{2} \end{aligned}$$

The results is a function of the phase difference φ that depends from the cable length used to drive the sensor. A manual tuning is therefore needed at installation to compensate the phase error related to different cable lengths.

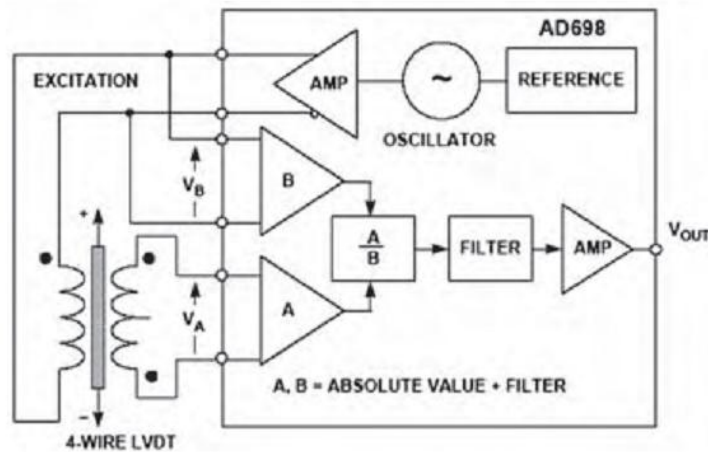


Figure 7. Schematic of commercial conditioning circuit AD698.

Another real-time digital signal processing (DSP) method of LVDT signal conditioning that achieves better linearity than the AD598 uses the spectral estimation (SE) of the magnitude of the output sine waves [11]. This algorithm tends to remove all the supposition about considering the sum of the two secondaries independent on the position of the core of the LVDT. When spectral estimation is used, the main problem is the computational load. If great accuracy is required, a large number of sample is to be considered. Besides, the frequency

spectrum is discrete and generally does not include the exact value f_p of the carrier, requiring complex windowing and interpolation techniques as a consequence. If 2^n samples of a sinusoidal signal at frequency f_p have been acquired at sampling frequency f_s , the 2^n frequency points f_k of the spectrum are:

$$f_k = k * \frac{f_s}{2^n} \quad k=0,1,\dots,n-1$$

If the sinusoidal signal applied at the primary coil respects equation above, that is $f_p = k * f_s / 2^n$, the window period $T_w = 2^n / f_s$ is equal to a multiple, by k , of periods of the signal ($2^n / f_s = k / f_p$), avoiding spectral leakage.

It is convenient to apply the Goertzel algorithm instead of computing the FFT related to the whole spectrum. The Goertzel algorithm is a recursive method to calculate the DFT and it can be split in two phases depicted in Figure 8: a feedback phase, that performs a second degree filter and a feedforward phase, where $x(n)$ are the samples, v_k is the output of the feedback phase after processing the n^{th} sample and the filter's output $y_k(N)$ is the k^{th} point of the frequency spectrum composed by $N=2^n$ points.

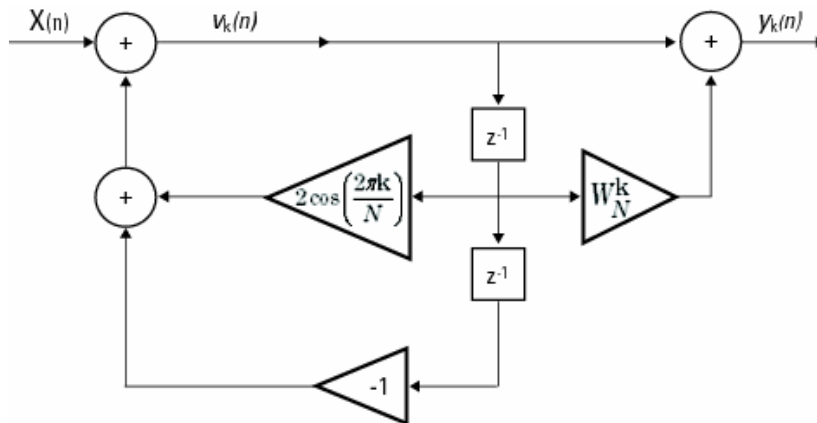


Figure 8. Goertzel Algorithm diagram.

The time domain difference equations for the Goertzel algorithm are:

$$v_k(n) = \cos\left(\frac{2\pi k}{N}\right) v(n-1) - v(n-2)$$

$$y_k(n) = W_N^k v(n-1) + v(n) \quad W_N^k = -e^{\frac{2\pi k}{N}}$$

Naturally from the output is necessary to calculate the magnitude of the result.

A possible solution can be implemented using a DSP processor and a AIC (Analog Interface Circuit), composed by a DAC (Digital to Analog Converter) followed by a reconstruction filter and two multiplexed channels with band-pass filter and an ADC as depicted in Figure 9.

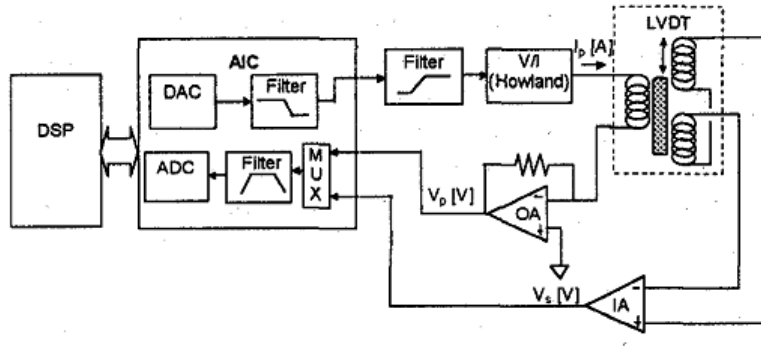


Figure 9. Schematic of a possible solution for the Spectral Estimation technique.

2.3.2 The Sine Fit conditioner

As seen for the Spectral Estimation technique after N samples of the acquired signal it is possible to retrieve a position of the core of the LVDT. Instead of a spectral analysis, a filtering and fitting algorithm can be used. The concept is to acquire N samples of the input sine wave and find the best sine wave that fits the input one. This technique is called the Sine Fit algorithm and can be used to calculate the magnitude of the secondary voltages without the drawbacks of spectral leakage. In the standards IEEE 1241-2000 [12] and IEEE 1057-1994 [13] used for the characterization of ADC, three and four parameter Least Squares (LS) model fitting procedures are proposed. The differences between the three parameter and four parameter algorithm is the number of unknown variable. In the four parameter algorithm the amplitude A , the phase ψ , the offset O and the frequency f are unknown. In the three parameter the frequency of the input sine wave is known. All these methods are based on an error sequence minimization and the properties of

ADC are calculated from this error sequence. The three parameter algorithm is analyzed in this section. Considering an input sine wave of frequency f_0 from N of its samples $y_0, \dots, y_{N-1}, y_N$, acquired at constant time instant $t_0, \dots, t_{N-1}, t_N$, the error that the algorithm tends to minimize is:

$$e = \sqrt{\sum_{n=1}^N [y_n - A \cos(2\pi f_0 t_n) - B \sin(2\pi f_0 t_n) - C]^2}$$

Then the best estimate for the input sine is :

$$g(t) = A \cdot \sin(2\pi f_0 t + \Psi) + O$$

Where A, Ψ and O are:

$$A = \sqrt{A^2 + B^2}$$

$$\Psi = \arctan(A, B)$$

$$O = C$$

Is possible to formulate a matrix expression of the error:

$$e^2(\mathbf{x}_0) = (\mathbf{y} - \mathbf{D}_0 \mathbf{x}_0)^T (\mathbf{y} - \mathbf{D}_0 \mathbf{x}_0)$$

Where :

$$\mathbf{y} = \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_N \end{bmatrix}, \mathbf{x}_0 = \begin{bmatrix} A \\ B \\ O \end{bmatrix}, \mathbf{D}_0 = \begin{bmatrix} \cos(2\pi f_0 t_1) & \sin(2\pi f_0 t_1) & 1 \\ \cos(2\pi f_0 t_2) & \sin(2\pi f_0 t_2) & 1 \\ \vdots & \vdots & \vdots \\ \cos(2\pi f_0 t_N) & \sin(2\pi f_0 t_N) & 1 \end{bmatrix}$$

The minimization formula:

$$\nabla_{\mathbf{x}_0} [(\mathbf{y} - \mathbf{D}_0 \mathbf{x}_0)^T (\mathbf{y} - \mathbf{D}_0 \mathbf{x}_0)] = \mathbf{0}$$

led to the result $\widetilde{\mathbf{x}}_0$:

$$\widetilde{\mathbf{x}}_0 = (\mathbf{D}_0^T \mathbf{D}_0)^{-1} \mathbf{D}_0^T \mathbf{y} = \mathbf{D}_0^\dagger \mathbf{y}$$

Estimating the amplitude of the two secondaries A_1 and A_2 is possible to retrieve the position of the core calculating the ratiometric as:

$$r(x) = \frac{A_1(x) - A_2(x)}{A_1(x) + A_2(x)}$$

With this algorithm the phase difference between the primary and secondary could be neglected. Moreover it gives the best results in terms of immunity to noise. The uncertainty of the measurements is function of the number of acquired samples and the amount of noise present. Let's consider 2000 samples of an input sine wave of unit amplitude at a 2500 Hz sampled at $f_s = 250$ Ksps with an ideal 16 bit ADC converter. The uncertainty on the amplitude estimation calculated on 500 repetition respect different amount of additive white Gaussian noise is depicted in Figure 10.

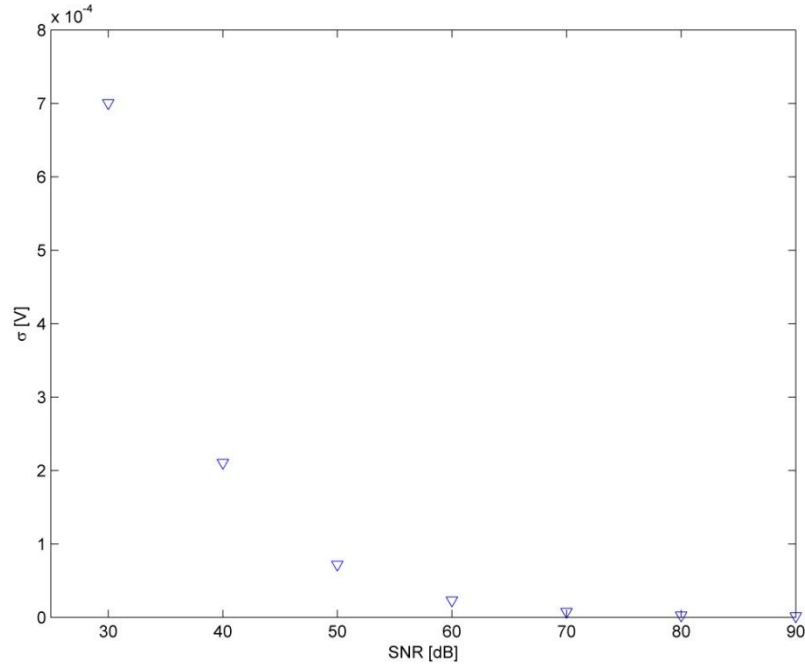


Figure 10. Uncertainty on amplitude estimation respect different value of SNR.

Another feature of the Sine Fit algorithm is immunity to crosstalk. Indeed the Sine Fit computes an average over the sampling window. An analytic formula of the frequency response of the algorithm is [14] :

$$A(f) \cong \sqrt{\left(\frac{f_s}{\pi N \Delta f} \sin\left(\frac{\pi N \Delta f}{f_s}\right)\right)^2} = \left| \text{sinc}\left(\frac{\Delta f N}{f_s}\right) \right|$$

As shown in Figure 11 it is possible to choose a set of input frequency not interfering to each other. Let's introduce Δf_{zero} :

$$\Delta f_{zero} = \frac{f_s}{N}$$

An input sine with a frequency spaced by an integer number of Δf_{zero} from the design frequency f_0 will not perturb the estimation of the f_0 tone amplitude. In order to ensure orthogonality of the LVDTs channels, multiple non-interfering frequency could be chosen to excite the LVDTs on the same cable and different Sine Fit algorithm parameters are necessary.

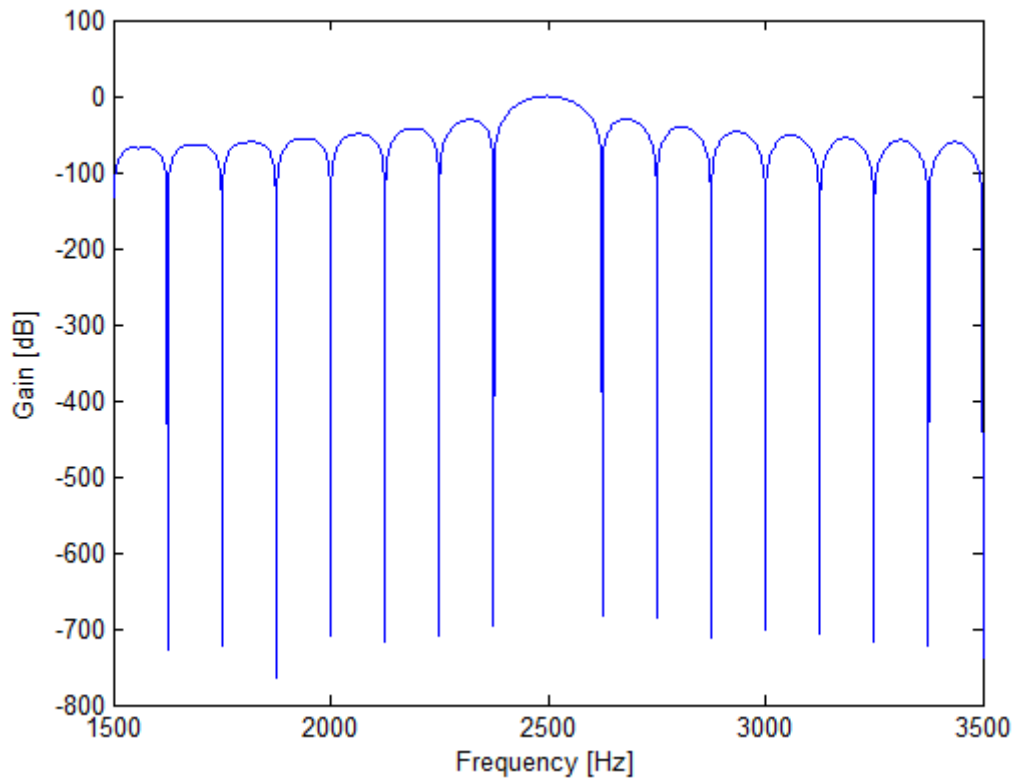


Figure 11. Frequency response of Sine Fit amplitude estimation.

2.3 Main requirements of the acquisition system and interface

The LVDT and the reading system of the LHC collimators assured a remarkable performances in terms of repeatability. Here details of such a system are given to fix the target specifications for the LVDT conditioner described in this work.

To compare the results obtained is necessary a reliable and precise working system. The system taken as reference is the collimators system, in particular the Position Readout and Survey (PRS) in the low level control system (LLCS) of the LHC collimators [15]. The LLCS is responsible of the accurate synchronization of 500 axes of motion at microsecond level. The required uncertainty of positioning for the LHC collimator jaws is one tenth of the beam core diameter, which at nominal energy is of the order of 200 millimeters, resulting in a demanded uncertainty of 20 micrometers. Another specification to be respected is the possibility to position any jaw within a well defined angle with respect to the nominal beam trajectory. To satisfy this requirement, each jaw can be moved on both ends by stepping motors. In order not to excite dangerous mechanical vibration, it is necessary to perfectly synchronize the two motors on each jaw at better than 1 millisecond. Jaws in different collimators need to respect movement functions sent by a central supervisory application which is not part of the LLCS. Each jaw must follow its given function within the already stated tolerance of 20 μm . With the nominal motor speed of 400 steps per second, and a reduction factor of 2 mm/revolution, this means that any motor (more than 500 overall) in the LLCS has to be synchronized within 10 ms all along the operation of the LHC. Each motor is equipped with a resolver to detect lost steps in order to check the consistency of the actual movement with the desired movement function. An LVDT is installed on each axis to measure the absolute position of each jaw extremity. The LVDTs also enable measurement of the distance between two jaws within the same collimator. A further difficulty is posed by the environmental conditions of the LHC. Due to the high level of radiation expected in the proximity of the collimators (several MGrays/year), no electronics can be embedded in the sensors or in the motors.

Furthermore, radiation safe alcoves for the installation of the driving electronics can be up to 800 m far from the collimator itself, generating a complex matching problem for conditioning electronics. Over such long distances the impedance of the cable may in fact transform the impedance of the sensor from inductive to capacitive. For early detection of any lost step the resolver reading must be fast and synchronous to the movement. LVDT readings are required to be fast in order to minimize the risk of undetected errors in jaw positioning.

The requirements in terms of the real-time behavior of the PRS are:

- 1) an uncertainty of positioning and reading of 20 μm in any condition and at any temperature;
- 2) frequency of monitoring of the LVDTs: 100 Hz.

The PRS is the module responsible for checking that the actual position corresponds to the desired one within a well defined tolerance, depending on the beam energy and the jaw position, received by the supervisory system. The position is read on LVDTs with a accuracy of better than 20 μm and at rate of up to 100 Hz. In case of problems, it aborts the beam

In conclusion the Table 1 summarize all the requirements of the collimation system and the measured performance of the actual system.

	Required	Measured
Position sensors reading uncertainty	20 μm	below 10 μm
Frequency of monitoring	100 Hz	100 Hz

Table 1. Summary of the position constraints of the PRS system.

2.4 Radiation effect and constraints

2.4.1 Radiation effect on semiconductor devices

The materials used for the LVDT make the sensor itself completely insensible to radiation environment. So the sensor is radiation hard. What makes the positioning system not reliable in radiation environment is the conditioning electronics. In this section a brief summary of radiation effect on semiconductor devices is given.

When an electronic circuit is exposed to radiation, in general there is a permanent or transient modification of the electrical properties of the active components of the circuit that can bring degradation of performances or a catastrophic failure.

The fundamental mechanisms that determine the radiation damage in Si, SiO₂ are:

- Ionization: Energy absorbed by electronic ionization in insulating layers, predominantly SiO₂, liberates charge carriers, which diffuse or drift to other locations where they are trapped, leading to unintended concentrations of charge and, as a consequence, parasitic fields.
- Displacement effect: Incident radiation displaces silicon atoms from their lattice sites. The resulting defects alter the electronic characteristics of the crystal.

Both mechanisms are important in integrated circuits. Some devices are more sensitive to ionization effects, some are dominated by displacement damage. Hardly a system is immune to either one phenomena and most are sensitive to both. These fundamental effects give rise to a degradation of performance which may or may not recover over periods of months.

The displacement damage is proportional to Non-Ionizing Energy Loss (NIEL) that depends on the particle type and energy. Non-ionizing energy loss has been calculated for a variety of particles over a large energy range and

Table 2 gives a comparison of displacement damage for several types of radiation [16].

Particle	proton	proton	neutron	electron	Electron
Energy	1 GeV	50 MeV	1 MeV	1 MeV	1 GeV
Relative Damage	1	2	2	0.01	0.1

Table 2. Displacement damage for several types of radiation

Displacement damage manifests itself in multiple way: formation of mid-gap states , creation of state close to the band and a change in doping characteristic. Usually the inter-band transition in Si needs momentum transfer because of the indirect band-gap, so direct transitions from the valence band to conduction band are extremely improbable. The introduction of mid-gap provides a new level for capture and emission processes. The devices most affected by this radiation damage are diode, transistor in bipolar technology , photodiode.

The ionization, also referred as total ionizing dose (TID) mainly forms electron-hole pairs in the Si. Absorbed dose is quantified using either a unit called the *rad* (an acronym for radiation absorbed dose) or the SI unit which is the gray (Gy); 1 Gy = 100 rads = 1 J/kg. The valence band electrons in the solid are excited to the conduction band and, if an electric field is applied, are highly mobile. Any solid, even an insulator, thus conducts for a time at a level higher than is normal. The positively charged holes are also mobile, but to a different degree. The production and successive trapping of the holes in oxide films cause serious degradation in MOS and bipolar devices [16]. The effect of charges trapping in MOS device is a shift in voltage threshold that can even led to a system failure. A special case of ionization effect are the Single Event Effects (SEE) mainly caused by a single, energetic particle, and they can take on many forms. *Single event upset* (SEU) is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particle lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs.". SEUs are transient soft errors, and are non-destructive. A reset or rewriting of the device results in normal device behavior thereafter. An SEU may occur in analog, digital, or optical components, or

may have effects in surrounding interface circuitry. SEUs typically appear as transient pluses in logic or support circuitry, or as bit flips in memory cells or registers. Also possible is a *multiple-bit SEU* in which a single ion hits two or more bits causing simultaneous errors. Multiple-bit SEU is a problem for single-bit *error detection and correction* (EDAC) where it is impossible to assign bits within a word to different chips (*e.g.*, a problem for DRAMs and certain SRAMs).

Besides soft events, destructive events might also occur. They are Single Event Latch-up affecting CMOS technology. The device is destroyed by an increase of the current of the power supply [17].

Power switches, such as Mosfet, IGBT, GTO, BJT can suffer of destructive events too; they can suffer of Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR) [17].

The ecosystem of radiation effects on semiconductor devices is shown in Figure 12

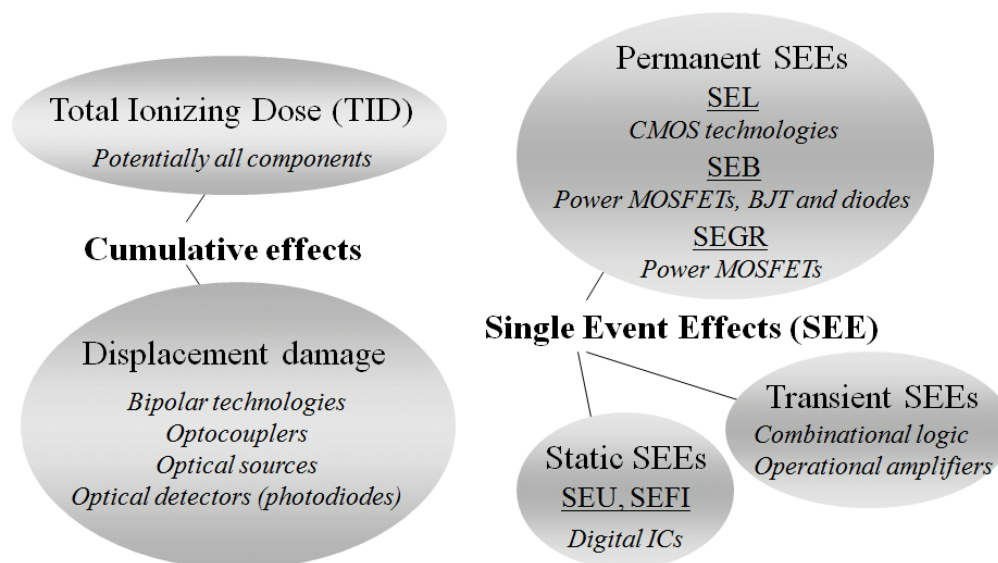


Figure 12. Ecosystem of the radiation effects divided in cumulative effects and single event effects.

The SEU effects are the very important ones in digital electronics so the basic mechanism is analyzed in more detail.

There are two primary methods by which ionizing radiation releases charge in a semiconductor device: direct ionization by the incident particle itself and ionization by secondary particles created by nuclear reactions between the incident particle and the struck device. Charge deposition is function of a particle's LET (linear energy transfer) which has the dimensions of $\text{MeV cm}^2 \text{g}^{-1}$. Both mechanisms can lead to integrated circuit malfunction. Hence the ionization induces a current pulse in a p-n junction. The charge injected by the current pulse at a sensitive 'off' node of a bistable data storage element may exceed the critical charge required to change the logic state of the element. The mechanism of current pulse generation is shown in Figure 13. The resulting change of state is what previously called a 'bit-flip'.

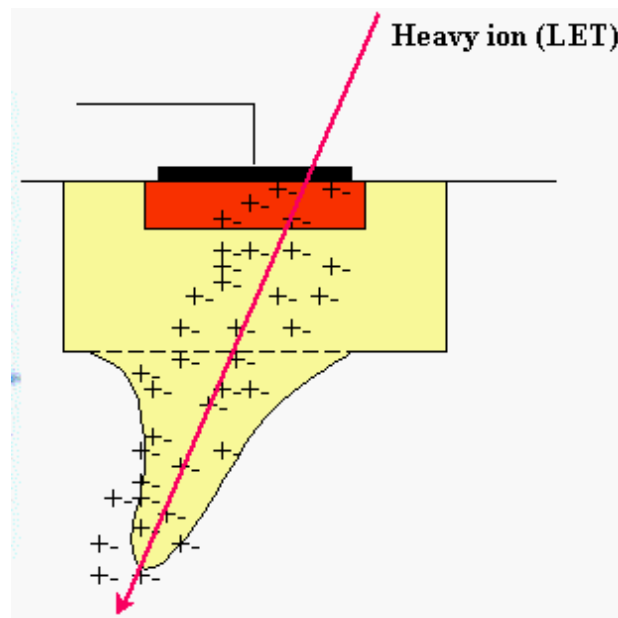


Figure 13.

The vulnerability of a device to SEU is defined by two parameters: threshold LET and saturated cross section [16]. The last one is when all incident ions are capable of producing an upset and no increase in upset rate is seen for an increase in LET. The cross section has a dimension of cm^2 and is a function of the surface area of the sensitive nodes. In the case of a proton beam irradiation, the cross-section of a device is calculated as the ratio of the number of SEU over the proton fluence and as a function of the incident proton energy

$$\sigma = \frac{N_{SEU}}{\Phi} [cm^2]$$

Where Φ is the fluence expressed as particles/cm².

2.4.2 Radiation Tolerant device constraints

The differences between Radiation Hard devices and Radiation tolerant ones is usually the maximum total ionizing dose acceptable. The radiation hard devices for space application usually are guarantee up to 300 krad. Most radiation hardened chips are based on their commercial equivalents, with some manufacturing and design variations that reduce the susceptibility to interference from radiations.

Usually the technique used to hardened a device can be physical and logical [18]. Some examples of physical techniques include: the manufacturing on insulating substrates instead of the usual semiconductor wafers, shielding the package against radioactivity, capacitor-based DRAM is often replaced by more rugged (but larger, and more expensive) SRAM. The logical techniques can be: the insertion of redundant elements used at the circuit level, built-in Error Detection and Correction module in RAM block.

A radiation tolerant devices are guaranteed for less total ionizing dose and usually do not differs from a component off the shelf (COTS). Moreover at CERN many radiation campaigns aim at testing if they respect the radiation constraints. If the devices pass the tests can be named as radiation tolerant[19].

In this work radiation tolerant devices and off the shelf components are used, hence the radiation constraints should be achieved. The constraints given are in terms of total ionizing dose and maximum fluence achievable. The maximum total ionizing dose is 100 Gy and the maximum achievable fluence is 10¹¹ pp/cm². The devices under test are discussed in the Chapter 3 and the experimental results are given in Chapter 4.

Chapter 3

Proof demonstrator and numerical algorithm design

In this Chapter, the algorithm employed for the LVDT reading of the collimator system is recalled. This system is used as reference for the target specifications. Afterwards, the proof demonstrator of the LVDT conditioner is described giving the rationale for the choice of the main devices, such as the FPGA and the ADC. Then, a detailed analysis of the numerical algorithm to be implemented on the FPGA is presented highlighting the techniques employed to reach the required target of numeric resolution of $0.5\ \mu\text{m}$.

3.1 The LVDT conditioner architecture

3.1.1 The LVDT conditioning of the collimation system

In the previous chapter the Positioning Readout and Survey system has been analyzed. The performances of this system are used to compare the results from the novel architecture. Hence a deeper analysis of the actual acquisition and conditioning system is mandatory. The main task of this system is to retrieve the position of the jaws of the collimator in real time. On each collimator 7 LVDTs measure the position of the jaws, 4 of them measure the absolute position, while 2 measure the gap between the jaws and the last one measure the height of the jaws. The main requirements, as already stated, is an uncertainty on the position of less

than $20\ \mu\text{m}$ with a survey frequency of 100 Hz. The actual system is based on National Instrument PXI platform running Lab-View RT. The hardware architecture of a PRS for three collimators is shown in Figure 1.

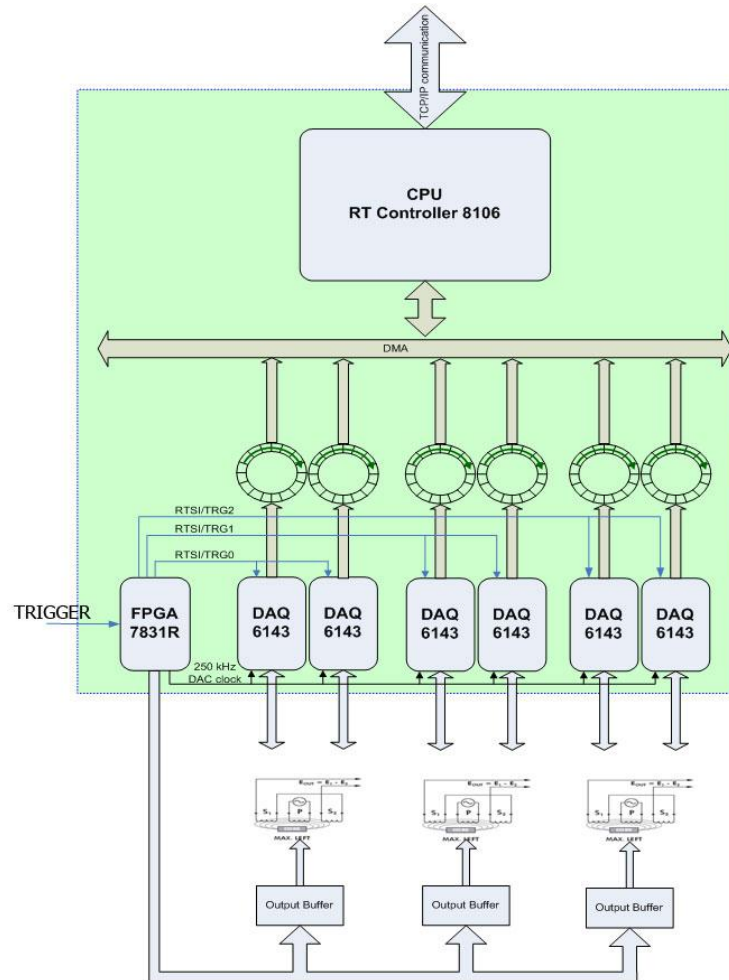


Figure 1. The PRS readout system architecture for the LVDT conditioning

An RT controller 8106 based on an Intel® Core 2 Duo Processor at 2.16 GHz is used to serve up to three collimators. Two DAQ cards NI PXI 6143 with 8 simultaneous differential analog inputs sampled at 16 bit and 250 kS/s is used to acquire the 14 signals coming from the secondary coils of the 7 LVDTs installed on each collimator. Data acquired are transferred to the CPU via DMA using circular buffers. In this way the LVDT signal acquisition is a background process and at each cycle the CPU reads the samples array needed for the demodulation from the circular buffer. An FPGA

card NI PXI 7831R having 8 analog outputs is used to generate the feeding signals for the 21 LVDTs. The frequencies of the 7 sine waves generated are orthogonal with respect to the frequency response of Sine Fit algorithm used for sine wave demodulation in order to reduce the crosstalk between LVDTs of the same collimator (see Chapter 2).

We can divide the performance of the actual system in timing performance and performance on position. The specification for the timing is a survey each 10 ms (100 Hz survey frequency). Considering that an acquisition of 2000 samples takes 8 ms at 250 Ksps, the Sine Fit algorithm should compute the results in less than 2 ms for 21 LVDTs. From the measurement done on the PRS system the Sine Fit Algorithm is computed in less than 1,5 ms with a negligible jitter of 50 μ s, so the 100 Hz specification can be easily satisfied.

The performance on the position is very satisfying because all the digital processing is done with floating point data type with a negligible effect of data quantization (word length effect). The typical uncertainty over 100 repeated measurement is about 0.3 μ m. Moreover other cause of the uncertainty like temperature drift (estimated 1 μ m /C°) could be directly compensated thanks to a PT100 sensor already built-in inside the LVDT.

The Sine Fit algorithm implemented in the CPU part works with matrix format as seen in Chapter 2. The whole matrix computation is left to the CPU but a considerable effort was done to speed up the algorithm.

The main optimization is in the calculation of the pseudo-inverse matrix $\mathbf{D}_0^\dagger$. Because only the secondaries amplitudes are needed to calculate the ratiometric the matrix $\mathbf{D}_0$ can be further simplified to an $N \times 2$ instead of $N \times 3$ (where N are the total number of samples) [14]. For a single secondary we have:

$$D_0 = \begin{bmatrix} \cos(2\pi f_0 t_1) & \sin(2\pi f_0 t_1) \\ \cos(2\pi f_0 t_2) & \sin(2\pi f_0 t_2) \\ \vdots & \vdots \\ \cos(2\pi f_0 t_N) & \sin(2\pi f_0 t_N) \end{bmatrix}; x = \begin{bmatrix} A_c \\ A_s \end{bmatrix}$$

Where f_0 is the input frequency, and x is the vector with the component in phase with a cosine A_c and a sine A_s .

For L LVDTs an $N \times 2L$ matrix is created and pseudoinverted.

$$D_L = [c_{f_1} s_{f_1} \cdots c_{f_L} s_{f_L}]$$

Where :

$$c_{f_j} = \begin{bmatrix} \cos(2\pi f_j/f_s) \\ \vdots \\ \cos(2\pi f_j N/f_s) \end{bmatrix} \quad s_{f_j} = \begin{bmatrix} \sin(2\pi f_j/f_s) \\ \vdots \\ \sin(2\pi f_j N/f_s) \end{bmatrix}$$

Where f_j is the input frequency and f_s is the sampling frequency.

Moreover is possible to group all the L LVDTs reading value in one matrix Y_L of size $N \times 2L$ and compute the matrix multiplication resulting in an $2L \times 2L$ matrix. The X_L matrix of amplitude have a diagonal structure:

$$X_L = \text{diag}(A_{f_1}^{(s_1, s_2)}, \dots, A_{f_L}^{(s_1, s_2)})$$

$$A_{f_j}^{(s_1, s_2)} = \begin{bmatrix} A_{c_{f_j}}^{s_1} & A_{c_{f_j}}^{s_2} \\ A_{s_{f_j}}^{s_1} & A_{s_{f_j}}^{s_2} \end{bmatrix}$$

The superscript s_1 and s_2 are related to the two secondaries.

Finally the results is given by:

$$X_L = D_L^\dagger Y_L$$

3.1.2 Architecture of the proof demonstrator

The main problem with the previously shown architecture is the radiation constraints. The PXI system is situated in the alcoves, far from the main sources of radiations but is not tolerant to them.

Beam targets and absorbers are widely used in all the main rings of CERN and position sensors are employed to control their position. One of the most reliable position sensor is the LVDT. There are zones in the other accelerator rings, such as the SPS, where the electronics cannot be protected in dedicated alcoves.

Therefore, a new board is required to be a generic acquisition card with numerical processor capabilities for reading LVDT or other position sensors. The architecture of a proof demonstrator is shown in Figure 2.

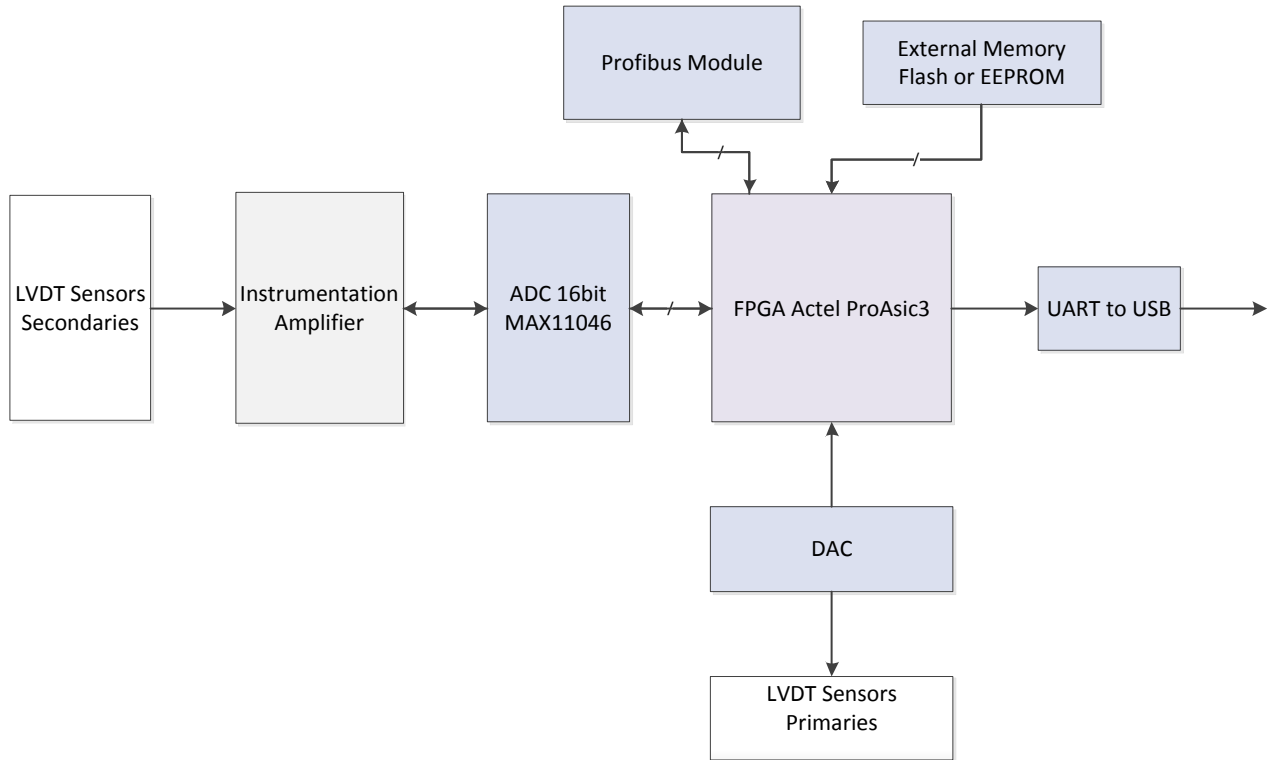


Figure 2. New architecture proposed for the LVDT conditioning.

3.1.3 Choice of the FPGA and ADC

The core of the project is an FPGA, not more a CPU. The type of FPGA technology and device family used in a design is a key factor for system reliability. The choice of an FPGA is mandatory because of the needing of digital processing power and due to radiation constraints. There are basically three types of FPGA technologies currently in existence: antifuse-based, flash-based, and SRAM-based.

The market of the FPGA is dominated by SRAM based device, characterized by very high densities of logic cell. The drawbacks of this technology are the power consumption and the volatile memory used to store the bit stream configuration.

This means that at every power-up an external configuration is loaded via a non-volatile memory (FLASH or EEPROM). The FLASH based FPGA, on the other hand, do not need any configuration memory outside the chip because the bit stream configuration is saved in the flash memory of the device. In Figure 3 the two different architectures of FPGA are depicted. The FLASH based FPGA are characterized by a lower densities of logic cell. This brings most of the designer to choose SRAM based designed that offers more flexibility. The Anti-fuse FPGA are one time programmable only device. The antifuse is a device that doesn't conduct current initially, but can be “burned” to conduct current (the antifuse behavior is thus opposite to that of the fuse, hence the name). The antifuse-based FPGA can't be then reprogrammed since there is no way to return a burned antifuse into the initial state.

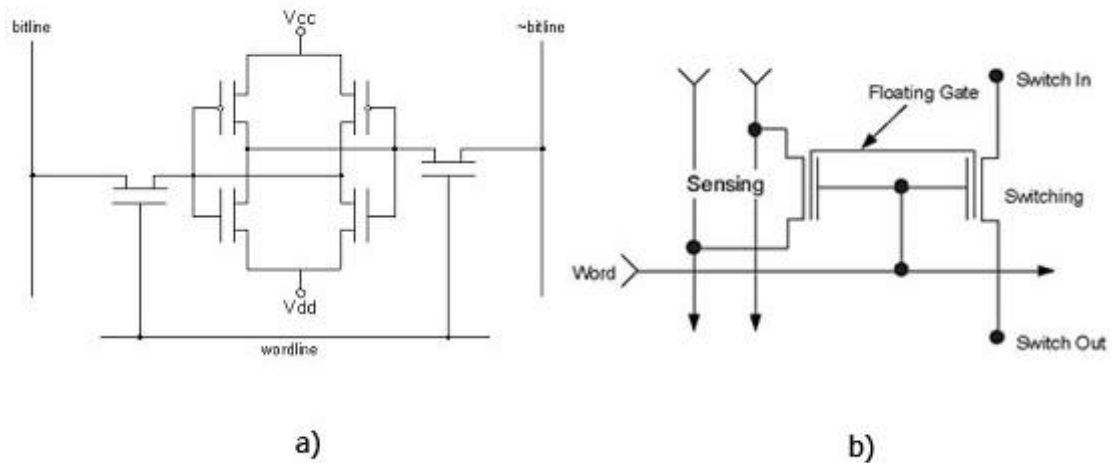


Figure 3. a) SRAM based cell of an FPGA b) Flash based cell of an FPGA

The three main brand of FPGA are Xilinx , Altera and Actel. The first two use SRAM technology, the third one use a 130 nm FLASH process to fabricate its devices. The choice of the FPGA falls on the Actel ProAsic 3 family [20]. The characteristics of this family are in Table 1

ProASIC3 Devices	A3P015	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Cortex-M1 Devices					M1A3P250	M1A3P400	M1A3P600	M1A3P1000
System Gates	15,000	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000
Typical Equivalent Macrocells	128	256	512	1,024	2,048	—	—	—
VersaTiles (D-Flip-Flop)	384	768	1,536	3,072	6,144	9,216	13,824	24,576
RAM kbits (1,024 bits)	—	—	18	36	36	54	108	144
4,608-Bit Blocks	—	—	4	8	8	12	24	32
FlashROM Bits	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024
Secure (AES) ISP ¹	—	—	Yes	Yes	Yes	Yes	Yes	Yes
PLLs	—	—	1	1	1	1	1	1
VersaNet Globals ²	6	6	18	18	18	18	18	18
I/O Standards	Std. & Hot Swap	Std. & Hot Swap	Std.+	Std.+	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS
I/O Banks (+JTAG)	2	2	2	2	4	4	4	4
Maximum User I/Os	49	81	96	133	157	194	235	300
Speed Grades	Std.	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2
Temperature Grades	C, I	C, I	C, I, T	C, I, T	C, I, T	C, I	C, I	C, I, T, M

Table 1. ProASIC3 family overview

The Logic Cells of this family are called VersaTiles and can be used as:

1. All 3-input logic functions
2. Latch with clear or set
3. D-flip-flop with clear or set
4. Enable D-flip-flop with clear or set

The choice of ProASIC3 is not driven by the performance, nor the number of logic cells but by the behavior in radiation environment [21].

From the last chapter we know the most important effects of radiation on semiconductor devices. The FPGA device are sensible to the SEE and to the TID effect. The SEU sensitivity in FLASH based devices is less compared to SRAM ones[23]. Moreover mitigation scheme can be applied to reduce or totally remove SEU. In the Paragraph 3.3 some mitigation scheme are shown.

The ADC MAXIM 11046 has 8 independent input channels. Featuring independent track and hold (T/H) and SAR circuitry, these parts provide simultaneous sampling up to 250ksps for each channel. . The input range, the dynamic performance, and the parallel architecture of 8 channels make the ADC MAXIM 11046 suitable for the LVDT conditioner. The effects of the radiation on this device have been measured and the preliminary results are encouraging. The device has not shown SEL signature with a p+ beam at 230 MeV and will be tested also in a dedicated CERN

facility H4IRRAD to prove its SEL immunity in a mixed radiation field. The details of the radiation tests are given in the Chapter 4.

The remote communication of the proof demonstrator is via USB. It is used a USB to UART bridge from Silicon Laboratories named CP2102 for debugging and testing purpose only. The final board should have a Profibus module to communicate with a PLC.

The DAC that should be included in the final card is yet to be chosen and tested in radioactive environment. Four references are actually under test.

The development board for the FPGA is a M1A3PL with a M1A3P1000L FPGA which contains 1 billion of gates and 24576 VersaTile. The board has a USB connectivity plus three 40-pin GPIO banks for interfacing to other equipment. It has 4 MB of SRAM and 16 MB of flash memory provided on board. The board has been tested with two different ADC board. One proto-board for the MAX11046 is custom built the second one is the evaluation kit from the MAXIM. The setup usually used is depicted in Figure 4. The connection with the custom board is done using MicroCoax cable and an adapter board put on the top of the development board. The connection for the evaluation kit is more simple because it use only several jumper wires for control and data signals directly connected to the GPIO pin of the development board. A break-out board for the DAC and Profibus Module is still in fabrication.

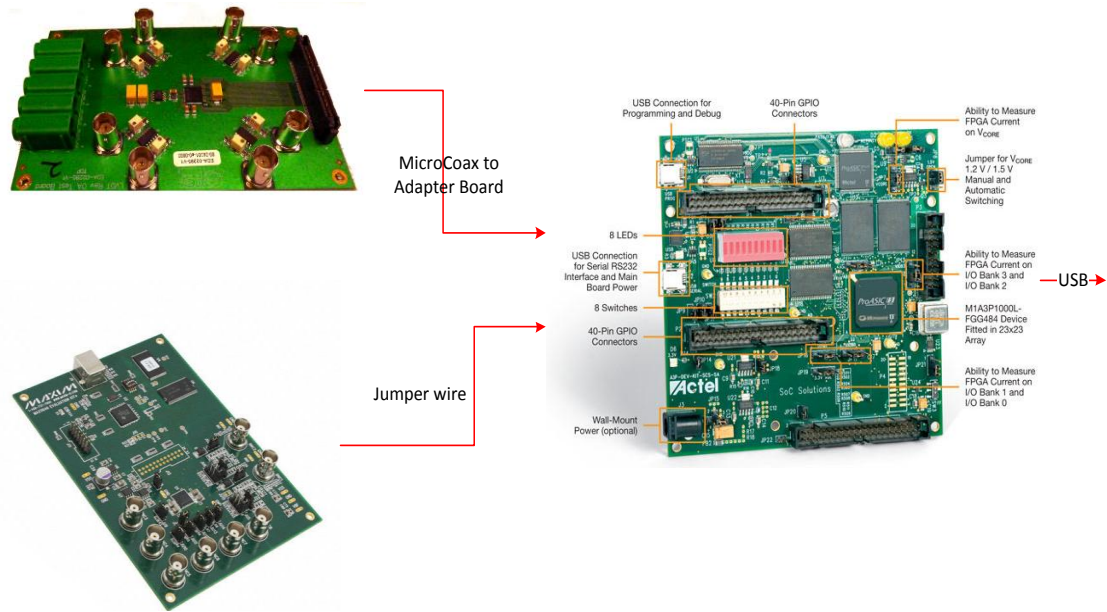


Figure 4. Development system used for testing. The two ADC boards are depicted on the left while on the right the FPGA development board is shown

3.2 The Algorithm analysis and design

3.2.1 Main choice for the algorithm design

Two choices can be made for the algorithm development on the FPGA. One choice is to use a soft or hard processor inside the FPGA and just implement via software the Sine Fit algorithm. This method, although simple, does not provide comparable performance with the current one. The main issue is due to low clock frequency and FPGA resources. Moreover some mitigation scheme cannot be implemented in soft/hard processor making difficult the process of verification. The second choice is to develop the whole hardware necessary for the Sine Fit inside the FPGA. One FPGA should calculate the position for several LVDTs but the total number depends from the area occupied by the design. This method is hard and time consuming but gives the best results even at low clock frequency.

The development of the algorithm starts from the analysis of the matrix operation up to the calculus of the ratiometric. The optimization of the algorithm done on PXI is not considered because it is an 'optimization' for CPU operations but it results in a complex design with no real benefits on FPGA. On the FPGA instead of creating a big matrix with all the samples of 7 or more LVDTs is better to process all the value from the LVDTs in parallel just cloning the hardware design for one LVDT. The other big difference from PXI system is the representation of the data. In the actual algorithm running on the CPU of the PXI all the operation are done in floating point, making the *word length effect* almost invisible. In the FPGA design is practically impossible to use Floating Point unit to compute the operation needed for the Sine Fit. The main problem is the area occupied by this unit and the time delay to retrieve the results. For these reasons the Fixed Point representation is used in the FPGA design. Naturally this choice brings some drawbacks. The positions retrieved from the FPGA differ from the PXI ones, bringing in a lack on the accuracy. So the first scope has been to test if the uncertainty obtained from the new fixed point algorithm satisfy the requirements. Moreover in choosing the fixed point representation more effort must be made to develop the whole system because each data operation is built individually. It is really important to understand and consider each operation on the data using a Fixed point arithmetic, because choosing in the proper way the number of bits to assign at each variable could considerably improve the calculus precision. Usually the fixed point representation in 2's complement is represented as $Q_{m,n}$ where m is the number of bits for the integer part while n is the number of bits for the fractional part. A $Q_{m,n}$ number can be written as:

$$-b_m 2^m + \sum_{i=-n}^{m-1} b_i 2^i$$

To obtain a good accuracy several optimizations and different solutions have been investigated. The different implementation tested are three. To speed up the test and development of the algorithm I used Matlab/Simulink to retrieve the results in

fixed point. Although Matlab has a built-in fixed point toolbox, this is not reliable on complex operation like square root or division. Actel and his partner Sinplify offer a Simulink toolbox, called Synphony Pro, that enables to evaluate an algorithm at a higher level of abstraction along with an exhaustive set of DSP blocksets. Actually this software permits to obtain a fully working hardware description but the performances in terms of area occupied on the FPGA and speed do not satisfy the requirements. The final version of the whole system is created from scratch using the hardware description language (HDL) Verilog and using also some Intellectual property from Actel.

The first two algorithms presented are called '*paper and pen*' because they are developed analyzing one by one the operation to be done. The third algorithm presented it is called *High resolution* because it shows better performance respect to the first two due to several optimizations and different implementations.

A step by step analysis of the algorithms follows. In all the analysis the sampling frequency of the ADC is 250Ksps and the input sine wave frequency is 2500Hz. The ADC has a 10 V range. The Sine Fit uses 2000 sample to calculate the amplitude value.

3.2.2 Paper and pen algorithm Low resolution and Medium resolution

The first two algorithm presented have the same structure shown in Figure 5 . Let's analyze each operation.

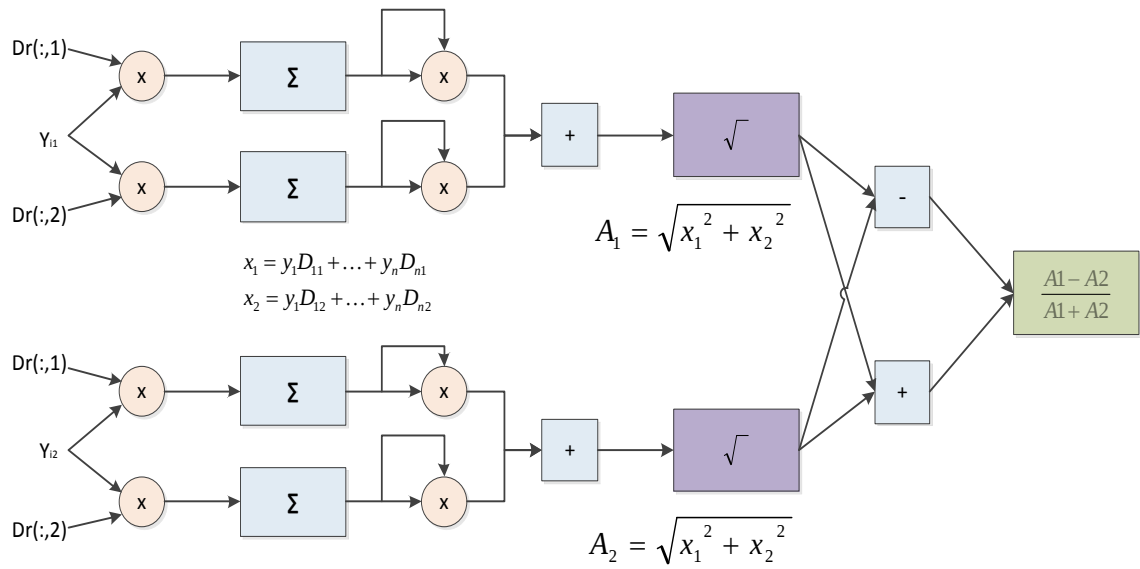


Figure 5. Schematic of "Paper and pen algorithm"

Starting from the matrix operation on one LVDT:

$$\tilde{\mathbf{x}}_0 = (\mathbf{D}_0^T \mathbf{D}_0)^{-1} \mathbf{D}_0^T \mathbf{y} = \mathbf{D}_0^\dagger \mathbf{y}$$

Where $\mathbf{y}$ is the vector with the input samples, $\mathbf{D}_0^\dagger$ is the pseudo-inverted matrix of the Sine Fit and $\mathbf{x}$ is the vector with the component in phase with the sine (A_s) and cosine (A_c). Rewriting it in the form:

$$\begin{bmatrix} D_{11} & D_{12} \\ \vdots & \vdots \\ D_{N1} & D_{N2} \end{bmatrix} [y_1 \quad \dots \quad y_N] = \begin{bmatrix} A_c \\ A_s \end{bmatrix}$$

The matrix multiplication above can be rewritten as sum of product:

$$A_c = \sum_{i=1}^N y_i * D_{i1}$$

$$A_s = \sum_{i=1}^N y_i * D_{i2}$$

Where D_{i1} and D_{i2} are the value of the pseudo-inverted matrix $\mathbf{D}_0^\dagger$ which could be called coefficient of the SineFit. So to compute the Sine Fit algorithm only multiplication and addition are needed. In hardware it means that only two multiply

and accumulate (MAC) unit are necessary to compute this matrix operation. After 2000 samples acquired the unit gives out the value of the component in phase with sine (and cosine). The hardware implementation of this unit is described in the Paragraph 3.2.3. For the moment what is really important to notice is that a multiplication of $n \times n$ bits brings to a results on $2n$ bits. This means that at least a $2n$ bits accumulator is needed to not lose any information, but the number of bits of the accumulator must be increased to not encounter an overflow.

To understand if we could obtain an overflow and how to prevent it is necessary to choose appropriately the representation. Usually the representation of the input y_i is in the Fixed point format $Q_{0,15}$. It means :

$$-1 < y_i < 1$$

The best quantization of the coefficient can be obtained making possible to represents the maximum value of the coefficient:

$$\max(D_{ik}) = 1e^{-3} \quad i = 1, \dots, N - 1 \text{ and } k = 1, 2$$

$$\log_2 \max(D_{ik}) \cong -9$$

The last equation shows that the representation on 16 bit to be used for the coefficient is $Q_{-9,24}$. The goodness of this quantization can be seen in the Figure 6 where it is possible to see that only 40 values over 2000 (2%) are out of the range of the quantization.

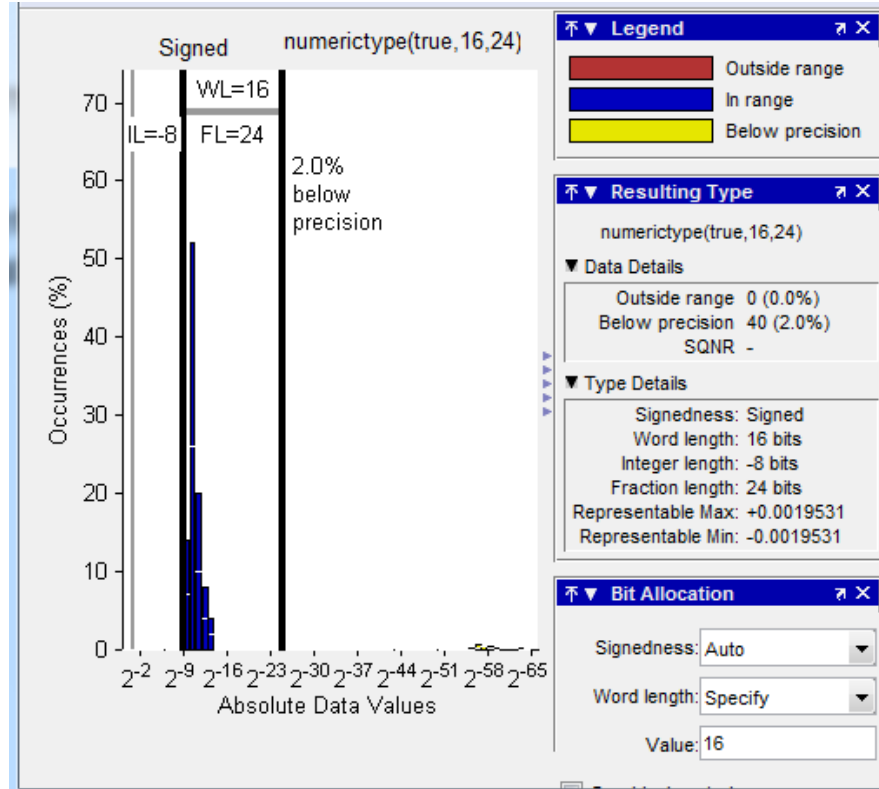


Figure 6. Quantization effect on the coefficient of the Sine Fit

Even choosing this representation the possibility of an overflow is still present. Let's consider:

$$A_c = \sum_{i=1}^N y_i D_{i1}$$

And calculate the maximum:

$$\max|A_c| = \sum_{i=1}^N |y_i| |D_{i1}| = \sum_{i=1}^N |D_{i1}|$$

We can actually have overflow if the maximum value does not fit in the results representation out of the accumulator. In our case the sum of the coefficient is

$$\sum_{i=1}^N |D_{ik}| = 1.2728 \quad k = 1, 2$$

$$\log_2 1.2728 = 0.3480 \cong 1$$

The result representation out of the multiplier is given by:

$$Q_{0,15} * Q_{-9,24} = Q_{-8,39}$$

The maximum value in this representation is about 0,0039, hence it is not possible to represent the maximum output value and an overflow could occur. Several technique can be used to prevent an overflow but most of them include a loss of accuracy. The best technique that can be used in an FPGA is increase the number of bits of the accumulator. The bits added to the accumulator are called *guard bits*. In our case 10 guard bits are needed because we want to represent the maximum value. This led to final output representation of $Q_{1,39}$. To accumulate with this representation a 41 bit accumulator is needed as depicted in Figure 7.

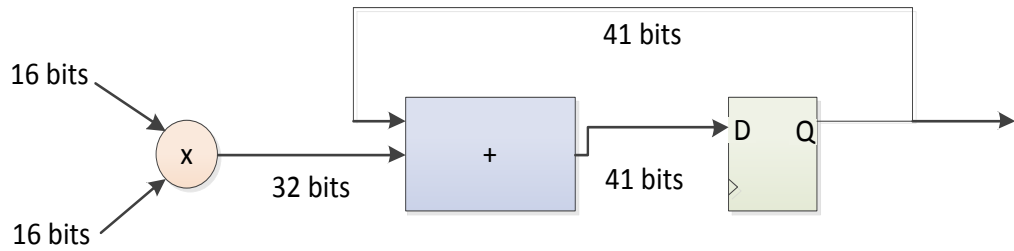


Figure 7. Multiply and accumulate cell with 41 bit accumulator.

The quantization of the coefficient brings a difference in the frequency response of the algorithm. The differences between a floating point computation of the amplitude and a fixed point one is depicted in Figure 8. It is possible to see that the error committed on the amplitude estimation is only 10 μ V.

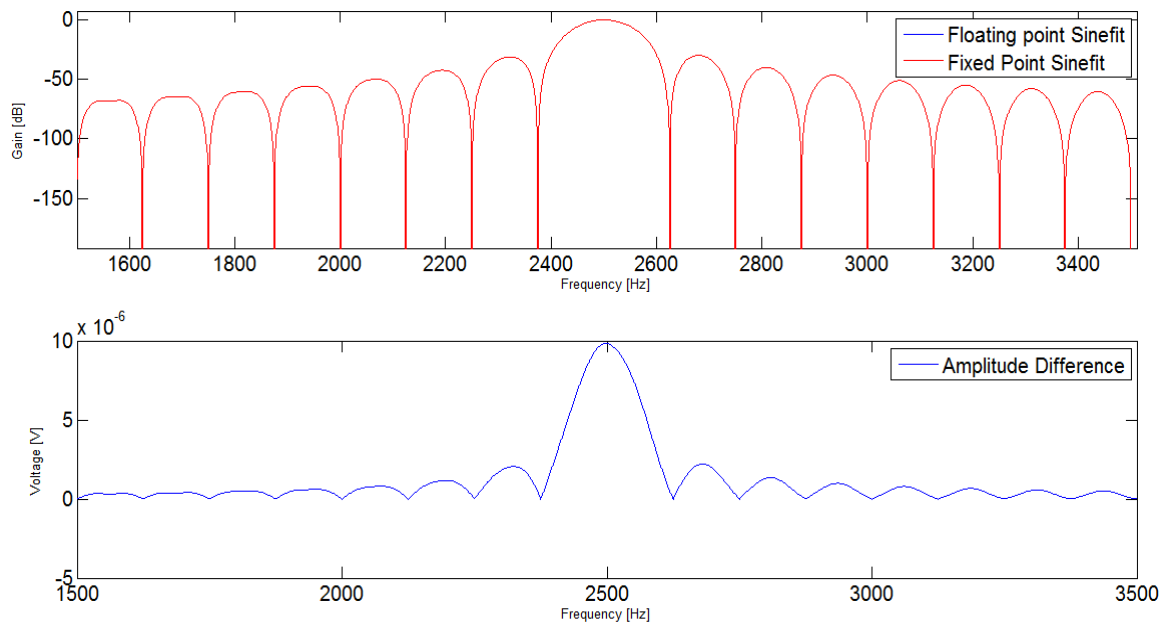


Figure 8. Differences between quantized and not quantized frequency response of the Sine Fit.

The formula to retrieve the Amplitude after the matrix operation is:

$$A = \sqrt{A_C^2 + A_S^2}$$

This is the most challenging operation because even if it looks simple it includes multiple operations. First of all, a square of the results from the matrix operation then the sum and the square root. The square of the value double the number of bits of the input value, so this brings to a 82 bits. It is very hard to deal with this very wide data bits. A multiplier of 41x41 bits would consume a lot of area and would slow down the entire algorithm. Moreover the square root should work on 83 bits like shown in the Figure 9.

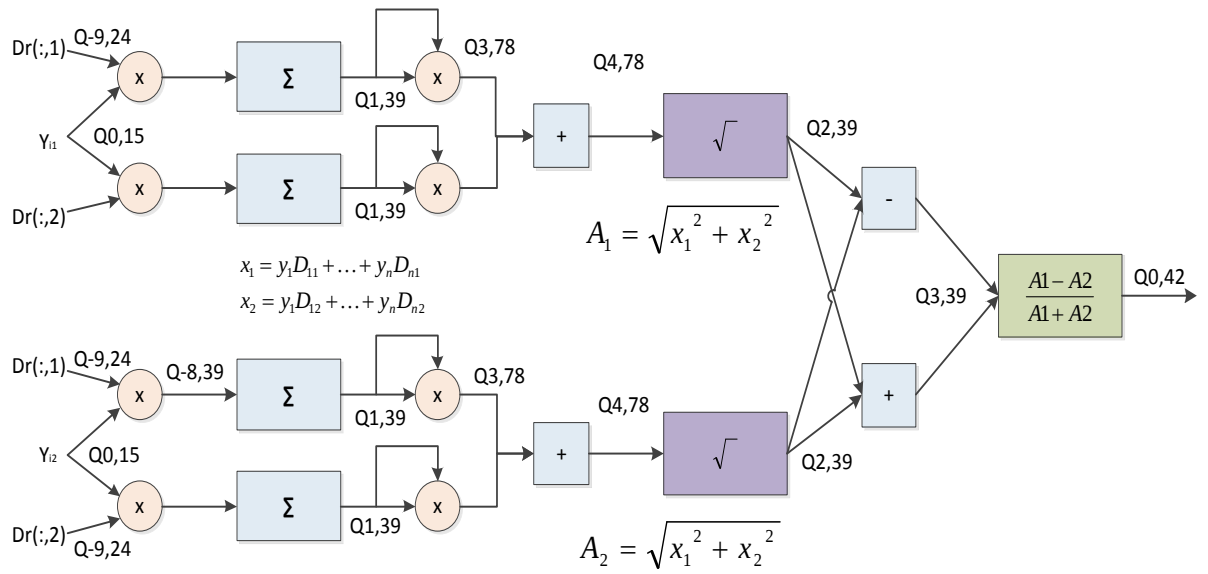


Figure 9. Full Sine Fit algorithm with the fixed point representation for each step.

The solution found for this problem is a variation of representation that reduces the number of bits. This also means a loss in the precision. The main difference of the two algorithm is the variation of representation at the output of the Multiply and Accumulate that brings to different resolutions Figure 10.

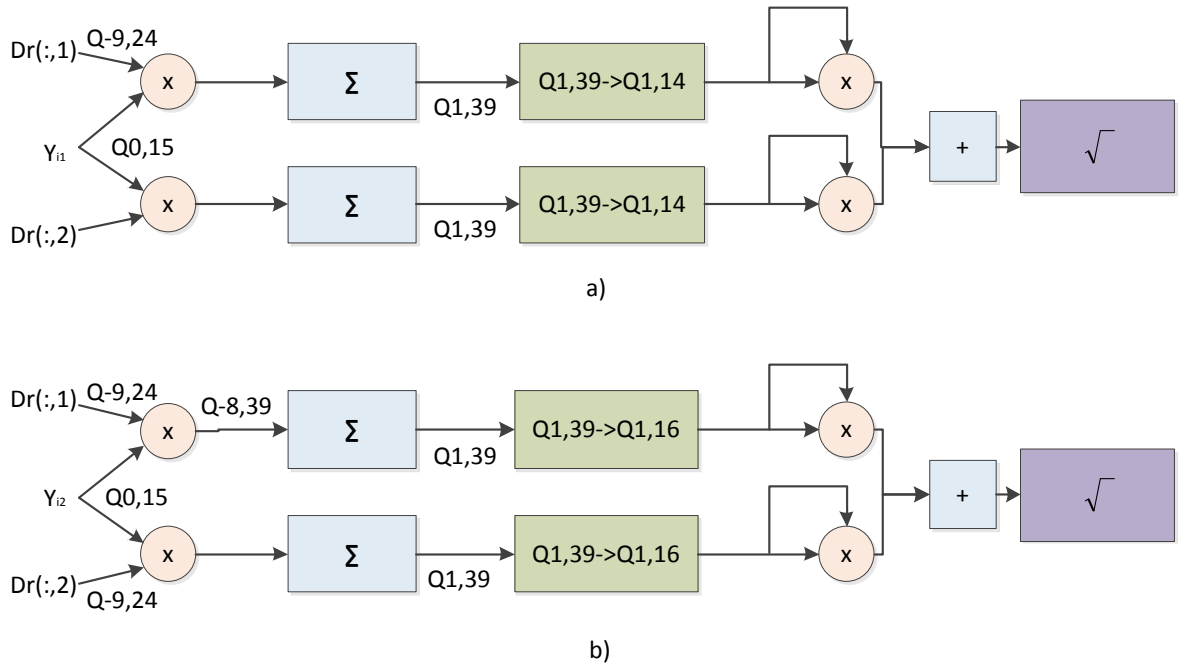


Figure 10. Variation of the representation at the output of the MAC cell for the
a) Low resolution b) Medium resolution

In one algorithm the 41 bits results is represented on 16 bits and on the other on 18 bits. For this reason the former is called *Low resolution* and the latter *Medium resolution*. In both the algorithm the variation is made with rounding so the error committed is:

$$\max |e_{Low\ res}| = 0,5 * 2^{-14}$$

$$\max |e_{Medium\ res}| = 0,5 * 2^{-16}$$

The results for this two type of implementation are shown in the next chapter.

The successive multiplication is an affordable 16x16 for the Low resolution scheme and 18x18 in the other. The results of the square operation are summed and then the square root is made. At this development and verification step how the square root is implemented is not mandatory. Moreover because it is used the toolbox Symphony in Simulink the implementation is hidden to the user. Some implementation method are discussed further. The toolbox used in Simulink suggests the best output representation for the square root. The output word

length is half of the input word length, and the number of output fraction bits is half of the number of input fraction bits.

In the division operation, since the results is always less than one the output could be represented with the maximum number of fractional bits.

In Figure 11 and Figure 12 the two algorithm implementation and their representations are shown. The results of this algorithms in terms of resolution on LVDT position is in the next Chapter 4.

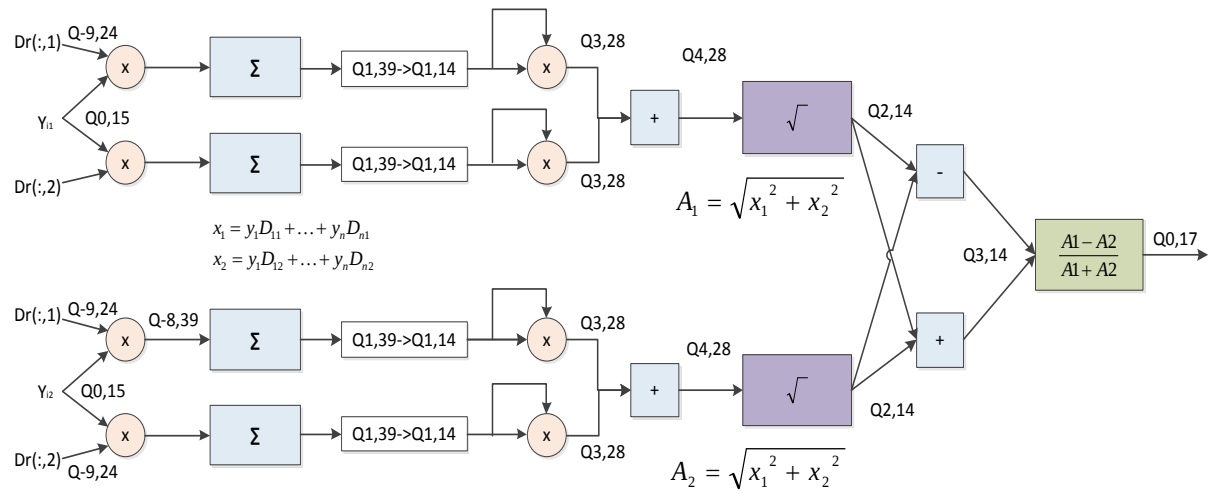


Figure 11. Full Low resolution algorithm with the representation for each step

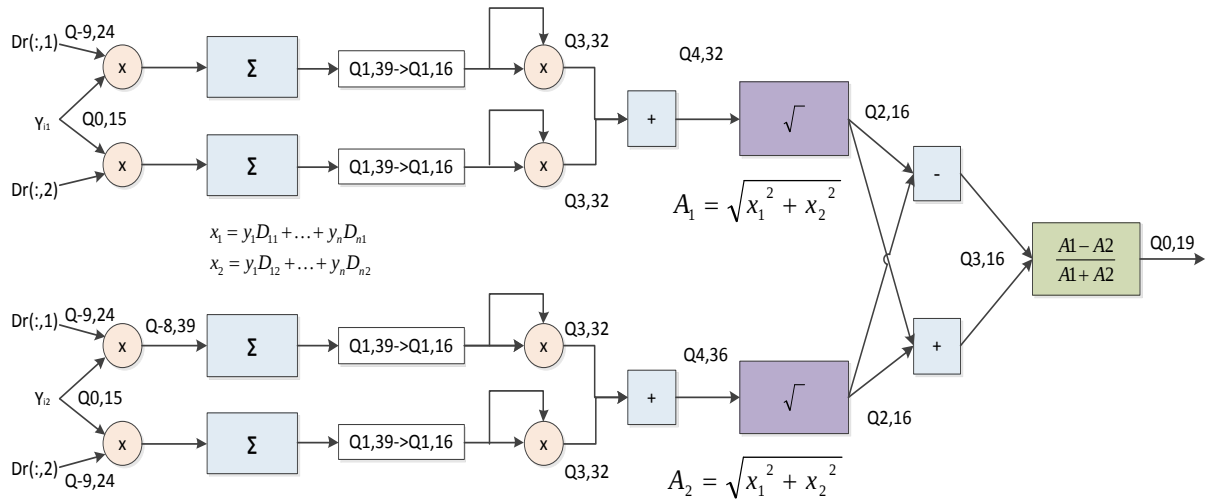


Figure 12. Full Medium resolution algorithm with the representation for each step

3.2.3 Novel Algorithm Implementation

Here is proposed a new implementation of the algorithm that reaches high performance in resolution and in area allocation. The development of the algorithm is directly done in hardware and the result compared to the Simulink simulation. The benefits of writing the code for the hardware synthesis is double: first of all there is the maximum freedom on the choice of the implementation that best fits the requirements (area, speed, resolution) moreover the system is already ready for an on-field test.

The new structure is depicted in Figure 13. It keeps the Multiply and Accumulate unit used before to compute the matrix multiplication. The difference now is that much care must be taken in consideration for the hardware implementation.

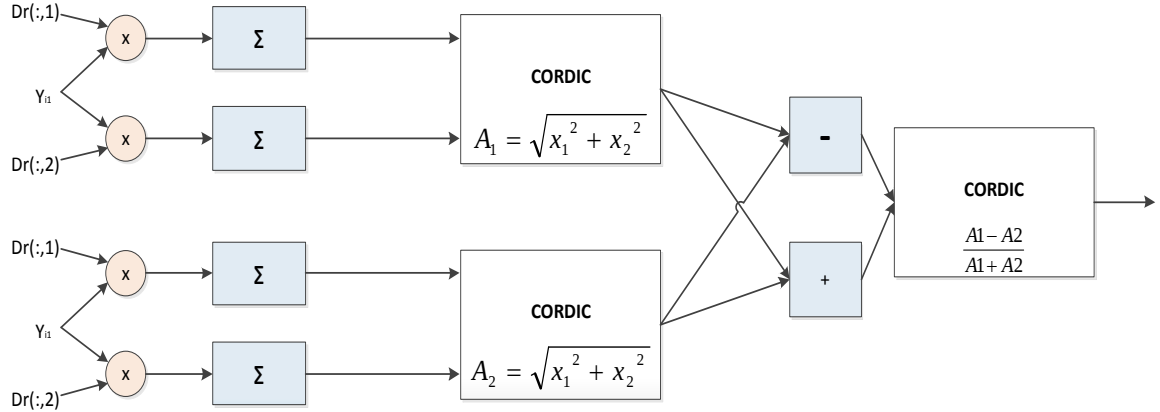


Figure 13. New algorithm architecture with CORDIC block for vector magnitude and for the division.

Usually the FPGA devices have several digital signal processing blocks that include a multiply unit and accumulation unit. The ProAsic3 family does not have any embedded multipliers nor accumulators, so the whole logic should be hardwired in the FPGA logic blocks. The multiplier used is an array multiplier [23]. The array multiplier is a very repetitive structure based on array of adders. With this implementation partial products are independently computed in parallel. Let's consider two binary numbers A and B, of m and n bits, respectively:

$$A = \sum_{i=0}^{m-1} A_i 2^i \quad B = \sum_{j=0}^{m-1} B_j 2^j$$

$$P = Ax B = \sum_{i=0}^{m-1} A_i 2^i \times \sum_{j=0}^{m-1} B_j 2^j = \sum_{i=0}^{m-1} \sum_{j=0}^{m-1} A_i x B_j 2^{i+j}$$

$$P = \sum_{k=0}^{nm-1} P_k 2^k$$

Where P_k is known as the partial product term. The hardware diagram of 4x4 unsigned multiplier scheme is shown in Figure 14. The main advantages of this structure is the scalability and the possibility to pipeline it. Moreover the array

multiplier is easy to implement. Actel offers the Intellectual Property of this type of multiplier free of charge and optimized for its FPGA.

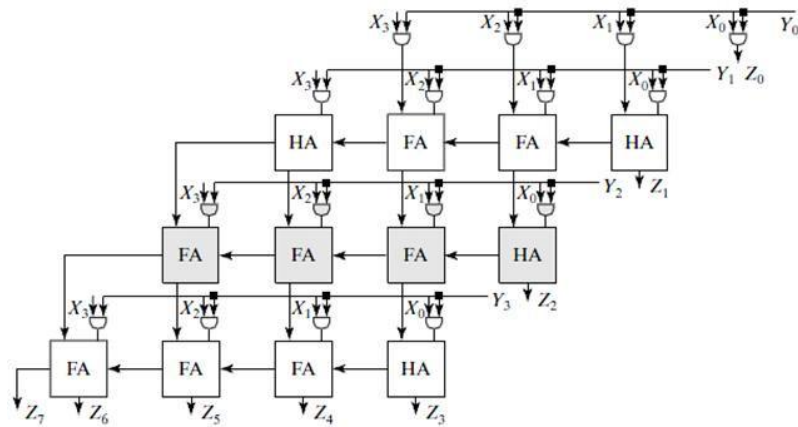


Figure 14. 4x4 Array Multiplier implemented in the ACTEL FPGA.

As shown in the Figure 14 a multiplication of $n \times n$ bits brings to a results on $2n$ bits. The accumulator used is a ripple carry adder. Several other implementations have been tested. The results are shown in Table 2. The ripple carry gives the best results.

MAC implementation	Area allocation	Clock Frequency
Ripple Accumulator	Core Cells : 1459 of 24576 (6%)	25.6 MHz 39.031 ns
Slansky Accumulator	Core Cells: 1727 of 24576 (7%)	31.2 MHz 32.035 ns
Fast Brent Kung	Core Cells : 1859 of 24576 (8%)	31.4 MHz 31.887 ns
Brent Kung	Core Cells: 1649 of 24576 (7%)	29.8 MHz 33.608 ns

Table 2. Area allocation results for MAC cell with different accumulator implementations.

In the previous implementation of the algorithm a change of variation at the output of the MAC unit is necessary and brings a big loss in resolution. In this implementation I avoided a change of variation and I managed to compute the square root on full precision.

It is important to remember the operation on the data after the MAC unit:

$$A = \sqrt{A_C^2 + A_S^2}$$

This complex operation is accomplished by only one algorithm: the COordinate Rotation Digital Computer algorithm (CORDIC) [24]. The CORDIC algorithm is usually used to pass from polar coordinates to Cartesian coordinates. For both modes the algorithm can be realized as an iterative sequence of additions/subtractions and shift operations, which are rotations by a fixed rotation angle (sometimes called micro-rotations) but with variable rotation direction. Due to the simplicity of the involved operations the CORDIC algorithm is very well suited for FPGA implementation.

The algorithm is derived from the general rotation transform:

$$\begin{aligned} x' &= x \cdot \cos\phi - y \cdot \sin\phi \\ y' &= y \cdot \cos\phi + x \cdot \sin\phi \end{aligned}$$

which rotates a vector in a Cartesian plane by the angle ϕ . These can be rearranged so that:

$$\begin{aligned} x' &= \cos\phi * [x - y \cdot \tan\phi] \\ y' &= \cos\phi * [y + x \cdot \tan\phi] \end{aligned}$$

if the rotation angles are restricted so that $\tan(\phi)=\pm 2^{-i}$, the multiplication by the tangent term is reduced to simple shift operation. Arbitrary angles of rotation are obtainable by performing a series of successively smaller elementary rotations. The iterative rotation can now be expressed as:

$$\begin{aligned} x_{i+i} &= K_i \cdot [x_i - y_i \cdot d_i \cdot 2^{-i}] \\ y_{i+i} &= K_i \cdot [y_i + x_i \cdot d_i \cdot 2^{-i}] \end{aligned}$$

Where :

$$K_i = \cos(\tan^{-1} 2^{-i}) = \frac{1}{\sqrt{1 + 2^{-2i}}}$$

$$d_i = \mp 1$$

The product of the K_i 's approaches 0.6073 as the number of iterations goes to infinity. Therefore, the rotation algorithm has a gain, A_n , of approximately 1.647.

$$A_n = \prod_n \sqrt{1 + 2^{-2i}}$$

The sequence on which direction to rotate can be represented by a decision vector. A third equation can be added to keep track of the rotation angle:

$$z_{i+1} = z_i - d_i \cdot \tan^{-1}(2^{-i})$$

The CORDIC algorithm could work in two different modes: rotation mode and vectoring mode. The rotation mode rotates the vector of a specified angle. The vectoring mode rotates the input vector on the x axis while recording the angle necessary to make that rotation.

The three equations are the same for the two modes:

$$\begin{aligned} x_{i+1} &= x_i - y_i \cdot d_i \cdot 2^{-i} \\ y_{i+1} &= y_i + x_i \cdot d_i \cdot 2^{-i} \\ z_{i+1} &= z_i - d_i \cdot \tan^{-1}(2^{-i}) \end{aligned}$$

In rotation mode, the angle accumulator is initialized with the desired rotation angle. The decision at each iteration is based on the sign of the residual angle after each step. The decision vector can be expressed by:

$$d_i = -1 \text{ if } z < 0, d_i = +1 \text{ if } z \geq 0$$

Which provide the following results:

$$x_n = A_n [x_0 \cos(z_0) - y_0 \sin(z_0)]$$

$$y_n = A_n [y_0 \cos(z_0) + x_0 \sin(z_0)]$$

$$z_n = 0$$

$$A_n = \prod_n \sqrt{1 + 2^{-2i}}$$

In the vectoring mode, the CORDIC rotates the input vector to align the result vector with the x axis. The result of the vectoring operation is a rotation angle and the scaled magnitude of the original vector. This is very interesting for the SineFit

algorithm because actually we could see the two vectors A_s and A_c as the coordinates of a vector in the polar plane. The vectoring function works by seeking to minimize the y component of the residual vector at each rotation. The sign of the residual y component is used to determine which direction to rotate next. An example of the vectoring rotations is in Figure 15. The equation seen for the rotation mode are the same for the vectoring mode, what is changed is the decision vector that can be expressed as:

$$d_i = -1 \text{ if } y < 0, d_i = +1 \text{ if } y \geq 0$$

Which led to the following results:

$$x_n = A_n \cdot \sqrt{x_0^2 + y_0^2}$$

$$y_n = 0$$

$$z_n = z_0 + \tan^{-1} \frac{y_0}{x_0}$$

It is important to notice that the CORDIC rotation and vectoring algorithms as stated could not converge. The limitation is due to the condition that each of the angles is more than half the previous one or, equivalently, each is less than the sum of all the angles that follow it. The condition can be expressed by:

$$|z_0 - z_n| \leq \sum_{i=0}^{n-1} \tan^{-1} 2^{-i}$$

Domain of convergence is $-99.7^\circ \leq z \leq 99.7^\circ$, where 99.7° is the sum of all the angles in the list; the domain contains $[-\pi/2, \pi/2]$ radians.

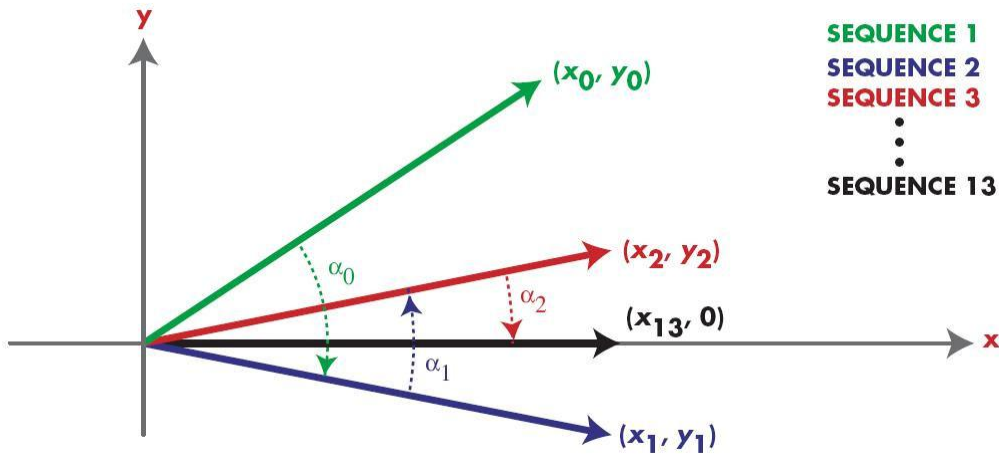


Figure 15. Vectoring Mode rotation in CORDIC algorithm

The question of the overflow could arise also in this operation. The main issue is due to the multiplicative factor and the choice to not change representation of the CORDIC input. The output of the CORDIC block $x_n = A_n \cdot \sqrt{A_C^2 + A_S^2}$ could bring to overflow if it does not fit the input representation ($Q_{1,39}$). If we try to calculate the maximum of the output considering only the representation of the operands we are actually overestimating the output range. If A_C and A_S coming from the MAC are in $Q_{1,39}$ their maximum value in this representation is about 2^1 , hence in the calculus of the maximum:

$$\max(x_n) = A_n \cdot \max\left(\sqrt{A_C^2 + A_S^2}\right)$$

By replacing the maximum value:

$$\max(x_n) = A_n \cdot 4 \cong 1,64 \cdot 4 = 6,56$$

This value does not fit in the output representation $Q_{1,39}$ and could led to overflow. This calculus, although correct, does not consider the real meaning of the vector magnitude operation. In our case the vector magnitude permits to retrieve the amplitude of the input sine wave. If we have considered the amplitude of the input sine wave in the range of ± 1 , it means that the maximum value of the vector magnitude could not overflow the unit value:

$$\max(x_n) = A_n \cdot \max\left(\sqrt{A_C^2 + A_S^2}\right) \cong 1.64 \cdot 1$$

The value 1.64 can be still represented in $Q_{1,39}$, hence no modification on the input representation of the CORDIC algorithm has to be made.

From the last set of equations is possible to notice that the CORDIC algorithm in vectoring mode can do all the operation necessary to retrieve the amplitude of one secondaries except of the A_n factor. Usually a CORDIC processor is followed by a scaling unit able to retrieve the correct result without multiplicative factor. In this High resolution algorithm, the scaling unit is useless because the two amplitude of the secondaries are scaled of the same A_n quantity (unless an equal number of CORDIC iteration are done), so the following ratio operation is completely unaffected by this factor.

The CORDIC algorithm, as described, can be used in multiple ways, some examples are Sine and Cosine calculation or the Arctangent of a specified input. But there is a generalization of this algorithm that can be used even for the division.

A modified version of CORDIC called *generalized CORDIC*, permits not only Circular rotation, but even linear rotation and hyperbolic rotation [25]. This generalization can be expressed in equations as follows:

$$\begin{aligned}x_{i+1} &= x_i - m \cdot y_i \cdot d_i \cdot 2^{-i} \\y_{i+1} &= y_i + x_i \cdot d_i \cdot 2^{-i} \\z_{i+1} &= z_i - d_i \cdot e_i\end{aligned}$$

Where where e_i is the elementary angle of rotation for iteration i in the selected coordinate system and m depends on the function. In the Table 3, the different values of $e(i)$ and m are given for each function.

m	Function	$e(i)$
1	Circular rotation	$\tan^{-1} 2^{-i}$
0	Linear rotation	2^{-i}
-1	Hyperbolic rotation	$\tanh^{-1} 2^{-i}$

Table 3. Different rotation for the generalized CORDIC algorithm.

In Figure 16 the three different rotation are shown where the value μ is indicated with m in Table 3.

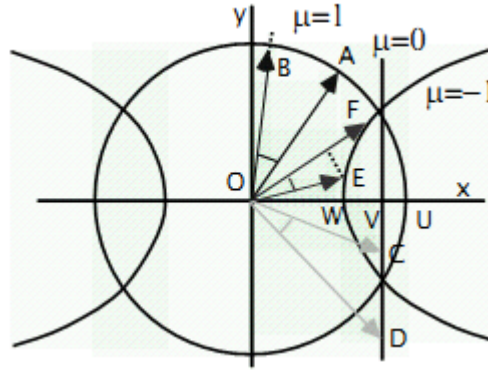


Figure 16. Circular, Linear and Hyperbolic rotation in two axis plane.

Let's focus the attention on the linear rotation. The equation for this type of rotation are:

$$x_{i+i} = x_i$$

$$y_{i+i} = y_i + x_i \cdot d_i \cdot 2^{-i}$$

$$z_{i+i} = z_i - d_i \cdot 2^{-i}$$

In rotation mode ($d_i = -1$ if $z_i < 0$, $d_i = +1$ otherwise) the linear rotation produces:

$$x_n = x_0$$

$$y_n = y_0 + x_0 \cdot y_0$$

$$z_n = 0$$

This operation is similar to the shift-add implementation of a multiplier, and as multipliers is not an optimal solution. The vectoring mode ($d_i = +1$ if $y_i < 0$, -1 otherwise) is more interesting for our scope, as it provides a method for evaluating ratios:

$$x_n = x_0$$

$$y_n = 0$$

$$z_n = z_0 - \frac{y_0}{x_0}$$

The rotations in the linear coordinate system have a unity gain, so no scaling corrections are required. If z_0 is chosen equal to zero the final results of the CORDIC in linear rotation is the ratio of the first data input y_0 and x_0 . In our case y_0 and x_0 are the sum and the difference of the evaluated amplitude of the secondaries coming from the previous CORDIC algorithm.

The accuracy of the CORDIC algorithm is the main issue in loss precision. Two major sources of the CORDIC computation are identified. The first is due to the quantized representation of the rotation angle by finite numbers of elementary angles. This error can be called approximation error. Each rotation angle is approximated by a linear combination of the n elementary angles, where n is the number of iterations. That is:

$$\sum_{i=0}^{n-1} d_i \cdot e(i) + \delta = \theta$$

Where δ is the error due to angle quantization. This error is bound by the smallest elementary angle :

$$\delta = e(n - 1)$$

The second type, called the rounding error is due to the finite precision arithmetic used in practical implementation. This error is due to the inner registers' finite word length and could be quantified by the use of the error propagation formula [26]:

$$f(n) = n\epsilon$$

$$\epsilon = 2^{-b-1}$$

Where $f(n)$ is the overall rounding error in n iterations and ϵ is the rounding error on a single word with b fractional bits.

Usually the best way to develop a CORDIC processor is to impose an upper limit on the error to commit and then calculate the number of bit of the inner registers and the number of iterations to perform. In our case because we are using a very long data word the best choice is to set only the number of iteration to the same

number of input bits. Hence the best choice is to use 39 iteration for the vector magnitude and 41 for the division:

$$n = b$$

A simulation on CORDIC for division is carried out to verify this statement. The CORDIC evaluates the ratio in fixed point and the maximum difference *Diff* between floating point ratio and the CORDIC result is used to calculate the effective number of bits:

$$b_{eff} = -\log_2(Diff) - 1$$

In Figure 17 the effective number of bits for the division results is shown against number of iteration. Considering an output with 41 bit of fractional part the maximum value of effective bits (39.41) is reached with 41 iterations.

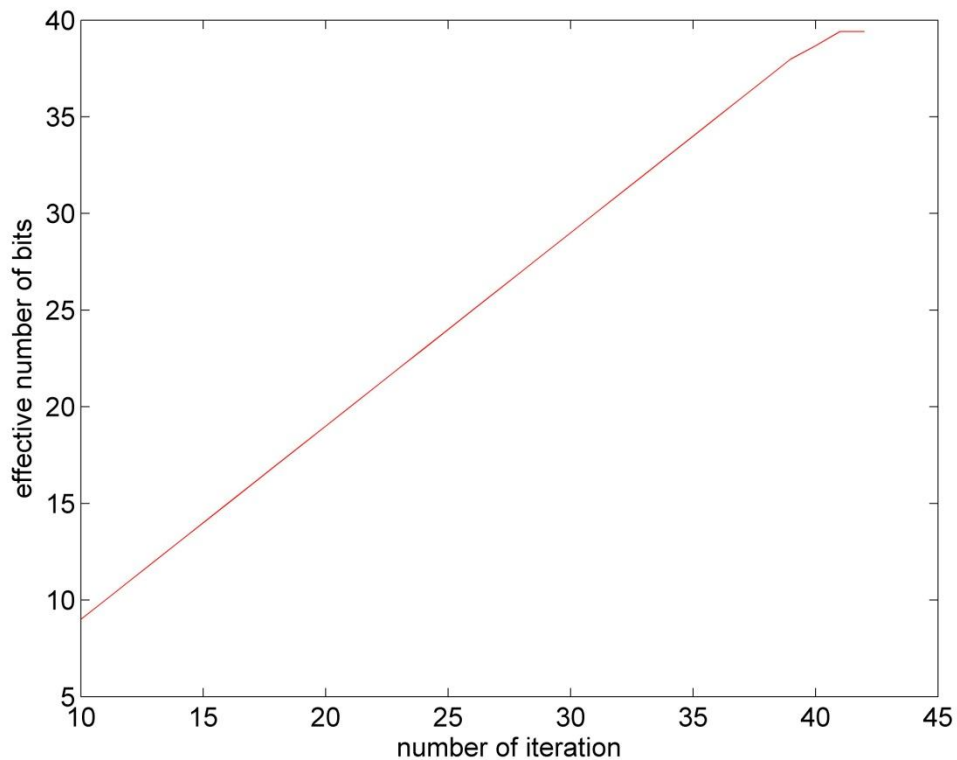


Figure 17. Effective number of bit for the division increasing the number of iteration of the CORDIC algorithm.

Three hardware implementations of this algorithm exist: Bit serial architecture , Word serial structure, and Fully parallel.

Whenever the CORDIC speed is not an issue, the Bit Serial architecture provides the smallest implementation. Figure 18 depicts the simplified block diagram of the bit-serial architecture. The shift registers get loaded with initial data presented in bit-parallel form; that is, all bits at once. The data then shifts to the right, before arriving to the serial adders/subtractors. Every iteration takes m clock cycles, where m is the CORDIC bit resolution. Serial shifters are implemented by properly tapping the bits of the shift registers. The control circuitry (not shown in Figure 18) provides sign-padding of the shifted serial data to realize its correct sign extension. The results from the serial adders return back to the shift registers, so that in m clock cycles the results of another iteration are stored in the shift registers.

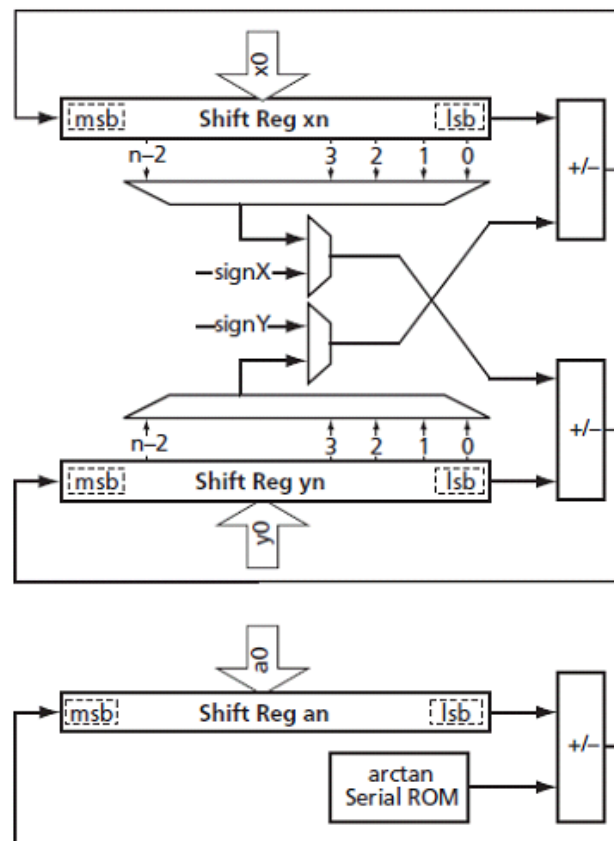


Figure 18. Bit-serial architecture of CORDIC processor

The word serial architecture (Figure 19) is based on the direct implementation of the CORDIC equations. The vector coordinates to be converted, or initial values, are loaded via multiplexers into registers RegX, RegY, and RegA. RegA, along with an

adjacent adder/subtractor, multiplexer, and a small arctan look-up table (LUT), is often called an angle accumulator. Then on each of the following clock cycles, the registered values are passed through adders/subtractors and shifters. They are loaded back to the same registers. Each iteration takes one clock cycle, so that in n clock cycles, n iterations are performed and the converted coordinates are stored in the registers.

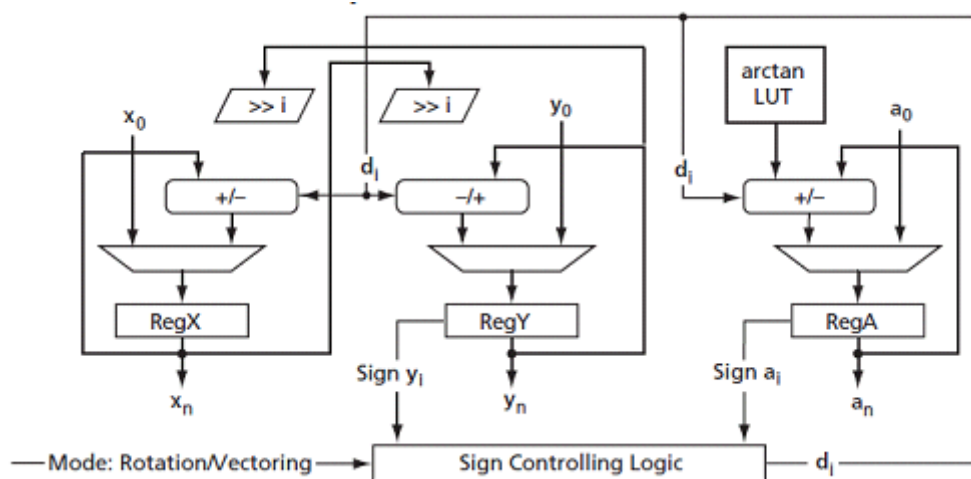


Figure 19. Word-serial architecture of CORDIC processor

Depending on the CORDIC mode (rotation or vectoring), the sign-controlling logic watches either the RegY or the RegA sign bit. It determines what type of operation (addition or subtraction) needs to be performed at every iteration. The arctan LUT keeps a pre-computed table of the $\arctan(2^{-i})$ values. The number of entries in the arctan LUT equals the desirable number of iterations, n .

The Parallel architecture presents an unrolled version of the sequential CORDIC algorithm. Instead of reusing the same hardware for all iteration stages, the parallel architecture has a separate hardware processor for every CORDIC iteration. An example of the parallel CORDIC architecture configured for rotation mode is shown in Figure 20

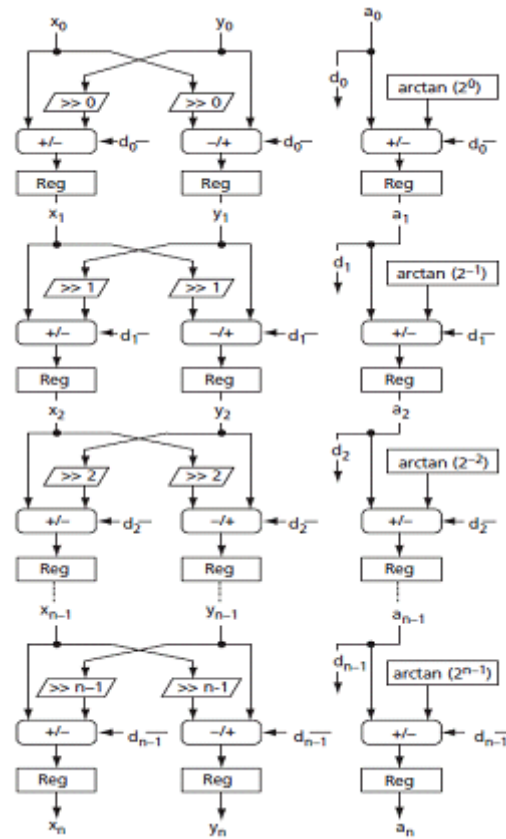


Figure 20. Fully parallel architecture of CORDIC processor

Each of the n processors performs a specific iteration, and a particular processor always performs the same iteration. This leads to a simplification of the hardware. All the shifters perform the fixed shift, which means these can be implemented in the FPGA wiring. Every processor utilizes a particular arctan value that can also be hardwired to the input of every angle accumulator. Yet another simplification is an absence of a state machine. The parallel architecture is obviously faster than the sequential architecture described in the Word-Serial architecture, but is also bigger in terms of area consumed. It accepts new input data and puts out the results at every clock cycle. The architecture introduces a latency of n clock cycles.

The results on the area occupancy and the speed achieved by the different implementations are shown in the

Table 4. The word length serial implementation has been chosen because of its speed and area occupancy.

Cordic Implementation	Area allocation	Clock Frequency
Bit Length serial with FF	Core Cells: 2163 of 24576 (9%)	82.8 MHz-12.080 ns
Word Length serial with FF	Core Cells: 4843 of 24576 (20%)	48.4 MHz-20.664 ns
Word Length serial without FF	Core Cells: 3133 of 24576 (13%)	47.6 MHz-20.994 ns
Parallel with 20 bit data input	Core Cells: 6220 of 24576 (25%)	36.1 MHz-27.673 ns

Table 4. Area allocated for the different implementations of the CORDIC.

This brief introduction on the CORDIC algorithm and its hardware implementation is useful to understand the choice made. The use of the CORDIC algorithm permits to obtain the vector magnitude without any compromise in terms of resolution because no word length variation is done at the output of the MAC unit. Even the ratio works on the full word length without any compromises. So each CORDIC in the system depicted in Figure 21 works on the full word length (41 bit for the vector magnitude and 42 bits for the division). In Figure 21 it is possible to notice two blocks that indicates the absolute value operation. These blocks are necessary for the first CORDIC because, as said before, the CORDIC doesn't converge if the input vector is not in the first or forth quadrant. The output on 42 bits is then contracted on 32 bits because the result might be treated by a PLC (Programmable Logic Controller) which has a 32 bit representation. The variation on data length is done with rounding so an error is introduced in this stage. The error committed is:

$$\max|e_{42-32}| = 0,5 \cdot 2^{-32}$$

This error can be accepts since it affects only the final data which is the ratiometric value or the position itself.

A state machine called FSM in the Figure 21, is necessary to give the right output value to the CORDIC algorithm after 2000 samples processed.

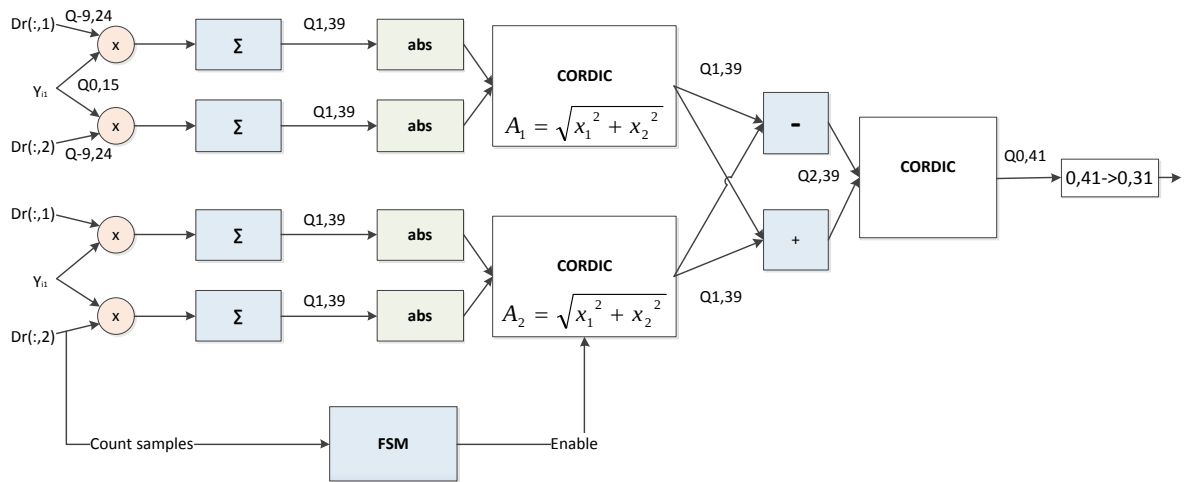


Figure 21. Final architecture of the High resolution algorithm for the LVDT reading

3.2.4 The Full System Architecture

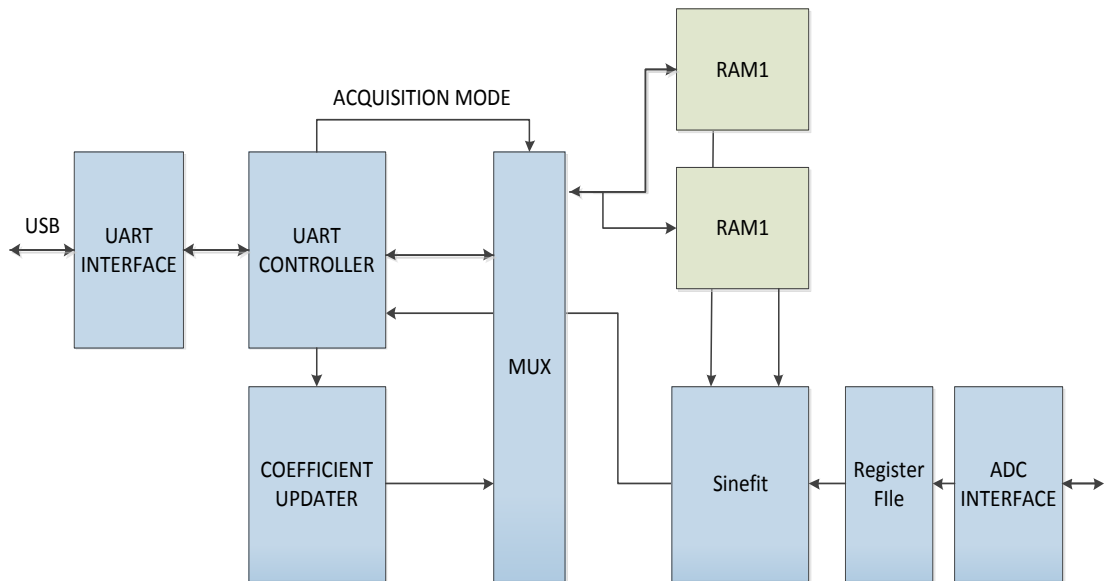


Figure 22. Embedded system developed to test the algorithm.

I developed a full embedded system (Figure 22) around the Sine Fit algorithm to be able to test and verify it. The whole system is mainly based on finite state machine (FSM). The choice of the FSM against a soft-processor is driven by the compactness and the reliability. The first module is an interface controller for the ADC. The main

feature of the controller is to generate the correct signals to configure the ADC and acquire the samples from it. An example of timing diagram for the ADC is depicted in Figure 23. The 'wait state' can be configured to change the sampling rate. The maximum sampling rate is 250 ksp/s which correspond to a wait-state of 500ns. The samples from the interface are stored in a 'register file' which permits to de-serialize the samples of each channel, making them accessible in parallel.

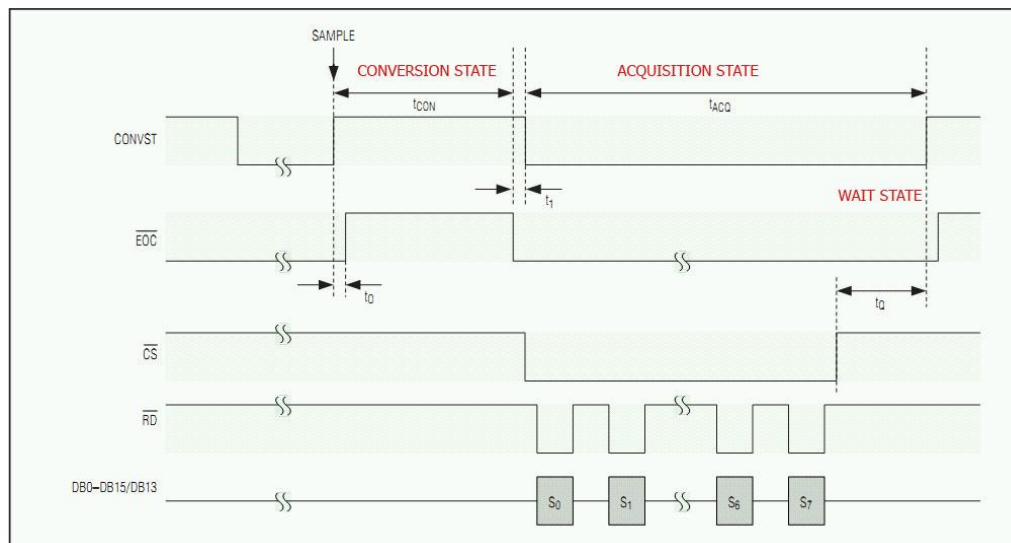


Figure 23. Timing diagram of the ADC MAX 11046.

The most important controller in the entire embedded system is the UART controller. This module is directly attached to the UART interface that receives and sends command and data on the USB.

I developed a simple communication protocol to send and retrieve information. The host PC always sends 2 byte over virtual COM port. The first byte is the command, while the second is the data. The FSM of the UART controller always waits for the data on the bus if the input FiFo is not empty it start to decode the command received. A list of the state , the commands and their functionality is in Table 5.

COMMAND	Data	Function
START=0x01		Start the acquisition
STOP = 0x02		Stop the acquisition
TRANSMIT1=0x03 ,		Transmit to the host the RAM1 coefficient
TRANSMIT2=0x04		Transmit to the host the RAM2 coefficient
CONFIGUART = 0x05 ,	Uart Baud Rate	Change the UART Baud Rate
CONFIGADC = 0x06 ,	Wait state counter	Change the ADC sampling Time
FILLMEMORY1 = 0x07 ,		Fill the RAM1 with the coefficient
FILLMEMORY2 = 0x08;		Fill the RAM2 with the coefficient

Table 5. Command and functionality table for the main state machine.

Actually only for testing purpose the coefficients of the SineFit are stored in the FPGA's RAM blocks but in future a module to load it from an external ROM/FLASH has to be developed. The coefficient updater module manage the ram memory as a circular buffer, retrieving the right coefficient each time a new samples is available and when it arrives at the end of the memory start from the first element.

The command and the data are sent from the Host via a Labview software which also read the position sent on the USB by the module.

3.3 Radiation effects mitigation scheme in FPGA device

The effects of radiations on the ACTEL FPGA are to consider. The FPGA is considered Latch-up free for the CERN environment since the LET threshold for SEL is 68 MeV·cm²/mg. Most likely, a further test will be carried out in a CERN dedicated facility where the DUT is exposed to a mixed radiation field, very similar to the one of the LHC tunnel.

The most important effects on Flash Based FPGA are SEE. Two different approaches can be used to harden the design against radiations: in the first, the designer take

care of implementing several techniques at high level description language (configured design on the FPGA). The second one is to choose an FPGA in which the vendor applied hardening technique at the FPGA matrix logic gates and flip-flops. Because our choice is a commercial FPGA device, in particular the ProAsic3 device, the designer must take care of the hardening technique. In this thesis only the SEU effects are taken in consideration.

Most common type of mitigation in FPGA involves triplication of circuitry and majority voter insertion. In the ProAsic3 family no configuration or clock lines triplication is needed for this reason the scheme is called: Localized Triple Mode Redundancy (LTMR). For the embedded SRAM the error detection and correction core (EDAC) can be used to detect and correct soft errors.

Actel recommends three techniques for implementing the logic of the sequential elements in radiation-tolerant FPGAs: C-C, TMR, and TMR_CC (Figure and Figure [27])

The C-C technique uses combinatorial cells with feedback (instead of flip-flop or latch primitives) to implement storage. TMR is an acronym for triple-module-redundancy (or triple voting). It is a register implementation technique; each register is implemented by three flip-flops (or latches) that “vote” to determine the state of the register. TMR_CC is also a triple-module-redundancy technique. Each voting register is composed of combinatorial cells with feedback (instead of flip-flop or latch primitives). Triple voting, or triple module redundancy (TMR), produces designs that are most resistant to SEU effects. Instead of a single flip-flop, triple voting uses three flip-flops leading to a majority gate voting circuit. This way, if one flip-flop is flipped to the wrong state, the other two override it and the correct value is propagated to the rest of the circuit. The results of TMR technique on the full design is in the Chapter 4.

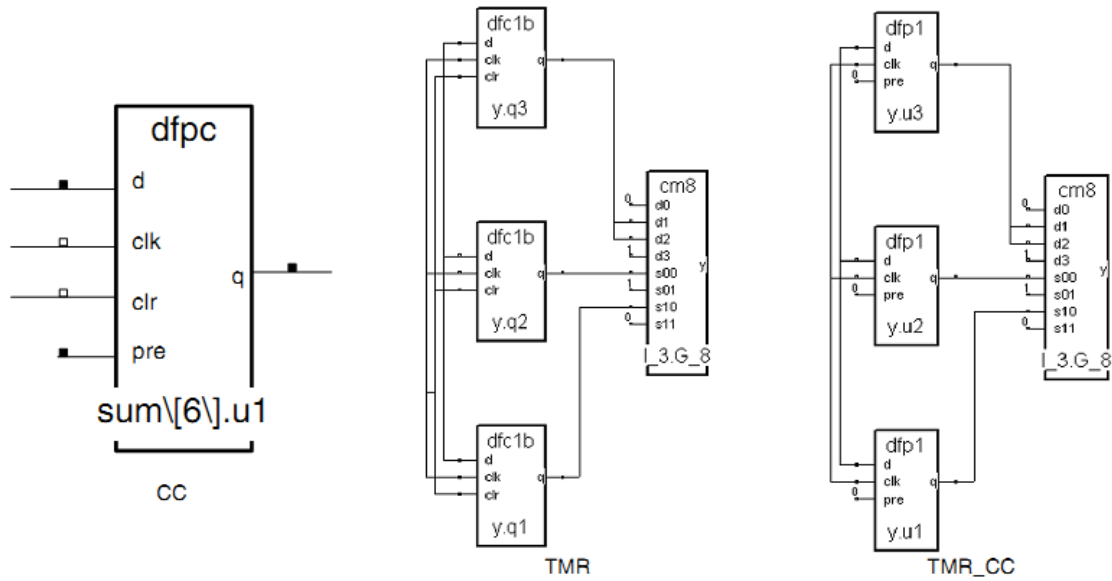


Figure 24. Different voting scheme: a)CC implementation b) TMR c) TMR implemented with combinatorial circuit.

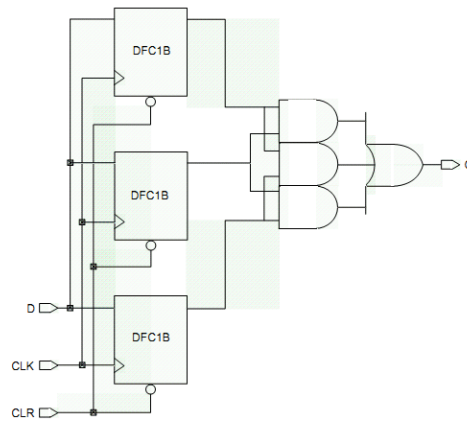


Figure 25. Zoom on TMR cell and implementation of voting scheme.

The RAM block of the FPGA are very sensitive to the SEE [21] , hence is often used an Error Detecting and Correction unit (EDAC) which try to detect and correct the data stored in the memory[28].

The EDAC core is not implemented in the final design but analyzed for further development. The integrity requirement of the data contained within the embedded SRAM is determined by the particular application and may range from noncritical to very critical. The EDAC core must be configured and the remainder of the design must react to the notification of SEU events by the EDAC core.

Errors in RAM blocks can be detected and corrected by employing Error Correction Codes (ECCs). ECCs incorporate redundancy adding extra bits to a data word and the result is called a *codeword*. With this redundancy, only a subset of all possible codewords contains valid messages. Valid codewords are separated from each other so errors are not likely to corrupt one valid codeword into another. At this point the encoded data can be stored. However, the capacity of the storage device must accommodate the data and the incorporated redundancy. When recovering data, a decoder first determines if a message read from the RAM is valid. This step is called error detection. If an error is detected, the decoder finds a valid message that is most similar to the one read and corrects the error. Theoretically, it is possible to detect and correct an arbitrary number of errors. Practically, though, a larger number of errors requires a larger redundant bit number and more complex encoder and decoder circuitry, and results in longer encoder/decoder latency. Latency is a crucial characteristic when it comes to the RAM EDAC circuitry. RAM EDAC circuitry cannot use ECCs such as Reed-Solomon, more efficient in terms of redundancy, because they introduce extreme latency. The error correction in RAM traditionally implements the Single Error Correction–Double Error Detection (SEC-DED) technique based on Hamming code. This technique provides the best characteristics in terms of redundancy bits, the die area used, and the shortest encoder/decoder latency. As memory density increases, a single ion impact can cause multiple-bit upsets in nearby cells. Though SEC-DED cannot correct multiple errors, it is quite safe to use it on Actel FPGAs, as these are well protected against multiple-bit upsets by design. Actel SRAM blocks are designed so that two bits of the same RAM word are never stored in nearby cells, whether in horizontal or vertical direction. Therefore, the probability of multiple-bit upset in SRAM blocks is negligible, and the SEC-DED technique proves to be highly efficient. CoreEDAC is based on a special shortened Hamming code proposed by Hsiao. This code provides better latency and area characteristics than other Hamming codes. An example of a RAM protected with EDAC is shown in Figure 26 During user write, user data comes

to the EDAC encoder , which calculates the parity bits and appends these to the user data, forming a codeword.

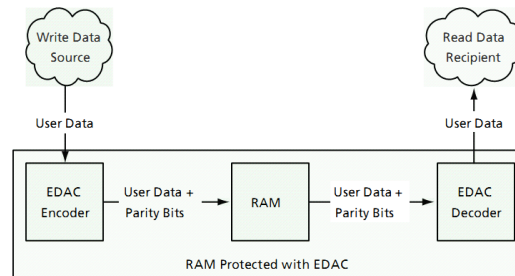


Figure 26. EDAC circuit schematic block.

The codeword is stored in the RAM. During user read, the read codeword first comes to the decoder, which detects and corrects errors (if any), discards parity bits, and outputs the corrected user data word.

Chapter 4

Experimental results

In this chapter all the experimental results and simulation carried out to characterize the entire system are shown and described. First a comparison of the 3 Sine Fit algorithms, presented in Chapter 3, is given, showing the difference in terms of performance and area allocation. Then, the radiation tests on the ADC MAXIM 11046 are presented.

4.1 Implementation Results and comparison

In this paragraph the results of the hardware implementation of the three algorithms presented in chapter 3 are shown. The Low and Medium resolution algorithms are developed using the toolbox Symphony in Simulink. The direct synthesis of these algorithms are really simple but the results in terms of area is not satisfactory at all. The results of the synthesis in terms of cell occupied is shown in

Table 1. The inner design and implementation choice are completely chosen by the toolbox and the designer has no option. The target device is a ProAsic3L A3P1000L device with 1 billion gates and 24576 VersaTile. This device is on the development board used as proof demonstrator.

Implementation	Area Occupied	Clock Frequency
Low resolution	Core Cells:35197 of 24576 (143%)	2.3 MHz - 434.570 ns
Medium resolution	Core Cells: 41780 of 24576 (170%)	1.7 MHz -588.235 ns
High resolution	Core Cells: 11881 of 24576 (48%)	25.6 MHz-39.031 ns

High resolution A3PE3000	Core Cells: 11465 of 75264 (15%)	23.9 MHz- 41.796
High resolution with TMR	Core Cells: 14572 of 24576 (59%)	24.7 MHz-40.427 ns

Table 1. Area allocation of the three algorithms developed.

The High resolution algorithm can easily fit in the FPGA of the development board. The A3P1000L FPGA is not the biggest ProAsic3 available. To verify that more than one SineFit algorithm (hence more than one LVDT) could fit in a bigger FPGA, I synthesized the High resolution implementation in a A3PE3000 FPGA with 3 billion gates and 75264 VersaTile. The results are very promising; in fact, more than one LVDT could be processed by a new developed board with the biggest FPGA of the ProAsic3 family.

In

Table 1, the area occupied after the implementation of the voting scheme to mitigate the radiation effect is also shown. As mitigation scheme is chosen the TMR and its implementation is completely demanded to the synthesis tool (Synplify Pro). Verification of the synthesis is mandatory to verify the correct application of the global voting system. The voting system is implemented with a Macro cell called MAJ3 and it cost only 1 VersaTile (Figure 1).

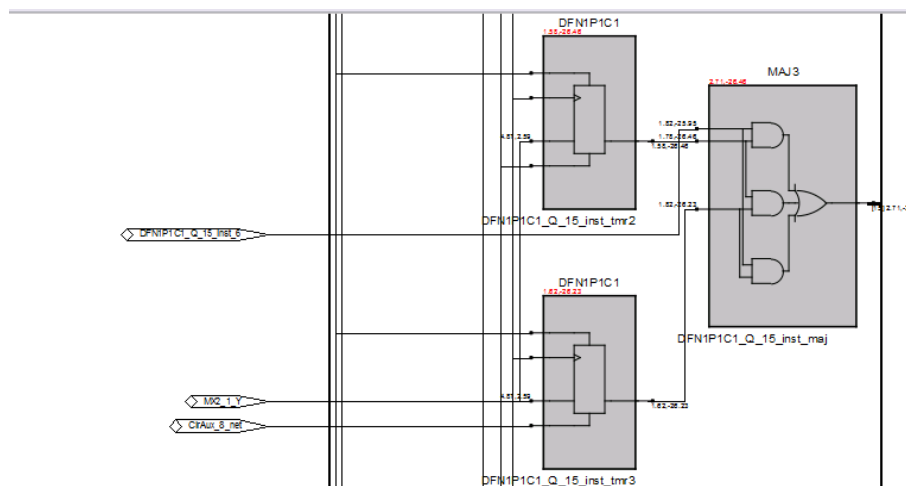


Figure 1. Implementation of TMR with a MAJ3 cell in the ProAsic3 FPGA.

The full embedded system proposed in Chapter 3 has been synthesized with the high resolution algorithm as signal processing unit and the results are shown in table.

Implementation	Area	Maximum frequency
Full Embedded System	Core Cells: 13059 of 24576 (53%)	25.6 MHz-39.0 ns
Full Embedded System with TMR	Core Cells: 17107 of 24576 (70%)	24.7 MHz-40.4 ns

Table 2. Area allocation of the full embedded system without the TMR and with redundancy applied.

The results obtained in terms of area occupied are satisfying because not only the full system fits in the FPGA on the development board, but even the system with the triplication scheme.

4.2 Speed performance

4.2.1 Maximum frequency achievable

According to the obtained results it is possible to run the system at a maximum clock frequency of about 20 MHz. The ADC sampling rate is 250 KHz, hence the acquisition of 2000 samples lasts 8ms. In order to achieve an output frequency of 100 Hz, the computation of the position should last no longer than 2ms. In the High resolution implementation after the last sample acquired, the position is evaluated in 4.4 μ s. This means that the whole algorithm lasts 92 clock cycles at 20 MHz. By so doing, the delay to retrieve the position with the FPGA implementation is fixed and there is no jitter. Moreover, increasing the number of LVDTs to be read will not lead to an increasing in the timing performance because each algorithms can work in parallel. Hence the

conclusion is that the position survey could go a bit faster than 100 Hz. Considering other time issue, the output frequency of 124 Hz (about 8.005 ms) can be achieved.

4.2.2 Speed VS resolution analysis

A research has been carried out to verify if it is possible to speed up the survey, by reducing the number of samples of the quantized sine wave on which the Sine Fit algorithm is applied. To reduce the acquisition length in the Sine Fit algorithm means averaging on less number of samples, hence a reduction in his capability to reject noise. Several simulations have been carried out with Matlab to retrieve the standard deviation of the evaluated position P , as a function of the number of samples of the input sine waves of the LVDT secondary coils. A simulation plans has been run by considering the input sine waves (emulation of the LVDT secondary coils) at different SNR. The position P is evaluated by considering different numbers of samples of the input sine wave (100 to 2000). The standard deviation as a function of the Number of samples and of the Signal to Noise Ratio (SNR) of the input sine wave, is depicted in Figure 2. It is possible to notice how good are the performance of the Sine Fit with 2000 samples even at lowest value of SNR.

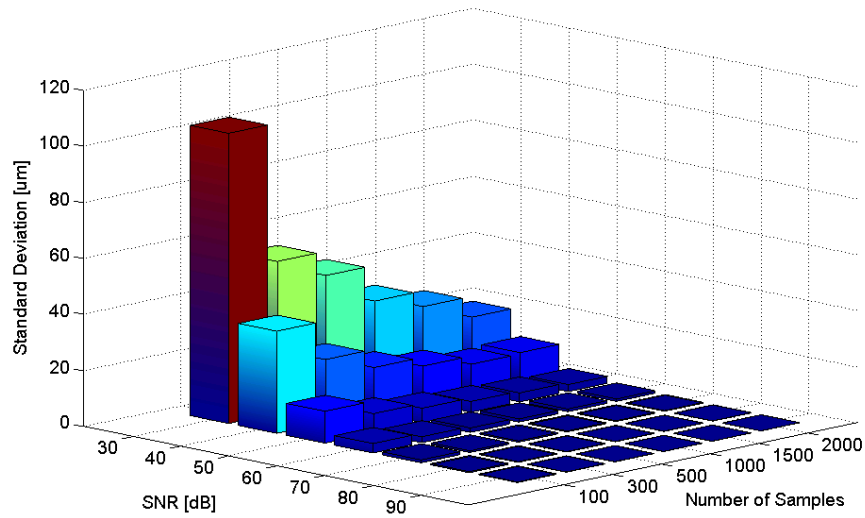


Figure 2. Standard deviation plotted against the number of samples acquired and a variable value of SNR.

Since the actual measurement of the LVDT indicates a maximum value of SNR of about 60 dB with 800 meter long cable, another simulation has been carried out to see how the standard deviation varies on different position at a fixed SNR. The simulation results for the full range ± 40 mm are in Figure 3. It is possible to notice that the same standard deviation for 1500 and 2000 samples, but at 1000 samples the uncertainty starts to increase to 1 μm . A target of 0.5 μm is used in this study. That target comes from the analysis of the LVDT data of the collimation system when it is in steady-state. The study shows that a higher output frequency can be reached if a lower uncertainty can be accepted.

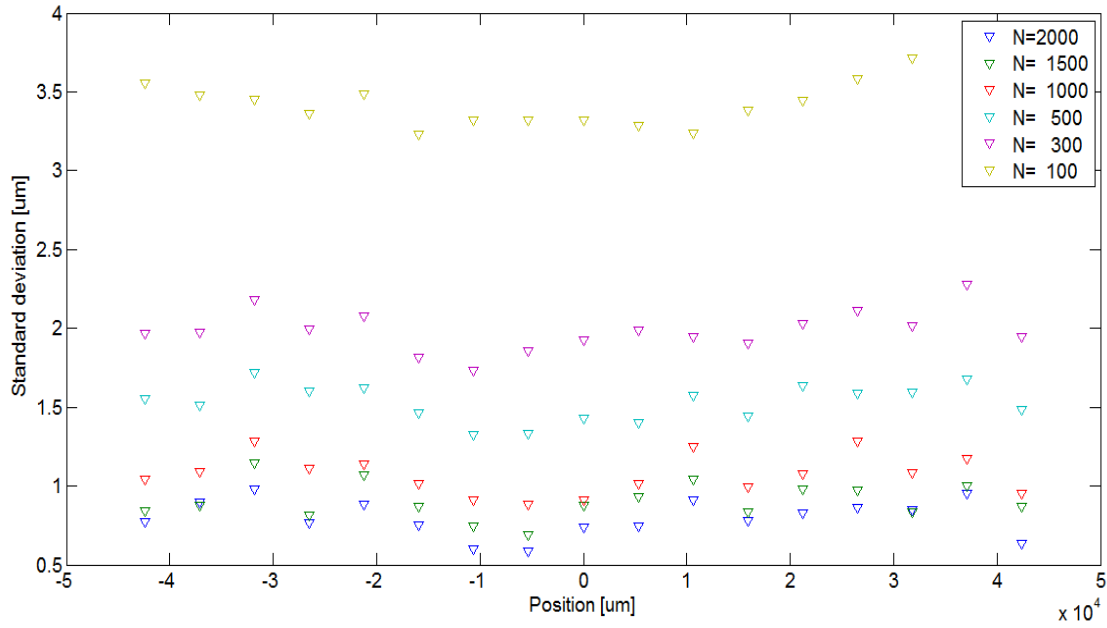


Figure 3. Standard deviation over 30 repetitions on different position with SNR=60dB

4.3 Evaluation of the minimum position step

The Sine Fit Algorithm implemented on the FPGA suffers of loss of precision mostly due to finite word length effect of the Fixed Point representation. It's mandatory to investigate the resolution of the algorithm implemented on the FPGA. The term resolution indicates the minimum step of the LVDT's core that can be measured by the actual system. The target has been fixed at 0.5 μm . Since no motor can move the LVDT's core with a resolution of 0.5 μm it was necessary to simulate this type of movement.

The simulations are carried out knowing that in the Null position the secondaries ideally have the same amplitude. It is then added to one secondary (and subtracted to the other one) a quantity that brings in floating point representation to a variation on the position of 0.5 μm . An additive Gaussian noise of 92 dB is added to the pure sine

waves. Then the wave is quantized to simulate an ideal ADC before feeding the algorithm.

The three algorithms developed have different resolutions. In the Low and Medium resolution the main issue is the variation of representation at the output of the MAC unit. It can be noticed from Figure 4 that in the Low resolution algorithm, the word length effect brings to a Null position. The results of Medium resolution algorithm are more satisfying because even if the positions evaluated do not follow the floating point results the difference between the two is less than $0.5\text{ }\mu\text{m}$ (Figure 5).

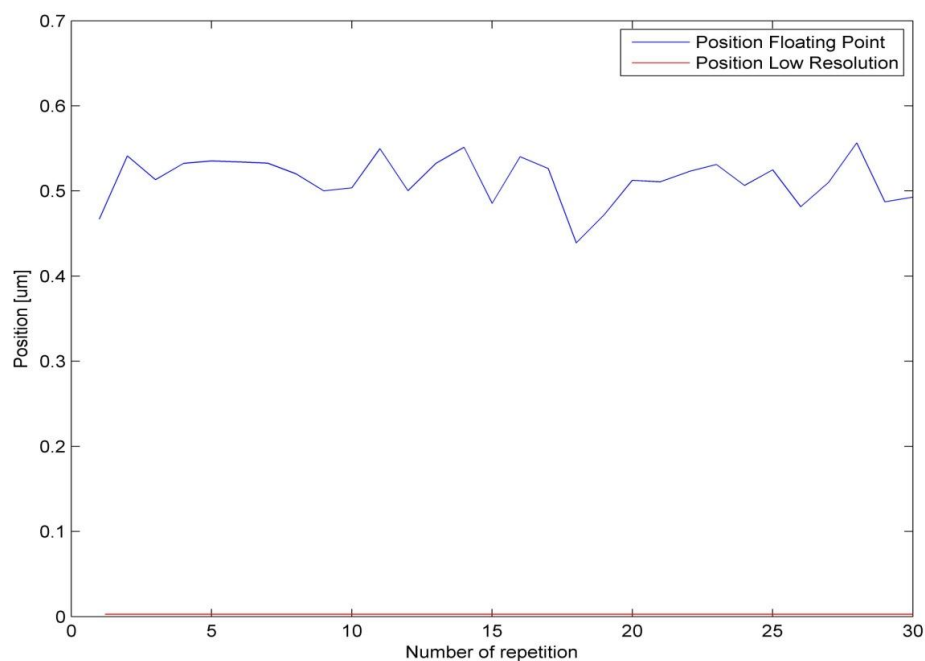


Figure 4. Low resolution word length effect on $0.5\text{ }\mu\text{m}$ of simulated step.

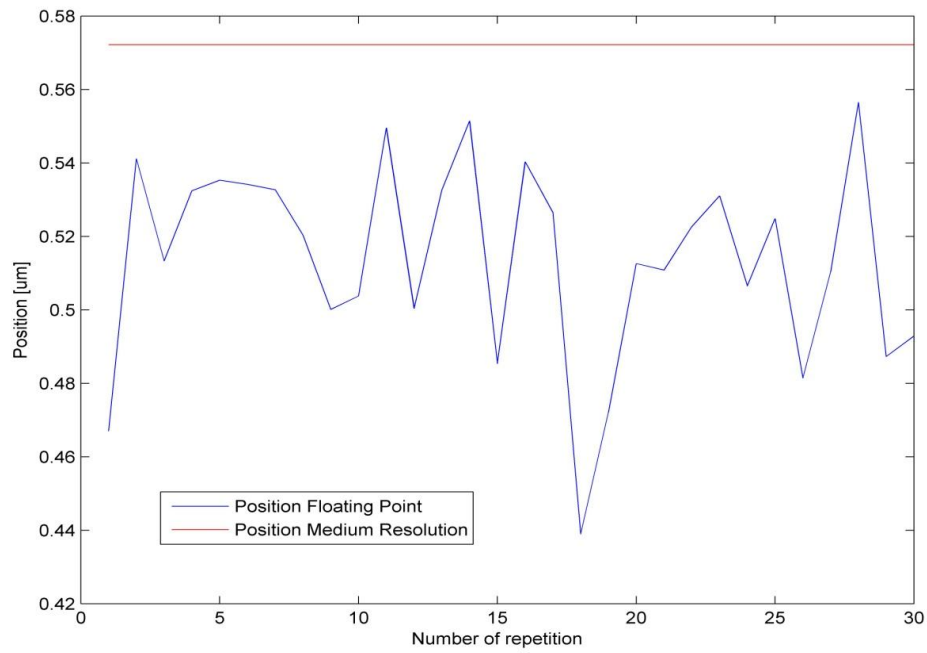


Figure 5. Medium resolution word length effect on 0.5 μm of simulated step.

The High resolution is the one which gives the best performance in terms of resolution because not only it follows the floating point results and the difference on positions is very low. The output of the High resolution algorithm is represented with both its full precision on 42 bits and reduced precision on 32 bit. The 42 bits wide results is very precise and led to a difference to less than $1e^{-6}$ μm. The results on 32 bit led to a greater difference of $1e^{-4}$ μm but still acceptable (Figure 6).

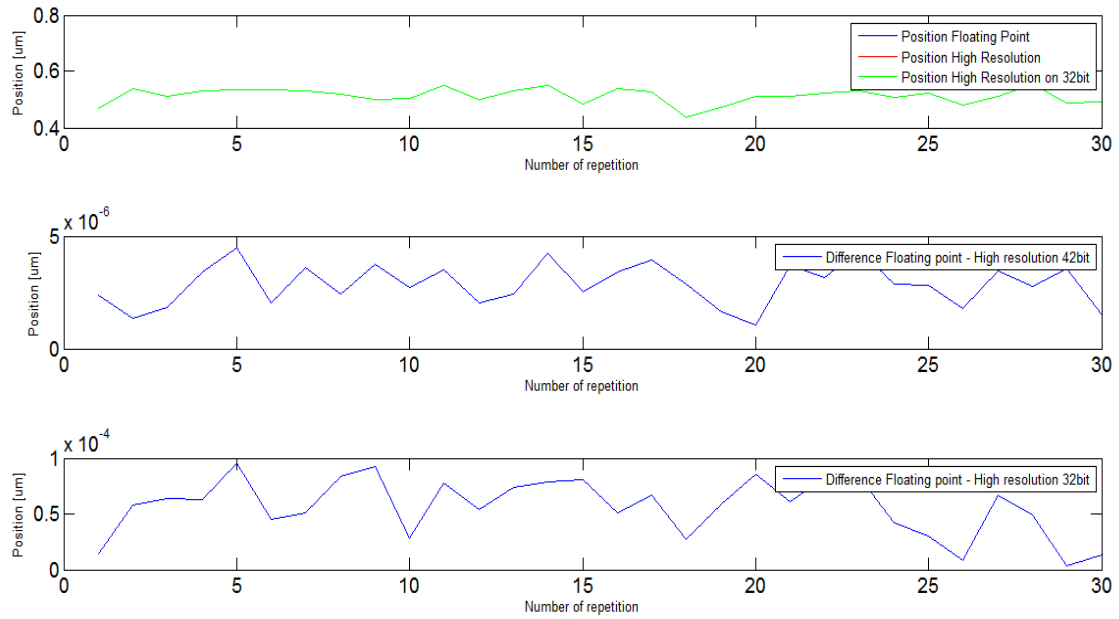


Figure 6. High resolution algorithm differences with floating point calculation.

Several measurements on the resolution have been carried out using real data acquire by the system actually in use on the collimators. The ADC raw data coming from the PXI DAQ board are stored and processed by the new developed Sine Fit algorithms. The value of the LVDT position evaluated by the floating point and the novel algorithms (fixed point representation) are compared. The minimum step that the stepper motor can do is 5 μm so we cannot actually measure a lower resolution. The measures are carried out doing 30 measurements in 4 different positions: at 9730 μm , 9715 μm , 9710 μm and at 9715 μm . In the last three measurements a step of 5 μm is evaluated. From Figure 7 to Figure 9 the results are shown for each algorithms. The differences on the measured position are very low confirming the simulations results.

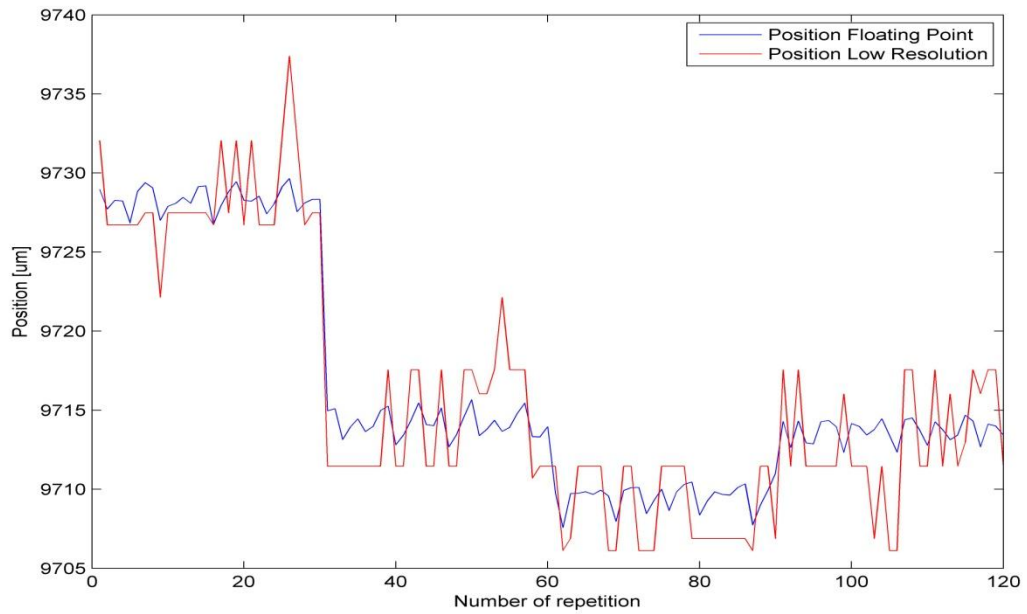


Figure 7. Low resolution word length effect on raw data from the ADC.

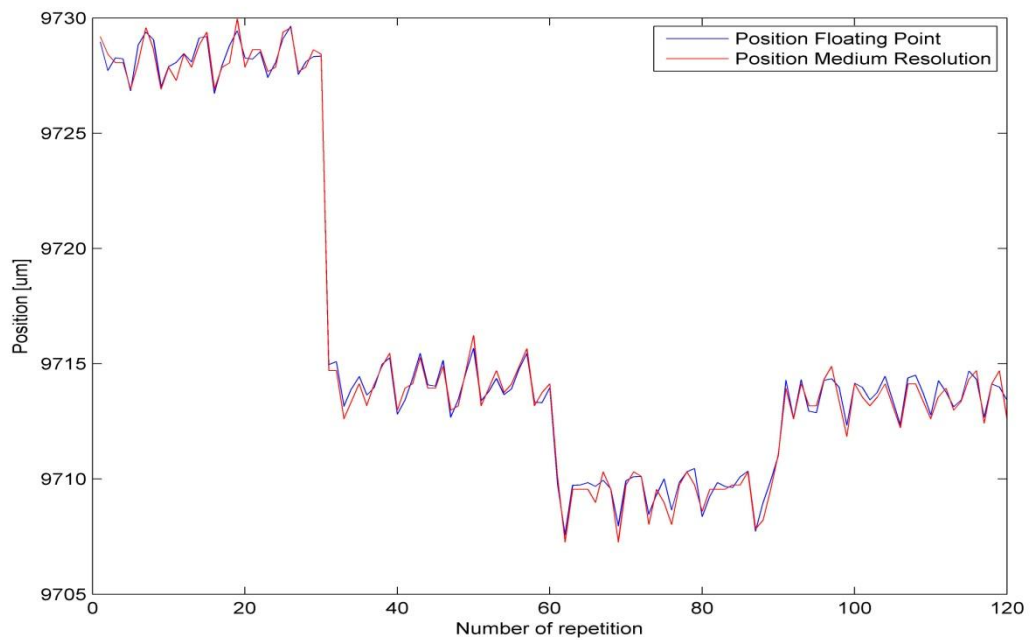


Figure 8. Medium resolution word length effect on raw data from the ADC.

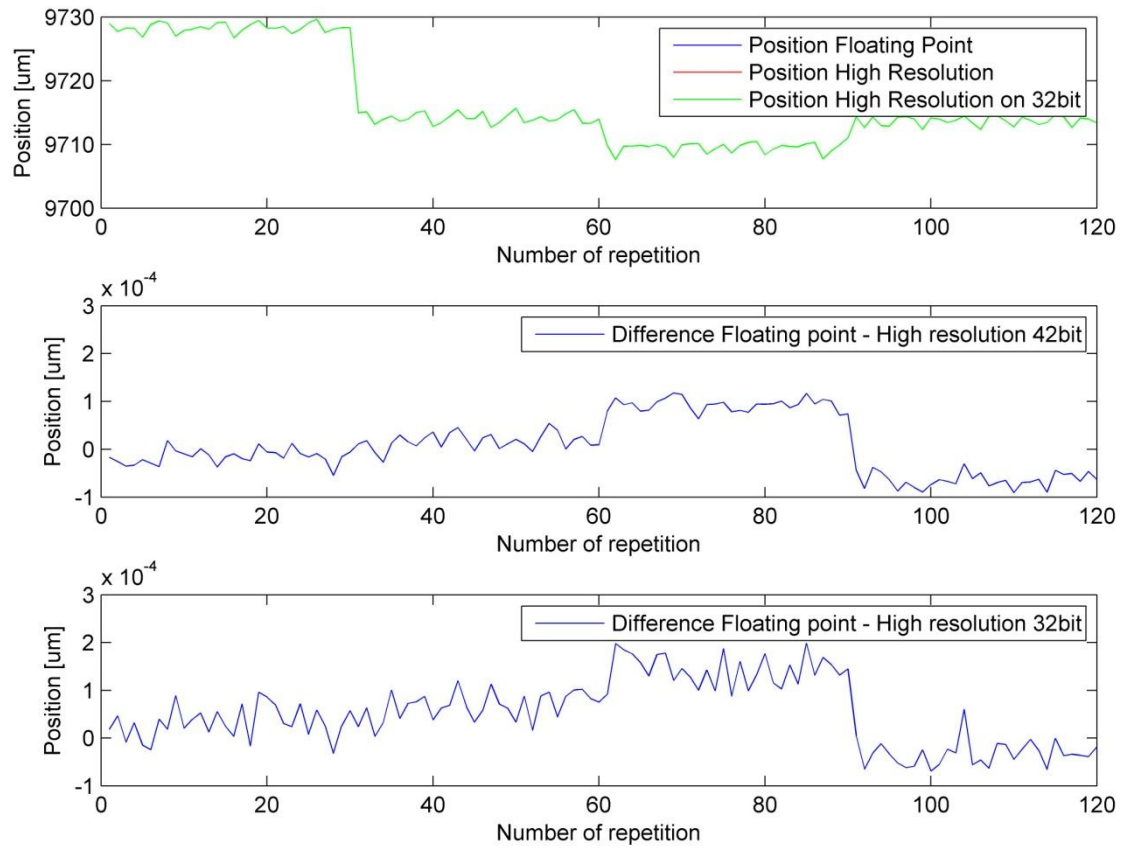


Figure 9. High resolution algorithm differences on raw data from the ADC.

To evaluate the goodness of each algorithm, the worst case difference on the position retrieved by the floating point algorithm and that one retrieved by the fixed point ones is calculated. In Table 3 these results are shown and it is possible to see that the maximum error committed by the Low resolution algorithm is very high (about 8 μm), while the behavior of the Medium resolution is still quite good. The High resolution algorithm show the best performance with an error less than 0,2 nm for both full precision (42 bits) and for 32 bits data length.

	Low Res Max error [μm]	Medium Res Max error [μm]	High Resolution with 42 bit Max error [μm]	High Resolution with 32 bit Max error [μm]
Position 9730μm	7,7499	0,7878	5,45E-05	9,57E-05
Position 9715μm	8,4810	0,5588	5,32E-05	1,20E-04
Position 9710μm	4,1310	1,0275	1,18E-04	1,99E-04
Position 9715μm	7,2870	0,8173	9,08E-05	6,94E-05
Total max error	8,4810	1,0275	1,18E-04	1,99E-04

Table 3. Maximum error committed on the evaluation of the position

4.4 Position Measurement Results

Other measurements were carried out on different positions to evaluate if the precision remain the same over the full LVDT range. The measurement were done by using the PXI DAQ board and retrieving the raw ADC samples. This is actually the best method to compare the results obtained with new algorithm and the ones retrieved with the PXI system. In such way we do not consider an eventual difference between the actual PXI ADC and the one used in our design (MAX11046).

The LVDTs work on ± 40 mm range and symmetrical positions are chosen for the measurements. On each position 30 measurements done and the mean and the standard deviation are evaluated. The list of positions and the results obtained are in Appendix. The table is grouped by position; for each position all the different algorithm implementations are compared to the floating point one. In Table 4 an example of measurement at -40 mm on the left (indicated with minus sign) is shown.

	Amp 1 [V]	Amp 2 [V]	Mean of ratiometric [mm]	Std [mm]	Difference on mean[um]	Max error against floating point [um]
double float	1,7983	4,2019	-40,05808	8,23E-04	-	-
single float	1,7983	4,2019	-40,05807	8,22E-04	-9,52E-03	9,28E-02
fixed 16 bit low res	1,7982	4,2019	-40,06101	3,10E-03	2,93	8,65
fixed 16 bit med res	1,7983	4,2019	-40,05816	1,11E-03	7,55E-02	2,32
High precision 42 bit	2,9614	6,9196	-40,05808	8,23E-04	2,35E-04	3,49E-04
High precision 32 bit	2,9614	6,9196	-40,05808	8,23E-04	3,25E-04	5,29E-04

Table 4. An example of measurement carried out over 40 mm range.

The difference on the amplitude value for high resolution is due to K factor (1.647) which does not influence the results. It is calculated the mean and the standard deviation for the 30 measurements on the same position. Then the difference with the mean of floating point algorithm is also calculated for every algorithm implementation. The value that can be used as a reference for the goodness of the algorithm is the maximum error committed over 30 measurements with respect to the double float. In Figure 10 all the measurement are plotted together and the differences between floating point value and High resolution implementation 32 bits results are plotted.

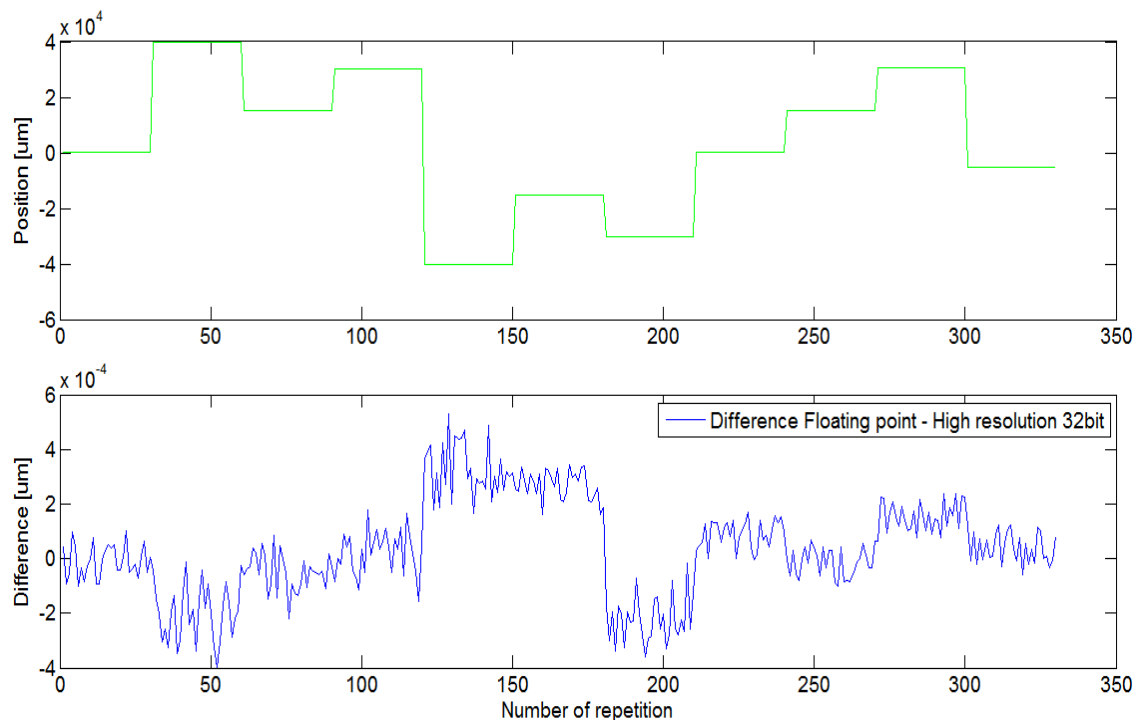


Figure 10. 30 measurements over the ± 40 mm range and the differences between floating point and the High resolution algorithm with 32 bit of output.

4.5 Radiation Test

4.5.1 FPGA Radiation effect

A preliminary test of radiation effects on FPGA ACTEL had already been done [29]. The test has been carried out in the facility at Paul Scherrer Institut (PSI) with a proton beam at 230 MeV. The devices were tested with a design on which is applied a register TMR. No SEU were observed on 3 devices up to a TID of 390 Gy and a fluence of 7.3×10^{11} particles/cm². The device is considered latch-up free up to $68 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ [30]. This demonstrates the goodness of radiation tolerant FPGA family ProAsic3 and its suitability for the LVDT conditioner board.

4.5.2 ADC Radiation Test

The ADC MAX11046 must be tested in radiation environment to see if it fits in the radiation constraints given in Chapter 2. The radiation test has been carried out with a proton beam at 230 MeV in the facility at Paul Scherrer Institut (PSI). In table the DUT and the initial DC value are described.

DUT type	16 channel ADC with 8 independent input channels and up to 250 kbps
DUT name	MAX 11046
Voltage reference initial	4.0973 V
Sampling rate	250 kbps
Connections	MicroCoax cable to FPGA development board.

Table 5. Device under test characteristic.

The irradiation has been carried out on 3 devices. The setup of the measurements is depicted in Figure 11. The internal reference circuit has been chosen , the digital supply voltage and the analog supply voltage are fed by an external power supply (Agilent E3648A). An over current protection is used to recognize latch-up events.

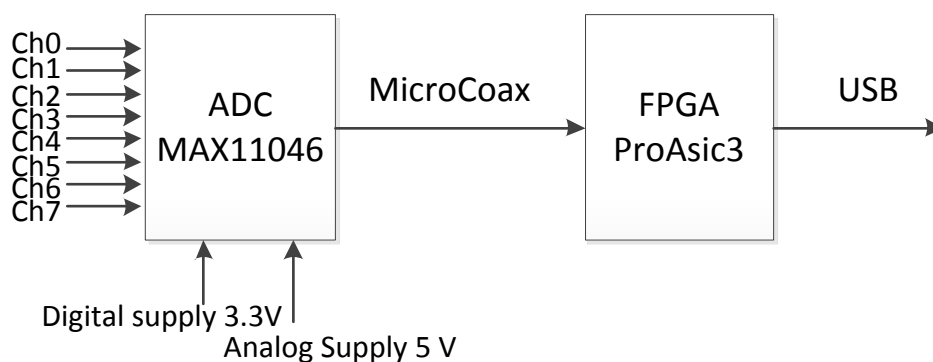


Figure 11. Block diagram of the setup for the radiation test.

The test is performed feeding the ADC with a DC input voltage. The measurements are divided in two parts, one is the calibration and the second the radiation test. In calibration measurements, the FPGA retrieve and store in its registers the maximum and the minimum value of the sampled input voltage for each channel. These values

are used in the second phase of the radiation test as thresholds of a dead band. If the ADC during the irradiation fall out the threshold values, a SEU happened. The ADC code and its number of occurrences are saved on the FPGA. The number of occurrences defines the Single Event Upset and ,therefore, the cross section of the DUT by knowing the total fluence.

The test is divided in beam Run; for each one the TID, the flux and the fluence given by the facility are reported (Table 6) .

Run	DUT	Flux pp/cm ² /s	Fluence pp/cm ²	Cumulative Fluence	dose rate (rad/s)	Cumulative TID [Gy]
29	MAX11046_1	1,00E+07	1,00E+10		0,55	
30	MAX11046_1	5,00E+07	2,00E+10		2,7	
31	MAX11046_1	1,00E+08	2,00E+10		5,7	
32	MAX11046_1	1,00E+08	1,00E+11		5,7	
33	MAX11046_1	1,00E+08	2,00E+11		5,7	
34	MAX11046_1	1,00E+08	4,50E+10		5,74	
				3,95E+11		208
36	MAX11046_2	1,54E+08	1,00E+11		8,3	
37	MAX11046_2	1,60E+08	1,46E+10		8,60E+00	
38	MAX11046_2	1,60E+08	3,30E+10		8,60E+00	
39	MAX11046_2	1,60E+08	1,00E+11		8,60E+00	
40	MAX11046_2	1,60E+08	1,00E+11		8,60E+00	
41	MAX11046_2	1,60E+08	1,00E+10		8,60E+00	
43	MAX11046_2	1,60E+08	2,00E+09		8,60E+00	
46	MAX11046_2	1,60E+08	3,60E+10		8,60E+00	
				3,96E+11		210
47	MAX11046_3	1,55E+08	7,10E+10		8,30E+00	
48	MAX11046_3	1,55E+08	7,70E+10		8,30E+00	
49	MAX11046_3	1,55E+08	1,50E+10		8,30E+00	
50	MAX11046_3	1,55E+08	1,00E+11		8,30E+00	
51	MAX11046	1,55E+08	1,00E+11		8,30E+00	
53	MAX11046	1,55E+08	4E+10		8,30E+00	
				4,03E+11		214

Table 6. Summary of the TID, flux and the fluence given by the facility for the three ADC

In Figure 12 the SEU counts for the channel 6 are reported on Z axis. On the Y axis the different run number and the input voltage applied in calibration phase are reported. The code affected by SEU is reported on the axis X.

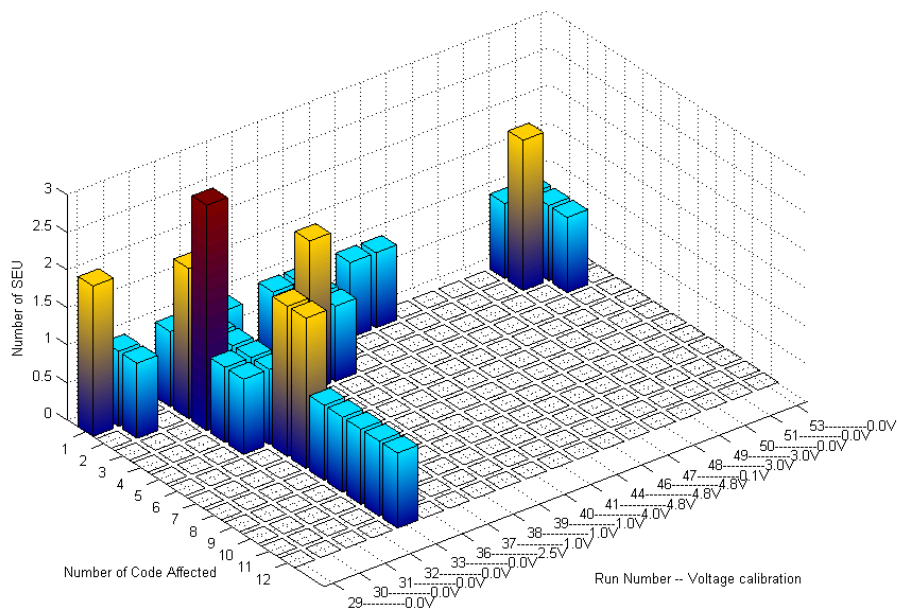


Figure 12. SEU count for channel 6 for different Run.

The Figure 12 gives an indication of how many value are out of bound but does not indicate how far from the threshold value they are. In Table 7 for each channel the maximum distance in mV from the threshold value is indicated for each channel. It is also indicated the calibration value and the range of the dead band between the maximum and the minimum threshold.

	MAX11046_1 Run 29-34			MAX11046_2 Run 36-46			MAX11046_3 Run 47-53		
DUT	Max Distance [mV]	Calibr. value [V]	Calibr. Range [mV]	Max Distance [mV]	Calibr. value [V]	Calibr. Range [mV]	Max Distance [mV]	Calibr. value [V]	Calibr. Range [mV]
Ch 0	1,83	1,00	1,83	17,24	0,17	178,77	1,5258	3,30	3,66
Ch 1	10,99	1,00	1,83	3,05	0,00	0,69	3,05	3,31	3,66
Ch 2	2,29	1,00	1,83	0,92	0,00	0,69	0,92	4,81	4,28
Ch 3	0,46	1,00	1,83	4,58	0,00	0,61	6,41	3,31	3,66
Ch 4	4999,39	0,00	0,69	1,53	-1,00	1,07	4,27	0,00	0,84
Ch 5	2,59	0,00	0,69	9,61	-1,00	1,22	3,36	0,00	0,54
Ch 6	1,83	0,00	0,69	1,37	-1,00	0,91	3,97	0,00	0,84
Ch 7	1,37	0,00	0,69	1,53	-4,00	4,27	2,44	3,00	3,35

Table 7. Maximum distance of SEU count from the threshold value.

From the Table 7 it is possible to notice that the values out of bounds are close to the calibration range. This could lead to think that the values out of range are mostly due to a variation of other parameter such as the voltage reference. The Channel 4 of the MAX11046_1 was blocked on the maximum on run 34 because of the device's failure. The voltage reference and the current consumption from power supply have been monitored during the irradiation. In Figure 13 the Voltage reference drift for the MAX11046_1 is reported. The voltage reference shows a drift of a few mV over 200 Gy. The typical plots of the analog power supply and the digital power supply (Figure 14 and Figure 15) indicate that at the end of the ADC's life the current consumption on analog power supply starts to increase of about 5 mA. In Table 8 the voltage reference drift, the analog supply current drift and the digital supply current drift are reported for each ADC tested.

	Voltage drift [mV]	Analog supply current drift [mA]	Digital supply current drift [mA]
MAX11046_1	1,9	-4,5	-1,3
MAX11046_2	3,2	-5,5	0,1
MAX11046_3	1,7	-6,2	-2,8

Table 8. Drift value of the voltage reference, analog supply and digital supply current.

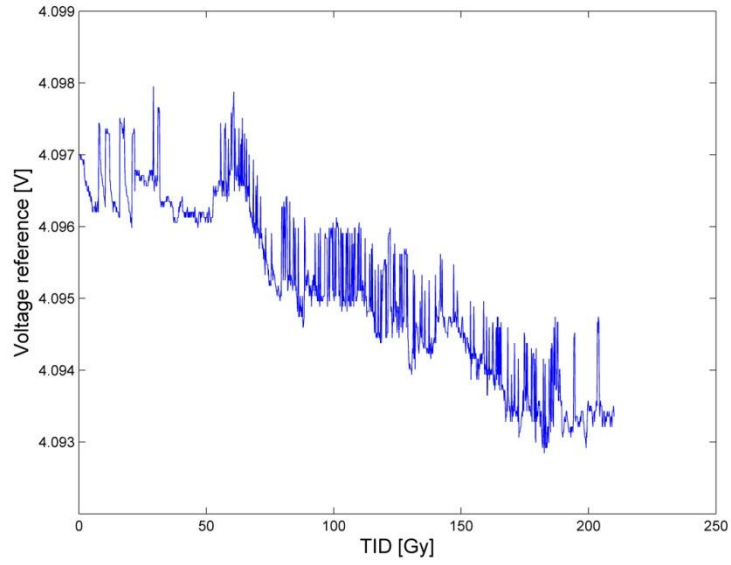


Figure 13. Voltage reference Drift against the TID.

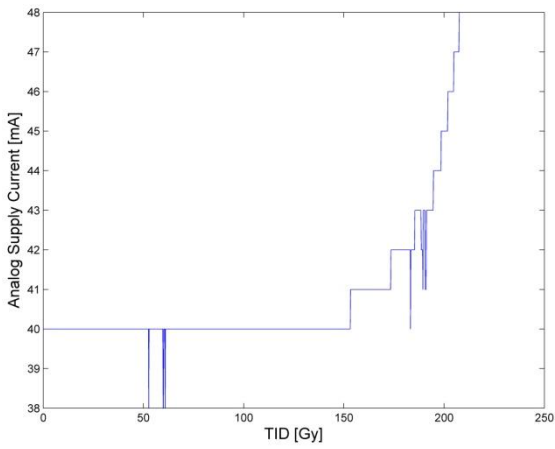


Figure 14. Analog supply current.

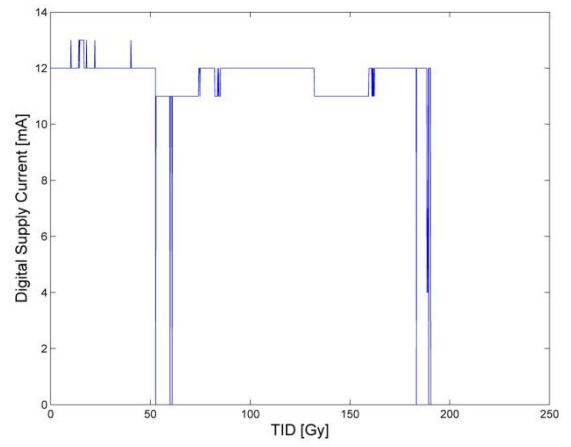


Figure 15. Digital supply current.

The most important value in this test is the cross section of the device defined as:

$$\sigma = \frac{N}{\Phi} \text{ cm}^2$$

The cross section has been calculated for every channel for every ADC tested. To increase the statistic, the cumulative cross section including the three devices has been calculated (Table 9).

Channel	σ [cm ²] MAX11046_1 Run 29-34	σ [cm ²] MAX11046_2 Run 36-46	σ [cm ²] MAX11046_3 Run 47-53	SEU Count
Ch 0	1,52E-11	6,06E-11	1,65E-11	36
Ch 1	1,27E-11	4,04E-11	2,75E-11	31
Ch 2	1,27E-11	2,53E-11	6,06E-11	37
Ch 3	2,53E-12	2,78E-11	6,89E-11	37
Ch 4	3,04E-11	2,27E-11	1,93E-11	28
Ch 5	4,05E-11	3,54E-11	2,20E-11	31
Ch 6	3,04E-11	2,27E-11	1,65E-11	27
Ch 7	1,01E-11	4,80E-11	4,13E-11	38
Cumulative	2,30E-10			265

Table 9. Cross section for each channel and cumulative cross section.

Taking the cumulative cross section as reference it is possible to evaluate The cross section per channel that result to be 9.5×10^{-12} cm². If one considers the cross section per device the cross section is 7.6×10^{-11} cm². Now is possible to calculate how many SEU per channel and per ADC are probable for a fluence of 10^{11} cm², which is fixed as a target. The results are shown in Table 10.

Estimated SEU per channel per year	0.95
Estimated SEU per ADC per year	7.6

Table 10. Estimated SEU per year.

The estimated SEU per year are very low and could be tolerated. Moreover no SEL are evident. Hence the ADC could be used on final LVDT readout module.

CONCLUSIONS AND OUTLOOKS

This thesis has been carried out at CERN in the Engineering department in the Equipment Controls and Electronics section part of the Source Target and Interaction group.

A proof demonstrator of a radiation tolerant LVDT signal conditioner has been conceived and developed. The requirements on the uncertainty of the LVDT conditioner were fixed on the basis of the performance of the LHC collimator system. The challenge was to assure those figures in a radiation environment characterized by a Total Ionizing Dose of 100 Gy, a High Energy Hadron (HEH) fluence of 10^{11} cm^{-2} , a 1 MeV equivalent neutron fluence of $3 \times 10^{11} \text{ cm}^{-2}$. In fact the conditioner is conceived to be used for the applications where the electronics cannot be protected against radiations.

The main parts of the proof demonstrator are the ADC for sampling the input sine waves of the LVDT secondary coils and the FPGA for evaluating the sensor position. The FPGA is the ACTEL ProAsic3, a commercial device that proved to be immune to Single Event Latch-up up to a LET of $68 \text{ MeV cm}^2/\text{mg}$ [30]. Preliminary tests showed that no SEU were observed up to a fluence of $6 \times 10^{11} \text{ cm}^{-2}$ of 230 MeV proton by using the TMR technique [29]. The FPGA shows failures at high TID of about 300 Gy. Those results are very promising and make the ACTEL a candidate for the LVDT conditioner.

The ADC is the 8 simultaneous channel MAX11046, 250 kSps, $\pm 10 \text{ V}$. It was tested with a 230 MeV proton beam. 3 devices were tested up to $4 \times 10^{11} \text{ cm}^{-2}$ and no latch-up event was registered at room temperature. The cross section of the soft single event was evaluated and resulted to be $9 \times 10^{-12} \text{ cm}^2$ per device per channel. If one considers the cross section per device the cross section is $7 \times 10^{-11} \text{ cm}^2$. That result shows that the expected number of SEU per device for the target fluence of 10^{11} cm^{-2} would be 8 which is an acceptable result. In fact, one has to consider that the target fluence can be reached over one year and the effective impact on the retrieved position of an SEU on the ADC is to be quantified. The voltage reference showed a low drift as a function of the TID and the failure of the device appeared at 210 Gy.

The use of the FPGA to retrieve the sensor position posed the challenge to reach an acceptable numerical position by using the fixed point representation. In fact, double

point representation would impose a huge overhead. The target for the numerical resolution was chosen on the basis of the real LHC collimation system and was fixed at 0.5 μm . Three types of numerical algorithm were evaluated. The data are treated on-line. The structure is based on a MAC (Multiply and Accumulate), a module to evaluate the square root and one for the final ratio operation. The last two operations are the most demanding in terms of precisions.

The algorithms had to be designed in HDL to reach an efficiency such that the implementation results feasible. The solutions were evaluated in simulation by emulating the secondary coil signals by sine waves with an additive Gaussian noise. A simulation plan was planned to study the effect on the numerical resolution of (i) the SNR and of (ii) the number of samples of the input sine waves. Then, the results were confirmed by using real data of an LVDT.

Only one algorithm proved to be efficient to assure the required numerical resolution. The implementation is based on the CORDIC algorithm which was exploited for the vector magnitude calculation and for the division. This is a new solution never implemented before which satisfy the imposed target. Moreover, the smart implementation of that algorithm allows reducing the area occupancy and, hence, one FPGA can be exploited to treat the data of multiple LVDT in parallel.

Therefore, the proof demonstrator successfully proved that a fixed point algorithm can be used to retrieve the sensor position of an LVDT with a numerical resolution of 0.5 μm . The ADC features are such to assure an uncertainty of the reading system within few μm as required. Further radiation tests will be carried out in a dedicated CERN radiation facility to prove the immunity to SEL in a *LHC like* environment of the devices. The impact of SEU of the ADC codes on the retrieved position remains to be evaluated. The Sine Fit algorithm could allow reducing the number of SEU that effectively corrupt the final reading. Finally, various DAC references are currently under investigation and will be tested under radiation to check their hardness up to the above specified limits.

Appendix

All the result for the measurements on the range ± 40 mm.

	Amp 1 [V]	Amp 2 [V]	Mean of ratiometric [mm]	Std [mm]	Difference on mean[um]	Max error against floating point [um]
double float	2,9995	2,9989	0,01059	6,49E-01	0,00E+00	0,0000E+00
single float	2,9995	2,9989	0,01059	6,53E-01	7,21E-03	8,2622E-02
fixed 16 bit low res	2,9995	2,9987	0,01277	2,71E+00	-2,17E+00	5,7938E+00
fixed 16 bit med res	2,9995	2,9988	0,01059	9,94E-01	7,60E-03	1,4101E+00
High precision 42 bit	4,9394	4,9383	0,01059	6,49E-01	-9,41E-05	1,3517E-04
High precision 32 bit	4,9394	4,9383	0,01059	6,49E-01	-9,07E-06	1,0282E-04
double float	4,1977	1,7997	39,98330	9,81E-01	0,00E+00	0,0000E+00
single float	4,1977	1,7997	39,98330	9,79E-01	2,57E-03	5,7600E-02
fixed 16 bit low res	4,1977	1,7997	39,98281	3,60E+00	4,96E-01	7,5738E+00
fixed 16 bit med res	4,1976	1,7997	39,98306	1,07E+00	2,42E-01	1,8933E+00
High precision 42 bit	6,9125	2,9637	39,98330	9,81E-01	-2,99E-04	4,8495E-04
High precision 32 bit	6,9125	2,9637	39,98330	9,81E-01	-2,00E-04	3,9893E-04
double float	3,4530	2,5516	15,01024	5,37E-01	0,00E+00	0,0000E+00
single float	3,4530	2,5516	15,01026	5,43E-01	-1,84E-02	1,1476E-01
fixed 16 bit low res	3,4528	2,5517	15,00814	2,08E+00	2,10E+00	7,1541E+00
fixed 16 bit med res	3,4529	2,5516	15,01022	8,52E-01	1,63E-02	1,6210E+00
High precision 42 bit	5,6861	4,2019	15,01024	5,37E-01	-1,56E-04	2,4039E-04
High precision 32 bit	5,6861	4,2019	15,01024	5,37E-01	-4,99E-05	2,2165E-04
double float	3,9125	2,0886	30,39242	8,82E-01	0,00E+00	0,0000E+00
single float	3,9125	2,0886	30,39241	8,74E-01	4,53E-03	7,2315E-02
fixed 16 bit low res	3,9125	2,0886	30,39190	2,09E+00	5,22E-01	3,3787E+00
fixed 16 bit med res	3,9124	2,0886	30,39234	1,22E+00	8,29E-02	1,5726E+00
High precision 42 bit	6,4428	3,4394	30,39242	8,82E-01	-7,08E-05	1,6585E-04
High precision 32 bit	6,4428	3,4394	30,39242	8,82E-01	2,33E-05	1,7970E-04
double float	1,7984	4,2020	-40,05808	8,23E-01	0,00E+00	0,0000E+00
single float	1,7984	4,2020	-40,05807	8,22E-01	-9,52E-03	9,2792E-02
fixed 16 bit low res	1,7982	4,2020	-40,06101	3,10E+00	2,93E+00	8,6473E+00

fixed 16 bit med res	1,7984	4,2020	-40,05816	1,11E+00	7,55E-02	2,3162E+00
High precision 42 bit	2,9615	6,9196	-40,05808	8,23E-01	2,35E-04	3,4914E-04
High precision 32 bit	2,9615	6,9196	-40,05808	8,23E-01	3,25E-04	5,2940E-04
double float	2,5463	3,4538	-15,12437	8,18E-01	0,00E+00	0,0000E+00
single float	2,5463	3,4538	-15,12438	8,18E-01	2,00E-03	1,1487E-01
fixed 16 bit low res	2,5462	3,4537	-15,12520	3,31E+00	8,25E-01	6,5733E+00
fixed 16 bit med res	2,5463	3,4537	-15,12437	1,21E+00	-7,95E-03	1,8108E+00
High precision 42 bit	4,1931	5,6874	-15,12437	8,18E-01	1,70E-04	2,2269E-04
High precision 32 bit	4,1931	5,6874	-15,12437	8,18E-01	2,68E-04	3,4404E-04
double float	2,0971	3,9012	-30,07677	1,02E+00	0,00E+00	0,0000E+00
single float	2,0971	3,9012	-30,07675	1,02E+00	-1,30E-02	6,7427E-02
fixed 16 bit low res	2,0970	3,9012	-30,07815	3,21E+00	1,38E+00	7,9105E+00
fixed 16 bit med res	2,0971	3,9012	-30,07701	1,41E+00	2,40E-01	1,3305E+00
High precision 42 bit	3,4534	6,4243	-30,07677	1,02E+00	-3,28E-04	4,6258E-04
High precision 32 bit	3,4534	6,4243	-30,07677	1,02E+00	-2,24E-04	3,6016E-04
double float	2,9508	2,9508	0,00055	1,13E-01	0,00E+00	0,0000E+00
single float	2,9508	2,9508	0,00059	1,18E-01	-3,91E-02	1,3249E-01
fixed 16 bit low res	2,9507	2,9507	0,00041	2,33E+00	1,40E-01	5,7207E+00
fixed 16 bit med res	2,9508	2,9507	0,00065	6,68E-01	-1,08E-01	1,6649E+00
High precision 42 bit	4,8592	4,8591	0,00055	1,13E-01	-1,17E-05	1,6743E-05
High precision 32 bit	4,8592	4,8591	0,00055	1,13E-01	9,00E-05	1,6782E-04
double float	3,4011	2,4975	15,31904	9,83E-02	0,00E+00	0,0000E+00
single float	3,4011	2,4975	15,31902	9,72E-02	1,76E-02	9,9637E-02
fixed 16 bit low res	3,4011	2,4975	15,31926	3,53E+00	-2,28E-01	5,5095E+00
fixed 16 bit med res	3,4011	2,4975	15,31898	7,44E-01	5,17E-02	1,6034E+00
High precision 42 bit	5,6008	4,1128	15,31904	9,83E-02	-1,05E-04	1,1151E-04
High precision 32 bit	5,6008	4,1128	15,31904	9,83E-02	-1,36E-05	1,0129E-04
double float	3,8536	2,0424	30,71986	1,45E-01	0,00E+00	0,0000E+00
single float	3,8536	2,0424	30,71987	1,46E-01	-9,82E-03	1,0861E-01
fixed 16 bit low res	3,8537	2,0423	30,72055	3,41E+00	-6,89E-01	6,0742E+00
fixed 16 bit med res	3,8536	2,0424	30,71966	8,73E-01	1,94E-01	1,5017E+00
High precision 42 bit	6,3459	3,3633	30,71986	1,45E-01	5,47E-05	6,1730E-05
High precision 32 bit	6,3459	3,3633	30,71986	1,45E-01	1,55E-04	2,3649E-04

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